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AMORPHOUS SILICON/LANGMUIR-BLODGETT FILM MIS DEVICES

by

J. P. LLOYD, B.Sc.

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A Thesis submitted for the
Degree of Doctor of Philosophy
in the University of Durham

March, 1984

30. JUL 1984

Thesis
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DECLARATION

I hereby declare that the work reported in this thesis has not previously been submitted for any degree, and is not being currently submitted in candidature for any other degree.

Signed J. P. Lloyd

The work reported in this thesis was carried out by the candidate

Signed Gareth Roberts

M C Petty

Directors of Studies

J. P. Lloyd

Candidate

ABSTRACT

Metal-insulator-semiconductor (MIS) structures based on glow discharge produced, hydrogenated amorphous silicon (α-Si:H), and incorporating Langmuir-Blodgett (LB) film insulating layers, have been investigated. Two distinct types of MIS diode have been considered : tunnelling diodes (insulator thickness <5 nm) and non-tunnelling diodes (insulator thickness > 10 nm). A preliminary study of insulated-gate field-effect-transistors (igfet's) has also been undertaken.

Simple Schottky barrier (MS) structures, which are effectively a first step towards tunnelling MIS devices, have been made and characterised : results showed that these were 'state-of-the-art' devices. A preparation procedure has been developed which facilitates the successful deposition of LB film materials onto α-Si:H. Tunnelling MIS diodes containing diacetylene polymer LB insulating films have been fabricated, and capacitance measurements showed that the films were of reasonable quality. The current-voltage characteristics of these diodes were rather non-ideal and, it is thought, were dominated by the effects of two distinct levels of surface states. The appearance of peaks in the illuminated conductance-voltage curves supports this interpretation. Solar cells with an MIS structure can show an enhanced efficiency compared with MS (Schottky) cells. By using varying numbers of LB monolayers, the effects of increasing insulator thickness on α-Si:H solar cell parameters have been ascertained. Though the results closely parallel those of other researchers, the presence of a surface 'oxide' layer of ∿ 4 nm thickness (as a result of the pre-LB film deposition etch) prevented optimisation of the cell efficiency. Further work is necessary in order to capitalise on the effect which has been demonstrated e.g. the development of a more suitable etch treatment, the use of different LB film materials.

Non-tunnelling MIS diodes were made using cadmium stearate/stearic acid LB films. The capacitance-voltage curves were very similar to those which have been reported for conventional MIS devices on single crystal semiconductors. The LB films, although of slightly poorer structural quality than is possible on single crystal substrates, were nonetheless reproducible. An unusual $\ln J$ v $V^{\frac{1}{2}}$ current-voltage dependence was found, which, it is suggested, was due to image-force effects. Large hysteresis was observed in the device characteristics due to polarisation or ionic motion. The characteristics were also influenced by the presence, in the upper half of the α-Si:H mobility gap, of a band of surface or bulk states. These simple structures could possibly be used as gas detectors, since the penetration of a gas into the LB film may well result in measureable changes in the device parameters.

For the first time, an igfet based upon the α-Si:H/LB film system has been produced. The device showed a change in source-drain current of almost three orders of magnitude for a gate voltage change of 10V. This compares well with the early results of other workers using more conventional insulators. It is thought that the device performance was limited by the poor semiconducting properties of the surface region of the α-Si:H, and that an alternative FET configuration would lead to improvements. Possible applications include the switching of large area liquid crystal displays (using FET arrays) or, more tentatively, the exploitation of the 'molecular tailoring' qualities of LB films to produce specific biological and chemical FET sensors.

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CHAPTER 1

INTRODUCTION

The development and application of new materials often leads to scientific progress and social change. This can be seen quite clearly in the rapid rise of single crystal silicon technology to its present highly advanced state, and the consequent changes in society brought about by the increasing use of semiconductor devices in computers, T.V's etc. Other single crystal semiconductors e.g. InP, GaAs are currently being investigated in the search for faster devices and improved performance. In certain applications however, rather different factors must be considered, for example, the ability to make thin semiconducting films over large areas, or the need for a very cheap device. To some extent these considerations may be more important than the speed of operation or the performance, and a trade-off must be made. These different criteria call for the use of different materials and indeed, there is one group of materials, namely the non-crystalline semiconductors, whose properties may be well suited to such needs.

Although amorphous and glassy semiconductors have been studied for some time, it is only in the last twenty years that their potential impact on the electronics world has become apparent. In particular the discovery that amorphous silicon (α-Si:H) produced by the glow discharge technique could be doped n- or p-type has generated enormous interest. This material may be deposited in thin film form, on a variety of substrates and over large areas. Coupled with its excellent photoconductivity and high absorption coefficient for visible light, these properties mean that solar cells based on α-Si:H could become a viable, low cost, alternative to single crystal Si cells. The semiconducting properties of α-Si:H, though poorer than those of single crystal Si, are outstanding for a disordered material and, open up other

applications such as thin film integrated electronic devices, transistors, optoelectronic imaging sensors and xeroxography. In short, α-Si:H has become almost the prototype amorphous semiconductor.

The Langmuir-Blodgett (LB) technique is another recently developed technology, although its origins can be traced back 200 years. LB films are produced from compressed organic monolayers by repeatedly passing the substrate through the monolayer (usually on a water surface) and building up a multilayer structure. The deposition method is a low temperature process and films of accurately defined thickness can be put down over large areas. A variety of different molecules may be used, enabling one to alter the thickness of each individual monolayer and the overall properties of the film. Research is being conducted into the exploitation of LB films on single crystal semiconductors where they usually form the insulating layer in some sort of MIS device. It is noticeable, however, that the large area and thin film capability of the Langmuir-Blodgett technique matches quite closely some of the advantageous characteristics of α-Si:H. Therefore it was considered that an investigation of MIS devices based on α-Si:H and incorporating LB films could be both very interesting and fruitful.

This thesis deals basically with two types of device: tunnelling MIS devices, and those with a non-tunnellable insulator. The former type may be used in solar cell applications. In this context the LB technique provides a unique method of studying the effects of insulator thickness in a controllable way using built-up multilayers. The study of non-tunnellable MIS structures leads the way to the production of an α-Si:H FET. One reason for the interest in such FET's is that they could be used for the direct switching of liquid crystal elements in large area displays. Once again the properties of LB films would appear to match the requirements very well. The structure of the thesis is as follows. Since α-Si:H is a relatively new material, chapter 2 is devoted to a broad review of its production, properties

and applications. Chapters 3 and 4 cover the basic theory of Schottky barrier and tunnelling MIS devices, and of non-tunnelling (thick insulator) MIS structures. LB film technology is introduced in chapter 5, which includes the historical background, experimental procedures, a summary of the electrical properties of the films and an outline of possible applications. In chapter 6 the various experimental arrangements used during the course of this study are described and the techniques of device fabrication are listed. Also included are the results of some important, preliminary experiments carried out at various stages in the fabrication procedure. Chapters 7, 8 and 9 contain the bulk of the experimental data. The first of these deals with the characterisation of Schottky barrier diodes on α-Si:H. These diodes form an effective 'first step' towards the tunnelling MIS devices which are discussed in chapter 8, and help to establish a standard by which the MIS devices can be judged. In chapter 8, detailed measurements on these novel tunnelling LB film/α-Si:H structures are reported and their solar cell properties are investigated. Chapter 9 is concerned with the non-tunnelling devices. A series of experiments is described which has led to the fabrication of the first α-Si:H/LB film FET. The closing chapter of the thesis summarises the conclusions and gives suggestions for further work.

CHAPTER 2

INTRODUCTION TO AMORPHOUS SILICON

2.1 Introduction

In a crystalline semiconductor the electron wavefunctions may be defined using Bloch functions which incorporate the periodicity of the lattice. The energy bands are clearly defined using the relations between energy and wavevector (E-k relations). In an amorphous semiconductor this periodicity is absent : k, the electron wavevector is no longer a good quantum number and Bloch's theorem is rendered invalid. However, solutions to the Schrodinger equation must still exist and hence the concept of a density of states is still valid[1]. Photoemission studies on crystalline materials have shown that the conduction and valence band densities of states are determined largely by the short range order i.e. the local bonding arrangements. Since short range order is preserved in amorphous materials the gross features of their electronic structure should be similar to that of their crystalline counterpart. The main differences occur at the band-edges, where, instead of a sharp 'cut-off' of states, the distribution tails into the forbidden gap. Two different types of state are known to exist. States which are well within the bands are extended in nature i.e. the wavefunctions extend throughout the whole semiconductor (although they are not Bloch functions). Nearer the band-edges, as the density of states reduces (i.e. in the 'tail' region), the states become localised i.e. each wavefunction has a large amplitude at a particular point which decays approximately exponentially with distance. The mobility of the carriers in these states is very low (since conduction must take place by a hopping mechanism) and vanishes completely at absolute zero. The transition from extended to localised states is an abrupt one, occurring at a definite energy which is known as the mobility edge because of the sudden change in carrier mobility.

Another cause of states in the gap of amorphous semiconductors is the presence of structural defects. It is thought that a defect-free amorphous semiconductor, i.e. one in which all bonds are satisfied and in which there are no inhomogeneities, has an electronic structure which exhibits limited band tailing such that there is a range of energies with a zero density of allowed energy levels (a 'pseudo-bandgap'). Real amorphous materials often contain very high defect densities e.g. vacancies, voids, impurities, dangling bonds etc. which lead to a finite density of states throughout the forbidden gap. If the density of states is large enough the Fermi level may become 'pinned' i.e. the position of the Fermi level is fixed relative to the conduction and valence bands, and is insensitive to substitutional doping or to the injection of excess carriers.

This chapter is concerned with hydrogenated amorphous silicon (α-Si:H) which is a rather unusual amorphous (α)-semiconductor. In general, most α-semiconductors may be assigned to one of two classes on the basis of their observed properties. Glassy α-semiconductors are commonly prepared by quenching molten material, although they can be deposited from the vapour phase. They are typified by the chalcogenides which are compounds containing a large proportion of one or more group VI elements. These wide bandgap (∿2eV) semiconductors display an activated conductivity with an activation energy equal to roughly half the optical bandgap. Their absorption varies according to the spectral Urbach rule i.e. the logarithm of the absorption coefficient is proportional to the photon energy. ESR measurements show a very low density of unpaired spins and it is very difficult to change the conductivity of chalcogenides by doping. Non-glassy α-semiconductors cannot be prepared from the melt. They are made in thin-film form by vacuum evaporation, sputtering, glow discharge decomposition of a gas or electrolytic deposition[1]. This

group is best represented by pure, evaporated α-Si or α-Ge. These have a tetrahedral 'diamond' structure locally and esr measurements detect a high density of unpaired spins. Their conductivity follows the Mott variable-range hopping law ($\ln \sigma \propto T^{-\frac{1}{4}}$) rather than the classical activation energy equation ($\sigma = \sigma_o \exp(-E/kT)$). These films are also insensitive to substitutional doping.

Films of hydrogenated α-Si and α-Ge produced by the glow discharge technique or by reactive sputtering in hydrogen are notable exceptions to the above classification, having markedly different properties from the other non-glassy semiconductors. For instance, α-Si:H displays a quite well defined optical absorption edge at ∿ 1.7eV. ESR measurements record a low density of unpaired spins and the conductivity at room temperature is observed to be activated rather than following a hopping law. In short, although α-Si:H is a non-glassy semiconductor, its behaviour is remeniscent of a chalcogenide. There is however one important difference : α-Si:H can be substitutionally doped to change its conductivity. Both p-type and n-type samples can be produced and the conductivity can be varied over a range of ten orders of magnitude. This unique (for an α-semiconductor) controllability of conductivity by doping, together with the relative ease with which large area thin film deposition can be achieved, has opened up the possibility of using α-Si:H in many different device structures. As a result α-Si:H is currently the object of a great deal of scientific and commercial interest.

The remainder of this chapter provides a more detailed introduction to amorphous silicon. The notation α-Si is used as a general term to include all different forms of amorphous silicon. When a specific form is being considered this is clearly stated e.g. evaporated α-Si, hydrogenated α-Si (α-Si:H) etc. The emphasis is on glow discharge produced α-Si:H, which

was the material used in this investigation, although other types of α-Si are included for comparison. Sections 2.2 and 2.3 deal with the preparation and structure of α-Si films. Because of the importance of the electronic structure of α-Si, section 2.4 discusses methods of measuring the gap density of states as well as the current models of the band structure. The electrical and otpical properties are summarised in sections 2.5 and 2.6 respectively, and the chapter closes with a review of the potential applications of α-Si:H.

2.2 Preparation of Amorphous Silicon

Pure amorphous silicon has traditionally been produced by radio frequency (r.f.) sputtering, vacuum evaporation and electrolytic deposition, although the latter method is not commonly used. R.F. sputtering is usually performed in an argon atmosphere using a prefabricated, polycrystalline or compressed powder target(2). Deposition rates of a few microns per hour can be attained with an Ar pressure of $\sim 10^{-3}$ torr. The inclusion of a small amount of Ar in the films (typically 1%) is unavoidable and forms the major impurity in a good system. Vacuum evaporation can produce α-Si films up to 20 μm thick with properties similar to sputtered material, given ideal conditions(1). These are ultra-high vacuum ($\sim 10^{-10}$ torr), pure source materials, a large source-substrate separation, ultra-clean, smooth substrates held at high temperatures (250-300°C) and a slow evaporation rate.

Films of hydrogenated α-Si are generally made directly, although the post-deposition hydrogenation of pure α-Si samples is possible. The most popular methods are the glow discharge technique and r.f. sputtering in a hydrogen atmosphere : these will be described in detail. Other techniques are described only briefly.

The Glow Discharge Technique

Hydrogenated amorphous silicon was first produced using the glow discharge (g.d.) decomposition of silane, SiH_4 by Sterling et al[3,4] in 1965. Subsequently, intensive investigations were carried out by Spear's group at Dundee[5, 6]. The plasma provides a convenient means of transferring energy to the gaseous molecules. The electrons contained in the plasma have sufficient energy (1-10eV) to break molecular bonds by collision, creating new species such as atoms, ions and free radicals. These species may then recombine to form more stable compounds. A glow discharge may thus be used to facilitate chemical reactions at low ambient temperatures.

The earliest apparatus used inductive coupling of the r.f. power to maintain the discharge[3,4] (see Fig. 2.1(a)). Silane gas flowed through the quartz chamber, over the substrate, mounted on a heated block. The system was operated at a power of 10-20W in the frequency range 0.5-100 MHz. The deposition rate ranged between 100 and 1000 $Å\ min^{-1}$. The electronic properties of films deposited in this fashion depend critically on a large number of variables e.g. substrate temperature (T_d), gas flow rate and pressure, r.f. power level, the floating potentials on various internal surfaces and the system geometry. The uniformity of the films is a problem owing to the small size of the discharge chamber, typically 5-7 cm internal diameter. Unfortunately this is difficult to overcome since the arrangement is not easily scaled up.

Large area specimens with a higher degree of uniformity may be deposited using a capacitively coupled r.f. discharge[5-7]. A schematic diagram of such a system showing the internal parallel plate electrodes is given in Fig. 2.1(b). The variables governing deposition are as listed for the inductively coupled system. Pure silane is passed through the system while the substrate is held at a constant temperature T_d. Flow rates, which can be between 10 and 30 standard cm^3 per minute are monitored electronically and

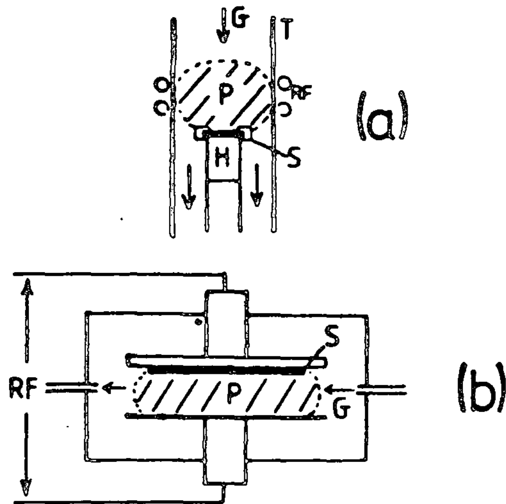


Fig. 2.1 Schematic diagram of gas phase deposition of an amorphous semiconductor using (a) inductive coupling of the r.f. and (b) capacitive coupling P is the plasma, S, the substrate and G is the gas flow direction.

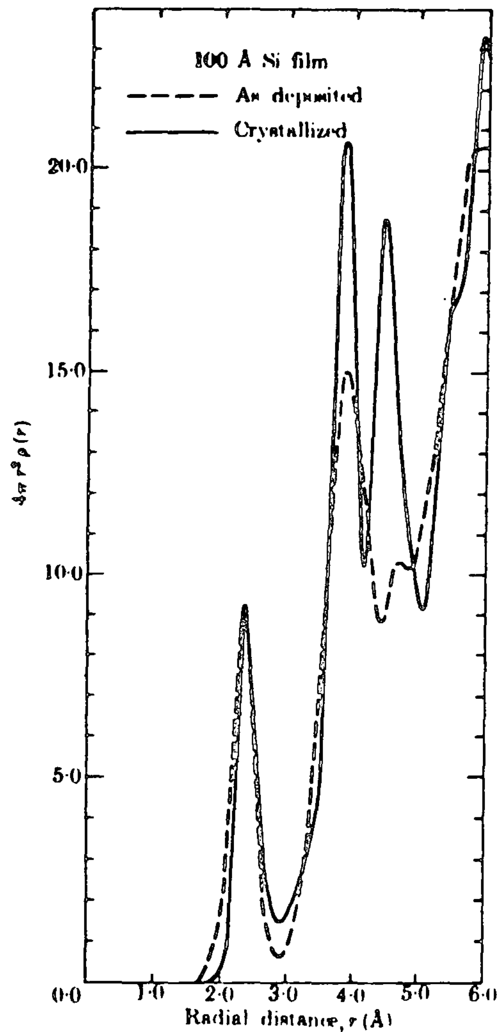


Fig. 2.2 Radial distribution function of amorphous (evaporated) and crystalline silicon as determined from analysis of electron diffraction data (29).

the gas is pumped away at the lower end of the chamber, maintaining a pressure of a few torr. Decomposition takes place inside the reaction vessel and α-Si:H is deposited on the internal surfaces. Operating frequencies are typically a few MHz with power levels of 10-20W, resulting in a growth rate of about 500 $Å\,min^{-1}$. For a given system with set operating conditions the main variable which determines the film properties is the deposition temperature. Recently, very large area (60 cm diameter) α-Si:H films have been produced with a low frequency (380 kHz) discharge[8]. However, this material seems to have rather poor electronic properties at present.

Thin films of α-Si:H have also been made in a d.c. glow discharge of SiH_4[9]; the substrate can be made either the cathode or the anode. In the case of an insulating substrate this method may still be used by placing a cathodic screen near the substrate.

The doping of α-Si:H was first reported by Chittick et al[4] although the first detailed experiments were carried out by Spear and LeComber[10]. To produce a doped layer, the correct dopant in gaseous form is mixed with the silane before passing into the reaction chamber. Phosphine (PH_3) or diborane (B_2H_6), for n- and p-type films respectively is admitted to a small known volume and its pressure is measured. It is then expanded into an evacuated cylinder and mixed with silane to attain a standard pressure. In this way a few volume parts per million can be added to the silane with a fair degree of accuracy. Any combination of n-type, p-type or undoped layers can be deposited simply by controlling the gas flow through the reaction vessel. The use of such toxic gases necessitates nitrogen 'purging' facilities to clean the apparatus.

Whichever experimental arrangement is chosen, the plasma in a glow discharge is always in close proximity to the substrate. The reactions taking place at this surface are very complex since they involve many

different chemical species e.g. silicon-hydrogen fragments, electrons. The production of reproducible films requires close experimental control over these reactions and is not easily achieved. As a consequence, different laboratories may produce films which are ostensibly the same and yet exhibit markedly different properties.

R.F. Sputtering

Reactive sputtering in hydrogen is a modification of the conventional inert gas sputtering technique. Hydrogen is added to the inert gas, the proportion being up to 20%. A target of pure Si is held at a large negative d.c. potential relative to the low pressure plasma of gas. Ions are accelerated to the target ejecting (usually) neutral atoms, some of which diffuse to the substrate. Paul et al[11] first showed the effect of hydrogen inclusion in sputtered α-Si:H films. The equipment used is very similar to a capacitively-coupled plasma decomposition system, the main differences being the much lower pressure ($\sim 5 \times 10^{-3}$ torr) and the higher d.c. potential (1-2 kV compared with $\sim$ 100V). Both the hydrogen partial pressure and the argon pressure are important variables in determining the film properties, and the bias may also be important. Doping from the gas phase has also been achieved in sputtered films[11].

Other Methods

Several other techniques are currently at an early stage of development. Chemical vapour deposition (c.v.d) of silane has been successfully used and doping of such films has been reported[12]. These films are thought to contain less hydrogen than g.d. α-Si:H because of the high deposition temperature (650°C). Thus post-deposition hydrogenation by annealing at $\sim$ 400°C in a hydrogen plasma may be necessary[13]. Miller et al have described α-Si:H formation by reactive evaporation[14] where atomic hydrogen is added to the silicon during the deposition process. More recently Caesar et al[15, 16]

have used ion beam deposition : the advantage claimed for this technique is that deposition occurs in a field free region, resulting in minimum heating, radiation and plasma damage to the growing film. Preliminary results suggest that this method may offer a greater control of the intrinsic defects and hence of the electronic properties of the films.

2.3 The Structure of Amorphous Silicon

2.3.1 Methods of Structure Determination

Diffraction Techniques. As with crystalline materials the major tools for structural assessment are X-ray, neutron, and electron diffraction. The practical and theoretical aspects of these techniques, as applied to the amorphous state, are discussed extensively in refs.[17-19]. Because amorphous solids lack any periodicity and are generally isotropic on a macroscopic scale their diffraction patterns consist of broad rings or 'haloes'. From the measured angular intensity distribution of scattered radiation a one-dimensional description of the atomic arrangement, known as the radial distribution function (RDF) can be calaculated. A plot of the RDF against r, the distance from an arbitrary atomic centre, displays peaks situated at r values corresponding to the average separation of nearest neighbours, next-nearest neighbours etc. The width of a peak gives the fluctuation in the interatomic spacing and the area under a peak is related to the co-ordination number.

Other Methods

Extended X-Ray Absorption Fine Structure (EXAFS) measurements may be used to complement diffraction studies[20, 21]. The sample is bombarded with X-rays photoejecting electrons from deep states. These electrons are backscattered by surrounding atoms and they interfere with the outgoing wave, thus modulating the absorption coefficient. An RDF can be obtained from the energy dependence of the absorption coefficient. The technique

is especially useful for investigating alloys, since each element can be examined independently using its own characteristic absorption edge and fine structure. EXAFS is substantially more sensitive to elements present in low concentrations than diffraction techniques.

The vibrational modes of bonded atoms can be investigated using infra-red (IR) radiation. Two methods are currently in use : infra-red spectroscopy[22], which involves absorption and reflection measurements, and Raman spectroscopy[22], which measures the scattering of IR photons in the creation or destruction of optical phonons. Local molecular groupings in amorphous materials can be identified by comparing results with those obtained on crystalline specimens (or with theoretical calculations) since each grouping has characteristic frequencies of vibration corresponding to the stretching and bending of the bonds.

2.3.2 Models of Structure

Models of amorphous solids are based on the concept of an 'ideal' amorphous material i.e. one which is free of impurities, voids, inhomogeneities and where all bonds are satisfied. Calculations of their RDF, density, local bonding arrangements and vibrational properties can be compared with experimental data. Two approaches are possible. The crystallite theory views a material in terms of regions, where the atomic order approaches that of the crystalline state (crystallites), interconnected by regions with a lesser degree of order. However, with small crystallites about 50% of the volume consists of these connecting regions, which must therefore be as important as the crystallites[23]. In the limit (i.e. as the crystallite size is reduced) the model becomes indistinguishable from the continuous random network (CRN) model, where the atoms are arranged according to certain constraints. The major constraint of the CRN is that every atom has its chemical bonding requirements satisfied: nearest

neighbour bond lengths are set to approximately their crystalline value ($\pm$1%) and bond angles are allowed to fluctuate within given limits.

2.3.3 The Structure of α-Si

Both X-ray[24-27] and electron diffraction[28-30] have shown that in pure α-Si the short range order of the diamond cubic lattice is more or less preserved. Fig. 2.2 shows a comparison of the experimentally determined RDF's of amorphous and crystalline Si. The correlation between the first and second peaks of the two sets of data indicates that each atom has four nearest neighbours, arranged tetrahedrally, with bond lengths within a few percent of their crystalline value. There are twelve next-nearest neighbours at an average separation of $\sqrt{8/3}$ of the crystalline bond length, but with an r.m.s. distortion of $\pm$10% from the normal tetrahedral angle (109° 28'). Beyond this any structure is lost, as evidenced by the missing third peak.

Polk[31] constructed a 440-atom, 'ball and stick' model to simulate the structure of amorphous silicon (and α-Ge). The continuous random network is shown in Fig. 2.3. It allows the relative orientation of neighbouring triads of bonds (known as the dihedral angle) to take up any value. The statistical distribution of dihedral angles gives the network its random character. This model has been refined[32-34] and seems to provide the best fit to experimental data, although different models have been proposed[35, 36].

The densities of pure α-Si films are usually between 3 and 15% lower than that of Si single crystals. Calculations based on CRN models predict only a 1-3% density difference. The discrepancy is generally attributed to the presence of voids in the structure and small angle electron and X-ray scattering experiments seem to confirm this[28, 29, 36]. The large density of defects ($\sim 10^{20}$ cm^{-3}) with unpaired spins is shown by the relatively large electron spin resonance (esr) signal. A substantial fraction of these

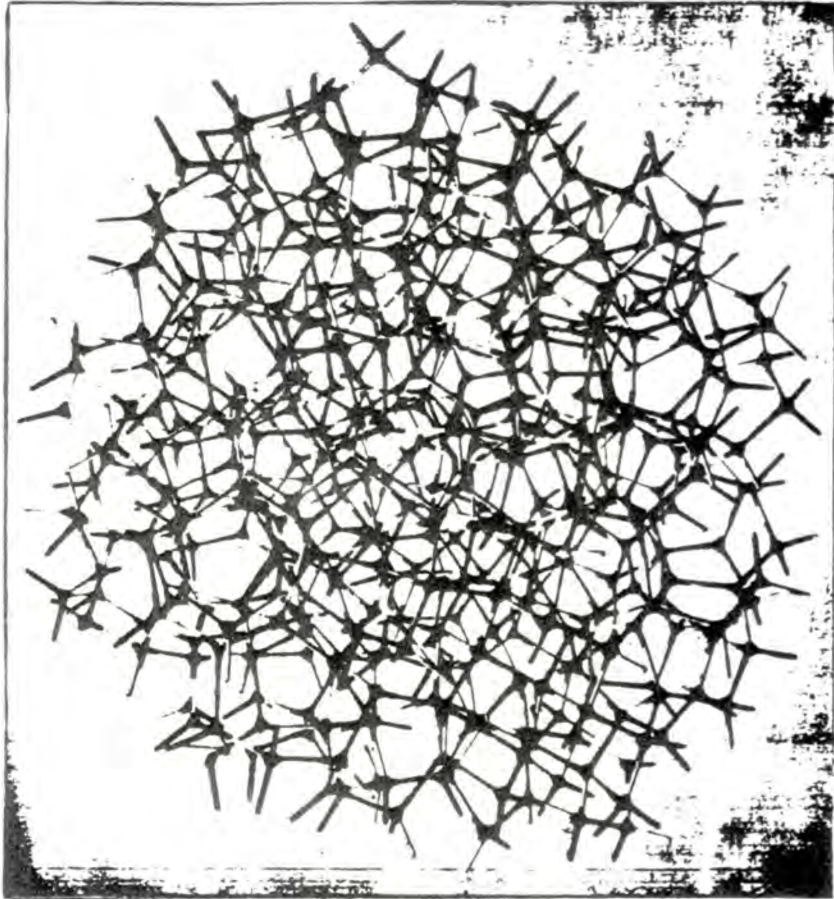


Fig. 2.3 The 440-atom continuous random network built by Polk (31) to simulate the structure of α-Ge.

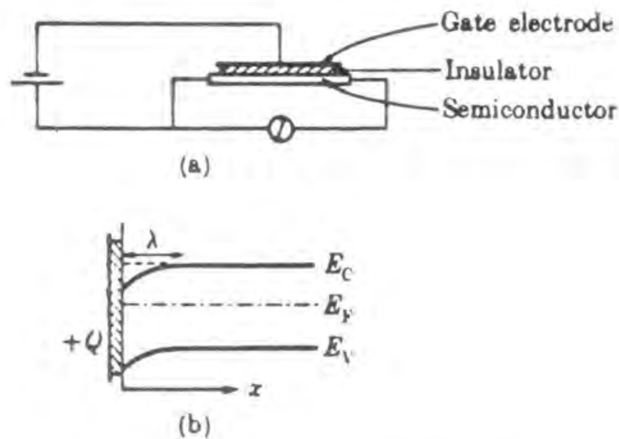


Fig. 2.4 (a) Experimental arrangement for field-effect measurements.

(b) Variation of potential with distance x below the surface of the semiconductor. A charge +Q on the gate electrode induces -Q which, in the absence of surface states, is distributed throughout a space charge region λ either in gap states or in the bands.

defect states may reside on the internal void surfaces[37]. The electronic states associated with these defects dominate the properties of such films (see sections 2.4 and 2.5).

Amorphous silicon films which incorporate hydrogen (α-Si:H) exhibit markedly different properties from pure α-Si. Undoubtedly, the hydrogen molecules neutralise the defects i.e. they satisfy dangling bonds, as shown by the substantially reduced esr signal. The electronic states associated with these defects are thus removed and no longer control the film properties. However, the amount of H_2 incorporated into the films (from 5 to 50 atomic percent) is many times larger than that required for defect passivation. Because of this α-Si:H should be treated more as an alloy material, of composition $\alpha\text{-}Si_{(1-x)}H_x$.

X-ray and electron diffraction results[27, 30] indicate that α-Si:H has the same basic structure as pure α-Si with a slightly higher degree of local order (i.e. some structure is evident to the third nearest neighbour). Various groups have investigated the incorporation of H using infrared and Raman spectroscopy. Some have identified the presence of hydrogen in the forms SiH, SiH_2, SiH_3[38] ; others have not detected the SiH mode[39]. More recently Lucovsky[40] has interpreted infrared data in terms of SiH, SiH_2 and $(SiH_2)_n$ groupings, where the latter chain has the same vibrational spectrum as SiH_3. The exact role of hydrogen in α-Si:H is still not clear. Moustakas et al[41] have suggested that, after defect passivation, hydrogen incorporation increases the gap density of states around the mobility edge. This question is also the subject of a review by Knights and Lucovsky[42].

Hydrogenated α-Si can be doped using trivalent or pentavalent impurities. It was originally thought unlikely that these dopants could be forced into four-fold co-ordination in α-Si:H, because of the flexibility inherent in a CRN structure[1]. However, measurements on P doped α-Si:H[10, 43] and

EXAFS studies of As doped films[44] give direct evidence of substitutional doping. With low dopant concentrations the doping efficiency is typically 20% for As and 30-40% for P. The structure is not significantly altered, except by high doping levels.

2.4 The Electronic Structure of Amorphous Silicon

2.4.1 Methods of Measuring the Gap Density of States

(a) The Field Effect Technique

This method probes the gap density of states (DOS) by displacing the state distribution with respect to the Fermi level. A typical specimen geometry is shown in Fig. 2.4(a). The conductivity of the surface layer of the semiconductor between source and drain is monitored by measuring the current for a fixed source-drain voltage. An electric field is applied normal to the sample by means of the gate electrode. The insulating layer must be of high quality and able to withstand high fields (up to 10^8 Vm^{-1}) with a minimum leakage current. The field induces excess charge at the semiconductor surface. Some of the charge is trapped in surface states at the semiconductor/insulator interface and some resides in bulk states (both band states and localised states) within the space charge region (see Fig. 2.4 (b)). The conductivity is modified by this excess charge and the changes can be related to the density of states at the Fermi level. The analysis is complex and several approaches are possible[45-50]. The main difficulty lies in distinguishing between charge in the surface states and charge in the bulk states. In principle, a surface state density $\sim 10^{13}$ cm^2 eV^{-1} would screen the specimen from the external field, making measurements of the bulk DOS impossible.

(b) Steady-State Admittance Measurements

Capacitance-voltage (C-V) measurements are closely related to the field effect technique, and have been widely used on crystalline materials with metal-insulator-semiconductor (MIS) devices, Schottky barriers or

p-n junction structures[51]. For small biases the resistance of the depletion region is much greater than that of the bulk and so the depletion width may be obtained directly from the measured capacitance, assuming uniform doping. The capacitance can also be related to the charge density in the depletion region and thus to the density of states. The frequency must be low enough to allow the localised states to follow the oscillating capacitance measurement voltage. Unfortunately, the presence of surface states can lead to spurious results, especially at low frequencies.

Capacitance v frequency (or temperature) measurements have the advantage that a regime may be chosen where surface state effects are minimised (usually high frequency, low temperature). Even so, the separation of bulk and surface contributions is not always simple and the technique is limited to measuring the DOS over a relatively small portion of the gap near E_F.

Admittance data may be obtained from tunnellable and non-tunnellable MIS devices. The extraction of a gap DOS is dependent on forming an equivalent circuit for the device. The application of this technique to amorphous semiconductors has been hindered by the poor theoretical understanding of such devices, making modelling difficult. Determining the exact role of surface states complicates matters further, allowing only estimates of the DOS to be made.

(c) <u>'Bulk' Measurements</u>

Traditional 'bulk' measurements e.g. transport data, optical effects, spin resonance are often viewed as giving a more representative value of the bulk DOS, even though interface effects can cause serious errors in films less than a few microns thick. Transport data such as conductivity, drift mobility, space charge limited currents etc. can be used to identify certain transport mechanisms and can shed light on the DOS (see section 2.5).

Optical properties like absorption, luminescence and photoconductivity can also yield information on features in the DOS, linking them with particular transitions or recombination mechanisms (see 2.6). Electron spin resonance (esr) is limited in that it can only detect states which have unpaired spins. Nonetheless, it can be used to determine an upper limit to the DOS, though it cannot identify where (in energy terms) those states lie.

(d) Non-Equilibrium Techniques

The most powerful of the transient techniques is Deep Level Transient Spectroscopy (D.L.T.S.)[52]. This relies on the band bending at a potential barrier to provide a depletion region. By creating a non-equilibrium state e.g. applying a voltage pulse, and monitoring the current or capacitance, information regarding the state density and energy location can be obtained. Surface and bulk states can be distinguished relatively easily and spatial variations in the DOS can be investigated (profiling). The data analysis for an amorphous semiconductor is rather involved, and care must be taken in modelling the device response. The technique can only be used for semiconductors on which a barrier can be produced, which often limits it to fairly conducting samples. Other non-equilibrium techniques involve measuring thermally stimulated currents (TSC) and thermally stimulated capacitance (TSCAP).

2.4.2 Models of the Gap Density of States in Amorphous Semiconductors

An early and influential model of the gap DOS in amorphous semiconducting alloys was proposed by Cohen, Fritsche and Ovshinsky in 1969[53] (the CFO model). They supposed that the tails of localised states from the conduction and valence bands (due to the non-crystallinity) would overlap, as shown in Fig. 2.5(a). States from the conduction band would be neutral when empty, while those from the valence band would be neutral when filled. The overlapping of the two tails would create centres of

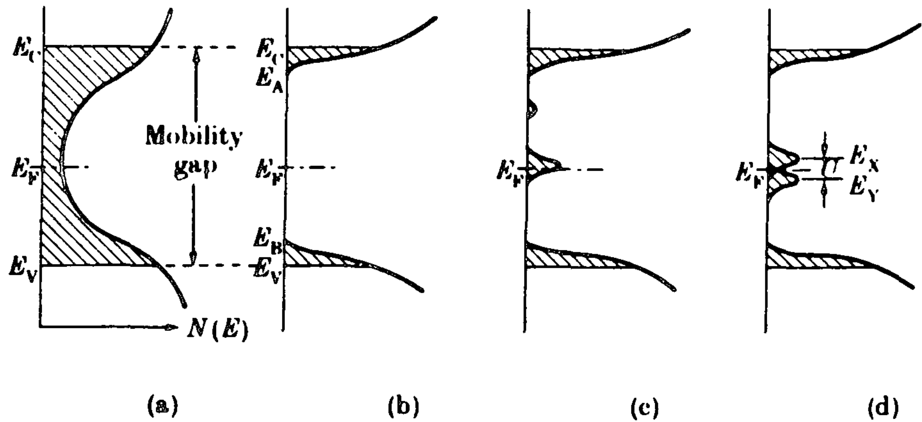


Fig. 2.5 Various forms proposed for the density of states in amorphous semi-conductors. Localised states are shown shaded. (a) the CFO model (53), (b) a real gap in the density of states, as appropriate to an 'ideal' (defect free) material (c) the same as (b) but with a partially compensated band of defect levels (55), (d) the same as (b) but with overlapping bands of donor (E_Y) and acceptor (E_X) levels arising from the same defect.

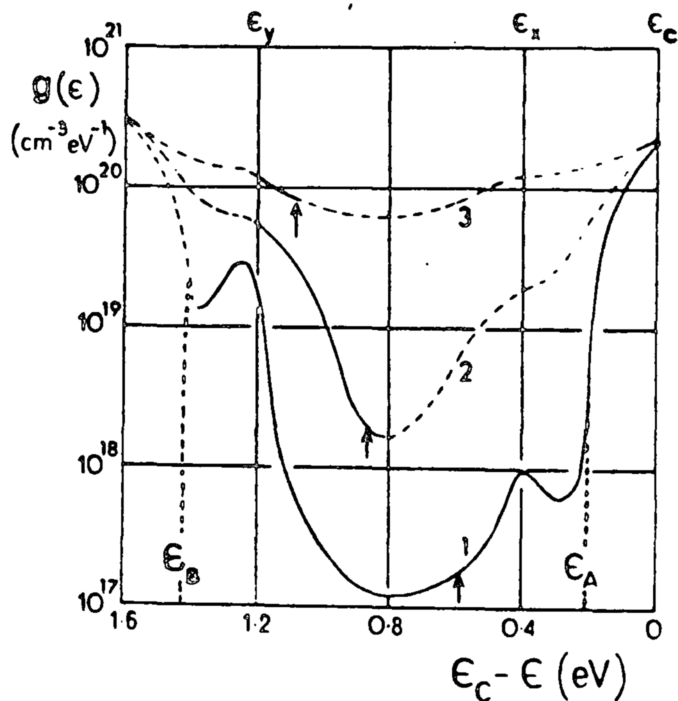


Fig. 2.6 Density of states $g(\varepsilon)$ in amorphous silicon determined by the field effect technique (61). Curve 1: glow discharge α-Si:H deposited at 550K, Curve 2: glow discharge α-Si:H deposited at 350K. Curve 3: evaporated or sputtered α-Si.

unpaired spin because the states would be charged, and this would pin the Ferm level (E_F) at this position, a phenomenon commonly observed in α-materials. At a given energy in the conduction and valence band these authors defined a'mobility edge' corresponding to the transition from localised to extended states, first suggested by Mott[54]. The range of energies between these two mobility edges is called the mobility gap. The density of states required to pin the Fermi level in this model is high and should be observable both optically and using esr measurements. Since many amorphous semiconductors and insulators are transparent in the visible or infrared and do not exhibit an esr signal equivalent to such a high DOS this model is not commonly applicable. More recently, theoretical calculations have indicated that the band tailing due to disorder should not be as extensive as to cause overlapping.

The generally accepted picture of the band edges in an ideal amorphous semiconductor (as previously defined) is shown in Fig. 2.5(b). A genuine band gap exists. States between E_c and E_v are localised with a very low carrier mobility (see section 2.5). The occurrence of defects can give rise to states in the gap, just as in a crystalline semiconductor, and various models have been proposed explaining observed properties in terms of defect states. Fig. 2.5(c) shows one such model due to Davis and Mott[55] where a band of acceptor levels is partially occupied by electrons from a weaker band of donors. Like the CFO model the density of states required to pin E_F is high, and is not observed experimentally. Roberts[56, 57] has suggested a model involving two defect levels (see also (58)) which would probably be narrow bands of states, as shown in Fig. 2.5(d). Such levels could be responsible for pinning E_F with densities which are too low to be detected optically and can be used to explain experimental data[59].

2.4.3 The Gap Density of States in α-Si

Films of pure α-Si prepared by evaporation or sputtering generally have high gap densities of states, particularly at the Fermi level, E_F.

This is shown by the observation of log conductivity v $T^{-\frac{1}{4}}$ behaviour (hopping conductivity) and also by the small value of the thermopower[60], both of which indicate transport at E_F. The estimated DOS is $> 10^{19}$ cm^{-3} eV^{-1} and E_F is invariably pinned near midgap. These samples give a large esr signal equivalent to a volume density of paramagnetic centres of 10^{19} - 10^{20} cm^{-3}.

Hydrogenated α-Si films show no signs of hopping conductivity and give no esr signal, indicating a much lower overall density of gap states. Glow-discharge produced α-Si:H has been extensively studied by the Dundee group, using the field effect technique[47, 48, 61]. Their results are summarised in Fig. 2.6. Films deposited onto substrates held at higher temperatures (∿ 500K) have the best electrical characteristics. The DOS generally increases with decreasing deposition temperature[61]. The main features of the DOS (see curve 1) are a broad minimum (of about 10^{17} cm^{-3} eV^{-1}) near the centre of the mobility gap bounded by two peaks at E_x and E_y, and a rapidly rising density at E_A corresponding to the tailing of the conduction band. Various authors[62, 63] suggested that some of these features may be artefacts of the analysis used by Spear and LeComber[47], although Grunewald et al[64] derived similar features (within a factor of 2 or 3) using a different analysis. Surface states are also a problem : if the DOS at the surface is different from that in the bulk then errors will be introduced in N(E)[65]. Field effect data can therefore only give an upper limit to the gap DOS and features of the state distribution must be verified by independent experiments.

A high degree of correlation has been found between the field effect DOS and data from other experiments. The low DOS in midgap is clearly demonstrated by the ability to move E_F easily by doping[10, 66]. Evidence for the existence of the peak at E_y comes from photoconductivity results, which exhibit features at hν = 1.1 - 1.2 eV, corresponding to an $E_y \rightarrow E_c$

transition[67]. Capacitance measurements confirm this high DOS at E_y[68], as does the increasing difficulty experienced in moving E_F through the region of E_y by doping[10, 66]. Furthermore, the transport of excess holes has been shown to be controlled through the trapping and thermal release of carriers by states situated at E_y[69]. The peak at E_x is more difficult to detect, because of its lower density. However, it has been identified by Beyer et al[70], and by Kablitzer et al[66], who estimated the DOS by measuring the number of implanted ions required to move E_F a given distance. Anderson and Spear have also implied its existence from photoconductivity measurements[71], as have Fuhs and Milleville from studies of thermally stimulated conductivity[72]. Finally the rapid rise in N(E) at the conduction band tail is demonstrated by the difficulty of moving E_F by doping[10,66] and the onset of the tail states has been located at about 0.2eV below E_c by electron drift mobility measurements[5].

More recently, Lang et al[73] have investigated the gap DOS using DLTS, TSCAP and TSC techniques. They report a much lower midgap density of states of the order of 10^{15} cm^{-3} eV^{-1}. Their DOS distribution is substantially different to the field effect results, with a deep minimum between 0.3 and 0.6 eV from the conduction band and a broad shoulder of states extending from the valence band to midgap. Some optical and transport data have been re-interpreted to provide support for this model. A similar distribution has been reported by some workers using C-V measurements on thick insulator MIS structures[74-76].

Space charge limited current (SCLC) measurements, first observed in α-Si:H by Ashok et al[77], may provide independent verification of the DOS distribution, since this type of conduction depends on the bulk distribution of localised states. Results published by den Boer[78] quote the density of states at midgap to be between 1-4 x 10^{16} cm^{-3} eV^{-1},

halfway between the field effect DOS and the DLTS DOS. The distribution of states over a small energy range (0.2eV) resembles the field effect DOS. Bhattacharya et al[79] have measured $N(E_F)$ by SCLC and field effect experiments. They obtain a value of 7.9×10^{16} cm^{-3} eV^{-1} from both methods. Mackenzie et al[80] have found similar densities of states and have shown that the distribution of these states over quite a wide range of energies is not dissimilar to the earlier field effect data of Spear and LeComber[47].

The origin of the two DOS peaks is still the subject of speculation. An early suggestion[10] associated these states with a defect similar to the divacancy in crystalline silicon, which produces states at comparable energies within the bandgap[81]. However, the inequality in the densities of the two levels observed in α-Si:H shows that this interpretation is too simple. It would seem that a whole range of possible defects must be considered[82].

2.5 The Electrical Properties of Amorphous Silicon

The electrical properties of evaporated films of α-Si are dependent on the exact preparation conditions. In particular these films may take up large quantities of oxygen during evaporation. Increasing oxygen concentrations lead to decreasing defect densities and conductivity[83]. The variation in conductivity with temperature is approximately $\sigma \propto T^{-\frac{1}{4}}$ which suggests hopping near the Fermi level as the normal conduction mechanism. Experiments by Knotek[84] on α-Si films of varying thickness deposited under the ultra-high vacuum provide conclusive evidence for variable range hopping, and he estimates the density of states of E_F to be $\sim 3 \times 10^{19}$ cm^{-3} eV^{-1}. This density is consistent with a pinned Fermi level as observed.

Glow discharge and sputtered α-Si:H films are generally much more resistive than evaporated α-Si films deposited at similar temperatures. The deposition temperature, T_d, is the main variable governing the

properties of these films. As shown in Fig. 2.7 an increase in T_d from 300K to 640K changes the room temperature conductivity of g.d. α-Si:H by over five orders of magnitude. The minimum at $T_d \sim 250K$ suggests a change in the conduction mechanism. According to Spear, at high T_d transport is due to electrons moving above the mobility edge and at low T_d to holes hopping through localised states near the valence band[5]. Measurements of drift mobility and conductivity seen to confirm this. Fig. 2.8 shows data taken by LeComber and Spear for an undoped g.d. α-Si:H sample deposited at T_d = 500K. They have identified three distinct temperature regimes and have associated each with a particular conduction mechanism as follows[85]. (Subsequent measurements on samples prepared at different values of T_d are in agreement.) For T > 250K the conduction is an activated process with an activation energy (from the slope of the μ_d graph) of ∿ 0.19eV. Electrons drift through the extended states but interact with the localised states by trapping and thermal release. Hence the measured drift mobility μ_d is trap controlled, with a room temperature value of ∿ 0.1 $cm^2\ sec^{-1}\ V^{-1}$. From this, the deduced mobility near the bottom of the extended states, μ_o is about 10 $cm^2 sec^{-1} V^{-1}$. Moore[86] has reported very similar results. As the temperature is decreased the probability of an electron being thermally released from a localised state drops, and at a given temperature the hopping of electrons between localised states will become the dominant transport mechanism. For T < 250K the drift mobility is of the order of $10^{-2}\ cm^2\ sec^{-1}\ V^{-1}$, which is consistent with phonon assisted hopping. A clear change in the slope is seen at T = 250K, and the hopping activation is ∿ 0.09eV. Moore has not found this large change in slope, which casts some doubt on the interpretation[86]. However, the conductivity data clearly exhibit these two regimes (see Fig. 2.8(b)). At T = 250K the slope changes from 0.62eV to 0.51eV, a difference of 0.11eV. Thus the change in slopes in μ_d and σ are approximately the same, as predicted by theory[1]. Estimates of the conductivity based on the previous value of

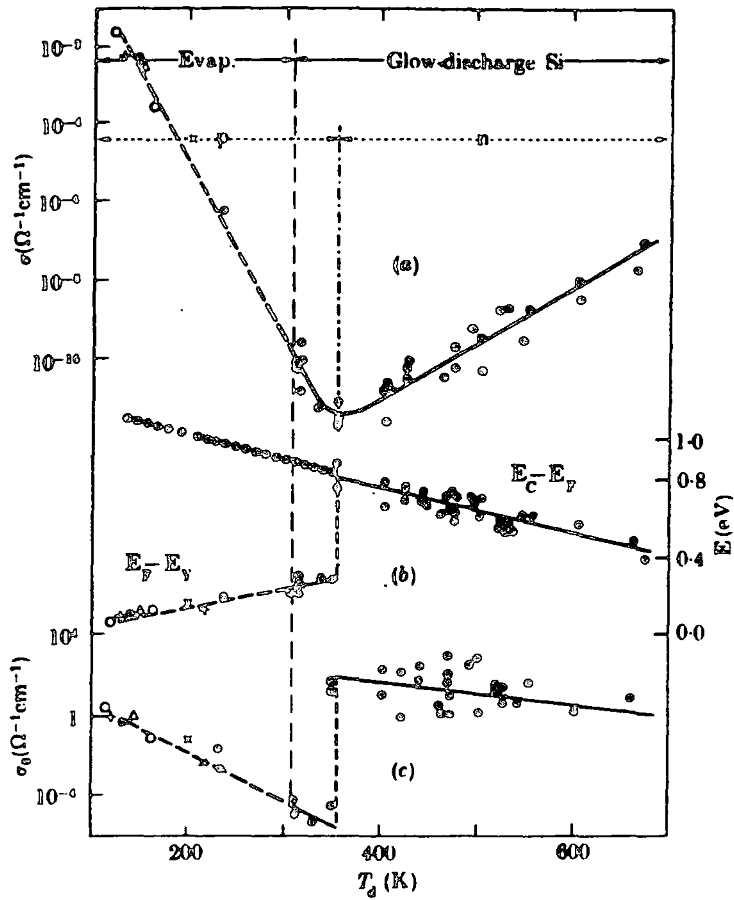


Fig. 2.7 Variation of (a) room temperature conductivity σ (b) activation energy of conductivity (c) pre-exponential factor σ_o for glow discharge α-Si:H with deposition temperature T_d. Points on the left of this figure refer to evaporated films for which T_d has no real significance (after ref (6)).

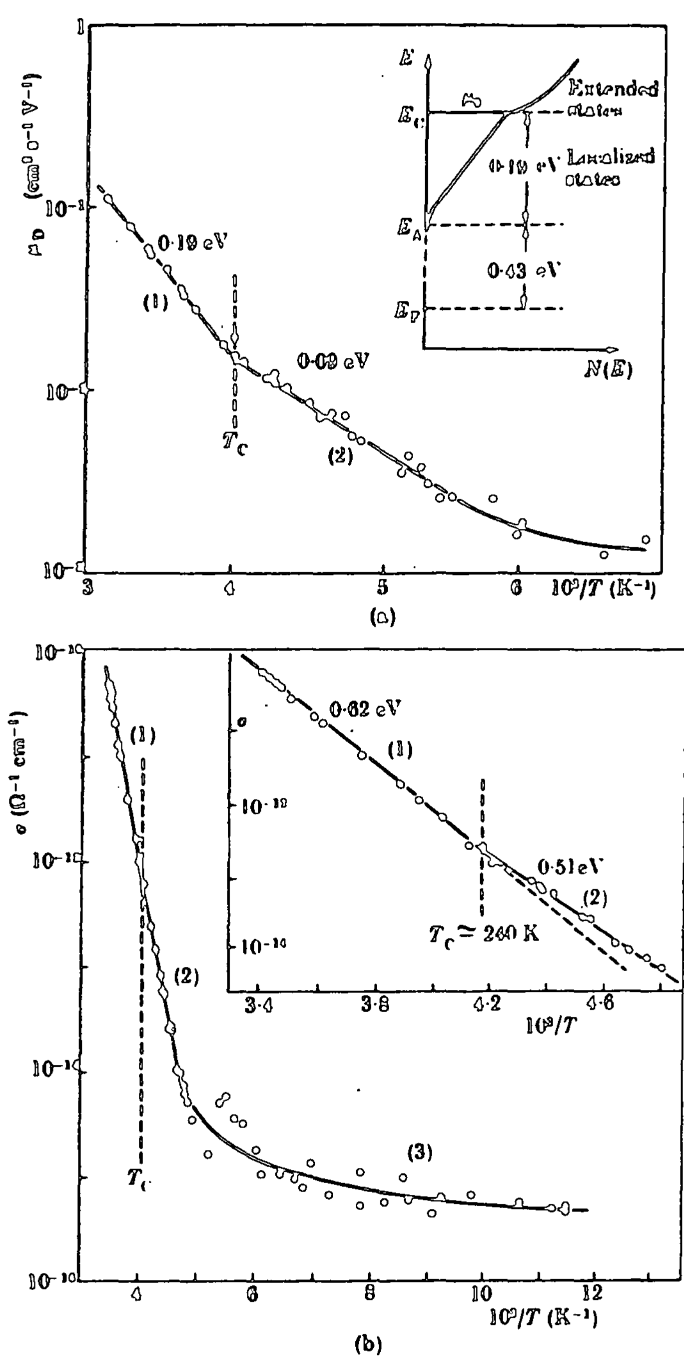


Fig. 2.8 Temperature dependence of (a) electron drift mobility μ_D (b) conductivity σ in a glow discharge α-Si:H film deposited at 500K (85).

μ_o and $(E_c - E_F) = 0.62$eV from the slope of σ v $^1/_T$ (for T > 250K) concur with experimental measurements. The conductivity v $^1/_T$ graph also suggests the existence of a third region. For T < 170K the hopping energy decreases still further. This is thought to be indicative of variable range hopping[87] between localised states near the Fermi level.

The drift mobility of holes is considerably less than that of electrons, with a room temperature value of between 5 and 6 x 10^{-4} cm^2 sec^{-1} V^{-1} [69,86]. The mobility is still trap-controlled and the μ_d v $^1/_T$ graph has a break point at 250K, with corresponding activation energies of 0.35eV (above) and 0.26eV (below).

The position of the Fermi level in films described so far is defect controlled. High temperature α-Si:H i.e. T_d ∿ 500-600K is invariably n-type, with $E_c - E_F$ approximately 0.6eV. Doping(as described in Section 2.2) enables the movement of E_F to within about 0.2eV of either mobility edge[10]. The introduction of phosphine (PH_3) as a dopant gas in concentrations of only a few p.p.m. increases the conductivity (n-type) by over two orders of magnitude (see Fig. 2.9). The rate of increase in the conductivity falls off with increasing dopant concentration as E_F moves into a higher density of gap states. The introduction of diborane (B_2H_6) during preparation leads, with small concentrations, to a reduction in conductivity corresponding to the shifting of E_F to midgap. Conduction becomes p-type as the dopant concentration is increased further.

Doped samples have been used in the study of the Hall effect and the thermopower. LeComber et al[88] have measured the Hall mobility as a function of temperature in both n and p-type specimens. They discovered an interesting sign reversal in the Hall voltage : p-type samples showed a Hall voltage in the direction normally associated with electrons and n-type specimens gave a p-type Hall voltage. The former sign reversal may be explained. Theoretical treatments in terms of small polaron conduction[89]

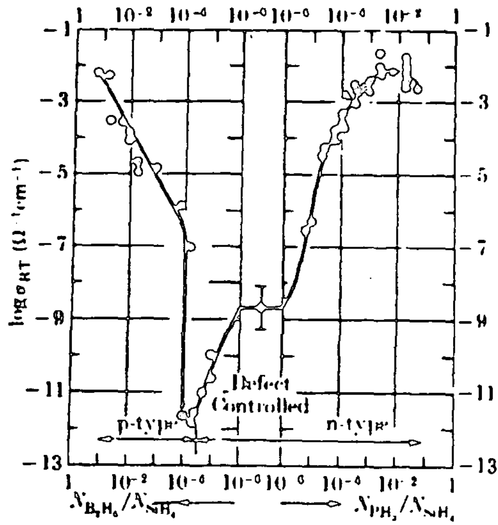


Fig. 2.9 Room temperature conductivity of n- and p-type α-Si:H plotted as a function of the gaseous composition from which the films were deposited (10).

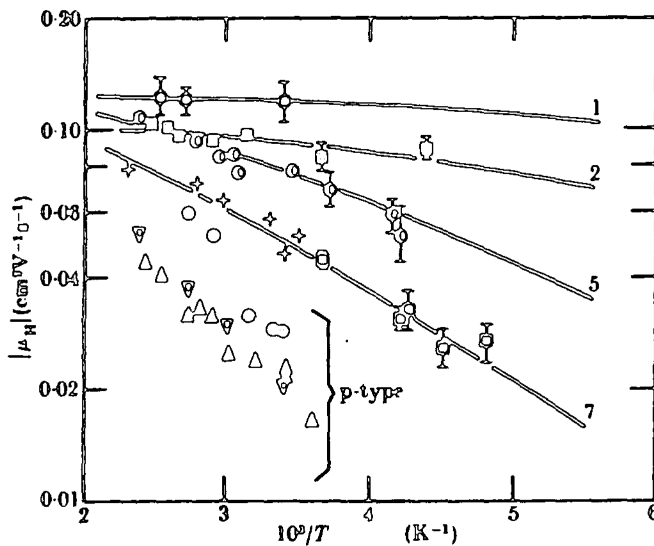


Fig. 2.10 Temperature dependence of Hall mobility for four n-type samples (1, 2, 5 and 7) and three p-type samples of glow discharge α-Si:H. The samples were prepared from silane containing the following p.p.m. of B_2H_6 (for the p-type films) and of PH_3 (for the n-type films): O, 2.3 x 10^4; ∇Δ, 5 x 10^4; 1, 98; 2, 304; 5, 2 x 10^3; 7, 3 x 10^4. The solid curves are theoretical (88).

and diffusive transport in the extended states near the mobility edge[90] both predict an n-type Hall voltage regardless of doping (majority carrier) type. The latter reversal is not clearly understood, although Emin has proposed a model which fits the experimental data by considering the nature of the local electronic states as well as the local geometry of the sites involved in conduction[91]. The magnitude and temperature dependence of the Hall mobility (shown in Fig. 2.10) are more easily explained. For lightly doped specimens μ_H is only slightly dependent on temperature, with a magnitude of between 0.1 and 0.2 $cm^2\ V^{-1} sec^{-1}$. This is in general agreement with Friedman's theory[90], although with increasing doping μ_H shows progressive deviations from the expected behaviour. LeComber et al[5, 88] have attributed this to the presence of a parallel conduction path associated with localised impurity states. Hopping through these states becomes the dominant transport mechanism, even at room temperature, in samples where the donor density exceeds 5 x 10^{18} cm^{-3}. Workers at Dundee[92] and Marburg[93,9 have measured the thermopower as a function of temperature. Both groups found that the sign of the thermopower corresponded to the majority carrier type and reported a single activation energy for lightly doped specimens (see Fig. 2.11). This activation energy, $E_{act}(s)$ is equal to the activation energy for conductivity, $E_{act}(\sigma)$ according to Jones et al[92], suggesting that transport is predominantly in the extended states. However, Beyer et al[93,94] have questioned the accuracy of high temperature measurements and have found an activation energy difference ($E_{act}(s)$ - $E_{act}(\sigma)$) of 0.05 - 0.2eV. This implies that the dominant transport mechanism is hopping through the localised states. With increasing doping both the magnitude of the thermopower and its temperature dependence decrease and the curves can no longer be described in terms of a single activation energy.

The magnitude of the a.c. conductivity of undoped g.d. α-Si:H films exhibits a systematic dependence on the deposition temperature T_d[95, 96].

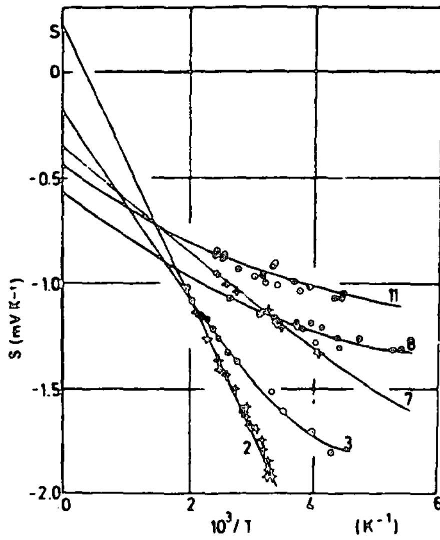


Fig. 2.11 Observed thermoelectric power S plotted as a function of reciprocal temperature for five n-type α-Si:H specimens. The sample numbers increase with increasing phosphorous content. The solid curves are theoretical (6).

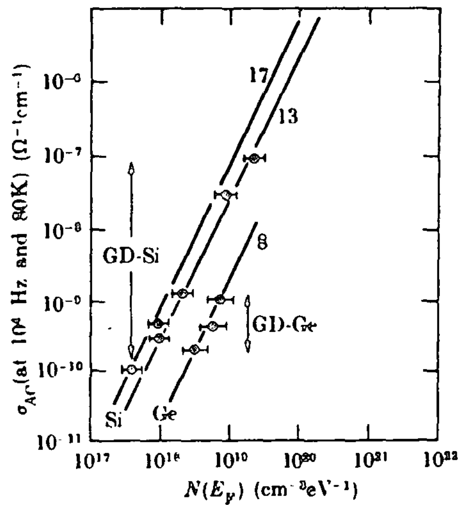


Fig. 2.12 A.C. conductivity at 10^4Hz and 80K for various films of glow discharge deposited α-Si:H and α-Ge:H plotted against the density of states at the Fermi level ($N(E_F)$) determined from field effect data (95).

More specifically, Abkowitz et al[95] have shown that a linear relation exists between $\sigma_{a.c.}$ and the density of states at the Fermi level (see Fig. 2.12). The variation in $\sigma_{a.c.}$ with frequency was almost linear ($\sigma_{a.c.} \propto \omega^{n}$ where $n \sim 0.95$) for lower temperatures. In heavily doped films the value of n may change with frequency, depending on the dopant[97]. Boron doped films have a conductivity varying as $\omega^{0.4 - 0.5}$ whereas phosphorous doped films exhibit n-values of 0.2 and $\sim$1 at low ($\sim 10^{4}$Hz) and high ($\sim 10^{6}$Hz) frequencies respectively, with a frequency-independent region in the mid-frequency range.

2.6 The Optical Properties of Amorphous Silicon

The position and shape of the optical absorption edge in amorphous silicon is strongly dependent on the method and exact conditions of preparation. Fig. 2.13 shows a compilation of data for several samples[67]. Two distinct regions are identifiable in the curves for glow discharge α-Si:H. Between photon energies of 1 and 1.4eV an absorption tail typical of amorphous semiconductors is seen, resulting from transitions involving localised states as well as extended states. At higher energies the absorption coefficient, α, rises sharply to almost 10^{5} cm^{-1} at 2.2eV, obeying the equation

$$\alpha \propto (h\omega - E_{o})^{2} \qquad (2.1)$$

ω is the frequency of radiation and E_{o} the extrapolated optical gap (1.5 - 1.9eV, depending on doping). The absorption edge shifts to higher energies as the deposition temperature decreases. This may be due to hydrogen incorporation which increases with decreasing T_{d}. The addition of hydrogen during the preparation of sputtered films has the same effect. It is interesting to note that the absorption coefficient of α-Si:H may be as much as an order of magnitude greater than that of crystalline

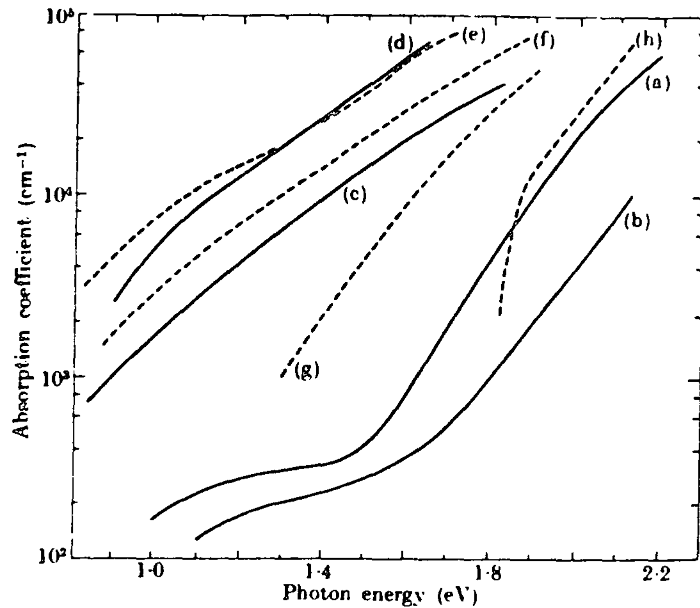


Fig. 2.13 Optical absorption edges in amorphous silicon prepared by different methods: (a) glow discharge films deposited from 500 to 600K; (b) glow-discharge films deposited at ∿300K; (c) and (f) sputtered films; (d) and (c) evaporated films; (g) annealed sputtered film (h) extrapolated edge for 'ideal' film (67).

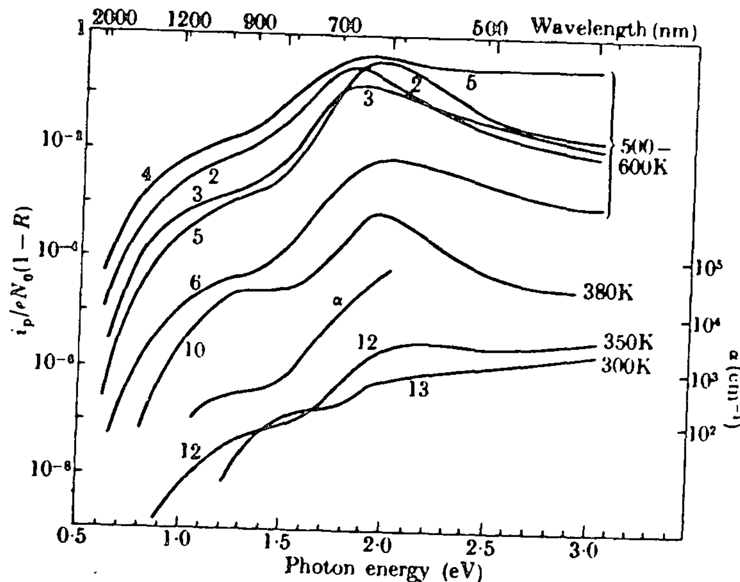


Fig. 2.14 Spectral dependence of photoconductivity in glow-discharge films of α-Si:H deposited at the temperatures indicated. The ordinate represents the number of charge carriers flowing around the circuit per absorbed photon. α is the absorption of a film with T_d = 500K (67).

silicon over the whole visible range. Sputtered and evaporated α-Si exhibit an absorption edge at lower energies than does glow discharge α-Si:H. The high absorption, even at low photon energies is indicative of a large density of localised states. Brodsky et al[98] have suggested that these states are due to structural defects e.g. voids, rather than an inherent property of the material. They showed that on annealing the absorption curves began to approach these of g.d. α-Si:H films (curve (g)). A theoetical curve for a 'void-free' specimen is also shown.

Amorphous silicon is strongly photoconductive. The absorption and photoconductivity of evaporated films show exactly the same spectral dependence i.e. the quantum efficiency is independent of energy[99]. This is not so for g.d. α-Si:H although the same structure is observed in both absorption and photoconductivity curves (see Fig. 2.14). These results have been explained by the Dundee group[67, 100, 101]. The onset of photo-conduction depends on T_d but lies between 0.6 and 0.8eV. This is attributed to the excitation of electrons from E_F to the extended states above E_c (see Fig. 2.6) or to the tail states above E_A. The latter transition is unlikely since both initial and final states are localised and their wavefunctions will only overlap slightly. In contrast, Spicer et al have explained this initial rise in terms of intrinsic absorption[102]. The shoulder between 1.1 and 1.3eV is thought to correspond to a maximum in the gap density of states about 1.2eV below E_c. The rapid rise in photoresponse above 1.5eV denotes the onset of transitions between the valence band and conduction band edges.

Luminescent spectra of α-Si:H have been widely reported and the subject has been reviewed by Street[103]. Four peaks have been sufficiently well characterised to be identifiable and their approximate spectra are shown in Fig. 2.15. Identifying a particular transition from the energy of a luminescence peak requires care, since large variations in peak position can

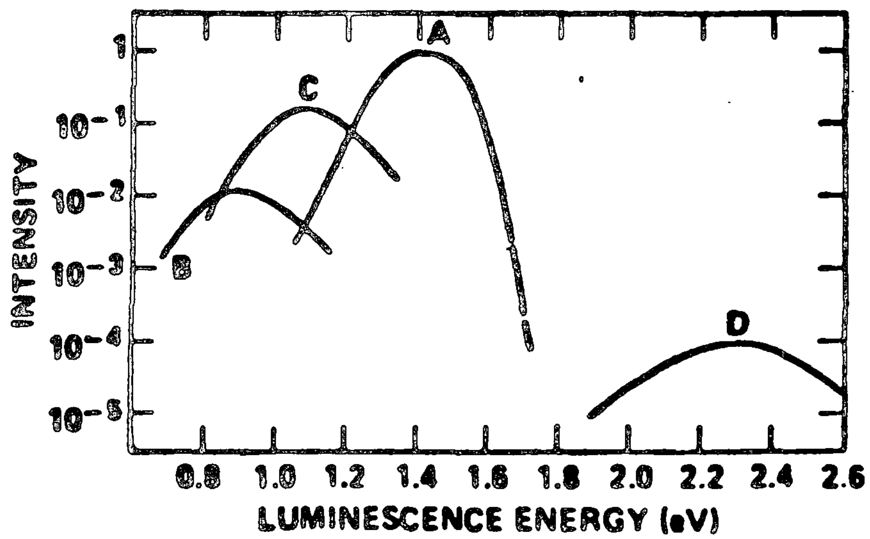


Fig. 2.15 Composite luminescence spectra of α-Si:H showing the four peaks which have been well characterised (103).

occur, depending on the manner of preparation. The largest peak at low temperatures ($\sim$10K) between 1.25 and 1.4eV has been associated with the transition $E_A \rightarrow E_B$ (see Fig. 2.6) i.e. between states at the band edges. The second most readily identifiable peak at 0.8 - 0.9eV corresponds to an $E_X \rightarrow E_B$ transition. The origin of the third peak around 1.1eV seems unclear. It has been attributed both to an $E_A \rightarrow E_Y$ transition and to the presence of oxygen as an impurity. The fourth, low intensity peak at 2.3eV (greater than bandgap) may be due to surface contamination and not an intrinsic property of α-Si:H.

Prolonged exposure to illumination can significantly affect the conductivity of α-Si:H films. This is the Staebler-Wronski effect[104] which can be reversed by annealing. Undoped or lightly doped films achieve their maximum conductivity after annealing at $\sim$ 200°C for 30 minutes. Subsequent illumination decreases the dark conductivity by up to four orders of magnitude. The decrease is proportional to the illumination intensity and the time of exposure. A stable 'light-soaked' state can be achieved by strong illumination ($\sim$ 200 mW cm^{-2}) with white light for about four hours. There has been controversy over whether surface or bulk changes are responsible for the effect[105, 106]. Recently, discussion has centred around two 'bulk' models. One proposes that illumination increases the gap density of states through forming extra dangling bonds : the subsequent shift in E_F explains the conductivity change. Evidence for this comes largely from e.s.r. measurements[107, 108]. The alternative model proposes a shift in E_F due to a change in occupancy of the gap states. This could result from the light-induced formation of hole[109] or electron traps[110]. Although it is not clearly understood, the Staebler-Wronski effect must be taken into account when interpretating experimental data. Reproducible results can be obtained by carefully limiting the exposure to light.

2.7 Applications of Amorphous Silicon

The current interest in amorphous silicon for use in devices began soon after the successful doping of the hydrogenated form was reported in 1975[111]. Carlson and Wronski at RCA laboratories demonstrated the potential of α-Si:H as a solar cell material[112] and subsequently many research groups have worked in this area. Hydrogenated α-Si may be used as a cheap alternative to the expensive, single-crystal Si : it has a higher optical absorption coefficient, can be deposited in thin film form in large areas and has reasonable semiconducting properties. Various device configurations have been investigated including p-n junctions, p-i-n structures, Schottky barriers, heterojunctions and metal-insulator-semiconductor diodes. Some of these incorporate new materials, for example α-Si:F:H, which has a lower gap state density than α-Si:H and can be more easily doped[113], α-Si:C:H which has a bandgap between 1.76 and 2.2eV depending on C content and makes a very good window material[114], and α-Si:Ge:H alloys which also have a tailorable bandgap[115]. The highest reported efficiencies are currently in the range 8-9% for α-Si:C:H/α-Si:H heterojunctions, tandem cells of α-Si:Ge:H alloys and α-Si:F:H cells with small areas, typically a few tenths of a cm^2 (see (116) and references therein). Larger cells have lower efficiencies e.g. 5-6% for areas of 100 cm^2[116]. The maximum theoretical efficiency is ∿19%, although large scale commercial applications would be economically viable at efficiencies of 10% (for large area). The major difficulty lies in the poor minority carrier transport properties of α-Si:H films. Despite intense research, little improvement has been made in these material properties, most gains in cell efficiency coming from better and more complex cell designs. The more recent discovery of hydrogenated microcrystalline amorphous silicon[117, 118] may provide a way forward through improved carrier lifetimes. Despite the difficulties, α-Si:H solar cells have appeared on the commercial market in lower-power applications e.g. driving

LCD calculators, watches etc. and it would seem that more widespread use is imminent.

Field-effect experiments by Spear et al[47, 61] naturally led to the development of field-effect transistors (FETs) based on α-Si:H. Early devices had an on-off current ratio of $\sim 10^3$, an on-resistance of $\sim 10^7 \Omega$, and an off resistance of over $10^9 \Omega$[119], and it was suggested that they would be suitable for switching liquid crystal display (LCD) elements. Liquid crystal displays are attractive for large area applications because they consume little power and are easily visible in high ambient light conditions. However, it is difficult to multiplex large arrays. The use of an FET to drive each individual LCD element could, in principle, overcome this problem. Thin film, II-VI based FET's have been developed for this purpose[120] but α-Si:H offers a greater stability and ease of large area fabrication. Different FET geometries and dielectric materials have been used by different workers[121-123] and device characteristics have been improved (.e.g minimum on-off current ratio $\sim 10^4$). Conventional photolithographic techniques can be applied to α-Si:H with only minor modifications, and arrays of FETs have been made with promising results[124]. These FET structures may well be useful in a wider range of integrated circuits. Matsumara and Hayama have produced an I.C. inverter on α-Si:H[125]. Further work by Snell et al[126] has produced NOR and NAND circuits and the more complex bistable flip-flop and shift register. Although limited by their frequency response at present, these units could form the peripheral circuits of an α-Si:H FET LCD matrix addressing system.

The combination of high photoconductivity and high dark resistivity found in α-Si:H may be exploited in several ways. Matsumara et al[127] have proposed and fabricated an α-Si:H image sensor I.C., consisting of a photoconducting region, an MIS capacitor and an FET. Similar structures have been made by LeComber et al[124]. With the FET 'off', current flows through

the photoconducting region and charges up the capacitor. When the FET is switched 'on' the capacitor discharges, providing an output current whose magnitude is a function of the illumination intensity. An array of such cells with an appropriate clock pulse train to switch the FET's can be used to record one- or two-dimensional images. Shimizu et al[128] have demonstrated the use of α-Si:H as a photoreceptor in electrophotography. The main difficulty lies in producing films with a high enough resistivity ($\sim 10^{12} \Omega$ cm). This is achieved by using films with a high gap density of states[129] or by employing a p-i-n structure[128]. The advantages of α-Si:H over conventional materials such as α-Se are (1) its excellent photosensitivity over the whole visible range, (2) controllable electrical properties, (3) good mechanical properties and spatial homogeneity, and (4) non-toxicity. The high response of α-Si:H near 650 nm, corresponding to a He-Ne laser, implies its suitability for use in laser line printers. If the present relatively high cost of fabrication could be lowered, α-Si:H would seem certain to replace other materials currently in use. Similar properties are required for the production of vidicon tubes. The first such device, using the high gap DOS method for highly resistive α-Si:H, was reported by Imamura et al[130]. Shimizu et al[131], have made a vidicon based on the p-i-n structure. Again, the range and degree of spectral response and the high stability of α-Si:H seem to offer many advantages over conventional tubes.

Further applications which make use of layers of doped α-Si:H include digital memory and high current carrying devices. High speed switching has been reported in p-n-i structures deposited onto a conducting substrate[132]. These devices could be used as programmable, non-volatile memories and from early results would seem to be superior to current technology (MNOS and FAMOS) in terms of switching speed (<100ns), retention time (> several weeks), operating voltages (1-8V) and stability. Very high current densities

(> 20 mA cm^{-2}) have been observed in devices consisting of an n^+ layer a few hundred angstroms thick, a 1 μm lightly phosphorous doped region and a p^+ layer on a conducting substrate[133]. Typical rectification ratios were better than 10^4 at 1V forward bias. Although their performance is inferior to that of single crystal p-n junctions, they could be used as a cheap alternative where requirements are less stringent.

High density information storage could be achieved in α-Si:H using purely optical means[134]. The difference in optical transmission between amorphous and polycrystalline silicon is greater than 10^5. A laser could be used to selectively anneal an α-Si:H film, resulting in high density optical storage. This would enable a visible light readout with negligible degradation over repeated use.

CHAPTER 3

SCHOTTKY BARRIER AND TUNNELLING MIS THEORY

3.1 Introduction

The results presented later in this thesis deal with the electrical properties of Schottky barrier and tunnelling MIS devices. This chapter contains summaries of the relevant theoretical background needed for the analysis of these experimental data. The theory of Schottky barriers on single crystal semiconductor substrates is covered in the first section. The characteristics of α-Si:H Schottky diodes are discussed in section 3.3, which includes a review of the current models for such devices. The incorporation of a tunnellable insulating layer between the metal and the semiconductor can have advantageous effects on the device properties. Section 3.4 deals briefly with possible conduction mechanisms in thin films. The theory of MIS tunnelling devices is outlined in the next section. The chapter concludes with a discussion of one particular field of application, namely solar cells.

3.2 The Theory of Schottky Barriers on Single Crystal Semiconductors

3.2.1 Barrier Parameters

The formation of a Schottky barrier when a metal comes into contact with a semiconductor has been widely discussed and is documented in many standard textbooks (see, for example ref. (1)). In view of this, only the most important features of Schottky barrier theory will be outlined here.

Consider a metal and an n-type semiconductor with work functions ϕ_M and ϕ_s respectively (the work function is the escape energy of an electron with energy corresponding to the Fermi level of the material). If $\phi_M > \phi_s$ then before contact is made the semiconductor Fermi level lies above that of the metal. On making contact, electrons flow from the semi-

conductor to the metal, and equilibrium is established when the Fermi levels on both sides line up. In equilibrium the semiconductor bands in the interface region are bent as shown in Fig. 3.1. (It should be noted that a barrier with similar properties on a p-type semiconductor would require that $\phi_M < \phi_S$.) In the absence of surface states the bands are bent upwards by an amount

$$eV_o = \phi_M - \phi_S \tag{3.1}$$

where V_o is known as the diffusion potential or built-in voltage. The barrier height, ϕ_B, seen by electrons travelling from the metal to the semiconductor is given by

$$\phi_B = \phi_M - \chi_S \tag{3.2}$$

(neglecting Schottky lowering), where χ_S is the semiconductor electron affinity. The difference between ϕ_S and χ_S gives the energy difference between the Fermi level and the bottom of the conduction band, ξ.

The bending of the bands means that the surface region of the semiconductor is depleted of majority carriers. Their removal leaves the fixed ionised donors uncompensated, so that in this so called 'depletion region' there is a net positive space charge. This is balanced by a negative charge on the metal surface which consists of extra conduction band electrons in a layer ~ 0.5 Å thick. The width of the depletion region in the semiconductor is much greater, since the donor concentration is many orders of magnitude less than the concentration of electrons in the metal. It is generally assumed that the depletion region has an abrupt ending (the depletion approximation). Within this region all of the donors are ionised and the space charge is entirely due to their uncompensated charge. At the edge of the depletion region the space charge density

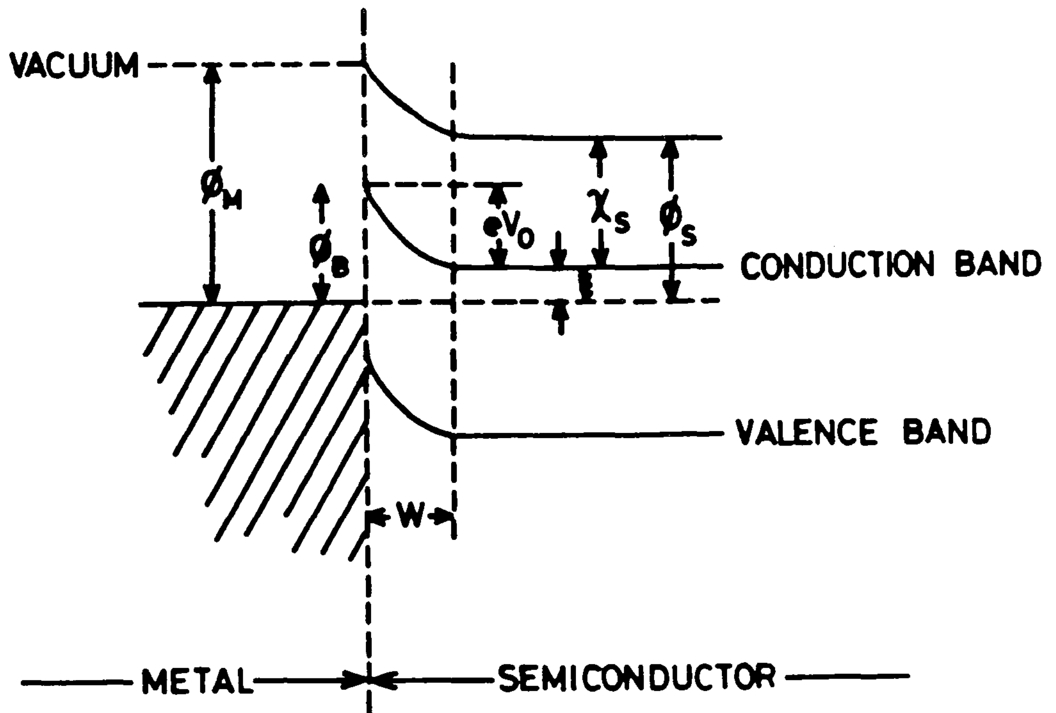


Fig. 3.1 Energy band diagram of metal- (n-type) semiconductor contact at thermal equilibrium.

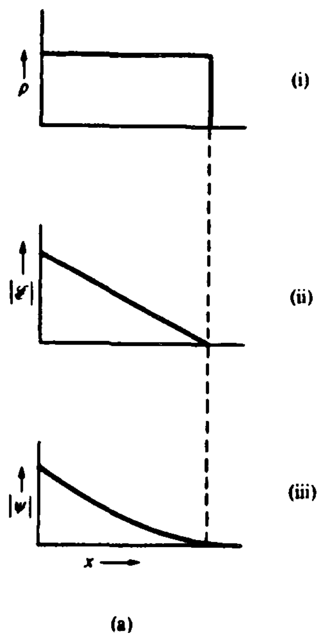


Fig. 3.2 Spatial variation of (i) charge density, (ii) electric field strength and (ii) electrostatic potential in a Schottky barrier. For an n-type semiconductor, ψ is negative and the electron potential energy ($-q\psi$) is positive.

abruptly falls to zero. In this case the shape of the barrier is determined by the distribution of donors. If the doping density is uniform throughout the semiconductor then the uncompensated donors give rise to a uniform space charge (see Fig. 3.2(a)). The electric field strength increases linearly from the edge of the depletion region to a maximum at the interface, and the electrostatic potential rises quadratically (Fig. 3.2(b) and (c)). The barrier profile is parabolic. The width of the space charge layer, W, may be calculated using Poisson's equation to be

$$W = \left[\frac{2\varepsilon_o \varepsilon_s}{eN_d} \cdot \left(V_o - V - \frac{kT}{e} \right) \right]^{\frac{1}{2}} \qquad (3.3)$$

where N_d is the uniform doping density. The capacitance associated with this layer (per unit area) is also voltage dependent and is given by

$$C = \left[\frac{\varepsilon_o \varepsilon_s \; eN_d}{2(V_o - V - kT/e)} \right]^{\frac{1}{2}} \qquad (3.4)$$

All practical devices invariably contain an interfacial layer between 10 and 20 Å thick as a result of sample preparation. However, this does not necessarily greatly affect the properties of the barrier if electrons can easily tunnel through it, that is, providing the voltage drop across the oxide is small the barrier height is still given by equation 3.2. On the other hand, the presence of surface or interface states can have a more pronounced effect on the barrier height. Surface states are allowed energy levels in the forbidden gap situated at the surface of a semiconductor crystal. They arise because of the interruption in the periodicity of the lattice. In chemical terms each surface atom can be thought of as having one unpaired electron; the electron occupies a localised orbit at right

angles to the plane of the surface and this is called a dangling bond. Such dangling bonds can be either donor-like (i.e. positively charged when empty) or acceptor-like (negatively charged when filled) in nature. In either case these are intrinsic surface states i.e. they are a property of an ideal free surface. States may also arise as a result of impurities (e.g. adsorbed gases or liquids) or defects at the surface of a crystal and these are known as extrinsic surface states.

Charge stored in surface states (either positive or negative) alters the band bending in the semiconductor. If the density of surface states is high enough then the extent of the space charge region in the semiconductor, and hence the barrier height will be determined not by the metal work function, but by the charge density associated with the surface states. Bardeen has introduced the concept of a neutral level ϕ_o for these states[2]: the states must be filled up to this level for the surface to be electrically neutral. Considering a semiconductor surface in isolation, the occupation of the surface states is governed by the bulk semiconductor Fermi level. If E_F does not coincide with ϕ_o then the surface is charged and the bands will be bent. In this case, when a metal is applied the extra charge associated with the contact potential (i.e. work function difference) may be taken up by the high density of surface states, without affecting the position of E_F appreciably. The barrier height is thus determined by the nature of the semiconductor surface and not by ϕ_M, and the Fermi level in the semiconductor has been 'pinned' relative to the band edges by the surface states. This extreme situation can occur in practice, although it is more usual to find that in general ϕ_B is dependent on both the metal work function and the surface state density.

3.2.2 Current Transport Mechanisms

Given the existence of a Schottky barrier there are a number of possible ways in which carriers can cross it. These are summarised

schematically in Fig. 3.3. They are (a) emission of electrons over the barrier from the semiconductor to the metal (b) quantum-mechanical tunnelling through the barrier, (c) recombination in the space charge region and (d) recombination in the neutral region (hole injection). Of these, process (a) leads to almost ideal Schottky diodes: the other mechanisms represent departures from ideality.

(a) Emission over the barrier

In order to pass over the barrier, electrons must travel from the semiconductor bulk to the interface. During the transition their motion is governed by (1) drift and diffusion under the influence of the electric field in the depletion region and (2) the height of the barrier at the interface. The current will be limited by whichever process is most restrictive to electron transport. The two theoretical extremes have both been studied: Schottky[3] assumed that diffusion and drift were the limiting processes, and Bethe[4] attributed the control of the current flow to the barrier height. Cromwell and Sze[5] have subsequently combined the theories to formulate a more general explanation of Schottky barrier behaviour. The salient features of these theories will now be summarised.

(i) The Diffusion Theory. In formulating this theory the following assumptions are made: (1) the barrier height ϕ_B is much greater than kT, (2) electron collisions dominate the transport in the depletion region, (3) the carrier concentrations at the barrier and the depletion region edge are unaltered by the current flow, (4) the impurity concentration of the semiconductor is non-degenerate i.e. it is not heavily doped, and (5) the charge carrier mobility is constant. The effects of image forces are also neglected. The forward bias current density obtained using this approach is

$$J = J_o \left[\exp\left(\frac{eV}{kT}\right) - 1 \right] \qquad (3.5)$$

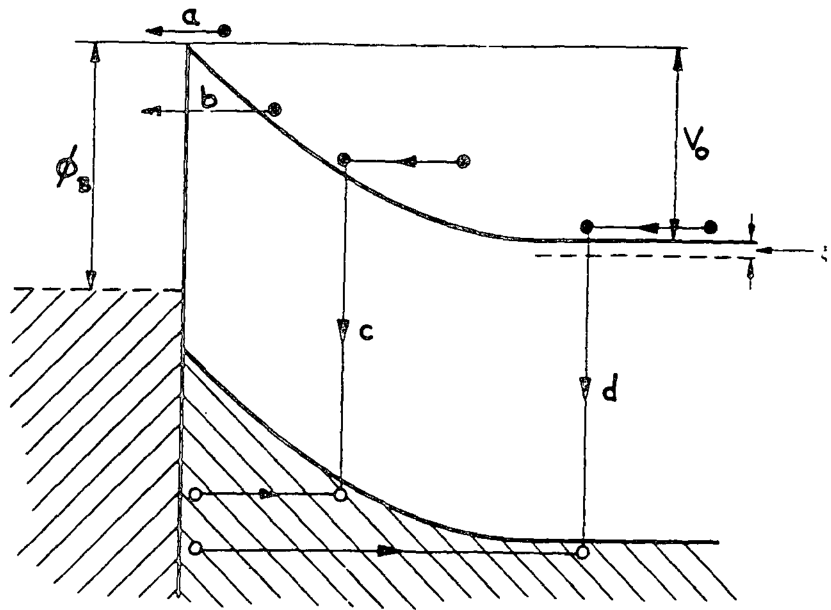


Fig. 3.3 Transport processes in a forward-biased Schottky barrier

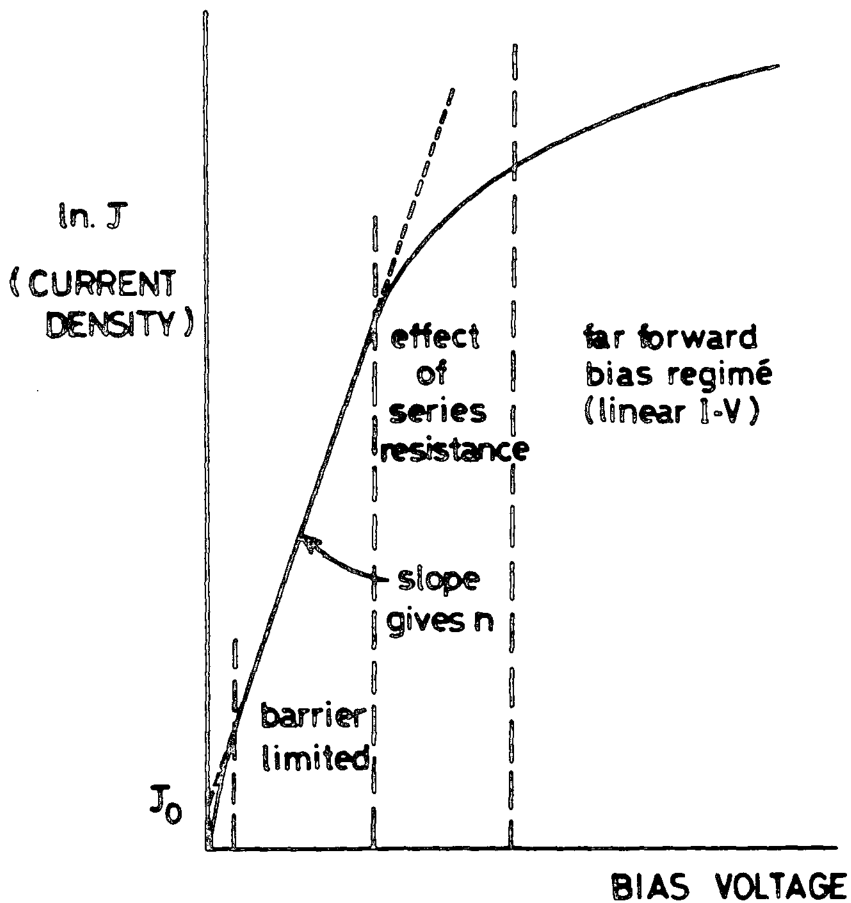


Fig. 3.4 Typical J-V curve (schematic) showing the various bias regimes.

where

$$J_o = \frac{e^2 D_n N_c}{kT} \left[\frac{2e\,(V_o - V)\,N_d}{\varepsilon_o\,\varepsilon_s} \right]^{\frac{1}{2}} .\exp\left(\frac{-e\phi_B}{kT} \right) \qquad (3.6(a))$$

$$= e\mu\ N_c\ E_s\ \exp\left(\frac{-e\ \phi_B}{kT} \right) \qquad (3.6(b))$$

and is known as the reverse saturation current density. N_d is the ionised donor concentration, N_c the effective conduction band density of states and D_n the diffusion coefficient for electrons whose mobility is μ. V is the applied bias voltage, and ε_s the permittivity of the semiconductor. E_s is the surface field in the semiconductor. Diffusion theory is thought to apply to low mobility semiconductors e.g. amorphous materials, although it should be noted that there is little definitive proof of this.

(ii) Thermionic Emission Theory. In this approach the electron collisions within the barrier region are neglected, making the shape of the barrier profile irrelevant as the transport depends only on its height. Apart from this, the basic assumptions are the same as for the diffusion theory. The forward bias current density is given by a similar expression

$$J = J_o \left[\exp\left(\frac{eV}{kT} \right) - 1 \right] \qquad (3.7)$$

but J_o in this case is

$$J_o = A^* T^2 \exp\left(- \frac{e\phi_B}{kT} \right) \qquad (3.8)$$

A^* is the Richardson constant for thermionic emission. The saturation current density for thermionic emission is more sensitive to temperature than the saturation current density for diffusion theory, however, J_o

(thermionic emission) is ideally voltage independent whereas J_o (diffusion theory) varies as $|V|^{\frac{1}{2}}$ approximately. Thermionic emission theory appears to adequately explain the behaviour of Schottky diodes on high mobility semiconductors, e.g. Si, Ge, GaAs providing the forward bias is not too large. Even relatively low mobility semiconductors such as GaP and CdS seem to exhibit thermionic-emission(6).

(iii) Thermionic Emission-Diffusion Theory. Crowell and Sze(5) have combined the two theories outlined above by introducing a recombination velocity, V_r, near the interface. This parameter may be defined by equating the net electron current into the metal to $eV_r(n-n_o)$ where n_o is the equilibrium electron density at the top of the barrier and n is electron density at the same point with a bias voltage applied. Their analysis produces the following current-voltage expressions

$$J = J_o \left[\exp\left(\frac{eV}{kT}\right) - 1 \right] \tag{3.9}$$

and $$J_o = A^{**} T^2 \exp\left(\frac{-e\phi_B}{kT}\right) \tag{3.10}$$

where $$A^{**} = \frac{f_P f_Q A^*}{\left(1 + f_P f_Q \cdot V_r/V_D\right)} \tag{3.11}$$

A^{**} is the effective Richardson constant, f_P and f_Q are the probability of electron emission over the barrier and the quantum mechanical transmission coefficient respectively and V_D the effective velocity due to drift and diffusion of electrons.

(b) Other Mechanisms

Processes (b), (c) and (d) may be considered together, in that they all cause departures from ideal diode behaviour. Under given circumstances it may be possible for carriers with energies less than ϕ_B to tunnel through the barrier. At low temperatures, or in heavily doped semiconductors, this tunnelling current may become dominant.

Recombination in the depletion region normally takes place via the localised states. Those states lying near midgap are the most effective recombination centres. The recombination current is given by[1]

$$J = J_o \left[\exp\left(\frac{eV}{2kT}\right) - 1 \right] \tag{3.12}$$

where
$$J_o = \frac{e n_i W}{2\tau_r} \tag{3.13}$$

n_i is the intrinsic electron concentration which is proportional to $\exp(-eE_g/2kT)$, W is the depletion region width and τ_r the carrier lifetime within the depletion region. The other recombination current component occurs when the barrier height is greater than half the bandgap. This is often the case, and the resultant band bending makes the semiconductor surface p-type. Under forward bias, a number of these holes might be expected to diffuse into the bulk semiconductor and recombine there, introducing yet another current component and further complicating the analysis of experimental data.

3.2.3. Practical Diode Characteristics

(a) Forward current characteristics

Experimentally, it is found that the forward currents of Schottky barriers deviate from the ideal form, as expressed in equations 3.5 and

3.7. Results may be fitted to a modified equation

$$J = J_o \left[\exp\left(\frac{eV}{nkT}\right) - 1 \right] \tag{3.14}$$

where J_o is the saturation current density obtained by extrapolating the log-linear I-V plot to V=0, and n is the diode ideality factor given by

$$n = \frac{e}{kT} \left(\frac{\partial V}{\partial(\ln J)} \right) \tag{3.15}$$

The value of n can be obtained from the slope of the ln J-V graph: a value of unity indicates an ideal Schottky diode. For bias voltages $> \frac{3kT}{e}$ equation 3.12 reduces to

$$J \sim J_o \exp\left(\frac{eV}{nkT}\right) \tag{3.16}$$

and it is this relation which is often plotted experimentally.

The ideal equations assume a bias independent barrier height, a condition which is not fulfilled in practice. Even in an 'ideal' diode the barrier height is modified, as a result of image forces, by an amount which depends on the bias voltage. Moreover, real diodes invariably contain an interfacial layer which also leads to a bias dependence of the barrier height (the consequences of having an interfacial layer between the metal and the semiconductor are discussed more fully in section 3.5). Both of these effects influence the J-V characteristic, resulting in ideality factors greater than unity. A further complication arises from the fact that most diodes exhibit temperature dependent ideality factors. This cannot be explained in terms of the effects described above. The following empirical law has been derived[7, 8]:

$$J = AT^2 \exp\left[\frac{-\phi_B}{k(T + T_o)}\right]\left\{\exp\left[\frac{eV}{k(T + T_o)}\right] - 1\right\} \quad (3.17)$$

where T_o is known as the excess temperature. It is constant with bias and over a wide range of temperatures. At any temperature n can be related to T_o by the expression

$$n = 1 + \frac{T_o}{T} \quad (3.18)$$

However, the effect is not an intrinsic property of an ideal Schottky diode. The fact that T_o values vary widely for different devices (produced on the same semiconductor substrate) indicates that it is probably an artefact of the surface preparation. This temperature dependence has been attributed variously to tunnelling, distributions of surface states and non-uniform doping of the surface region. Any combination of these is also possible.

A typical ln J-V plot for a Schottky diode is shown schematically in Fig. 3.4. Such a graph provides a large amount of data on the diode parameters. Firstly, from the linear portion of the curve the ideality factor can be calculated using equation 3.13. The extrapolation of the linear region to zero bias yields the saturation current density J_o. From this value the barrier height may be calculated using either thermionic emission theory (equation 3.8) or diffusion theory (equation 3.6) providing the relevant constants are known. It should be noted that the determination of barrier heights using this method is only reliable if the ln J-V plot is a good straight line, with an n-value reasonably close to unity e.g. $n < 1{,}1$. In other cases, where the diode is far from ideal the barrier height is not clearly defined.

Deviations from linearity occur in forward bias, usually as a result of the diode series resistance R_s. The sample resistance consists of the series combination of the barrier resistance R_b and the series resistance R_s (arising from the resistance of the bulk substrate and the back contact). The voltage applied to the sample is simply divided between these two resistances. At small forward bias voltages $R_b >> R_s$ and the voltage dropped across the neutral region of the semiconductor is negligible. As the forward bias is increased an increasing proportion of the applied bias will fall across the series resistance i.e. the voltage across the barrier will be less than the apparent applied voltage. A plot of applied voltage v current will deviate from the straight line behaviour predicted by theory. At a high enough forward bias, when the semiconductor bands are flattened, the disappearance of the depletion region leaves only the series resistance. At this point the J-V graph becomes linear and R_s can be obtained very simply from the reciprocal slope. Goodman[8] has analysed this region with the aim of finding the built in potential V_o. He points out that for a given diode current and voltage, an increase in the current by a factor of e requires an applied voltage charge of $^{kT}/_{e}$ across the barrier (see equation 3.5) plus the consequent voltage drop across the bulk resistance. He also shows that since kT/e at room temperature is very small compared with the voltage dropped across the series resistance, this factor may be neglected without serious error. In this case any applied voltage in excess of the diffusion potential V_o (which is required to flatten the bands) is dropped across R_s. The J-V relationship, to a first approximation, is given by

$$J \simeq \frac{V - V_o}{R_s} \qquad (3.19)$$

Hence a linear plot of J against V should be a straight line in this region, and extrapolating back to the voltage axis (i.e. J=0) gives the (approximate) diffusion potential, V_o directly.

(b) Reverse current characteristics

The thermionic-emission theory predicts that the reverse current should saturate at the value $J_o = A^*T^2 \left(\frac{-e\phi_B}{kT}\right)$. Diffusion theory on the other hand predicts a rise in the reverse current with a $V^{\frac{1}{2}}$ dependence. In practice most barriers show non-saturating reverse characteristics, but the $V^{\frac{1}{2}}$ law is not always seen. Various factors can contribute to these deviations from ideality. As in the case of the forward current a bias dependent barrier height due to image force lowering or an interfacial layer will have an effect. Image force lowering results in a reverse current which is proportional to $V^{\frac{1}{4}}$ for large reverse bias. The tunnelling of carriers through the barrier is of greater significance in reverse bias because of the larger fields involved. The field reduces the thickness of the barrier, increasing the likelihood of tunnelling contributing to the current flow. If the barrier height is large and the semiconductor has a low carrier lifetime, an appreciable increase in the reverse current may occur due to the generation of electron-hole pairs in the depletion region. This current component increases in proportion to the width of the depletion region[1] and is most evident at low temperatures. Because of the complicated nature of reverse bias conduction, which often involves several of these different current components, it is difficult to obtain much definitive information from reverse bias data.

(c) Capacitance Characteristics

The depletion region of a Schottky barrier behaves in some respects like a parallel plate capacitor. The application of a bias voltage (forward or reverse) changes the band bending and hence the width of the semiconductor

depletion region. The accompanying change of charge results in a change in capacitance. In a single crystal semiconductor where the space charge is entirely due to the ionised impurity atoms (i.e. neglecting the free carrier contribution) we recall that the capacitance per unit area is given by

$$C = \left[\frac{\varepsilon_o \varepsilon_r \, e \, N_d}{2(V_o + V_r - kT/e)} \right]^{\frac{1}{2}} \tag{3.20}$$

for an n-type material where N_d is the ionised donor density and V_r is the applied reverse bias voltage. Rearranging equation 3.20 gives

$$\frac{1}{C^2} = \left(\frac{2}{\varepsilon_o \varepsilon_r \, e \, N_d} \right) (V_o + V - kT/e) \tag{3.21}$$

The kT/e term is quite often omitted from this expression : this is equivalent to making the depletion approximation. A plot of $\frac{1}{C^2}$ against bias voltage should yield a straight line, providing the donor concentration is uniform throughout the space charge region. The intercept of this line on the voltage axis gives the built in voltage, V_o, and the slope gives N_d. This is a very commonly used method for measuring these parameters. Even if N_d is not constant, the slope at any point still yields N_d at the edge of the depletion region, enabling doping profiles through a material to be measured. Ideally the $\frac{1}{C^2}$ v V plot would not alter with frequency (providing the measuring frequency was less than reciprocal of the dielectric relaxation time). In practice, interface states, bulk traps and the presence of an interfacial layer (see section 3.5) can give rise to a frequency-dependent diode capacitance. A graph of $\frac{1}{C^2}$ v V may also be non-linear as a result of these effects.

3.3 Schottky Barriers on Hydrogenated Amorphous Silicon

3.3.1 Current - Voltage Characteristics

Schottky barriers on α-Si:H generally follow the modified diode equation (eq. 3.14) applicable to single crystal semiconductors. The question as to which theory of Schottky barrier current transport is applicable to α-Si:H is as yet unresolved. The underlying similarity between the diffusion theory (DT) and the thermionic emission theory (TET) makes the distinction difficult. Comparing equations 3.4(b) and 3.8 it can be seen that the current voltage curves differ only by the pre-exponential factor J_o. In principle however, it is possible to distinguish between the two mechanisms by means of the temperature dependence of the reverse saturation current. For DT a graph of $\ln J_o$ v $1/T$ should give a straight line whereas a $\ln J_o/T^2$ v $1/T$ plot is linear for TET. Problems arise experimentally because of the very low current levels measured in α-Si:H. This restricts the temperature range over which measurements can be taken[10].

Because of the low carrier mobility in α-Si:H one might assume that DT is more applicable, as have Wronski et al[11, 12]. Alternatively Wilson and McGill[13], whilst acknowledging that DT may be the correct method of analysis, claim that the application of TET involves fewer assumptions and gives essentially the same results. More rigorous studies have been undertaken by Mishima et al[14], Deneuville and Brodsky[10] and by Thompson et al[15], but with varying conclusions. Mishima et al[14] have investigated the temperature coefficient of the barrier height, comparing the results with ϕ_B obtained directly from internal photoemission measurements and also the agreement between measured and theoretical n values. They conclude that diffusion theory dominates in α-Si:H Schottky barriers. Deneuville and Brodsky[10] found the temperature dependence of J_o in their diodes to be inconclusive, but infer the presence of thermionic emission from the injection properties of the α-Si:H in a transistor structure[16]. Similarly,

Thompson et al[15] favour TET as the dominant mechanism at room temperature from their experiments on sputtered α-Si:H.

Clearly more work needs to be done in this particular area. At the present time, the approach of Wilson and McGill[13] would seem to be the most appropriate, given that calculations of ϕ_B using DT and TET are indeed very similar. For the purposes of comparing barrier heights this uncertainty makes very little difference, providing one is consistent.

3.3.2 Capacitance Characteristics

In the case of α-Si:H Schottky diodes the variation in capacitance with applied voltage does not follow the simple equations presented in section 3.2.3. The fundamental difference is that the net space charge in the depletion region is determined not just by ionised donors which may be present, but also by the localised state distribution within the mobility gap. Because the gap density of states varies considerably with energy, the gap state contribution to the capacitance will also be energy dependent. It may also be position dependent i.e. the distribution may change throughout the sample, though this is usually assumed not to be so. The overall effect of these complications is to produce a capacitance which is dependent on both the barrier energy and the width of the barrier region.

Fig. 3.5 shows the situation in the surface region of a metal n-αSi:H Schottky contact. The metal has a high work function causing band bending at the semiconductor surface as shown. As a result of the surface band bending some of the localised states which are below the Fermi level in the bulk are raised above the Fermi level in the depletion region. This is equivalent to a change in occupancy of the elevated states. It is assumed that the Fermi level remains flat throughout the depletion region, and that any applied bias is dropped across the semiconductor-metal interface. On the application of a small a.c. signal

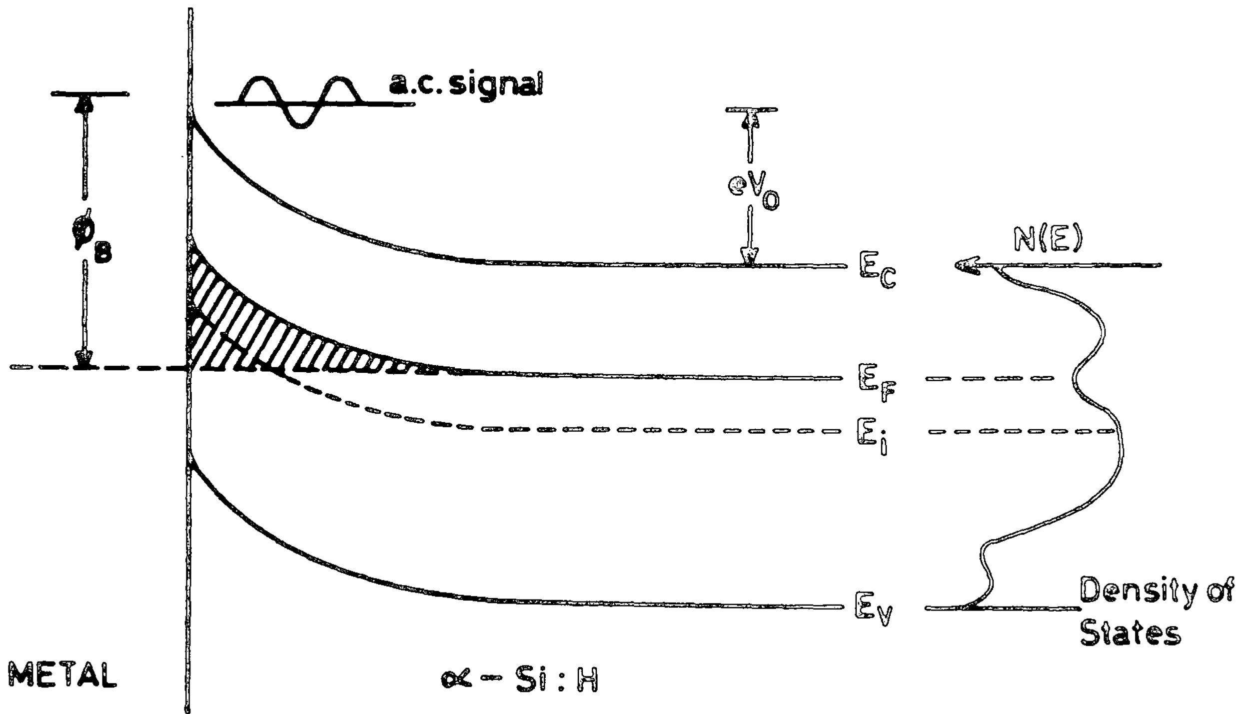


Fig. 3.5 Energy band diagram for a metal - n α-Si:H Schottky barrier. The density of states is also shown. The hatched area represents the region of energy and space occupied by states that have been pulled above E_F at the barrier.

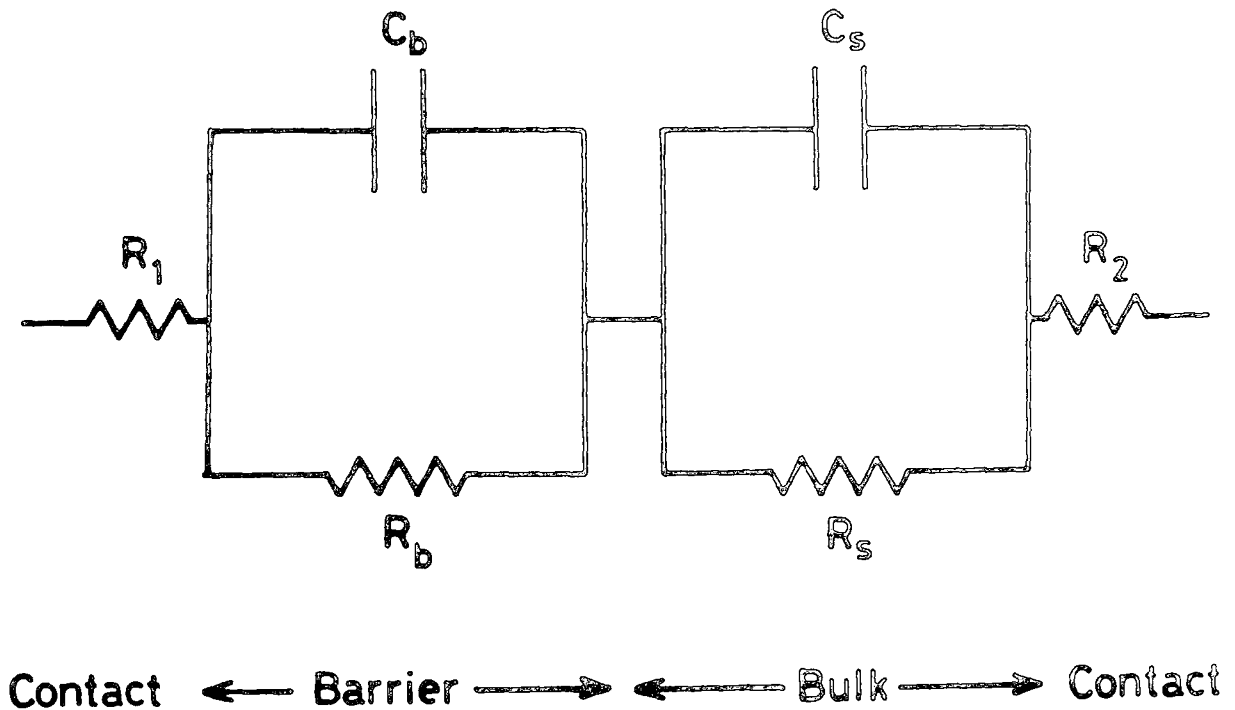


Fig. 3.6 The equivalent circuit for a Schottky barrier for capacitance-frequency measurements.

the Fermi level is moved up and down, in sequence with the signal. During the first cycle this means that some states are raised above the Fermi level. Whether they change their occupancy depends on whether they can respond i.e. empty during the signal period. If they can do so, they will contribute to the capacitance of the system. In α-Si:H, with its continuous distribution of localised gap states, the density of states crossing E_F at any time in response to an a.c. signal depends on the band bending, which in turn is a function of the applied bias. Hence the gap density of states can be related to the capacitance of the device. Unfortunately, the relationship between the two is far from simple. The response time (or lifetime), τ, of the states is dependent on their position in the mobility gap. Therefore at different positions throughout the depletion region the states crossing E_F will have different time constants. For thermal relaxation only

$$\tau = \tau_o \exp (E_c - E_s)/kT \qquad (3.22)$$

where E_c is the conduction band edge energy, E_s is the energy of the state and τ_o is a constant. In crystalline silicon τ_o has a value of $\sim 10^{-13}$ secs[17]. Any theory of the capacitance of an α-Si:H Schottky diode must take into account the lack of response of some of the states. The usual assumption, which in the case of α-Si:H is a good one, is that all the states with $\tau < \frac{1}{f}$ (f = frequency of measuring signal) do relax and contribute to the capacitance, whereas those with $\tau > \frac{1}{f}$ make no contribution at all. The exponential variation of τ with energy means that this 'cut-off' is very sharp indeed. Contact effects must also be considered as a contributing factor to the measured device capacitance and resistance. The commonest approach is to split the device into two regions, the barrier and the bulk, each represented by a separate parallel R-C network, as shown

in Fig. 3.6. Contact resistances are added in series to complete the model.

3.3.3. A Review of Theoretical Models

(a) Spear et al

The earliest attempt to analyse small signal capacitance data on α-Si:H Schottky diodes came from the Dundee group[18-20]. They made use of the lifetime approximation and the equivalent circuit described above. Starting from their density of gap states, determined experimentally using the field effect technique, they calculated the barrier profile by solving Poisson's equation. Allowing for the partial response of the states by a 'cut-off' procedure, they calculated the device capacitance using the equation for the barrier capacitance due to Roberts and Crowell [21]

$$C = \frac{\varepsilon_o \varepsilon_r \rho(V_o)}{Q} \qquad (3.23)$$

$$Q = \left[2\varepsilon_o \varepsilon_r \int_0^{E_s} \rho(E)\, dE \right]^{\frac{1}{2}} \qquad (3.24)$$

ε_r is the relative permittivity of α-Si:H.

To explain their experimental measurements these authors found it necessary to include the effects of the device equivalent circuit. Neglecting the contact resistances (see Fig. 3.6) the frequency response of the circuit may be expressed in the equations

$$C = \frac{R_b^2 C_b + R_s^2 C_s + \omega^2 R_b^2 R_s^2 C_b C_s (C_b + C_s)}{(R_b + R_s)^2 + \omega^2 R_b^2 R_s^2 (C_b + C_s)^2} \qquad (3.26)$$

$$G = \frac{R_b + R_s + \omega^2 R_b R_s (R_b C_b{}^2 + R_s C_s{}^2)}{(R_b + R_s)^2 + \omega^2 R_b{}^2 R_s{}^2 (C_b + C_s)^2} \qquad (3.27)$$

For frequencies less than 10^3 Hz the frequency dependent terms may be neglected compared with the others. In this range $C = C_b$ and $G = \frac{1}{R_b}$ i.e. the true barrier properties will be measured, providing $R_b >> R_s$ which will be true in reverse and small forward bias. As the forward bias is increased R_b falls rapidly such that $R_b << R_s$ and $C \rightarrow C_s$ while $G \rightarrow \frac{1}{R_s}$. At frequencies greater than 10^3 Hz the measured capacitance should approach the geometrical capacitance i.e.

$$C = C_G = \frac{C_b C_s}{C_b + C_s} \qquad (3.27)$$

This fall in C from C_b to C_G occurs at a frequency

$$\omega = \frac{R_b + R_s}{R_b R_s (C_b + C_s)} \qquad (3.28)$$

The C-ω, G-ω results of the Dundee group are reproduced in Fig.3.7. The rise in C at low frequencies has been attributed to the increasing response of deeper lying gap states. Apart from this good agreement is observed between theory and experiment. The conductance graph shows a sharp rise at high frequencies. Snell et al[15] have fitted these data by including the effects of contact resistance in their model. According to their calculations this rise in G occurs at a frequency $\omega = \frac{1}{R_c C}$ enabling the total contact resistance R_c to be determined.

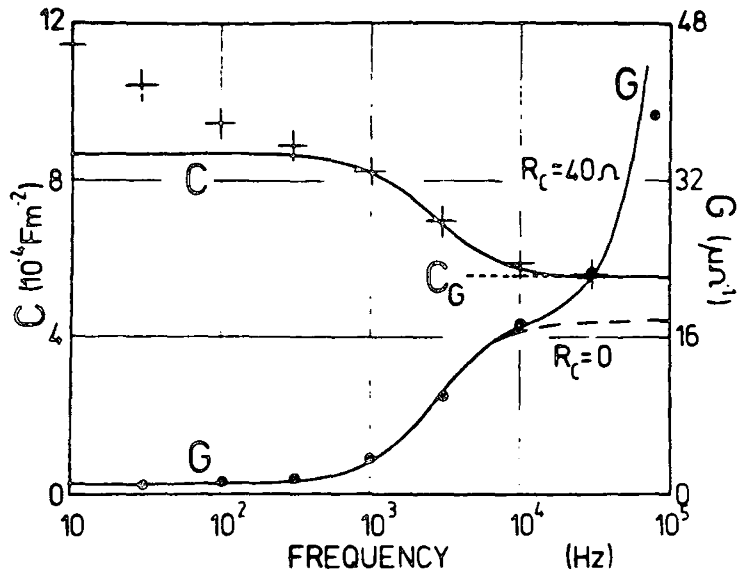


Fig. 3.7 C-w, G-w data as reported by Snell et al[19]. The solid curves are theoretical, the points are experimental.

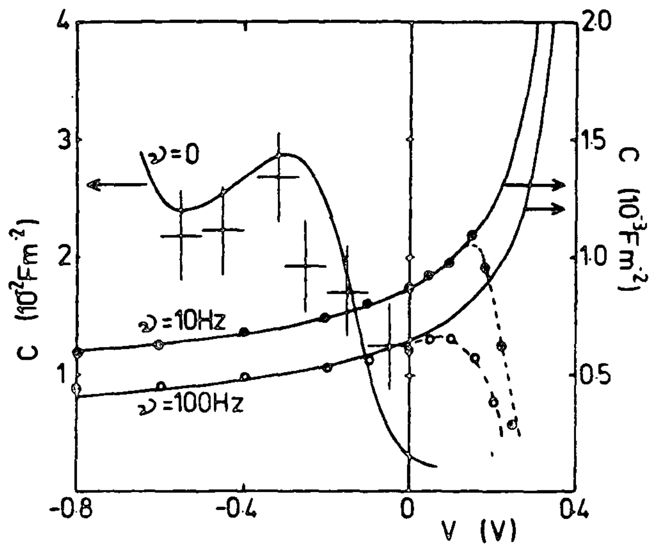


Fig. 3.8 Theoretical and experimental capacitance-voltage data (denoted by solid lines and points respectively). See ref (19).

The capacitance voltage curves from this group are shown in Fig.3.8. Again, their simple theory adequately explains the experimental data. The fall off in C at forward bias is explained in terms of the series resistance. The behaviour of the barrier capacitance is noticeably unlike that of crystalline Schottky barriers. It should,however be pointed out that this theory only explains data measured on undoped (intrinsic) α-Si:H : it fails to predict the behaviour of doped films. According to theory, the capacitance maximum should move towards higher V_F as $(E_C - E_F)$ is decreased. The opposite trend is observed in practice[19,20]. Also the experimental results reported by this group have not been reported by any other group. This may be due to the different measuring system they have used, namely an a.c. bridge as opposed to the phase sensitive techniques employed by other workers.

(b) Beichler et al

Beichler et al[22] performed a very similar analysis on their data. They assumed a barrier shape on the basis of the depletion approximation and also a constant density of gap states. Their analysis centred on the frequency response of the device capacitance, and their results are shown in Fig. 3.9. This simple model could adequately explain the results on intrinsic α-Si:H, but the data for doped material proved difficult to analyse. It was noted that the device capacitance increased with falling frequency and that no saturation was observed, even at frequencies of 10^{-3} Hz. Their C-V data, shown in Fig.3.10, exhibit some interesting features. Firstly, they found that C decreased with increasing reverse bias at all frequencies used, in contrast to Snell et al[19,20]. They attribute this to a different spectrum of response times for the gap states. There is also a very sharp rise in C for forward bias voltages greater than about 0.3V. The authors have tentatively attributed this to the contribution of interface states: they estimate a density of $\sim 10^{13}$ cm^{-2} eV^{-1} states contributing to the device capacitance.

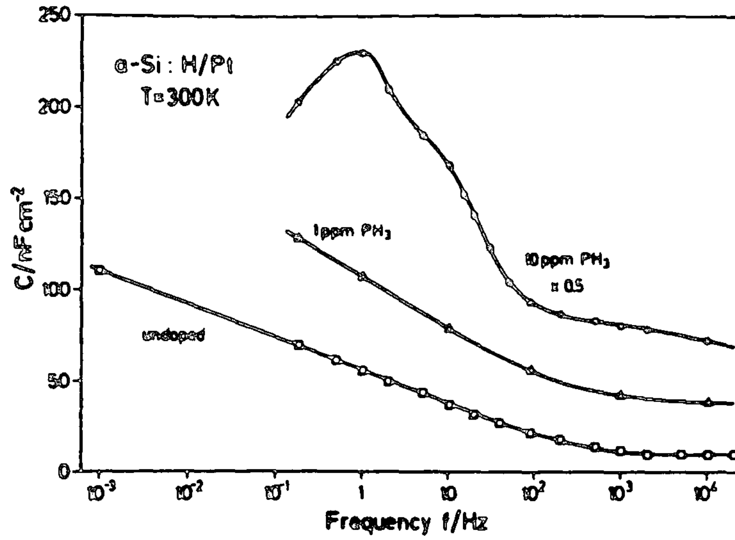


Fig. 3.9 Frequency dependence of the capacitance for differently doped Schottky diodes (after Beichler et al (22)).

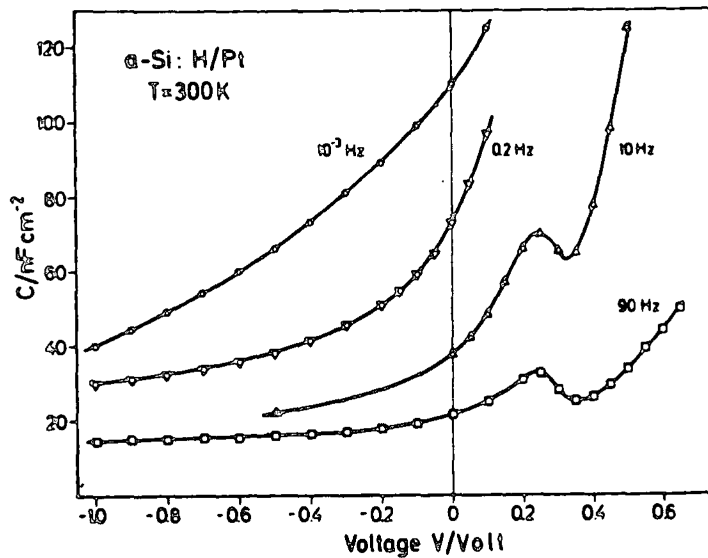


Fig. 3.10 C-V characteristics of an undoped α-Si:H Schottky diode at different frequencies (see ref. (22)).

(c) Viktorovitch et al

Both of the theories presented so far attribute the frequency dependence of the capacitor to the spread of lifetimes of the gap states. The rest of the diode, i.e. the bulk semiconductor and contacts, is assumed to be significant at high frequencies or in doped samples. Several other approaches have been used. Viktorovitch and co-workers[23-25] have defined a characteristic distance, x_i, from the metal-semiconductor interface, using the time dependence of the gap state response at different depths below E_c. For a given temperature and frequency x_i is unique and is such that for $x > x_i$ all the states can follow the a.c. measuring signal, whereas for $x < x_i$ none of the states can respond. By splitting the depletion region into n very thin slices, each represented by an R-C circuit, they have arrived at an equivalent circuit (see Fig. 3.11) which enables x_i to be determined. They have attempted to associate different parts of the circuit with specific mechanisms in the diode, and have introduced the possibility of an interface state contribution, stressing the importance of distinguishing between bulk and interface state effects. Assuming a constant density of states the analysis gives the frequency dependence of the zero-bias capacitance as

$$C(\omega) = \frac{\varepsilon}{L_o}\left[1 + \ln\left(\frac{e|V_o|/kT}{1 + \ln(\omega/\omega_o)}\right)\right]^{-1} \qquad (3.29)$$

where $$L_o = \left(\frac{\varepsilon}{eN_o}\right)^{\frac{1}{2}} \qquad (3.30)$$

ω_o is a constant and L_o is the Debye length associated with the bulk states whose density is N_o ($cm^{-3}\ eV^{-1}$). Viktorovitch has fitted his C-ω data to this theory using a value of $\tau_o \approx 10^{-17}$s, and has estimated a

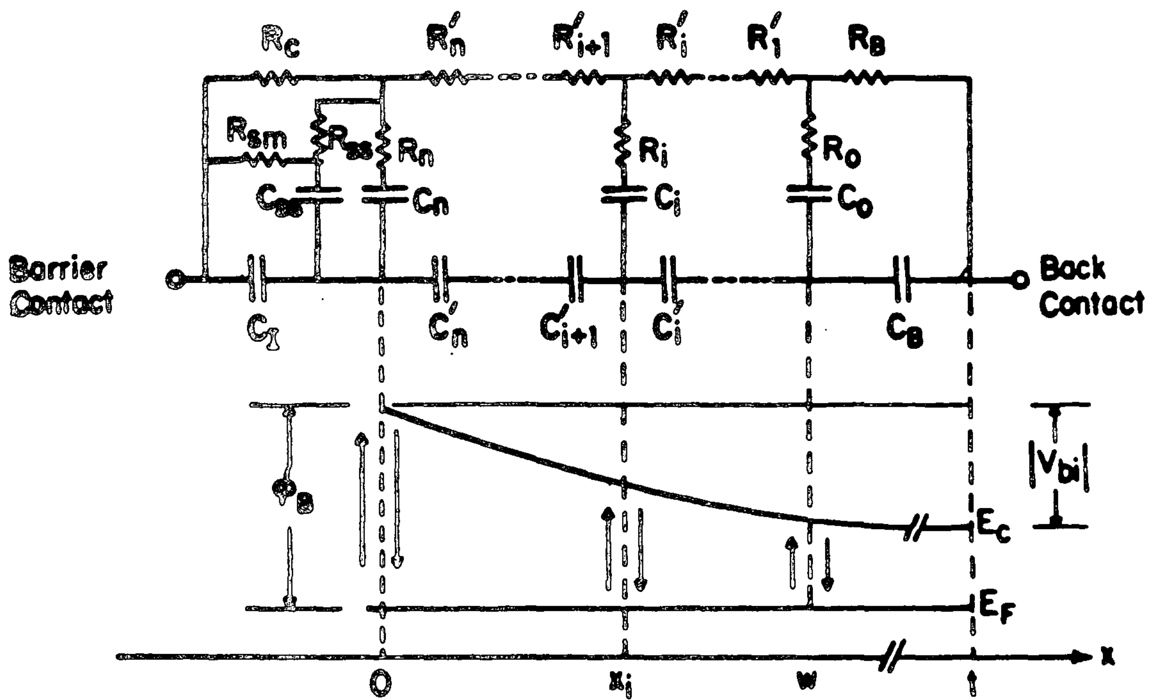


Fig. 3.11 General equivalent circuit for an MIS device. In the case of a Schottky diode C_I is infinite. Interaction between the states at the Fermi level and the conduction band is illustrated by the arrows in the partial energy-band schematic representation below the circuit diagram (after Viktorovitch (25)).

surface state density at midgap of $\sim 10^{13}$ cm^{-2} eV^{-1}. Because of the surface state contribution Viktorovitch claims that no bulk state information can be extracted from capacitance-voltage data. The analysis has also been extended to the conductance of Schottky barrier and MIS devices. However, the assumption of a sharply defined cut off between states contributing to the device conductance and those which do not contribute is rather arbitrary.

(d) Abram et al

Abram and Doherty(26) have approached the problem from more fundamental considerations i.e. solving Poisson's equation to arrive at a model which is very similar to that of Viktorovitch(23-25). Using an experimentally determined gap density of states these authors have shown that it is possible to calculate the capacitance-voltage curve. Hence they have shown that it is possible to derive the bulk density of state distribution from C-V data even at finite frequencies. This may be achieved by assuming an N(E) distribution, calculating the C-V curve and then adjusting N(E) and τ_o by trial and error until the calculated and experimental C-V data match. A similar approach can be applied to the device conductance(27). In this case, by integrating Poisson's equation through the depletion region, the device conductance may be found without any assumptions. The expression for the conductance thus derived is identical to that obtained independently by Cohen and Lang(28) in their recently published extensive work. Their calculations were performed with a view to the interpretation of D.L.T.S. results and admittance-temperature data in terms of the density of states. Whilst their calculations are general in their application, their companion experimental paper(29) deals largely with doped α-Si:H films. They suggest however that admittance-temperature measurements may be the best method (i.e. least susceptible to errors due to interface states) for determining N(E). This experimental work remains to be done.

(e) Tiedje et al

Tiedje et al[30, 31] have used an approach which explains the frequency dependence of an α-Si:H Schottky barrier and allows the barrier profile to be deduced. The whole device is represented by a resistor and capacitor, both frequency dependent, in series. At very high frequencies the α-Si:H simply acts as a dielectric and the measured capacitance is $C = \frac{\varepsilon_o \varepsilon_r A}{d}$ where d is the film thickness. At lower frequencies the bulk semiconductor begins to relax and the localised states make an increasing contribution. The capacitance is given by

$$C = \frac{\varepsilon_o \varepsilon_r A}{w + L_s} \quad \text{where} \quad L_s(\omega) = \left[\frac{\varepsilon_o \varepsilon_r kT}{n(\omega) e^2}\right]^{\frac{1}{2}}$$

$$\text{and} \quad n(\omega) = N_c \frac{kT}{\delta} (\omega \tau_o)^{-\delta} \exp\left[\frac{E_F - E_C}{kT}\right] \qquad (3.31)$$

At very low frequencies an ω^{-2} dependence is expected. Thus the resultant C-ω plot should exhibit a well defined structure. Tiedje et al have analysed data on various samples using this method and have shown that metal-intrinsic α-Si:H diodes have similar barrier profiles, regardless of the metal used.

Summarising, it is hard to estimate the accuracy of the various models discussed because of the wide variety of experimental results which have been published for ostensibly the same experimental conditions. The question as to which effects are truly due to the bulk properties of α-Si:H and which are purely experimental artefacts has not been satisfactorily answered. More work is needed, both experimentally and theoretically before these problems can be solved.

3.4 Conduction Processes in Insulating Films

The use of thin insulating films in devices means that even small applied voltages produce very large electric fields. As a consequence a

variety of different conduction mechanisms can occur. These are now summarised. For a given insulator each process may dominate in turn in different temperature and bias regimes. However, the processes are not independent of one another and the interpretation of results is often difficult.

(a) Ohmic Conduction

Insulators can exhibit ohmic conduction, especially at low fields. As for a semiconductor the conductivity is

$$\sigma = ne\mu \tag{3.32}$$

for electrons or holes, where n is the carrier density and μ its mobility. The magnitude of the conductivity of insulators is considerably lower than that of semiconductors, due to the greatly reduced number of carriers in the conduction or valence bands. As well as ohmic (i.e. drift) conduction, diffusion can occur due to spatial variations in the carrier density. However, drift is normally the dominant component.

(b) Space Charge Limited Conduction

This occurs because of the injection of charge carriers from a metal or semiconductor into an insulator and becomes important when the number of injected carriers exceeds the number of free carriers in a material. In insulators, because of the small number of free carriers, injection as a result of an applied bias can lead to very large effects at room-temperature, as it easily leads to charge imbalance. The effect of these injected carriers is largely determined by the presence (or absence) of traps which can trap and store injected charge in equilibrium with free charge. The maximum effect is in the trap-free case where all of the injected carriers are available to take part in conduction processes. The injected carriers form a space charge layer in the surface region which limits the charge reaching the bulk.

Carriers of both types can be injected and the most general representation of this mechanism is

$$J \;\alpha\; d\left(\frac{V}{d^2}\right)^m \qquad (3.33)$$

where d is the sample thickness and m is a constant, not necessarily an integer. e.g. for the trap-free limit m = 2, for double injection m = 3.

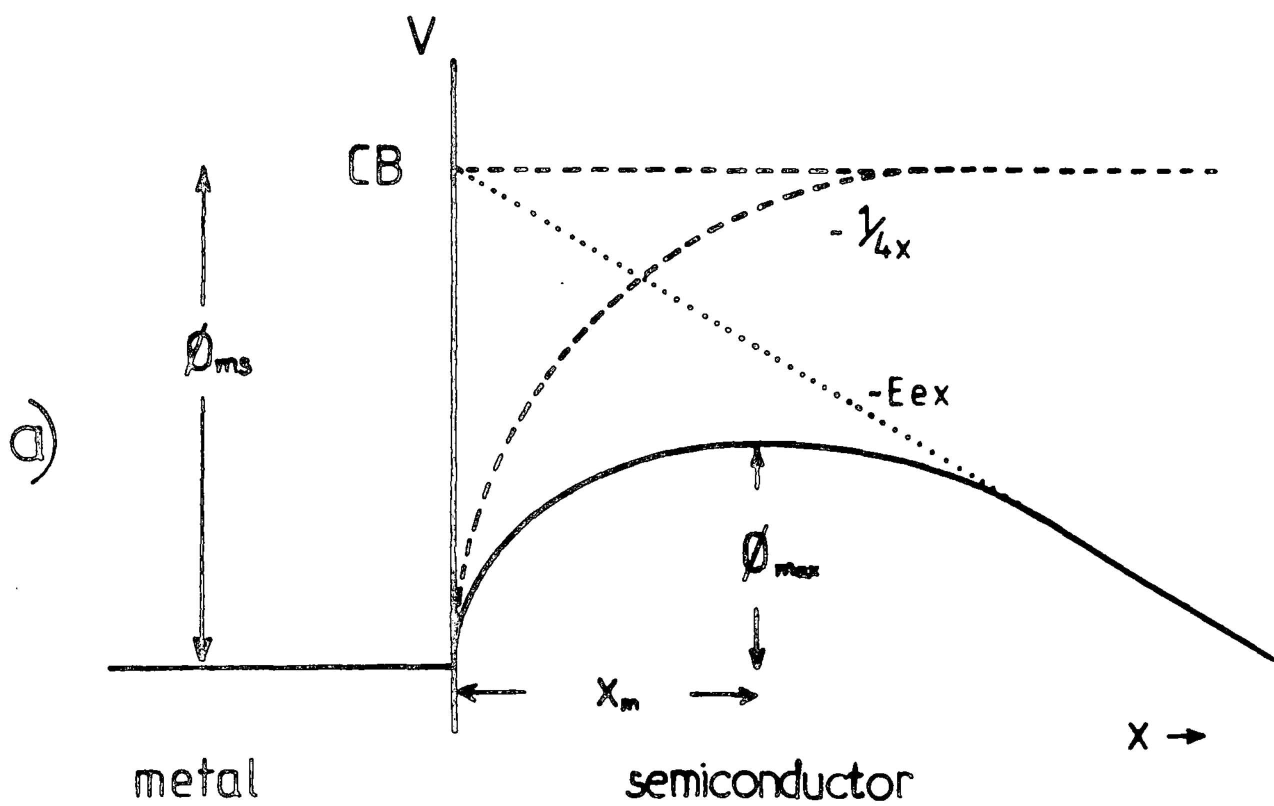
(c) Schottky Emission

In the presence of a high field, Schottky emission of electrons may occur from the metal (at negative potential) into the conduction band of the insulator. This mechanism corresponds to the thermal activation of carriers over the metal-insulator barrier together with the Schottky lowering of that barrier due to the applied field. A schematic diagram of a metal-insulator barrier under the influence of an applied field is shown in Fig. 3.12. The energy required to excite an electron from E_F to the conduction band of the insulator

$$\phi(x) = \phi_{MI} - \left\{ \frac{e^2}{4\pi\varepsilon_o\varepsilon_r\, 4x + \frac{e^2}{\phi_{MI}}} \right\} - Eex \qquad (3.34)$$

where ϕ_{MI} = the initial work function difference, with no applied field, Eex is the Schottky lowering of the barrier and the middle term is the P.E. acquired by the electron leaving the metal. The maximum height of the barrier is found by differentiation

$$\phi_{max} = \phi_{MI} - \sqrt{\frac{Ee^3}{4\pi\, \varepsilon_o\varepsilon_r}} \qquad (3.35)$$



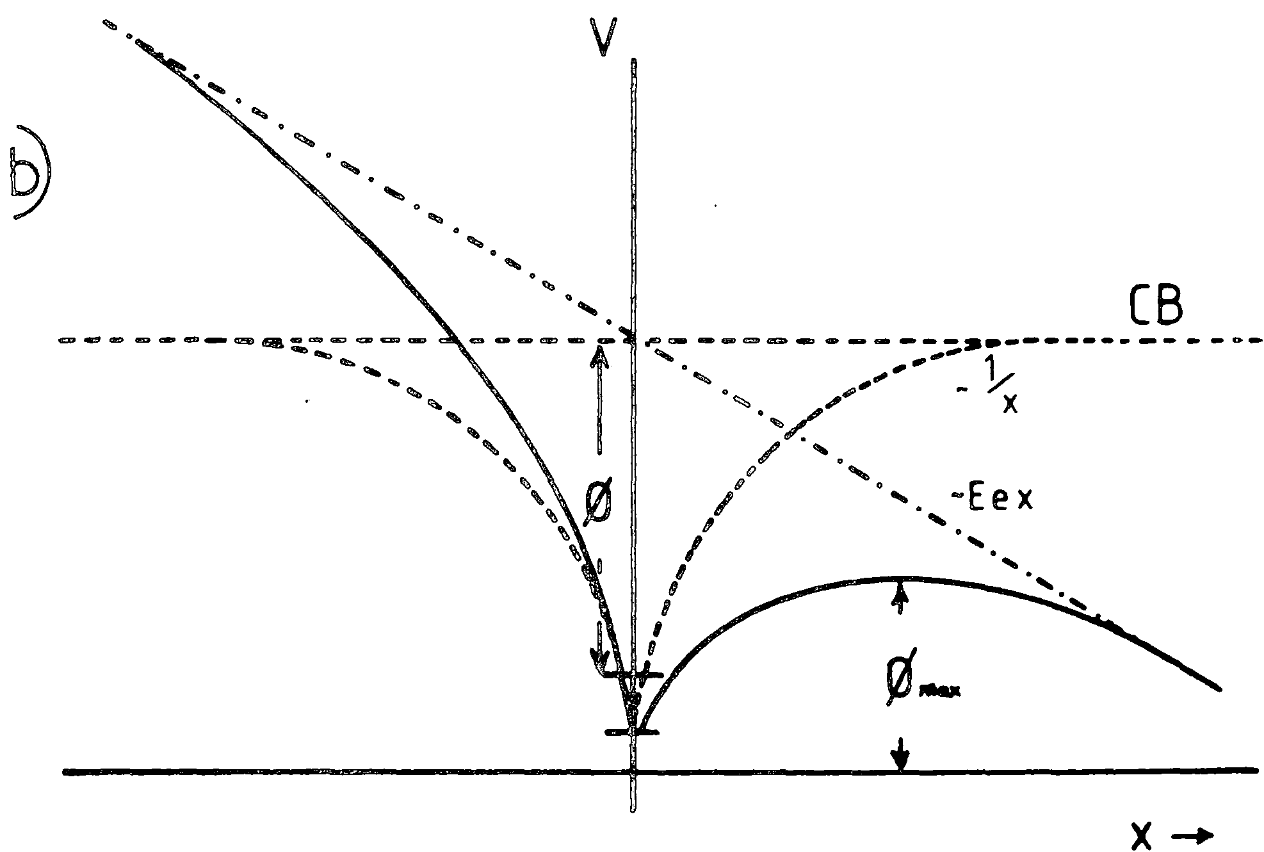


Fig. 3.12 Schematic representations of (a) the Schottky emission process and (b) the Poole-Frenkel emission process. CB denotes the bottom of the conduction band.

and the resulting current density from Schottky emission is proportional to the number of carriers with this energy.

$$\text{i.e.} \qquad \sigma \propto \exp\left(-\frac{\phi_{max}}{kT}\right) \tag{3.36}$$

$$\propto \exp\left(-\frac{\phi_{MI}}{kT}\right) \exp\left(-\sqrt{\frac{Ee^3}{4\pi\varepsilon_o\varepsilon_r}}\left(\frac{1}{kT}\right)\right) \tag{3.37}$$

or more simply

$$j \sim \exp\left(-\frac{C}{T}\right) \exp\left(\frac{-b\sqrt{V}}{T}\right) \tag{3.38}$$

where b and c are constants. This type of conduction, which is a barrier limited conduction, is readily identifiable by plotting either $\ln J$ v $V^{\frac{1}{2}}$ or $\ln (J/_{T}2)$ v $1/_{T}$. The constants may be determined from these straight lines.

(d) Poole-Frenkel Conduction

This mechanism is similar to Schottky emission except that the barrier in this case is that of a trapping centre (localised state) in the bulk of the insulator. Carriers can be excited from these traps to the insulator conduction band. If the barrier has a coulombic potential (i.e. varies as $1/_{x}$ with distance x) and assuming a positively charged trap (see Fig 3.12(b)) the excitation energy is

$$\phi(x) = \phi - \left(\frac{e^2}{4\pi\varepsilon_o\varepsilon_r x}\right) - Eex \tag{3.39}$$

Fig. 3.13 Current-voltage characteristics (schematic) of a solar cell in the dark and under illumination.

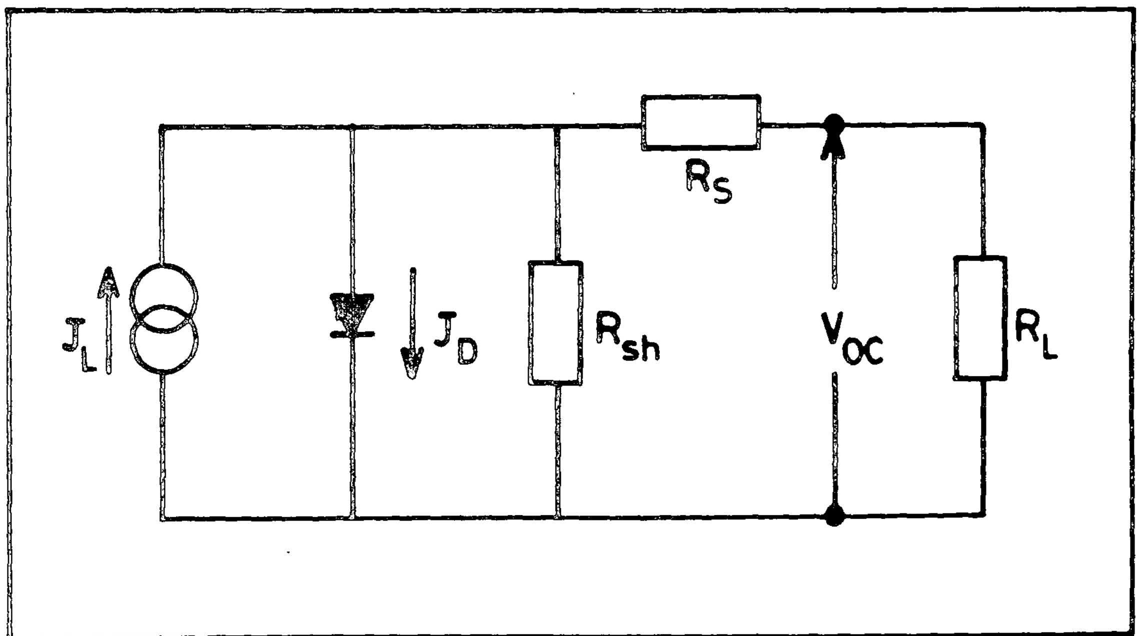


Fig. 3.14 The equivalent circuit of a solar cell.

where ϕ is the trap to conduction band energy. Proceeding as before

$$\phi_{max} = \phi - 2\sqrt{\frac{Ee^3}{4\pi\varepsilon_o\varepsilon_r}} \quad (3.40)$$

and hence

$$j \sim \exp\left(\frac{C'}{T}\right) . \exp\left(\frac{-2b\sqrt{V}}{T}\right) \quad (3.41)$$

This expression is similar to that for Schottky emission, but there are important differences in the constants. It should be noted that this consideration of Poole-Frenkel (P.F.) conduction is not general, as it deals with only one specific situation (see above assumptions). However, if this is the case, the two mechanisms can be distinguished by several means. Firstly, the barrier lowering due to the applied field for PF conduction is twice that for Schottky emission, because of the immobility of the positive charge associated with the traps. This means that the slope of ln J v $V^{\frac{1}{2}}$ graphs for these mechanisms will differ by a factor of two (the slope for P.F. being the largest). Also P.F. conduction does not show a straight line relationship for $\ln J/T^2$ V^1/T whereas Schottky emission does, although in practice a wide temperature range must be measured to demonstrate this as the function changes only slowly with temperature. A further distinction can be drawn by the effect of scaling the sample thickness. P.F. conduction is a barrier limited current, but it is also a bulk process, and as such the current should scale with film thickness. Schottky emission is dependent on the surface barrier and changes with the particular contact metal used : a change in the metal work function ϕ_M shifts the ln J > $V^{\frac{1}{2}}$ curve vertically. It must be emphasised that both conduction processes are <u>field</u>, not voltage dependent. Allowance must be made for this with samples of different thickness.

The Poole-Frenkel constants can be altered for traps in certain charge states. A particular case of interest is where the trapping centres lie beneath the Fermi level and can be regarded as neutral traps. This results in an extra factor of two in the denominator of equation 3.41 and makes the expression virtually identical to the Schottky emission equation (eq. 3.38). In this situation the two mechanisms become very difficult to distinguish experimentally.

It is possible to construct a general scaling law which applies to all forms of barrier limited conduction. If the potential is assumed to vary as $1/r^m$, the current density is related to applied field by the expression

$$\ln J \;\alpha\; E^{m/m+1} \qquad (3.42)$$

where E is the electric field. Hence for a Coulombic potential, m = 1 and the expression reduces to the familiar Poole-Frenkel result. Any mechanism which obeys this law can be said to be barrier limited.

(e) Ionic Conduction

This is similar to a diffusion process, where defects drift through a material under the influence of an applied field. The effect can be enhanced by the presence of moisture. Ions or vacancies 'jump' over the potential barriers to the next site. In general, d.c. ionic conductivity decreases with the length of time the field is applied,because it is difficult to inject or remove ions from the insulator. After the initial current flow positive and negative space charges build up at the insulator interfaces, distorting the potential distribution. On removal of the bias large internal fields remain and some, but not all of the ions, flow back to their equilibrium positions. This may well result in hysteresis.

3.5 Theory of Tunnelling MIS Diodes

An MIS diode may be considered as a modification of a simple MS (Schottky barrier) device. Assuming the thermionic emission theory

applies, we recall from section 3.2.2 that the dark current-voltage relationship for an ideal Schottky barrier is given by

$$J = A^{*} T^{2} \exp\left(\frac{-e\phi_B}{kT}\right)\left[\exp\left(\frac{eV}{kT}\right) - 1\right] \qquad (3.43)$$

If a tunnellable insulating layer is introduced between the semiconductor and the metal this equation must be altered. According to Card and Rhoderick[32], for bias voltages greater than 3kT/e the dark forward current is given by

$$J = A^{*} T^{2} \exp\left(-\chi^{\frac{1}{2}}\delta\right) \exp\left(\frac{-e\phi_B}{kT}\right) \exp\left(\frac{eV}{nkT}\right) \qquad (3.44)$$

where the χ is the mean barrier height (in eV) due to the insulating layer of thickness δ (in anstroms). The effects of introducing the insulating layer may best be understood with reference to this equation. They are as follows:

(1) The potential distribution in the diode will be changed by the presence of an interfacial layer : some of the voltage in the system will be dropped across the layer. Even at zero bias there will be a voltage drop across the insulator because of the difference between the work functions of the metal and the semiconductor. This leads to a reduction in the potential across the depletion region which reduces the band bending and results in a lower zero bias barrier height, ϕ_B, than in the ideal Schottky barrier case. Under bias conditions the applied voltage will be divided between the insulator and the semiconductor. This makes ϕ_B a function of the applied bias and alters the shape of the J-V curve. The effect is allowed for in equation 3.44 by the inclusion of the ideality factor, n.

(2) The presence of the insulator acts as a barrier to current flow. Obviously, the magnitude of any currents will be reduced from the equivalent ideal Schottky barrier case, but providing the insulator is not too thick, (say < 30Å) substantial currents may still flow through the layer by tunnelling. The exp $(-\chi^{\frac{1}{2}}\delta)$ term in equation 3.44 represents the majority carrier tunnelling probability. This likelihood of a carrier tunnelling through the barrier falls exponentially with increasing insulator thickness δ. The mean barrier height, χ, depends on the band structure of the thin insulating layer, which may be substantially different from the band structure of a thicker layer (or a 'bulk' sample of the material). In terms of the J-V plot, this effect manifests itself as a reduction in the reverse saturation current density, J_o.

(3) The incorporation of fixed charge in the insulator will upset the charge distribution in the system resulting in a change of barrier height ϕ_B. It is equivalent to altering the metal work function, making it smaller or larger, depending on the sign of the charge. An effective metal work function may be defined[33]

$$\phi_M' = \phi_M - \left(\frac{Q_{fix}\ \delta_{eff}}{\varepsilon_i} \right) \qquad (3.45)$$

where ϕ_M is the true metal work function, Q_{fix} is the amount of fixed charge and δ_{eff} the distance of that charge from the metal. ε_i is the permittivity of the insulator.

(4) The influence of surface or interface states can change ϕ_B in a similar way to fixed charge in the insulator, These states are usually assumed to be located at, or near, the semiconductor/insulator interface. They may be charged by (a) electrons tunnelling between these states and the metal, and by (b) interaction with electrons in the conduction and valence bands of the semiconductor. The charge state ie occupancy of any

interface state distribution is determined by whichever of these two processes is dominant, and will be a function of the applied bias voltage. Hence surface states constitute a voltage dependent fixed charge. Their effect is to alter the variation of J with V (i.e. the shape of the J-V plot) and this is expressed through the n-factor in equation 3.44. Card and Rhoderick[32] have related the ideality factor to the density of interface states and the insulator thickness δ by the following equation

$$n = 1 + \frac{\left(\frac{\delta}{\varepsilon_i}\right)\left(\frac{\varepsilon_s}{W} + e\,D_{sb}\right)}{1 + \left(\frac{\delta}{\varepsilon_i}\right) e\,D_{sa}} \tag{3.46}$$

ε_i and ε_s are the insulator and semiconductor permittivities respectively. The interface states are divided into two groups, such that all the states in one group (density D_{sa}) are in equilibrium with the metal while those in the other group (density D_{sb}) are in equilibrium with the semiconductor. The above equation holds generally, but often one group of states will dominate and the expression may be simplified. It is clear that if the states are located at the semiconductor/insulator interface, their communication with the metal will become more difficult as the insulator thickness is increased. For sufficiently thick insulators all the states will be in equilibrium with the semiconductor. Card suggests the criteria[1] that if $\delta > 30$Å then $D_{sa} \rightarrow 0$, but if $\delta < 30$ Å then $D_{sb} \rightarrow 0$.

(5) It is worth mentioning the effect of the incorporation of an insulating layer on the minority carrier injection ratio γ, although this does not have a significant influence on the J-V characteristics. The minority carrier injection ratio for a Schottky barrier diode (assuming an n-type semiconductor) may be written very simply as

$$\gamma = \frac{J_p}{J_p + J_n} \tag{3.47}$$

where J_p and J_n are the total current densities carried by electrons and holes respectively. In a Schottky diode γ is usually very low (typically 10^{-4} - 10^{-5} in Si) due to the fact that the minority carriers have to surmount a somewhat larger barrier than the majority carriers (hence $J_n >> J_p$). However, the presence of an interfacial insulating layer can substantially increase γ. In the case of very thin insulators this occurs because J_n is reduced, while J_p remains approximately constant. This may be explained as follows. The electron current in a Schottky diode is limited by thermionic emission over the barrier. In an MIS structure the insulator represents an additional barrier, inhibiting electron flow since they must tunnel through it. The electron current is thus reduced, becoming proportional to the majority carrier tunnelling probability. In contrast, the hole current is limited by diffusion through the neutral (bulk) region of the semiconductor and is largely unaffected by the insulating layer. Hence J_p remains roughly constant. For thick insulating films a major re-alignment of the semiconductor bands with respect to the metal Fermi level can occur[34]. This can greatly increase the number of holes tunnelling from the metal to the semiconductor, and the minority carrier current component may rise to $\sim$10% of the total current.

Although these effects have been considered separately in a real device any combination of them could be operating under forward bias conditions.

Turning to reverse bias, the insulating layer causes the effective barrier height to decrease with increasing bias. This appears as a non-saturation of the reverse current. It has been shown that the reverse currents of diodes with fairly thick insulators can exceed those of diodes with thinner insulating layers, since the increased barrier lowering over-compensates for the lower tunnelling probability in the thicker insulator[32].

The ability to exercise a degree of control over the various current components by virtue of the insulating layer has led to a number of interesting

applications of MIS devices. Among these are injection electroluminescence, where the greatly increased minority carrier generation is exploited. This principle has been successfully demonstrated on a number of semiconductors (see (35) and references therein). MIS structures have also been used as solar cells where they possess distinct advantages over Schottky barrier devices. This particular application will be discussed in the next section.

Finally, the effect of introducing an insulating layer on the device capacitance must be considered briefly. A plot of $1/C^2$ against V, such as is commonly used to find the barrier height will generally be modified. This situation has been analysed by Cowley[35] and Crowell and Roberts[37] and more recently by Fonash[38]. For the purposes of this thesis it is sufficient to note that shifts in the intercept on the voltage axis can occur, giving very large values for the diffusion potential. The slope of a $1/C^2$ v V graph can also change as a result of surface state effects. Indeed, surface states can cause non-linearity in these plots, making their analysis very difficult.

3.6 Solar Cells

A solar cell is a photovoltaic device designed to convert sunlight into electrical power and to deliver this power into a suitable load in an efficient manner. A great deal of interest is being shown in α-Si:H as a solar cell material using various device configurations e.g. p-n, p-i-n, Schottky barrier and MIS devices. The work on tunnelling MIS structures presented in chapter 8 of this thesis was carried out with a view to enhancing the solar cell performance of α-Si:H Schottky barrier structures by including an interfacial insulating layer. Thus, the relevant solar cell theories and parameters will now be outlined.

3.6.1 Schottky Barrier Devices

The current flowing in the dark when a bias is applied to a Schottky barrier has been already discussed. On illumination, photogenerated

carriers, i.e. electron-hole pairs, are created in the semiconductor due to the absorption of photons with energy $E > E_g$, the bandgap energy. Because of the band bending, an electric field exists in the region of the semiconductor surface (i.e. the depletion region), and this field tends to separate the electron-hole pairs, sweeping them in opposite directions. This produces a forward voltage across the barrier. The appearance of a forward voltage across an illuminated junction is called the photovoltaic effect. If a load resistor is connected across the diode a photocurrent, which we can call J_L will flow in the reverse direction. To achieve a high J_L as many photons as possible must pass through the metal contact to be absorbed in the semiconductor. The net current under illumination is given by

$$J = J_o \exp\left(\frac{eV}{nkT}\right) - J_L \tag{3.50}$$

assuming that n and ϕ_B are unaffected by light[39].

Typical dark and light J-V characteristics of a Schottky barrier solar are shown schematically in Fig. 3.13. From these curves several important parameters may be defined. Using equation 3.43, for J = 0 we have the open circuit voltage,

$$V_{oc} = n\left[\phi_B + \frac{kT}{e} \ln\left(\frac{J_L}{A^* T^2}\right)\right] \tag{3.51}$$

Also at V = 0 the current becomes the short circuit current

$$J_{sc} = - J_L \tag{3.52}$$

By a judicious choice of load resistance approximately 80% of the available power (given by $I_{sc} \times V_{oc}$) can be extracted. This is shown in Fig. 3.13 by the maximum power rectangle, touching the curve at (V_m, J_m). The fill factor, F.F., of the cell is defined as

$$F.F = \frac{J_m V_m}{J_{sc} V_{oc}} \tag{3.53}$$

which enables us to write the cell efficiency as

$$\eta = \frac{J_m V_m}{I_{ph}} = \frac{J_{sc} V_{oc} \, F.F.}{I_{ph}} \tag{3.54}$$

where I_{ph} is the incident light intensity. The theoretical efficiency of a device may be fairly high, but in practice there are many loss mechanisms which prevent this from being attained. Real devices can be represented by an equivalent circuit of a very simple kind as shown in Fig. 3.14. This consists of a current source providing the photocurrent I_L in parallel with a diode passing the dark current I_d. These are shunted by a high resistance R_{sh} and the whole circuit has an additional series resistance R_s, R_L being the load resistance. Ideally R_{sh} would be infinite and R_s would be zero. In reality these deviations are expressed in the diode ideality factor, in its departure from unity.

3.6.2. MIS Solar Cells

The enhancement of solar cell performance as a result of inserting a thin insulator between a metal and semiconductor to form an MIS device has been widely reported (see (40) and references therein). Although the exact role of this interfacial layer may depend on many factors, its presence invariably results in an increased open circuit voltage. This is easily understood in terms of a suppression of the majority carrier dark current

as discussed in section 3.4. The experimental observation that the photo-current is not suppressed by the presence of the insulating layer is more difficult to understand. It should be remembered that the majority carrier current is limited by thermionic emission over the barrier and is therefore proportional to the probability of electrons tunnelling through the insulating layer. Conversely the minority carrier current is limited by diffusion through the neutral region of the semiconductor, and so will be relatively unaffected by any interfacial layer which might be present. As a result the photogenerated current, which consists of minority carriers, is not suppressed providing the insulator thickness is less than a few tens of angstroms.

If the dark current-voltage relationship is given by equation 3.44 then the open circuit voltage of an MIS solar cell (neglecting any recombination currents) is

$$V_{oc} = n \left[\phi_B + \frac{kT}{e} \chi^{\frac{1}{2}} \delta + \frac{kT}{e} \ln \left(\frac{J_L}{A^* T^2} \right) \right] \tag{3.55}$$

once again assuming that n and ϕ_B are unaffected by illumination. Hence V_{oc} increases due to increases in n, $\chi^{\frac{1}{2}}$ and δ . If δ is such that J_L and F.F. are not reduced then an increase in the cell efficiency will occur over that of the corresponding Schottky barrier cell.

The current 'state-of-the art' of MIS solar cell technology has recently been reviewed by Singh et al[41]. Work on p-type single crystal silicon dominates the field, and has produced the highest efficiency to date: 18.3% for a 3 cm^2 cell. GaAs has been extensively studied with reported cell efficiencies (for 1 cm^2) between 15 and 17% at present. Devices on InP are at an earlier stage of development and only 6% efficiency has been achieved so far. Various polycrystalline semiconductors have also been used, the most efficient being Si and GaAs at around 14%. The newest type of device incorporates amorphous silicon (α-Si:H) and already the

efficiencies have reached nearly 7%. The attraction of MIS solar cells lies in their inherent simplicity of fabrication, which lends itself to low cost, mass production. Unfortunately, many devices degrade over relatively short periods of time due to chemical instabilities and this has hindered progress. However, as Singh et al[41] point out, the most recent ageing tests on high efficiency cells indicate a much increased life expectancy and it may be that this problem will be overcome in the near future.

CHAPTER 4

THICK INSULATOR MIS THEORY

4.1 Introduction

A thick-insulator MIS device may be defined as one in which the effects of carrier tunnelling through the insulator are negligible. This is generally true for insulator thicknesses greater than about 5 nm. Since the MIS structure was first proposed as a voltage variable capacitor in 1959[1,2] it has been extensively studied, and has become an important device for use in semiconductor surface analysis and the basic 'building block' in many integrated circuits. Already MIS transistors and charge coupled devices (CCD's) are widely used and research into MIS thin film transistors looks promising.

This chapter outlines the basic physics of MIS devices, beginning with a consideration of the ideal MIS diode. The effects of various deviations from ideality are discussed in section 4.3 and this leads to a brief summary of some methods of measuring the surface state density in the following section. The chapter concludes with sections on the principles of operation of insulated gate field effect transistors in general, and more specifically, on thin film transistors. The subject of conduction processes in the insulating layers of MIS devices incorporating LB films will be discussed in the next chapter.

4.2 The Ideal MIS Diode

The MIS device structure is depicted schematically in Fig. 4.1. The insulator thickness is d, and V is the voltage applied to the metal electrode (the bias voltage). The definition of an ideal MIS device, which forms the basis of an understanding of real devices, is as follows, and may be understood with reference to Fig. 4.2.

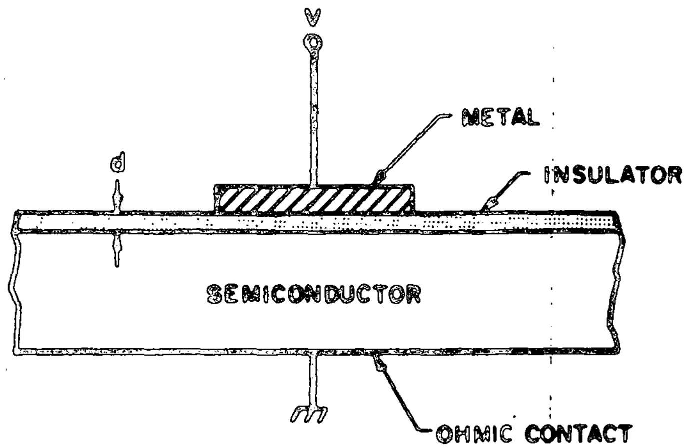


Fig. 4.1 Metal-insulator-semiconductor (MIS) diode

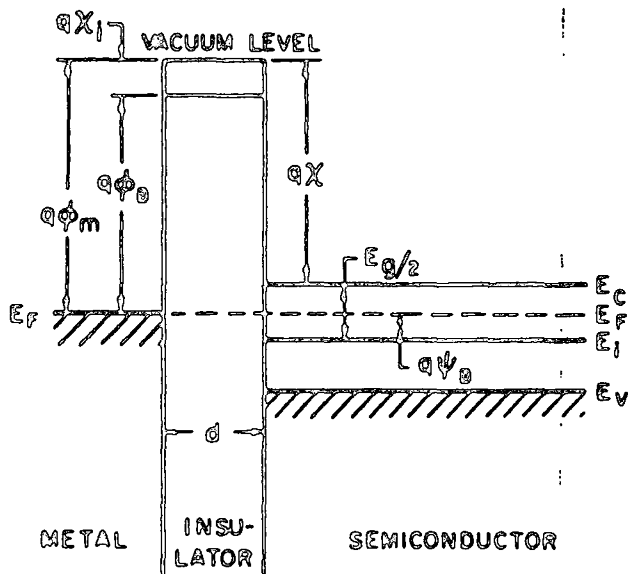


Fig. 4.2 Energy-band diagram of an ideal MIS (n-type) diode at zero bias voltage.

(1) With no applied voltage the energy difference between the metal work function ϕ_M and the semiconductor work function ϕ_S is zero. Consequently, there is no band bending in the semiconductor, a situation which is commonly known as the flat band condition. For an n-type semiconductor this may be expressed by the following equation.

$$\begin{aligned} \phi_{MS} &\equiv \phi_M - \phi_S \\ &\equiv \phi_M - \left(\chi + \left(\frac{E_g}{2}\right) - \psi_B\right) \qquad (4.1) \\ &\equiv 0 \end{aligned}$$

where ϕ_{MS} is the work function difference, χ is the semiconductor electron affinity, E_g the bandgap and ψ_B the potential difference between the Fermi level E_F and the intrinsic Fermi level E_i (situated at midgap).

(2) Charge can only exist in the system within the semiconductor and on the metal surface immediately next to the insulating layer. This holds for any bias condition. The charge on the metal surface will always be equal in magnitude and opposite in sign to that within the semiconductor, maintaining charge neutrality over the junction region.

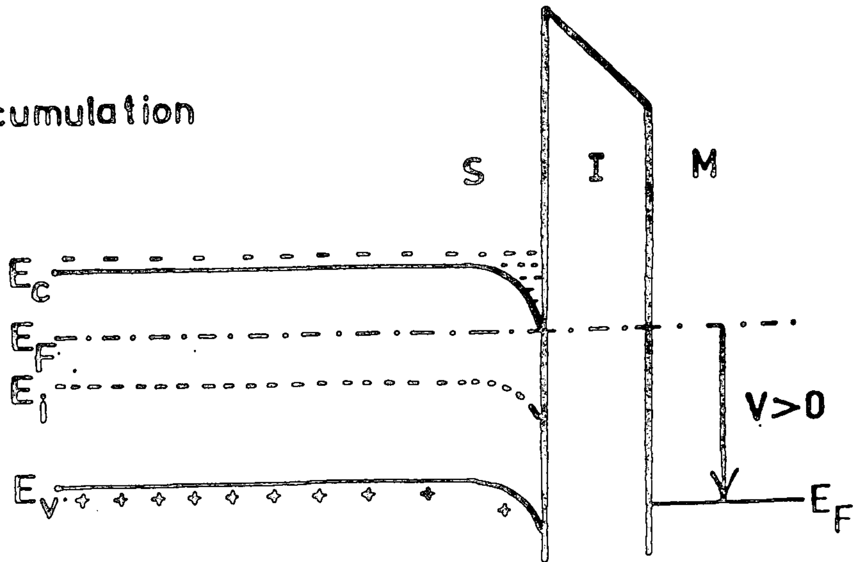
(3) The insulating layer is infinitely resistive i.e. it has zero conductivity over the whole bias voltage range. Thus, the ideal MIS diode is a truly voltage, or more accurately a field-controlled device.

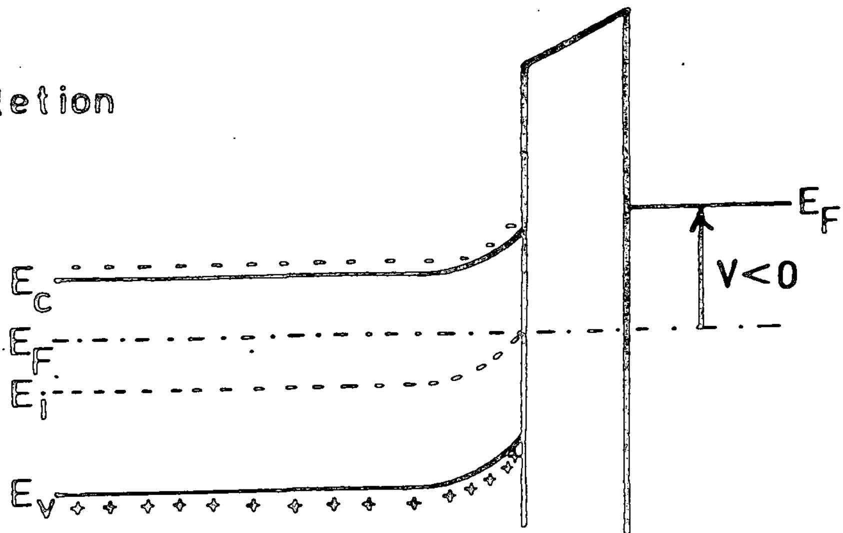
Applying a bias voltage to the metal electrode affects the semiconductor surface and changes the device characteristics. It is common to define the direction of the bias as either forward or reverse. For an n-type semiconductor forward bias is a positive voltage on the metal electrode with respect to the ohmic contact, and reverse bias is a negative voltage. The situation is reversed for a p-type specimen.

The band diagrams of Fig. 4.3. show the different bias voltage regimes of an MIS diode based on an n-type semiconductor. According to Fermi- Dirac statistics the majority carrier (electron) concentration is inversely proportional to $\exp\left(\frac{E_c - E_F}{kT}\right)$. On the application of a positive voltage to the metal contact the conduction band bottom bends downwards towards the Fermi level, reducing $(E_c - E_F)$ and creating negative charge at the semiconductor surface by increasing the majority carrier density. This condition is known as accumulation (Fig. 4.3(a)). If a small negative voltage is applied to the top electrode (reverse bias) the bands in the semiconductor are bent upwards. The density of majority carriers, in this case electrons, is decreased at the semiconductor surface leaving a fixed positive space charge due to the ionised donors. The device is said to be in depletion (see Fig. 4.3(b)). As the negative bias voltage is made larger the bands continue to bend upwards. When the band bending is such that the intrinsic Fermi level E_i crosses the Fermi level at the surface, the device is said to be inverted (Fig. 4.3(c)). In this condition the surface region is so depleted of majority carriers that the minority carrier density is greater than the majority carrier density. Thus, in an n-type material, a narrow p-type region is formed at the surface.

The degree of band-bending present in an MIS device is often described in terms of the surface potential ψ_s. This parameter is shown for an n-type semiconductor in Fig. 4.4. and may be defined as the difference between the intrinsic Fermi level in the bulk of the semiconductor and at its surface. Hence, at flat-band, condition ψ_s is zero (no band bending). The following regions of surface potential can be defined.

$\psi_s > 0$	Accumulation:- bands bent downwards
$\psi_s = 0$	Flat-band
$\psi_B < \psi_s < 0$	Depletion:- bands bent upwards
$\psi_s = \psi_B$	Midgap
$\psi_s > \psi_B$	Inversion:- bands bent upwards





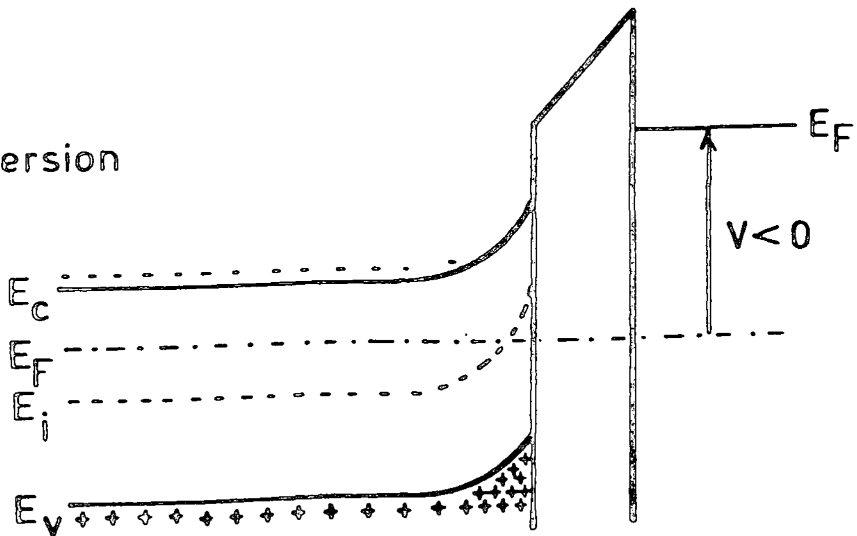


Fig. 4.3 Energy-band diagrams for an MIS structure depicting (a) accumulation, (b) depletion, and (c) inversion

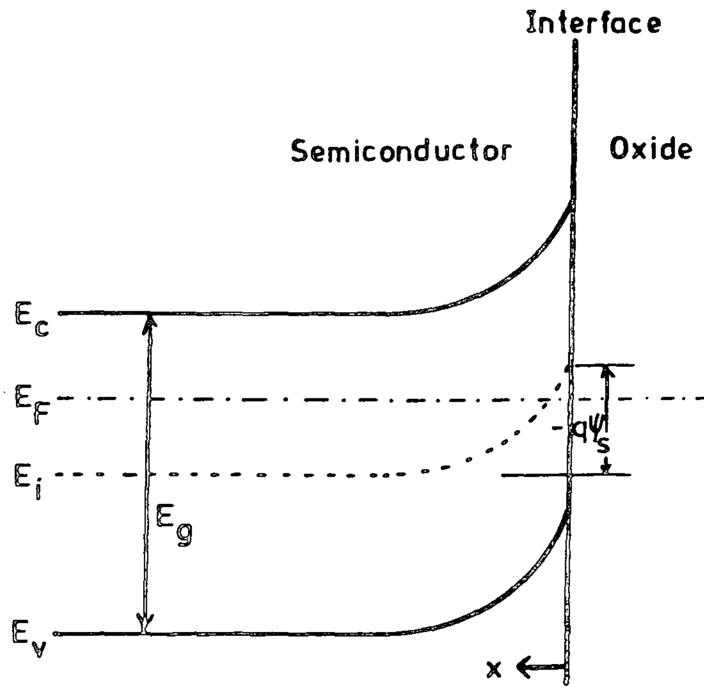


Fig. 4.4 Band diagram of MIS diode in inversion showing the surface potential ψs

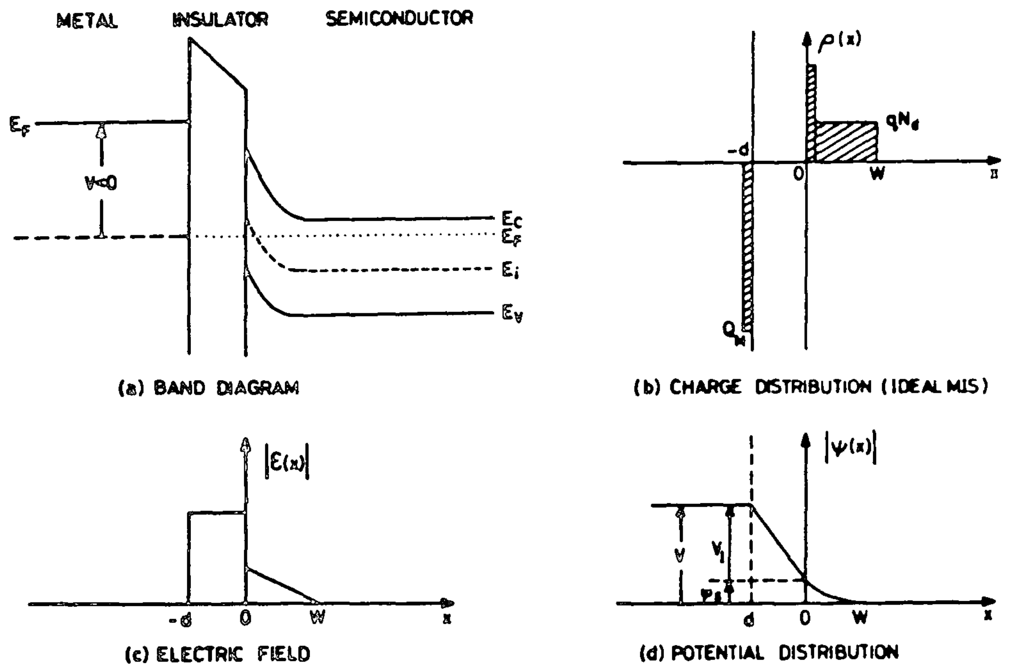


Fig. 4.5 (a) Band diagram of MIS diode (inversion)
(b) Charge distribution
(c) Electric field
(c) Potential

The surface potential may be substituted into the standard expressions relating bulk potential to carrier concentration to obtain the electron and hole concentrations at the surface. The surface electric field and the potential as a function of distance (x) can be found by successive integrations of Poisson's equation.

$$\frac{\partial^2 \psi}{\partial x^2} = \frac{-\rho(x)}{\varepsilon_o \varepsilon_s} \qquad (4.2.)$$

where ε_o is the permittivity of free space, ε_s is the relative permittivity of the semiconductor and $\rho(x)$ is the total space charge density. Using Gauss' law the space charge distribution can also be calculated. Fig. 4.5 shows the variation in these parameters with distance for an n-type semiconductor in inversion.

Any charge in the semiconductor must be mirrored by an equal and opposite charge on the metal electrode. Because these two regions of charge are separated by an insulating layer they will give rise to a small signal capacitance. The value of this capacitance is directly related to the surface potential, which in turn defines the degree of band-bending. Hence, a capacitance-bias voltage graph is a very good representation of the charge state of the device. The total capacitance of the system is a series combination of the insulator capacitance C_I, which is a constant for a given thickness d, and the semiconductor space charge capacitance, C_{SC}, which is bias dependent.

$$C = \frac{C_I \, C_{SC}}{C_I + C_{SC}} \qquad (4.3)$$

As the bias voltage is changed, so the value of C changes, reflecting the variation in C_{SC} as shown in Fig. 4.6.

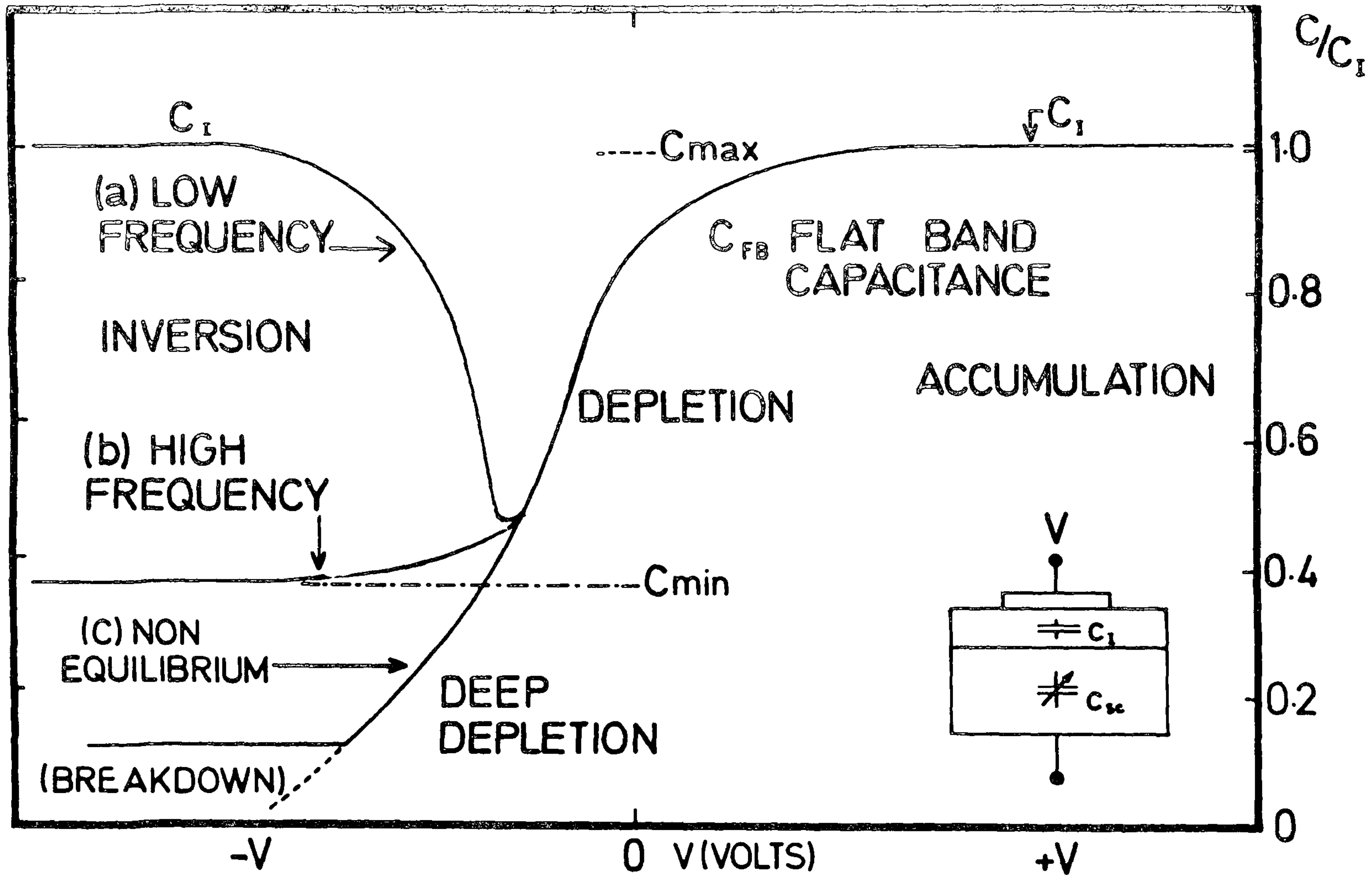


Fig. 4.6 Idealised MIS Capacitance-voltage curves (n-type semiconductor).

In the accumulation region there is a high density of majority carriers at the semiconductor surface, and hence a high differential capacitance associated with the space charge region. Because C_{SC} is large the total capacitance approaches C_I, which is its maximum value. With a small reverse bias the depletion region formed acts as a dielectric in series with the insulator, and the value of C falls. The capacitance goes through a minimum (the low frequency minimum) as the reverse bias is increased, and then begins to rise again with the formation of the inversion layer. The formation of the inversion layer is dependent on the bulk generation of minority carriers and their subsequent transport to the inversion region. It also depends on the removal of electrons from the surface region to the bulk, extending the depletion region. The former process is the limiting one because of the lower mobility of the minority carriers, and means that one of three different situations can occur in the bias region corresponding to inversion, depending on the frequency. If the frequency of the applied a.c. measuring signal is low enough so that the minority carrier concentration can follow it i.e. the minority-carrier generation-recombination rate is sufficiently fast for charge exchange with the inversion layer to take place in step with the signal, then C will rise to the maximum value of C_I again. At higher frequencies the minority carriers will not respond to the a.c. signal. The presence of the inversion layer effectively shields the semiconductor from the field, so that the depletion width, and hence the semiconductor capacitance, C_{SC}, stays the same, even with increasing bias. Thus the total capacitance remains constant, with a value C_{Min}, as the reverse bias is increased. At very high frequencies, or more usually under pulsed conditions, there is no time for the inversion layer to form and the device is said to be in deep depletion. In this case the value of C continues to fall with increasing reverse bias until breakdown occurs. Deep depletion may also result from

having a leaky insulator where exchange removes the inversion layer as soon as it is formed.

From the ideal C-V curves we can define certain parameters which will be important for characterising an MIS diode. The total capacitance (per unit area) at flat-band is found by taking the differential capacitance of the semiconductor depletion layer as $\psi_S \to 0$ and substituting in 4.3. Thus it can be shown that

$$C_{FB} = \frac{\varepsilon_i \varepsilon_o}{d + \frac{1}{\sqrt{2}} \left(\frac{\varepsilon_i}{\varepsilon_s} \right) L_D} \tag{4.4}$$

where ε_i = relative permittivity of insulator

ε_s = relative permittivity of semiconductor

d = insulator thickness

and L_D is the extrinsic Debye length, a measure of the depth of penetration of the electric field into the semiconductor.

$$L_D = \sqrt{\frac{2\, kT\, \varepsilon_s\, \varepsilon_o}{n_{no}\, q^2}} \tag{4.5}$$

where n_{no} is the equilibrium density of electrons in the semiconductor bulk.

Also important are the maximum and minimum values of the capacitance. The maximum value corresponds to the geometrical capacitance of the insulating layer

$$C_{max} = \frac{\varepsilon_i\, \varepsilon_o}{d} \tag{4.6}$$

The high frequency minimum is simply the combination (according to equation 4.3) of $C_I = \varepsilon_i\varepsilon_o/d$ and $C_{SC} = \varepsilon_s\varepsilon_o/W_M$ where W_M is the maximum depletion layer width. Thus

$$C_{min} = \frac{\varepsilon_i \varepsilon_o}{d + \left(\frac{\varepsilon_i}{\varepsilon_s}\right) W_M} \tag{4.7}$$

and

$$W_M = \left[\frac{4 \varepsilon_o \varepsilon_s kT \ln\left(\frac{N_d}{n_i}\right)}{e^2 N_d} \right]^{\frac{1}{2}}$$

where N_d is the ionised donor density and n_i the intrinsic carrier density. From these expressions it follows that

$$\frac{C_{max}}{C_{min}} = 1 + \frac{W_m \varepsilon_r}{d\varepsilon_s} \tag{4.9}$$

Hence, as the insulator thickness is decreased the ratio of $C_{max} : C_{min}$ increases.

The discussions so far have dealt with the capacitance characteristics of an ideal MIS device. It is worth emphasising that in the ideal case the conductance of such a device will be zero for all values of bias.

4.3 Causes of Deviation from Ideality

Practical MIS diodes differ from the ideal case in many ways. The following sections outline the major causes of the deviations and how they modify the device characteristics.

4.3.1 Work Function Differences

In the ideal MIS device it was assumed that the metal work function ϕ_M and the semiconductor workfunction ϕ_S were identical. This is not normally the case and in most devices there will be some band-bending, even at zero bias. The capacitance-voltage curves will be shifted from the ideal by an amount equal to the work function difference.

$$V_{shift} \equiv \phi_M - \phi_S$$

$$\equiv \phi_M - (\chi + \frac{E_g}{2} + \psi_B) \qquad (4.10)$$

By using different top metal electrodes it is possible to change the zero-bias state of a device from accumulation, through depletion to inversion.

4.3.2 Surface States

Impurities and defects in semiconductors are associated with energy levels in the forbidden gap. Localised states occur at the surface of a semiconductor where the crystal lattice and symmetry are strongly disturbed, and these are known as surface states[3-8]. They are characterised by their density, their position in the bandgap (i.e. their energy) and by their capture cross-section. Because of the two dimensional nature of the surface their density is measured per unit area, per unit energy, in contrast to bulk states which are measured per unit volume, per unit energy. Localised states also occur at the interface between two materials. These interface states are similar to surface states and are often referred to by that name.

The state of charge of an interface state is determined by its position relative to the Fermi level at the interface. The state will be in its most positive condition when it is above the Fermi level. Two types of states exist, namely donor-type states and acceptor states. Donor states can be

neutral (when filled) or can become positive by donating an electron. Acceptor states can be either neutral (empty) or negative when they accept an electron. The probability of occupation of a surface state is governed by the familiar Fermi-Dirac distribution function:

$$F(E_T) = \frac{1}{1 + g \exp\left(\frac{E_F - E_T}{kT}\right)} \qquad (4.11)$$

for donor states and

$$F(E_T) = \frac{1}{1 + \frac{1}{g} \exp\left(\frac{E_T - E_F}{kT}\right)} \qquad (4.12)$$

for acceptor states. E_T is the energy of the state and g is the ground state degeneracy, a numerical factor which takes into account the effect of electron spin on the probability of occupation of a state. Values of g vary considerably, but are typically 2 for donors and 4 for acceptors.

When an electric field is applied to an MIS diode the Fermi energy remains constant, providing thermal equilibrium is maintained (see Fig.4.5). Thus, the band - bending which takes place shifts the entire band structure with respect to the Fermi level and results in a change of occupancy of some states. The electrical effects of the surface states may be explained qualitatively as follows:-

Capacitance: an interface state is an additional allowed state at the interface of a device. It thus adds a capacitance of one elementary charge per state. This capacitance is critically dependent on the surface potential ψ_s and hence on the applied voltage V. The peak in the capacitance occurs at the voltage

where the interface state crosses the Fermi level. The interface state capacitance contributes to the overall device capacitance and so alters the shape of the ideal C-V curve.

Conductance: consider a small a.c. signal applied to an MIS diode with surface states. During the first half of the cycle the conduction band edge bends down towards the Fermi level, and some surface states move from being above E_F to below it. These states become occupied by electrons, but this happens after an average time τ, the time constant of the states, rather than instantaneously. On the second half of the cycle the conduction band edge bends away from E_F. The now filled surface states are raised above F_F again and they lose their electrons in a characteristic time τ. This time delay, associated with the capture and emission of carriers by the surface states, may be represented by a resistor and capacitor in series. Thus, there is a conductance arising from the surface states which manifests itself as a peak in the conductance-voltage curve. The peak occurs at a voltage which corresponds to the surface states crossing E_F.

Surface Potential: in contrast to those already mentioned, this is a d.c. effect. Any charge stored in the interface states modifies the electric field at the surface i.e. to change the surface potential by a given amount requires a different bias voltage from the ideal case. The capacitance-voltage curves for deviceswith interface states are more'stretched out' than the ideal curves.

For a device with a single level interface state the equivalent circuit (after Nicollian and Goetzberger ref (9)) is shown in fig. 4.7(a). where R_{ss} and C_{ss} are the resistance and capacitance associated with the surface states, The parallel branch of the equivalent circuit can be converted to two components, C_p and G_p, as shown in Fig. 4.7(b). These parallel components are frequency dependent

$$C_p = C_{sc} + \frac{C_{ss}}{1 + \omega^2 \tau^2} \tag{4.13}$$

$$\frac{G_p}{\omega^2} = \frac{C_{ss} \; \omega \tau}{1 + \omega^2 \tau^2} \tag{4.14}$$

where $\tau = R_{ss} C_{ss}$, the interface state lifetime. The input admittance of this circuit is

$$Y_{in} = G_{in} + j\omega \; C_{in} \tag{4.15}$$

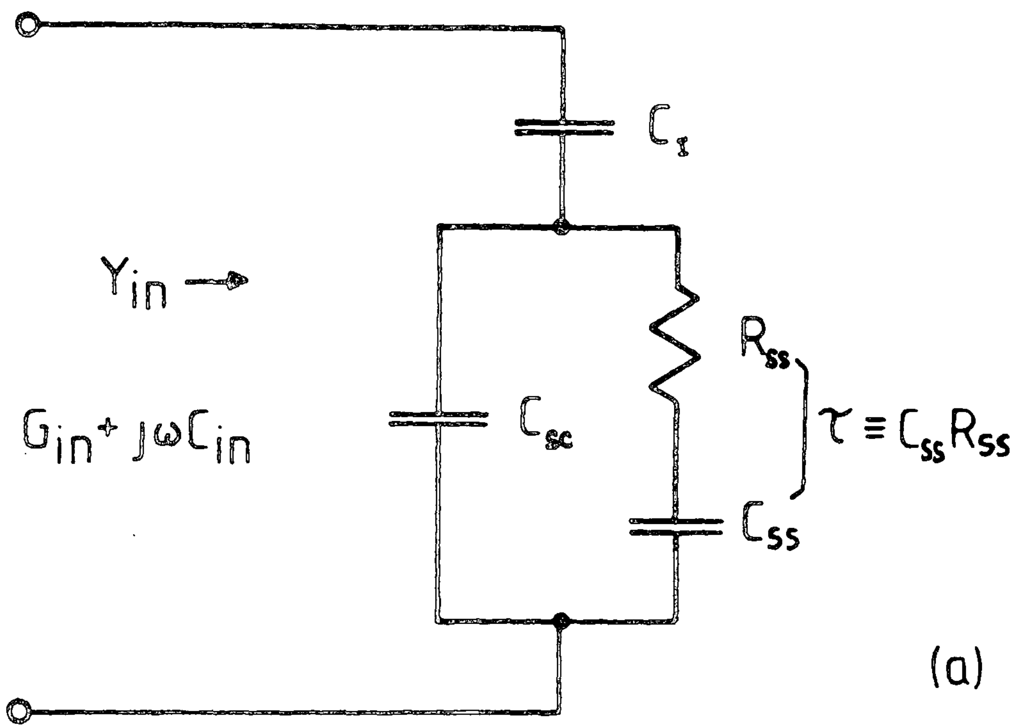
where

$$G_{in} = \frac{\omega^2 C_{ss}{}^2 R_{ss} C_I{}^2}{(C_I + C_{sc} + C_{ss})^2 + \omega^2 R_{ss}{}^2 C_{ss}{}^2 (C_I + C_{sc})^2} \tag{4.16}$$

and

$$C_{in} = \frac{C_I}{C_I + C_{sc} + C_{ss}} \left[C_{sc} + \frac{C_{ss} (C_I+C_{sc}+C_{ss})^2 + \omega^2 (C_{sc} C_{ss} R_{ss})(C_I+C_{sc})}{(C_I+C_{sc}+C_{ss})^2 + \omega^2 R_{ss}{}^2 C_{ss}{}^2 (C_I+C_{sc}} \right.$$

(4.17)



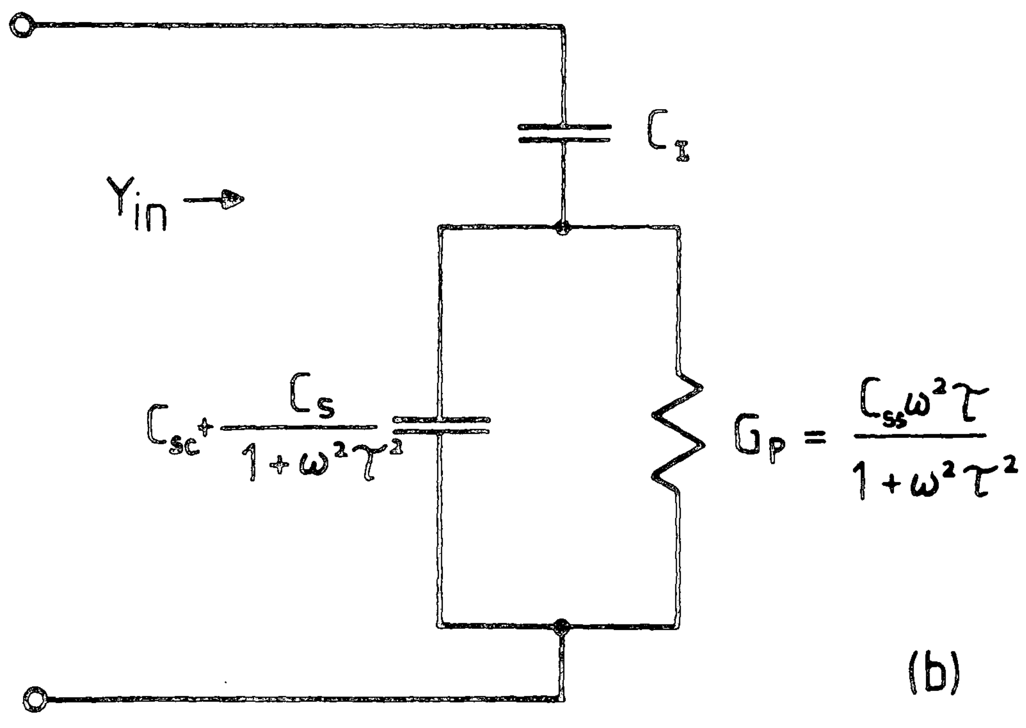


Fig. 4.7 Device equivalent circuits incorporating surface state components (R_{ss}, C_{ss})

Close examination of equation 4.14 reveals that G_p/ω is a function of frequency, with a peak occuring at the value $\omega\tau = 1$ i.e. when the Fermi level crosses the level of the interface state. The value of G_p/ω at the peak is given by

$$\frac{G_p}{\omega}(\max) = \frac{C_{ss}}{2} = \frac{e^2 N_{ss}}{8kT} \qquad (4.18)$$

i.e. there is a direct correlation between the peak height and the surface state density N_{ss}. Hence, the measurement of G_p as a function of frequency can be used for surface state density determination. It should also be noted that the expression for C_{in} (equation 4.17) also contains information regarding the surface states, and so capacitance measurements can be used to find N_{ss}. There are various different methods for determining N_{ss} : these will be discussed in section 4.4.

Unfortunately, experimental conductance curves do not display the single time constant character of the single level model, except in the inversion region. In general, the curves are much broader in frequency and this can be attributed to a continuous distribution of states rather than a single level. Nicollian and Goetzberger(9) have modified their equivalent circuit to account for this, treating the continuous distribution of states as a set of infinitely close single levels. This involves connecting all of the single level networks in parallel. The analysis of this circuit leads to wider conductance curves, but cannot adequately explain the experimental observations: we must consider another factor.

Two distinct approaches have been taken in an attempt to correlate theory and experiment. The tunnelling model proposed by Preier(10) assumes that the interface states are not located at the interface, but are distributed throughout the insulator, and that they communicate with the semiconductor

via tunnelling. However, this theory is not widely accepted because most workers have not been able to fit their data to the proposed model. The alternative theory of Nicollian and Goetzberger[9] is based on the assumption that the fixed charges and charged interface states are distributed at random, causing local fluctuations in the field at the semiconductor surface i.e. fluctuations in the surface potential. In the analysis, the previous expressions for C_p and G_p are integrated over the various values of ψ_s, resulting in parallel conductance versus voltage curves which have their maxima at different frequencies, ensuring a broader G_p/ω versus ω curve. Unfortunately, the expressions for the various parameters are far from simple and one has to rely on computer curve fitting techniques to extract their values from experimental data. It is noteworthy that the use of this 'complete' analysis only makes a small numerical difference in the final value of N_{ss} (a factor of 2 or 3).

4.3.3 Surface Charge and Insulator Space Charge

The presence of charge at or near the semiconductor-insulator interface modifies the surface potential ψ_s and results in deviations from the ideal case. This charge can exist at or near the interface and also in the bulk of the insulating layer. Surface charge is generally defined as a charge distribution located within $\sim$ 100 Å of the interface whose magnitude does not vary, even when ψ_s is changed. The charge density is largely determined by the device fabrication conditions, most notably the semiconductor preparation and the insulator deposition procedure. The effect of such a charge on the MIS capacitance curves is to shift the curves laterally i.e. along the voltage axis. For example, the introduction of fixed positive charge at the interface of an MIS device reduces the electric field at the semiconductor surface, since, as shown in Fig. 4.8, some of the field lines will terminate on positive charges. This means that more surface charges

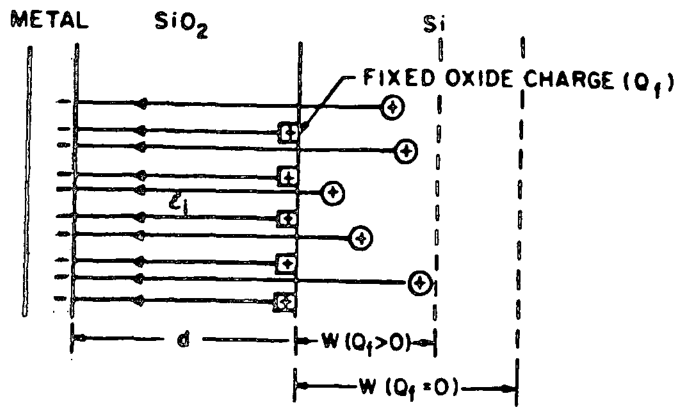


Fig. 4.8 Effect of fixed surface charge on MIS diode

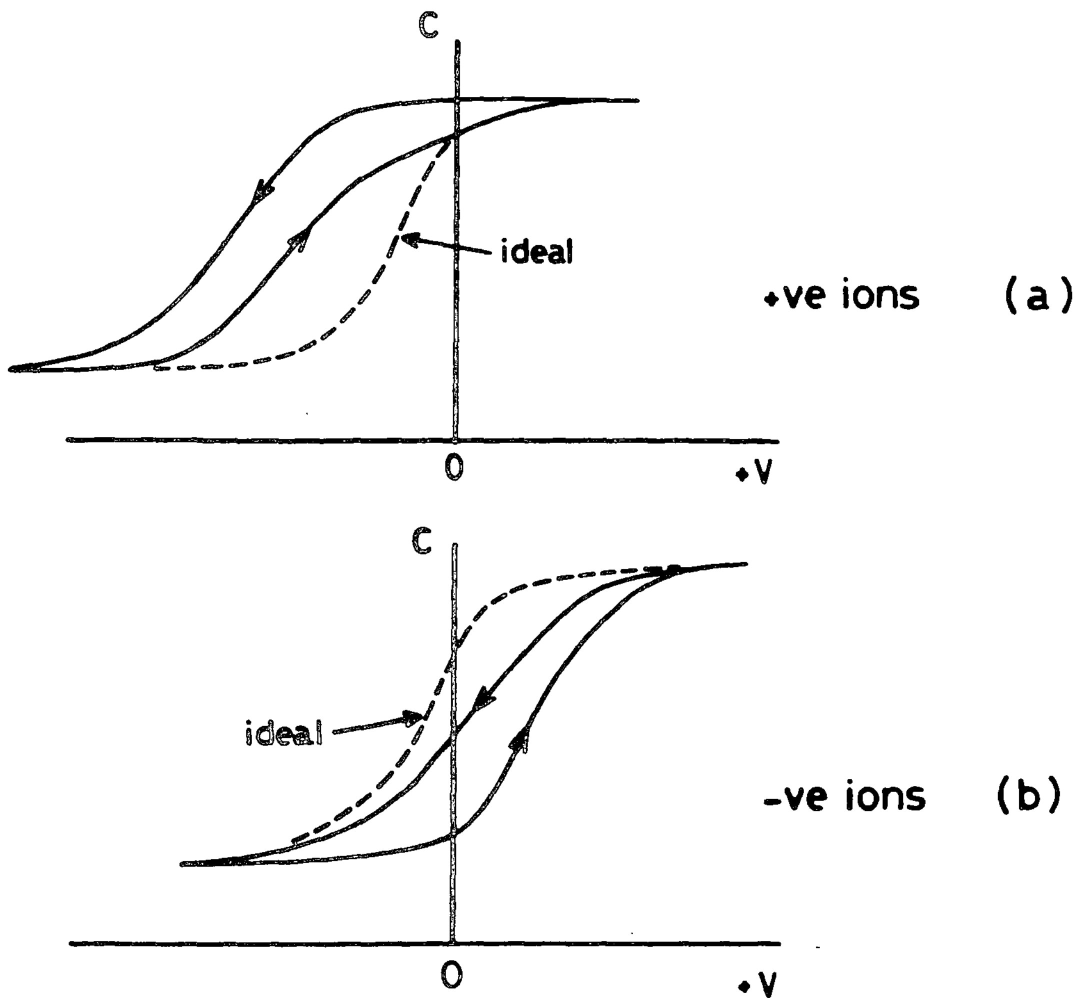


Fig. 4.9 Hysteresis effects in an n-type MIS device (a) due to positive ion movement (b) negative ion movement.

on the metal are needed to produce a given field at the semiconductor surface. That is, it requires a higher bias voltage to produce a given surface potential. The voltage shift ΔV is given by the following simple expression

$$\Delta V = \frac{Q_{fc}}{C_I} \qquad (4.19)$$

where Q_{fc} is the fixed charge and C_I the insulator capacitance.

Mobile ions in the insulating layer are, perhaps, the major contributing factor to instabilities in MIS devices. Under the influence of an applied field the ions can drift, causing a measure of irreproducibility in results and complicating their analysis[11]. Consider an n-type MIS device containing positive ions. When a positive bias is applied the ions will be repelled from the metal top electrode to the semiconductor interface, where they will reside. Under a negative bias the ions will drift back again to the metal/insulator interface. Providing that the drift mobility of the ions is reasonably high and the bias voltage ramp speed is fairly slow, the ions will be able to respond to the ramp signal. Under these conditions the capacitance-voltage curve will be shifted towards reverse bias compared with the ideal curve. The movement of the ions will also tend to distort the shape of the curves. If the ramp speed is increased then the ions will not be able to respond immediately to the changing bias and the capacitance-voltage curves will show a hysteresis effect. Again, assuming positively charged ions, forward bias ramping produces a curve which is shifted towards reverse bias. The return bias voltage sweep gives a curve falling between this curve and the ideal one, its exact position depending on the ion mobility and the ramp speed. This is illustrated in Fig. 4.9(a). Also shown is the effect due to negative ions, where the shift is in the opposite direction (see Fig. 4.9(b)). It is worth noting

however, that the direction of hysteresis is the same for both types of ion.

Hysteresis of a similar direction can also occur as a result of polarising the insulating layer. This can take place with high fields which align the dipoles in the insulator: a given field in the opposite direction is then required to reorientate the dipoles, and this causes hysteresis. The large effective dipole layer in the insulator also shifts the curve laterally from the ideal case.

Charge injection into the insulator is another source of hysteresis. The injection may be from either the metal or the semiconductor, or both, depending on the initial bias conditions. Some of the injected carriers remain at the semiconductor/insulator interface, whilst the rest drift through the insulator and are trapped there. The trapped charge shifts the C-V curves along the voltage axis. If the metal injects, the sense of the hysteresis is the same as for the processes already described i.e. anti-clockwise. Injection from the semiconductor is easily recognised from its clockwise hysteresis direction. In cases where both contacts inject, the trapped carriers from the semiconductor usually dominate because of their proximity to the semiconductor/insulator interface. Carrier injection is a difficult problem to evaluate as both the injection rate and the carrier mobility are difficult to measure.

4.3.4 Temperature Changes

Increasing the temperature of an MIS device moves the Fermi level through the semiconductor bandgap towards the conduction band. This leads to a progressive shift in the C-V curve but, under ideal conditions, no band bending. If, however, there are surface states, moving the Fermi level alters their occupancy and changes the charge at the interface. The amount of band-bending will change and so will the flat-band voltage, V_{FB}.

Temperature changes also affect the inversion region of the C-V curve. The inversion layer charge can only communicate with the semiconductor bulk by means of generation-recombination (i.e. under steady state conditions). Increasing the temperature increases the inversion charge generation rate, which facilitates the more rapid formation of such a layer. Hence, raising the temperature at a given frequency increases the reverse bias capacitance, giving a 'low frequency' type response. Fig. 4.10 illustrates this effect.

4.3.5 Illumination

The effect of illumination is similar to that of raising the temperature i.e. it is seen mainly in the inversion region. Under illumination the capacitance in inversion approaches the low frequency value. In contrast to the temperature effect, illumination is a non-equilibrium situation because the light only penetrates a narrow region at the semiconductor surface. In this region two main processes take place. Firstly, the minority carrier generation time constant is decreased. Secondly, electron-hole pairs are formed in the surface region, causing a decrease in ψ_s for a given applied bias. This means that the space-charge layer is reduced in width giving a corresponding increase in capacitance. Both mechanisms enhance the inversion region formation, although the latter mechanism is dominant at high frequencies. The conductance is also affected by the large density of photogenerated carriers at the semiconductor surface. In general, the magnitude of the conductance peak is greatly increased under illumination. This effect has been studied by Poon and Card[(12)] who have used illuminated C-V and G-V data to measure the surface state density at the Si/SiO_2 interface.

4.3.6 Substrate Resistance

An ideal MIS device has an infinite resistance. Obviously this is not the case in practice as the substrate will have a finite resistance R_s.

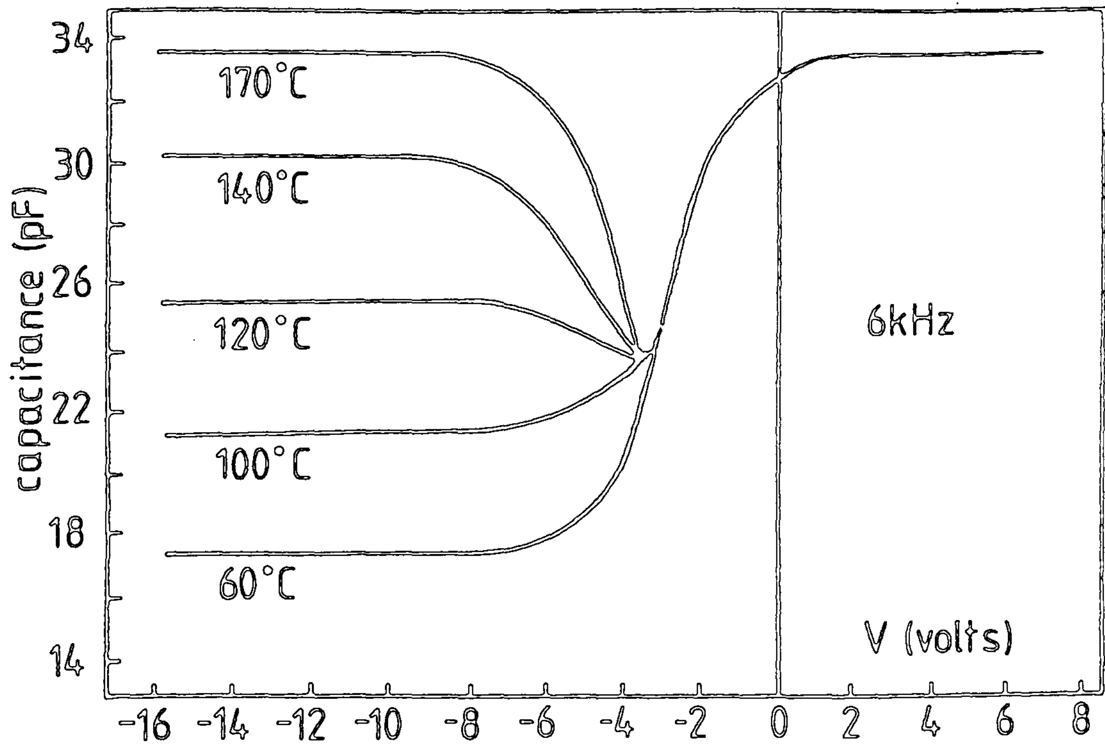


Fig. 4.10 The effect of temperature variation on C-V curves.

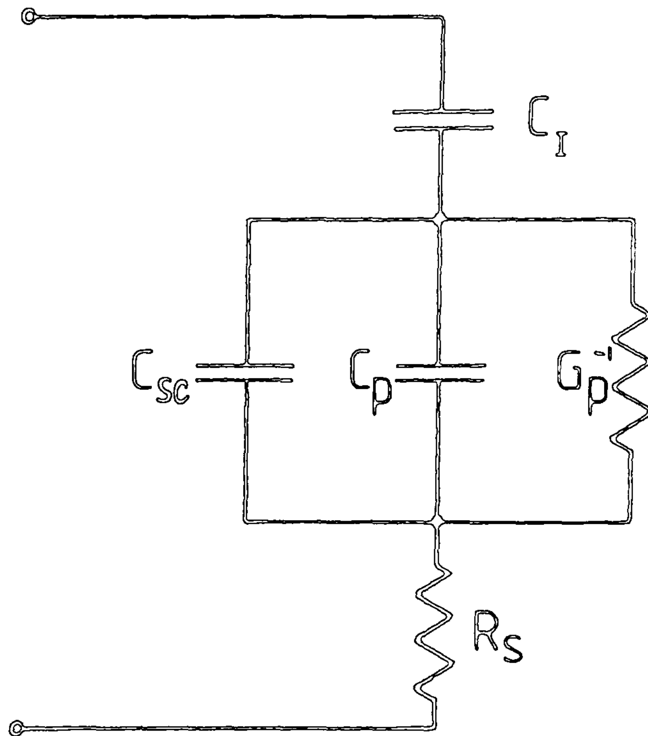


Fig. 4.11 Device equivalent circuit showing additional components to allow for substrate resistance.

This is easily included in the equivalent circuit (see Fig. 4.11), the main effect on the device characteristics being an increase in the background conductance, manifesting itself in a sharp rise in the measured conductance as accumulation is approached. The value of capacitance measured in accumulation is also slightly affected, falling from its ideal value of C_I. These changes are expressed in the equations

$$R_s = \frac{G_m}{(G_m^2 + \omega^2 C_m^2)} \tag{4.20}$$

and

$$C_I = C_m \left[1 + \frac{G_m^2}{\omega^2 C_m^2} \right] \tag{4.21}$$

where G_m and C_m are the measured conductance and the measured capacitance respectively.

Poor ohmic contacts have a similar effect on the device characteristics, the barrier acting somewhat like an additional series resistance. Accurate modelling of such a contact is very difficult because of the frequency and voltage dependent nature of the barrier.

4.3.7 Surface Leakage

The surface inversion layer in an MIS device communicates with the bulk semiconductor by means of recombination-generation. For high reverse bias and relatively high frequencies (i.e. above the 'cut-off' frequency) the inversion layer is unable to respond quickly enough and the C-V curves display only the accumulation and depletion characteristics of the device. However, under certain conditions the inversion layer can have a marked influence on the characteristics. This behaviour was first reported by

Nicollian and Goetzberger[13] who observed a rising capacitance in inversion (i.e. 'low frequency' behaviour), even at frequencies of a few MHz in Si/SiO_2 MIS devices, where the cut-off frequency is normally about 100 Hz. They also reported two distinct peaks in the G-V curve, compared to the usual single peak. These results can be explained in terms of a lateral a.c. current path due to the inversion layer (shown schematically in Fig. 4.12 (a)). Current flows through the insulator as a displacement current and spreads out through the high conductivity inversion region. It then flows across the depletion region in an area much larger than that of the top electrode, causing an increase in the semiconductor capacitance without any need for recombination or generation. The equivalent circuit proposed by Nicollian and Geotzberger to explain this effect is shown in Fig. 4.12(b). It contains two extra components, R_c and C_c, representing the lumped resistance and capacitance of the channel outside the top electrode area. R_F is the inversion layer resistance. The agreement between the response of this circuit and experimental data is good. The appearance of a second conductance peak is shown to be due solely to the surface leakage. Thus, it may be said that the presence of any surface leakage gives rise to anomolous a.c. characteristics.

4.3.8 Amorphous Semiconductors

Tunnelling MIS structures based on α-Si:H (including Schottky barriers which invariably contain an interfacial layer) were discussed extensively in the previous chapter. It was shown that such diodes exhibited characteristics (in particular capacitance-voltage and-frequency characteristics) which differ markedly from those of single crystal MIS devices. This is because the space charge in the α-Si:H arises from the occupation of the localised gap states and not (as in a single crystal) from the 'uncovering' of ionised impurity atoms. As a result, the space charge is not constant throughout the depletion region and the barrier profile is modified[14,15].

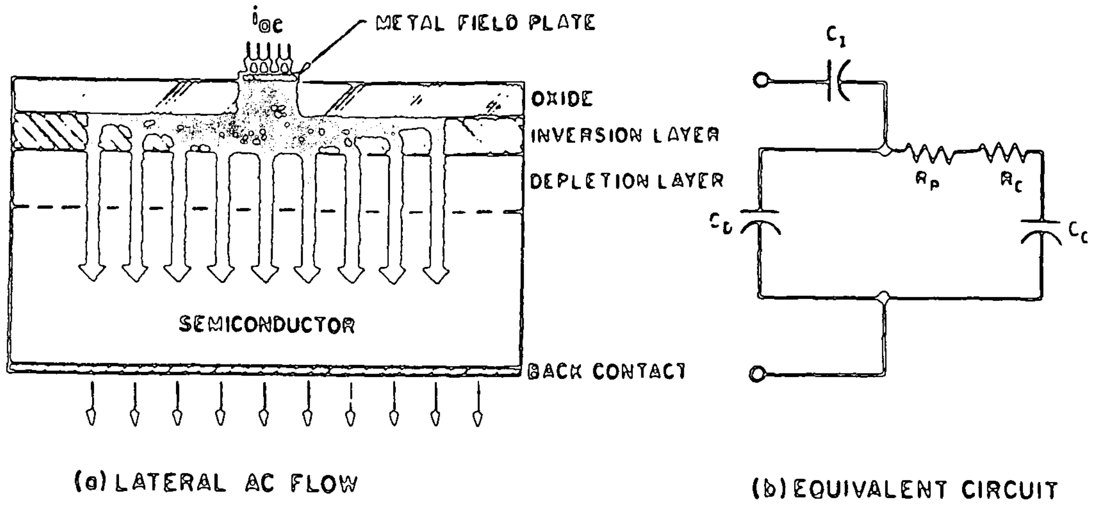


Fig. 4.12 (a) Lateral a.c. flow pattern (b) Equivalent circuit (after ref. (13).

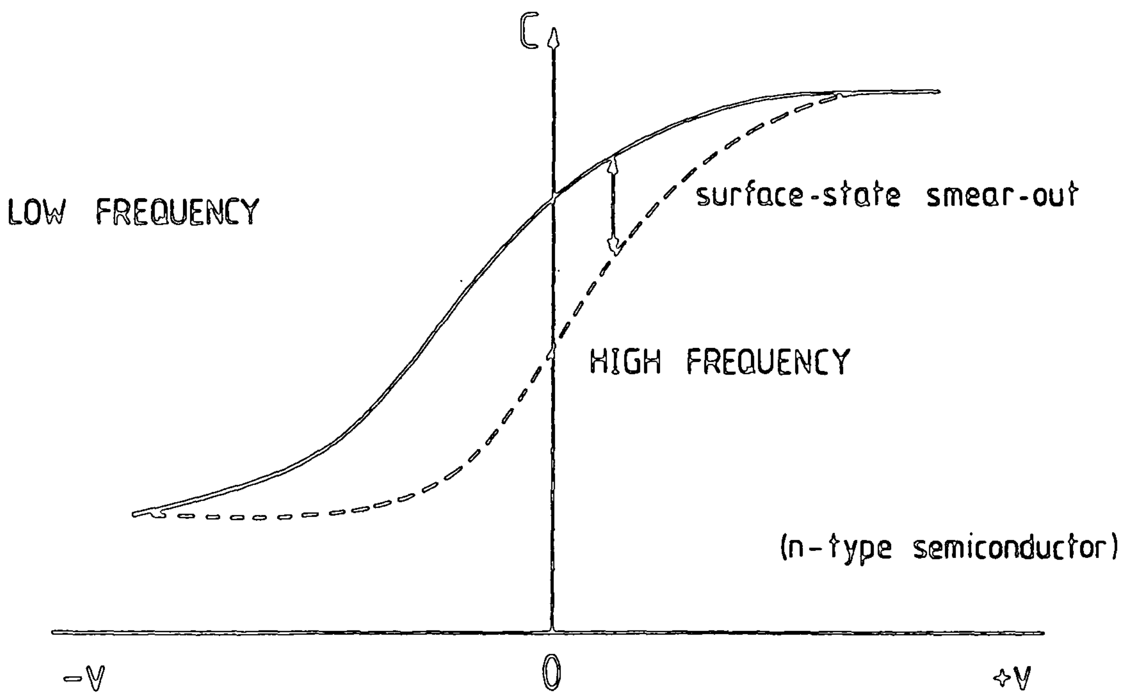


Fig. 4.13 High and low frequency capacitance curves illustrating the effect of surface states.

Furthermore, these localised states have relatively long time constants which alter the device response to a time varying signal.

Most of the work on non-tunnelling MIS devices on α-Si:H has been orientated to transistor measurements e.g. the field-effect technique (see section 2.4.1) and direct i.g.f.e.t. applications (see section 2.7): there is very little published admittance data. However, in principle the situation is not vastly different from that described above for a tunnelling device, and so the comments regarding the origin of the space charge and the barrier profile are still applicable. The time constants of the localised states are likely to result in a complicated frequency response. If all of the states can respond to the applied signal, the device characteristics should be fairly ideal. Dohler et al[16-18] have taken this approach and in their admittance measurements have calculated the frequency/temperature combinations necessary to ensure a total gap-state response. Their C-V data are very similar to ideal single crystal-type curves. If, on the other hand, the frequency and temperature are such that some or all of the states cannot respond, then one would expect C-V characteristics whose shape is rather different. Thus, the use of an amorphous semiconductor may be regarded as a deviation from an ideal, thick insulator MIS device because of response-time problems.

4.4 Measurement of Surface State Density

Many different methods exist for measuring the surface state density N_{ss}, but they fall into two main categories: those which measure charge in (quasi) equilibrium with the applied electric field, and those which rely on the transient charging and discharging of the surface states. The choice of a particular method is not straightforward, depending on the ease of sample preparation, the viability of the required electrical measurements and the complexity of the data analysis. Only those methods which are

relevant to this thesis i.e. those based on MIS devices will be discussed here. There are other techniques, such as the charge pumping technique which require MIS transistor structures, which will not be described.

4.4.1 Capacitance Techniques

The frequency of measurement is an important variable in governing the capacitance characteristic of a real MIS device. At high frequencies the surface states cannot respond to the applied signal and their contribution to the device capacitance will be zero. However, they will manifest their presence because of the charge stored in them, shifting the C-V curve from the ideal case[19]. This displacement is proportional to the amount of trapped charge Q_{ss} that appears for various band bending positions. At each energy value

$$Q_{ss} = C_I V_{shift} \tag{4.22}$$

and so

$$N_{ss} = \frac{Q_{ss}}{e} = \frac{C_I}{e} V_{shift} \tag{4.23}$$

Hence a graph of N_{ss} against applied bias can be obtained. Unfortunately, this method, known as Terman's technique, is very sensitive to errors in the determined value of C_I and takes no account of surface potential fluctuations, which will introduce spurious surface state densities.

At very low frequencies the surface states contribute directly to the device capacitance. A comparison of high and low frequency curves shows a 'smear out' effect due to surface states (see Fig. 4.13). The frequency must be much lower than the reciprocal time constants of the interface states and of minority carrier generation/recombination if the surface states are to respond. Typical values of frequency required for maintaining thermal equilibrium are less than 1 Hz. Although possible (see ref. (20), a.c.

capacitance measurements in this frequency range are difficult to perform. The low frequency technique is perfected in the quasi-static approach of Kuhn[21]. This involves applying a slowly changing d.c. ramp to the sample and is thus equivalent to a zero frequency measurement. The displacement current produced is directly proportional to the differential capacitance at a given bias

$$I = \frac{dQ}{dt} = \frac{dQ}{dV}\,\frac{dV}{dt} = C_{LF}\,\frac{dV}{dt} \qquad (4.24)$$

where C_{LF} is thelow frequency capacitance and $\frac{dV}{dt}$ is the constant ramp rate of the bias voltage, which must be slow so that the quasi-static state is maintained. The surface state density can then be derived from C_{LF}, providing the semiconductor capacitance is known[17]. Particular attention must be given to the experimental details, since the measured displacement current is often less than picoamps. All cables must be carefully screened and stray capacitance minimised. Leakage currents are also a problem : if the insulator is of poor quality electrically the high leakage current may mask the displacement current, making measurements impossible. The technique is, however, fairly quick and straightforward and has become a standard approach in many laboratories.

All of the methods mentioned so far produce information on the surface state density as a function of applied voltage. Often we require N_{ss} as a function of energy position in the bandgap, and this necessitates the conversion of bias voltage to surface potential and hence to the band-bending. Various procedures exist, each with their own particular advantages in terms of accuracy, ease of measurement and theoretical calculations required. They are described in detail in the recent work by Nicollian and Brews[22].

As well as these equilibrium techniques, transient capacitance methods can be used to study surface state distributions. These employ temperature

changes and different biases and sometimes optical excitation to investigate the movement of carriers to and from trapping levels (see Chapter 2 : section 2.4). Much of the work on these techniques, notably DLTS, has been carried out recently, but they are rapidly becoming a standard approach to supplement more conventional measurements.

4.4.2 The Conductance Technique

This technique was first used by Nicollian and Goetzberger in 1967[9]. As shown earlier, the same information on the surface state density is contained in both the measured capacitance and conductance (as functions of voltage and frequency) of an MIS device. The surface state capacitance must be extracted from the measured capacitance which consists of surface state, space-charge region and insulator contributions: this extraction causes difficulties. Inaccuracies also arise because the difference between two capacitances must be calculated to determine N_{ss}. In contrast to this the conductance arises solely because of the surface states, making the extraction of N_{ss} more simple. Furthermore, the effect of frequency on the conductance is much greater than on the capacitance. This is shown in Fig. 4.14 where a change in frequency from 5 kHz causes a 14% change in C and a 100% change in G. Thus conductance measurements can yield more accurate and reliable results than capacitance methods.

Experimentally, the conductance technique involves measuring the small signal admittance (as capacitance C_M and conductance G_M) of the device as a function of frequency and bias. C_M and G_M (see Fig. 4.15(a)) are related to the surface state density by means of equivalent circuits. In these circuits the response of the device is represented by different components, some of which must be subtracted for the N_{ss} analysis. Fig. 4.15(b) shows a typical set of measured characteristics for the equivalent circuit shown in the inset. The semiconductor capacitance C_p, in parallel with G_p, represents both the space-charge layer capacitance and the surface state capacitance. As the

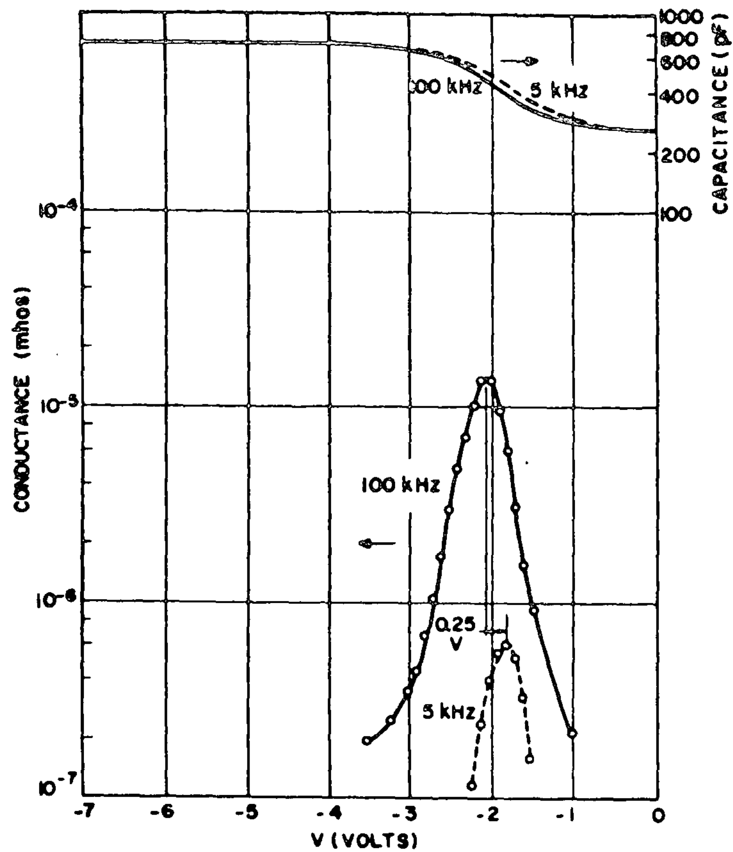


Fig. 4.14 Comparison of MIS capacitance and conductance measurements at two frequencies (after ref.(9)).

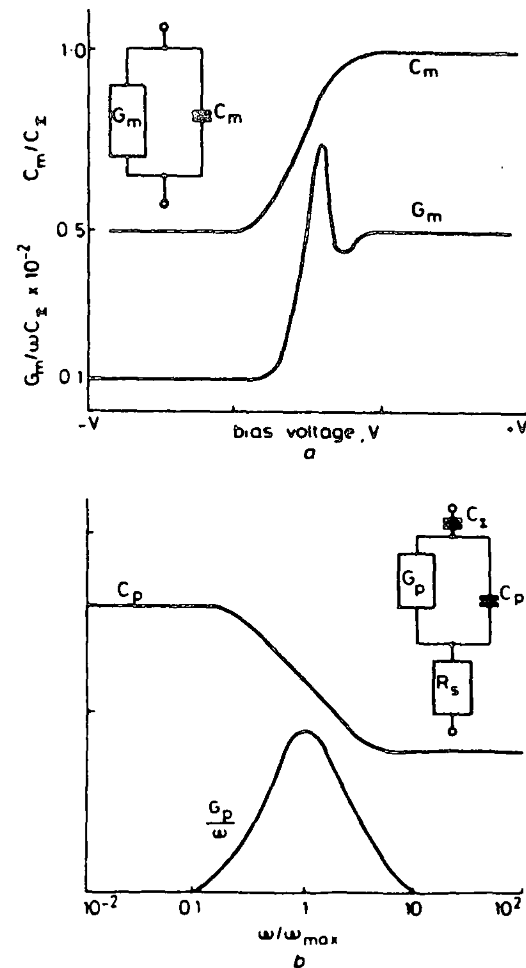


Fig. 4.15 Admittance characteristics of MIS structure and the corresponding equivalent circuits.

frequency decreases the surface state capacitance rises, with a corresponding rise in C_p. The circuit elements C_I and R_s are associated with the insulator capacitance and the device series resistance respectively. Their values may be calculated using equations 4.20 and 4.21. These equations assume that the individual terms are bias and frequency independent. Practically this may not be so e.g. if the insulator has a frequency dependent permittivity this will have to be corrected for at each frequency.

The parallel capacitance and conductance contain all the surface state information and they are dependent on both the frequency and the bias.

$$G_p = \frac{\omega^2 C_I^2 (G_M - \omega^2 C_M^2 - R_s - R_s C_M^2)}{(\omega^2 C_I R_s C_M - G_M)^2 + \omega^2 (C_I - C_M - C_I R_s G_M)^2} \qquad (4.25)$$

$$C_p = \frac{\omega^2 C_I C_M (C_I - C_M) - C_I G_M^2}{(\omega^2 C_I R_s C_M - G_M)^2 + \omega^2 (C_I - C_M - C_I R_s G_M)^2} \qquad (4.26)$$

(both per unit area). To extract N_{ss} from the capacitance data a theoretical value for the semiconductor capacitance would have to be assumed. This causes similar problems to those encountered with the capacitance techniques discussed earlier. The parallel conductance is directly related to N_{ss}, the relation being given by equation 4.18, assuming the single time constant model. This equation would be slightly modified if the continuum model was used. Thus, the peak height of the G_p/ω v ω curve can be used to measure N_{ss}. To relate the N_{ss} values to the surface potential, one can use the normal techniques (see last section) or use the value of C_p in the depletion region[23].

The usual experimental procedure is to measure the device capacitance and conductance with respect to bias at different frequencies. These data are replotted as parallel conductance, G_p (correcting for R_s and C_I) against bias. Finally, G_p/ω against ω is plotted for particular bias values, each corresponding to a certain amount of band bending i.e. a certain energy in the bandgap. The surface state density for each energy is then obtained from the peak height (G_p/ω max) if the curve shows a single-time constant response. If the continuum model is more applicable, then N_{ss} depends on the peak height and width. There are a number of methods for evaluating N_{ss}. The original approach, proposed by Goetzberger et al[24], involves comparing experimental curves with standard curves, and is very time consuming. Simplified methods which do not require curve fitting are possible e.g. the Simonne technique[25], where N_{ss} is found directly from a standard curve, using only the ratio of (G_p/ω) max compared to G_p/ω at a frequency a factor of five different. Even so, lengthy calculations are required although these can be obviated by the use of microcomputers. Martin et al[23] have described such a system which employs a modified version of the Simonne technique.

4.5 Field Effect Transistor Principles

The principle of the surface field effect transistor (F.E.T.) dates back to the early 1930's[26, 27], although it is only during recent years that such devices have been commercially exploited. In general terms, the operation of an FET depends on the electrostatic modulation of a current flowing between two electrodes (known as the source and drain) on a semiconductor. Control of the source-drain conductance is effected by the modulation of the space charge region under a control gate, which is situated between the source and drain electrodes. This space charge region may be created using a Schottky Barrier, a p-n or heterojunction, or a dielectrically insulated metal gate. The latter category, known as the

insulated gate (or MIS) field effect transistor (IGFET), is a logical extension of the MIS capacitor described earlier, and it is this type of device which forms the basis of the present very large scale integrated circuit technology e.g. microprocessors and semiconductor memories.

The basic structure of an IGFET is illustrated in Fig. 4.16. It consists of an p-type semiconductor with two n^+ diffusions, which are the source and drain contacts. The metal gate electrode spans the source-drain gap and is electrically isolated from these electrodes by the insulating layer. The most important device parameters are also shown, namely the channel length L i.e. the source-drain spacing, the channel width Z and the insulator thickness d. With no voltage applied to the gate the device consists of two back-to-back n^+-p junctions, and so the only current flowing will be the reverse leakage current of the junction. If a large enough positive voltage is applied to the gate then an inversion layer will form at the semiconductor surface. This will mean that a highly conducting n-type channel will connect the two n^+ source and drain regions, resulting in a large current flow. The conductance of this channel can be varied by changing the gate bias voltage.

The device illustrated in Fig. 4.16 is known as an n-channel device, because of the majority carrier type of the conducting channel. The conversion to a p-channel device structure involves simply exchanging p for n and reversing the polarity of the voltages. Both of these n- and p-channel structures are enhancement type or 'normally off' transistors: a bias voltage must be applied to the gate to enhance the conductivity or to turn the device on. The other main category of IGFET, the depletion mode transistor, will be discussed later. The source and drain contacts have been depicted as diffused n^+-p (or p^+-n) junctions, their purpose being to make good ohmic contacts to the inversion channel. Such contacts can also be achieved using simple Schottky barriers : a metal which forms a

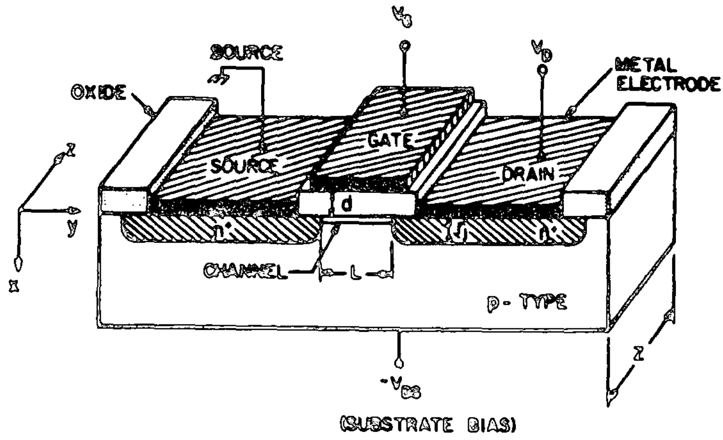


Fig. 4.16 Schematic diagram of a IGFET

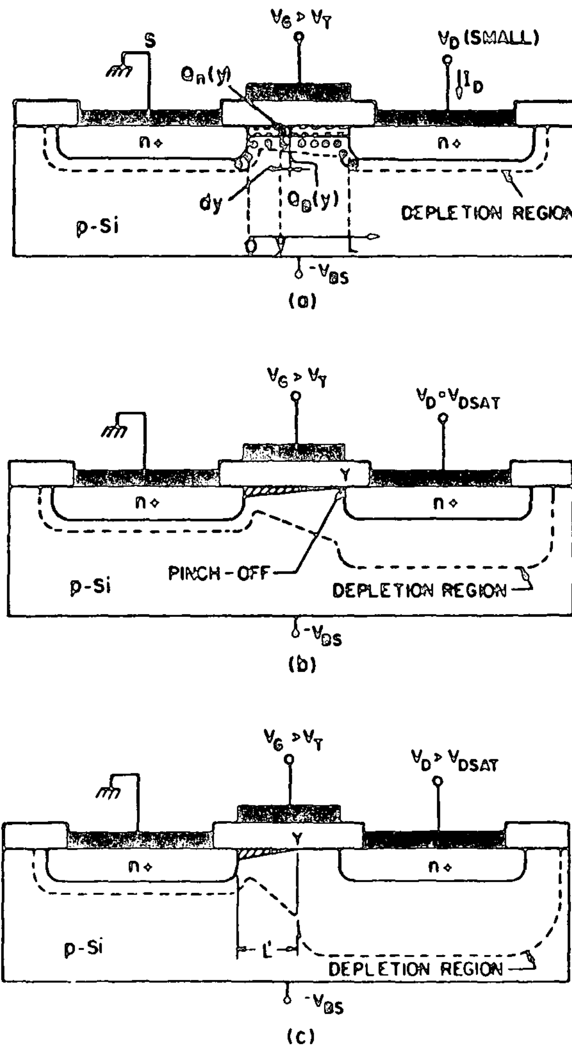


Fig. 4.17 Operating regions of an IGET (a) linear region (b) onset of saturation (c) pinch-off.

Schottky barrier on the bulk semiconductor should form an ohmic contact to the inversion layer.

The operation of an n-channel enhancement FET will now be considered in qualitative terms. Consider a device with a gate voltage applied so as to form a surface inversion layer as shown in Fig. 4.17(a). If a small source-drain voltage, V_D, is applied (assuming the source is grounded) a current will flow through the conducting channel. Under these conditions the channel will act like a resistance, the drain current I_D being proportional to the source-drain voltage : this is the linear region. As the drain voltage is increased the field in the semiconductor near the drain electrode will be reduced, causing a reduction in the depth of the inversion channel. At a certain drain voltage, $V_{D\ sat}$, the depth of the channel will be reduced to zero i.e. the field near the drain contact is not large enough to support an inversion region. This is called the pinch-off point (see Fig. 4.17(b)). At this point the drain current saturates at the value $I_{D\ sat}$, the current flowing through the inversion channel and being injected across the depletion region near the drain. Further increases in V_D simply reduce the effective channel length as shown in Fig. 4.17(c). Typical characteristics of this type of device are depicted in Fig. 4.18 showing the linear and saturation regions. Also shown is the locus of $I_{D\ sat}$ and $V_{D\ sat}$ as a function of gate bias.

A theoretical description of the operation of an FET is not straightforward as it involves three dimensional current flow. The accepted theory is based on a number of assumptions. Firstly, it is assumed that we can consider a cross-section of the device and secondly, that this can be further split into two simpler one-dimensional problems. To do this one must say that the gate voltage appears entirely across the insulator, so that the control field is in the y-direction (see Fig. 4.16), and that the source-drain conduction takes place in a thin surface sheet driven by a field in the x-direction

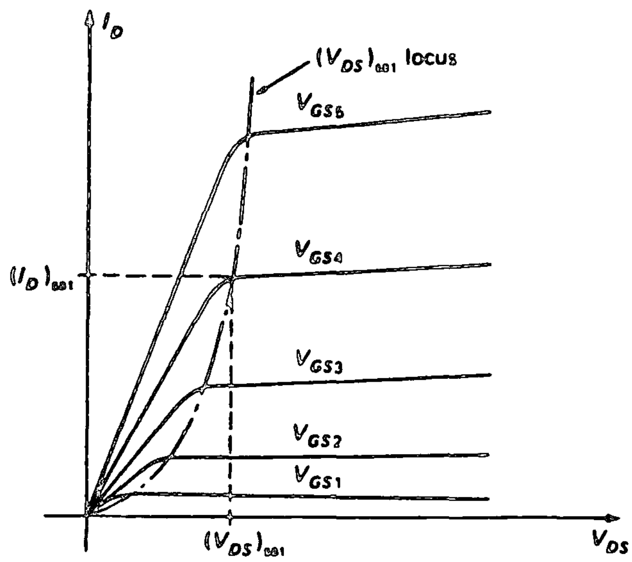


Fig. 4.18 Output characteristics of an n-channel enhancement mode IGFET

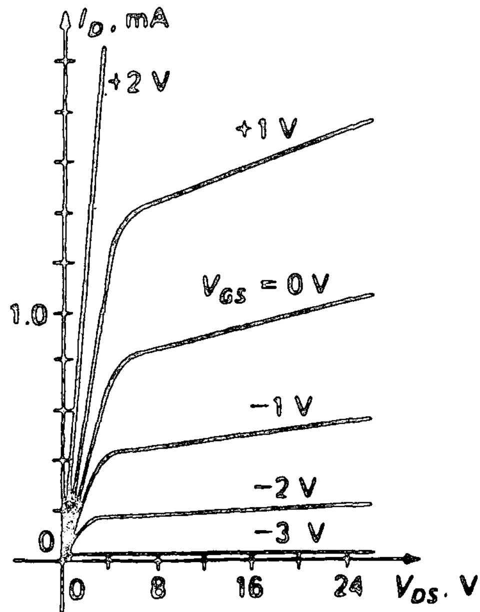


Fig. 4.19 Output characteristics of an n-channel depletion mode IGFET

only. The standard analysis[28] gives the following relations.

$$I_D = \frac{C_G \mu}{L^2} \left[(V_G - V_T) V_D - \frac{V_D^2}{2} \right] \qquad (4.27)$$

where C_G is the gate capacitance, μ is the field effect surface mobility and V_T is the threshold voltage, the minimum gate voltage required to produce an inversion channel. Saturation occurs when $V_D = V_G - V_T$ and so we can write that

$$I_{D\ sat} = \frac{C_G \mu (V_{D\ sat})^2}{2L^2} = \frac{C_G \mu}{2L^2} (V_G - V_T)^2 \qquad (4.28)$$

A measure of the FET gain is given by the transconductance g_M. This is obtained by differentiating equation 4.28 with respect to gate voltage.

$$g_M = \left[\frac{\partial (I_{D\ sat})}{\partial V_G} \right]_{V_D} = \frac{\mu C_G}{L^2} (V_G - V_T) = \frac{\mu C_G}{L^2} V_{D\ sat} \qquad (4.29)$$

This quantity represents the change in output drain current per unit change in gate potential for a given drain voltage in the active region i.e. below $I_{D\ sat}$. The definition of g_M emphasises the voltage controlled nature of an IGFET device.

The alternative mode of operation for an FET is the depletion-mode. The main difference between a depletion device and an enhancement device is that in a depletion-mode device an inversion channel exists even with zero gate voltage. Hence, at $V_G = 0$ the transistor will be turned on. By applying the correct polarity of gate voltage the conductance of the channel can be enhanced by increasing the inversion layer width or reduced

by replacing it with a depletion region. The inversion layer can be produced by a diffused layer, or by charge in the insulator, or by the band-bending induced by the gate electrode. Depletion mode FET's can be made either p- or n-channel. Typical output characteristics for an n-channel device are shown in Fig. 4.19.

The theoretical analysis of a depletion-mode FET is more difficult than that of an enhancement-mode one, because the gate voltage is dropped partly across the insulator, and partly across the space charge region. The simplest approach is to use the enhancement device theory presented earlier with the threshold voltage shifted e.g. for an n-channel depletion mode device V_T will be negative, as opposed to $V_T > 0$ for an enhancement mode transistor. Although this is rather a crude approximation it produces reasonable results, and is commonly used. Various authors have proposed more accurate models of depletion mode devices but these have tended to be rather specific in their application e.g. devices with heavily doped channels, and quite complex in nature[29-31].

Because of the nature of pinch-off in a depletion-mode device the gate electrode need not cover the whole source-drain spacing (since destroying the inversion region in any one part of the channel will interrupt the source-drain current). This is an advantage in that it reduces the gate capacitance, leading to a better high frequency response. Hence, depletion-mode devices are used rather than enhancement-mode ones in high frequency applications.

4.6 Thin Film Transistors

The thin film transistor (TFT) is an insulated gate field effect transistor in which the current is modulated on the same basic principle as the MIS transistor described in the previous section. The differences lie in the fact that all of the component materials, including the semiconductor, are thin films. This means that some of the materials properties

are different, most notably those of the semiconductor which will not be a single crystal, and the modes of conduction are thus more complicated. Fig. 4.20 shows the construction and drain characteristics of a TFT. Comparing this with Fig. 4.18 reveals the similarity in construction between the two types of device. The device characteristics are also very similar to single crystal IGFET's, and to a first approximation one can apply the same theory to both[32].

Several device configurations are possible, and these have been categorised by Weimer[33] as shown in Fig. 4.21. Each configuration has its own particular advantage e.g. ease of construction, avoidance of surface contamination etc. TFT's in general have advantages over conventional silicon MOS devices in that they are generally simpler to fabricate; often the process can be completed without breaking vacuum. The fabrication procedures usually require lower temperatures than silicon technology. The substrates used are commonly glass or ceramic, making electrical isolation of neighbouring devices easy, and also reducing the cost. Difficulties arise in ensuring the quality of the semiconductor layer. Thin films of semiconductor tend to have more defects and imperfections than single crystals, leading to large interface state densities, and it is this more than anything else which has hindered the development of TFT's.

Despite this, TFT's using a variety of semiconductors have been reported e.g. CdS, CdSe, InAs, InSb, PbTe, PbSe and Te[34]. State of the art TFT's have on/off ratios of better than 10^5 to 1, with a device area of $< 25\mu m^2$. Reports of devices with operating voltages of $\sim$ 230V and of devices capable of dissipating 6W on continuous d.c. operation, demonstrate the high voltage and high power capability of TFT's[35]. Thus, even at the present state of development TFT's could be used where silicon technology cannot meet the requirements at a low enough cost. This is the case when a large number of active devices are required to cover a large area e.g. in a solid-state

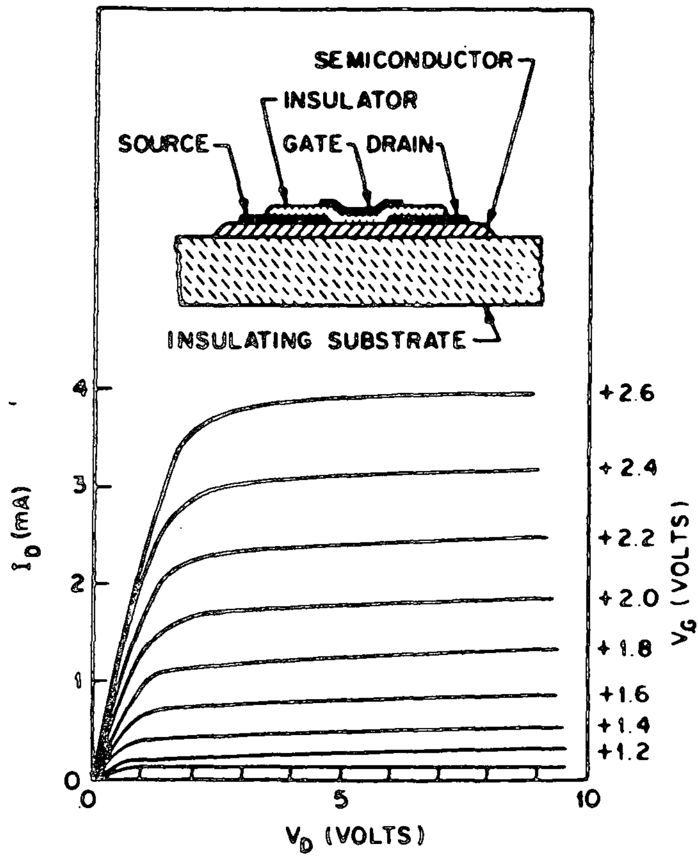


Fig. 4.20 Typical TFT structure and drain characteristics

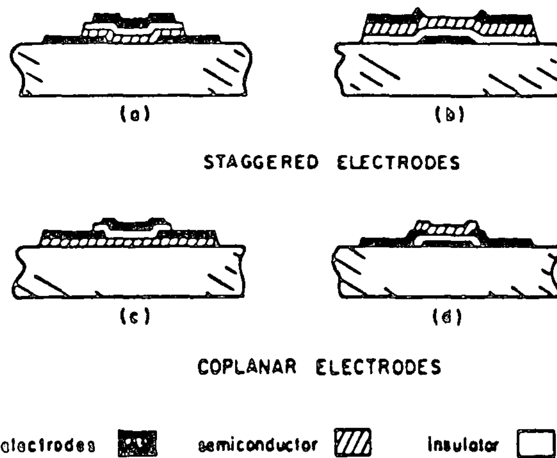


Fig. 4.21 Electrode configurations for TFT's.

flat panel display. Such displays could use liquid crystals or electro-luminescent powders, both of which are compatible with thin film technology. Interconnection problems can be reduced by realising the required logic circuits in integrated form on the edges of the TFT matrix. Indeed, in a fully-integrated display system, addressed and refreshed by a TFT matrix, the only external circuitry required would be the information and memory circuits.

CHAPTER 5

LANGMUIR-BLODGETT FILM TECHNOLOGY

5.1 Introduction

In this chapter the technology of LB films is discussed. The first sections deal with the historical background and the general principles behind LB film deposition. The details of the Langmuir Trough with its associated instrumentation, and the dipping conditions, are also described. Section 5.6 is a review of the electrical properties of LB films, which are of particular relevance to this thesis. The chapter concludes with a summary of potential applications.

5.2 Historical Background

The history of monomolecular films can be traced back to the work of Benjamin Franklin who reported his studies of oil films on water to the Royal Society in 1774[(1)]. Over one hundred years passed, before the first system for the control and manipulation of such films was proposed by Fraulein Pockels[(2)]. She used this equipment, which became known as a 'trough', to measure the variation in surface tension of contaminated water. The first suggestion that these films might be monomolecular, i.e. only one molecule thick, came in 1899 following the detailed studies of Lord Rayleigh[(3)]. However, little significance was attached to any of these reports until the pioneering work of Irving Langmuir at the G.E.C. Laboratories, shortly after the first world war. Langmuir developed the basic theoretical concepts needed to explain previous observations[(4)] and, with the assistance of Katharine Blodgett, succeeded in producing an experimental system capable of controlling the monolayer film formation and transferring the film onto a solid substrate[(5, 6, 7)]. Despite these significant contributions by Langmuir and Blodgett there was little interest due to the instability of the films and a seeming lack of applications.

After the second world war research into monomolecular films was revived. In particular Kuhn produced some elegant work which illustrated the use of monomolecular films in the building of supermolecular structures for optical and energy transfer studies[8]. The current widespread interest in these films, which now bear the names of the researchers Langmuir and Blodgett, has grown rapidly in the last few years following improvements in the design of the deposition system[9] and the synthesis of new materials[10,11]. Many new areas of application have been opened up, stimulating a broad research program in both industry and universities.

5.3 Principles of Langmuir-Blodgett Film Deposition

The principles underlying Langmuir-Blodgett (LB) film deposition are simple, although their practical realisation requires meticulous attention to detail. To prepare these films a suitable organic material is dissolved in a solvent and deposited onto a liquid surface (the subphase). The solvent evaporates, leaving the organic molecules floating on the subphase (see Fig. 5.1(a)). The molecules are enclosed within a barrier system : on compression the film goes through various phase changes analogous to 'gas' and 'liquid' phases and eventually forms a quasi-solid which is only one molecule thick (as in Fig. 5.1(b)). This monomolecular layer can then be transferred to a solid substrate simply by passing the substrate through the surface of the subphase. The thickness of the deposited film is defined precisely by the molecular length. Multi-layer structures can easily be assembled by repeatedly dipping the substrate in and out of the subphase.

There are stringent requirements for all the materials involved in LB film deposition. The subphase, which is usually water, must be very pure so as to avoid any influence on the properties of the monolayer. The monolayer material itself must also be as chemically pure as possible and must satisfy two further criteria. Firstly, it must be relatively insoluble in the subphase, so that the monolayer is not continually being lost into

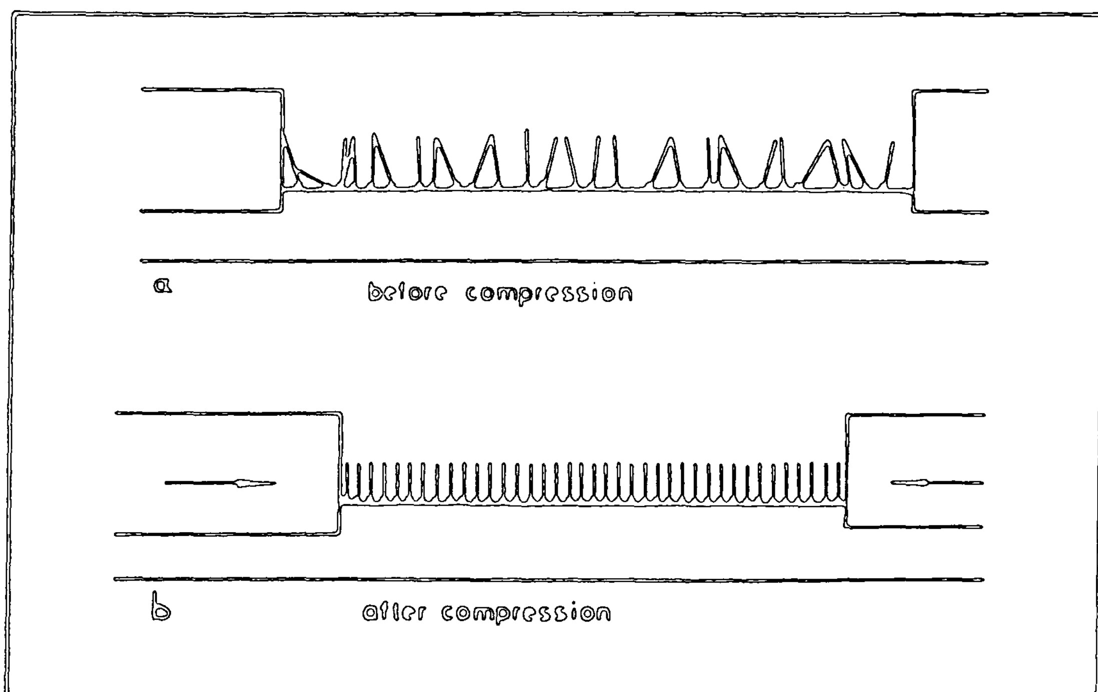


Fig. 5.1 Dispersed molecules on a water surface (a) scattered molecules with their hydrophilic terminations in the aqueous subphase (b) the aligned molecules after compression.

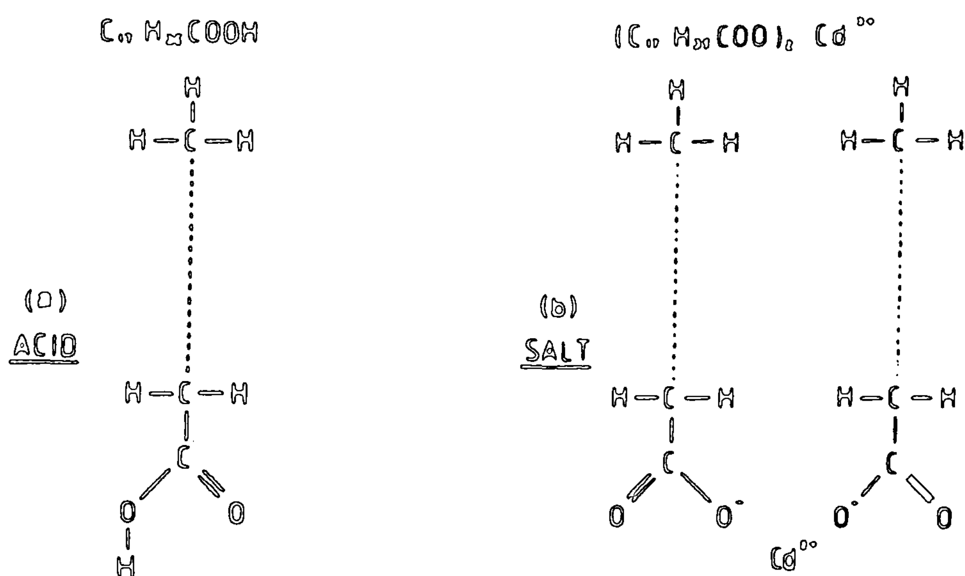


Fig. 5.2 Representation of the chemical structure of stearic acid and its cadmium salt.

solution, and secondly, the molecules must be amphipathic i.e. they must contain a hydrophobic group and a hydrophilic group to give correct alignment on the subphase. Many compounds fulfill these requirements, the most commonly studied being the fatty acids. Other materials which have interesting properties can be modified for LB film work by appropriate chemical substitutions.

The molecular structure of a typical fatty acid, namely stearic acid ($C_{17}H_{35}$ COOH) and its cadmium salt, are shown in Fig. 5.2. The hydrocarbon chain and the methyl group are hydrophobic. The phase changes occurring in a film due to increasing compression can be monitored by measuring the surface pressure (i.e. differential surface tension) as a function of film area. The resulting plot is called an isotherm (if T=const.) and an idealised graph for stearic acid is given in Fig. 5.3. The graph shows regions analagous to gas, liquid and solid phases. In the 'gaseous' phase there is no ordering of the molecules, whereas some ordering is present in the quasi-liquid state. The 'solid' phase corresponds to a tightly packed monomolecular layer with increased interactions between molecules. Further increases in pressure lead to the collapse of the film.

Deposition onto a substrate is effected with the monolayer in the quasi-solid phase. For good quality films the surface pressure must be kept constant, even while the monolayer is being removed, so as to prevent the film entering the liquid phase region. There are three modes of deposition known as X, Z and Y type. Of these three, Y-type is most often seen, and this process is illustrated in Fig. 5.4. As the substrate enters the subphase, a first monolayer may be deposited hydrophobic-end first. (In practice, a monolayer does not always deposit on the first entry.) Subsequent traversals of the water surface pick-up monolayers in a 'head-to-head, tail-to-tail' configuration as shown. In X-type deposition molecules are picked up each time the substrate enters the water, not on withdrawal. Hence, the hydrophobic

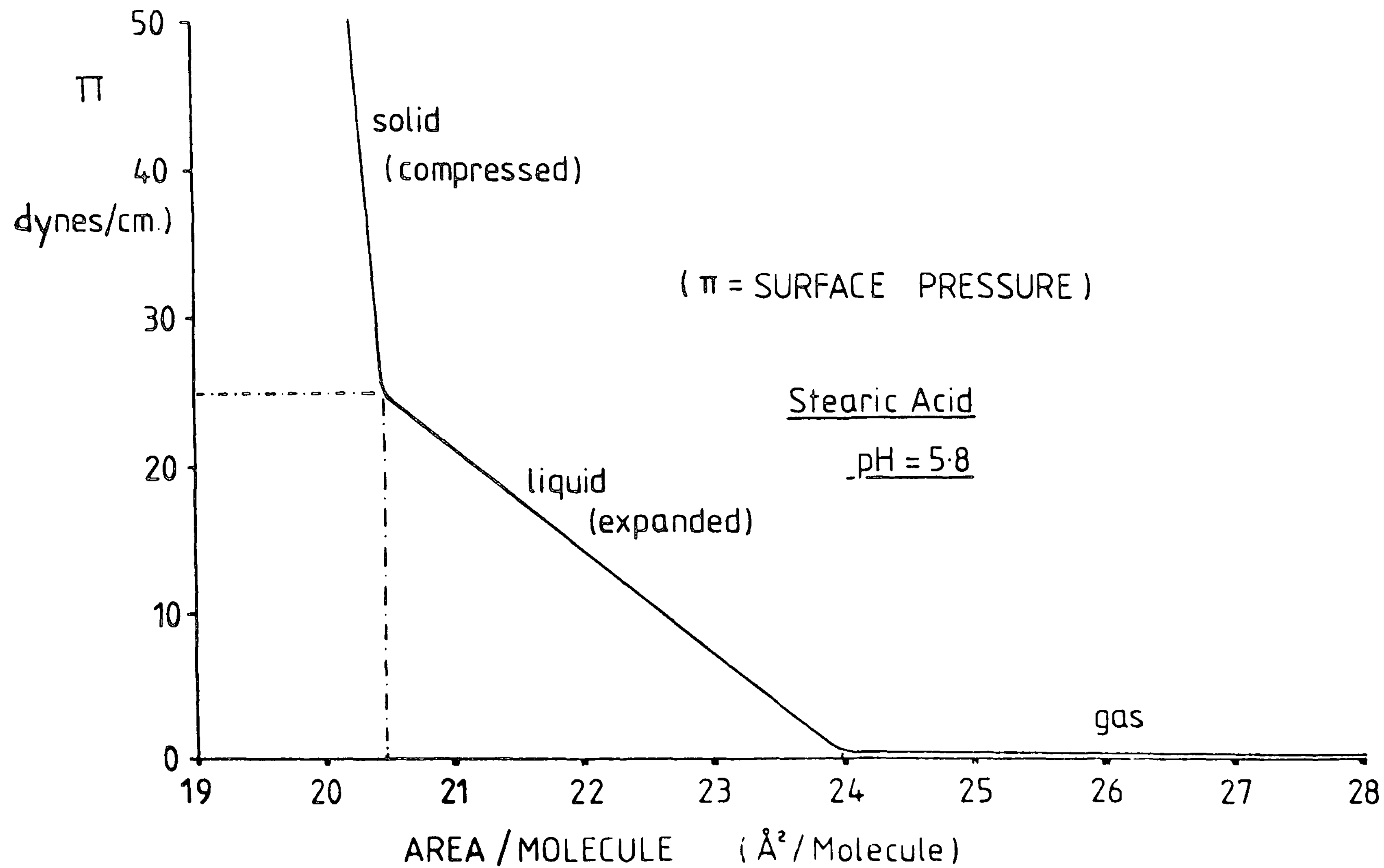
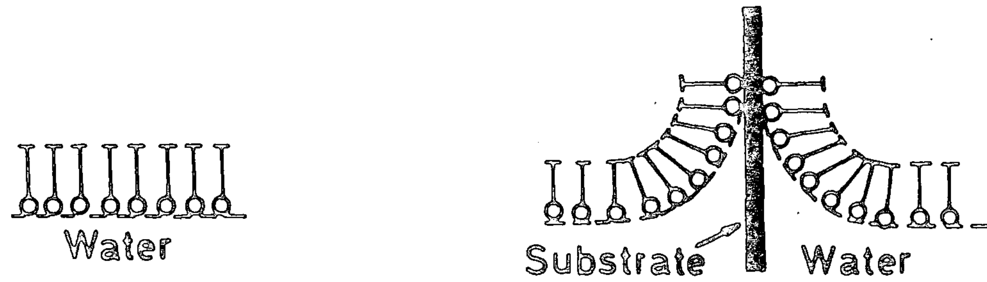


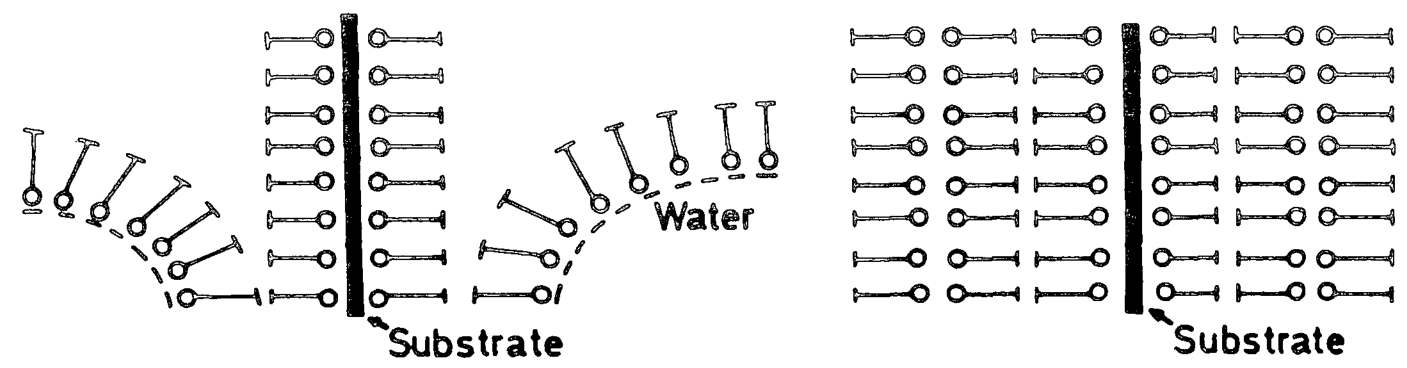
Fig. 5.3 Idealised compression isotherm for stearic acid.



(a) Monolayer on the surface of the water.

(b) First layer on withdrawal.

MONOLAYER DEPOSITION



(c) Second layer (2nd Insertion)

(d) Slide with three layers (after 2nd Removal)

Fig. 5.4 Y-type monolayer deposition

ends will deposit first and subsequent layers will be 'head-to-tail' repeatedly. Z-type deposition also gives the repeated 'head-to-tail' structure, but since pick up is only on withdrawal the hydrophilic end deposits first. These deposition mechanisms are described in detail in Gaines classic book on LB films(12). It should be noted that re-ordering of the molecules may take place after deposition. In particular, X-type structures can revert to Y-type ordering after the film is transferred.

5.4 Deposition Equipment and Instrumentation

The Durham Langmuir trough facility is housed in a class 10,000 micro-electronics clean room which provides a clean, dust-free environment. The basic design of all the troughs is similar and incorporates many improvements and modifications made apparent over seven years of operation. The current systems are relatively sophisticated and reliable, allowing the reproducible deposition of various LB films onto a range of carefully prepared substrates.

A schematic diagram of a Langmuir trough and a photograph of one of the troughs used in Durham are shown in Figs. 5.5 and 5.6 respectively. The trough consists of a piece of soda glass of a U-shaped cross section with end plates clamped in position and sealed with PTFE strips. Wherever possible inert materials are used to avoid contamination problems. The sub-phase is water which has been especially purified to a resistivity of 18 MΩcm using a Millipore 'Milli-Q reagent grade' system. The LB film is enclosed by a constant perimeter barrier apparatus. The barrier itself is made of PTFE coated, glass fibre tape and is supported on a set of PTFE rollers. The surface area enclosed by the barrier can be adjusted by moving one set of rollers across the trough. The barrier is shown in its positions of maximum and minimum area in the inset of Fig. 5.5 (diagrams (a) and (b) respectively). Movement of the barrier is controlled electronically to maintain a constant

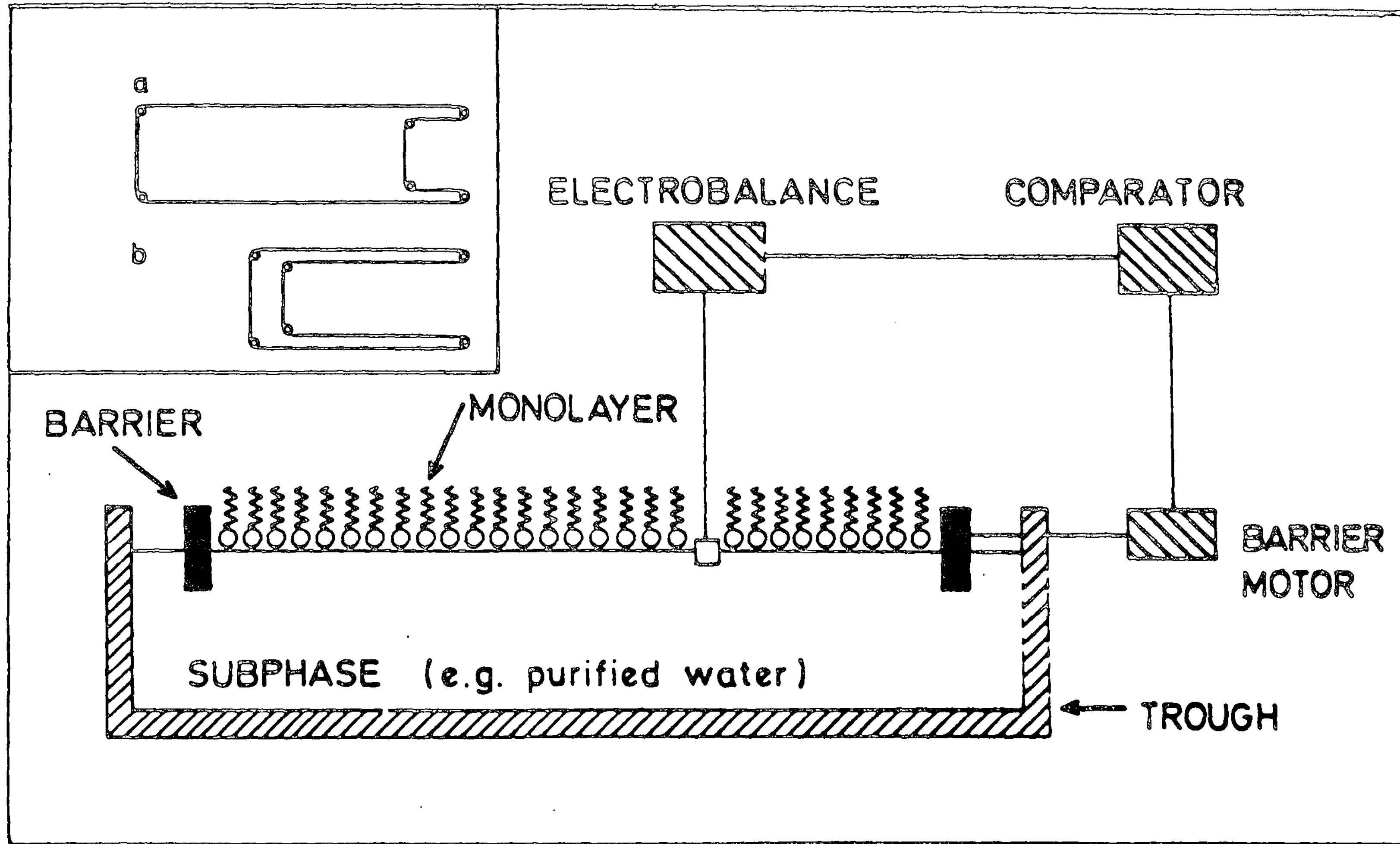


Fig. 5.5 Schematic diagram of a Langmuir Trough.

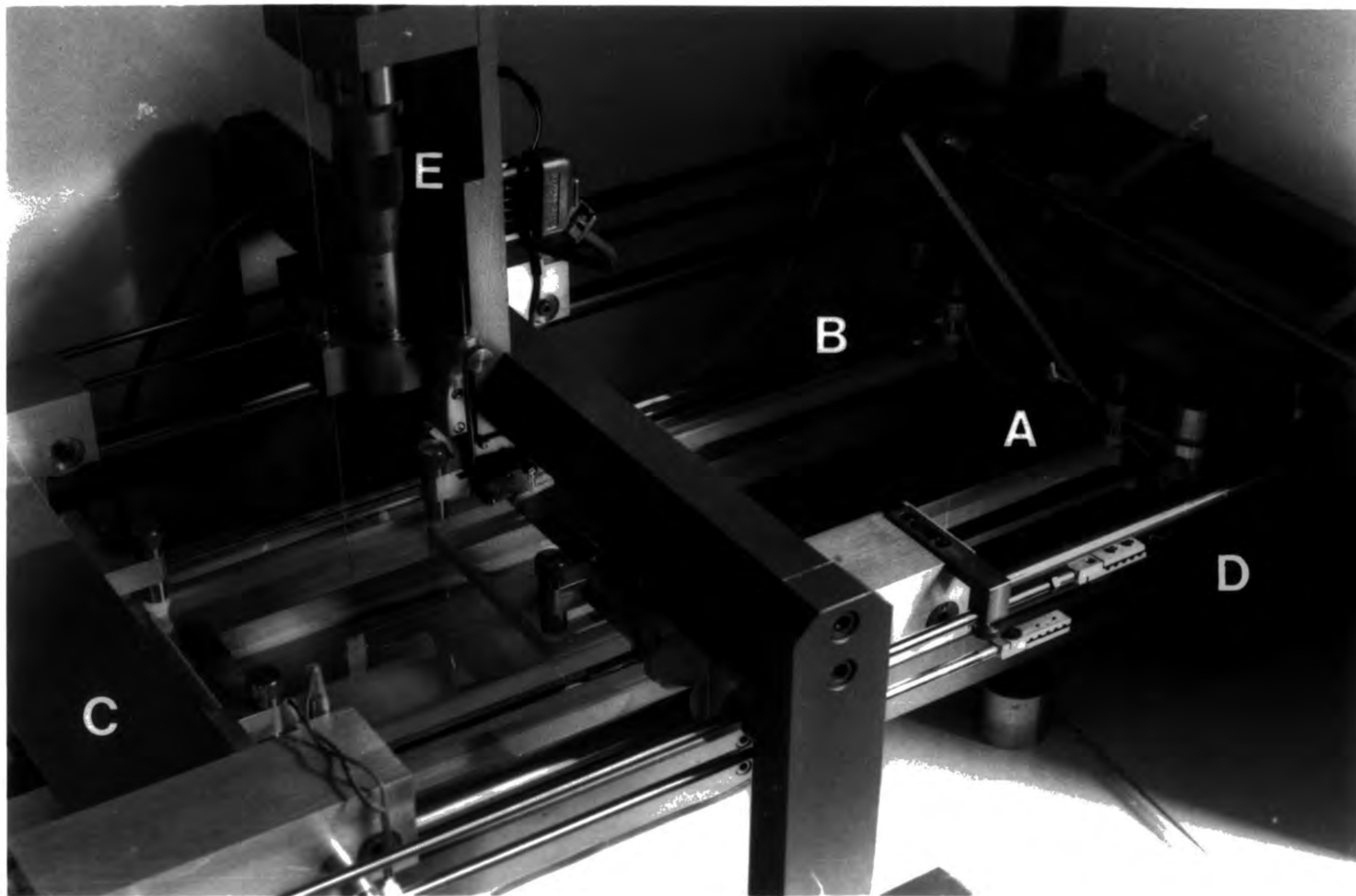


Fig. 5.6 **Photograph of a Durham trough**

A : constant perimeter barrier system
B : glass trough
C : metal beams supporting barrier
D : toothed belt driving the barrier
E : dipping head

surface pressure, which may be set at any value as desired. The surface pressure is measured using a Wilhelmy plate[13] system which converts surface pressure into a vertical force : this force is measured with a sensitive microbalance and the signal is used to control the barrier motor.

The monolayer transfer apparatus consists of a motor driven micrometer screw thread (with variable speed), with a substrate holder attached. The maximum limits of travel (i.e. the upward and downward extent of the dipping) are set by means of microswitches and moveable stop rods. Again, a degree of electronic automation has been incorporated which allows the user to set the required number of dippings and to leave the trough unattended.

The other ancillary equipment to the trough comprises two chart recorders and a pH meter. Isotherms i.e. pressure v. surface area graphs were recorded on a Bryans 2000 X-Y chart recorder. A W and W 312 2X/T chart recorder was used to continuously monitor the surface area and surface pressure with time throughout dippings, thus giving a direct record of the film 'pick-up'. The pH of the subphase is a critical parameter for good deposition. This was measured using a Pye Unicam PW409 pH meter. The pH of the subphase was adjusted as necessary with dilute acid (HCl) or alkali (NH_4OH).

5.5 Deposition Conditions

The work reported in this thesis was based on two LB film materials; cadmium stearate and diacetylene monomer. The different conditions relating to the deposition of these two types of film are as follows. LB films known as 'cadmium stearate' films are actually a mixture of cadmium stearate and stearic acid. Monolayers of pure stearic acid are difficult to transfer to a substrate. This may be overcome by adding some divalent ions to the subphase e.g. Cd^{2+} ions, by dissolving $CdCl_2$ in the subphase. These ions improve the lateral bonding between molecules in the film by converting stearic acid to the salt, cadmium stearate (see Fig. 5.2), and

thus they aid deposition. The proportion of acid which is converted to the salt depends on the pH. Typical conditions used were a 2×10^{-4} molar solution of $CdCl_2$ in the subphase and a pH of 5.7, giving a salt content of approximately 60% in the film[14]. The constant surface pressure was 25 dynes cm^{-1}. Comprehensive details of the dipping procedure may be found in reference[15].

The fatty acids, although simple to work with and well characterised, are not very suitable for device applications, since they have a relatively poor thermal stability. A more promising group of materials is the diacetylenes. An example of this group, known as 12-8 diacetylene, is shown in Fig. 5.7. It can be deposited in the form of a monomer and subsequently polymerised with ultra-violet light. During this polymerisation, chains containing conjugated double and triple bonds are formed, although the integrity of the film is maintained[16]. The deposition conditions used for the monomer were a pH of ~ 6.2 and a surface pressure of 15 dynes cm^{-1}. The subphase contained 2.5×10^{-4} molar $CdCl_2$. Polymerisation was achieved by a 30 minute irradiation with an intense 300 nm source. The temperature of the subphase for all dippings performed (both stearate and diacetylene) was the clean room ambient temperature, which was approximately constant at 17^oC.

5.6 Review of Electrical Properties

5.6.1 D.C. Conduction

The electrical properties of LB films are closely dependent on their structural perfection, since, like most organic solids, conduction can take place through defects. It is only since about 1971 that films of sufficiently high quality for reliable electrical characterisation have been consistently produced. Discrepancies still exist between results reported by various groups, most probably due to slight differences

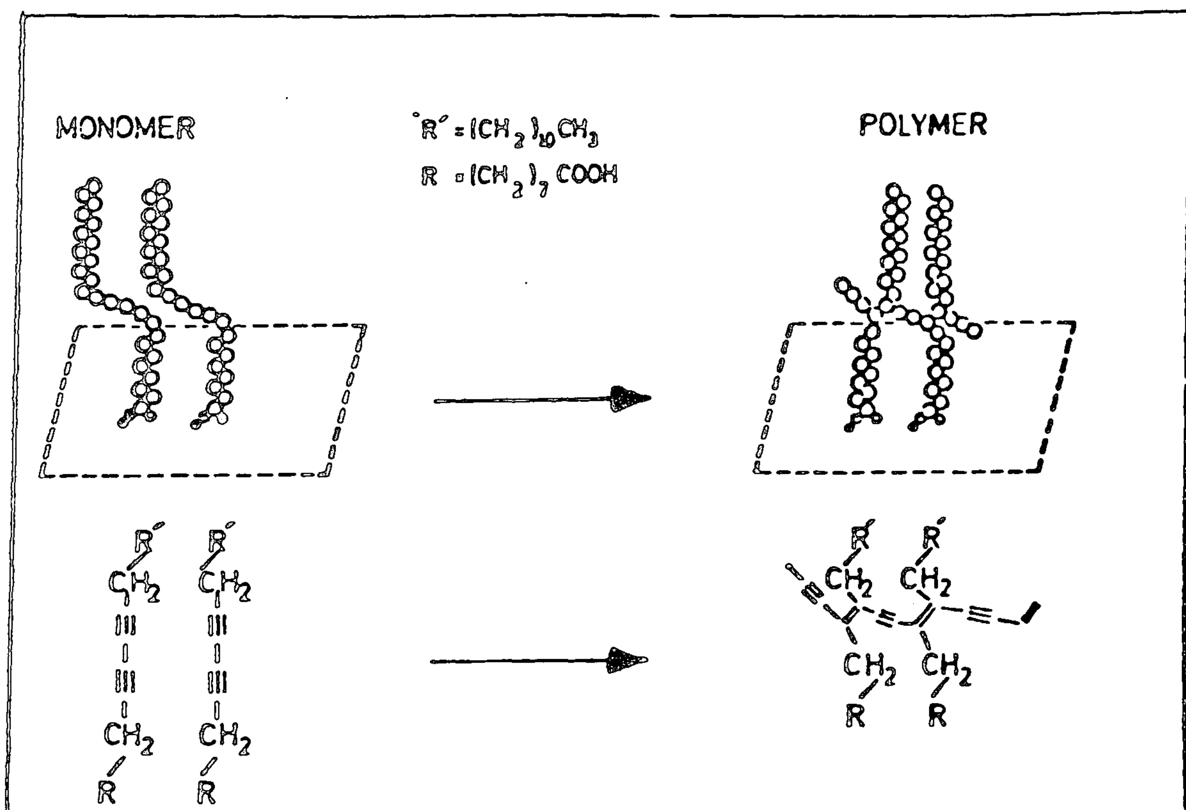


Fig. 5.7. Schematic diagram showing the relationship between the diacetylene fatty acid monolayer (left) and the corresponding polymer produced on uv irradiation (right).

in film preparation, deposition and measurement conditions. For example, some researchers use de-ionised water rather than ultra-pure water as the subphase; differences in pH affect the acid/salt ratio and hence the stability of films, and dipping with different surface pressures causes variations in the lateral compactness of monolayers. Changes in the gas ambient can lead to significant changes in the magnitude of measured currents : air, dry nitrogen and vacuum have been used by various workers. Also, the use of different substrates can lead to irreproducible data. Particular care must be taken with aluminium oxide to ensure consistent oxide growth on successive substrates. Nevertheless, it is possible to paint a broad picture of conduction in LB films.

Electron tunnelling appears to be the dominant conduction mechanism in LB films consisting of one or two monolayers. Evidence for this comes from the work of Mann and Kuhn[17,18] and Polymeropoulos [19] with LB films deposited onto aluminium oxide on glass. The oxide was assumed to be too conducting to affect the results. Using fatty acids of different molecular chain lengths, they independently demonstrated the exponential dependence of the low field tunnelling conductivity on insulator thickness, which is indicative of tunnelling. The temperature invariance of these results[19] and the good agreement between theoretical and measured J-V curves[17, 18] both support this interpretation. Careem and Hill[20] measured tunnel currents for stearic acid monolayers which closely followed the theoretically predicted voltage and temperature dependence over a wide range, although the aluminium oxide base layer gave rise to an additional current component at low voltages. Furthermore, tunnelling has been observed in monolayer MIM structures where one[21, 22] or both of the contacts[23] is superconducting. The unusual log J v $V^{1/4}$ dependence seen by Roberts et al[24] for a monolayer of arachidic acid has also been reported by Ginnai et al[25]. No suitable explanation has yet been found for this,

although the temperature independence of their data is strongly suggestive of tunnelling. Perhaps the most conclusive evidence for tunnelling yet has been presented by Ginnai et al[25]. Their observation of inelastic tunnelling (IET) in single layer barium stearate LB films demonstrates the existence of a large tunnel current, since IET accounts for only 1% of all electron tunnelling. As well as this their data cannot be explained in terms of conduction through pinholes in the LB film.

LB films of 3 or more monolayers are generally too thick for tunnelling to occur. At low fields ie up to about 10^5 Vcm^{-1} (corresponding to a few fractions of a volt applied to typical film thicknesses) fatty acid multilayers pass a current which is roughly proportional to the applied voltage[17,27-2 At high fields, conduction following a $\log J \alpha V^{\frac{1}{2}}$ law is commonly found. This may be the result of one of several conduction mechanisms, namely the Schottky effect, the Poole-Frenkel effect, or tunnelling through field lowered barriers in the film (see Section 3.4). For films in the thickness range 3 to 9 monolayers the current seems to be injection limited by the Schottky Effect. This is inferred from the slope of the reported $\ln J \alpha V^{\frac{1}{2}}$ graphs[20,30], and from the activation energy of the conductivity which is consistent with theory[20]. Honig has published $\ln J \alpha V^{\frac{1}{2}}$ graphs with different slopes in different voltage ranges[27]. The slopes did not fit either the Schottky or Poole-Frenkel theory, although they were closer to the former, and the currents were electrode-dependent, which also suggests that the Schottky effect was dominant. Roberts et al[24] reported $\ln J \alpha V^{\frac{1}{2}}$ behaviour with a weak temperature dependence for fatty acid films on Al_2O_3 and InP. Because of the independence of current on polarity, even with disimilar metal electrodes they have interpreted their results as Poole-Frenkel conduction. Moreover, they were able to calculate the film permittivity from their data with a reasonable degree of accuracy. Poole-Frenkel conduction has also been observed by Careem and Hill[20] and

Nathoo and Jonscher[28], in films of nine or more monolayers. They estimated the distance between the donor-like centres to be approximately equal to the molecular length i.e. the charge carriers hop from molecule to molecule.

Diacetylene polymer has been much less studied, being a relatively new LB film material. However, Kan et al[31] have published data which is quite consistent with those for the fatty acids, namely a $\log J \propto V^{\frac{1}{2}}$ current-voltage dependence.

5.6.2. A.C. Conductance

The frequency dependence of the conductance of fatty acid LB films has been studied by a number of researchers. The conductance varies according to

$$G \propto \omega^n \tag{5.1}$$

where ω is the angular frequency and n lies between 0.5 and 1. Two contributions to the a.c. conductivity may be identified[32, 33]. The first, which dominates at frequencies greater than 1 Hz, has been associated with the response of the lattice, and in particular the dipolar COOH group[34]. This component, which is proportional to ω, shows peaks which can be correlated with known phase changes in the structures under investigation. At lower frequencies the second component manifested itself with an ω^n dependence where $n < 1$. This was attributed to the hopping of carriers between localised states situated at the monolayer- monolayer interfaces. The carriers have been shown to originate from the electrodes i.e. they are injected into the films. A typical G-ω graph is shown in Fig. 5.8. The value of n has been linked to the LB film quality by Roberts and McGinnity[34], values of n close to unity signifying good insulator properties. Thus G v ω measurements can be used to test the quality of deposited LB films. It is worth noting in this context, that results on diacetylene polymer yield G vω^n graphs where n is approximately one[31].

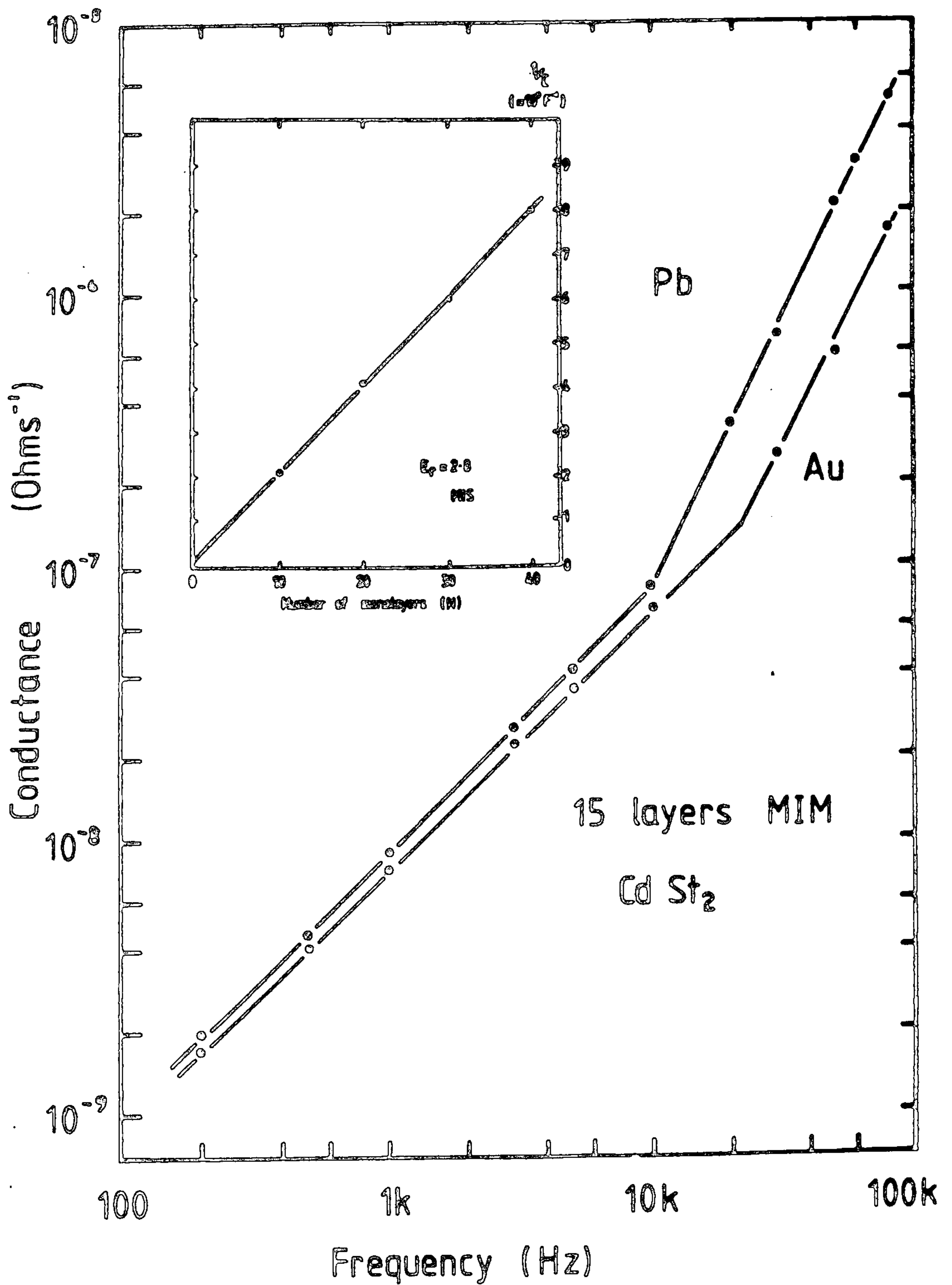


Fig. 5.8 Variation of a.c. conductance with frequency for good quality film. Inset shows a typical capacitance plot for CdStearate/stearic acid thick films.

5.6.3 A.C. Capacitance

Capacitance measurements are a very useful tool in the characterisation of LB films. Graphs of the reciprocal capacitance against the number of monolayers are commonly plotted. A consideration of the simple equations shows that this relationship should be linear if the monolayers are stacking reproducibly.

$$\frac{1}{C} = \frac{d}{\varepsilon_o \varepsilon_r} N \qquad (5.2)$$

where C is the capacitance per unit area, $\varepsilon_o \varepsilon_r$ the permittivity of the film whose molecular chain length is d. N is the number of monolayers deposited. Apart from the test for linearity the slope of a $\frac{1}{C}$ v N graph yields the dielectric thickness of the LB film i.e. $\frac{d}{\varepsilon_r}$. The effect of any underlying 'oxide' layer on the substrate has been neglected in equation 5.2. A simple correction can be made as follows

$$\frac{1}{C} = \frac{d}{\varepsilon_o \varepsilon_r} N + \frac{d_{ox}}{\varepsilon_o \varepsilon_{ox}} \qquad (5.3)$$

Thus the intercept of the appropriate graph also gives information regarding the surface layer.

The linearity of $\frac{1}{C}$ v N graphs for fatty acids and diacetylene polymer is good[24,31] in general (see inset of Fig. 5.8). It is commonly found that the point for the first layer lies above the line and this has been attributed to the unique properties of the first layer. This may be due to a reaction between the substrate and the initial monolayer[35].

Good LB films show little change in capacitance with frequency, even up to frequencies of 10^6 Hz. Any dispersion in ε_r which leads to a frequency dependent capacitance and conductance is usually linked with poor d.c. electrical characteristics.

5.7 LB Film Applications

At the present stage of development of LB film technology the potential applications are many and wide-ranging. The feasibility of some ideas has been demonstrated, but clearly a large amount of work is necessary if all the possible avenues are to be fully explored. This section outlines the main areas of application, both proven and speculative. The subject may be divided into two areas, depending on the LB film material used i.e. those applications making use of fairly 'conventional' LB film materials e.g. fatty acids, and those utilising novel molecules whose structure and properties are more complex.

The simplest applications exploit the good insulating properties of LB films. Messier et al[36] have fabricated low voltage, low loss capacitors using LB films in a metal-insulator metal (MIM) structure. These devices could have an additional use as hygrometers since their capacitance varies linearly with ambient humidity[36]. The metal-insulator-semiconductor structure is of even greater interest because of its widespread use in planar electronic devices and integrated circuits. The development of MIS devices on semiconductors other than silicon has been hindered by their lack of native oxides with good insulating properties. The suitability of LB films in this context is obvious. The Durham group principally, has shown that LB films can be deposited onto many semiconductors e.g. InP, GaP, GaAs, CdTe, CdS, InSb, CMT. This shows promise for a variety of useful electronic devices; for instance an FET structure incorporating LB films on InP has already been reported[37].

The combination of good insulating properties and an accurately controllable thickness can be put to use in devices requiring ultra-thin insulators i.e. tunnelling MIS devices. The efficiency of a Schottky barrier solar cell can be increased by the insertion of such a layer[38]. LB films lend themselves to the investigation of this phenomenon as a

function of insulator thickness (which is very difficult with other insulators) and may well be of use in practical devices, as demonstrated by Dharmadasa et al[39, 40] and Tredgold et al[41]. The electroluminescent efficiency of MS diodes is also enhanced by introducing a tunnellable insulator, through an increase in the minority carrier injection ratio[42]. LB films have been successfully used for this purpose on GaP by Batey et al[44, 45]. An obvious extension of this work involves using II-VI materials such as ZnS and ZnSe where it is impossible to form p-n junctions. Their use as LED's is thus dependent upon an MIS type structure. The large area capability of Langmuir troughs is an added advantage in both solar cell and LED applications.

LB films are currently being marketed by the Japanese as dilute, radioactive sources and standards. Conventional films such as stearates are used, and the cadmium is replaced by a known amount of a radioactive nucleide e.g. cobalt. By depositing normal Cd Stearate layers on top of these sources the physical range of low energy electrons can be studied[45].

The optical properties of LB films are also of interest and have led to investigations of their use in the field of optical waveguides[46]. The thickness of the films can be precisely controlled and the refractive index depends on the material used, allowing considerable 'fine tuning' to obtain the required values. Losses as low as 5 dB cm^{-1} have been reported[47] and even lower losses may occur using other materials. It is possible to conceive of LB films having various other optical uses, such as cladding for waveguides, fibre-film couplers, and even selective absorption (using LB films incorporating dye molecules).

Investigations are at present being carried out into the use of LB films of more complex molecules as photoresists in the fabrication of integrated circuits. The very thin layers possible with LB films would result in an increased resolution via a reduction in the scattering of

the electron beam used to expose the photoresist. The results have been encouraging, with a resolution of better than 60 nm reported by Barraud et al[48] using ω-tricosenoic acid. It would seem likely that electron beam resists will soon be in commercial use. This topic is the subject of a recent review by Peterson[49].

Aromatic compounds i.e. those including benzene ring structures can, with suitable substitutions, be made into LB monolayers. Their electrical properties can be very interesting e.g. lightly substituted anthracene derivatives exhibit an anisotropy in conductivity of the order of 10^8 [50]. Anthracene is also well known as an electroluminescent material with emission occurring in the blue. In conventionally deposited films the efficiency is poor, but LB films of anthracene may increase the light output obtainable because of their freedom from defects, as well as their lower operating voltages.

The advances in 'chemical engineering' i.e. the ability in this context, to modify molecules to make them suitable LB film materials has led to other suggested applications. These include high temperature semiconducting films and, possibly, piezo- and pyro-electric films, produced by depositing different successive monolayers to build in a dipole moment. The incorporation of dye molecules into LB film structures may lead to improved solar cell efficiencies by using a greater proportion of the solar spectrum, exploiting a technique known as dye sensitisation[51, 52]. It is also interesting that some merocyanine dyes exhibit non-linear optical effects and have been shown to have extremely high figures of merit[53]. Modification of such dyes to produce them in LB film form might well be fruitful. Magnetic LB films are also a possibility and some work has been carried out by IBM. Ferromagnetic ions in monolayer and multilayer structures have been used to study truly 2-dimensional magnets[54] and may find application in thin bubble memory chips.

LB films may also find uses in some routine chemical processes. They have distinct advantages over conventional catalytic materials, since very small amounts of material are spread over comparatively large areas, (typically 1 μgm per monolayer) giving a very large number of active sites. The adhesion of certain polymers to Al_2O_3 can be improved by interposing an LB film, and this is currently being investigated. Films of ω-tricosenoic acid show promise as encapsulants which only use small amounts of material and are deposited in a low temperature process with a large area capability[55].

Finally there is the most speculative but perhaps the most exciting area; that of biological sensors. Monomolecular films bear a close resemblance to naturally occurring cell membranes, and they have been used by biochemists in simulations of biological processes. One can foresee the possibility of constructing complex film structures which would be sensitive to a particular ionic or biological species e.g. enzymes, antibodies etc. The incorporation of such films into an I.G.F.E.T. (as the insulator) could lead to a large variety of microelectronic sensing devices. The idea of making synthetic structures to copy natures photosynthesis process has also been suggested : if possible, it could revolutionise our energy systems.

CHAPTER 6

EXPERIMENTAL TECHNIQUES AND DEVICE FABRICATION

6.1 Introduction

The characterisation of any semiconductor device involves making many different measurements. This chapter contains the descriptions of the various instruments and experimental arrangements which have been used to analyse the α-Si:H and associated devices. Sample chamber construction is covered in the first section, and this is followed by an outline of the electrical measurement techniques such as d.c. conductivity and admittance characteristics. A short section is also included on the measurements made on field-effect transistor structures. The chapter continues with two sections devoted to the surface analytical techniques of Auger Electron Spectroscopy (AES) and reflection high energy electron diffraction (RHEED), which were used to gain information at various stages of device fabrication. The rest of the chapter is concerned with the fabrication of devices on α-Si:H, and in particular with the practical difficulties associated with the incorporation of LB films. Sample configurations and experimental details are outlined. A series of experiments is also described (and the corresponding results presented) which have led to the successful construction of α-Si:H/LB film devices.

6.2 Sample Chambers

It is vitally important that devices should be electrically screened during measurements. The further requirements of a controlled environment e.g. atmosphere, temperature etc. and the physical ease with which measurements can be made, mean that experimental arrangements must be carefully thought out. Two types of sample chamber were used in the various experiments performed : a custom built sample chamber and a commercial exchange gas cryostat. These two systems will now be described.

6.2.1 Custom-built Sample Chamber

Several different sample chambers constructed within the Departmental workshops were used, The basic design of all of these was similar, and a typical schematic diagram is given in Fig. 6.1. The outer chamber was made of brass or aluminium, providing electrical shielding for the working space inside. Joints were gas tight, enabling the chamber to be evacuated using a rotary pump. Measurements could be taken under vacuum or in an inert gas atmosphere of dry nitrogen. Containers of silica gel (desiccant) were mounted in the base of the chamber in an attempt to keep the effects of moisture to a minimum. These containers were removable to allow the silica gel to be regenerated by heating. Samples were mounted onto a table whose temperature was controlled by means of a Peltier heater(1) (Cambion 801-3958-01 ceramic thermionic module). This was fixed to a heat sinking base consisting of a copper block with cooling water circulating through it. Temperatures in the range of -20 to +40°C were possible using this arrangement. The back contact was generally made using air-drying silver paste to the sample substrate. Top contacts were made with the aid of a small (0.25 mm or 0.5 mm diameter) gold ball attached to a micromanipulator system. This enabled a large number of top contacts to be tested quickly and easily. Illumination of the sample could be effected by the small lamp installed near the sample mounting table : the lamp was powered by an external supply. Alternatively the cover of the chamber incorporated a large glass port with a metal cover, enabling external illumination sources to be used. All signal connections left the chamber via a screened connection box. Co-axial cables were used to connect this box to the various instruments. These precautions were found to be essential to reduce noise to a minimum.

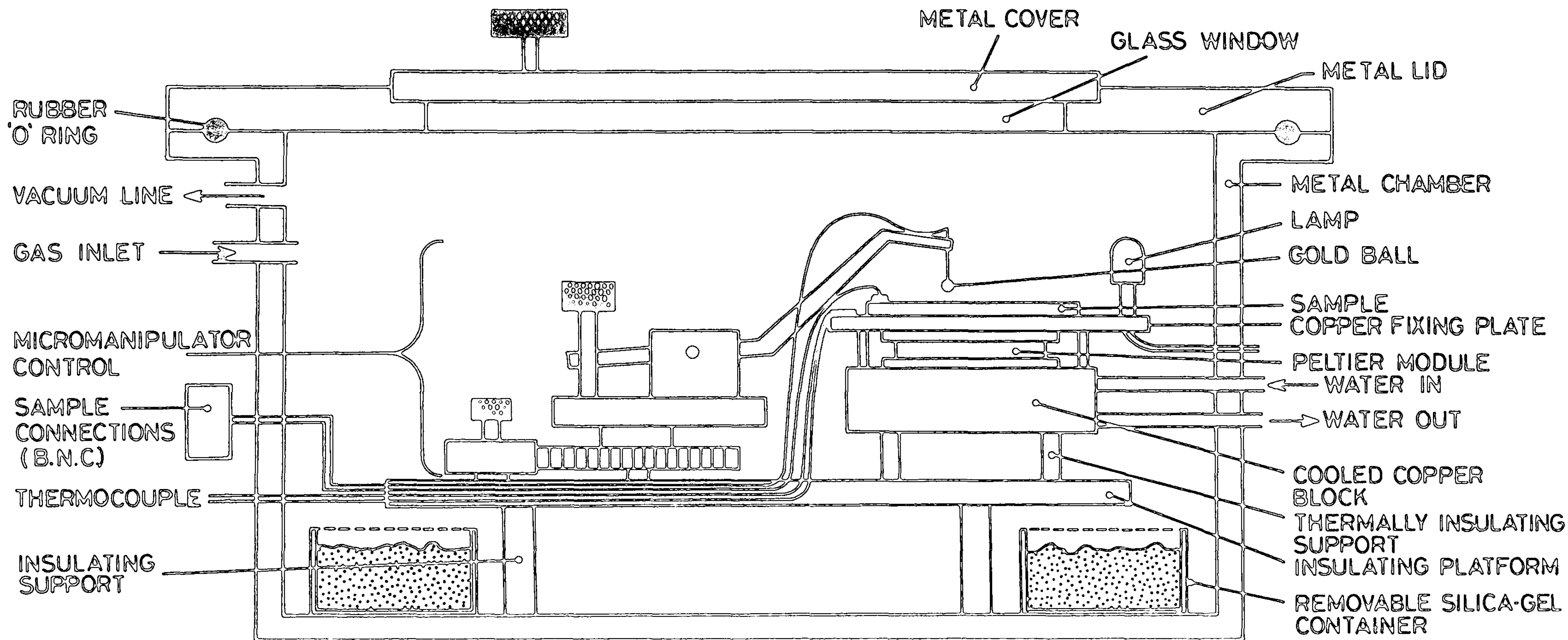


Fig. 6.1 Schematic diagram of a sample chamber custom-built in the Departmental workshops.

6.2.2. Exchange Gas Cryostat

The other electrical measurement system used was based on the Oxford Instruments DN704 liquid nitrogen exchange gas cryostat. A schematic diagram of the unit is shown in Fig. 6.2. It is designed around a 20 mm clear internal diameter sample tube to which a heat exchanger is attached. The copper heat exchanger is cooled with liquid nitrogen fed via a supply tube from the liquid nitrogen vessel. The N_2 gas exhausts from the heat exchange block and exits through the top plate as shown in the diagram.

This cryostat could accommodate large samples, up to 6 cm x 2.5 cm in size, and the main vacuum did not have to be broken to change samples. The vessel was of welded stainless steel construction, incorporating an activated charcoal sorb which cryopumped when cool. This ensured a good vacuum in the outer chamber without the need for continuous pumping. Sample changing was a simple operation, as it only necessitated the removal and repositioning of the sample holder. The inner chamber i.e. the sample space, could be evacuated and refilled with a suitable exchange gas (He) to avoid condensation of water vapour on cooling.

The cryostat was fitted with a platinum resistance thermometer and a 39-ohm heater wired to the 10-pin electrical connector at the top plate. Temperatures in the range of 77k to 300k could be achieved by balancing the heat input to the heat exchange block against the cooling power available. This was realised using an Oxford Instruments digital temperature controller (DCT2). This instrument maintained the temperature at a desired value : its measuring accuracy was $\pm$ 0.1K.

The advantage of this system lay in its very wide range of operating temperatures. However, this was offset by the increased difficulty experienced in making electrical contact to the devices. Invariably air-drying silver paste (solvent based) or graphite paste (water based) had to be used for both top and bottom contacts. This was found to be time

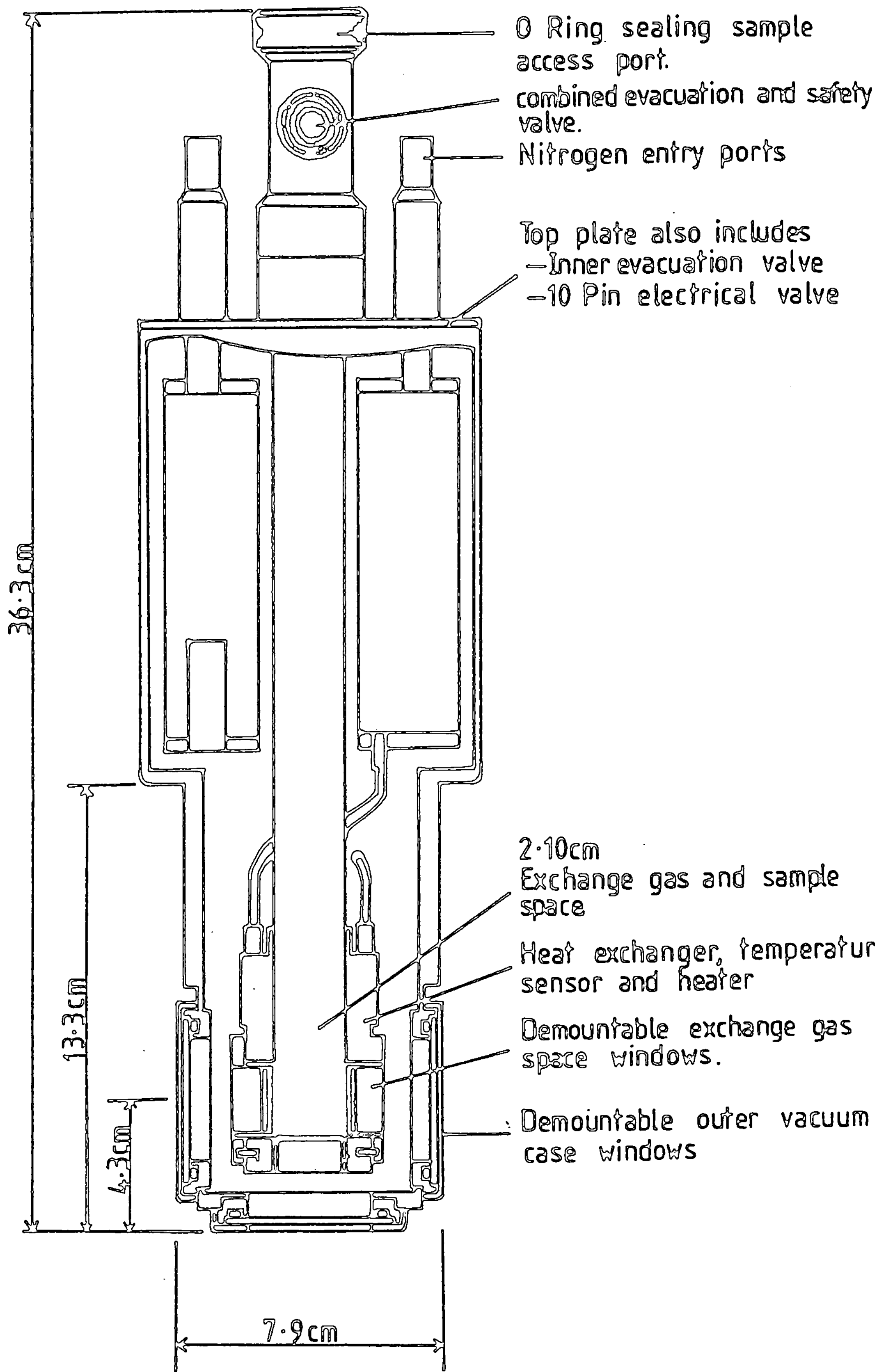


Fig. 6.2 Schematic diagram of Oxford Instruments DN704 liquid nitrogen cryostat.

consuming and to sometimes result in degradation of devices, presumably due to solvents or water used in the pastes. As a consequence this cryostat was only used when the temperature variation in the chamber described previously was insufficient.

6.3 D.C. Conductivity Measurements

The experimental arrangement used for measuring d.c. conductivity data is shown as a block diagram in Fig. 6.3. The equipment used was not complex, but scrupulous attention to noise reduction was necessary, especially at low current levels (10^{-12} - 10^{-13} A). Samples were housed in shielded chambers as described. The power supplies used were a Keithley 241 Regulated High Voltage Power Supply (0 - 900 volts in 0.01 V steps), and a Time Electronics Type 2003 S d.c. voltage calibrator. Both units had switchable polarity. The latter unit ranged from 0-10 volts in steps of 0.01 μV and was battery operated to reduce mains noise. The current was measured with a picoammeter (Keithley Model 410 A or 414 A) which was connected to a chart recorder (JJ instruments model CR 500). The recorder was used to monitor the current transient after switching the voltage, to ensure that the equilibrium current was measured. Coaxial cables were used for all connections.

6.4. Admittance Measurements

Admittance measurements were performed using phase sensitive techniques. A block diagram showing the major components of the system used is given in Fig. 6.4. The most important instruments and circuitry will now be discussed in detail.

6.4.1 Phase Sensitive Detection System

The use of phase sensitive detection as a means of recovering signals buried in noise is now quite commonplace. Small signal admittance measurements were made using an Ortholoc 9502 lock-in amplifier. This instrument measures the phase and magnitude of an a.c. signal produced by the

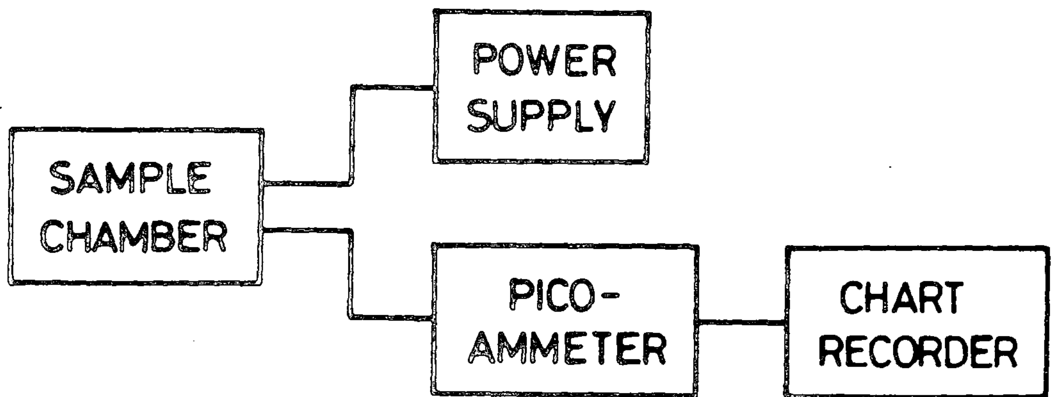


Fig. 6.3 Experimental arrangement for d.c. conductivity measurements.

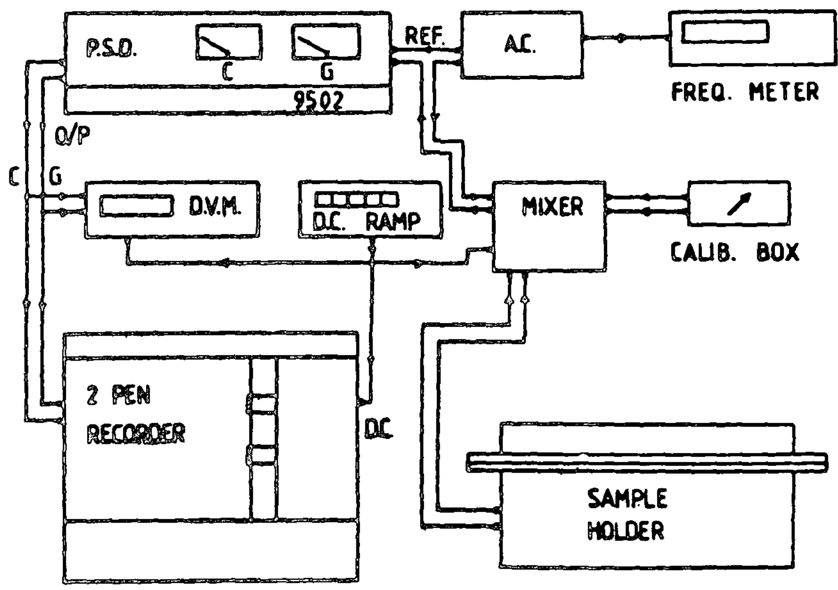


Fig. 6.4 Block diagram of admittance measurement system.

excitation of the device from an a.c. source, and resolves the signal into the in-phase and out-of-phase components with respect to the a.c. excitation.

The 9502 lock in amplifier consists of a low noise amplifier, a reference unit and two phase sensitive detectors (p.s.d) A block diagram of the 9502 is shown in Fig. 6.5. A p.s.d. may be thought of as a multiplier circuit, whose output v_O is the product of the two input signals v_I, from the device, and v_R, the reference voltage. Let us represent these signals in the form

$$v = V \cos (\omega t) \tag{6.1}$$

The input signal v_I consists of the synchronous waveform which is to be detected, and noise (at random frequencies). If we consider only the sample frequency ω_S then we can write

$$v_O = v_R v_S = V_R V_S \cos (\omega_R t) \cos (\omega_S t) \tag{6.2}$$

If V_R is scaled to unity

$$v_O = V_S \cos (\omega_R t) \cos (\omega_S t) \tag{6.3}$$

which, remembering that $\omega = 2\pi f$, can be written

$$v_O = \tfrac{1}{2} V_S \left[\cos 2\pi t (f_R - f_S) + \cos 2\pi t (f_R + f_S) \right] \tag{6.4}$$

In practice, of course the noise frequency $f_N = f_S$ can assume any value. If a low pass filter having a cut-off frequency $f_C << f_R$, is applied to this signal, only frequencies having $(f_R - f_N) < f_C$ will be passed i.e. frequencies very near to f_R. When $f = f_R$ i.e. the condition required where the detected signal is in sychronism with the a.c. excitation, the output

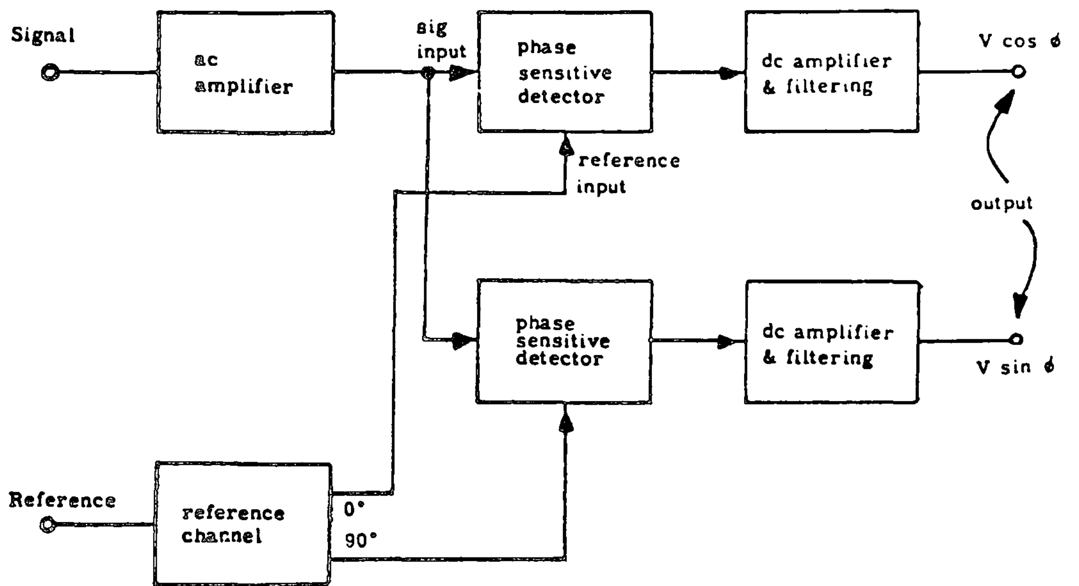


Fig. 6.5 Block diagram of Ortholoc 9502 p.s.d.

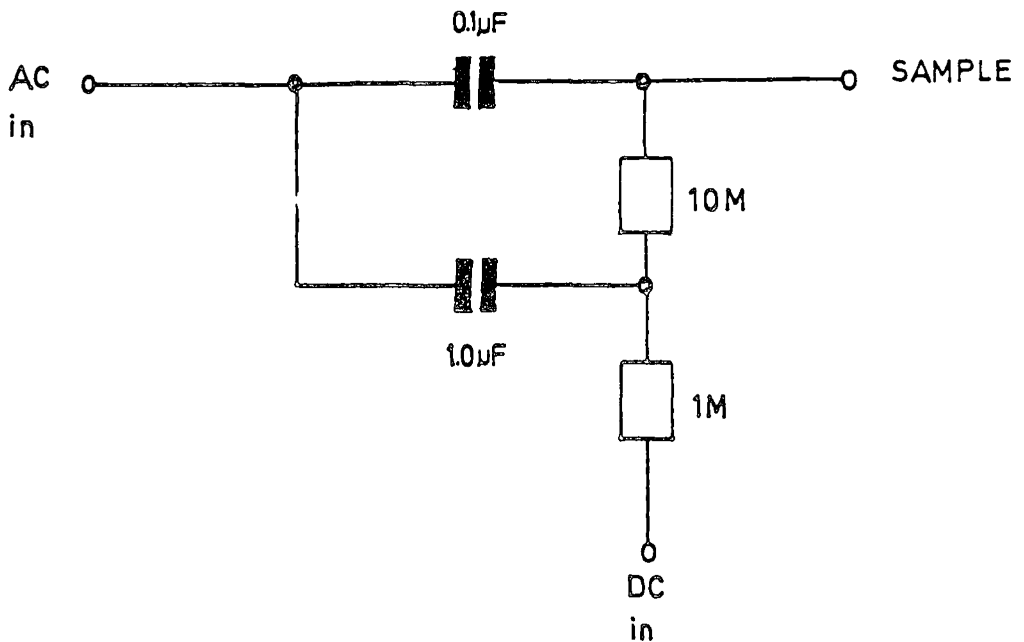


Fig. 6.6 Mixing circuit for a.c. and d.c. signals

v_O is simply a d.c. voltage whose magnitude is proportional to the signal amplitude and phase difference (between the signal and the a.c. excitation). If

$$v_I = V_I \cos(\omega_R t + \phi) \tag{6.5}$$

then

$$v_O = V_I \cos(\omega_R t + \phi) \cos(\omega_R t) \tag{6.6}$$

$$= \tfrac{1}{2} V_I \left[\cos(2\omega_R t + \phi) + \cos\phi \right] \tag{6.7}$$

After filtering out the 2ω component

$$v_O = \tfrac{1}{2} V_I \cos\phi \tag{6.8}$$

The p.s.d has a calibration facility for changing the phase to elimate ϕ (i.e. $\phi \rightarrow 0$). This is done simply by adjusting the phase for the maximum signal. Quadrature components can be measured using another p.s.d. with a 90° phase shift in ϕ.

The reference unit in the 9502 system takes a periodic input of any shape and converts it to a square wave of the same period. The output of this unit is suitable for the p.s.d. reference. Such a unit adds to the versatility of the set-up because it allows any form of excitation to be applied to the sample. The unit also has a frequency doubling capability.

The 9502 lock-in amplifier allows a very large improvement in signal/noise ratio over more conventional methods. The exact value obtainable is rather dependent on the final filtering that is applied to the signal, but the improvement can be by a factor of 200 or more.

6.4.2 Input Circuitry and Signal Sources

The experiments performed require the a.c. excitation of the device together with a simultaneous d.c. ramping, to move the Fermi level through

the semiconductor bandgap. The a.c. signal was derived either from the internal oscillator in the 9502 lock-in amplifier or from a Farnell Function Generator FG3 with a range of 0.02 Hz to 200 kHz. The signal level was always less than 25 mV r.m.s. The latter oscillator was connected to the Ortholoc via an attenuator, to allow a fine control of the signal amplitude. The D.C. ramp was provided by a custom built ramp-generator (designed and built in the Departmental workshops). This unit had variable ramp speeds from 5 to 500 mV sec^{-1} and a linearity of better than 1%.

The a.c. and d.c. signals must be mixed and applied to the sample. However, great care must be exercised in the design of the mixing circuit to avoid introducing stray capacitance and phase shifts, which lead to errors. The circuit used follows that of Boudry[2] and is shown in Fig.6.6. A simple R-C network could be used, but a very large time constant would be required to keep the phase errors to an acceptable value. The two stage network shown has much better properties : a time constant of only 1 second is quite adequate.

For measurement purposes the sample admittance may be thought of as a parallel combination of the measured conductance G_M and capacitance C_M

$$Y_M = G_M + j\,\omega C_M \qquad (6.9)$$

The driving signal v_I gives rise to a current i_M, and

$$i_M = v_I \; Y_M \qquad (6.10)$$

From equation 6.9

$$G_M = \frac{Re\ (i_M)}{v_I} \qquad (6.11)$$

and

$$C_M = \frac{Im\,(i_M)}{V_I} \qquad (6.12)$$

These are the in-phase and out-of-phase components of the signal.

A sense admittance (i.e a resistor or a capacitor) is commonly used to measure i_M. Using an active detector is a better approach because of the lower input impedance and the fact that the current measurement is direct. A virtual earth amplifier is suitable for this task : its extremely low input impedance (high input admittance) means that the cable admittance has only a negligible effect. The circuit used is shown in Fig. 6.7, again following that of Boudry who gives a detailed description of the circuit in his paper[2]. The network is formed from an operational amplifier with shunt feedback (see Fig. 6.8) whose output voltage V_f is given by

$$V_f = -Z_F\, i_M \qquad (6.13)$$

where Z_F is the feedback impedance. The choice of a capacitor is made as this impedance eliminates any frequency dependence from the conversion factors i.e. if $Z_F = {}^{1}/_{j\omega C_F}$ then from equations 6.11 and 6.12

$$G_M = \frac{C_F}{v_i\ Im(V_f)} \qquad (6.14)$$

and

$$C_M = \frac{-C_F}{v_i\ Re\,(V_f)} \qquad (6.15)$$

The circuit includes an active feedback loop as well as the capacitive one. This acts as a leakage path for any d.c. displacement currents which could upset the amplifier output.

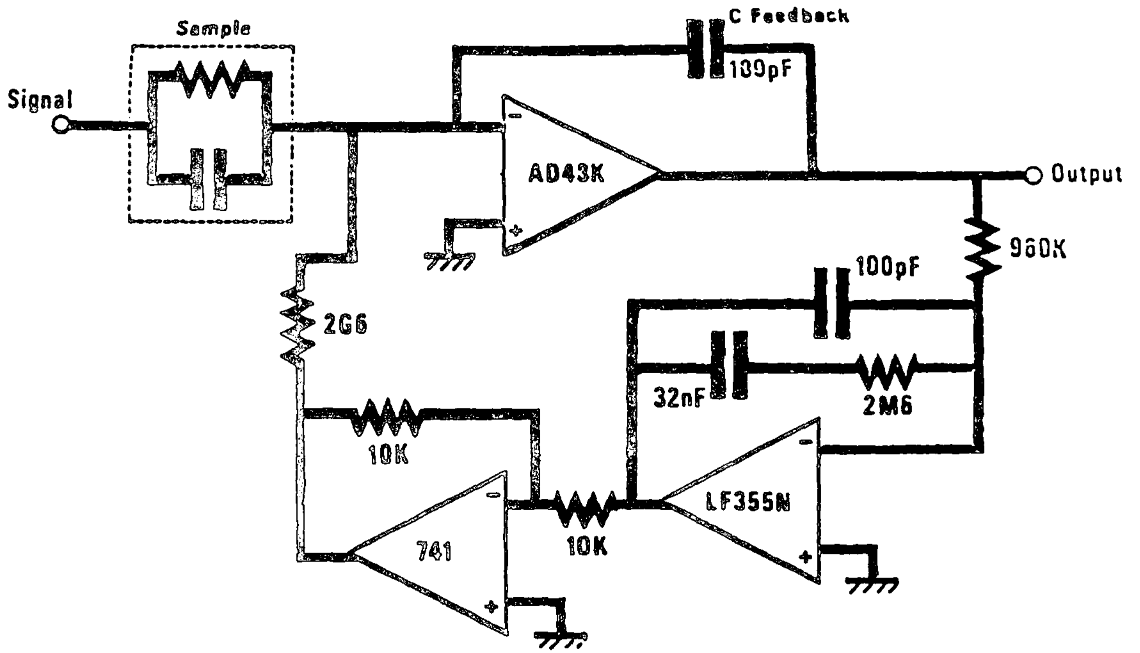


Fig. 6.7 Circuit diagram of virtual earth amplifier

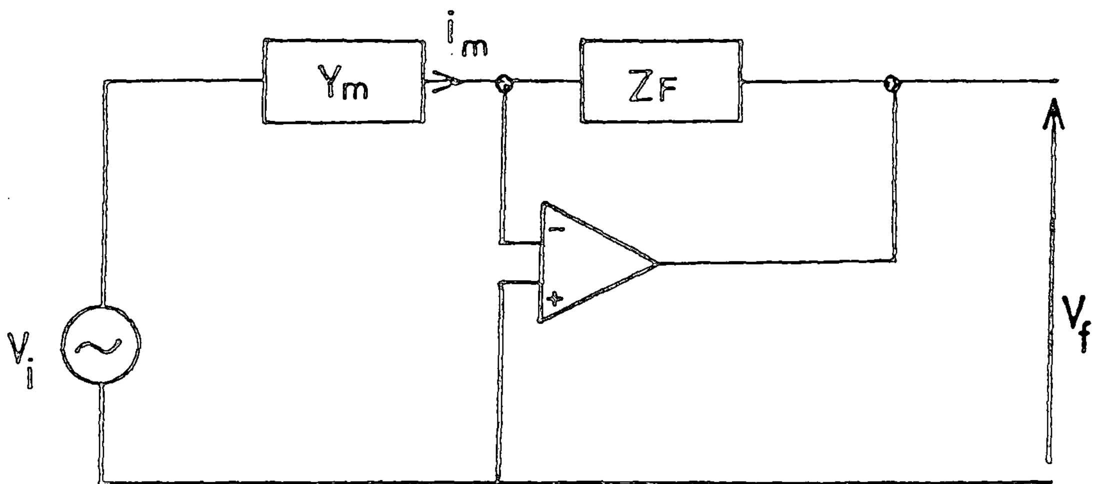


Fig. 6.8 Virtual earth amplifier measurement configuration

6.4.3 Calibration Procedures

Stray admittance introduces frequency dependent errors: this loss may be represented by an effective change in the phase of the reference signal whose magnitude changes with frequency. In practice, some stray admittance is unavoidable, and thus it is necessary to calibrate the Ortholoc at every frequency. The calibration procedure was carried out using polystyrene, low-leakage capacitors : the exact values of capacitors and resistors used in this process were measured individually using a Boonton 72BD capacitance meter and a Wayne Kerr B522 Component Bridge. The procedure was as follows:

(1) With the sample disconnected the zero offset controls on the lock-in were used to adjust the meter readings to zero. This allows compensation for any strays.

(2) A capacitor of roughly the same capacitance as the sample was inserted. Assuming it to be ideal, the phase control was used to zero the conductance channel.

(3) The calibration capacitor was disconnected and the zeros re-checked. If necessary the process was repeated. The voltage corresponding to the calibration capacitor was then recorded to enable the direct conversion from output volts to capacitance.

(4) A resistance was then connected to allow calibration of the conductance channel.

6.4.4 Other Instrumentation

Direct reading of the p.s.d. output voltages from the meters on the Ortholoc was not very accurate, To overcome this the voltages were measured using a Farnell DM 131 auto-ranging multimeter. This could be switched to read either channel, or the value of d.c. bias. Capacitance-voltage and conductance-voltage data were recorded directly onto a Bryans 26000 A3 dual pen X-Y recorder for subsequent analysis.

6.5 Field Effect Transistor Measurements

The experimental arrangement for measuring the electrical characteristics of FET's is shown schematically in Fig. 6.9. The device was mounted in a specially constructed metal box which was both light-tight and electrically shielded. Containers of silica gel were placed in the bottom of the box to ensure dry conditions. The other instruments used were as described in section 6.2.

6.6 Auger Electron Spectroscopy

Auger Electron Spectroscopy (AES) is a versatile and sensitive technique for the analysis of the surface composition of materials. In an MIS device the nature of the surface region is vitally important and a better understanding of it can lead to improvements in device performance. AES provides a convenient method for the analysis of the surface of real, practical devices and as such has become a standard laboratory analytical technique. The basic principles of the method will now be outlined. For a more comprehensive coverage of AES the reader is referred to the book 'Surface Physics' by M. Prutton[3].

In AES the excitation of the sample is provided by means of an electron beam of energy 1-5 keV or a low energy X-Ray beam. The depth sampled by such a beam is typically 10 Å or so i.e. of the order of a few atomic layers. When the beam strikes the sample surface it dislodges electrons from the core levels of the surface atoms. Electrons can be restored to the core level by one of several processes e.g. X-ray emission, complex processes (where some energy is used to emit an electron, some is lost as phonons and some as radiation) or an Auger process. The Auger process may be understood with reference to the energy level diagram given in Fig. 6,10. After the initial electron ejection an electron from one of the outer shells drops down to the vacant core level. All of the energy released by this fall

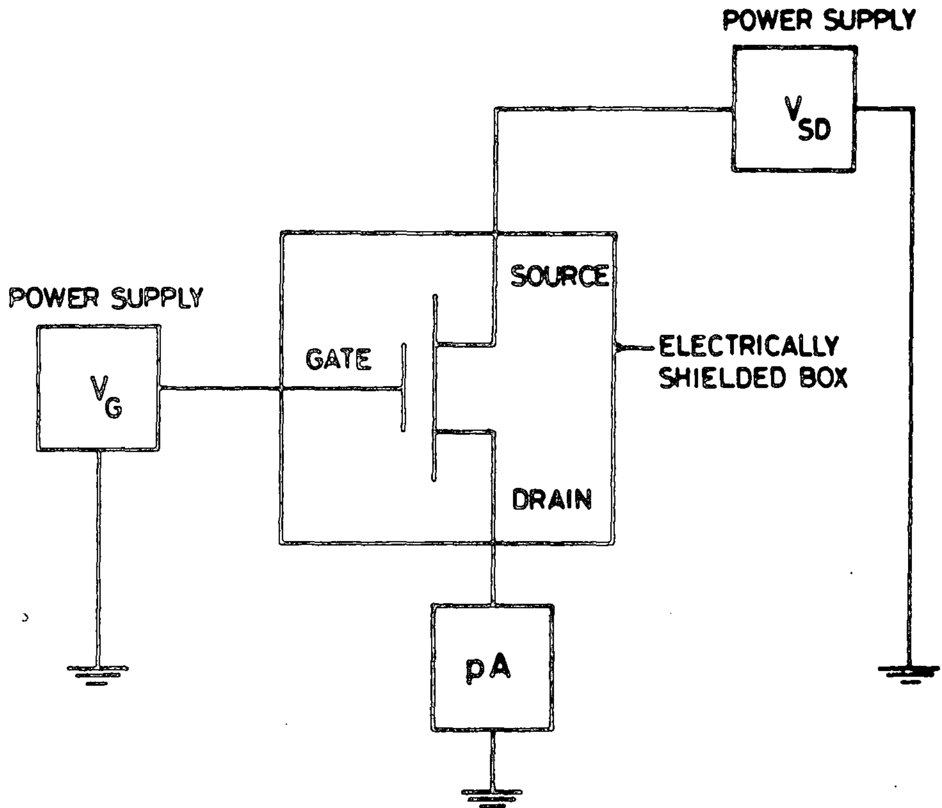


Fig. 6.9 Schematic diagram of FET measurement set-up

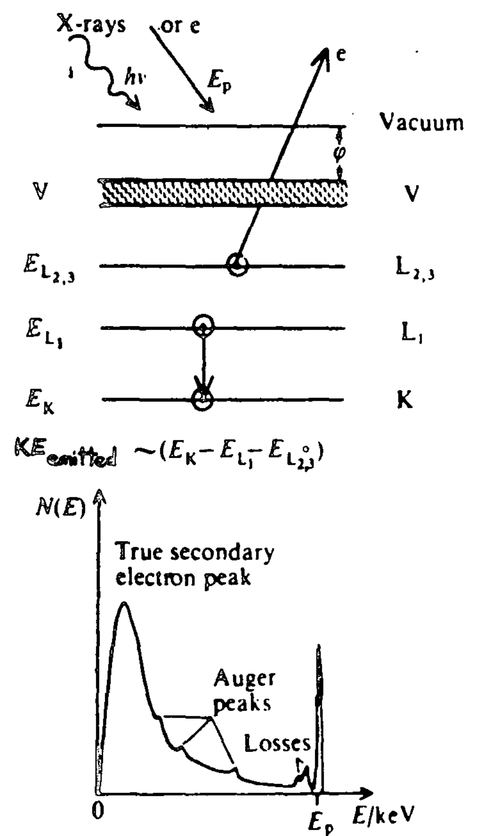


Fig.6.10.Energy band diagram illustrating the processes involved in Auger spectroscopy. The levels E_k etc. correspond to the binding energies of electrons measured from the vacuum level. The graph below indicates the number N(E) of electrons with kinetic energies between E and E + dE which will be measured in the electron energy distribution leaving the solid. The horizontal scale corresponds approximately to those commonly found in practical cases. (after ref. (3)).

is then given to another outer shell electron. This electron is emitted from the atom with a characteristic energy which is independent of the energy of the exciting beam. If the initial electron is ejected from the K-shell and its place is filled by one from the L_1 shell, the electron ejected from the $L_{2,3}$ shell has an approximate energy

$$E\ (\text{Auger}) = E_K - E_{L1} - E_{L2,3} \qquad (6.16)$$

and is referred to as a $KL_1\ L_{2,3}$ Auger electron.

Such emissions are highly probable for low incident beam energies and atomic numbers that are not too high. This high probability means that even small amounts of material on a surface can give rise to Auger emission. An energy analysis of the emitted electrons yields identification of the elements present and their ionic charge state, as the energy of each electron is characteristic of a particular transition in its parent atom. There are several spectrometer arrangements used for this energy analysis involving both electrostatic and magnetic effects : each method has its own particular advantages. In practice, in addition to Auger processes there is a large amount of secondary emission. Fortunately this can easily be removed by differentiation (see Fig. 6.10), for example making use of lock-in amplifier techniques. The fact that Auger peaks are very sharp in energy makes them easily identifiable. In systems where an ion gun facility is available AES provides a very convenient means of depth profiling. The sample may be stripped by accelerated inert gas ions at the same time as AES probing is carried out : the variation in sample constitution with time gives the depth profile.

Some preliminary investigations of the surface of α-Si:H after various etches were undertaken at Plessey (Caswell) Ltd. The system used was a standard four-grid hemispherical retarding field analyser with a

glancing incidence electron gun (Vacuum Generators model LEG 3) providing up to 10 μA at 2.4keV. An ion-beam etching facility using 5keV Xenon ions was also available.

6.7 Reflection High Energy Electron Diffraction

Reflection High Energy Electron Diffraction (RHEED) is another technique which can be employed in the study of surfaces. Although it is not widely used it is a fairly straightforward method of surface analysis which has certain advantages over more conventional techniques. Firstly, it is fairly easily implemented on most existing transmission electron microscope systems. It is capable of dealing with large area samples and does not require any specialised sample preparation. RHEED can be used non-destructively to provide information on the presence of surface films, the crystal orientation and perfection of the surface region, the degree of preferred orientation of crystallites at the surface,and various other crystalline properties. Furthermore, the results obtained are relatively simple to interpret.

A comprehensive review of the topic of RHEED has recently been published by Russell[4]. Only the salient features of the technique will be outlined here. A monoenergetic electron beam (energy 10-100 keV) is directed at the surface of the specimen. For this energy range the electrons have wavelengths between 0.12 and 0.04 Å, given by

$$\lambda = \sqrt{\frac{150}{V\,(1 + 10^{-6}\,V)}}\ \text{Å} \qquad (6.17)$$

where λ is the wavelength and V is the accelerating voltage in volts. Using the Bragg equation

$$\lambda = 2\, d_{hkl}\, \sin\, \theta \qquad (6.18)$$

where d_{hkl} is the interplanar spacing, this corresponds to a Bragg angle θ between 0.5° and 1.5°, i.e. only those planes oriented at a few degrees to the surface will diffract a beam that strikes it at glancing incidence. The resulting diffracted pattern, which comes from the top few layers of atoms, may be observed on a fluorescent screen, or recorded on photographic film.

Analysis of the pattern can yield a large amount of information. The type of pattern e.g. spots or rings gives the amount of crystalline order (single crystal, polycrystalline or amorphous). The crystal structure and interplanar spacing can be deduced from the geometry of the pattern. Identification of the contents of the unit cell i.e. which particular elements are present, is also possible, although experimental limitations and the lack of any sound theoretical back up make it difficult.

In general, RHEED is very quick and easy to perform. Coupled with its other virtues it provides an ideal method of device surface analysis, complementing the AES technique discussed earlier. Measurements were performed on a modified transmission electron microscope (Japanese Electronics Optics Lab. Co. Ltd. JEM 7A/120 TEM) using an accelerating voltage of 100 kV.

6.8 Device Fabrication

The electronic devices whose properties are described in this thesis were fabricated in a series of steps. These may be identified as follows:

(a) Preparation of semiconductor substrate.

(b) Substrate treatment.

(c) Deposition of LB film layer (if applicable).

(d) Top contact evaporation.

The remaining part of this chapter will deal largely with steps (a), (b)

and (d). The LB film deposition conditions (c) were discussed in section 5.5. Some data concerning the quality of the deposited LB films will be reported here. The handling and storage of devices will also be outlined.

6.8.1 Substrate Preparation

The majority of α-Si:H substrates used in these studies were prepared at the University of Dundee by the glow discharge technique[7]. The semi-conductor was usually deposited onto stainless steel held at approximately $300^{o}C$, although conducting glass was sometimes used as a base for certain samples. A highly doped (n^{+}) layer 10-20 nm thick ensured good ohmic contact between the steel (or ITO layer) and the bulk α-Si:H film, which was undoped. The overall film thickness was approximately 1 μm. For comparison, films of α-Si:H from different sources were also used. These were produced by Plessey Research (Caswell) Ltd. and by Xerox Corporation (Palo Alto Research Centre) using the same method and under similar conditions to those described above.

Semiconductor substrates for FET measurements were also supplied by the University of Dundee. These consisted simply of a layer of undoped α-Si:H on glass (Corning 7059). On each sample a number of chromium source-drain contacts were evaporated. The channel length was about 70 μm and the width about 2 mm.

6.8.2 Substrate Treatment

Schottky barrier diodes were constructed following a very simple routine. The α-Si:H substrate was first etched for approximately 2½ minutes in buffered HF (40% HF: 40% NH_4F in 1:5 volume ratio) to remove any oxide layer. After thorough rinsing in ultra-pure water ('Milli-Q' reagent grade) the sample was mounted in the vacuum chamber and pumped down as quickly as possible so as to minimise any fresh oxide growth. Top contacts of the appropriate metal were then deposited (see section 6.8.4).

For LB film devices the surface treatment was more elaborate. The first requirement for LB film deposition is that the substrate should be clean i.e. free from dirt, grease and other contaminants. This may be achieved very simply by refluxing in iso-propyl alcohol (I.P.A.) vapour for several hours (usually overnight). For some substrates e.g. glass or aluminium on glass, this treatment is sufficient, but in other cases further treatment is required before dipping is successful. This is certainly true for single crystal silicon where a buffered HF etch is needed to remove the oxide layer prior to dipping. Considerable difficulty was experienced with α-Si:H and it was found that only rarely could LB films be deposited after simple degreasing. Thus, a series of experiments was carried out to determine a suitable pre-deposition substrate preparation which would enable consistent, successful dipping.

(a) Contact Angle Measurements

The angle of contact between the water subphase and the substrate during dipping must play a major role in determining whether or not a monolayer will be deposited. No studies of this area of LB films have been published in the literature. As a result the exact relationship between the angle of contact and the dipping probability is not clear. However, since the hydrophilic end of the molecule is transferred first (i.e. Y-type) this would tend to suggest that a strongly hydrophilic substrate would aid deposition. To test this, measurements of the angle of contact between a water droplet and semiconductor substrates of α-Si:H and single crystal silicon were made. This was done by treating a substrate with different etches and then dropping a small amount of millipore water onto it using a hypodermic syringe. The angles were measured from photographs taken through a travelling microscope. Single crystal silicon was used as a comparison, as more is known about its dipping characteristics than its amorphous counterpart. The results for the various surface treatments

used are given in Table 6.1. Wherever possible several droplets were photographed and the mean angle of contact taken. Some of the actual data are reproduced in Fig. 6.11. It can be seen that the water drop was reflected in the highly polished substrates, leading to a mirror image effect. This was compensated for by drawing a line joining the two end points and using this as the base line in measurements.

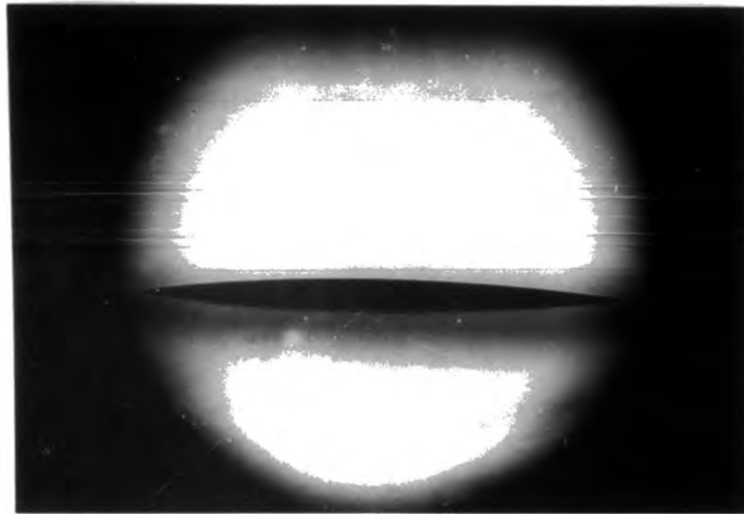
From these results it is interesting firstly to note the difference between the single crystal and the amorphous state. The contact angles for similar etches are quite different for the two materials, with those on α-Si:H being consistently lower. The naturally occurring oxide on single crystal Si is well characterised, but comparatively little is known about the surface of α-Si:H. It would seem that the two surfaces are distinctly different, and this may well be due to the presence of hydrogen inhibiting oxide formation. Goldstein and Szostak have estimated the initial sticking coefficient of oxygen on α-Si:H from Auger measurements and found it to be about an order of magnitude less than that for single crystal silicon(5). Ellipsometry measurements by Ponpon and Bourdon(6) have shown that single crystal Si and α-Si:H do have very different room temperature oxidation rates. The parabolic increase in oxide thickness with time (for $t < 10^7$ secs) suggests that the growth is limited by diffusion processes.

The most surprising feature of the results given in Table 6.1 is the strong correlation between successful dipping and high contact angle i.e. a hydrophobic surface. This is the opposite to the expected behaviour. The semiconductor CdTe also exhibits good monolayer pick-up when a high contact angle is observed. From this one must conclude that there are several factors to take into account when considering the relationship between contact angle and dipping, e.g. whether any form of bonding takes place between the substrate and monolayer, the ease of removal of water trapped

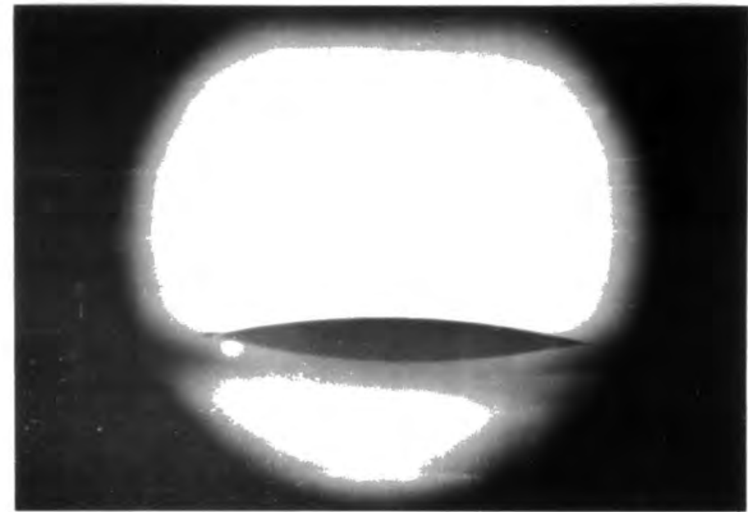
Etch Treatment	Single Crystal Silicon		α-Si:H	
	Mean Contact Angle	Dipping Success	Mean Contact Angle	Dipping Success
Untreated	43°	Sometimes	26°	Sometimes (rare)
IPA Reflux	24°	None	8°	None
IPA reflux + 2½ mins. buffered HF etch	53°	Good	17°	None
IPA reflux + ∿20 secs in HNO_3:HF: glacial acetic acid	29°	-	17°	None
10 mins ultrasonic cleaning in Decon 90*	43°	-	2°	None
IPA reflux + 2½ mins buffered HF + 15 mins in fresh chlorine water	-	-	28°	Good

* Decon Labs. Ltd., Conway St., Hove, Sussex

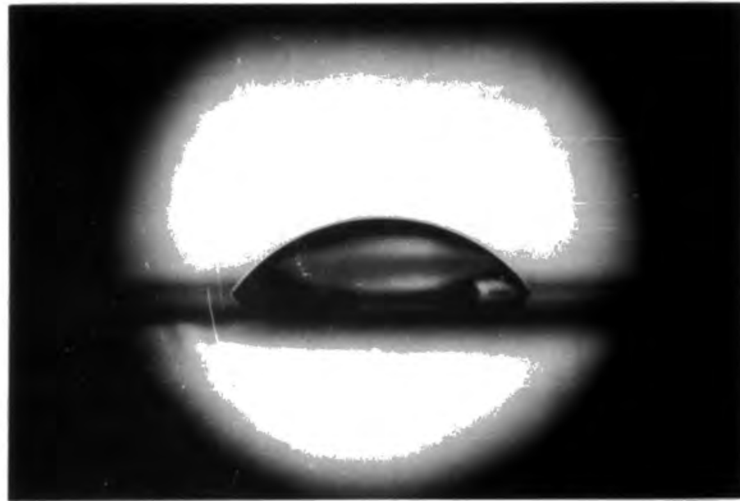
Table 6.1 Contact angle results on single crystal and hydrogenated amorphous silicon



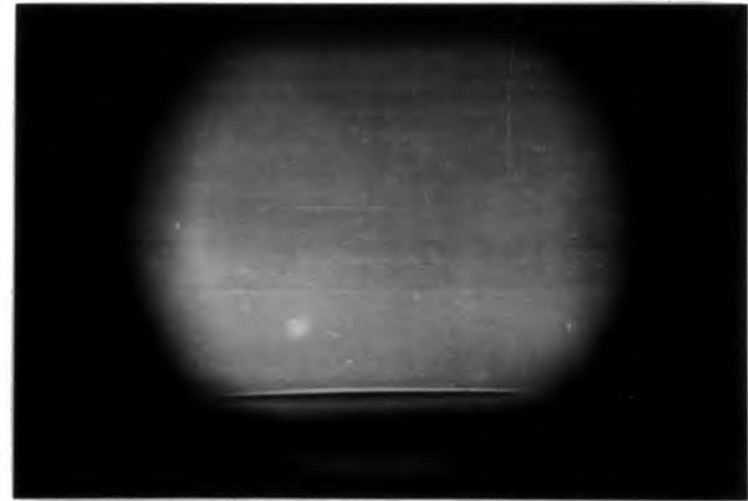
(a) α-Si:H after refluxing in I.P.A.



(b) α-Si:H after I.P.A reflux + buffered HF.



(c) Single crystal Si after I.P.A. reflux + buffered HF



(d) α-Si:H after ultrasonic cleaning in Decon 90.

Fig. 6.11 Contact angle photographs

between the film and substrate etc. The experiments performed tell us little of the individual processes occurring at the trough surface, which it would be interesting to investigate. However, they do imply that there is some definite link between contact angle and dipping probability and it is felt that such measurements, after further research, may provide a quick, empirical method of testing a pre-deposition etch to see whether it will enhance deposition.

(b) Scanning Auger Analysis

Having discovered a pre-deposition etch treatment which produced fairly consistent results, the investigation was carried a step further in an attempt to discover the exact function of each stage in the treatment. This was achieved using scanning Auger analysis to monitor the surface species on the semiconductor. The technique has already been described (see section 6.6) and only the results will be summarized here. The samples used were all cut from the same specimen so as to avoid effects due to differences in the substrates. The surface of the sample was analysed after each of the etching stages, namely

(a) Refluxing in I.P.A. vapour.

(b) 2½ mins etch in buffered HF, followed by thorough rinsing in millipore water.

(c) 15 mins etch in freshly prepared chlorine water, again followed by rinsing.

After the appropriate etching, samples were transferred as quickly as possible to the vacuum chamber to minimise any atmospheric contamination. The Auger spectrum of the surface was recorded and then the surface was cleaned with an ion gun to establish the depth at which the various constituents were present i.e. whether they were truly surface features. No quantitative analysis was performed.

It is worth noting that, as expected, after cleaning with Xe^+ ions for a sufficient length of time, all samples gave the same spectrum. This consisted of peaks due to elemental silicon and very small amounts of carbon and oxygen (the presence of hydrogen cannot be detected since it only has one electron, making Auger processes impossible). It is assumed that the C and O are contaminants in the bulk film, introduced during deposition, possibly through a leak in the vacuum system. This spectrum may be thought of as the 'base' or 'substrate' spectrum.

Three of the spectra recorded are shown in Fig. 6.12. The spectrum Fig. 6.12(a) is that of a sample refluxed in I.P.A. vapour and the peaks show the presence of elemental silicon and silicon bonded with oxygen, as well as carbon, nitrogen, calcium and sulphur. The latter elements (C, N, Ca and S) are commonly found on unetched substrates, although the carbon peak was noticeably large, suggesting up to 20% surface coverage approximately. The reason for this high carbon content is not clear, but it may be due to some cracking of the alcohol molecules during refluxing. The oxygen peak consists of two contributions; one from adsorbed oxygen molecules and the other from oxygen which is bonded to silicon atoms. The peak due to bonded oxygen is shifted very slightly from that of the adsorbed gas, but the result in this case is a broader peak than normal. Again there may be some connection between the refluxing process and the surface oxygen level. After ion bombardment the Si(O), N, Ca and S peaks disappeared completely, confirming that they were surface contaminants. The magnitude of the C and O peaks was greatly reduced. Clearly, although refluxing in I.P.A. may degrease the sample adequately, the surface is not chemically clean, and some etching is required to remove the surface layer before the fabrication of electronic devices. The possibility also arises that I.P.A. refluxing may give rise to increased carbon and oxygen contamination.

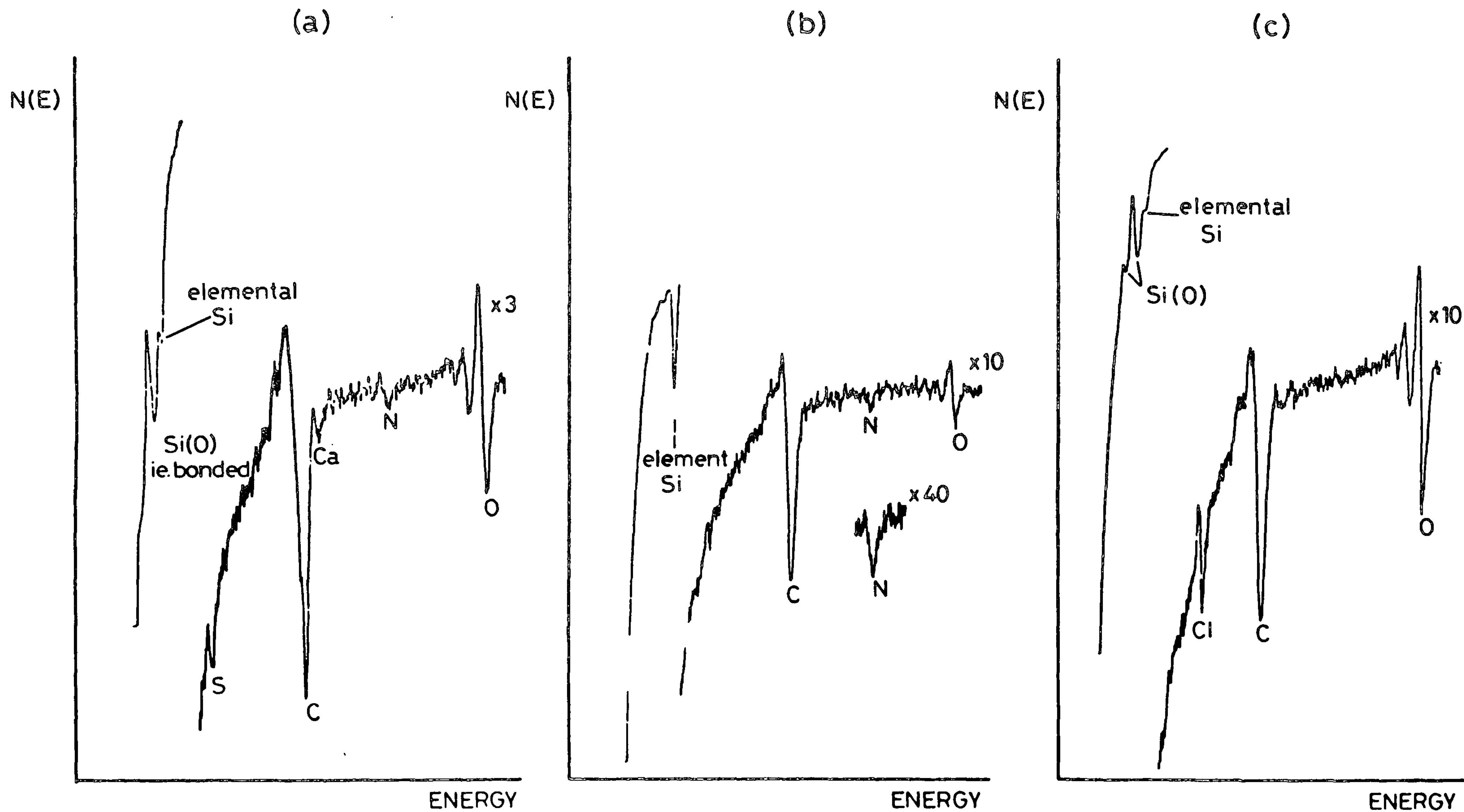


Fig. 6.12 Scanning Auger analysis on samples with three different preparation procedures.
(a) refluxed in I.P.A, (b) refluxed in IPA and etched in buffered HF,

Buffered Hydrofluoric acid (1:5 HF:HNO_3 by volume) is widely used in silicon technology as an oxide stripper. Fig. 6.12 (b) shows the Auger spectrum of a sample which was refluxed in I.P.A. and then etched for 2½ mins. in buffered HF. The most noticeable effect is the almost total removal of the Si(O) peak, which is to be expected. (A small amount of oxide will form between etching and insertion into the vacuum system : this is unavoidable). The reduction is reflected in the reduced O peak which is largely due to adsorbed oxygen. The carbon peak is reduced from that in Fig. 6.12(a) but it is still unusually large. In general though, the surface is relatively clean after this treatment.

In Fig. 6.12(c) the effect of carrying the etching a stage further is shown i.e. the sample was refluxed in I.P.A., etched for 2½ mins in buffered HF and then washed for 15 mins in freshly prepared chlorine water. After this treatment the C peak is largely unchanged. The Si(O) peak has returned and implies an oxide coverage of a large part of the surface : the O peak is correspondingly increased. The presence of chlorine on the surface is also indicated. Further etching in buffered HF does not remove the Cl peak, implying that the chlorine is not just 'sitting' on the surface but is bonded in some way e.g. physisorption or chemisorption. The surface layer, once formed, is very stable, as the spectrum exhibits no change even when the sample is left in air for several days.

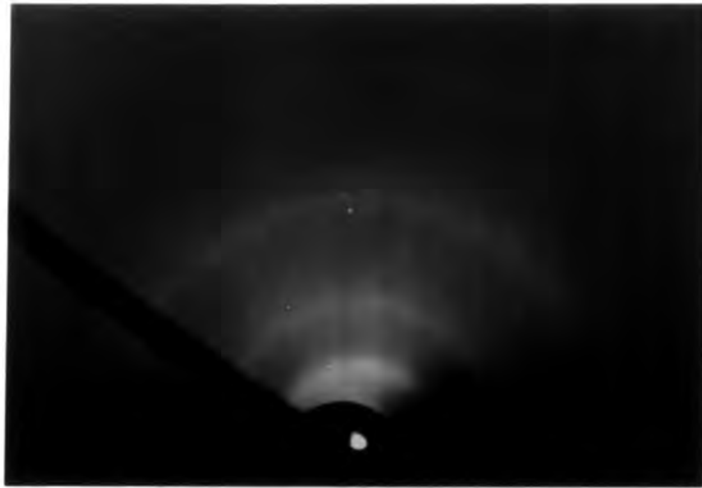
Further investigations would be needed to clearly establish the role of chlorine in improving the dipping probability. From the results presented however, it would seem that the role of chlorine is an 'active' one i.e. it is not a case of the chlorine having an effect on the surface which enhances dipping, but rather that the chlorine becomes attached to the α-Si:H surface and actively participates in the dipping procedure. One possible explanation is as follows. There is evidence to show that the first monolayer of LB film reacts with the substrate, involving some sort

of ion exchange[8,9]. In α-Si:H, the presence of hydrogen may well passivate the surface, leaving it generally unreactive and thus unreceptive to LB films. (Alternatively the surface may be passivated because of the oxide coverage). Chlorine, as an oxidising agent, could initiate a number of reactions at the α-Si:H surface e.g. by breaking Si-H bonds leaving dangling bonds which could react with O, or OH groups, or by bonding onto elements already present on the surface. Whichever reactions take place, it is likely that the chlorine left on the surface is chemically bonded to Si atoms via an intermediate group e.g. oxygen or carbon. The partial coverage of surface bonded chlorine may then react with cadmium ions from the cadmium stearate during dipping to form complexes, thus aiding the pick-up of the monolayer.

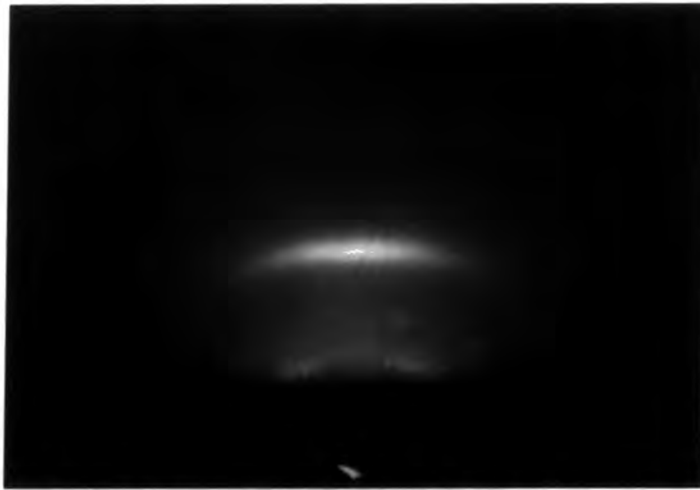
6.8.3 LB Film Quality

Having achieved successful LB film deposition onto α-Si:H it was necessary to check the quality of the deposited films. There are several methods which may be used, each of which gives information on different aspects of the film quality. Electrical measurements involve the addition of a metal contact to form an MIS structure and test the insulating qualities of the multilayer (J-V) as well as the reproducibility of the monolayer thickness ($^1/_C$ v N). Experiments of this type were performed, and the results will be described in subsequent chapters. Data from RHEED monographs give information on the degree of structural perfection of an LB film : these data will now be discussed.

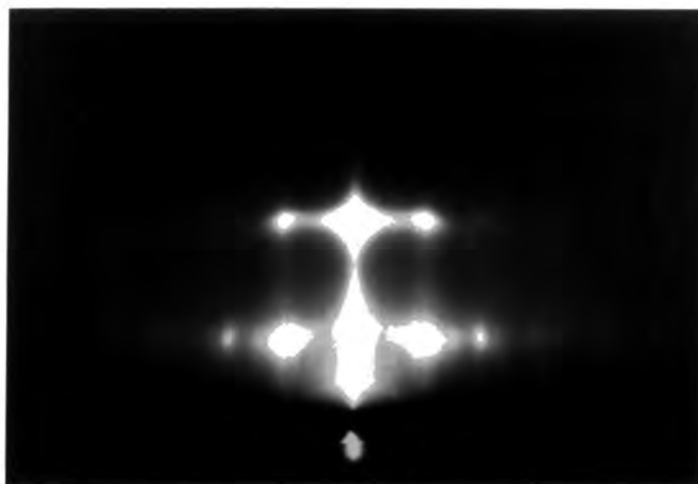
Fig. 6.13(a) shows an RHEED micrograph for an α-Si:H sample with no LB film covering. The diffuse rings clearly show that the film is truly amorphous, and the spacing of the rings corresponds to the average spearation of the (silicon) atoms. Fig. 6.13(b) shows an RHEED micrograph for an α-Si:H sample with 11 monolayers of cadmium stearate deposited. This LB film thickness was chosen because experiments on other semiconductor



(a) α-Si:H substrate



(b) α-Si:H with 11 monolayers CdStearate



(c) Single crystal InP with 11 monolayers CdStearate ({100} surface).

Fig. 6.13 RHEED micrographs.

substrates showed that thicker films exhibited a lower degree of order, while thinner films gave rise to diffraction patterns with a significant contribution from the substrate. The diffuse rings have disappeared to be replaced by arcs, and their spacing is different from the pattern in Fig. 6.13(a), indicating that the arcs are indeed due to the LB film. Arc patterns are associated with structures which are made up of grains, where all of the grains have a preferred common orientation, which is perpendicular to the plane of the substrate[4]. The appearance of an arc rather than a spot means that the grains do not have a common orientation in the plane of the sample; in fact the length of the arc is a measure of this misorientation. The observation that the diffraction pattern did not change when the sample was rotated about the axis perpendicular to the surface leads to the conclusions, (a) that the grains are randomly oriented in the plane of the sample, and (b) that the grain size is very much smaller than the effective area sampled by the electron beam. (This area corresponds to an ellipse whose major axis is defined approximately by the length of the sample (in our case $\sim$ 5 mm), and whose minor axis is defined by the spot size of the beam ($\sim$200 μm).)

Russell et al[10] have studied cadmium stearate LB films on a number of different substrates using the RHEED technique. Fig. 6.13(c) shows their data for an 11-layer film on single crystal InP. Almost identical patterns were obtained on Si and GaAs. The spot pattern is clear evidence for a high degree of order in the LB film i.e. not only in the stacking of the monolayers but also in their structure in the plane of the substrate. The streaking of the spots is largely due to the highly polished nature of the InP surface and hence the flatness of the LB film, leading to a limited penetration depth of glancing-angle high-energy electrons. The full details of the analysis are inappropriate here; it is sufficient to note that the structure observed in the diffraction pattern is that of the C_2H_4 subcells, and that the packing of the molecules is orthorhombic.

Comparing Figs. 6.13(a) and 6.13(b) we note that, although the film on α-Si:H exhibits a lower degree of order, both diffraction patterns arise from the same structure. The influence of the substrate on the LB film structure is obviously important. It would seem that either the topography (i.e. surface roughness) or the atomic arrangement of the α-Si:H results in LB films with a lower structural perfection than is normally attainable on single crystal semiconductors.

6.8.4 Top Contact Evaporation

All evaporations were carried out using an Edwards 305 vacuum coating system, comprising of rotary and diffusion pumps (incorporating a cold trap) evacuating a glass work chamber to pressures of the order of 10^{-7} torr. Pressure measurements were made using the Pirani and Penning gauges fitted to the system. A quartz crystal film thickness monitor attachment was used to monitor the thickness of evaporated films. Metals were evaporated either from molybdenum boats or, where appropriate, tungsten filaments. Up to four separate sources could be used, powered from an integral low tension supply. The samples were mounted onto a copper substrate holder which could be heated via an internal heater or cooled through contact with an external liquid nitrogen reservoir. Electrode patterns were defined by contact masking. In all cases the metal source was shuttered i.e. no deposition onto the sample was allowed until a steady stream of evaporated metal was established. The rate of deposition could also be monitored.

For Schottky barrier contacts, evaporations were carried out at pressures between 10^{-6} and 10^{-7} torr. The rate of deposition used was variable, but was typically 0.2 Å sec^{-1} for gold and somewhat higher for palladium (approaching 1 Å sec^{-1}) which was more difficult to control.

LB films are quite susceptible to damage due to the heating effect of the stream of metal vapour during evaporation, or of the radiant heat from the evaporation source, causing shorting of the films by burning

through to the back contact. Certain precautions must therefore be taken in fabricating devices incorporating LB films. In the course of this project two methods were used to avoid this type of damage. The first method was based simply on cooling the substrate holder, and thus the sample, to very low temperatures ($\sim$ - 120°C), and performing a slow evaporation (i.e. a rate of about 0.05 Å sec^{-1}). The procedure may be outlined as follows:

1. The sample was inserted into the vacuum system and the work chamber was roughed out.
2. The chamber was flushed three times with dry nitrogen to ensure the removal of all water vapour (to prevent condensation on the sample during cooling).
3. Substrate cooling was commenced (the temperature was monitored using a thermocouple). At 0°C the baffle value was opened and the chamber pumped down using diffusion pump.
4. After several hours the metal was evaporated as slowly as possible.

This method proved to be quite successful. The main disadvantages were the length of time taken and the cracking of metal contacts which sometimes occurred during warming up (i.e. back to room temperature).

The second method employed was rather simpler. The sample was mounted and the chamber evacuated as normal to a pressure $\sim 10^{-6}$ -10^{-7} torr. The evaporation was then carried out in stages, commencing with a 5 Å deposition, then 10, then 15, and so on. A twenty minute gap (minimum) was left between each evaporation. This procedure was found to be quite adequate and was used in preference to the first because no electrode cracking problems were encountered.

The storage and handling of devices is an important consideration. After LB film deposition and before top contacts were evaporated, all

samples were stored in a desiccator to ensure that the film had thoroughly dried out. Between measurements devices were returned to the desiccators again to avoid the degradation and inconsistencies in measurements which can arise from the absorption of water vapour by LB films. Samples were also stored in the dark at all times to avoid light induced effects in the α-Si:H substrates (see section 2.6).

A photograph of a completed sample (actual size 2x4 cm) is shown in Fig. 6.14. The light, outer edge of the specimen is the stainless steel base, to which the back contact is made. The inner, darker rectangle is the α-Si:H. Different parts of the substrate were dipped with different LB film thicknesses, and these can be clearly seen on the right hand side. The regions correspond to 31, 27, 23, 19, 15 and 11 layers of cadmium stearate/stearic acid LB film. The large number of circular, gold top contacts (actual size ∿ 0.5 mm diameter) meant that many devices on a single substrate could be characterised to obtain 'typical' device properties.

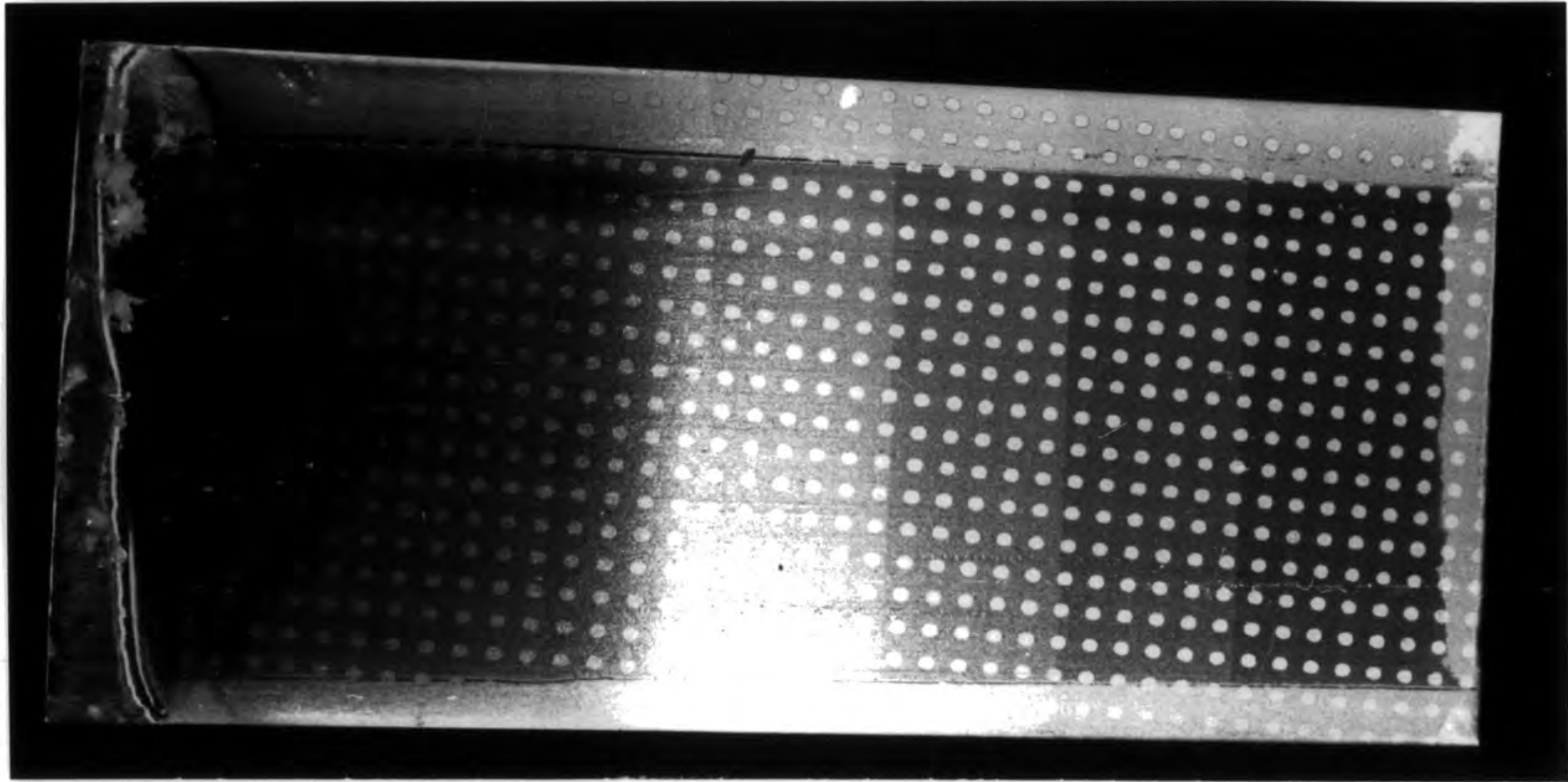


Fig. 6.14 Photograph of a completed sample showing α-Si:H/LB film MIS devices of varying insulator thickness

CHAPTER 7

SCHOTTKY BARRIER RESULTS

7.1 Introduction

One of the aims of the work presented in this thesis was to fabricate and test tunnelling MIS devices utilizing LB films on α-Si:H. Now the basis for such MIS devices is the simple metal-semiconductor structure. Consequently, it was felt that an investigation of α-Si:H Schottky diodes, with a view to a good understanding of their properties, was an essential precursor to the MIS studies. This chapter therefore contains the results obtained on α-Si:H Schottky barriers. The first section deals with some of the problems associated with different Schottky contact metals. In the following two sections the detailed characterisation of the devices using current-voltage and admittance v voltage (and frequency) measurements is described. The final section is concerned with the effects on device performance brought about by the etch treatment necessary to achieve LB film deposition. A summary of the data and the important conclusions is given at the end of the chapter.

7.2 Schottky Barrier Contact Metals

Schottky barrier devices were formed on a number of different undoped α-Si:H substrates, using both gold and palladium as the metal electrode. The fabrication details have already been described (see section 6.8.2). The choice of gold as a Schottky barrier metal was made because of its relatively high work function (∿5.2eV) and ease of evaporation. Of all the high work function metals eg Pt, Pd, Au, Cr, gold is by far the easiest to thermally evaporate by means of resistive heating. Thin, semi-transparent contacts, suitable for measurements under illumination, can also be made without difficulty. Unfortunately, problems were encountered with the stability of some gold - Schottky barrier devices. Similar effects have been noted by other workers when using gold electrodes[1]. After a short

time, sometimes only a few days, the rectifying properties of these diodes disappeared, possibly due to the diffusion of gold atoms into the α-Si:H. The application of an electric field usually accelerated the rate of degradation and so, in general, gold contacts were only used for relatively short term measurements. Palladium, which has a work function approximately equal to that of gold, proved more troublesome to evaporate by resistive heating under vacuum (the recommended technique, namely electron-beam evaporation was not available). However, it was found to result in more stable devices[2] and was used for some measurements.

7.3 Current-Voltage Characteristics

The semi-logarithmic plot of the dark J-V characteristics of a good α-Si:H Schottky diode is shown in Fig. 7.1. These curves are for a Pd top contact of thickness ∿ 100 Å and area ∿ 1.96×10^{-3} cm^2 on undoped (weakly n-type) Dundee α-Si:H, deposited on a stainless steel substrate. The back contact comprises a highly doped n^+ layer (see section 6.8.1). The measurements were taken at room temperature and at atmospheric pressure. The inset to Fig. 7.1 shows a linear J-V plot of the data taken at bias voltages greater than 0.4V.

The general shape of the curves is very similar to that for Schottky diodes based on single crystal semiconductors and also corresponds well with data on α-Si:H published by other workers[2-9]. The forward current-voltage curve exhibits a linear portion at low voltages, whilst at higher voltages the current becomes limited by the series resistance. The reverse current rises slowly with increasing reverse bias. The diode has a rectification ratio (at 0.3V) of almost 10^4; comparable values reported in the literature range from 10^3 to 10^5 [3, 6, 9]. The various regions of the curves will now be discussed in some detail.

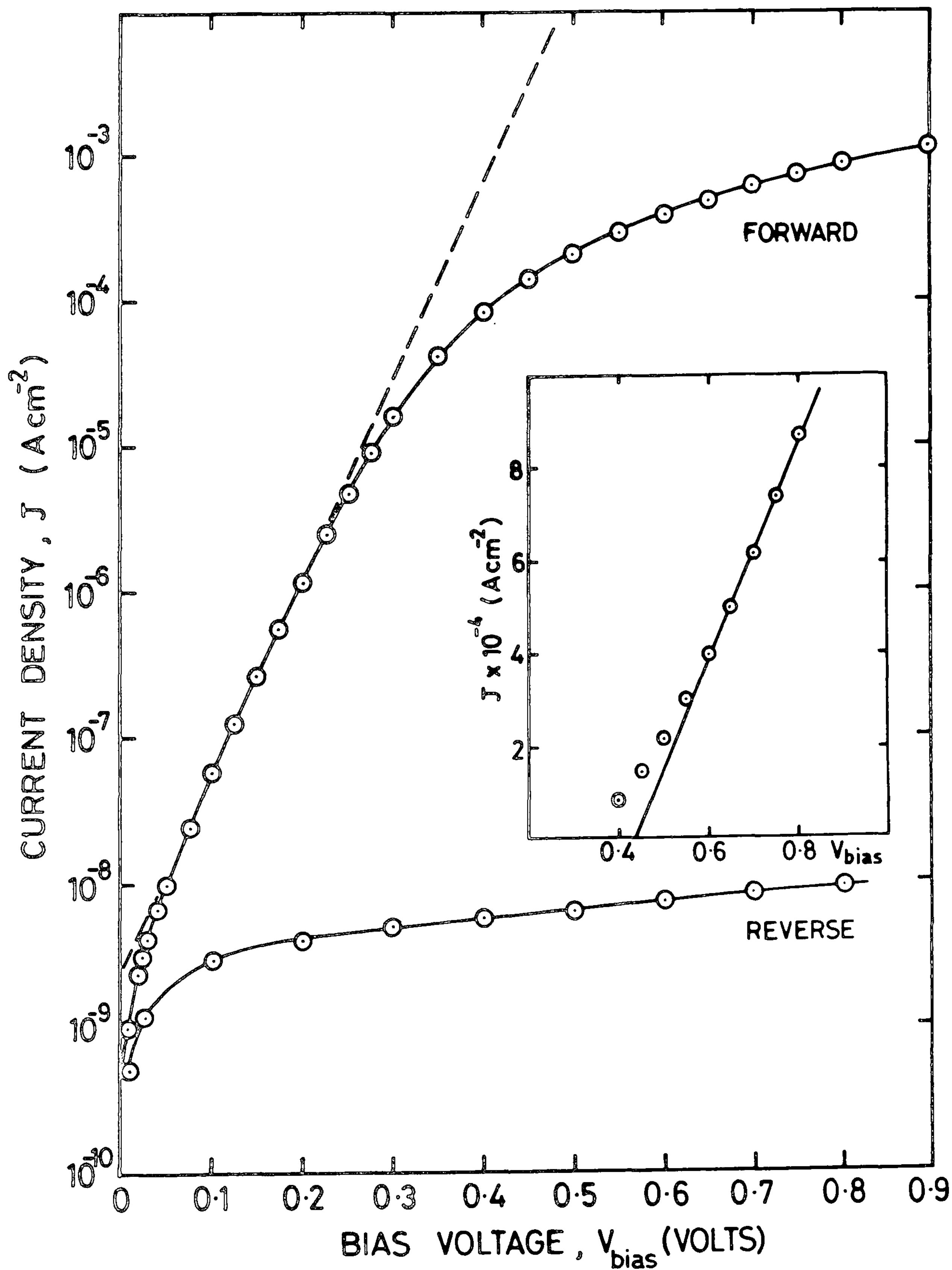


Fig. 7.1 Forward and reverse current characteristics for Pd - n-αSi:H Schottky barrier measured in the dark at room temperature. Inset shows linear J-V plot for forward bias.

7.3.1 Forward Bias

Barrier Limited Region

For bias voltages greater than 3kT/e and less than 0.3V the forward ln J v V characteristic is approximately linear, obeying the modified diode equation

$$J = J_o \exp\left(\frac{eV}{nkT}\right) \qquad (3.16)$$

From this linear region two important diode parameters may be found, namely the ideality factor n and the saturation current density J_o. The n value is derived from the slope of the line and is 1.28 for this particular diode. For an ideal device n would be unity, and n-values greater than this can arise for a number of reasons (see section 3.2.3). The effect of barrier lowering caused by the applied bias (the Schottky Effect) leads to non-ideality and n-values slightly greater than one. Clearly this is not sufficient to explain the deviation from ideal behaviour in our present case. Recombination in the depletion region, the presence of an interfacial layer and surface states can all give rise to ideality factors rather larger than one, and any one or a combination of these mechanisms could be responsible for an n-value of 1.28. Ideality factors from 1.01 to 2 have been reported for α-Si:H Schottky diodes[2-4,6-9]. It would thus seem that a value of 1.28 was not unreasonable. Indeed, in a rather extensive study of Pd/α-Si:H Schottky diodes, Thompson et al[3] measured n = 1.23 for unannealed devices.

The saturation current density is given by the intercept of the extrapolated linear region on the current axis. From Fig. 7.1 this gives $J_o \sim 2.4 \times 10^{-9}$ A cm^{-2}. In Schottky barrier work on single crystal semiconductors the barrier height ϕ_B can be calculated from the J_o value using

either the thermionic emission equation

$$J_o = A^* T^2 \exp\left(\frac{-e\,\phi_B}{kT}\right) \qquad (3.8)$$

or the diffusion theory equation

$$J_o = e\mu\, N_c\, E_s \exp\left(\frac{-e\,\phi_B}{kT}\right) \qquad (3.6(b))$$

whichever is appropriate. The correct method for calculating ϕ_B from J_o (determined from the J-V curves) for α-Si:H diodes is a matter of current debate. Different authors have reported the existence of diffusive transport[3,4,10] and also thermionic emission[6,8,11] in α-Si:H barriers. The situation is far from clear, but as Wilson and McGill have pointed out[12] the two theories give rather similar results, and since both calculations involve a number of assumptions the choice is rather arbitrary. The thermionic emission barrier height ϕ_B (therm) may be calculated from equation 3.8 assuming the value of the Richardson's constant A^*. Following Wilson and McGill[12] and taking $A^* = 100\ A\ cm^{-2}\ k^{-2}$, the value for n-type single crystal Si, ϕ_B (therm) for the device whose characteristics are shown in Fig. 7.1 is 0.90 eV. The application of diffusion theory requires a knowledge of the pre-exponential factor in equation 3.6(b). If, after Wronski et al[3], this is taken to be $3 \times 10^6\ A\ cm^{-2}$ then ϕ_B (diff) is 0.87 eV. Other workers have found similar barrier heights[3-5, 7-9]. It should, however, be noted at this point that the application of thermionic-emission theory or diffusion theory is questionable in many cases. If the diode is far from ideal i.e. if $n > 1.1$ then both approaches are invalid, and the physical significance of the calculated barrier height is unclear.

This consideration does not seem to have been widely appreciated in many of the papers published on this topic. Nonetheless, the values of ϕ_B do form a useful means of comparing the characteristics of different diodes.

Series Resistance Limited Region

Under forward biasing in excess of 0.3V the J-V graph begins to deviate from the ln J $\propto$ V relationship, indicating the increasing effect of the diode series resistance. This occurs simply because of the voltage drop across the bulk semiconductor and the 'ohmic' back contact. The series resistance for this diode was ohmic, as shown by the linear J-V relationship plotted as the inset in Fig. 7.1. From the slope of this line the series resistance is estimated to be $\sim 2 \times 10^5\ \Omega$. Neglecting the back contact resistance this corresponds to a resistivity of about $4 \times 10^6\ \Omega$ cm, assuming an α-Si:H film of 1μm thickness. This resistivity is rather low, even taking into consideration the spread in the conductivity of different undoped α-Si:H films deposited under ostensibly the same conditions[13]. There are several possible explanations. The film may have been unintentionally doped, although this is unlikely because of the well-tried and scrupulous deposition procedures employed at the University of Dundee. Alternatively, an overestimate of the film thickness would result in a reduced resistivity, but the size of the discrepancy cannot be explained by this. The most likely cause is the presence of pinholes in the film giving rise to shorting to the back contact. Such pinholes have been shown to occur in glow discharge α-Si:H and they are thought to originate from the presence of fine dust particles in the reaction chamber during growth[9].

The linear J-V plot in the series resistance limited regime (see inset of Fig. 7.1) can be used to find the built in voltage, V_o, which measures the semiconductor band-bending. Goodman[14] has shown that the extrapolation of the line to zero current (i.e. the voltage axis) gives

an approximate value for V_o. For the device whose characteristics are shown in Fig. 7.1, $V_o \approx 0.44$ V. Wronski et al[3,4] have also used this 'far-forward bias' technique with similar results. The experimentally determined values of V_o and ϕ_B may be used to find $(E_C - E_F)$ since $\phi_B = V_o + (E_C - E_F)$. In our case this gives a value of 0.46 eV. Typically, $(E_C - E_F)$ is around 0.6 eV in α-Si:H samples deposited at 250°C. However, bearing in mind the uncertainty in ϕ_B, because of the high n-factor, the agreement is reasonable.

7.3.2 Reverse bias

The slowly rising current with reverse bias shown in Fig. 7.1 is quite typical for α-Si:H and has been seen by most other research groups[2, 5-7,9]. The notable exception is the RCA group who have reported saturated reverse currents[3,4]. 'Soft' reverse J-V characteristics are often found in metal-single crystal semiconductor Schottky diodes and may be due to a number of factors e.g. a field dependent barrier height, tunnelling of carriers because of edge effects or generation in the depletion region.

7.3.3 Temperature Dependence of Forward J-V Characteristics

The temperature dependence of the forward bias J-V characteristics of a gold α-Si:H Schottky diode are shown in Fig. 7.2. The substrate was Dundee α-Si:H, as for the device described in the previous section, and the Au top contact was ∿ 150 Å thick and ∿ 2mm in diameter. Measurements were made in the dark under a low pressure of helium. Similar data have been published by workers in several other laboratories[3,7,11] although they have used higher temperatures than those shown in Fig. 7.2. High temperatures were not used in these investigations because of the danger of effects due to annealing and/or device degradation.

It is interesting to note that the curves retain a linear region at each temperature investigated. The n-factor calculated from these graphs

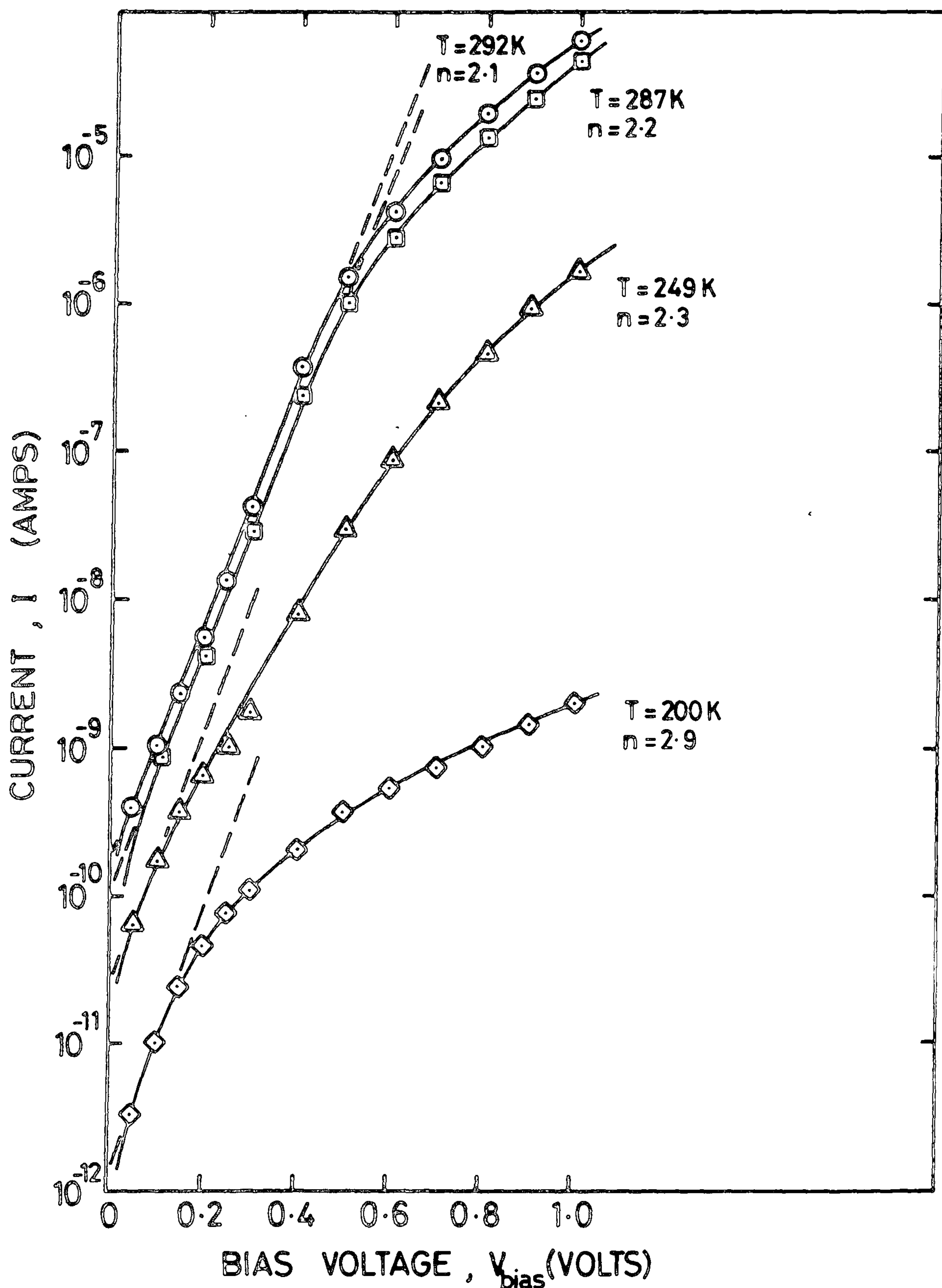


Fig. 7.2 Forward I-V curves at different temperatures for an Au-n-α Si:H Schottky diode

is distinctly temperature dependent, changing from 2.1 at 292K to 2.9 at 200K. However, it does not follow the so called 'T_o rule' (see section 3.2.3) proposed by Padovani and Sumner[15], namely

$$n = 1 + \frac{T_o}{T}$$

where T_o is the excess temperature, since a plot of n against $1/_T$ is non-linear. Deviations from this rule can occur at low temperatures because of edge effects causing thermionic field emission[16]. Experiments using guard ring structures would be necessary to remove the possibility of this effect occurring. An ideality factor which increases with temperature has also been observed by Vieux-Rochaz et al[7], whereas Wronski et al[3] and Sussman et al[9] found n to be temperature independent. These apparently contradictory results on similar α-Si:H samples would suggest that slight differences in Schottky diode preparation procedures between the groups can have a significant influence on experimental results.

The magnitude of J_o decreases as the temperature is reduced, which is to be expected. Calculations of the barrier height by thermionic emission theory (TET) and by diffusion theory (DT), using the same assumptions as before, show that the barrier height follows the same trend. Over the one hundred degree range ϕ_B (therm) drops from 0.88eV to 0.65eV, whilst ϕ_B (diff) falls from 0.85eV to 0.64eV. This is non-ideal behaviour, since equations 3.8 and 3.6(b) both assume a temperature independent ϕ_B. Normally, the barrier height can be found from the slope of a $\ln \frac{J_o}{T^2}$ v $\frac{1}{T}$ plot (for TET) or a $\ln J_o$ v $\frac{1}{T}$ plot (for DT) using these equations. This approach has been used by several authors[3,4,7,9]. However, for these diodes such plots would be meaningless.

A linear plot of current versus voltage in the far forward bias region has been made for each of these different temperatures. Three of these are shown in Fig. 7.3. The series resistance, R_s, of this diode remained ohmic over the whole of the measured temperature range. The extrapolation of the linear I-V data yields a value for the built-in-potential[14] of $\sim$ 0.41 V which is independent of temperature. The magnitude of R_s obtained from the slope of the room temperature curve corresponds to a resistivity of the order of 10^{10} Ω cm, which is a little higher than expected. This magnitude fell exponentially with temperature. A plot of R_s against $1/T$ should have an activation energy, E_{act}, which corresponds to the energy difference between the Fermi level and the conduction band. For this diode E_{act} was calculated to be 0.22 eV. Published data on comparable samples gives E_{act} $\sim$ 0.6 eV[3,7,9]. There are several possible explanations for this discrepancy. Any temperature dependence of the carrier mobility μ will affect the graph since, strictly speaking the carrier density should be plotted against $1/T$. LeComber and Spear[17] have shown that a change in the electron mobility occurs at T $\simeq$ 250 K when the main conduction path moves from the extended states to the localised states. This transition temperature is in the middle of the temperature range used and could therefore affect the slope of the graph. Yu and Snow[18] have investigated surface effects on metal-single crystal Si Schottky diodes. They have shown that edge effects and surface charge can lead to changes in the activation energy as measured from conductivity v $1/T$ plots. It may be that this is applicable to certain α-Si:H barriers. Finally, it has been assumed that the series resistance is entirely due to the bulk α-Si:H and that the back contact resistance is negligible in comparison. This may not be the case, although to significantly affect the results the contact resistance would have to

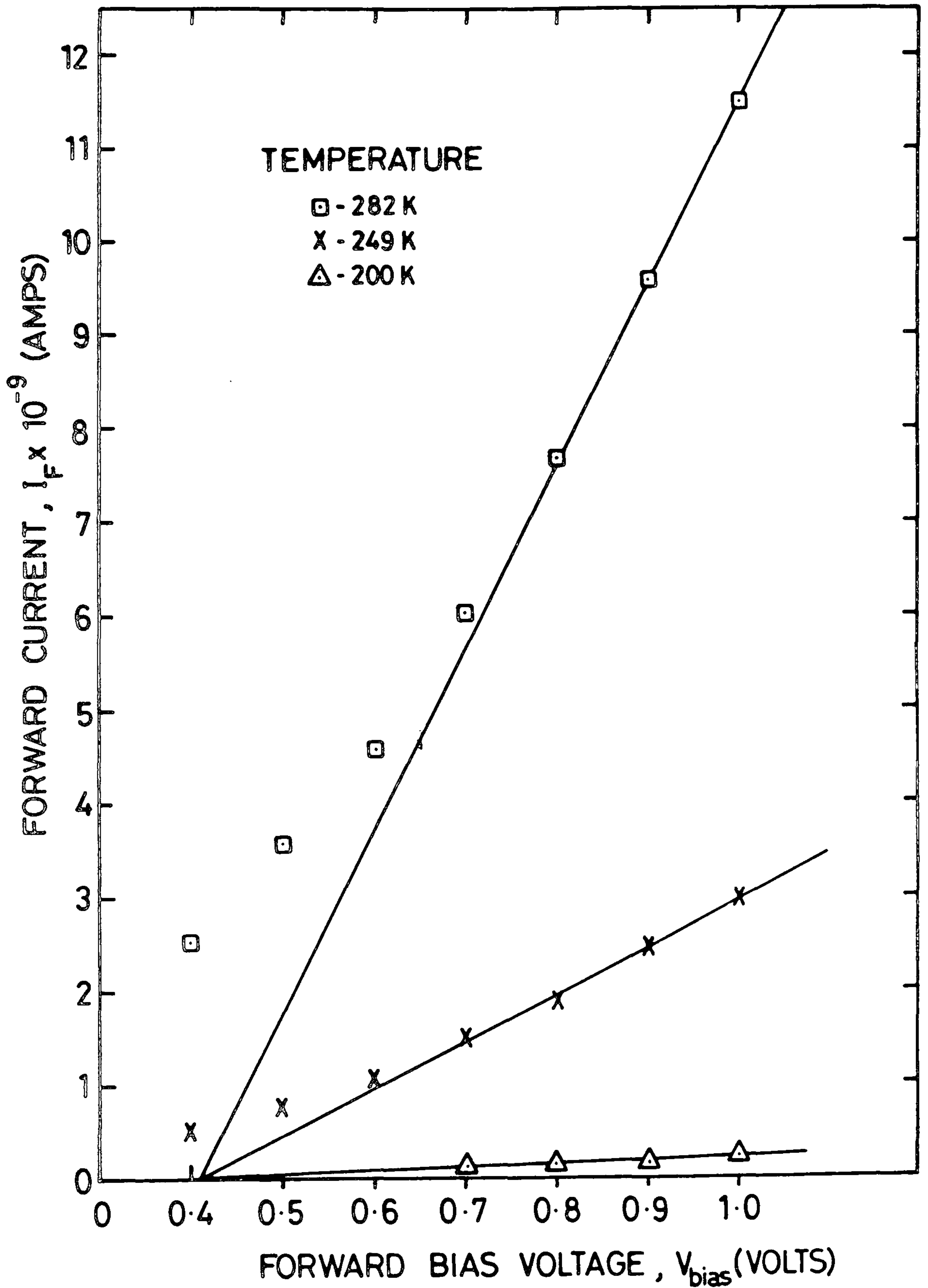


Fig. 7.3 Graph showing the linear dependence of I on the forward bias at various temperatures for the device whose ln I-V characteristics were shown in Fig. 7.2.

be very high indeed. Clearly, further investigations e.g. over a wider temperature range would be necessary in order to clarify the situation.

7.3.4 Device Reproducibility

The reproducibility of device characteristics is important in establishing the validity of experimental results. To test this, devices were fabricated using the same procedure on different semiconductor substrates, and on each one a large number of diodes was made. The important parameters of different batches of diodes ie. the ideality factor, n, and the barrier height, ϕ_B, are summarised in Table 7.1. The figures shown are typical results for a given device batch. The properties of different sets of diodes were found to vary considerably, reflecting the wide variation of Schottky barrier data reported in the literature(2-9). The ideality factors calculated from the slope of the ln J v V curves (of different sets of diodes) ranged between 1.22 and 2.16 i.e. all devices were rather 'non-ideal'. It can be seen that the n-values differed not only between diodes made on different semiconductor substrates, but also between successive batches of diodes made on the same substrate. It seems likely that these differences were due to slight variations in the fabrication procedure e.g. the time delay between completion of etching and insertion into the vacuum system for electrode evaporation. This could affect n by introducing interfacial layer of varying thickness and composition. The lowest n-value recorded (1.22 for an Au/α-Si:H device) is quite typical (3,4,6,8,10) although more ideal diodes can be made(2). This lower limit may be due to the particular α-Si:H samples used (i.e. an intrinsic property of the α-Si:H interface) or more probably a result of the method of preparation employed. The use of an oil-free evaporation system could possibly lead to improvements in device ideality.

The barrier heights shown in the table were calculated using the thermionic emission theory and the diffusion theory as previously described.

The variation for the different samples is consistent with results in the literature[2-9]. It can be seen that both theories lead to very similar values of ϕ_B, although ϕ_B (diff) is always slightly lower than ϕ_B (therm).

Table 7.1 shows data for devices made on α-Si:H from three different independent sources : the Dundee group (devices 1-7), Xerox Corp (device 8) and Plessey Research (Caswell) Ltd. (device 9). These samples were all deposited under similar conditions. No significant differences were found between J-V characteristics on the three different types of sample, which would seem to indicate that they are basically the same. However, it is thought that the J-V curves are not very sensitive to some differences which might occur e.g. variations in the gap density of states, etc. since published results from different groups often show similar J-V data but conflicting C-V data.

7.4 Capacitance and Conductance Measurements

The capacitance of α-Si:H Schottky diodes has been widely studied and many contrasting results have been reported. Various authors have attempted to explain their results using different models and these have been summarised in Chapter 3. The interpretation of capacitance and conductance data is rather tentative at this stage since the amorphous Schottky barrier is still only poorly understood. The data presented in this section will therefore be compared with other published results and discussed in the light of presently available theories. The diodes were fabricated mostly on Dundee α-Si:H : data for devices made on α-Si:H from other sources are mentioned briefly at the end of the section.

7.4.1 Frequency Effects

The zero bias capacitance (per unit area) and conductance of a Pd/α-Si:H Schottky diode are plotted in Fig. 7.4. as a function of

Device Number	Substrate Identification	Metal Contact	n Value	ϕ_B (therm) (eV)	ϕ_B (diff) (eV)
1	XSi 69	Pd	1.28	0.90	0.87
2	α-Si 10	Au	1.22	0.99	0.97
3	α-Si 4A	Au	1.60	0.94	0.92
4	α-Si 4A	Au	1.48	0.97	0.94
5	α-Si 4A	Au	1.85	0.90	0.87
6	α-Si 4A	Au	2.16	0.88	0.85
7	α-Si 4A	Au	1.50	0.94	0.91
8	α-Si 25 (Xerox)	Au	1.22	1.03	1.00
9	α-Si 8 (Plessey)	Pd	2.14	0.97	0.94

Table 7.1 Schottky barrier parameters for a variety of different devices (All data for room temperature)

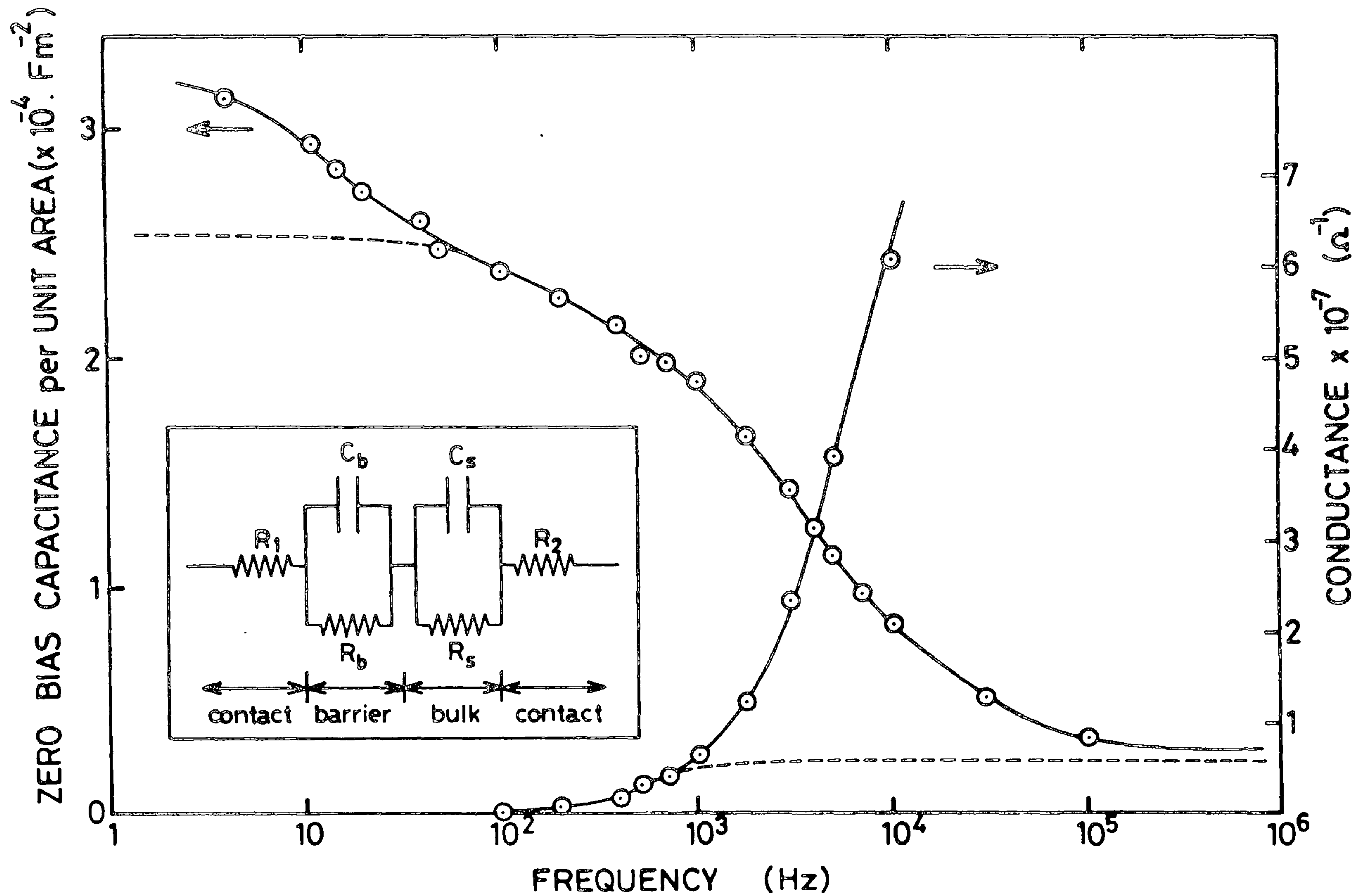


Fig. 7.4 The capacitance and conductance as a function of frequency for the device whose J-V characteristics were shown in Fig. 7.1. Measurements taken in the dark, at room temperature. Inset shows equivalent circuit.

frequency. This is the same device whose current-voltage characteristics were given in Fig. 7.1. All measurements were made in the dark with the sample at room temperature and atmospheric pressure.

Capacitance

The capacitance data are very similar to measurements reported by several different groups[6,19,20,21]. They most closely resemble the work of Beichler et al[19] and Snell et al[6,21], and the curves published by the latter group are shown in Fig. 7.5. As the measuring frequency is increased from about 1 Hz the absolute magnitude of the measured capacitance falls slowly. The rate of decrease in the capacitance becomes greater at frequencies above about 10^3 Hz and then falls again until at 10^5 Hz the capacitance has reached a constant, minimum value.

The observed frequency dependence may be explained by taking into account firstly, the existence of states in the gap of α-Si:H, and secondly, the equivalent circuit of the specimen as a whole.

(1) The Presence of States in the Gap

In an ideal metal/single-crystal semiconductor Schottky diode the barrier capacitance should be independent of frequency, up to the limit corresponding to the dielectric relaxation time of the semiconductor. However, real diodes often exhibit a capacitance which is a complicated function of frequency because of the presence of trapping levels in the bulk semiconductor or interface states[22]. It is therefore not surprising that Schottky barrier devices on α-Si:H have a frequency dependent capacitance, since localised states are known to exist in a continuous distribution across the forbidden gap. Their effect may be understood as follows. The lifetime of these states is a function of their position (in energy) relative to the conduction and valence band edges. It is

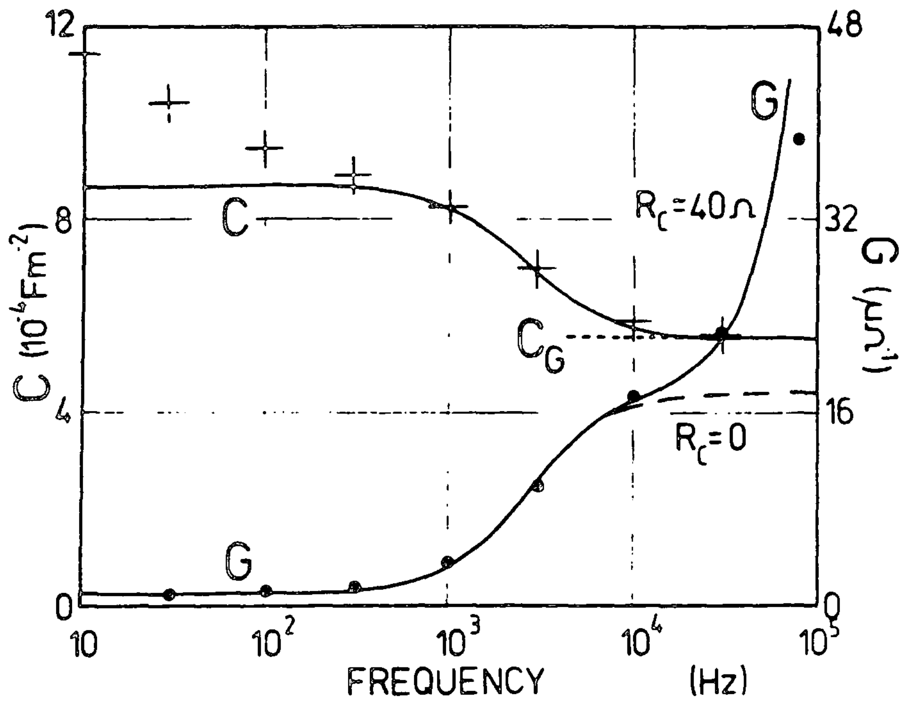


Fig. 7.5 Capacitance-frequency and conductance-frequency curves for a gold/α-Si:H Schottky barrier (after Snell et al, ref. (6)).

generally assumed that the lifetime, τ, increases exponentially with energy difference $(E_C - E_S)$, where E_C is the energy of the conduction band edge and E_S the energy of the state. That is

$$\tau = \tau_o \exp\left(\frac{E_C - E_S}{kT}\right) \qquad (3.22)$$

where τ_o is a constant. Because of the band-bending in the semiconductor depletion region, some of the localised states which would be below the Fermi level in the bulk are raised above E_F, and their state of occupancy is changed. As discussed in Section 3.2.2, the application of a small a.c. signal modulates this localised state occupancy and gives rise to a differential capacitance. However, only these states with lifetimes satisfying the inequality

$$\tau << \frac{1}{f}$$

where f is the measuring frequency, will be able to respond to the signal, and contribute to the measured capacitance. Thus, the magnitude of the barrier capacitance is expected to decrease with increasing frequency, as fewer and fewer states can respond. The exact form of the frequency dependence is not simple, depending on the exact distribution of gap states, the device bias voltage, temperature etc.

(2) The Device Equivalent Circuit

The above discussion relates to the barrier capacitance of a diode. In practice, devices are made on substrates whose thickness is far greater than the depletion width, thereby adding a 'bulk' region to the barrier region. Real devices must also have metallic contacts, which may or may

not be ohmic and of low resistance. Consideration must be given to possible frequency effects arising from these. In other words, one must be sure that the true properties of the barrier are being measured rather than some artefacts of the device configuration. A suitable equivalent circuit for modelling this is shown in the inset of Fig. 7.4 (following the approach of Snell et al[6]). The barrier has a resistance R_b and a capacitance C_b. The bulk resistance and capacitance are R_s and C_s respectively, and the contact resistances are represented by R_1 and R_2. All of these components are voltage and frequency dependent.

From the analysis of the circuit[6] the measured capacitance is given by

$$C = \frac{R_b{}^2 C_b + R_s{}^2 C_s + \omega^2 R_b{}^2 R_s{}^2 C_b C_s (C_b + C_s)}{(R_b + R_s)^2 + \omega^2 R_b{}^2 R_s{}^2 (C_b + C_s)^2} \qquad (3.26)$$

neglecting contact resistances. Two distinct frequency regimes may be identified using this expression. At low frequencies ($\lesssim 10^3$ Hz) the measured capacitance should be constant and equal to the barrier capacitance, providing that the barrier resistance R_b is much greater than the series resistance of the bulk R_s. From Fig. 7.4 it can be seen that the C-ω curve does exhibit a shoulder at low frequencies (< 100 Hz), and the constant barrier capacitance has been sketched in (see dotted line). Nonetheless, it is clear that as the signal frequency is reduced the measured capacitance begins to rise again. Exactly the same trend has been observed by Snell et al[6] (see Fig. 7.5), and measurements by Beichler et al[19] indicate that the capacitance is still rising at frequencies as low as 10^{-3} Hz i.e. the predicted saturation is not seen. This is because of the increasing contribution of the gap states, some of which must have extremely long lifetimes (> 10^3 sec).

With increasing frequency we note a region of dispersion centred at about 10^3 Hz. The model predicts that at high frequencies the measured capacitance should fall to the geometrical capacitance of the structure:

$$C = C_G = \frac{C_b C_s}{(C_b + C_s)} \tag{3.27}$$

This is found to be true in our case : the high frequency capacitance agrees within experimental error with the geometrical capacitance calculated using $\varepsilon_r = 12.0$ and the nominal 1μm thickness of the α-Si:H film. From the centre frequency of the capacitance dispersion we can obtain a value for R_s, the bulk resistance, using equation 3.28. The value of R_s was calculated to be $\sim 2.8 \times 10^5$ Ω which compares very favourably with the value of series resistance taken from the far-forward-bias J-V graph.

Conductance

The zero bias conductance - frequency curve for the Pd/α-Si:H diode is also shown in Fig. 7.4. The conductance is very low (approaching zero) for frequencies less than 100 Hz. Above this value the device conductance rises slowly and begins to level off. On reaching 10^3 Hz the conductance increases sharply. Snell et al[6,21] are the only authors to present corresponding sets of capacitance and conductance data as a function of frequency (see Fig. 7.5). There is very good agreement between our data and theirs. According to the analysis of the equivalent circuit the measured conductance is given by

$$G = \frac{R_b + R_s + \omega^2 R_b R_s (R_b C_b^2 + R_s C_s^2)}{(R_b + R_s)^2 + \omega^2 R_b^2 R_s^2 (C_b + C_s)^2} \tag{3.27}$$

At frequencies below about 10^3 Hz, providing $R_b >> R_s$, the measured conductance, G, approaches $1/R_b$ i.e. a true measurement of the barrier conductance. For higher frequencies the conductance curve should flatten

out (see dotted line in Figs. 7.4 and 7.5) if the contact resistances are negligibly small. Snell et al[6,21] have fitted their data by including the effects of contact resistance : they calculate that the sharp rise in conductance should occur at a frequency $\omega = \frac{1}{R_c C}$. Using this expression the total contact resistance, R_c, can be determined. The conductance for our devices rises at a lower frequency than that of Snell et al[6,21] indicating a contact resistance somewhat higher than 40Ω.

7.4.2. The Effect of Bias Voltage

Capacitance

The effect of bias voltage on the capacitance of the Pd/α-Si:H Schottky barrier is shown in Fig. 7.6 for five different measuring frequencies. Once again this is the same device whose characteristics were shown earlier in Figs. 7.1 and 7.4. The measurement conditions have already been described. The frequency dependence discussed in the previous section is quite clearly seen in these curves. The absolute magnitude of the capacitance increases as the frequency decreases and more of the gap states can make their contribution, which is consistent with the data shown in Fig. 7.4. The data are in very good agreement with the published curves of Beichler et al[19], and of Viktorovitch and Jousse[23]. To facilitate comparison their results are reproduced in Figs. 7.7 and 7.8. It should be noted that Viktorovitch and Jousse were working on sputtered α-Si:H.

For the purposes of discussion the C-V characteristics may be divided conveniently into two regions i.e. forward and reverse bias.

Forward bias

The C-V curve measured at 4Hz shows a steep rise in capacitance in forward bias. This is commonly observed in metal/single-crystal semiconductor Schottky barriers : as the forward bias is increased the change in charge reduces the band-bending and the depletion width, and the capacitance rises accordingly. Beichler et al[19] and Viktorovitch and

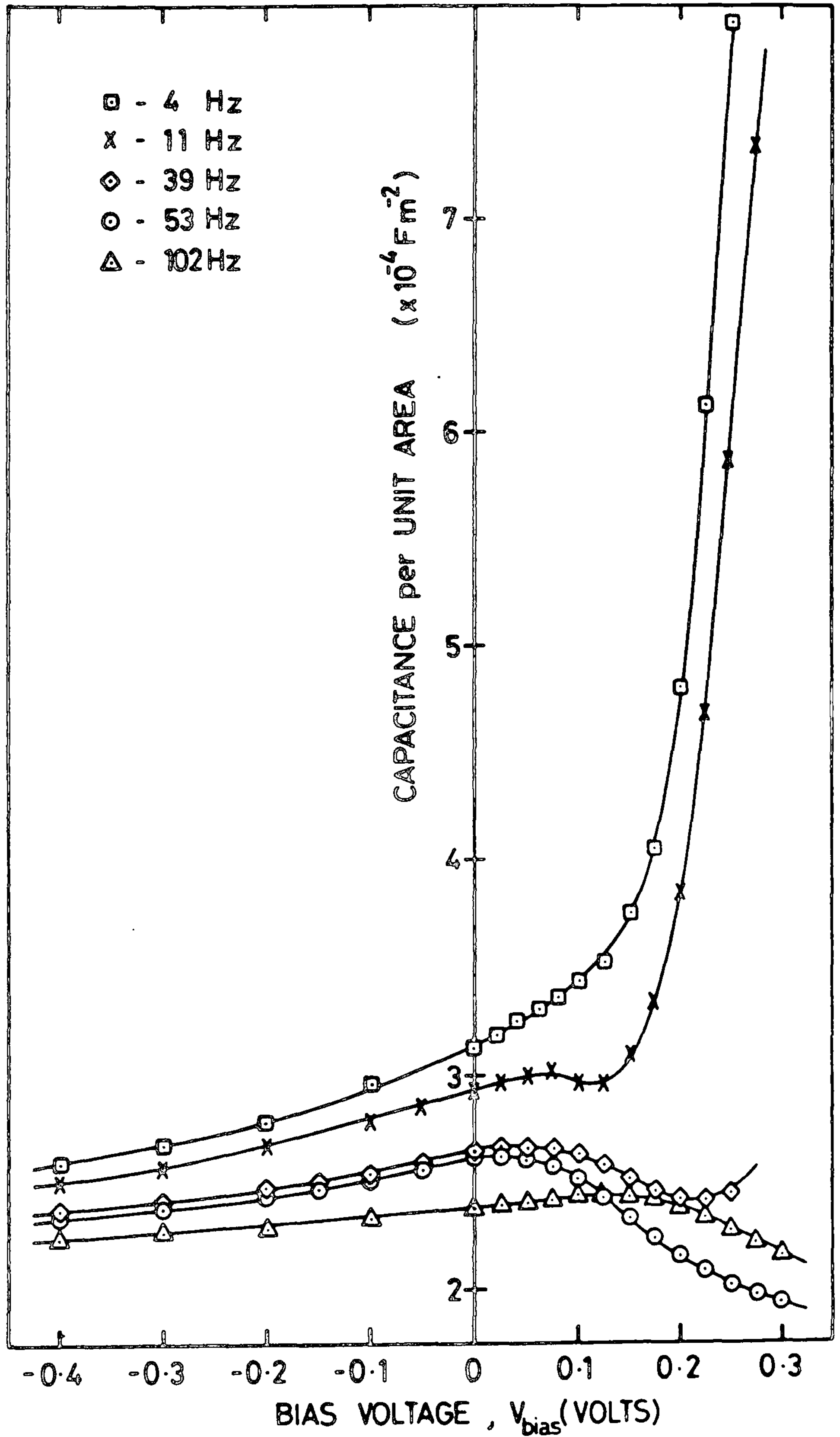


Fig. 7.6 Capacitance-bias data at several frequencies for Pd-n-α-Si:H Schottky diode (Device 1, see Table 7.1) at room temperature in the dark.

Jousse[23] show virtually identical curves for similar frequencies (see Figs. 7.7 and 7.8). It would seem at first sight that in general, for frequencies in the range 0.2 - 4Hz, the behaviour of α-Si:H diodes is rather 'conventional'.

As the measuring frequency is increased some structure becomes apparent in the C-V data. A small peak in capacitance appears, followed by a sharp rise, which is reminiscent of the 4Hz curve. These features are also seen in Figs. 7.7 and 7.8. A fall in the forward bias capacitance has also been reported by Snell et al[6,21]. These authors maintain that this fall-off is not a property of the barrier but rather an effect of the sample as a whole, and they have explained their data in terms of a simple series resistance effect. This approach has also been used by Beichler et al, and remains the only viable explanation to date.

The initial rise in C at very low forward bias is clearly the true barrier response, as seen in the 4Hz curve. Using the equivalent circuit shown in the inset of Fig. 7.4 it can be shown that as long as $R_b >> R_s$ the measured capacitance is indeed the barrier capacitance. As the forward bias is increased the barrier resistance R_b drops rapidly and this condition no longer holds. In this case the capacitance will approach C_s, the bulk capacitance, and if the forward bias is further increased it will fall to the geometrical capacitance of the structure. This may well explain the observed fall in capacitance in our data.

The subsequent rapid rise in C has not been reported by Snell et al[6,21], nor can it be explained in terms of the simple equivalent circuit approach. Although it is not shown in Fig. 7.6 the capacitance rise was observed even at the higher frequencies used e.g. at 102Hz C began to increase at V_{bias} = 0.8V. Similar features appear in the results of Beichler et al[19], and Viktorovitch and Jousse[23] report the increase up to frequencies of a few kilohertz. The most obvious explanation is that we are observing the

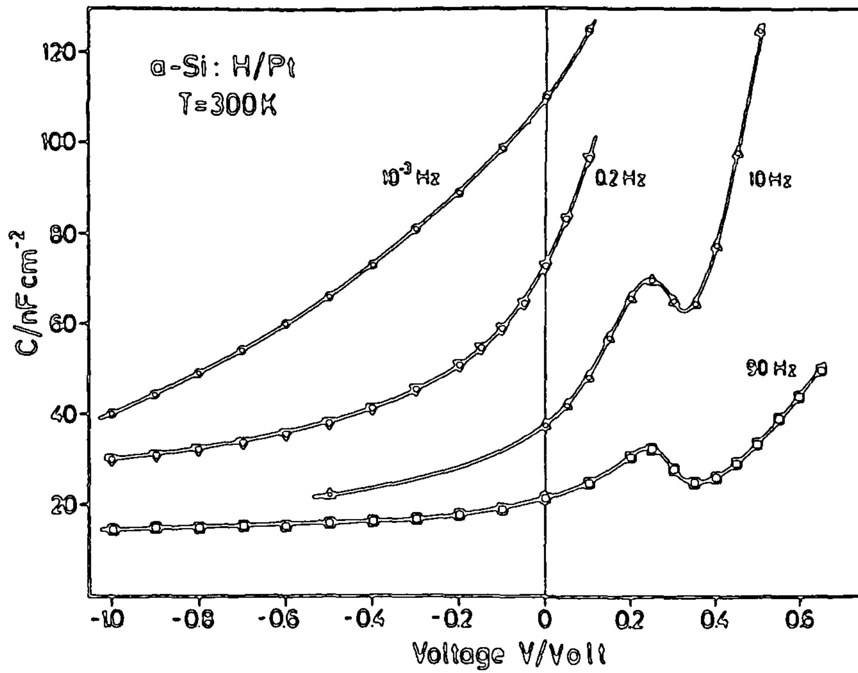


Fig. 7.7 C(V) dependence of a metal/undoped α-Si:H diode (after Beichler et al, ref. (19)).

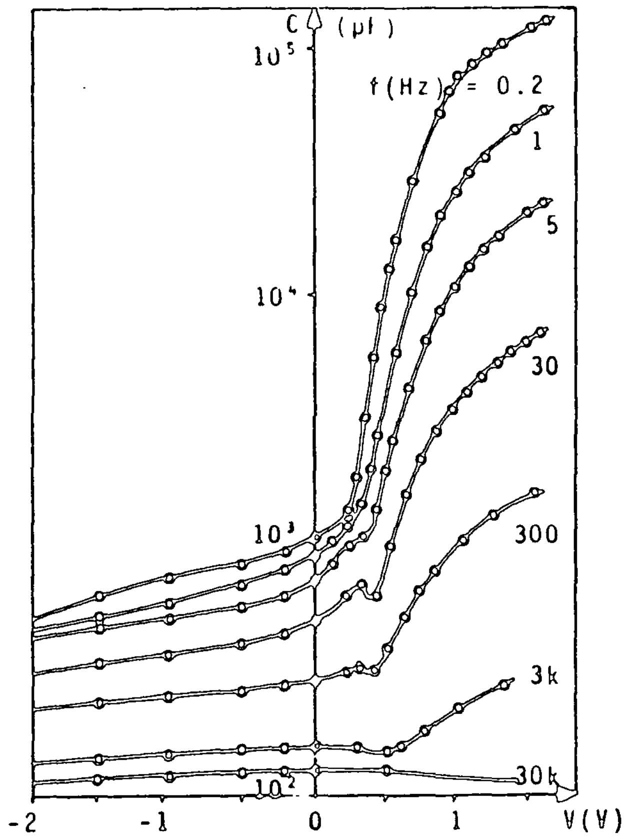


Fig. 7.8 C(V) characteristics of a gold/undoped α-Si:H diode (after Viktorovitch and Jousse, ref (23)).

true barrier properties once again, in which case a rise in capacitance in forward bias is expected. However, some alternative explanations have been proposed.

Beichler et al[19] have attributed the rise to surface states. The existence of surface states in α-Si Schottky diodes was first suggested by Wronski and Carlson[4] who estimated a density of $\sim 3 \times 10^{13}$ cm^{-2} eV^{-1}. If only a fraction of these states are in equilibrium with the semiconductor the barrier height will be bias dependent, leading to an n-value greater than unity[22]. It is interesting to note that Beichler et al[19] report n-values of $\sim$ 1.2, quite comparable with those reported here for the best diodes. These authors contend that the interface states, being far removed from the conduction band, will have very long lifetimes, so that they will only contribute to the capacitance if the temperature is sufficiently high or if a large enough forward bias is applied. A surface state contribution would also be expected at very low frequencies (since the lifetimes can be $\sim 10^{-3}$ secs). The data shown in Fig. 7.6 would seem to be consistent with this approach. As the frequency is increased fewer of the surface states can respond, hence the rise in C is not so rapid and takes place at increasing bias voltages. At very high frequencies one would expect no surface contribution at all, no matter what the bias voltage, i.e. there would be no rise in capacitance. Viktorovitch and Jousse have confirmed this with their C-V measurements at 30 kHz.

Recently, an investigation has been carried out by the Dundee group into the effect of the n+ back contact on the C-V characteristics[24]. It has been suggested that the injecting properties of this n^+ region are of crucial importance. The injection of electrons into the bulk can reduce the bulk resistance R_s considerably and hence increase the bias voltage range over which $R_b >> R_s$ i.e. the true barrier capacitance C_b can be measured over a wider bias range. Unfortunately, the injection of electrons can also lead to an anomolous rise in C as the forward bias is increased past

the flat-band voltage of the device. The data available at present are not conclusive but the possibility that the capacitance rise reported here is an injection effect cannot be ruled out.

The distribution of bulk states in the mobility gap can also lead to structure in the C-V curve. This is most evident in the case of static C-V measurements : at finite frequencies the curves can be considerably modified because of the partial nature of the gap state response[25,26]. It is considered unlikely that this is responsible for the features seen in Fig. 7.6. In particular, variations in the gap state density cannot lead to a decrease in the forward bias capacitance, they would merely alter the slope of the increasing value i.e. the slope would always be positive.

Reverse Bias

The diode capacitance was found to decrease with increasing reverse bias at all frequencies investigated (see Fig. 7.6). This is as expected in single-crystal based diodes and could be taken as evidence for 'conventional' behaviour. That this is not the case is demonstrated quite clearly by re-plotting the data of Fig. 7.6 as $^{1}/_{C^2}$ against bias, as shown in Fig. 7.9. Instead of the usual straight line graph, which is indicative of a uniform doping concentration, we observe a curved characteristic. Some authors have attempted to interpret such data as two straight line segments[4,9]. Spear et al[27] have pointed out some of the problems of trying to apply the theories appropriate to crystalline semiconductors to amorphous materials. The basic difference is that in an α-Si:H barrier the space charge is not simply due to a uniform ionised impurity concentration, but is largely due to the gap state density distribution. This gap state distribution varies with both distance through the sample and energy, and the result is a non-uniform space-charge distribution. However, bearing this and other complications (such as the frequency dispersion) in mind, it is possible to extrapolate the curves to the voltage axis (whilst maintaining the same curvature as in reverse bias). This yields an

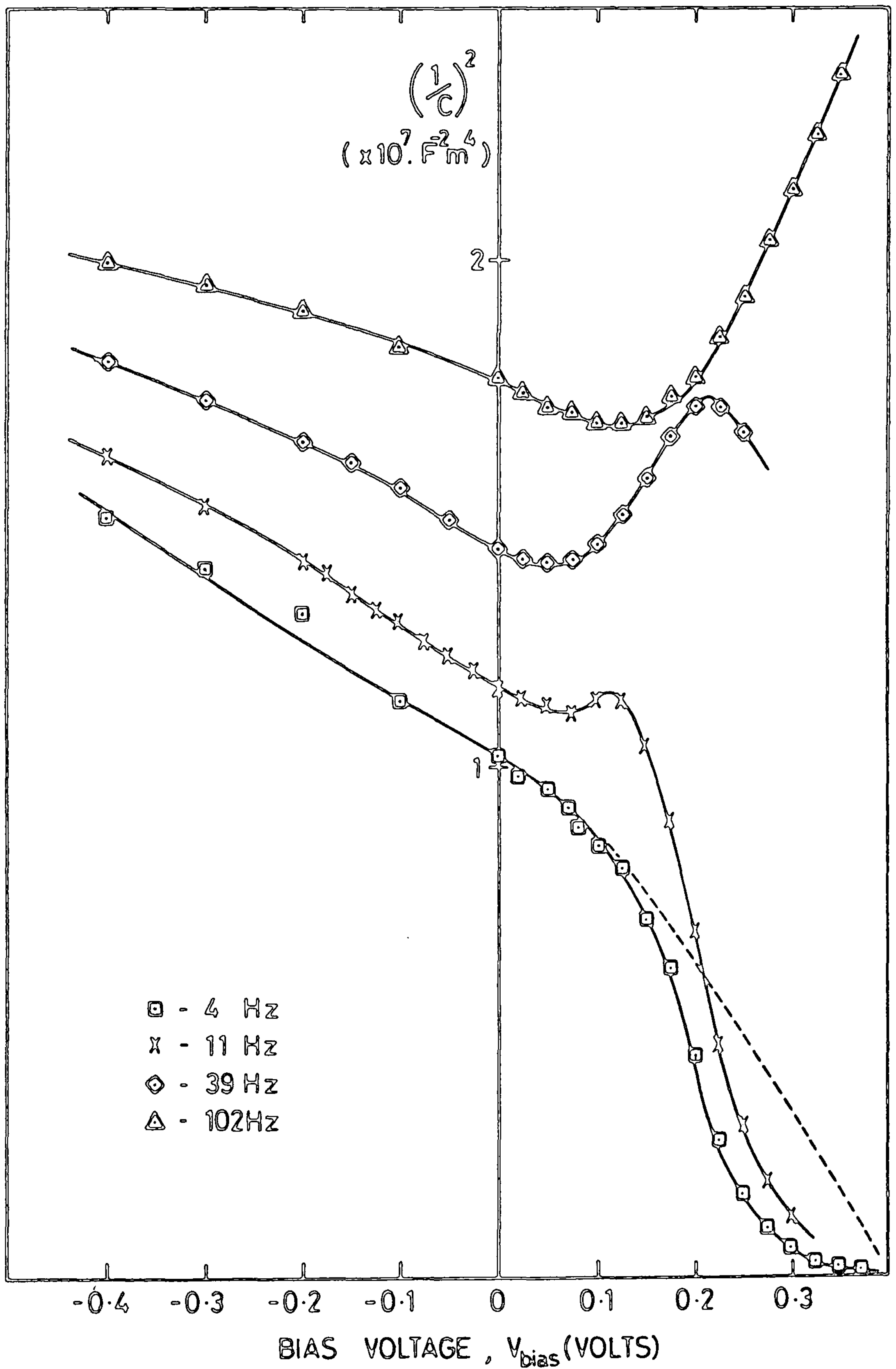


Fig. 7.9 $1/C^2$ v V_{bias} plotted for Device 1 at room temperature in the dark showing the departure from the theory applicable to single crystal Schottky barriers.

approximate value for the diffusion potential[4,27]. From the 4Hz curve in Fig. 7.9 this extrapolation gives $V_o \approx 0.4V$ which compares favourably with the value obtained from the J-V graph in far-forward bias (see Fig.7.1 inset). It should be stressed that this method of obtaining V_o is not reliable, especially for doped samples[27]. The deduction of the ionised impurity density from the slope of these curves is also not meaningful. Nonetheless, it is interesting to note that the figure obtained from our data of $\sim 10^{16}$ cm^{-3} compares well with published results on similar material[4,27,28].

Conductance

Fig. 7.10 shows the conductance-voltage characteristics of the Pd/α-Si:H Schottky barrier. These correspond to the C-V data shown in Fig. 7.6. The curves are rather featureless. In reverse bias the conductance is approximately constant, the absolute magnitude decreasing with frequency. In forward bias a rapid rise in conductance is seen. Very similar curves have been reported by Viktorovitch and Jousse[23].

These data cast some more light on the C-V measurements shown in Fig. 7.6. In particular, they suggest another explanation for the structure seen in the forward C-V characteristics. Using the measurement system described earlier (see section 6.4), a sharp rise in device conductance, as seen here, can cause instrumental effects. The lock in amplifier resolves the signal into its quadrature components ($V \cos\phi$ and $V \sin\phi$), representing the capacitance and conductance. If the conductance becomes much greater than capacitance (or vice versa) then ϕ becomes either very large or very small. Such ϕ values are outside the specifications of the system and large errors in the resolved components can occur. In an attempt to determine the extent of these errors the device was modelled using discrete components i.e. decade resistance and capacitance boxes. While the capacitance was kept constant the resistance was decreased (i.e. conductance increased) and the measured capacitance was monitored. With increasing

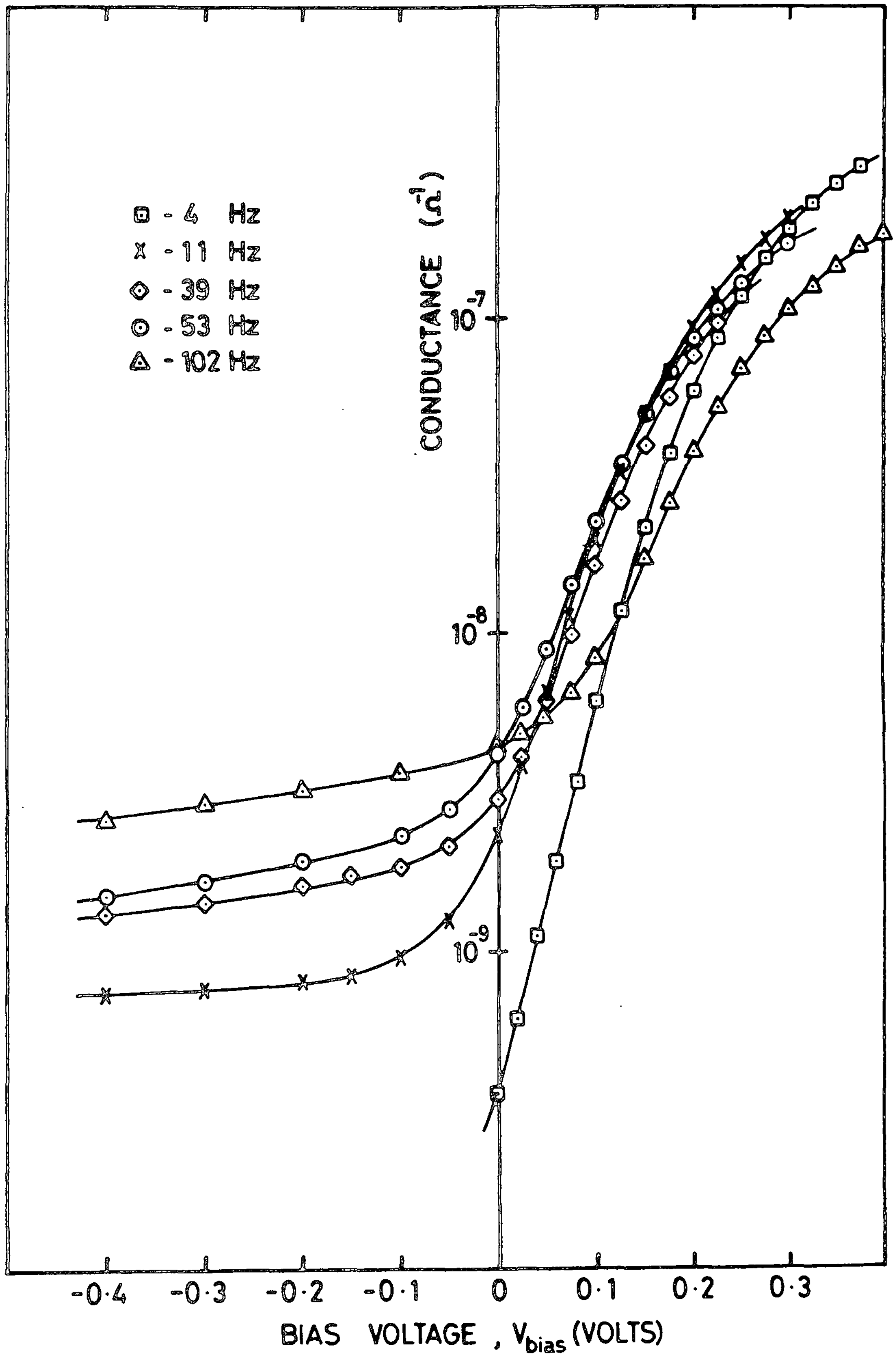


Fig. 7.10 Conductance-bias data corresponding to that shown in Fig. 7.6

conductance the capacitance reading was observed to fall by a small amount: the percentage drop was not sufficient to explain the fall in C recorded for the sample (see Fig. 7.6). Continuing to increase the conductance led eventually to a rapid increase in the measured capacitance as the conductance channel on the phase sensitive detector overloaded. It was found, however, that a judicious choice of scaling factors on the instrument made measurements possible without overloading the system, even with a rapidly increasing conductance. As a result it is thought that the rise in capacitance in forward bias is most probably not an instrumental effect.

The lack of any structure in the G-V curves is also noteworthy. If the sharp rise in the forward-bias capacitance is due to surface states, as proposed by Beichler et al(19), then one might expect to see some peaks in the G-V curves. Their non-appearance could mean one of two things. Firstly, it is possible that the peak is present but is swamped by the effect of series resistance (see chapter 4). Alternatively, either the surface state density is negligible or else their occupation is controlled entirely by the metal Fermi level(23): whichever is the case, the states will not contribute to the measured capacitance.

7.4.3 Diodes made on α-Si:H from Different Sources

In a further attempt to compare α-Si:H from different sources the C-V, G-V characteristics were studied as a function of frequency for diodes made on both Plessey and Xerox α-Si:H (undoped). The results were broadly similar to those obtained on Dundee α-Si:H and show the same general trends. The notable difference was the non-appearance of a peak in the capacitance under forward bias. The C-V characteristics all resembled the low frequency (4Hz) Dundee curve, with the capacitance decreasing slowly in reverse bias and increasing rapidly in forward bias. Higher frequencies led to a flattening of the curve. The lack of any peak would seem to suggest that diodes on Plessey and Xerox α-Si:H had a somewhat lower series resistance than those made on α-Si:H from Dundee, so that

the true barrier response is observed over a wider bias voltage range. This is most probably due simply to an n^+ back contact of lower resistance or perhaps to a more injecting back contact, as discussed in section 7.4.2. In either case it is not surprising that slight differences occur in the quality of the ohmic contacts made to α-Si:H produced by different laboratories, since some variability is encountered between different batches of α-Si:H from the same source[1].

7.5 Results for Etched Semiconductor Substrates

As described in section 6.8 it was found necessary to use a pre-deposition surface treatment to achieve deposition of LB films onto α-Si:H. It is well known that the characteristics of Schottky barriers are critically dependent on the nature of the semiconductor surface immediately prior to the evaporation of the metal contact. From the results of the scanning Auger analysis presented in chapter 6 it has been shown that the use of a chlorine water etch leaves a surface layer whose main constituents are chlorine and oxygen, in some bonded form. It is extremely likely that such a layer would alter the device characteristics from the ideal Schottky barrier case. This is important in view of the fact that the MIS devices to be discussed in the following chapter were prepared by treating the whole α-Si:H substrate, depositing various thicknesses of LB film, and evaporating metal contacts, thus creating MIS devices with insulating layers varying from zero to say, five monolayers thickness. The 'zero layer' devices do not therefore correspond to the Schottky barrier contacts discussed in the previous sections, but rather to diodes which have undergone the standard pre-deposition treatment prior to top contact evaporation. This type of diode will be referred to hereafter as a 'treated' contact. Any modification in device performance caused by the insertion of LB film insulating layers must therefore be considered relative to the performance of 'treated'

contacts and not straightforward Schottky contacts. In view of this some experiments were performed in order to investigate the properties of 'treated' MS contacts.

An α-Si:H sample (Dundee) was prepared in the usual manner except that only half of the sample was etched in chlorine water. Following this, the sample was mounted in an evaporator as quickly as possible for top electrode deposition (gold, in this case). The dark current-voltage characteristics on both the 'etched' and 'unetched' regions were measured. Data for a contact from both of these regions are shown in Fig. 7.11. Clearly, the diode behaviour has been adversely affected by the etching. For the treated contact the forward current has fallen, and the reverse current has increased by three orders of magnitude. Although there was quite a high degree of variability between different contacts, measurements made on six different devices in each region indicated that the diode rectification ratio was, in general, decreased by the chlorine-water etch. It must, however, be pointed out that under ideal circumstances a study involving many different α-Si:H substrates and much larger numbers of contacts would have been undertaken, to ensure the reliability of these results. Unfortunately, time did not permit this.

The reduction in the forward current, I_F, as a result of the chlorine-water etch may be very easily explained in terms of the introduction of an interfacial layer by the etch procedure. Such a layer can reduce the majority carrier current[29], but if this was the case a corresponding drop in the reverse current would be seen. The large increase in I_R, which has been observed accompanying the decreased I_F value, suggests that there is a change in the barrier height taking place. Charge in the interfacial layer could be responsible for this, according to Fonash[30], by causing a change in the effective metal workfunction. A lowering of the barrier height, which would be necessary to explain the data in Fig. 7.11, would require a net positive charge in the interfacial layer. This is

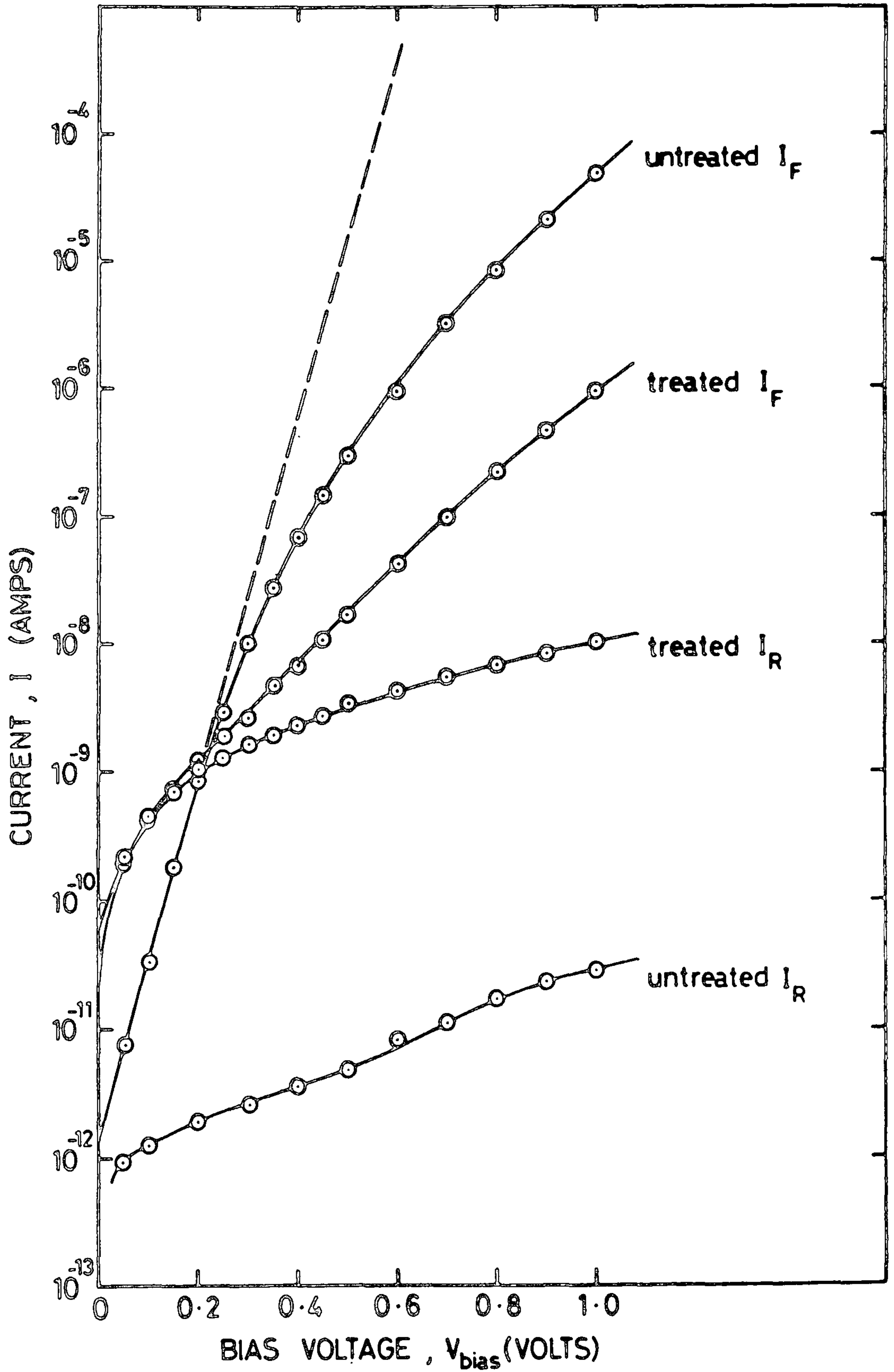


Fig. 7.11 Forward and reverse current-voltage characteristics for 'treated' and 'untreated' Au Schottky contacts measured in the dark at room temperature.

possible, although with the presence of chlorine in the layer one might intuitively expect a negative charge (Cl^-). An alternative explanation for the reduction in the barrier height would be that the formation of the interfacial layer introduces interface states. Charge stored in interface states can reduce the band-bending in the semiconductor and hence affect the barrier height[22]. In the author's opinion this explanation is the most probable of the two.

7.6 Summary and Conclusions

Schottky diodes have been fabricated on Dundee α-Si:H (undoped) using gold and palladium metal contacts. The following points can be made

(a) J-V measurements on these diodes correspond very well with other published data, with comparable ideality factors and rectification ratios.

(b) C-V and G-V measurements also concur reasonably well with the results of other workers, and the characteristics have been explained using a simple equivalent circuit.

(c) The properties of Schottky diodes on substrates which had been etched and prepared for LB film deposition have also been investigated. The rectification ratio was found to be substantially reduced compared with untreated diodes. This was attributed to a change in the barrier height ϕ_B.

It has, thus, been demonstrated that 'state-of-the-art' Schottky diodes have been made on Dundee α-Si:H. It has also been shown that the preparation procedures for LB film deposition leads to a significant degradation in diode characteristics, and this should be born in mind when considering the MIS results presented in the next chapter.

Diodes were also made on α-Si:H samples prepared by Plessey Research (Caswell) Ltd. and the Xerox Corp. Although the J-V characteristics were similar to those of Dundee α-Si:H devices, the C-V curves were slightly different. This was attributed to a difference in the properties of the ohmic contact.

CHAPTER 8

THIN INSULATOR MIS RESULTS

8.1 Introduction

In this chapter the results obtained for 'thin' insulator MIS devices are presented. The definition of a 'thin' insulator MIS device is, as previously stated, one which incorporates an insulating layer of tunnellable dimensions i.e. < 50Å. The main aim of this work was to investigate the effect of the insulating layer thickness on the device characteristics, using built-up monolayers of Langmuir-Blodgett films. In section 8.2 the choice of a particular LB film material is discussed, and the procedures adopted for securing representative, repeatable data are outlined. Capacitance measurements are reported in the following section, and in section 8.4. current-voltage data are presented and discussed. The effects of light on the capacitance-voltage and conductance-voltage data are dealt with in section 8.6. The final experimental section is concerned with one of the applications of tunnelling MIS diodes, namely solar cells. The introduction of LB films of different thicknesses into these devices gives rise to changes in the solar cell parameters (open-circuit voltage, short-circuit current etc) : these effects are discussed. The chapter closes with a short summary.

8.2 Practical Details

8.2.1 LB Film Materials

The fabrication of MIS devices incorporating only a few Langmuir-Blodgett monolayers was found to be extremely difficult. The deposition of cadmium stearate films onto α-Si:H presented few problems, providing the usual surface pre-treatment described in section 6.8.2 was carried out. However, films consisting of 1-5 layers of Cd Stearate were destroyed by placing the sample under high vacuum, which was necessary for the evaporation of top contacts. This 'stripping' of the film is indicative of a relatively

poor LB film-substrate adhesion. It has not been observed when using LB films on other semiconductor substrates. There are two possible approaches which could lead to an improvement in the situation: (a) the use of a different LB film material which may have better adhesion properties, (b) the use of an alternative surface treatment for the α-Si:H substrates. Because of the availability of a number of new LB film molecules it was felt that approach (a) would be less time consuming than a systematic search for another pre-deposition surface treatment. Diacetylene has already been successfully deposited onto single crystal semiconductors by the Durham group using the Langmuir-Blodgett technique[1,2]. The 12-8 diacetylene and stearic acid molecules both have similar end groups i.e. the carboxyl acid group at the hydrophilic end. This implies that if stearic acid can be deposited onto α-Si:H then diacetylene should also deposit under similar conditions. Of course, the similarity in end groups also means that one would expect to find comparable film-substrate adhesive forces. However, the major advantage in using diacetylene lies in its polymerisability following deposition. Under ultra-violet illumination, double and triple bond cross links form between the molecules in the film[3] (see also chapter 5). This cross linking is likely to result in a more structurally stable film which, it was thought, might be more resistant to stripping under high vacuum. This was discovered to be true : diacetylene films survived the top electrode deposition process, providing care was taken. The results presented in the remainder of this chapter will therefore deal with metal/diacetylene-polymer/α-Si:H (MIS) devices.

It is interesting to note that the deposition of diacetylene onto α-Si:H did not follow the usual pattern i.e. pick-up on both entry and exit from the water subphase (Y-type deposition). For the samples used in this investigation, pick-up was only observed on the way out of the subphase. This is known as Z-type deposition, although it is rarely seen in practice. Indeed, if a substrate has different 'front' and 'back' surfaces it can

sometimes appear to show Z-deposition, e.g. on entry into the subphase, if the front picks up a film but the back returns its film to the water there is a zero area charge. However, careful experimentation showed that for both thin (1-5 monolayers) and thick films of diacetylene on α-Si:H the deposition was truly Z-type.

8.2.2 Device Reproducibility

The properties of Schottky barrier and tunnelling MIS devices are critically dependent on the exact nature of the semiconductor surface. Hence, in any study of these devices the repeatability of results is of paramount importance, since the characteristics can be quite different, even for devices fabricated under ostensibly identical conditions. The size of samples used in this study permitted the fabrication of over 150 devices on a single substrate. The LB film was deposited in a stepped thickness structure (e.g. 0, 1, 2, 3, 4 layers), giving approximately 30-40 contacts for each particular film thickness. Wherever possible, results were taken as an average over a number of contacts. When the type of data required precluded this approach, a number of devices were tested, and results were taken on a representative contact i.e. 'typical results'. Discrepancies in device behaviour can occur not only because of regional variations or imperfections in either the substrate or the LB film, but also because of variations in the contact area. Given the use of thermal evaporation and contact masking procedures an experimental spread in contact area of ± 10% would not be unreasonable.

8.3 Capacitance Measurements

Capacitance measurements are an effective first step in the assessment of the quality of an LB film. Usually metal-insulator-metal (MIM) structures are used for these investigations. The capacitance should fall in inverse proportion to the number of deposited monolayers, if each monolayer

is of a reproducible thickness. We recall that

$$\frac{1}{C} = \frac{d_{LBF}}{\varepsilon_o\ \varepsilon_{LBF}} N + \frac{d_{ox}}{\varepsilon_o \varepsilon_{ox}} \qquad (5.2)$$

where C is the capacitance per unit area, d_{LBF} is the thickness of the monolayer, ε_{LBF} its relative permittivity and N, the number of monolayers. In general, some natural 'oxide' layer will exist under the LB film : its thickness is d_{ox} and its dielectric constant is ε_{ox}.

In view of the difficulty experienced in fabricating these α-Si:H MIS devices incorporating LB films, it was important to be able to test the film quality 'in situ' i.e. in the device. Now, when films are deposited onto a semiconducting substrate (i.e. an MIS device) one must consider the added complication of the capacitance associated with the space charge layer in the semiconductor. This will give rise to another capacitance in series with both the 'oxide' and the LB film capacitance. The effect of this contribution can be ignored however, if the MIS device can be accumulated (see section 4.2). In this regime the measured capacitance should approach the insulator capacitance. This enables a true measurement of the insulating film properties to be made, even on a semiconducting substrate.

8.3.1 Capacitance-Voltage Data

In order to determine whether an MIS device can be accumulated one can measure the capacitance-voltage characteristics. Fig. 8.1 shows a typical set of C-V curves for Dundee α-Si:H MIS diodes incorporating 12-8 diacetylene polymer films ranging from zero to four monolayers thickness. The gold top contact was ∿ 100 Å thick and 0.5 mm in diameter. All of the measurements were taken at room temperature and pressure, in the dark,

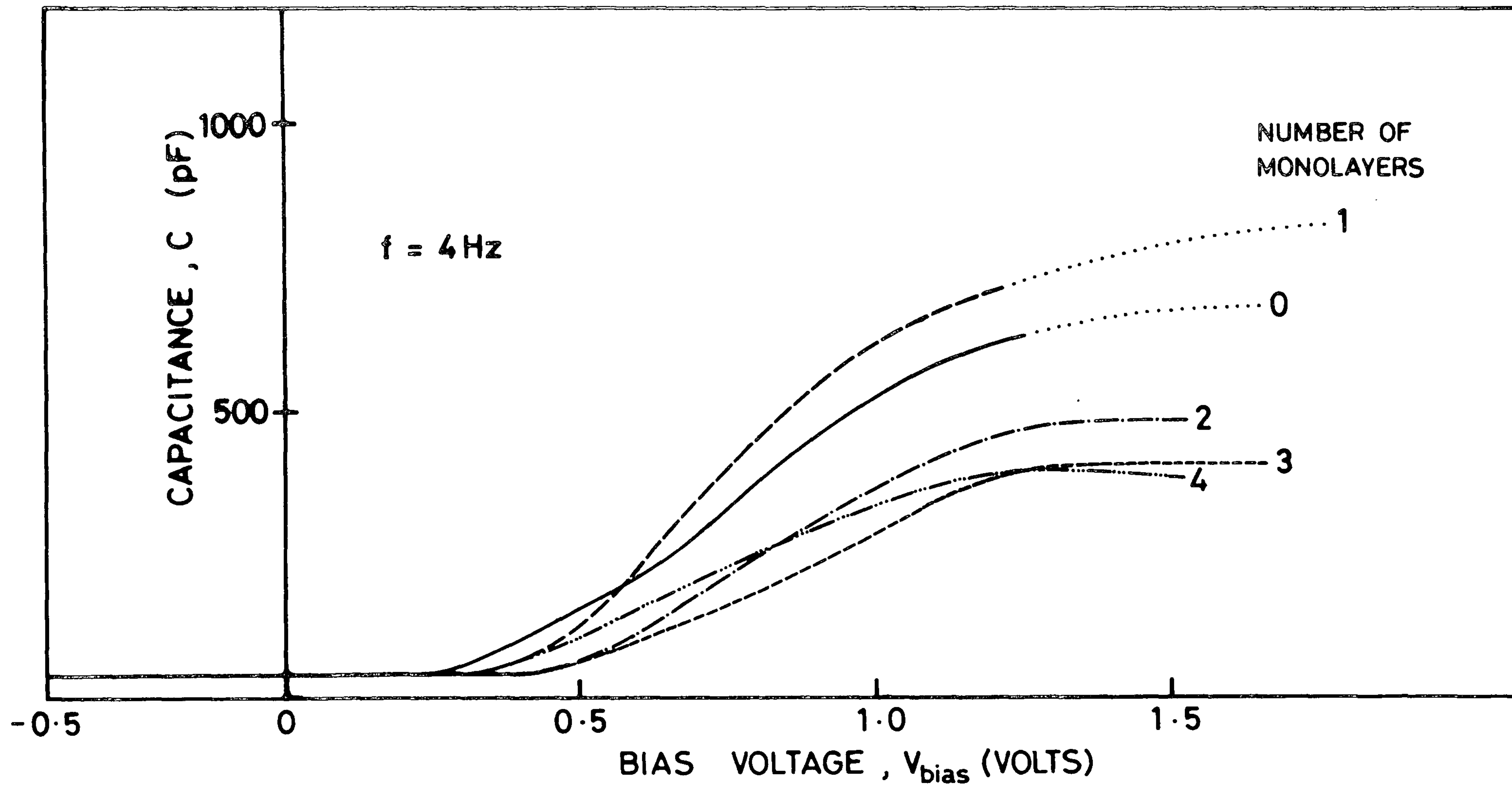


Fig. 8.1 Typical C-V characteristics for devices incorporating different numbers of LB film monolayers. Measurements taken in the dark. The bias was scanned from negative to positive at 10 mV sec^{-1}.

using a 4Hz measuring signal. The bias voltage was scanned (using a ramp generator) from negative bias to positive bias at a rate of 10 mV sec^{-1}. The devices showed some hysteresis which has been omitted from the diagrams for the sake of clarity. The observed hysteresis was never greater than 0.1V. Hysteresis effects on this scale are commonly observed in MIS devices. They may arise because of mobile ions in the insulator, the response of deep lying gap states, or even because of instrumental (response time) effects. Care was taken to ensure that results were always taken on the same branch of the hysteresis curve. This allowed valid comparisons to be made between different insulator thicknesses whilst neglecting the hysteresis.

The zero layer curve displays a constant capacitance in reverse bias. This implies the existence of an inversion layer, such as is seen in thicker insulator (non-tunnelling) MIS structures. For a normal Schottky barrier the capacitance should decrease with increasing reverse bias, as the depletion width reduces. In forward bias it is interesting to note the rise in capacitance is followed by a levelling off. This tendency of the forward bias C-V curve to flatten out is indicative of the formation of an accumulation layer. In an ideal Schottky diode this cannot happen, since any excess majority carriers which begin to accumulate at the semiconductor surface will simply move into the metal. If, however, an interfacial layer is present between the metal and the semiconductor, it can impede the removal of the excess carriers, providing it is of sufficient thickness (a few tens of angstroms). In this case an accumulation layer can be formed. Hence the data in Fig. 8.1 suggest that the 'zero layer' devices do incorporate a natural oxide layer. It is not surprising that this should be so, since the whole sample was etched in the standard pre-LB film deposition manner. This process is expected to leave some sort of interfacial 'oxide' layer of an unknown thickness.

The devices incorporating LB films exhibit the same general C-V trends as have already been described, clearly showing an accumulation region

in forward bias. In this region the capacitance should approach that of the insulating layer. Comparing experimental values of the accumulation capacitance, C_{accum}, with the calculated geometrical capacitance of the LB film reveals that for the 3 and 4 layer devices there is good agreement, within experimental error ($\pm$ 10%). However, as the number of monolayers decreases the discrepancy becomes larger e.g. for the 1 layer device C_{accum} is less than 70% of the expected value. Such differences cannot be attributed to experimental error. The most likely explanation of this trend is that the post-etch interfacial layer extends over the whole sample, and is thus in series with the LB film. The capacitance of this interfacial layer will influence the total insulator capacitance most at low LB film thicknesses, where the LB film capacitance is highest. Depending on the relative magnitudes of these capacitances, the total insulator capacitance could fall short of the LB film capacitance.

8.3.2 Reciprocal Capacitance v LB Film Thickness

The accumulation capacitance of many different devices on the same sample, whose typical C-V curves were shown in Fig. 8.1, were measured. Capacitance data, averaged over ten contacts for each LB film thickness region, are plotted in the form of a $^1/_C$ against N graph, where N is the number of monolayers, in Fig. 8.2. As before, these data were measured at room temperature and pressure, using a 4Hz measuring frequency. A bias of +1V was applied to the devices to ensure accumulation. For the particular data shown the sample was illuminated with normal room lighting. Because of the large photoconductive effect in α-Si:H such a diode under illumination is more like an MIM structure. Illumination did not change the absolute magnitude of the accumulation capacitance, although it was found to affect the C-V curve (see section 8.5.1). Measurements taken on accumulated devices in the dark produced identical results.

The $^1/_C$ - N plot is a good straight line, showing the same general trend in C_{accum} as that observed in the C-V curves (Fig. 7.14). The error bars

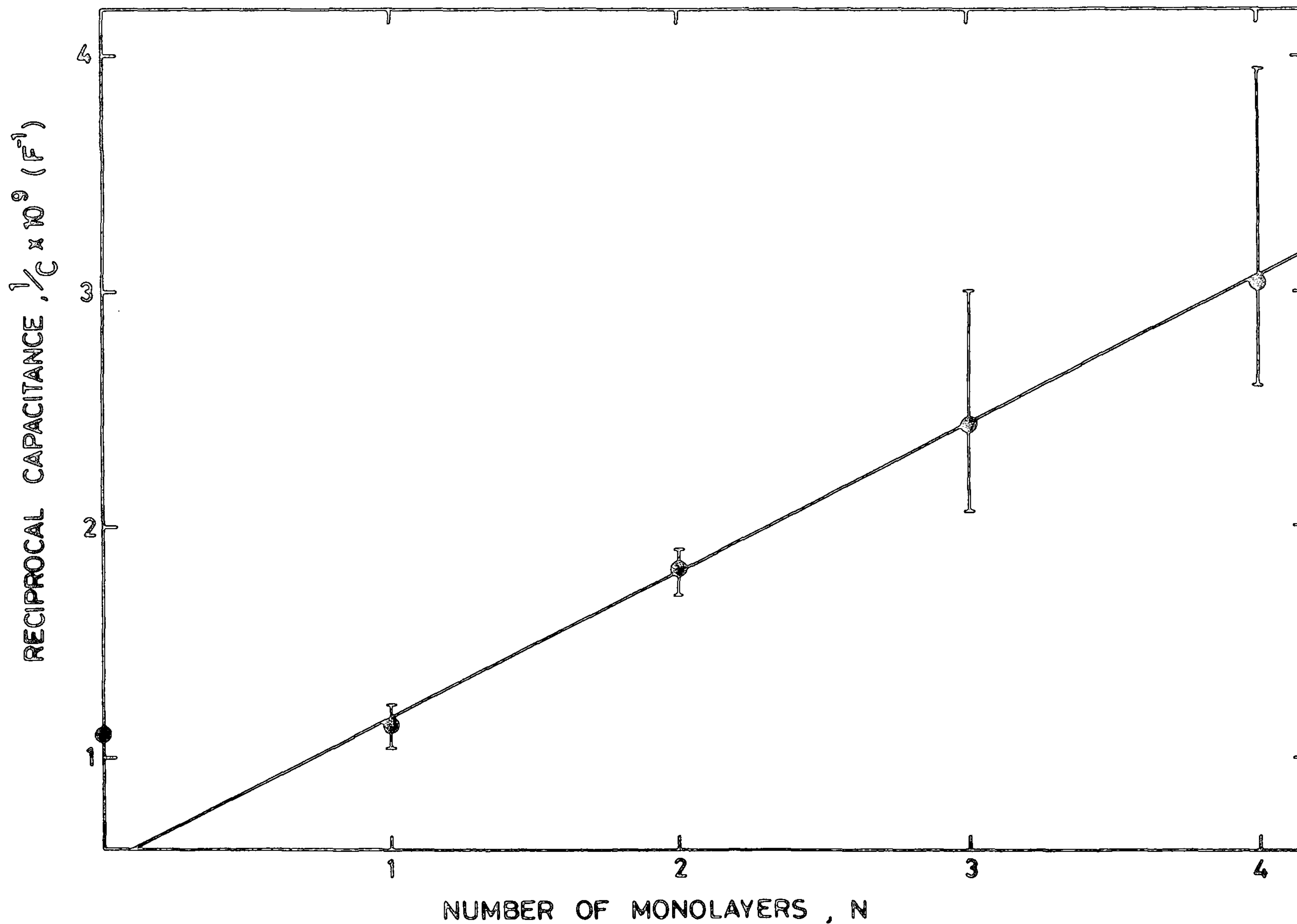


Fig. 8.2 Reciprocal capacitance v no. of monolayers for devices in accumulation under white light illumination. Error bars show the spread in measured capacitance over ten different contacts.

shown indicate the spread in measured capacitance over 10 contacts. Using equation 5.2 the slope of the line yields the dielectric thickness of the monolayers; thus $d_{LBF}/\varepsilon_{LBF}$ = 1.1 nm. This value compares favourably with that of 1.3 reported by Kan et al[1] for diacetylene polymer in an MIM structure. Assuming ε_{LBF} to be $\sim$ 2.5 this gives a molecular length of $\sim$ 28 Å which is not unreasonable. From the intercept of the line the dielectric thickness of the 'oxide' layer can be found. In this case $\frac{d_{ex}}{\varepsilon_{ox}}$ = 94 nm. To estimate the thickness of this layer one would need to know ε_{ox}, which in turn requires a knowledge of the exact composition of the layer. This is difficult, but as a guide, if we assumed the layer to be composed of SiO_2, ε_{ox} would be 4.0 : the corresponding thickness is $\sim$ 40 Å. Whatever the exact composition of the 'oxide' layer the relative permittivity would not be expected to vary greatly from this value (certainly not by orders of magnitude). Hence, it seems likely that we are dealing with an 'oxide' layer which is several tens of angstroms thick, as postulated earlier.

The discrepancy between the measured capacitance and the LB film capacitance at low N values is clearly shown in Fig. 8.2. In particular we note the fact that the values of $1/C$ are almost identical for the zero and one layer devices (see also Fig. 8.1). The differences in the values for the zero and the one layer devices are well within the limit of experimental error. There are two possible explanations for this phenomenon. Firstly, it could be that the 1 layer LB film is of such poor quality i.e. has a high density of pinholes and imperfections, that it is effectively shorted out, and so has only a marginal effect on the device capacitance. Successive monolayers may fill the pinholes, thus preventing shorting and producing the expected capacitance. With an increasing number of monolayers the devices would more closely approach the ideal case. An alternative, and in the author's opinion more probable explanation, is that the single monolayer has been stripped off the substrate during top contact evaporation, but

that the thicker layers have been left intact. This would mean that the one layer devices did not, in fact, incorporate any LB film, but simply the natural post-etch 'oxide' layer. Thus, one would expect the same accumulation capacitance for both the zero layer and one layer devices, as indeed is the case. If this explanation is applicable the points on Fig. 8.2. for N = 0 and N = 1 should in fact be the same point. The fact that it lies on the line at N = 1 is not surprising if we consider that the thickness and relative permittivity of this natural 'oxide' layer are comparable with that of a monolayer of diacetylene.

8.4 Current-Voltage Measurements

The effect of LB film thickness on the forward bias I-V characteristics of diodes made on Dundee α-Si:H is shown in Fig. 8.3. These data are for the same set of devices as was used in the previous section. Diodes on this sample incorporated LB films ranging in thickness from zero to four monolayers. Measurements were made in the dark, at room temperature, with the specimen under a low pressure of dry nitrogen (continuous flow). This atmosphere ensures the reproducibility of current-voltage curves, since the effects of water vapour are avoided. For each film thickness the forward and reverse currents at a bias of 0.5V were measured for 5 to 10 different contacts. A representative contact was then chosen on the basis of these results, and its full I-V characteristic was recorded. Thus the data shown in Fig. 8.3 are typical.

8.4.1 Forward Bias

It is worth re-emphasising that the zero-layer device is not a true Schottky barrier because of the pre-deposition etch 'oxide' layer. The characteristics of this type of device were described earlier, in section 7.5. The curve shown in Fig. 8.3 follows the standard diode equation $J = J_o \exp\left(\frac{eV}{nkT}\right)$ over the very small bias range from 0.1 - 0.2 volts. The ideality factor measured from this region is $\sim$ 1.66. This high value of n is consistent with the presence of an interfacial layer. The barrier

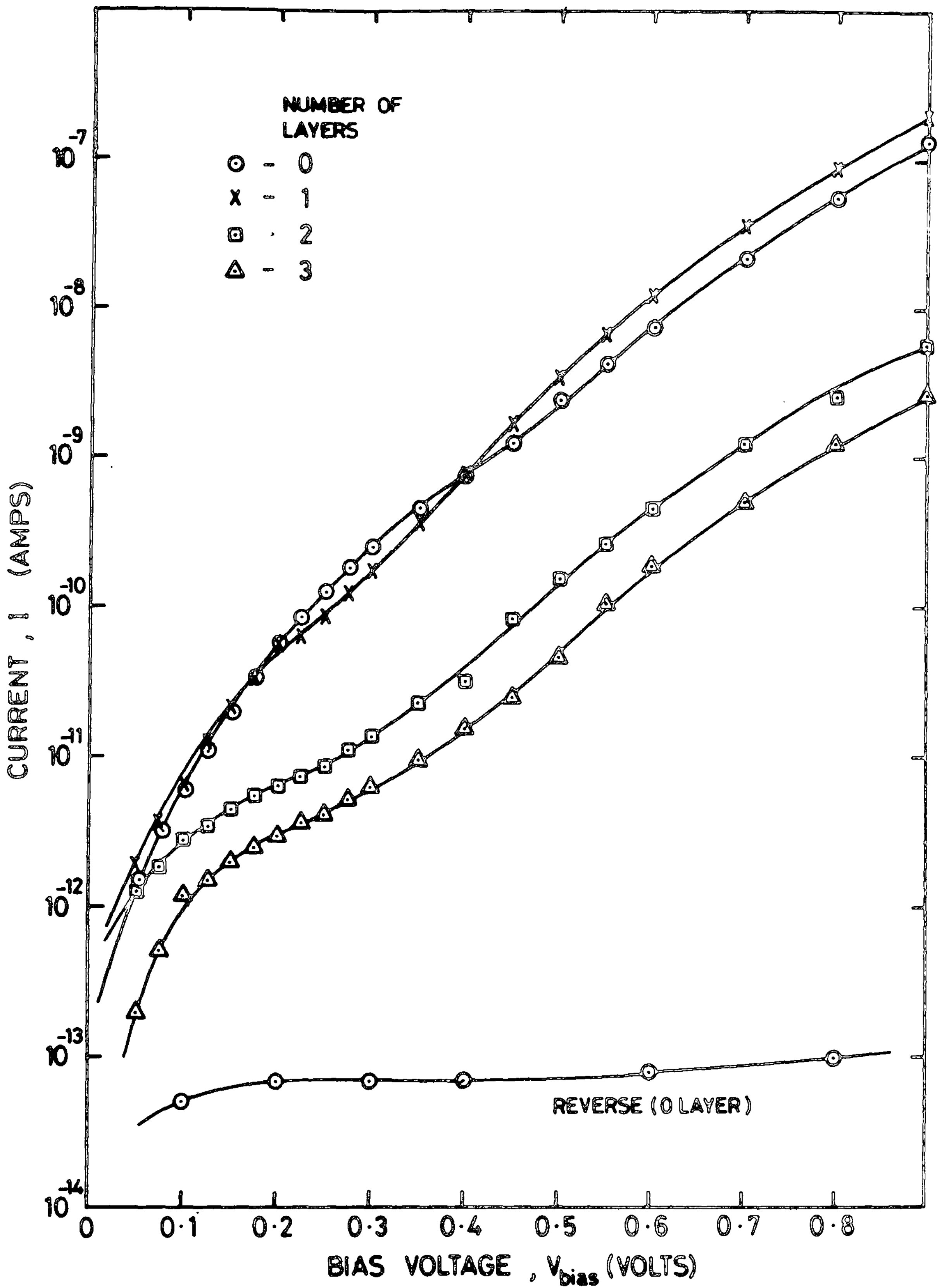


Fig. 8.3 Typical forward current-voltage characteristics for MIS devices with different thickness insulators. Readings taken in the dark under a low pressure of dry nitrogen. A typical reverse characteristic for a zero layer device is also shown for comparison.

height calculated from the extrapolated J_o value using thermionic emission theory is about 0.99 eV. It should be remembered, however, that this calculation is strictly not applicable with such a non-ideal diode. At higher bias voltages the diode displays increasingly non-ideal behaviour.

The general trends discussed in conjunction with the capacitance data are mirrored in the forward bias I-V data of Fig. 8.3. There is a marked similarity between the curves for the zero and one-layer devices, corresponding to their very similar capacitance reported earlier. Within the limits of experimental error it is not possible to distinguish between these two curves. The small variations may well be due to changes in contact area, or to slight differences in surface properties. This seems to further support the suggestion that the single monolayer was stripped during top contact deposition. Without doubt the first monolayer, if present, has no effect on either the current flowing in the device or its capacitance. For the device incorporating two layers of diacetylene polymer the current fell by almost two orders of magnitude (for bias voltage > 0.3V), which is the expected effect. The inclusion of a third layer led to a further fall in current by a factor of two. Interestingly, the curves for 3 layers and for 4 layers (not shown) were rather similar. In general though, it can be said that the forward current was reduced by the insertion of the LB film, while the shape of the curves remained the same.

8.4.2 Reverse Bias

For all devices measured, the reverse currents were of the order of 10^{-13} Amps: no change was observed with film thickness. The reverse current-voltage characteristic of the zero layer device is shown in Fig. 8.3. A slight increase in the current was observed with increasing

reverse bias. Unfortunately, the small magnitude of these reverse currents and the consequent measurement difficulties precludes any analysis of these data.

8.4.3 Possible Mechanisms to Explain Forward Bias I-V Curves

It is clear from the curves shown in Fig. 8.3 that a full explanation of their shape is rather more complex than for an ideal Schottky diode. For instance, the 'double hump' structure, which is evident in all the curves, could imply that there are two different current mechanisms in operation, each of which dominates over a particular bias range. The effects of introducing the LB film layers must also be explained. Similar results have been reported by other researchers, notably Tredgold et al[4,5] and Batey et al[6] working on the GaP/LB film system, and Kar and Dahlke who used Si-SiO_2-metal structures[7]. Various interpretations of such curves have been proposed, and these will now be discussed.

(a) Thermionic Emission Model

This approach involves the basic assumption that the diodes are behaving as modified 'ideal' Schottky barriers. It should really only be used in situations where the departure from ideality is small, however, its application in our case is instructive. The appropriate equation describing these modified J-V characteristics is

$$J_{dark} = A^{*}T^{2} \exp\left(-\chi^{\frac{1}{2}}\delta\right) \exp\left(\frac{eV}{nkT}\right) \qquad (3.44)$$

As described in chapter 3, the J-V curve may be affected in a number of ways, notably through a change in the tunnelling probability factor ($\exp(-\chi^{\frac{1}{2}}\delta)$), or through a change in the n-value, or through charge stored in the insulator.

Considering the curves in Fig. 8.3 in the bias range $V_{bias} > 0.4V$, we observe the expected decrease in current with increasing LB film thickness. Approximating these curves to a straight line, it is clear that the

n-value is roughly the same in all cases. Hence, this is not the mechanism responsible for current control. The other two mechanisms mentioned above are possibilities.

(i) Change in the Tunnelling Probability

In an ideal Schottky diode, once the carriers have surmounted the barrier they are free to enter the metal contact. In the presence of an interfacial insulating layer the carriers must overcome the barrier and then tunnel through this layer, and as a result the current magnitude should fall. Since n is approximately the same for all the curves in the bias region under consideration, the difference in current magnitudes between the devices may be used to calculate $(\chi^{\frac{1}{2}}\delta)$. The figures obtained are 2.8 and 3.7 for the 2-layer and 3-layer devices respectively. Roberts et al[8] found a very similar value of $(\chi^{\frac{1}{2}}\delta) = 2.2$ for an MIS device on CdTe incorporating 2 layers of C-4 anthracene LB film. The dependence of this term on the insulating layer thickness for Si/SiO_2 MIS devices has been investigated quite extensively by Card[9]. Although thicknesses comparable with our data were not used, an extrapolation of his data predicts a $(\chi^{\frac{1}{2}}\delta)$ term much larger than was observed here. By substituting in the appropriate value of δ, the mean barrier height (in electron volts) presented by the interfacial layer can be calculated. Assuming the molecular length of 12-8 diacetylene to be 30 Å gives $\chi = 2.2 \times 10^{-3}$ eV for the 2-layer device, and $\chi = 1.7 \times 10^{-3}$ eV for the 3-layer device. We note, along with Roberts et al[8], that this is substantially less than the χ-values reported by Card[9], albeit for a different semiconductor/insulator combination.

(ii) Incorporation of Fixed Charge in the Insulator

The presence of fixed charge in the insulator leads to a genuine change in the barrier height of a diode. This effect is simply a reflection of the change in metal work function which the charge causes. The effective metal

work function is given by[10]

$$\phi_M' = \phi_M - \left(\frac{Q_{fix} \; \delta_{eff}}{\varepsilon_i \varepsilon_o} \right) \qquad (3.45)$$

Rearranging this equation gives

$$Q_{fix} = \frac{\varepsilon_i \; \varepsilon_o}{\delta_{eff}} \; (\phi_M - \phi_M')$$

Now $(\phi_M - \phi_M')$ is the change in metal work function. By extrapolating the I-V curves in Fig. 7.16 to V = 0 we can find J_o and hence ϕ_B (assuming $A^* = 100$ A cm^{-2} K^{-1}). The difference in ϕ_B values between the devices shown is equal to $(\phi_M - \phi_M')$, and this factor can thus be experimentally determined. Using the above equation the amount of charge necessary to explain the data shown in Figure 7.16 may be estimated. Assuming $\varepsilon_i = 2.5$ and δ_{eff} = (LB film thickness + 'oxide' thickness), where the LB film thickness is 30 Å per monolayer and the 'oxide' thickness is ∿ 40 Å, the fixed charge density is found to be 1.03×10^{11} cm^{-2} for both the 2-layer and the 3-layer devices. Again, this compares well with the figure of 4×10^{11} cm^{-2} reported by Roberts et al[8] for the CdTe/C-4 anthracene MIS system. The sign of the fixed charge also agrees with the work of these authors[8] : the increasing barrier height as the number of monolayers rises means that the charge is negative. Although this charge may be within the diacetylene polymer layer i.e. a property of the LB film, it is also possible that the pre-deposition etch may be responsible, since it is known to leave chlorine on the α-Si: H surface, some of which may exist in its ionic form (Cl^-).

The shape of the I-V curves at low bias voltages (<0.4V) for devices incorporating LB films cannot be explained in terms of a thermionic emission model. It would seem that there is an excess current, over and above the thermionic-emission current. Hence, another model must be used.

(b) The 'Pinhole' Model

This model has been suggested by some authors[4,5] to explain their results in the low bias region. The argument used is that pinholes exist in the LB film, and at low bias voltages the leakage current through these pinholes is considerably greater than the other current components (e.g. the thermionic emission current). As the bias voltage is increased the 'pinhole' current component saturates, whereas the other components continue to increase and eventually become dominant. The shape of J-V curves would thus be very similar to those seen in Fig. 8.3. The magnitude of the current should also reduce with increasing LB film thickness, as the pinhole paths are reduced. At first sight this might seem like a reasonable explanation of the data shown. However, the bias voltage at which the 'pinhole' current component saturates should decrease with increasing number of monolayers. Careful examination of the data reveals that this is not the case, and it is thus thought that this model is not applicable.

(c) Surface State Model

The effect of surface states (or interface states) must also be considered as a possible cause of the complex shape of the forward ln I-V curves. This can occur in two ways.

(1) If a distribution of surface states exist in the bandgap, either at the LB film/'oxide' interface or at the 'oxide'/α-Si:H interface, then these states can be emptied or filled by the movement of the Fermi level as a bias voltage is applied. The change of occupancy of such states means that the ratio of the voltage dropped across the insulator to the voltage dropped across the semiconductor is changed from the ideal case. Moreover, the amount of deviation from ideality is dependent on the surface state density at the Fermi level : since E_F moves through the bandgap at the surface with applied bias, the deviation from ideality is bias dependent. Hence, the ln I-V characteristic may be non-ideal, with a very 'bumpy' shape.

(2) According to Kar and Dahlke[7], the presence of surface states can lead to the observation of an excess current, such as was noted earlier in Fig. 8.3. Indeed, some of their I-V curves for Si/SiO_2/metal diodes exhibit humps, due to these excess currents, which are very similar to the data presented here. The excess current arises because of majority carriers from the semiconductor which surmount the barrier (due to the band bending) and move to the surface states via a generation-recombination mechanism. They then tunnel through the insulator to the metal. The magnitude of this current component depends on the surface state density and the time taken to tunnel through the insulating layer.

The origin of a hump in the I-V curve may be understood as follows. Suppose a distribution of surface states exists over a small range of energy within the bandgap, and that the distribution is sharply peaked. Whilst the states are above E_F they are empty, and make no contribution to the current. As the bias is increased the Fermi level begins to move upward through the states, and they start to contribute to the current. The excess current reaches a maximum as E_F scans through the peak in the distribution, and when all of the states are below E_F i.e. they all respond, the excess current saturates. Obviously, in the case of a real surface state distribution, which may exhibit several peaks, there would be an equivalent number of humps in the I-V curve (providing the surface state excess current component was not negligible compared with the other current components).

The data shown in Fig. 8.3 could well be explained in terms of this model. Kar and Dahlke reported surface state excess currents (maximum) of about 10^{-5} A with a 28 Å oxide layer : this corresponds to a maximum in the surface state density of 6.8 x 10^{12} cm^{-2}. Densities of surface states of the order of 10^{13} cm^{-2} have been reported on α-Si:H [(11)]. Although the interface resulting from etching α-Si:H in chlorine water has not been characterised in this way, comparable densities of states can be expected, and hence quite large excess currents could result. It is thus quite reasonable to interpret the two humps in the current-voltage curves of Fig. 8.3 in terms of two peaks in the surface state density distribution.

8.4.4. <u>Summary</u>

The discussion of the J-V data may be summarised as follows:

(a) <u>The shape of the zero layer curve</u>

(1) for V < 0.2V the current follows the modified Schottky barrier equation with n = 1.66 and ϕ_B = 0.99 eV. This confirms the presence of an interfacial layer.

(2) For 0.2 < V < 0.4 volts an 'excess' current is observed, which cannot be explained by using the thermionic-emission model. This current

may be due to pinholes in the LB film or to a peak in the interface state distribution.

(3) For $V > 0.4$ volts the J-V curve exhibits another hump. This may be interpreted in terms of the modified (very non-ideal) Schottky barrier equation, perhaps with series resistance effects, or attributed to another peak in the interface state density.

(b) The effects of the LB film

In general, (except for the 1-layer case) the current magnitude is reduced with increasing LB film thickness. This may be explained as

1. a decrease in the probability of carriers tunnelling through the film, or
2. the effect of a negative fixed charge density, which effectively changes the metal work function by an amount which is dependent on the insulator thickness.

The variation in current with thickness at low bias voltages seems to discount the pinhole model of conduction.

8.5 Light Induced Effects

8.5.1 Capacitance-Voltage Data

The effect of white light illumination on the C-V characteristic of an MIS device is illustrated by comparing the two curves shown in Fig. 8.4 Both plots are for the same device, incorporating 1 monolayer of diacetylene polymer. The dark C-V data of this device were shown earlier in Fig. 8.1. The illuminated data were taken at room temperature, with an illumination intensity of about 5×10^{-4} W cm^{-2} (room lighting). The measuring frequency was 4 Hz in both cases.

The illuminated C-V curve is largely unchanged in shape compared with the dark curve, but it is shifted towards more negative bias voltages. The magnitude of this shift is approximately 0.5 V. This effect is most probably due to the presence of trapped charge somewhere in the system. The direction of the shift implies that the charge must be positive. This trapped charge

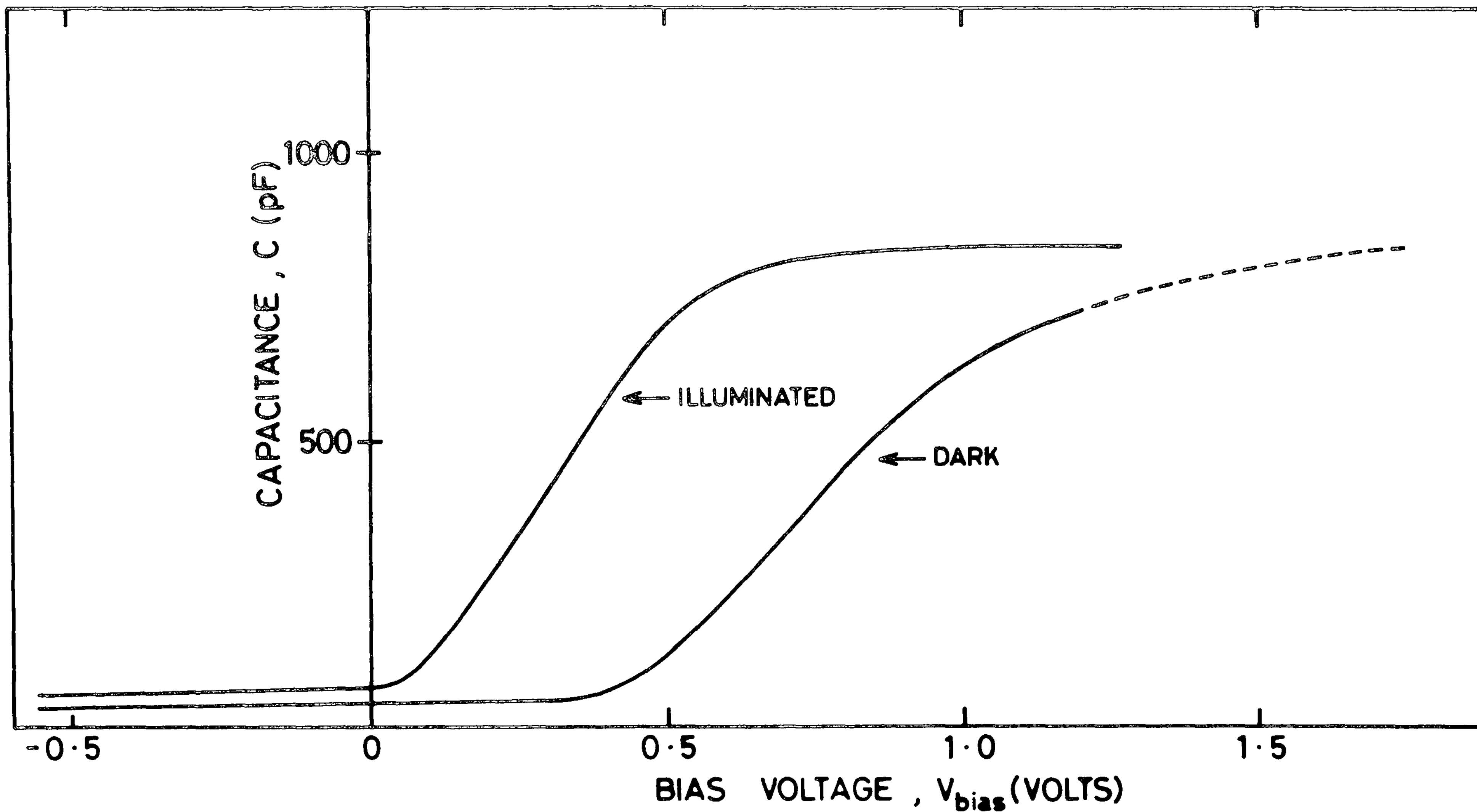


Fig. 8.4 Capacitance-voltage characteristics of an α-Si:H MIS device incorporating 1 monolayer of diacetylene. The dark C-V curve appeared in Fig. 8.1. Measuring frequency 4Hz, illumination intensity 5×10^{-4} W cm^{-2}.

causes a change in the flat-band voltage of the device i.e. a given amount of band-bending requires a less positive voltage than in the 'no-charge-stored' case. Also we note that the capacitance in accumulation is the same both in the dark, and under illumination. This confirms that the device was truly accumulated in the dark, as mentioned in section 7.3.2.

Illuminated C-V data for the full range of devices corresponding to those shown in Fig. 8.1 are shown in Fig. 8.5. The measurement conditions were as stated above.* It can be seen that the comments made concerning the one layer device are generally applicable. The shift along the voltage axis is between approximately 0.5 and 0.6V (negative) in all cases. Furthermore, the accumulation capacitance is largely the same as the value in the dark, except for the zero-layer contact. The approximately constant shift in bias voltage, which shows no sign of consistent scaling with LB film thickness, is interesting. It implies that the charge is not stored in the LB film itself, but rather at the 'oxide'/semiconductor interface. The charge cannot exist at the LB film/ 'oxide' interface, since the same shift occurs with no LB film present.

8.5.2 Conductance-Voltage Data

The conductance-voltage curves for these devices, corresponding to the C-V data of Fig. 8.5, are shown in Fig. 8.6 (the hysteresis is omitted). The dark G-V curves, which are not shown, exhibited no peaks : in forward bias the conductance increased rapidly. The most obvious effect of illumination is the introduction of a well defined conductance peak. The magnitude of the peak decreases with increasing LB film thickness, and its position moves to slightly more negative voltages. Although the exact magnitude and (to a lesser extent) the position of the peak varied slightly from device to device, measurements taken on many contacts indicate that the general trends shown in

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*The devices showed the same amount of hysteresis as encountered in the dark C-V measurements. As before, the hysteresis has been omitted from the diagrams for the sake of clarity.

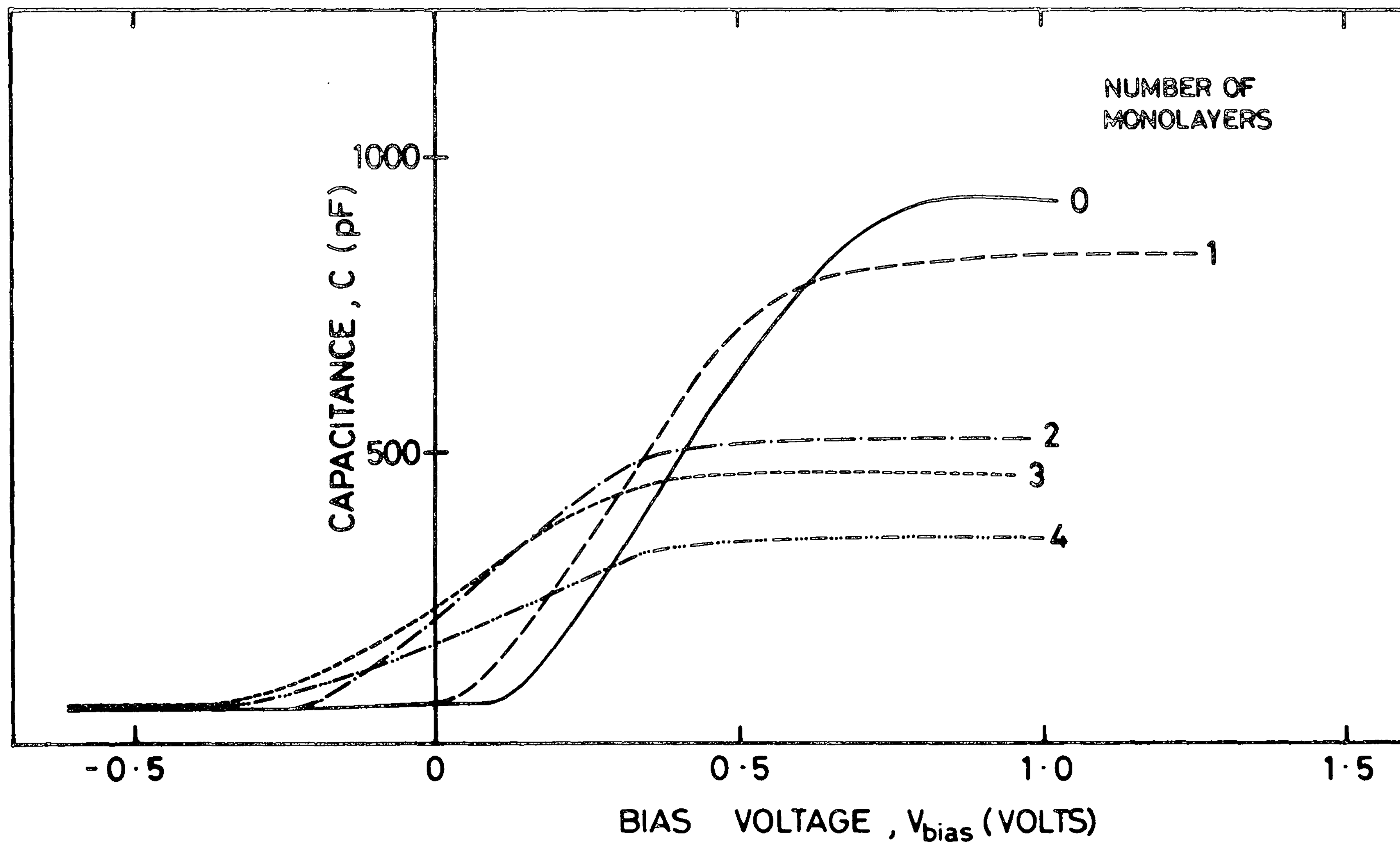


Fig. 8.5 Typical C-V characteristics under illumination for those devices whose dark C-V curves were shown in Fig. 8.1. The bias was scanned from negative to positive at 10 $mVsec^{-1}$. Illumination intensity 5×10^{-4} W cm^{-2}.

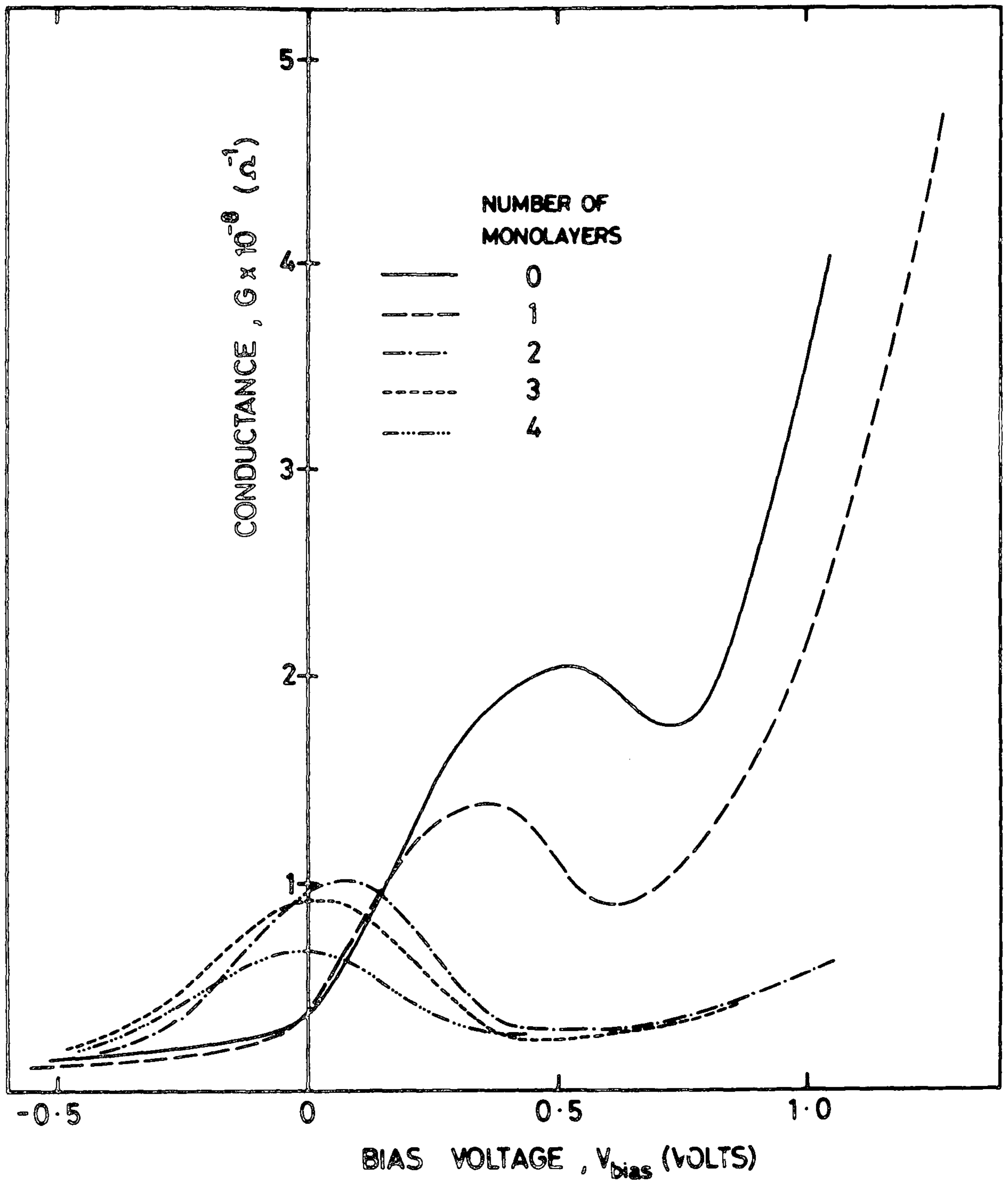


Fig. 8.6 Illuminated G-V curves corresponding to the C-V data shown in Fig. 8.5.

Fig. 8.6 are typical. Also, the magnitude of the conductance peak was found to increase as the measuring frequency was increased, but its position in bias remained constant.

The appearance of these peaks could be associated with the presence of interface states in the devices. The fact that the conductance peak remains fixed in bias as the frequency is increased implies that we are dealing with a single level of states rather than a distribution. As the peaks are observed for all devices, including the zero layer diodes, we must conclude that if interface states are responsible then they are not situated at the LB film/pre-deposition 'oxide' interface. They are therefore probably located at the 'oxide'/semiconductor boundary. This level of states could be critically dependent on the exact details of the etching procedure, or a fundamental property of the α-Si:H itself. The origin of the observed G peaks may be explained very simply by invoking the existence of such states. Under illumination, the quasi-Fermi level for electrons is such that the interface states (or some of them) are filled with photogenerated electrons. In the dark these states would normally be below E_F and hence they would be empty. When a bias is applied the quasi-Fermi level is swept through this interface state level, emptying the states. The electrons so released can contribute to the measured signal, producing a peak in the conductance. The presence of trapped electrons in interface states would also explain the shift in the C-V curves on going from the dark to illumination.

The magnitude of the conductance peaks can be related to the charge trapped in the states, and hence to the interface state density at a given bandgap energy (corresponding to the bias voltage). Unfortunately, the difficulties associated with the non-equilibrium conditions caused by illumination make any quantitative analysis impossible.

It is also possible that the conductance peaks may be associated, not with surface states, but rather with the parameters of the particular devices e.g. contact resistance, sample series resistance. The equivalent circuit of

a real MIS device contains components which represent the device as a whole i.e. barrier region, bulk semiconductor and 'ohmic' contacts. A model may contain several voltage dependent capacitors and resistors, and under certain conditions the combination of these components may give rise to completely spurious conductance peaks.

Further experiments would be needed to try and ascertain the correct origin of the observed conductance peaks. However, if they are a result of interface states this could be of some importance in solar cell applications, especially in Schottky barrier or MIS devices where they could influence the device characteristics and stability considerably.

8.6 Solar Cell Measurements

Although the devices which have been described in this section were not fabricated with a view to solar cell measurements it was felt worthwhile to perform some test measurements on them. It should be borne in mind that low photocurrents were expected in view of the lack of optimisation in the device structure and substrate preparation conditions e.g. the top electrode thickness was not optimised for sheet resistance and transmission of light, and no anti-reflection coating was used. However, the overall effect of the increasing insulator thickness should be observable, even though the device performance may not compare favourably with published solar cell efficiencies.

Fig. 8.7 shows the short-circuit current (I_{SC}) and open-circuit voltage (V_{OC}) as a function of the number of monolayers, N. The measurements were made at room temperature under white light illumination of about 5×10^{-4} W cm^{-2}. Results were averaged over at least five different contacts for each LB film thickness. The graph clearly shows a decrease in both I_{SC} and V_{OC} as N increases, with the fall in I_{SC} being rather more pronounced. The difference in both I_{SC} and V_{OC} between the zero and one layer devices would seem to suggest that there is an LB film present, although, as discussed previously, its quality as an insulator is evidently rather poor.

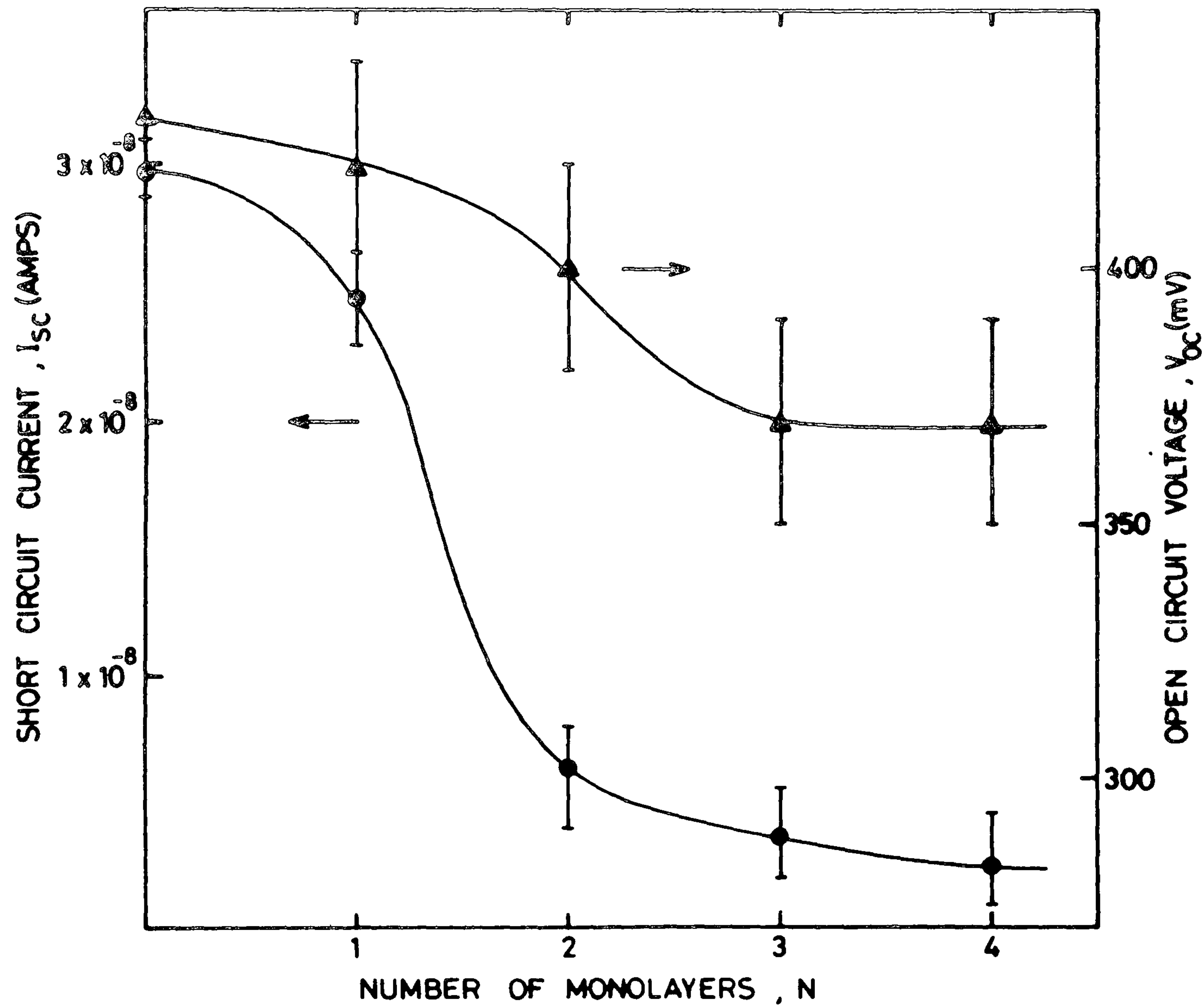


Fig. 8.7 Open circuit voltage and short circuit current measurements as a function of number of monolayers. Illumination intensity approximately 5×10^{-4} m W cm^{-2}.

The degradation of the solar cell performance by the incorporation of several monolayers is shown more clearly in Fig. 8.8. This graph shows the illuminated I-V curves for typical zero layer and 2-layer devices. The characteristics were measured under 15 m W cm^{-2} white light illumination. Even for the zero layer device the short circuit current is rather low and the fill factor is very poor. The concave nature of the curve at higher forward biases is indicative of a high series resistance, probably due to a poor ohmic back contact to the α-Si:H. This factor, together with the lack of device optimisation mentioned earlier, would account for the low values of I_{SC} observed. The two layer device has an open circuit voltage and short circuit current which have been markedly reduced.

Roberts et al[8,12] have already demonstrated the feasibility of using LB films as the insulator in MIS solar cells on single crystal CdTe, resulting in an increased efficiency. A direct comparison can be made between the data shown in Fig. 8.7 and their data, and also with the published results of Wilson and McGill[13], who have studied MIS solar cells on Dundee α-Si:H. For convenience, the relevant graphs from these two groups are reproduced as Figs. 8.9 and 8.10. Both graphs show a rise in V_{OC} as the insulator thickness increases. Wilson and McGill[13] found a peak in V_{OC} with a 20 Å layer of TiO_x, while for thicker insulators, V_{OC} fell quite rapidly. Roberts et al[8] reported a maximum in V_{OC} at approximately the same insulating layer thickness (24 Å of C4 anthracene LB film) which remained constant as the thickness increased. The short circuit current of a device should not be affected by the presence of a tunnellable insulator to any great extent. Insulators which are too thick (> 20-40 Å) inhibit tunnelling and thus reduce I_{SC}. This expected trend has been observed by Roberts et al[8]. Wilson and McGill reported the unusual result of a short circuit current which increased on the insertion of an insulating layer of less than 20 Å[13]. It is thought that this is due specifically to the nature of the α-Si:H solar cell[14]. Because

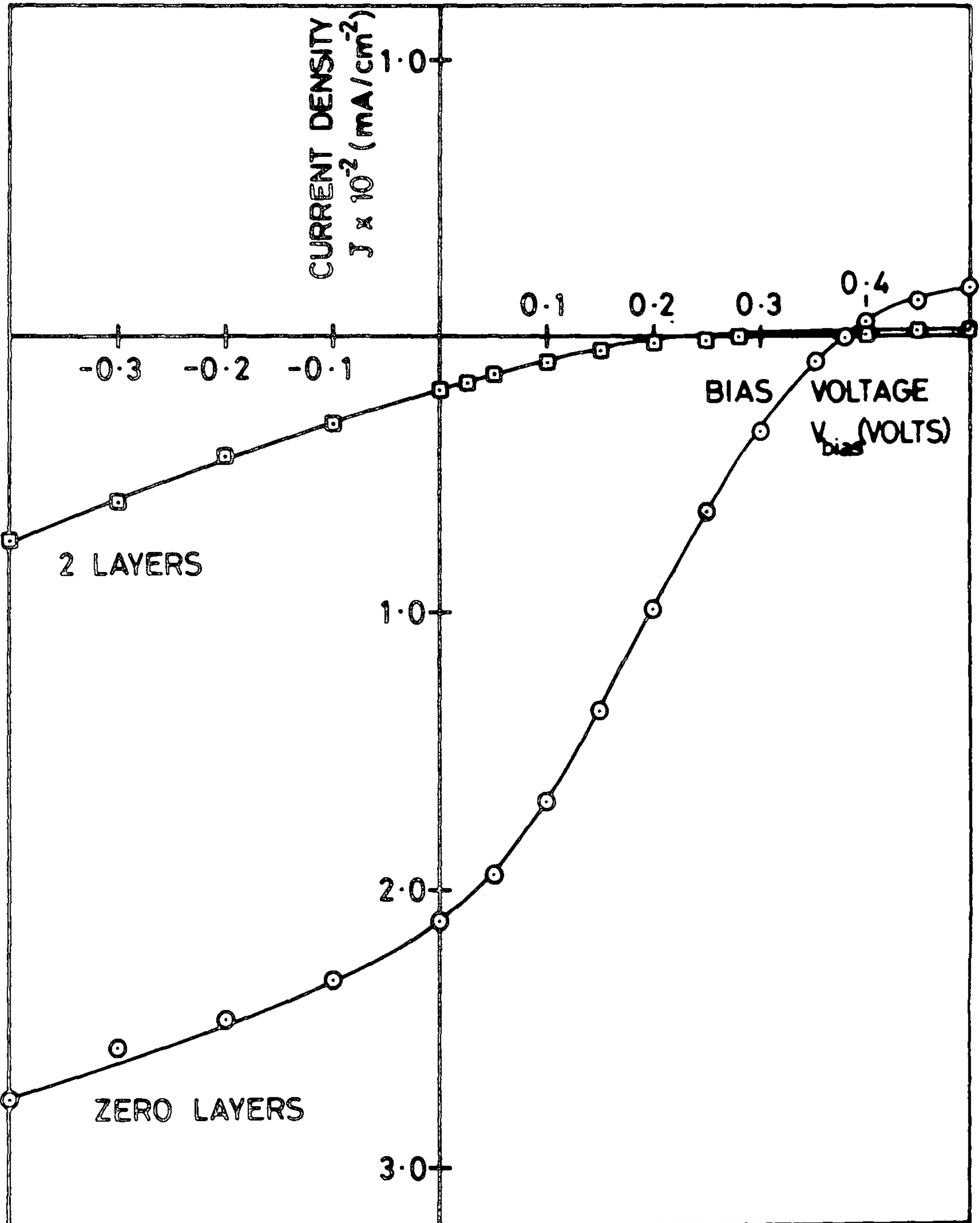


Fig. 8.8 Illuminated I-V curves (15 $mWcm^{-2}$ white light) for devices incorporating zero layers and two layers of diacetylene polymer. The two-layer device shows degraded solar cell operation.

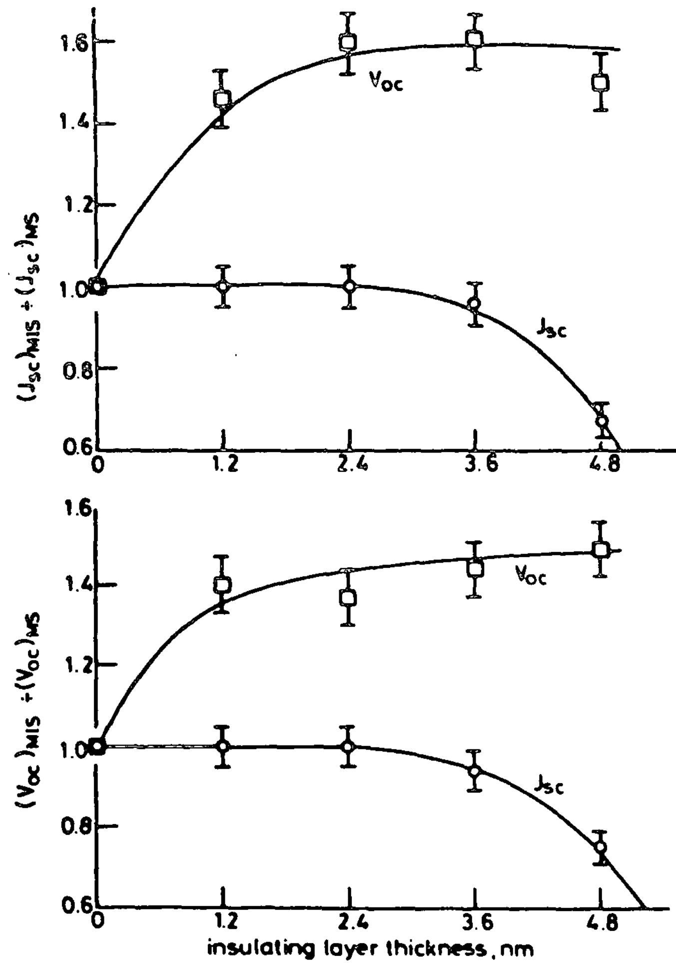


Fig. 8.9 Variation in V_{oc} and I_{sc} with insulator thickness for MIS devices on Single crystal CdTe. Data for two different substrates under AM1 illumination (after Roberts et al (38)).

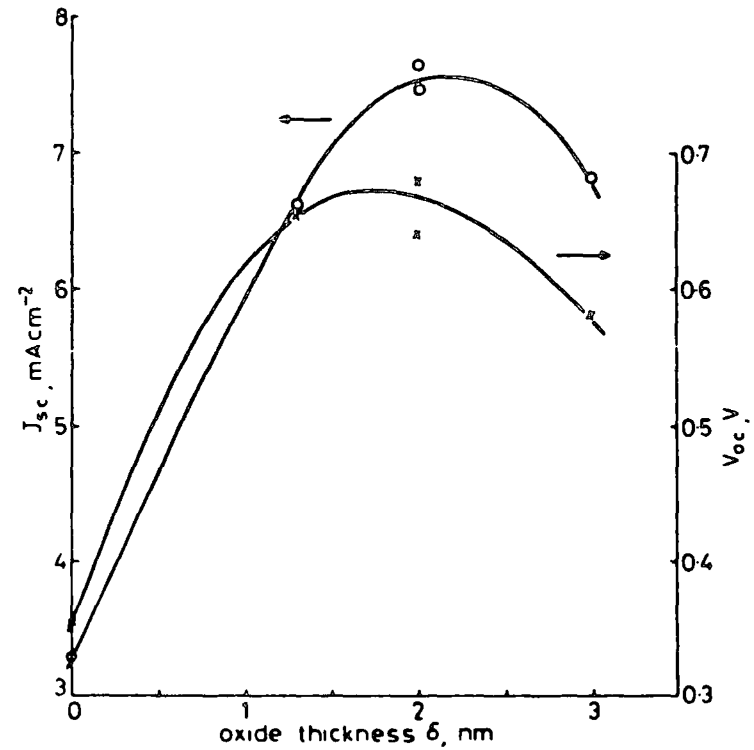


Fig. 8.10 Variation in V_{oc} and I_{sc} with insulator thickness for MIS devices on Dundee α-Si:H, in ~60 m Wcm^{-2} simulated sunlight (after Wilson and McGill (12)).

of the poor carrier lifetime in α-Si:H, photogenerated carriers are only collected when they are formed within the depletion region. Carriers produced in the bulk semiconductor recombine before they can be separated. If an insulating layer is interposed between the metal and the semiconductor the depletion width can be increased. According to McGill et al[14], 13 Å of oxide produced an increase of 540 Å in the depletion width. Hence, the number of photogenerated carriers collected (i.e. I_{SC}) is increased, and because of the relatively high absorption coefficient of α-Si:H, the rise can be quite substantial.

Obviously there is no peak in either I_{SC} or V_{OC} in Fig. 8.7, however, the effect of increasing the number of LB monolayers is quite clearly seen. From data presented earlier it should be noted that the zero monolayer points do not correspond to devices with no insulating layer. Indeed, the post-etch 'oxide' has been shown to be of quite a substantial thickness, equivalent to about one monolayer of LB film. Bearing this in mind, the curves of Fig. 8.7 are very similar to those of Wilson and McGill (see Fig. 8.10), with the peak in I_{SC} and V_{OC} in our case occurring at an insulator thickness less than, or equal to the post-etch 'oxide' thickness. It would seem that the LB film monolayers are having precisely the desired effect, but that the pre-deposition etching procedure has left an interfacial layer which is already greater than or equal to the optimum thickness for I_{SC} and V_{OC} enhancement. It follows that an alternative method of preparing the semiconductor substrate for LB film deposition must be found before the true potential of LB films for optimising the efficiency of α-Si:H solar cells can be realised.

8.7 Summary and Conclusions

Tunnelling MIS devices incorporating diacetylene polymer LB films have been successfully fabricated on Dundee α-Si:H. The data presented in this chapter may be summarised as follows.

(1) Capacitance measurements indicated that the deposited diacetylene monolayers were of reasonable quality and were stacking in a reproducible fashion. The $1/C$ v N graph yielded a dielectric thickness which corresponds with published data. The single monolayer case was the notable exception, and results suggested that this layer had been 'stripped' during top contact deposition, or else that it had very poor insulating properties.

(2) Capacitance measurements showed further that the etch treatment used before LB film deposition resulted in the formation of an interfacial 'oxide' layer. If the relative permittivity of this layer was assumed to be 4.0 then its thickness was estimated as $\sim$ 40 Å.

(3) The I-V data presented also exhibited the anomalous 1-layer behaviour described in (1). For thicker LB films the magnitude of the current decreased with increasing number of monolayers. The shape of the curves at low bias voltages (< 0.4V) has been explained in terms of an excess current mechanism involving surface states. At higher bias voltages the observed characteristics may be attributed either to surface states, as before (but involving surface states at a different energy), or to some modified form of thermionic emission involving the tunnelling coefficient of the insulator or fixed charge effects. It is thought that the high ideality factors involved make this latter explanation unlikely.

(4) Illumination with white light caused the capacitance-voltage curves to shift towards negative bias. This has been interpreted as evidence for the storage of photogenerated carriers in the surface states, which are probably located at the 'oxide'/semiconductor interface. The G-V curves exhibited peaks under illumination, which also points to the existence of surface states. The frequency dependence of these peaks shows that the states are at a single energy level.

(5) Solar cell measurements clearly demonstrated the effect of including an LB insulating film on the device characteristics. The results closely

parallel the work of Roberts et al[8] and Wilson and McGill[13], who have shown that increases in solar cell efficiency can result from the insertion of an insulator between a metal and semiconductor. Unfortunately, the presence of the 'oxide' layer discussed in (2) meant that any increase in efficiency which may have occurred in our devices was not seen. This 'oxide' layer was of a thickness greater than, or equal to, that required for efficiency enhancement. Allowing for this, the data presented here agree well with published results on α-Si:H[13].

CHAPTER 9

THICK INSULATOR MIS RESULTS

9.1 Introduction

This chapter deals with MIS structures which incorporate a thick i.e. non-tunnellable, insulating layer. The main aim of the work was the production of a practical, insulated-gate FET device based on the α-Si:H/LB film system, which may, for example, have application in the switching of liquid crystal display elements. One of the attractive features of this system is the large area capability of the Langmuir trough, an important consideration for display applications. Progress towards this goal of a practical device necessarily involves the investigation of the constituent parts of the device, and of simpler structures. The results presented in this chapter are organised in the following way. The first section deals with the admittance characteristics of MIS devices. Typical capacitance-voltage and conductance-voltage curves are introduced and the problem of hysteresis is discussed : some of the effects of illumination are also mentioned. Data are then presented which illustrate the effects of changing (1) the number of LB film monolayers, (2) the LB film material and (3) the frequency of measurement. The section concludes with a discussion of the application of the conductance technique for the evaluation of interface state densities. In the following section the current-voltage behaviour of these MIS structures is reported, and the interpretation is considered. The final section is concerned with field effect transistor measurements. In it, the characteristics of the first α-Si:H/LB film FET are presented, and the device performance is discussed in relation to α-Si:H FET's incorporating more conventional insulators. The chapter closes with a brief summary of the results.

9.2 Admittance Characteristics

9.2.1 Capacitance-Voltage and Conductance-Voltage Curves

Fig. 9.1 shows an example of the measured capacitance and conductance of an Au/cadmium stearate/α-Si:H (Dundee) MIS device as a function of gate bias voltage. The device structure is also shown (see inset). The gold electrode was approximately 100 Å thick and ∿ 1.25 mm in diameter (area ∿ 1.25 x 10^{-6} m^2). The insulating layer consisted of 31 monolayers of cadmium stearate LB film. Measurements were made in the dark, at room temperature and pressure, using a 29 Hz measuring signal. The bias voltage was ramped with a sweep rate of 5 mV sec^{-1} (direction as indicated). Before scanning, the device was kept in accumulation (at about +3V bias) for about 20 minutes. Hysteresis effects were encountered, although these have been omitted from the diagram for the sake of clarity. This problem will be fully discussed later on in this section.

The data exhibit a close similarity to those obtained for many MIS devices based on single crystal semiconductors. These include conventional systems such as Si/SiO_2[1], and other devices incorporating LB films which have been developed more recently e.g. on Si, InP, CdTe and GaP[2,3]. They are also in agreement with the small amount of published data on α-Si:H/SiO_2 MIS devices, which is limited to C-V measurements[4-6].

(a) Capacitance

The capacitance-voltage curve clearly shows accumulation and depletion characteristics. In accumulation, the measured capacitance corresponds reasonably well to the calculated geometrical capacitance. The experimental error involved can be estimated at approximately ± 10%, given the use of contact masking in electrode evaporation and the subsequent variations in electrode area. The errors inherent in the calculation, namely those from assuming the molecular length and dielectric constant of the film, are much smaller in comparison. The data for the depletion region may be plotted as $1/C^2$ against V. A straight line fit to such a plot yields an ionised

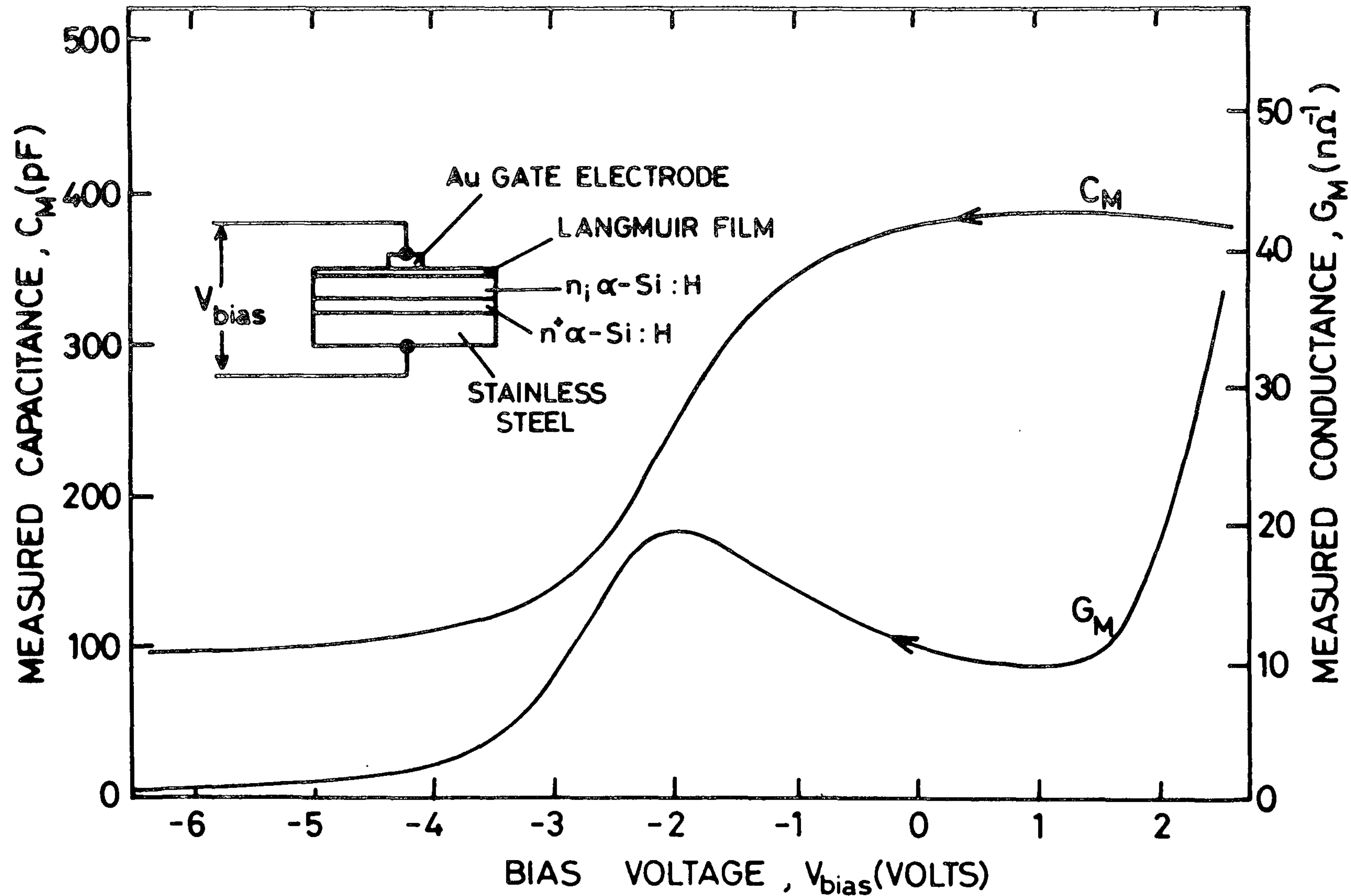


Fig. 9.1 Measured values of capacitance and conductance at 29Hz for an undoped α-Si:H/$CdSt_2$ capacitor (31 monolayers of $CdSt_2$; device area 1.5 x 10^{-6} m^2; voltage sweep rate 5 mV sec^{-1}).

donor concentration, N_d, of the order of 10^{16} cm^{-3}, using the theory established for crystalline semiconductors. This is the same magnitude as data published by Spear et al[7] for α-Si:H films produced under similar conditions. However, as these researchers emphasise, the capacitance technique is not a reliable method for calculating N_d for amorphous materials.

At more negative bias voltages the constant value of capacitance seems to indicate that the surface of the undoped α-Si:H has been inverted. It should be noted, however, that this is not conclusive evidence for inversion. It is also interesting to note that the increase in capacitance, due to minority carrier response in the 'inversion' region, does not appear. The usual reason for this is that the measuring frequency is too high for the minority carriers to respond e.g. in single crystal Si this cut-off frequency is about 100 Hz[8]. From Fig. 9.1 it is clear that for α-Si:H the minority carrier response cut-off frequency is much lower, which is consistent with a reduced minority carrier life-time. The effects of frequency on the admittance characteristics will be dealt with in a separate sub-section.

(b) Conductance

The measured conductance curve in Fig. 9.1 exhibits a distinct peak in the depletion region. Such peaks are commonly observed in single-crystal semiconductor MIS diodes[1-3] and may arise for a number of reasons. According to Nicollian and Goetzberger[1], there may be a conductance contribution associated with (1) loss in the insulating layer, due to the capture and emission of carriers at various defects, traps etc, (2) loss in the semiconductor space charge region, due to the interaction between carriers and bulk levels (states), and (3) loss at the interface because of capture and emission of carriers by interface states. Any or all of these effects may be present in a given diode, although in the latter case it is likely that

one of them will be dominant. In this context it is interesting that MIS devices incorporating cadmium stearate (and other) LB films on a number of single crystal semiconductor substrates exhibit peaks in their conductance-voltage characteristics[2,3]. The many detailed measurements performed by the Durham group have shown that identical LB films on different semiconductors give rise to conductance peaks of differing magnitude and position (with respect to the capacitance-voltage curve). This would suggest that the origin of the peaks is not loss in the insulating layer, since identical films would then be expected to produce similar peaks. On the other hand, evidence presented in Chapter 6 from RHEED experiments indicated that LB films on α-Si:H were of poorer structural quality than those deposited onto single crystals. Defects in the film could lead to an enhanced conductance and it may be that LB films on α-Si:H should be treated as a special case, in which case the results obtained on single crystal semiconductors are not applicable.

In forward bias the conductance increases rapidly. This is most probably due to conduction through the LB film. The device series resistance may also be a contributing factor, although when this is dominant the conductance-voltage curve flattens out at a non-zero value. From such a plateau the series resistance may be calculated using equation 4.20, substituting the accumulation capacitance and conductance. Although a small plateau does appear in the G-V curve of Fig. 9.1, the problem of hysteresis (see later) and the difficulty in separating the effects of series resistance and film leakage render any calculations meaningless.

9.2.2. The effects of Illumination

Illumination of the devices with light of photon energies greater than 1.6 eV (the α-Si:H bandgap) was found to have several effects on the admittance data. These effects will be discussed as appropriate throughout the chapter, but it is pertinent to consider one of them in particular at this point. Under illumination the C-V and G-V curves were shifted to more

negative bias voltages. Both the curves were shifted by the same amount i.e. the conductance peak was observed at the same value of capacitance in the dark and in the light. Now, under illumination the space charge width in the α-Si:H will be decreased, and at a given voltage the semiconductor surface potential is reduced. This involves a change in the distribution of the applied voltage throughout the device i.e. more voltage is dropped across the insulator and less across the semiconductor. Following Nicollian and Goetzberger[1] we note that the appearance of the G peak at the same capacitance value under different conditions means that the loss is associated with a particular value of surface potential, and not with the magnitude of the field in the insulator. We may thus conclude that the conductance peak is not due to loss in the insulating layer.

9.2.3 Hysteresis Effects

The degree of hysteresis encountered in these devices was very large. Fig. 9.2 shows the data previously shown in Fig. 9.1, now including the hysteresis (note the decreased conductance scale). The direction of the voltage sweep is shown by the arrows. This sense of hysteresis i.e anti-clockwise, is generally associated with the drifting of ions through the insulator or with the formation of dipoles (polarisation) within the insulator, or at its interfaces[9]. There are some reports of hysteresis in LB film MIS devices in the literature[10,11], and it is normally attributed to the presence of mobile ions which were introduced into the films during monolayer deposition or absorbed during electrode evaporation. Workers at Durham have also noted such effects (see for example refs (12) and (13)). However, in general the magnitude of the hysteresis, even in the poorest devices, is much less than is observed for these α-Si:H based diodes. Clearly then, hysteresis on the scale shown in Fig. 9.2 is a property of the Au/cadmium stearate/α-Si:H system.

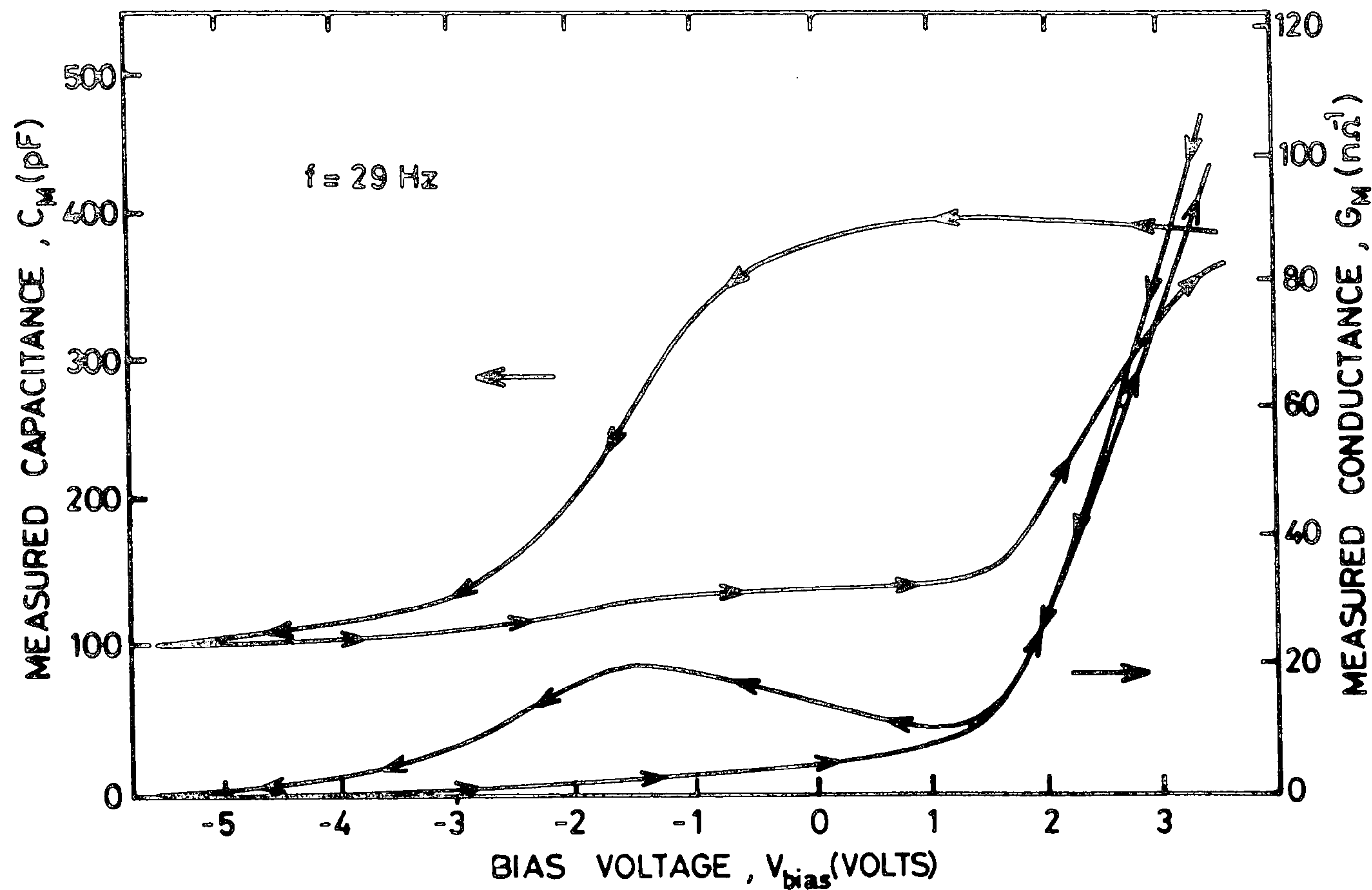


Fig. 9.2 Capacitance and conductance data as in Fig. 9.1 but showing the effects of hysteresis. Direction of voltage sweep as shown by arrows.

The magnitude of the hysteresis was found to be dependent on two of the experimental parameters in particular : the sweep rate of the bias voltage and the range over which the bias voltage was scanned.

(1) Bias voltage sweep rate: the curves shown in Figs. 9.1 and 9.2 were measured using the slowest sweep rate available, 5 m V sec^{-1}. As the rate of change of voltage was stepped up, the hysteresis effects worsened. In Fig. 9.3, data taken at two different sweep rates are shown for comparison. The single arrows indicate a rate of 5 m V sec^{-1} and the double arrows 20 m V sec^{-1}. The measuring frequency was 29 Hz. The shape of the curves has not changed at all, indicating that the basic processes taking place in the diode are unaffected. The effect is a pure shift along the voltage axis in both directions i.e. an increase in hysteresis, and is a result either of the inability of the low mobility ions to respond to the changing voltage immediately, or of the time constant associated with the polarisation. Higher sweep rates gave even worse hysteresis and no 'saturation' of the effect was noted. It should also be emphasised that, under the conditions used, the response time of the experimental system was not a significant factor.

(2) Bias voltage scan width. Fig. 9.4 shows capacitance versus voltage curves for three different bias voltage scan widths. The corresponding conductance-voltage curve has been sketched in for reference (broken line). The measuring conditions were as previously described, and the frequency was 29 Hz. Starting with the device in accumulation and ramping towards depletion the hysteresis was minimal, providing the direction of the scan was reversed before reaching negative bias. This is shown by the curves marked with single arrows (+ 2V → + 1V → +2V sweep) and with double arrows (+ 2V → 0V → +2V sweep). Biasing into negative voltages, corresponding to the conductance peak region, resulted in the large hysteresis shown by the triple arrow curve (+ 2V → -2V → +2V sweep). The hysteresis was not increased any further by sweeping to more negative voltages.

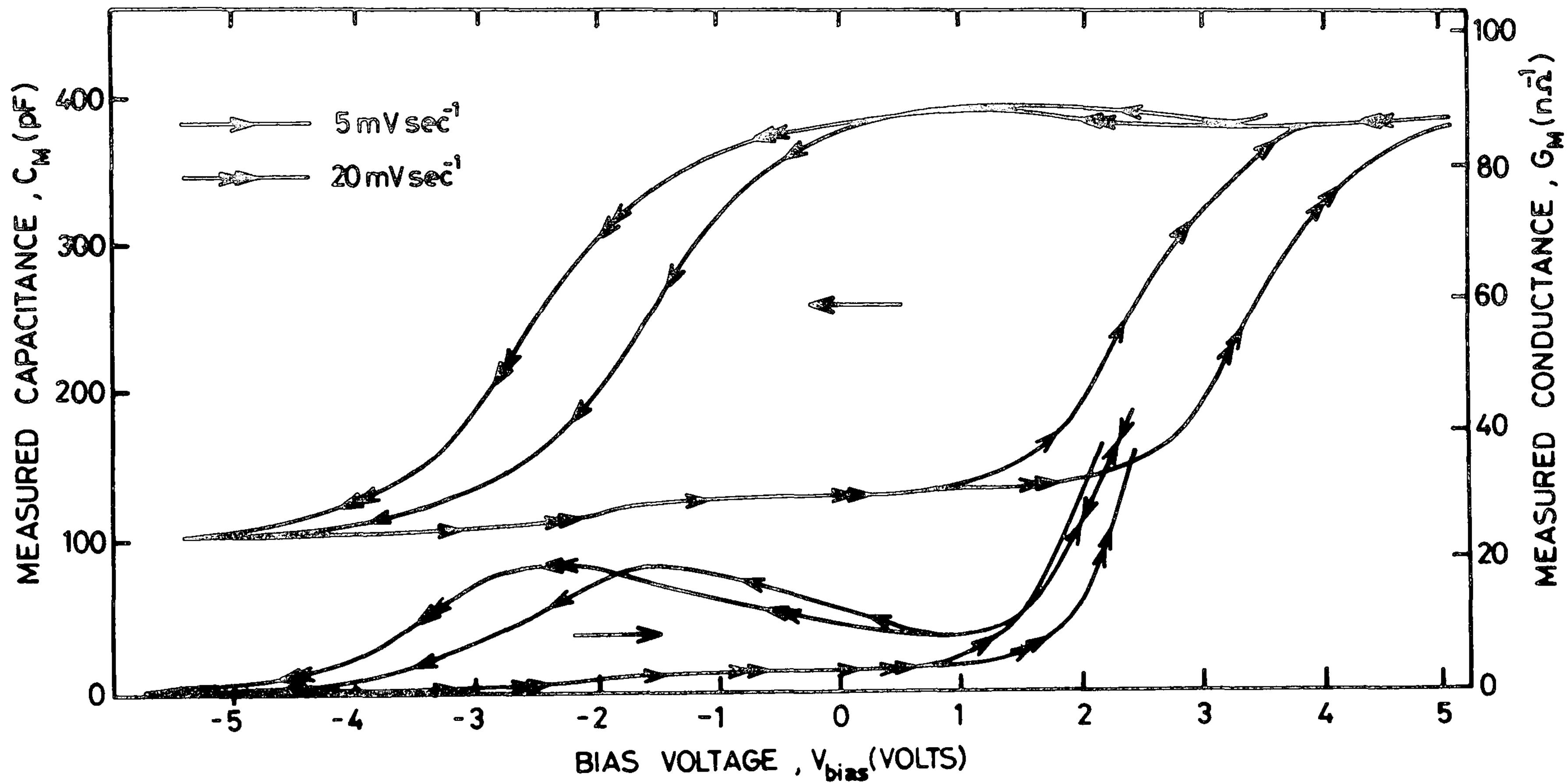


Fig. 9.3 Effect of bias voltage sweep rate on the observed hysteresis in the capacitance and conductance. Sweep rates and directions as shown : measuring frequency 29 Hz.

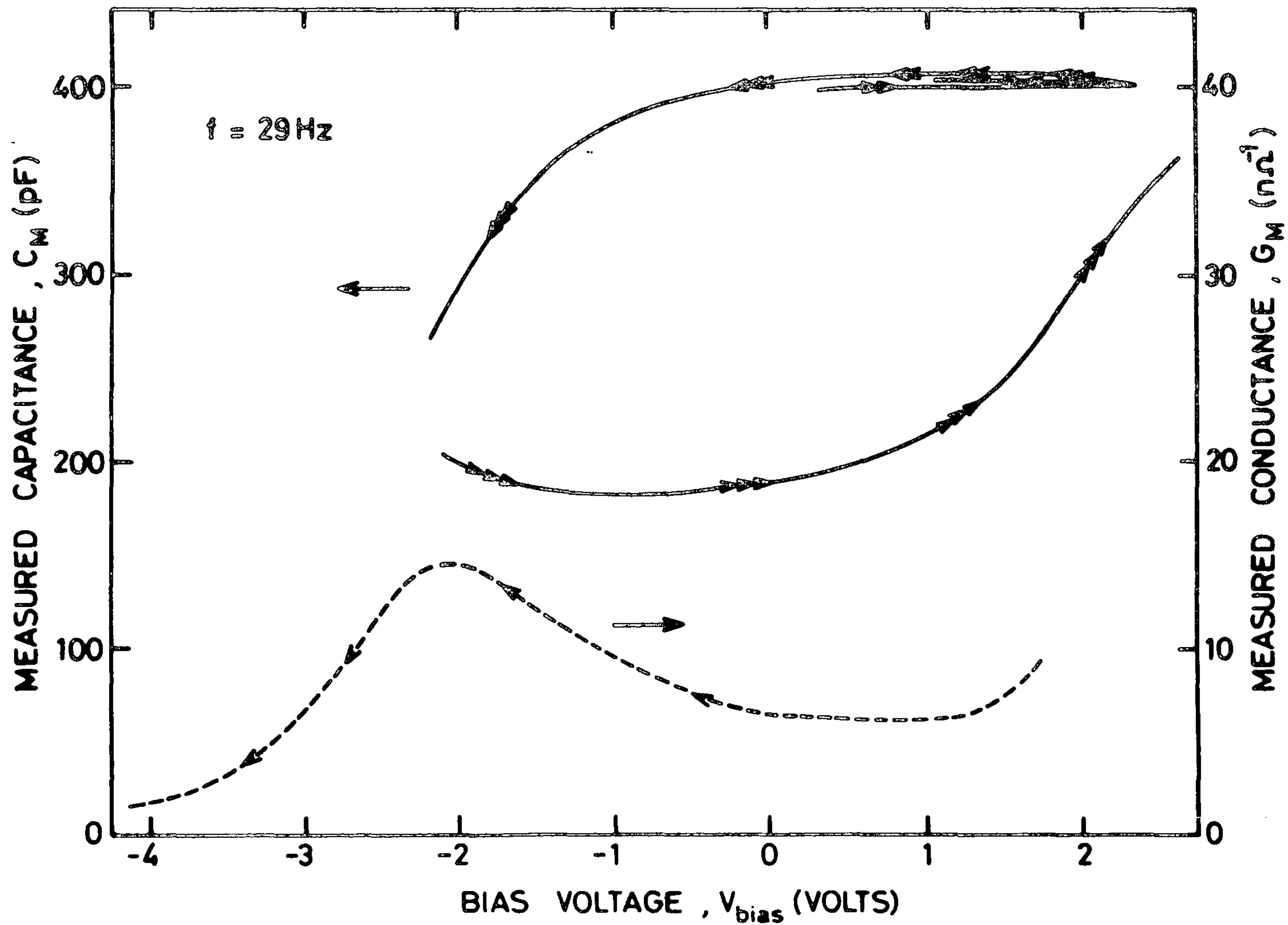
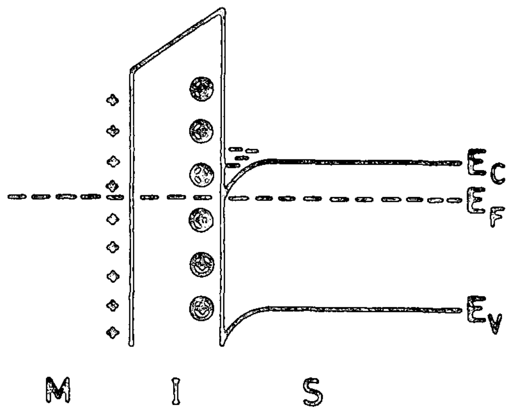
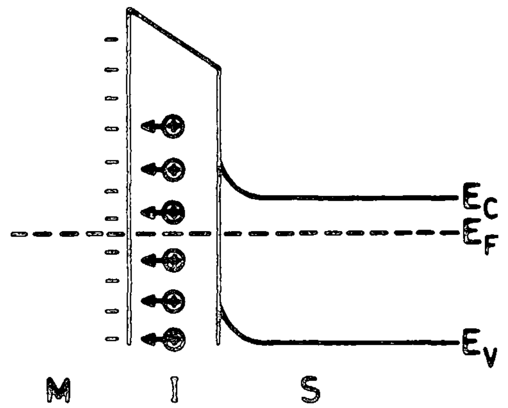


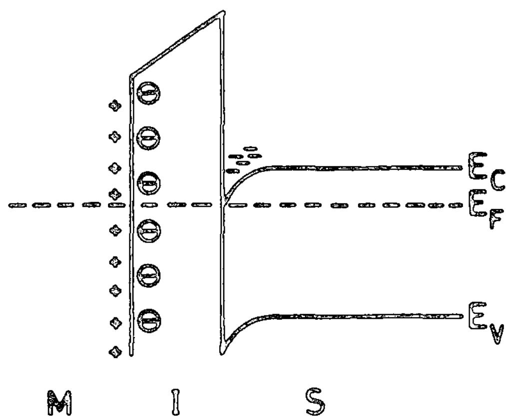
Fig. 9.4 Effect of bias voltage scan width on the magnitude of the hysteresis in the capacitance. Single arrows : +2V → +IV → +2V sweep. Double arrows: +2V → OV → +2V sweep. Triple arrows : +2V → -2V → +2V sweep. The dotted curve shows the corresponding conductance-voltage characteristic.

This behaviour may be understood by considering a simple model for ion drift. Assuming that the hysteresis is due to the presence of positive ions in the insulating film, the situation in accumulation may be described in terms of the energy band diagram shown in Fig. 9.5(a). In accumulation, the metal electrode is positively charged and any mobile positive ions will be repelled towards the metal/semiconductor interface. This process is enhanced by the presence of the electron accumulation layer at the semiconductor surface, which attracts the positive ions. Thus, if left in accumulation for a reasonable period of time (as was the case experimentally), we may assume that all of the mobile ions will reside at the metal/semiconductor interface as shown. For bias scans where the voltage remains positive the semiconductor surface remains accumulated, and since the metal is always positively charged the ions will not move. Hence no hysteresis is observed. If, however, the device is scanned into the negative bias region, the ions will be attracted towards the metal electrode. Furthermore, the semiconductor becomes depleted of majority carriers at its surface, removing the ionic attraction which was present during accumulation. The resulting ionic movement (see Fig. 9.5(b)) causes hysteresis. It is, of course, equally likely that the hysteresis could be due to the motion of negative ions. In this case a similar model can be applied, the difference being that in accumulation the ions reside at the metal/insulator interface. Biasing into depletion causes movement towards the semiconductor (see Figs. 9.5(c) and (d)).

The observed behaviour may also be understood using the polarisation model, the alternative explanation for the hysteresis. An ideal dipole layer is a sheet of positive charge separated by a given distance from a sheet of negative charge. Such dipoles may exist within the insulator or at its interfaces. The dipoles are aligned when a field of a given magnitude is applied. It then requires a certain field in the opposite direction to re-orientate the dipoles, and thus hysteresis occurs. With reference to Fig. 9.4., it is quite probable that in accumulation all the dipoles are







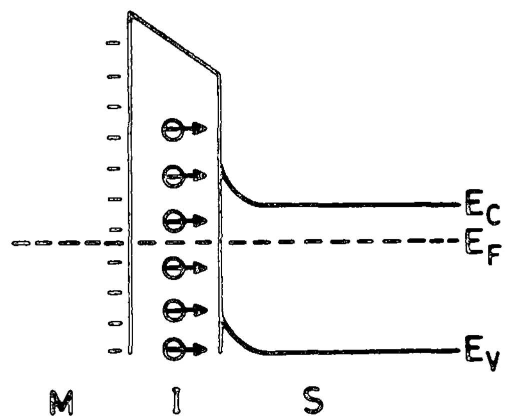


Fig. 9.5 Schematic diagrams showing the ionic movement which could lead to hysteresis with positive ions (a and b) or negative ions (c and d).

aligned. As long as the bias voltage sweep remains positive this alignment is undisturbed, and there is no hysteresis. When the bias is swept from +2V to -2V and back again, reorientation of the dipoles occurs with the resulting hysteresis.

Finally, it was discovered that illumination with light of energy, E, greater than the bandgap of the α-Si:H ($E > 1.6$eV) caused a drastic reduction in the hysteresis. The voltage difference between the two branches of the capacitance curve is several volts in the dark, and only a fraction of a volt under illumination. The change is obviously linked with the absorption of light by the α-Si:H, which produces an increased carrier density at the semiconductor surface. It is thought that the reduction in hysteresis is due either to the neutralisation of ions at, or near the semiconductor surface by some of this extra charge, or to the effect of the charge in screening any dipoles from the reorientating electric field.

The problem of hysteresis can, to some extent, be circumvented by using the slowest possible bias voltage ramp speeds, and by ensuring that measurements on different devices are made under identical conditions e.g. the same bias voltage 'history', the same temperature etc. Slow ramp speeds were used in the experiments described in this chapter, even though they made data collection very time consuming. Care was also taken to ensure that sets of data were taken under comparable circumstances by adopting standard procedures e.g. leaving a sample in the dark for a given length of time after exposure to light whilst making pressure contact to a device, and holding a device in accumulation for a certain time before recording any data.

9.2.4 Changes in Insulator Thickness

The effect of changing the insulator thickness on the capacitance of an MIS device incorporating an LB film is of particular interest, since it gives information on the stacking of the monolayers and on their dielectric strength. This was investigated by dipping an α-Si:H sample with a number

of different LB film thicknesses, namely 11, 15, 19, 23, 27 and 31 monolayers of cadmium stearate. The usual pre-deposition etching system was used. The top contacts were about 200 Å of evaporated gold, and each contact area was 1.96 x 10^{-7} m^2 (± 10%).

(a) C-V in the dark

Fig. 9.6 shows typical C-V curves for 11, 15 and 23 cadmium stearate monolayers. The data were recorded at room temperature and pressure, at a frequency of 4 Hz. To ensure the reproducibility of the results a standard measurement procedure was adopted. After contact to a device was made the sample was left in the dark (at zero bias) for approximately 1 hour. It was then held at + 1V forward bias for 20 minutes before the C-V curve was measured, using a bias voltage ramp speed of 10 mV sec^{-1}. All the curves shown were taken from the same hysteresis branch.

In the accumulation region the measured capacitance should be constant and equal to the insulator capacitance. Comparing the calculated capacitance due to the different LB film layers (C_{INS}) with the experimental accumulation values (C_{accum}) we find reasonable agreement. Interestingly, the measured values were always below the theoretical figures by an amount not exceeding 10%. Although this is within the experimental error arising from variations in electrode area and from stray capacitance, it is unlikely that C_{accum} would be consistently less than C_{INS} : a scatter of points greater than and less than the theoretical values would be expected. A possible explanation is that there was an interfacial layer present, resulting in a double dielectric structure and the consequent short-fall in accumulation capacitance. It could also be that the surface was not fully accumulated.

(b) C-V under illumination

The illuminated curves corresponding to the C-V data shown in Fig. 9.6 are given in Fig. 9.7 (i.e for the same devices). The measurements were taken under normal room lighting (white light), corresponding to an intensity of about 0.5 m W cm^{-2}. All other conditions were as described for Fig. 9.6.

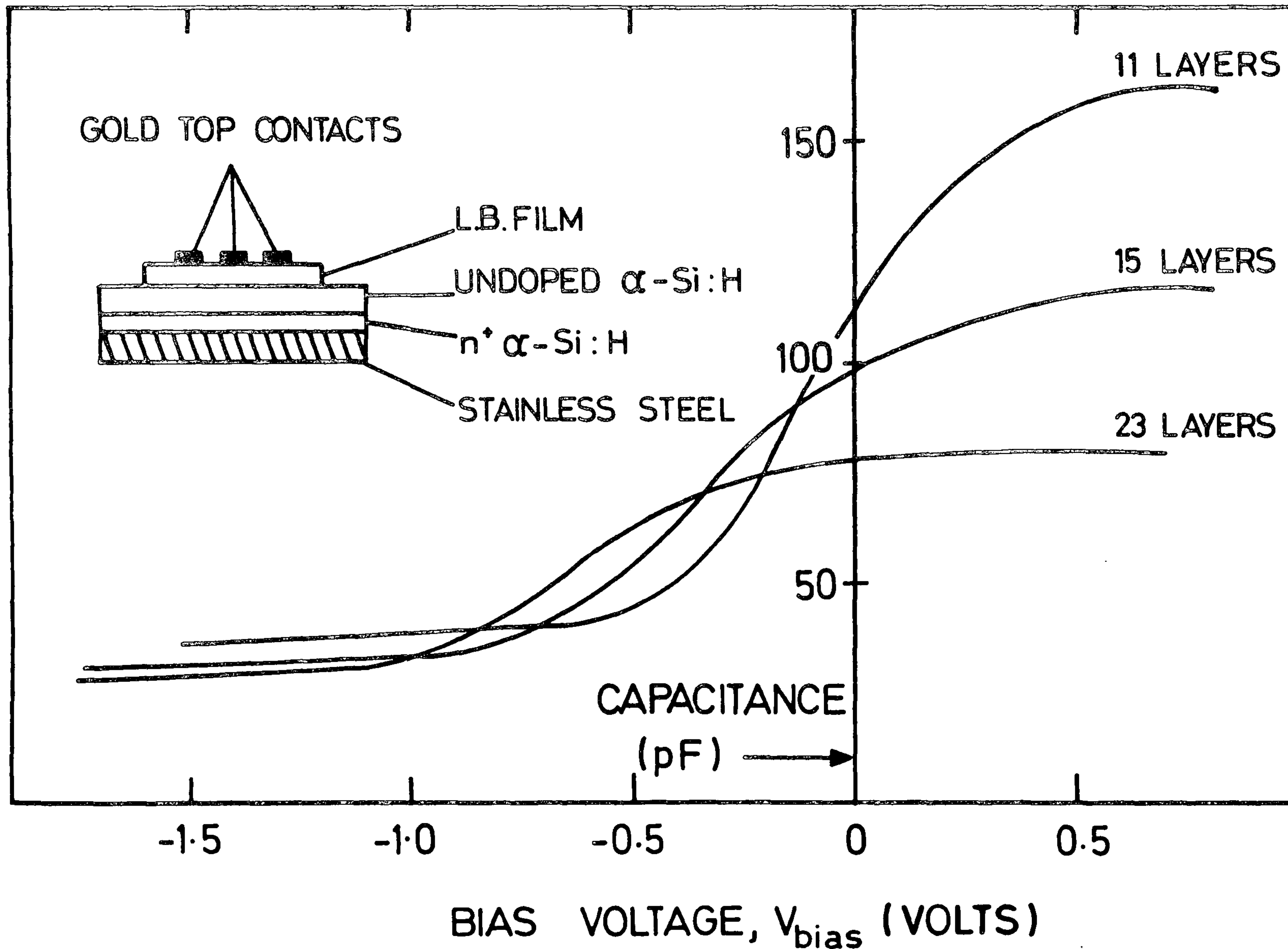


Fig. 9.6 Typical C-V curves for $Au/CdSt_2/\alpha$-Si:H MIS devices incorporating 11, 15 and 23 monolayers of cadmium stearate. Measurements taken at 4Hz, in the dark.

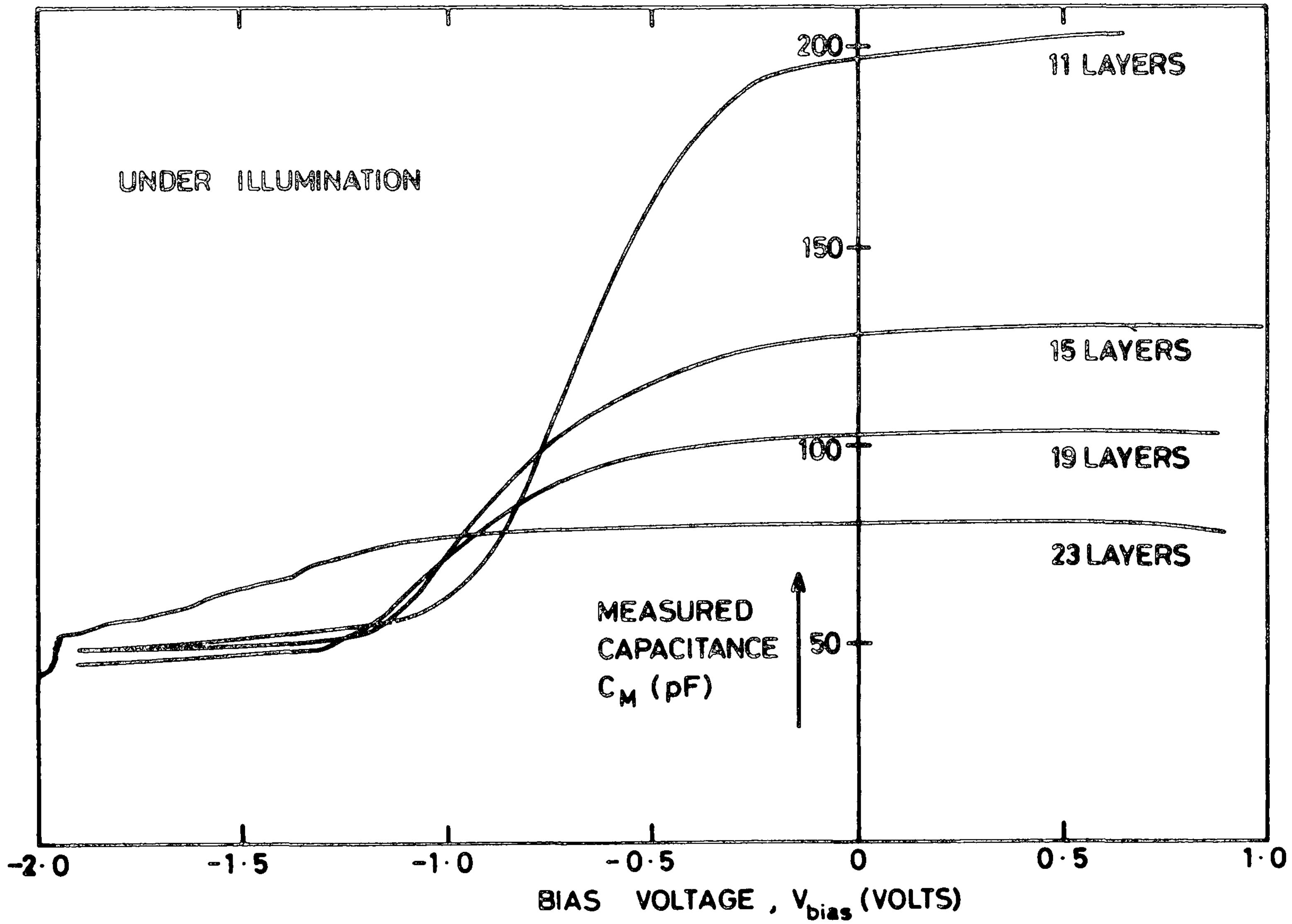


Fig. 9.7 Illuminated C-V curves corresponding to those shown in Fig. 9.6.

The accumulation capacitance under illumination rose from its dark value. All of the curves gave a measured value greater than the calculated insulator capacitance, with the margin of error ranging from 0-7%. The only exception was the 11 layer curve, which showed a 20% increase in C_{accum}: the reason for this anomalous behaviour is not understood. The general trend, however, may be understood if one considers the increase in the free carrier density in the α-Si:H caused by the photons. The production of electron-hole pairs in the α-Si:H reduces the surface potential, which results in a reduction of the width of the space charge layer and a corresponding increase in capacitance[14]. Hence, the measured capacitance in accumulation should more closely approach the insulator capacitance. The agreement between experimentally obtained and predicted values is quite acceptable.

The effect of light on the capacitance in the 'inversion' region is more marked. This is normally the case in single crystal MIS devices[14]. As well as reducing the surface potential, illumination decreases the time constant of minority carrier generation, and this allows the inversion layer to respond to higher frequencies than in the dark. As a result, illumination can lead to a rise in capacitance in inversion which, in the dark, is usually associated with a low frequency measurement (see chapter 4). Although this effect must be present in our devices, it is evident from the constant inversion capacitance under illumination that the inversion layer still cannot respond to the 4 Hz signal. The magnitude of the inversion capacitance, though constant, is increased from its dark value by 67%. This must be attributed to the reduction in surface potential discussed in conjunction with the accumulation region.

A comparison of Figs. 9.6 and 9.7 shows that illumination causes the curves to shift to more negative voltages. After exposure to light the devices must be left for several hours before the curves return to their original values. The voltage shift is approximately the same for all of the film thicknesses used. This behaviour is consistent with the incorporation

of fixed positive charge somewhere in the system. It is most probable that this consists of trapped photogenerated charge. The charge may be trapped in the LB film or at the LB film/semiconductor interface. If, as is likely, there exists an interfacial 'oxide' layer then there are a greater number of possibilities : within either the LB film or the 'oxide' layer, or at the LB film/'oxide' or 'oxide'/semiconductor interfaces. The time taken for the devices to recover points to traps which have a very long lifetime ($\gtrsim 10^4$ secs).

(c) <u>$^1/_C$ v N results</u>

The scaling of the accumulation capacitance with LB film thickness seen in both Fig. 9.6 and Fig. 9.7 is a clear indication that the monolayers of cadmium stearate are stacking in a reproducible fashion. This can be more clearly represented by plotting the reciprocal capacitance against the number of monolayers, N (see 5.6.3). Such a plot, for devices on the same substrate as those whose C-V characteristics were shown earlier, is given in Fig. 9.8. Two sets of data are shown, both of which were measured at 4 Hz. The circles represent data taken in the dark, with the device biased into accumulation, thus allowing a true measurement of the insulator capacitance. The curves shown in Fig. 9.6 were used for this. The squares denote data measured with the sample illuminated with white light and at zero bias. From the C-V curves, these conditions also correspond to accumulation. These results are the averaged measurements over ten different contacts at each film thickness. The spread in these measurements was generally less than 6%, which demonstrates the uniformity of the films over large areas. The good straight lines obtained in both cases confirm the reproducibility of monolayer deposition.

It can be seen that there is really very little difference between the dark and illuminated data : the intercept on the $^1/_C$ axis is approximately the same and the difference in slopes is less than 7%. Taking the

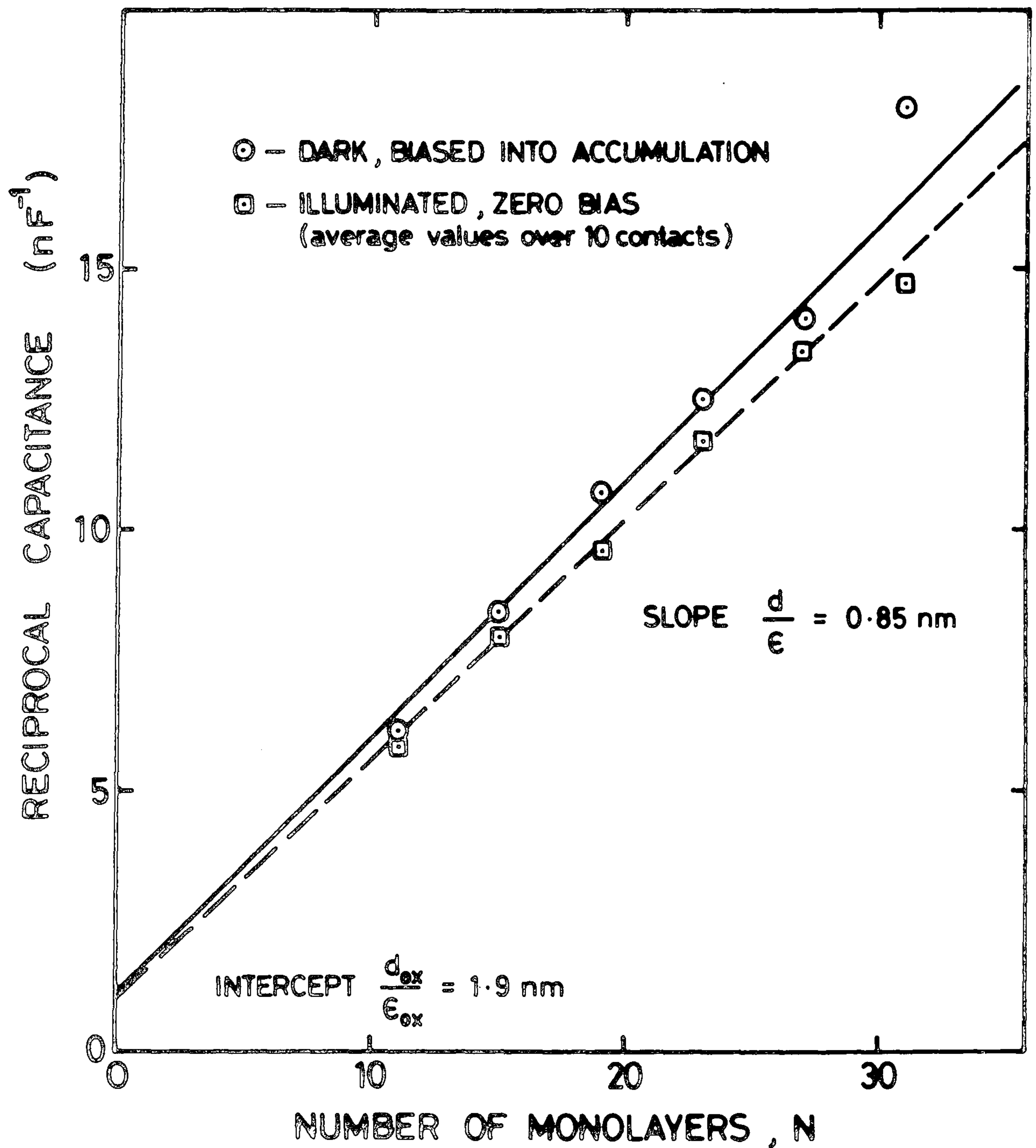


Fig. 9.8 Reciprocal capacitance versus number of monolayers for devices on the same substrate as those whose C-V characteristics were shown in Figs. 9.6 and 9.7

illuminated data, the slope yields the dielectric thickness of the insulator to be (d/ε_r) $\sim$ 0.8 nm. Assuming the relative permittivity of cadmium stearate to be 2.5[15], the monolayer thickness is calculated to be $\sim$ 2.1 nm. This value is rather low compared with the chain length of about 2.5 nm reported by many workers[13, 16-18]. The presence of an interfacial 'oxide' layer, as postulated earlier, is confirmed by the non-zero intercept of the graph. The dielectric thickness of this layer (i.e. d_{ox}/ε_{ox}) is $\sim$ 1.9 nm. Because of the uncertainty of the composition of this layer the thickness cannot be accurately calculated, as the relative permittivity is unknown. However, as a guideline, if the 'oxide' layer had a relative permittivity of 3.9 (equivalent to SiO_2), this would correspond to a 7.4 nm covering. The capacitance of this layer would appear in series with the insulator capacitance, and is of the right order to explain the shortfall in capacitance in the dark discussed earlier.

(d) Flatband Voltage Changes

Further inspection of Figs. 9.6 and 9.7 reveals that increasing the number of LB film monolayers increases the device flat-band voltage. Hickmott, in his work on the Si-SiO_2 interface[19-20], has demonstrated that the variation in flatband voltage, V_{FB}, with insulator thickness can give information concerning any charge distributed throughout the insulator, and any dipole layers within the insulator or at its interfaces. The generalised expression for the flatband voltage of an MIS capacitor may be written as follows[19].

$$V_{FB} = \phi_{MS} - \frac{\sigma t}{\varepsilon_o \varepsilon_r} - \frac{d}{L}\left(\frac{Q_I}{C_{INS}}\right) - \frac{Q_{SS}}{C_{INS}} + \phi_F \qquad (9.1)$$

where ϕ_{MS} is the metal-semiconductor work function difference with respect to the intrinsic Fermi level, and ϕ_F is the difference between

the semiconductor Fermi level and midgap. The other terms denote contributions from various charges within the device structure. Q_{SS} represents the charge at the semiconductor/insulator interface (in Cm^{-2}), which may be fixed charge and/or charge in the surface states. C_{INS} is the insulator capacitance, and $(\varepsilon_o \varepsilon_r)$ the insulator permittivity. Charge distributed throughout the insulator may usually be represented by a centroid of charge, Q_I, at a distance d from the metal/insulator interface. The effect of such charge is included through the third term, where L is the insulator thickness. Finally, dipole layers may exist at the interfaces, or in the insulator, and this is allowed for in the second term. Here, σ is the charge density (Cm^{-2}) and t is the distance of separation of the two sheets of charge.

The effect of these various types of charge on the flatband voltage v insulator thickness graph may be seen more easily by re-writing equation 9.1 as follows.

$$V_{FB} = -\left(\frac{d}{L}\frac{Q_I}{C_{INS}} + \frac{Q_{SS}}{C_{INS}}\right) + \left(\phi_{MS} - \frac{\sigma t}{\varepsilon_o \varepsilon_r} + \phi_F\right) \qquad (9.2)$$

By substituting for C_{INS} we have

$$V_{FB} = -\left(d\frac{Q_I}{\varepsilon_o \varepsilon_r} + \frac{Q_{SS}}{\varepsilon_o \varepsilon_r}L\right) + \left(\phi_{MS} - \frac{\sigma t}{\varepsilon_o \varepsilon_r} + \phi_F\right) \qquad (9.3)$$

From this equation it is clear that:

(1) the introduction of dipole layers anywhere in the structure will cause changes in the intercept of the graph $\left(\frac{\sigma t}{\varepsilon_o \varepsilon_r}\right)$

(2) any change in the position of the bulk Fermi level with respect to midgap will change the intercept (ϕ_F).

(3) differences in the charge stored at the semiconductor/insulator interface between devices will change the slope of the graph $\left(\frac{Q_{SS}}{\varepsilon_o \varepsilon_r}\right)$.

(4) changes in the charge distribution throughout the insulator can give rise to changes in the intercept or the slope, depending on the exact nature of the distribution. If d is a constant, independent of the insulator thickness L, then the first term in equation 8 may be grouped with the terms in the second bracket. In this case the charge distribution will change the intercept of the graph. Alternatively, d may be a function of L eg. $^{d}/_{L}$ may be a constant, in which case changes in the distributed charge will cause a change in the slope.

In Fig. 9.9 the flatband voltage is plotted against the number of LB monolayers, N, for the devices which have already been described. The value of V_{FB} was found by calculating the flatband capacitance, using equation 4.4 and assuming a free carrier density of 5×10^{16} cm^{3}, and then reading V_{FB} from the experimental C-V curves (see Figs. 9.6 and 9.7) Data are shown for dark and illuminated conditions, and the error bars indicate the effect of changing the free carrier density in the calculation between 10^{16} and 10^{17} cm^{-3}.

Despite the limited number of experimental points, both sets of data appear to be reasonable straight lines with the same slope. From this observation we may say that illumination does not change the amount of charge stored at the semiconductor/'oxide' interface. The sign of the slope (negative) is indicative of positive charge in the system. Although this is the same slope as measured by Hickmott for the Si/SiO_2 based MOS diode, it is the opposite slope to that reported by Martin for cadmium stearate LB films on single crystal (p-type) silicon(12). This may be due to the fact that different interfacial 'oxide' layers form on the Si and the α-Si:H prior to LB film deposition. The 'oxide' on Si could be negatively charged, while that on α-Si:H may incorporate positive charge. Alternatively, the LB films on the respective substrates may contain charges of opposite sign, as a result of differences in the deposition and electrode evaporation procedures. From the slope, the value of Q_{SS} was calculated to

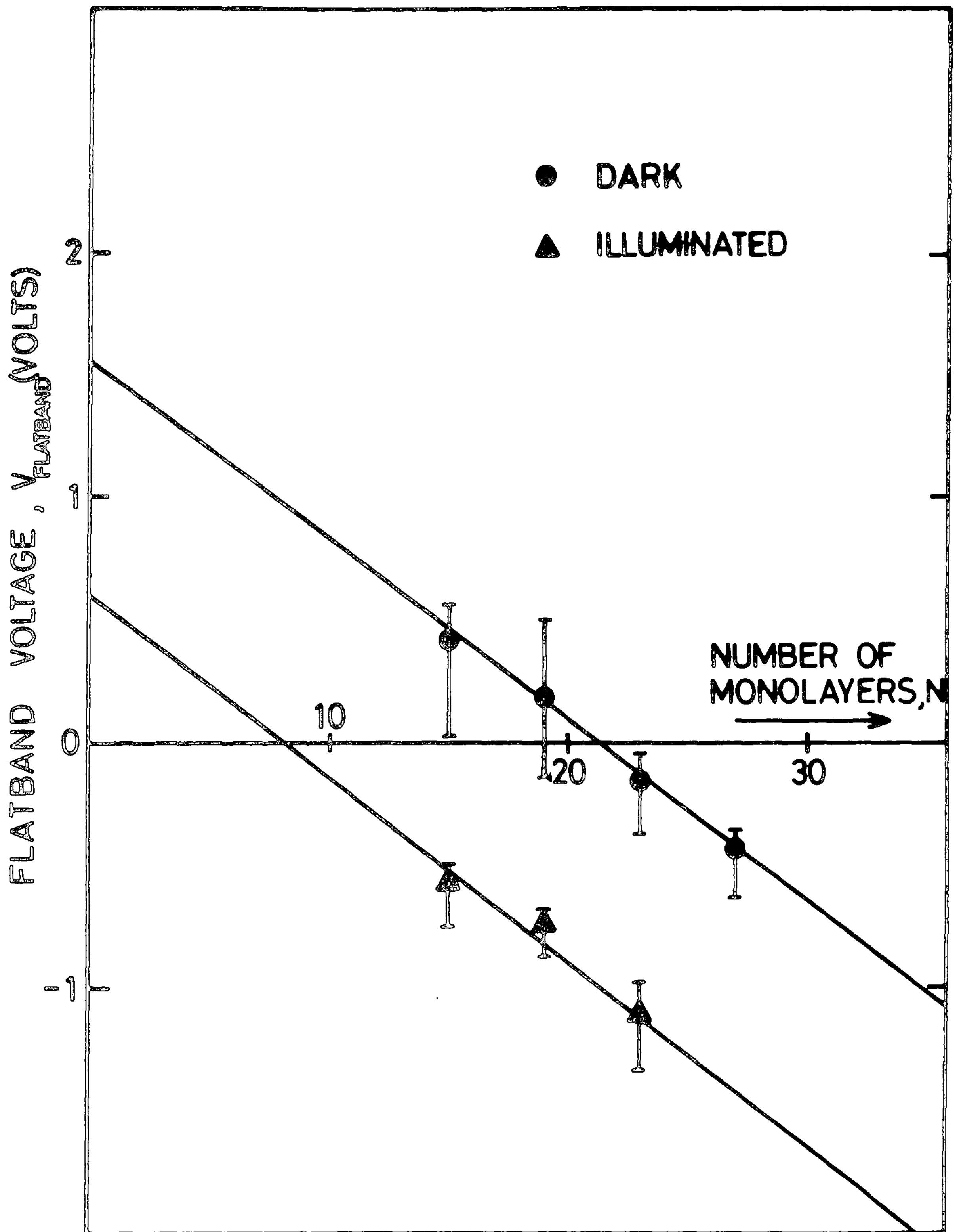


Fig. 9.9 Flatband voltage versus number of monolayers for the devices whose characteristics were shown earlier.

be 6.75×10^{-4} Cm^{-2}, which is equivalent to 4.2×10^{11} electronic charges (positive) per cm^2.

Turning to the intercepts of the two graphs, illumination causes a reduction in the intercept voltage from 1.56V to 0.6V. No quantitative conclusions can be drawn from the absolute magnitude of these intercepts because of the hysteresis in the C-V curves. Providing the same branch of the curves is used consistently, then this has no effect on the slope of the graph, but the errors in the intercept are unacceptably large. However, the difference in the intercepts of the two graphs is noteworthy. There could be three contributions to this reduction. Firstly, illumination will alter the densities of electrons and holes in the α-Si:H. Because the semiconductor film is only 1 μm thick, absorption will take place throughout the film, and will cause an effective change in ϕ_F. Thus, one would expect a change in the intercept. Secondly, the introduction of a centroid of net charge at a fixed distance from the metal/LB film interface could be taking place. In real terms this could be a charge distribution in the LB film or the 'oxide' or at the LB film/'oxide' interface. The third possible contribution could be from the formation of dipole layers. From these results alone it is not possible to distinguish which of these three mechanisms are in operation.

9.2.5 Changes in the Insulator Material

Diacetylene polymer was introduced and described in chapter 6. Because of its properties it may be a more realistic insulating material than cadmium stearate for incorporation into practical devices. Its use in tunnelling MIS structures was reported in the previous chapter. Preliminary measurements to assess the viability of diacetylene polymer in thick insulator MIS devices are discussed here.

Films of diacetylene monomer were deposited onto Dundee α-Si:H after the normal pre-deposition etch in the manner described in chapter 6. They were subsequently polymerised by exposure to ultra-violet light. The devices

were completed with ∿ 15 nm thick evaporated gold contacts, 0.5 mm in diameter. The admittance data of such a device incorporating 12 layers of diacetylene are shown in Fig. 9.10. These data were taken in the dark at a frequency of 11 Hz, using a 5 mV sec^{-1} bias voltage scan rate. The sample was held at + 2.5V bias for 20 minutes before ramping.

As in the case of cadmium stearate films on α-Si:H, the capacitance curve clearly shows regions of accumulation and depletion, and again suggests the presence of an inversion layer. The accumulation capacitance corresponds to the insulator capacitance within the limits of experimental error. It is interesting to note the appearance of two peaks in the conductance-voltage curve. An extra conductance peak can occur as a result of lateral conduction due to a surface inversion layer in the semiconductor. However, in our case, both peaks occur in the bias voltage range where the semiconductor is depleted. It is possible that the peaks could be due to two distinct, single-level traps (surface or bulk), or even two distributions of levels which are well separated in energy. The exact nature and origin of the conductance peaks bears further investigation. The characteristics are complicated by the presence of large hysteresis effects. The direction of the hysteresis is anticlockwise, as in α-Si:H devices utilising cadmium stearate LB films, and could be due to ion drift or polarisation. Since Kan et al[(3)] have reported admittance characteristics for diacetylene polymer MIS devices on single-crystal InP and GaP with minimal hysteresis, we must conclude that these effects are a property of the α-Si:H/LB film system. It could be that the diacetylene films on α-Si:H are generally of poorer structural quality than those on single crystal substrates, as seems to be the case for cadmium stearate: this in turn may result in an increased hysteresis. The sharply rising conductance at only 0.6V forward bias, which must be due to conduction through the film, would seem to support this idea.

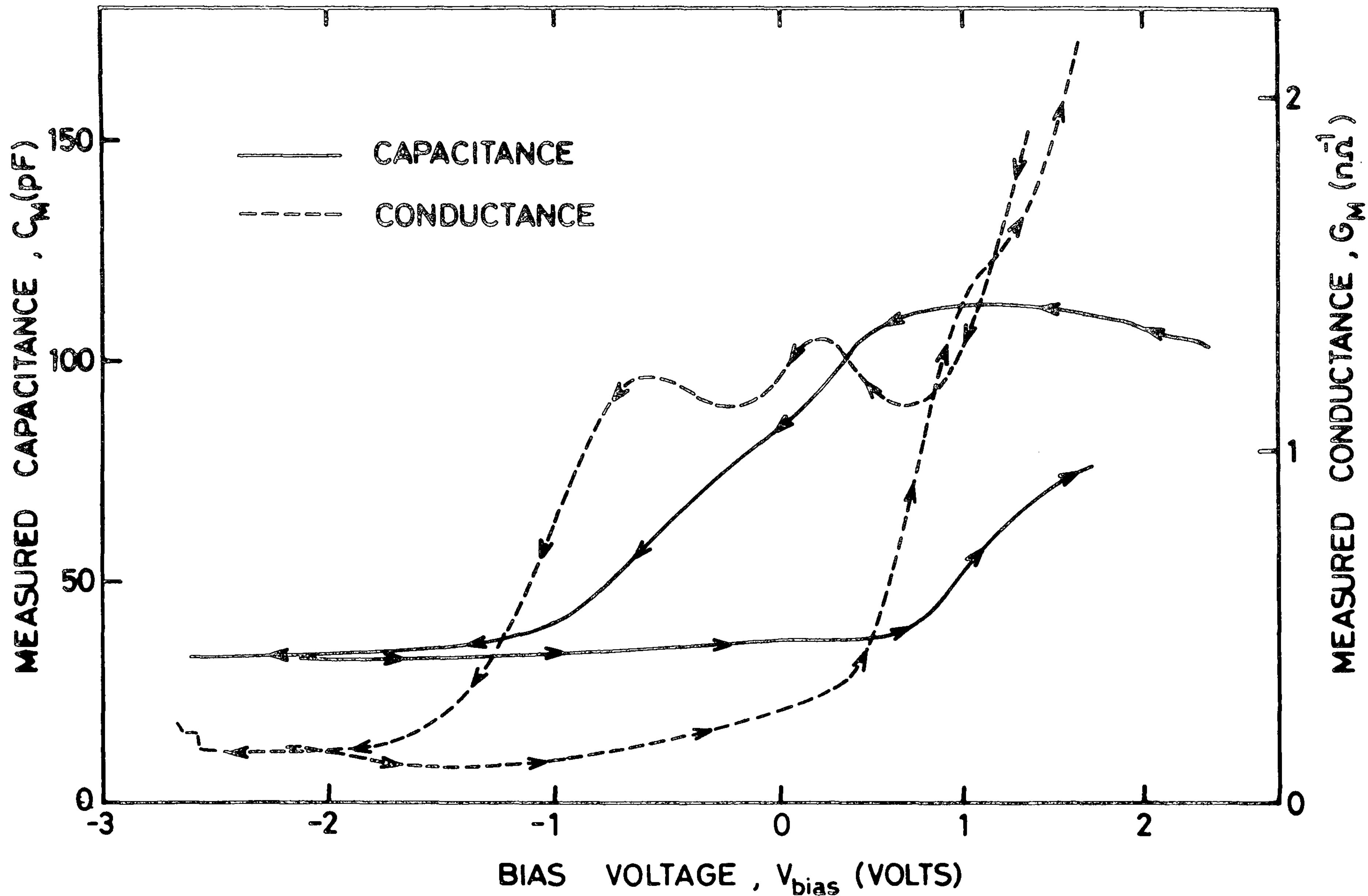


Fig. 9.10 Admittance-voltage data for an α-Si:H MIS device incorporating 12 monolayers of diacetylene polymer. Measuring frequency 11 Hz; voltage sweep rate 5 mV sec^{-1}.

Clearly, much work remains to be done before firm, positive conclusions can be drawn concerning devices of the type described here. Nevertheless, the preliminary results are reasonably encouraging.

9.2.6 Changes in the Measuring Frequency

(a) C-V curves

The effect of frequency on the C-V curve for the MIS device whose admittance characteristics were shown in Fig. 9.1, is given in Fig. 9.11. The measurements were made in the dark, and before recording each curve the device was biased into accumulation for approximately 20 minutes. The direction of the bias sweep is indicated by the arrows.

At the lowest frequency measured (3Hz) the accumulation capacitance, C_{accum}, is consistent with the geometrical capacitance of the insulating layer, within the limits of experimental error. Because of the rather large experimental error in the measured capacitance of $\pm$ 10%, the same could be said of several of the low frequency curves (up to a few tens of Hz). Since, however, the total capacitance of an MIS diode cannot exceed the insulator capacitance, the 3Hz curve must be taken as being the closest to true accumulation.

As the measuring frequency is increased the accumulation capacitance begins to fall. The rate of fall is fairly slow at first, but a sudden drop is observed at frequencies around 200 Hz. With further frequency increases, C_{accum} continues to drop until at about 1kHz the C-V curve is almost flat i.e. there is no increase in the device capacitance when biased into the 'accumulation region'.

There are three possible explanations of this frequency dispersion, each associated with a different part of the MIS diode.

(1) Frequency dispersion in the insulator could give rise to the effects seen in Fig. 9.11. This could equally well be in the LB film layer or in the interfacial 'oxide' layer on the semiconductor surface. As far as the

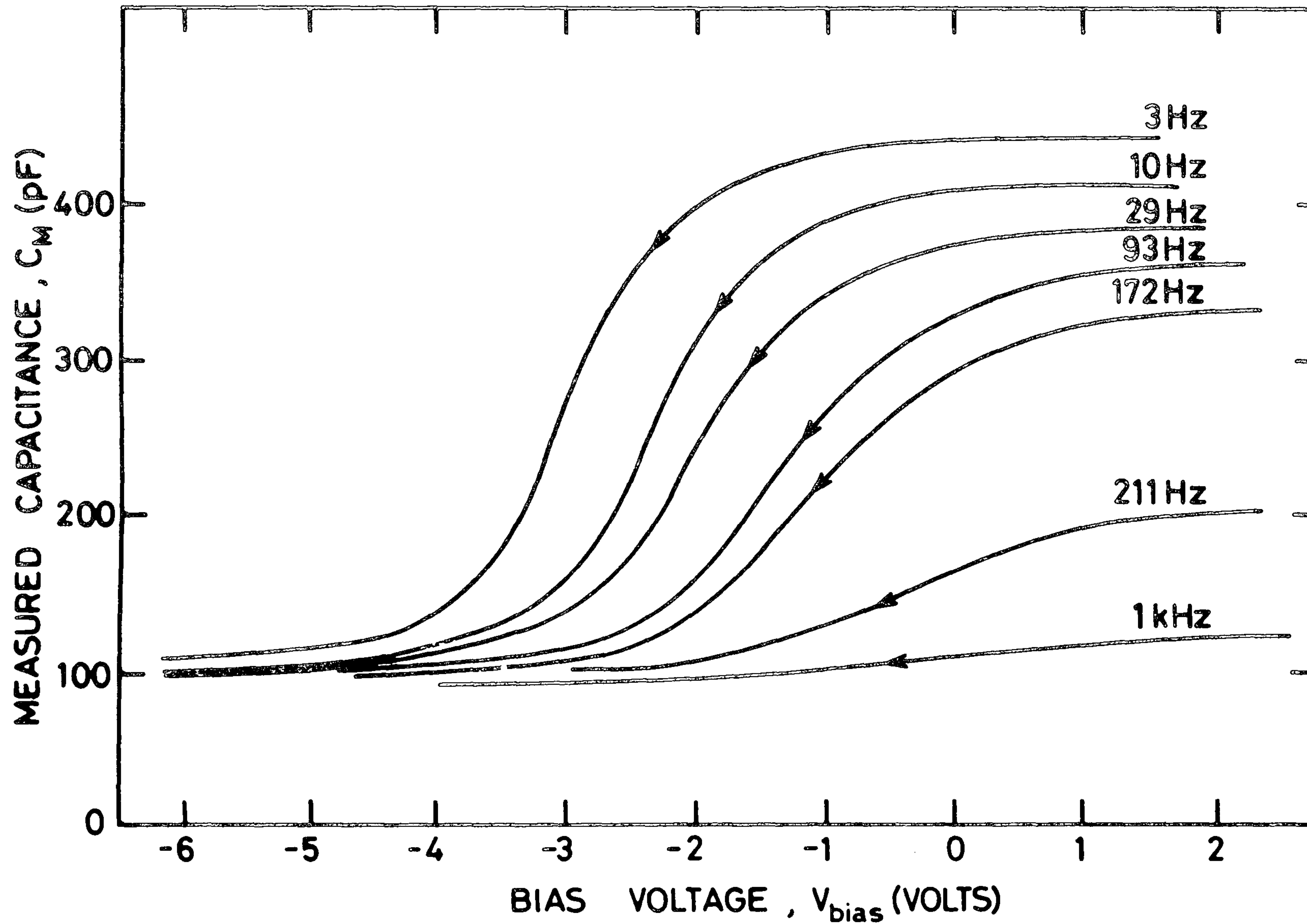


Fig. 9.11. The effect of frequency on the C-V curve of the device whose admittance characteristics were shown in Fig. 9.1.

LB film is concerned, this argument is almost certainly not applicable. Measurements performed with cadmium stearate LB films in both MIM and MIS structures[13,21] reveal no such dispersion in the measured capacitance throughout the frequency range under consideration. This approach will be further supported by other results to be discussed later in this section.
(2) Any frequency effects occurring in the semiconductor must affect the device capacitance, since it consists of the series combination of the insulator capacitance (C_{INS}) and the semiconductor capacitance (C_{SC}). It has been clearly demonstrated that α-Si:H has an electronic structure in which there is a distribution of localised states throughout the energy gap. The density and time constants of these states are both functions of the energy (see chapter 2). The space-charge in devices based on α-Si:H arises, not from uncompensated ionised impurity atoms, but largely from the charge in these localised states (see (22) and section 4.3.8). The response of these states is thus very important in determining the space-charge layer capacitance. The spectrum of state lifetimes leads to pronounced frequency effects (see for example (23,24)).

Turning now to the curves in Fig. 9.11 we note that in accumulation at 3Hz, $C_M = C_{INS}$, implying that the differential capacitance of the accumulation layer (C_{SC}) is very high ($C_{SC} \gg C_{INS}$). As the frequency increases, less and less of the gap states are able to respond and to contribute to the semiconductor capacitance[23, 24]: hence C_{SC} falls. This will affect the total measured capacitance, causing the observed reduction. Measurements on α-Si:H Schottky barriers[23, 24] also show that at a given frequency (10^3-10^4Hz) the capacitance saturates and equals the geometric capacitance of the α-Si:H. This agrees well with the data shown in Fig. 9.11 where the C-V curve is virtually flat at 1 kHz. This may be attributed to the saturation of the semiconductor capacitance (i.e. no gap states can respond) so that the device equivalent circuit becomes simply two voltage-independent capacitors in series (C_{INS} + the geometric semiconductor capacitance).

(3) Effects at the semiconductor/insulator interface could also be responsible for the observed frequency dispersion. Sawada and Hasegawa[25] have published very similar data to those shown in Fig. 9.11 for MOS devices on single crystal GaAs. Sykes et al[26], working on LB film/single crystal InP MIS devices, have reported the same phenomenon. The former authors have proposed a model which invokes the presence of an interface-state band (ISB) i.e. an anomalous, band-like, high density distribution of interface states at a certain position in the energy gap. This distribution does not pin the Fermi level, but rather limits the range of movement. The pseudo-accumulation and frequency dispersion which is observed is attributed to the partial filling of this band of interface states. This may be understood as follows. As the device is biased from depletion to accumulation the Fermi level effectively moves upwards through the bandgap at the semiconductor surface, and the capacitance changes with the band bending. At a given energy the Fermi level reaches the bottom of this interface state band (acceptor-like states in our case), and any further increases in bias are compensated for by changes in the occupancy of the states, i.e. by beginning to fill the band. The semiconductor surface region is thus unaffected by the bias voltage changes and hence the capacitance remains unaltered, as in genuine accumulation. The magnitude of this pseudo-accumulation capacitance depends on the frequency because the interface states have a certain lifetime, or even a distribution of lifetimes. Although this model seems to explain the experimental data in general, one feature casts doubt on its applicability, namely that at low frequencies $C_{accum} \sim C_{INS}$. It is thought that this would be unlikely to occur, even if all the interface states could respond to the signal.

(b) G-V curves

Changes in the frequency were found to have a large effect on the conductance peak observed in the G-V curves. This effect is shown in Fig. 9.12 for four different frequencies. The data were taken from the G-V curves recorded simultaneously with those in Fig. 9.11. The height of the peak

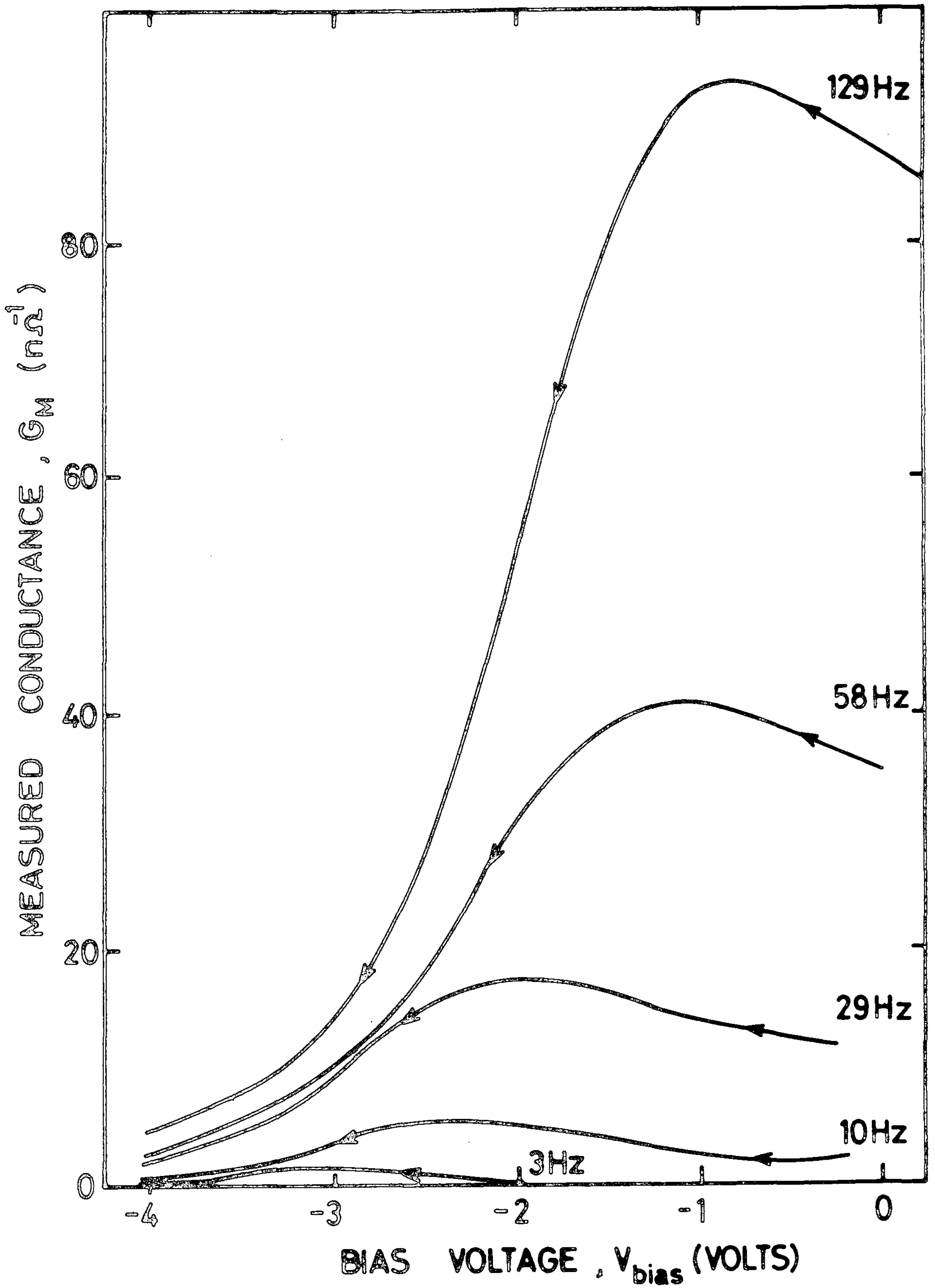


Fig. 9.12 The effect of frequency on the observed conductance peak. Data measured simultaneously with those shown in Fig. 9.11.

increases rapidly with rising frequency. The position of the peak is also shifted, moving to more negative voltages (i.e. towards 'inversion') as the frequency decreases.

The interpretation of this behaviour, which is quite often seen in conventional MIS work, follows that of Nicollian and Goetzberger[1]. They proposed that it was due to the existence of a distribution of energy levels, as opposed to a single level state. These states may be either bulk states (in the semiconductor) or interface states. This interpretation is quite consistent with the capacitance data. If the states are at the interface then this would seem to support the I.S.B. model. On the other hand the states may be within the semiconductor. In this context it is very interesting to note that the bulk density of states distribution, as measured by the field effect technique, has a distinct peak in it within the upper half of the bandgap, approximately 0.2 eV above E_F[27].

(c) Capacitance and Conductance in Accumulation

The overall effects of frequency are perhaps shown most clearly in Fig. 9.13. These capacitance and conductance data were measured in the dark, on the device whose characteristics were shown in Figs. 9.11 and 9.12. A bias of + 1.25V was applied to maintain the device in accumulation. Twenty minutes were allowed between each frequency step to allow equilibrium to be established.

Fig. 9.13 shows that, as discussed earlier, the frequency dispersion is not dominated by the properties of the LB film. A direct comparison may be made between Fig. 9.13 and the admittance-frequency data shown in Fig. 9.14 for a 5-layer $CdSt_2$ LB film in an MIM configuration. The a.c. characteristics of an LB film are a good indication of the film quality[13]. Normally, fatty acid films exhibit a conductance which varies as $G \propto \omega^n$ where $n \sim 0.9$[21]. The capacitance follows a $C \propto \omega^{1-n}$ law, so that in this case an $\omega^{0.1}$ dependence is observed[13]. When the

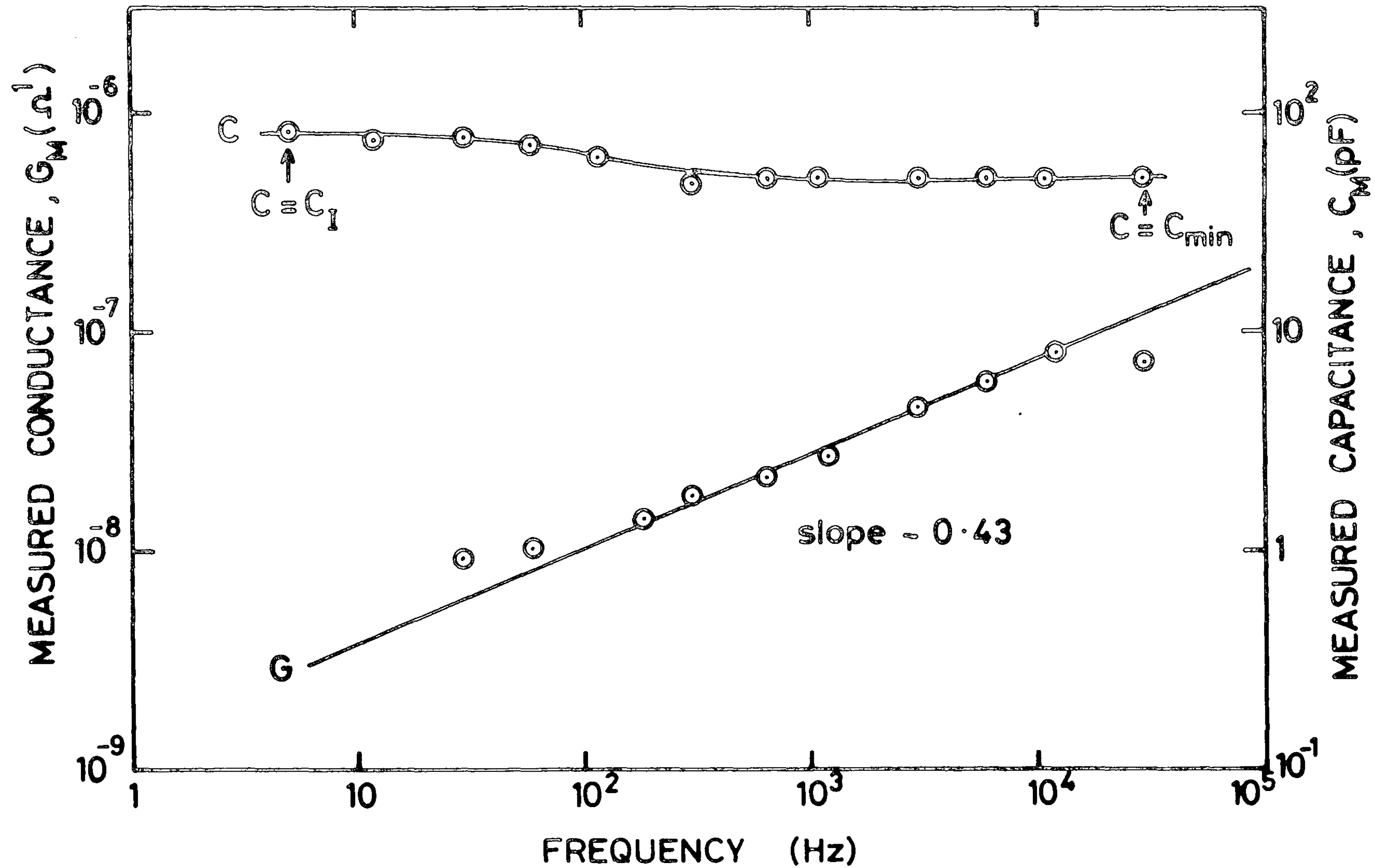


Fig. 9.13 The accumulation capacitance and conductance of the device whose admittance data were shown in Figs. 9.11 and 9.12. Measurements taken in the dark.

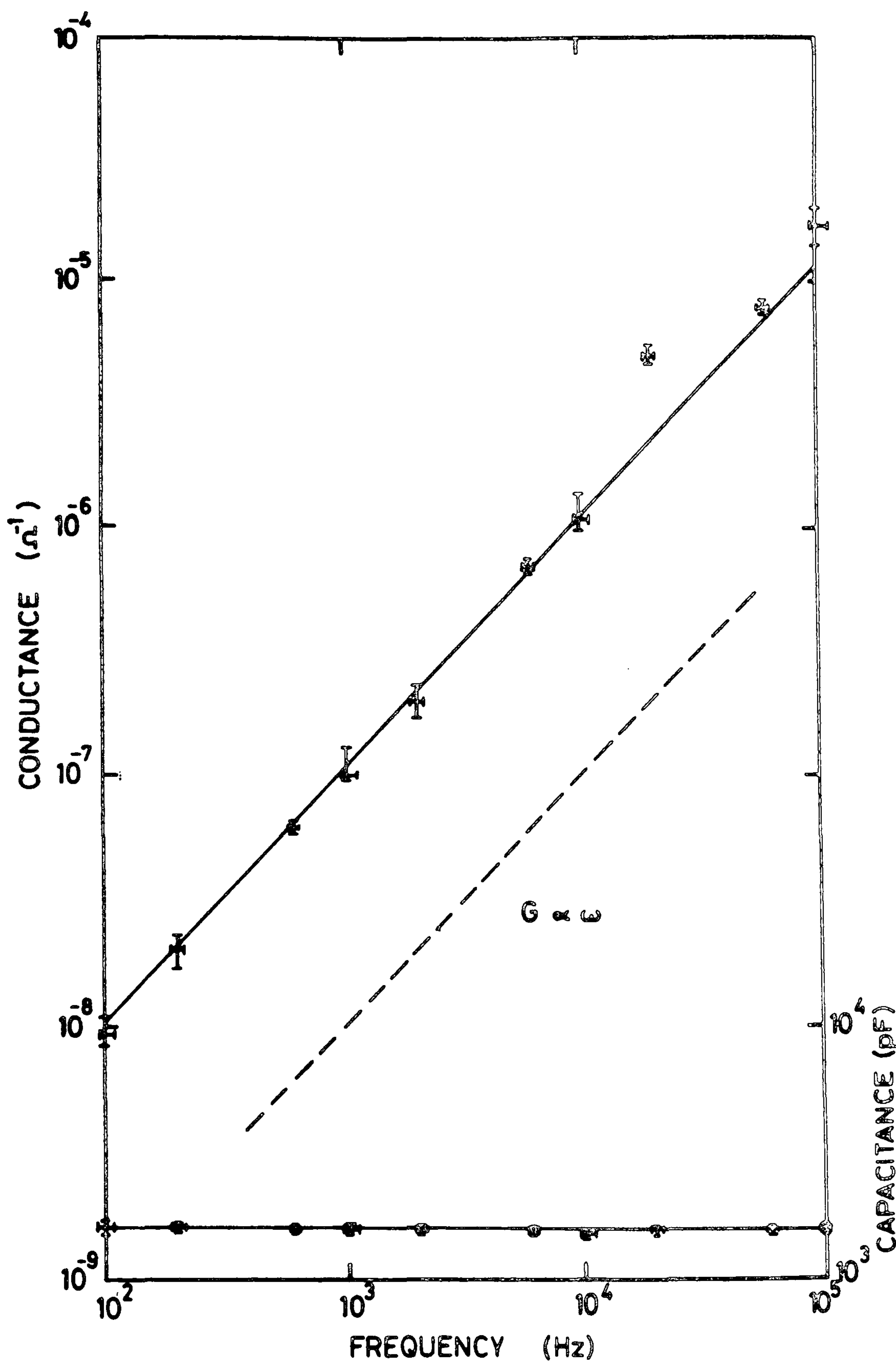


Fig. 9.14 Admittance-frequency data for an MIM structure incorporating 5 monolayers of cadmium stearate LB film. The contact metals were gold and aluminium, and the area was $\sim 8 \times 10^{-7}$ m^2.

film quality is poor, lower values of n are reported, corresponding to conduction through an increased density of defect sites[13,28]. Typically, n can be between 0.7 and 0.9. From Fig. 9.13, the slope of the conductance-frequency line gives n = 0.43. As well as being an exceptionally low figure, one would also expect to see a $C \propto \omega^{0.6}$ dependence. Since this is not so, it would suggest that the α-Si:H is playing a major role in determining the frequency dependence of the device characteristics.

9.2.7 Application of the Conductance Technique

It was originally intended to use the conductance technique of Nicollian and Goetzberger[1] to analyse the data in order to characterise the α-Si:H interface. During the course of the research it became apparent that there were a number of difficulties in doing this.

(1) The very large hysteresis associated with the admittance data makes it very difficult to ascertain the 'true' C-V and G-V curves of a device, and this is a major problem. According to Goetzberger et al[9] the evaluation of such data is difficult, if not impossible.

(2) The frequency dispersion is an added complication to any interpretation, since it demonstrates that the admittance characteristics are likely to be strongly influenced by the bulk α-Si:H, as well as the interface.

(3) The analysis of the data involves the calculation of the device parallel conductance, G_p. From chapter 4 we recall that this requires a measurement of the capacitance and conductance in accumulation to allow a correction for series resistance to be made. The value of the accumulation capacitance is reasonably well defined, being approximately equal to the insulator capacitance at low enough frequencies. However, there is a considerable uncertainty in the conductance value in accumulation. The sharp rise in conductance in forward bias makes it impossible to isolate the genuine accumulation conductance due to series resistance, which should be constant with bias.

Although a full analysis of the data was performed, it was decided subsequently that the application of the conductance technique and the use of the particular equivalent circuit associated with it was inappropriate, and that the errors involved were so large as to preclude any meaningful calculations.

9.3 D.C. Conductivity Data

Capacitance measurements are a useful tool for investigating the stacking of monolayers, but current-voltage characteristics provide a more rigorous test of the electrical qualities of a film. Figs. 9.15 and 9.16 show data for two different cadmium stearate film thicknesses on the same α-Si:H substrate, plotted as ln J v $V^{\frac{1}{4}}$ and ln J v $V^{\frac{1}{2}}$ respectively. The C-V characteristics of these devices were shown earlier in Fig. 9.6. Measurements were taken in the dark, at room temperature and atmospheric pressure.

The lower set of curves corresponds to the situation where a depletion region exists at the α-Si:H surface (metal top contact negative). By comparison with Fig. 9.6 we note that the sudden increase in slope in the 15-layer graph occurs at the same voltage as does the flattening out of the C-V curve. This may be further evidence for the formation of an inversion layer, with a consequent increase in the number of carriers available for transport through the insulator, although the change in slope was not observed in all devices (see 31 layer graph), and in some cases the slope decreased in this bias range. Whether the surface is depleted or inverted it is likely that the current through the device is limited by generation and recombination in the semiconductor space charge region, rather than by the insulator. As such , these curves are unlikely to provide a reliable indication of the mechanism of current flow through the LB film.

A reversal of the polarity of the applied bias gave rise to the upper set of curves, showing a general increase in the measured current. For bias voltages below + 0.5 V, when the semiconductor surfaces is not fully accumulated, this increase is not too large (approximately one order of

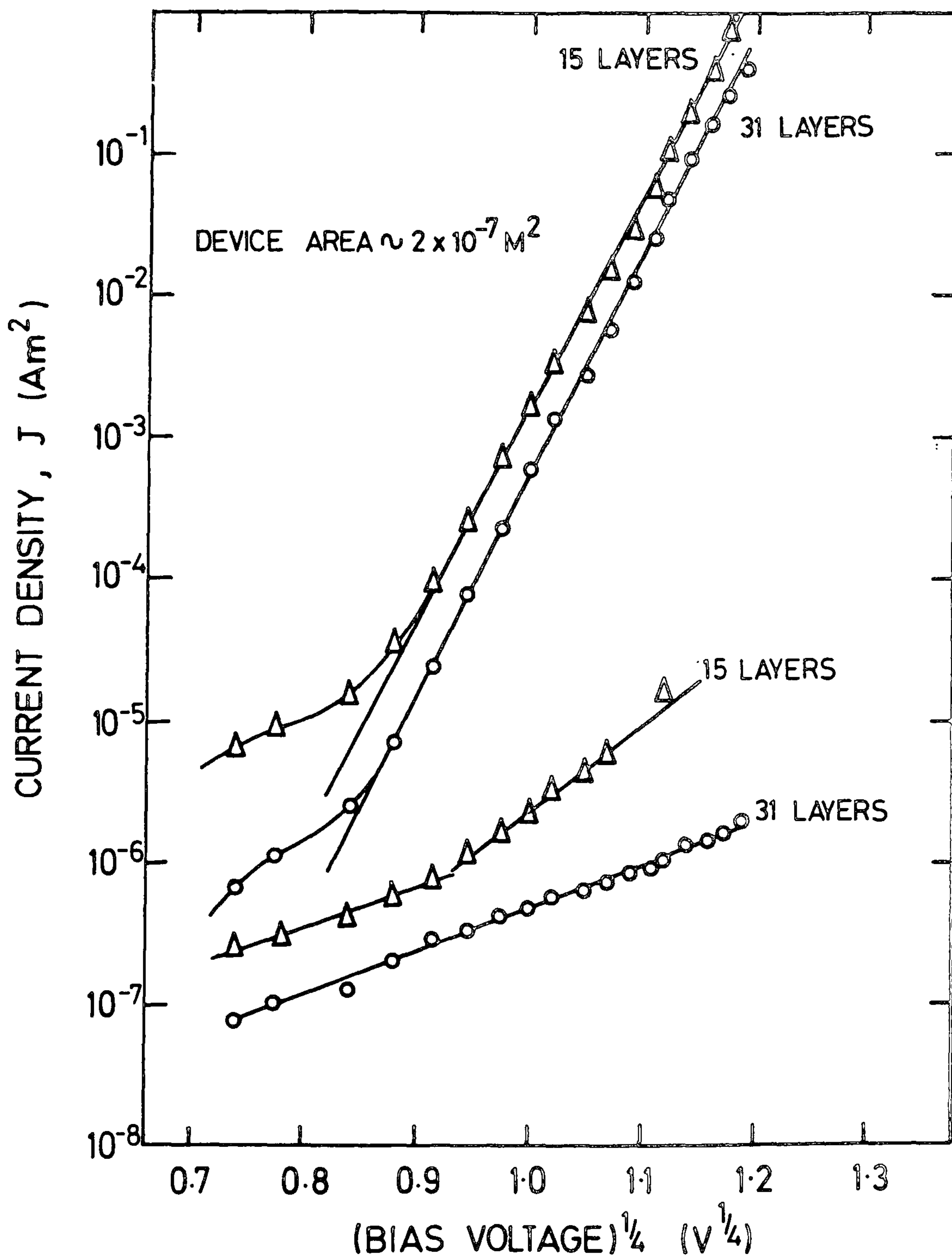


Fig. 9.15 Current density versus (bias voltage)$^{\frac{1}{4}}$ for devices containing two different LB film thicknesses (15 and 31 layers) on the same α-Si:H substrate. Device area 2 x 10^{-7} m^2. The lower set of curves is for negative bias on the metal top contact; for the upper set the polarity is reversed.

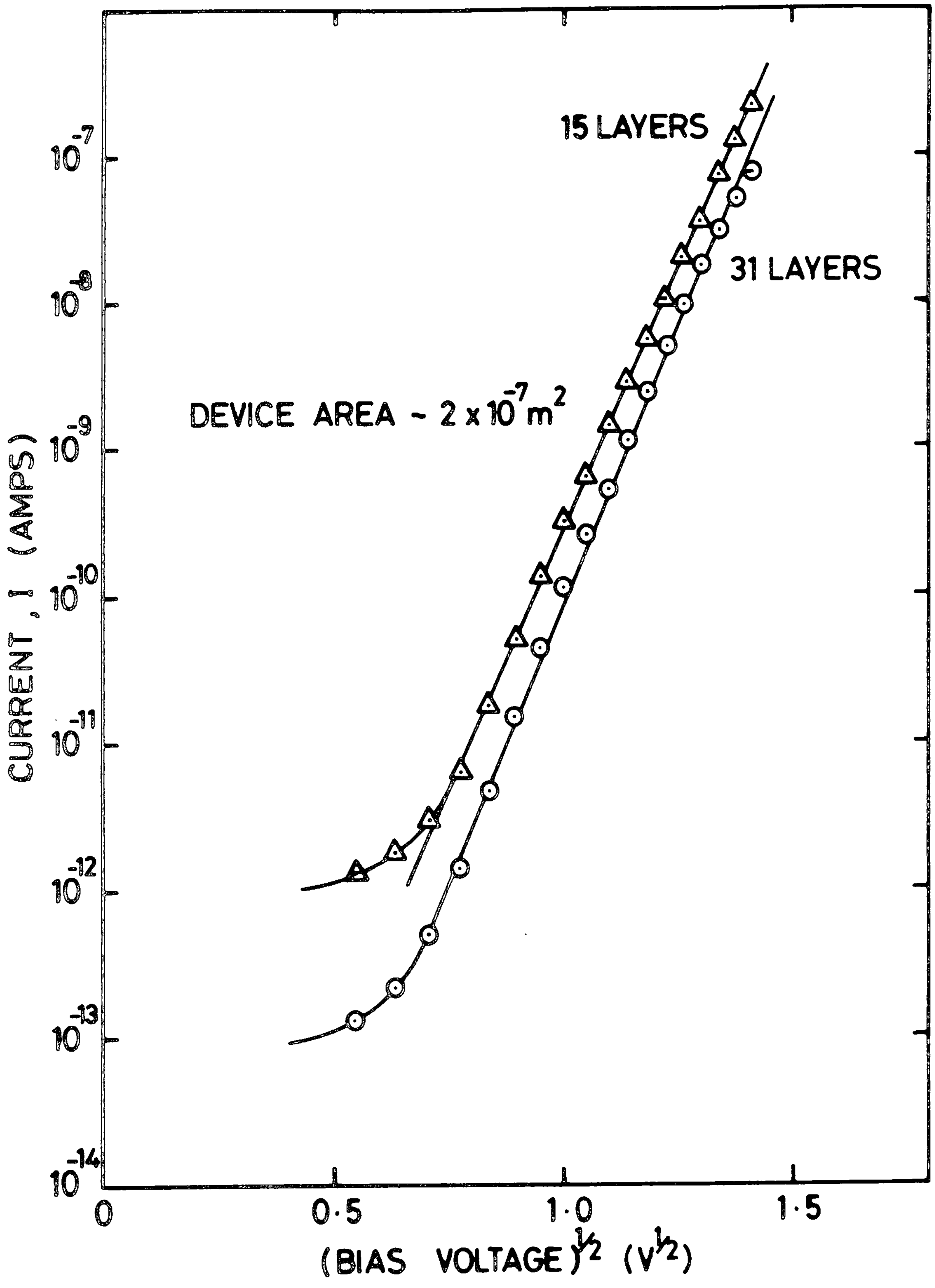


Fig. 9.16 The data as shown in Fig. 9.15 replotted as ln J v $V^{\frac{1}{2}}$.

magnitude). Indeed, in some devices this increase was not observed, and the current was independent of bias polarity in this range. When true accumulation was reached (bias voltage > + 0.5V) the current rose more rapidly with voltage. In this state the device may be thought of as more like an MIM structure, since there is a plentiful supply of carriers on both sides of the insulator, hence the current is more likely to be insulator limited. The data are plotted as $\ln J$ v $V^{\frac{1}{4}}$ and $\ln J$ v $V^{\frac{1}{2}}$ to demonstrate the difficulty of interpretation. The good straight-line fit obtained against $V^{\frac{1}{4}}$ is striking, although such a result is unusual for a multilayer LB film. The fit of the data plotted as $\ln J$ v $V^{\frac{1}{2}}$ is slightly poorer. The latter current-voltage relationship has, however, been reported by several authors for LB multilayer films[13,21], and has generally been interpreted in terms of Poole-Frenkel conduction. This mechanism is dependent on the electric field in the device according to

$$\ln J \propto E^{\frac{1}{2}} \tag{3.42}$$

and so, if the insulator thickness is doubled whilst the voltage is constant, the log of the current should fall by a factor of 0.7. This involves a change in current of several orders of magnitude. Such a scaling of current with insulator thickness is clearly not observed in Fig. 9.16. If the conduction mechanism was field dependent one would also expect a change in the slope of the $\log J$ v $V^{\frac{1}{2}}$ graph as the insulator thickness was varied. Again, this is not seen. Moreover, the slope of the lines give a large overestimate of the permittivity of the LB film (calculated using equation 3.41). In view of these anomalies, it would seem that Poole-Frenkel conduction is not applicable, and that a plot of $\ln J$ v $V^{\frac{1}{4}}$ provides the best fit to the data.

Although $\ln J$ v $V^{\frac{1}{4}}$ has not been observed before in a multilayer $CdSt_2$ LB film, it is not uncommon in other circumstances. Roberts et al[21] and Ginnai et al[29] have both reported this relationship for MIM structures

containing a single monolayer of cadmium stearate and barium stearate respectively. The latter authors have investigated the conduction mechanism in detail and conclude that tunnelling through the LB film is dominant. This explanation would seem to fit the data of Roberts et al[21] as well, since they found that the characteristics were independent of temperature in the range $-50^{o}C$ to $+50^{o}C$, which is strongly suggestive of tunnelling. Kampas and Gouterman[30] have noted ln J v $V^{\frac{1}{4}}$ behaviour in porphyrin films several hundred nanometers thick, sandwiched between two metal contacts (aluminium and silver). They have interpreted their results by assuming the presence of a Schottky barrier at both electrodes, and by attributing the current flow to image force effects[31]. The lowering of a barrier due to image forces has also been used to explain the reverse bias characteristics of Schottky diodes on single crystal semiconductors which show a ln J v $V^{\frac{1}{4}}$ dependence[32,33].

Since the temperature dependence of the J-V characteristics of the MIS diodes reported here was not investigated, the tunnelling model cannot be ruled out. However, it is highly unlikely that carrier tunnelling would be the dominant mechanism through a 31 layer LB film, even if the film quality was poor. The image force effect approach is, in the authors opinion, a more viable explanation. In the case where the semiconductor surface is accumulated there is no barrier at the semiconductor/'oxide' interface and the α-Si:H acts merely as a source of carriers. Any barrier must therefore be at the metal/LB film interface, or possibly at the LB film/'oxide' interface. When the bias voltage is reversed a potential barrier exists at the semiconductor/'oxide' interface (in depletion or accumulation). It was suggested earlier that the current in this situation was limited by generation and recombination in the semiconductor space charge region. An alternative explanation is that image force lowering of the barrier at this interface becomes dominant. Hence, the image force model can tentatively be used to interpret the ln J v $V^{\frac{1}{4}}$ graphs. Further work needs to be done to establish this with certainty.

9.4 Field Effect Transistor Results

The output characteristics of an α-Si:H depletion mode field effect transistor, incorporating a 31-layer $CdSt_2$ LB film, are shown in Fig. 9.17. Also shown is a schematic diagram of the device structure. The particular structure used in these preliminary investigations was chosen because of the simplicity of fabrication. It was found that, for the sample whose characteristics are shown in Fig. 9.17, LB film deposition could be achieved without the normal etching treatment : the sample was simply degreased in I.P.A. vapour. The LB film was thus deposited onto the surface 'oxide' layer which was present on the α-Si:H. The source and drain electrodes were chromium and the gate electrode consisted of a 10 nm thick aluminium strip. The source-drain separation (channel length) was 70 μm and the channel width was ∿ 2 mm. No hysteresis effects were observed during the measurement of the characteristics. On changing the gate voltage or the source-drain voltage the current settled to its equilibrium value within a few seconds. This would seem to indicate that the LB film is acting as a good insulator i.e. the leakage current is negligible. The graph clearly shows transistor action i.e. the modulation of the $\ln I_{SD}$ v V_{SD} curve by the application of a gate voltage. A gate voltage of about 10V has a significant effect on the current flowing in the device.

A more useful representation of these data, namely the transfer characteristics, is shown in Fig. 9.18. On the application of a gate voltage of 10V the source-drain current rises by almost three orders of magnitude. This increase in the conductivity of the channel is due to the formation of an accumulation layer (of electrons) at the surface of the α-Si:H. With increasing positive potential on the gate more electrons are drawn into the surface region and the bands are bent downwards so that (E_C-E_F) is reduced (E_C is the conduction band mobility edge). In contrast to single crystal FET's, the Fermi level in α-Si:H must move through a continuous density of localised states in the mobility gap. According to

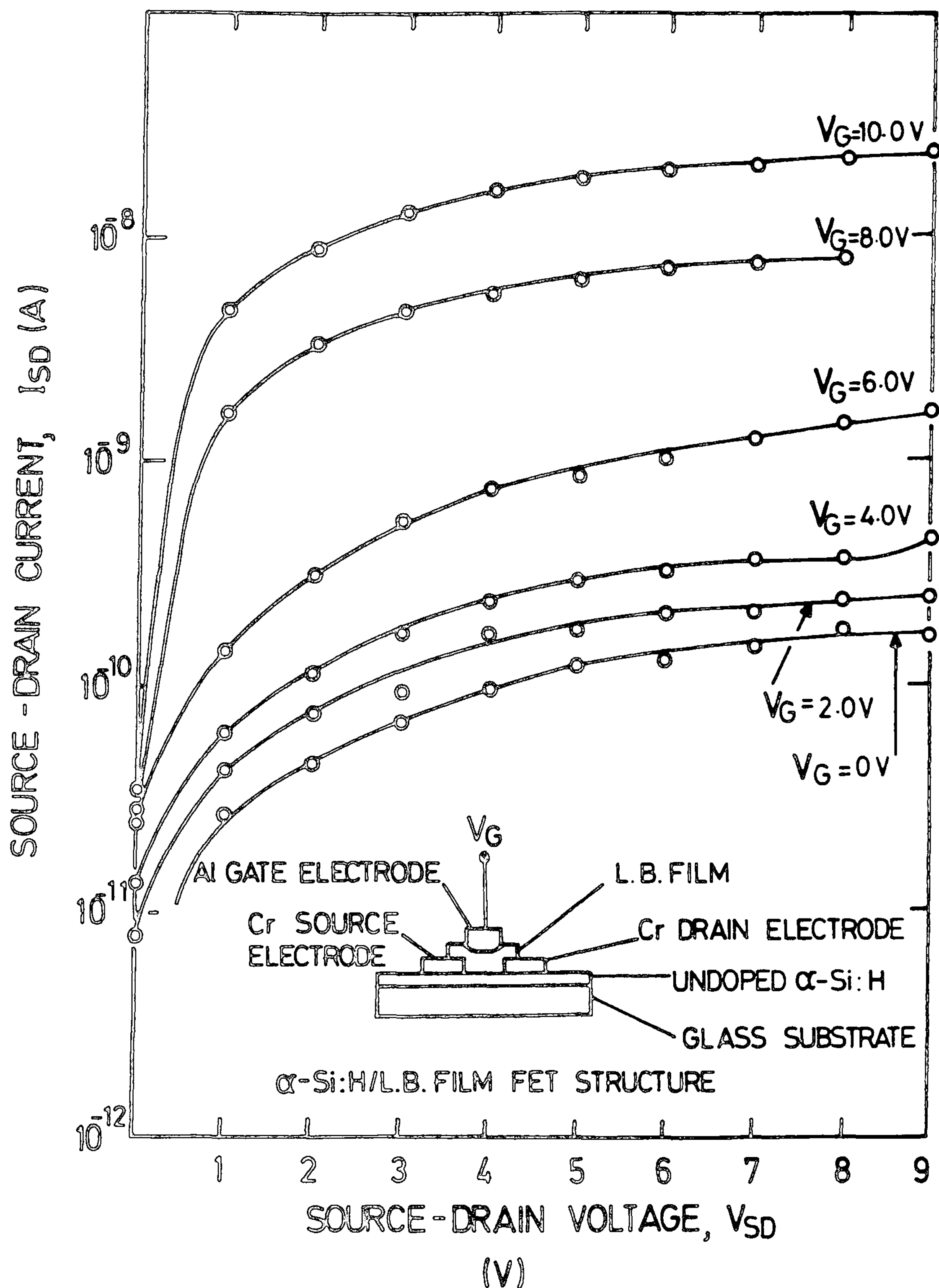


Fig. 9.17 Output characteristics of an α-Si:H FET with a 31-layer $CdSt_2$ LB film insulator. The device structure is shown schematically in the inset.

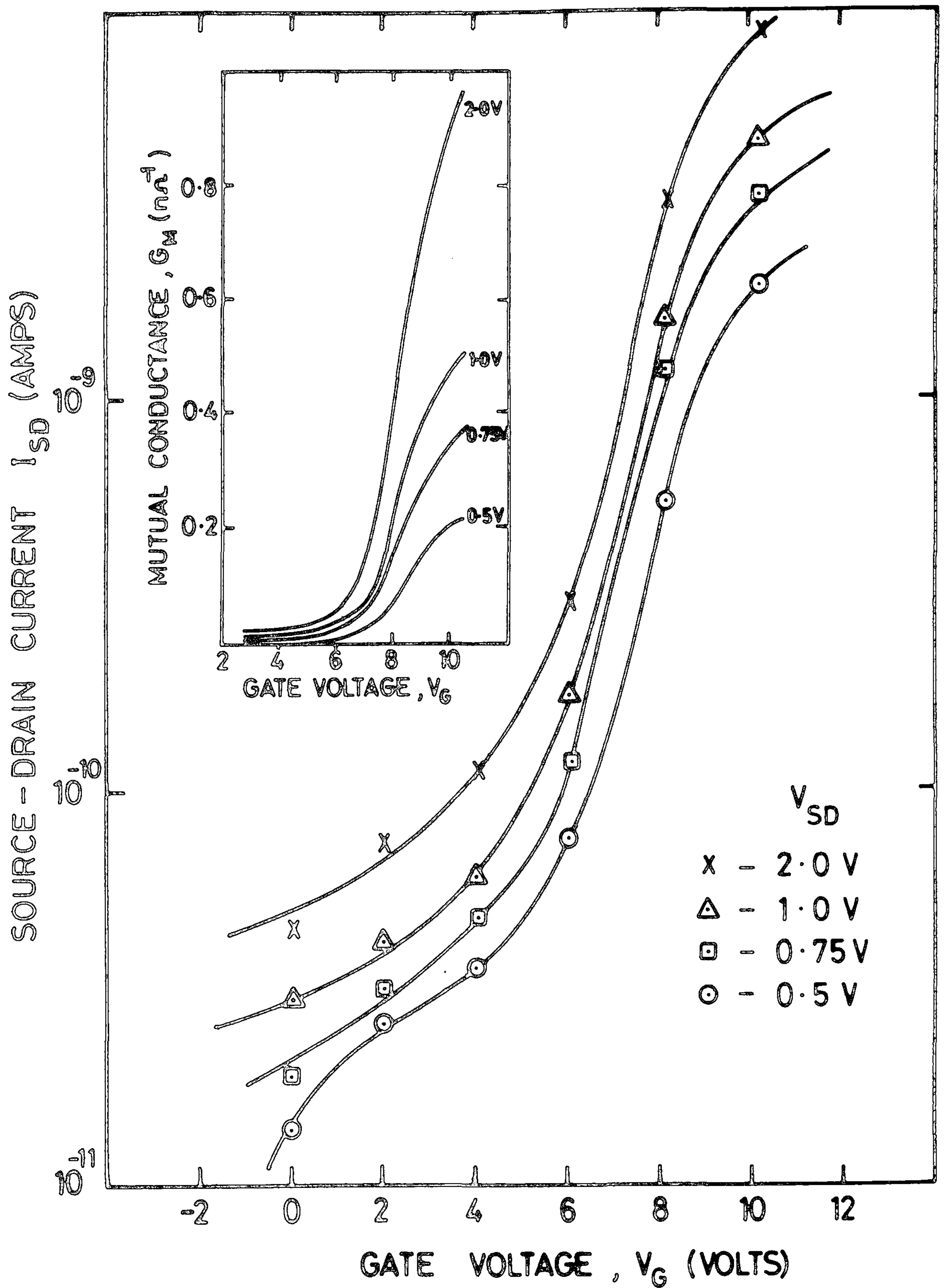


Fig. 9.18 Transfer characteristics of the FET whose output characteristics were shown in Fig. 9.17. The inset shows the transconductance of the device as a function of the gate voltage.

the measurements of Spear et al[24], using the field effect technique, the density of localised states increases rapidly as E_C is approached. This would explain the slower rise in I_{SD} observed at higher gate voltages, as it is more difficult to move the Fermi level through higher densities of states. The device characteristics may also be influenced by parasitic resistance associated with the source and drain contacts, both in their shape and in the absolute magnitude of the currents.

The transconductance of this particular device as a function of gate voltage is plotted as the inset to Fig. 9.18. The curves, obtained from the slope of the transfer characteristics, are shown for several values of source-drain voltage. A rapid rise occurs in g_M for gate voltages greater than the threshold voltage, V_T ($\sim$ 6V), as reported by Snell et al[34]. Using the standard equation for the transconductance of a field-effect transistor based on a crystalline material, an exceptionally low effective mobility, $\mu \sim 4 \times 10^{-4}$ cm^2 V^{-1} sec^{-1}, is obtained. The values reported in the literature generally lie between 0.1 and 0.4 cm^2 V^{-1} sec^{-1}. [34,35] A low mobility is to be expected, due to the amorphous nature of the semiconductor substrate and to the presence of interface states at the α-Si:H/ 'oxide' boundary. However, the calculated mobility in our case is so low as to cast doubt on the validity of applying the simplified FET equations. Certainly, it would seem that the poor semiconducting properties of the α-Si:H surface region are dominating the device characteristics. At the higher gate voltages measured the mutual conductance is observed to rise less rapidly than at threshold. However, there is no drastic flattening out of the curves which would occur if the source and drain contact resistances were significant. From this we may assume that parasitic resistive effects do not affect the device characteristics over the measured voltage ranges.

Overall the data presented here are slightly poorer, but comparable to the characteristics of the first reported α-Si:H FET's[36]. Although the

magnitude of the currents, the mutual conductance, and in particular the effective mobility are low when compared with recent results, the shape of the characteristics still agrees well with published data[34-38]. The reason our data are somewhat poorer would seem to be a fundamental difference in device design. Other research groups[34-38] have employed FET structures where the active region of the semiconductor is that part which was deposited first during the glow discharge process (see Fig. 9.19). The structure used here means that the α-Si:H formed at the end of the deposition process (when the system is being shut down) becomes the active region. It may well be that the properties of these two parts of the α-Si:H differ significantly. A further disadvantage in our case is the presence of the natural 'oxide' layer on the α-Si:H surface. In the other structures used the active α-Si:H surface is enclosed within the device, and so no 'oxide' can form. The occurence of this 'oxide' layer could result in an interface which is substantially different from that encountered by other workers e.g. the interface state density distribution may be different, there may be mobile and/or fixed charge in the oxide etc. Whatever the exact nature of the differences it is clear that they are detrimental to the device performance. Nevertheless, it has been demonstrated that viable FET's incorporating LB films can be fabricated on α-Si:H. It is reasonable to assume that alternative device geometries could lead to significant improvements in the observed characteristics.

9.5 Summary and Conclusions

The results presented in this chapter have dealt mainly with the investigation of non-tunnelling MIS structures. They may be summarised as follows.

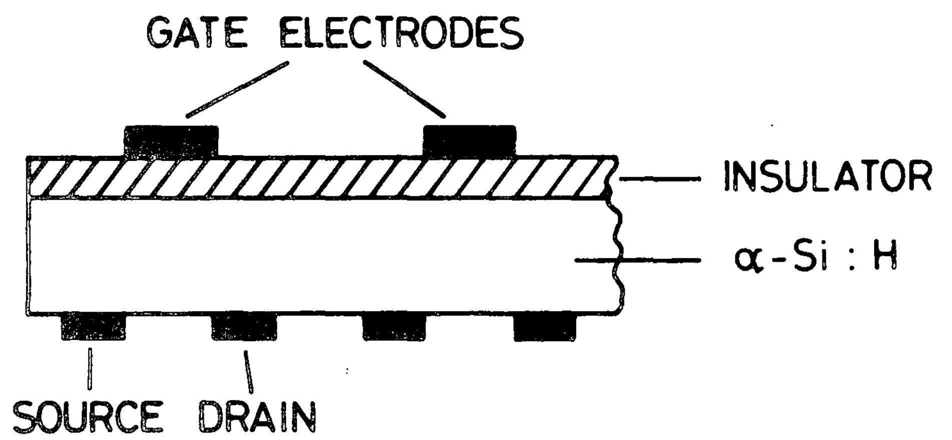


Fig. 9.19 Schematic diagram of the FET structure used by most researchers.

(1) It has been shown that the α-Si:H surface may be accumulated and depleted, and perhaps inverted. The ability to achieve this is important, since it is a pre-requisite for FET operation. Capacitance-voltage data (see Fig. 9.1) exhibit very similar features to those obtained for MIS devices on single crystal semiconductor substrates.

(2) Capacitance-voltage data have also been used to investigate the quality of the LB films (see Fig. 9.8). A dielectric thickness of 0.8 nm per monolayer was obtained for $CdSt_2$, which is low compared with other published data(13,16-18). The accumulation capacitance for devices incorporating different LB film thicknesses showed that the monolayers were stacking reasonably well. However, RHEED data reported in chapter 6 inferred that the overall order in the LB films was rather poorer than on single crystal semiconductors. This was supported by the observation of a rising conductance in forward bias, which denotes conduction through the film.

(3) The current-voltage characteristics (see Fig. 9.15) of these MIS devices were shown to follow a $\ln J$ v $V^{\frac{1}{4}}$ law, which has not been observed before in structures containing multilayer LB films. This unusual dependence has been tentatively attributed to image force effects.

(4) From capacitance data it was concluded that the α-Si:H surface was covered with an 'oxide' layer of dielectric thickness d_{ox}/ε_{ox} = 1.9 nm. This is equivalent to a 7.4 nm covering of SiO_2.

(5) The direction of the observed hysteresis showed the presence of ions in the insulator layer or of polarisation effects. The magnitude of the hysteresis was large, and hampered the interpretation of data.

(6) There was positive charge stored at the interface between the α-Si:H and the natural 'oxide' layer. Measurements of flatband voltage against the number of monolayers revealed a charge density of 4.2×10^{11} cm^{-2}. This may be fixed charge and/or interface state charge.

(7) The frequency dispersion encountered in both the capacitance-voltage curves (Fig. 9.11) and the conductance-voltage curves (Fig. 9.12) indicated the presence of a band of either surface or bulk states in the upper half of the α-Si:H bandgap. Unfortunately, the density of these states could not be measured, since hysteresis and insulator leakage made the application of the conductance technique impossible.

(8) Under illumination there was a voltage shift in the device admittance characteristics due to the storage of positive charge (or the removal of negative charge). The hysteresis was also reduced. This has been attributed to the neutralisation of ions, or to the screening of dipoles due to the increased surface charge density in the semicondcutor.

The studies undertaken have given some insight into the various processes occurring in these MIS diodes. Further clarification of the picture could be achieved with an extended range of experiments e.g. to investigate the temperature dependence of the J-V curves. Nonetheless, the MIS characteristics were sufficiently good to make the development of insulated gate field effect transistors worthwhile. This goal was achieved and from the device characteristics the following points may be noted.

(a) The transistor showed an increase in current of almost three orders of magnitude for a change in gate voltage of 10V.

(b) In general, the device characteristics were similar to those of the first reported α-Si:H FET's, but rather poor compared with more recently published data.

(c) The device properties seemed to be dominated by the poor semiconducting properties of the active region of the α-Si:H. This was compounded by the presence of an interfacial layer which may have resulted in an interface which was significantly different to those encountered by other workers using alternative FET configurations.

(d) It seems reasonable to predict that considerably better device characteristics could be achieved with α-Si:H/LB film FET's employing a different device geometry.

CHAPTER 10

CONCLUSIONS AND SUGGESTIONS FOR FURTHER WORK

An investigation into the use of Langmuir-Blodgett (LB) films in MIS devices based on undoped α-Si:H has been undertaken. Structures containing 'thick' i.e. non-tunnellable and 'thin' (tunnellable) insulators have been examined. As a first step, simple Schottky barriers (MS diodes) were fabricated. These diodes had characteristics which were comparable with those reported by many researchers i.e. they were 'state of the art' devices. Their properties have been explained in terms of currently available models. In order to deposit LB films onto the α-Si:H some surface treatment was required. Experiments showed that a buffered HF etch followed by washing in freshly prepared chlorine water led to successful deposition. Auger electron spectroscopy indicated that this left a partial coverage of chlorine atoms bonded to the α-Si:H surface. However, the treatment also adversely affected the Schottky diode performance : diodes made on 'treated' α-Si:H exhibited reduced rectification ratios, due to a reduction in the barrier height, ϕ_B. These 'treated' diodes formed the basis for comparison with the tunnelling MIS devices.

The studies of tunnelling MIS structures incorporating diacetylene polymer LB films revealed that, in general, successive monolayers were deposited reproducibly, and that their insulating properties were reasonable. The current-voltage characteristics of these diodes seemed to be dominated by surface state effects. An interfacial 'oxide' layer of about 40 Å thickness was left by the pre-deposition etch : this layer played an important role in determining the solar cell properties of the devices. Although the effect of increasing LB film thickness observed by other workers was clearly seen,

the 'oxide' layer proved to be greater than, or equal to, the thickness required for optimum efficiency. Nevertheless, the demonstration of this effect is important, and further work should result in the ability to optimise α-Si:H solar cell efficiency using LB films. This could be achieved by finding a pre-deposition etch which produces a thinner 'oxide' layer, or by using a different LB film material which does not require such a pre-deposition treatment. During the course of this work much progress has been made in the development of α-Si:H solar cells, particularly in Japan, and some cells are now commercially available. Despite this it is felt that further work on LB film/α-Si:H MIS solar cells is still worthwhile, since some of the unique benefits of this system remain unexplored e.g. the use of dye sensitising LB films which could increase the inherent efficiency of α-Si:H cells.

The main aim of the work on non-tunnelling MIS structures was to produce an α-Si:H/LB film FET. One possible application of such a device could be in switching large area arrays of liquid crystal display elements. In pursuit of this end a detailed investigation of thick insulator MIS diodes was performed. Firstly, it was shown that the α-Si:H surface could be accumulated, depleted and possibly inverted : the ability to achieve this is vital to FET operation. The quality of the cadmium stearate LB films incorporated in these diodes was somewhat poorer than is generally found when using single crystal semiconductors. The device current-voltage characteristics followed an unusual ln J v $V^{\frac{1}{4}}$ law, which has not been reported for multilayer LB films before. This was tentatively attributed to the effects of image forces. Measurements were complicated by the presence of hysteresis due to ion drift in the insulator or to polarisation effects. This meant that the measurements of the surface state density using the conductance technique, which had been planned, were impossible.

Nonetheless, the results were encouraging enough to continue the work to the production of an FET. It is worth noting at this point that even these simple MIS structures may have application, for example as gas detectors, where the penetration of gas molecules through the porous LB film could alter the device characteristics. This may well merit further research.

The characteristics of an α-Si:H/LB film FET, the first of its kind, have been presented here. The device characteristics compare reasonably well with those of the first reported α-Si:H FET's, which used conventional insulators, giving an increase in current of almost three orders of magnitude for a gate voltage of 10 V. The route towards improved performance would seem to be via a change in the device configuration, since the surface properties of the α-Si:H and the presence of an interfacial 'oxide' layer are thought to dominate the characteristics. Further work then is needed to investigate the various possible configurations, and to bring the performance of these devices up to the standard of the recently reported conventional insulator FET's. Although the competition to produce α-Si:H based display switching arrays is strong, another area of application is, in the author's opinion, more exciting and potentially more fruitful: that is, the field of biological sensors. With α-Si:H FET's incorporating LB films we have the possibility of tailoring the 'molecular nature' of the insulator. This could lead to highly specific sensors e.g. ion-sensitive FET's (ISFET's) or chemically sensitive FET's (CHEMFET's). The ability to deposit α-Si:H onto a wide range of substrates e.g. plastics, could also be useful. The α-Si:H/LB film system may perhaps form the basis of a variety of cheap, specific sensors for the medical diagnostic industry.

FIGURE CAPTIONS

Chapter 2

Fig. 2.1 Schematic diagram of gas phase deposition of an amorphous semiconductor using (a) inductive coupling of the r.f and (b) capacitive coupling. P is the plasma, S, the substrate and G is the gas flow direction.

Fig. 2.2 Radial distribution function of amorphous (evaporated) and crystalline silicon as determined from analysis of electron diffraction data (29).

Fig. 2.3 The 440-atom continuous random network built by Polk (31) to simulate the structure of α-Si or α-Ge.

Fig. 2.4 (a) Experimental arrangement for field-effect measurements.

(b) Variation of potential with distance x below the surface of the semiconductor. A charge +Q on the gate electrode induces -Q which, in the absence of surface states, is distributed throughout a space charge region λ either in gap states or in the bands.

Fig. 2.5 Various forms proposed for the density of states in amorphous semi-conductors. Localised states are shown shaded. (a) the CFO model (53), (b) a real gap in the density of states, as appropriate to an 'ideal' (defect free) material (c) the same as (b) but with a partially compensated band of defect levels (55), (d) the same as (b) but with overlapping bands of donor (E_y) and acceptor (E_x) levels arising from the same defect.

Fig. 2.6 Density of states g(ε) in amorphous silicon determined by the field effect technique (61). Curve 1: glow discharge α-Si:H deposited at 550K, Curve 2: glow discharge α-Si:H deposited at 350k. Curve 3: evaporated or sputtered α-Si.

Fig. 2.7 Variation of (a) room temperature conductivity σ (b) activation energy of conductivity (c) pre-exponential factor σ_o for glow discharge α-Si:H with deposition temperature T_d. Points on the left of this figure refer to evaporated films for which T_d has no real significance (after ref (6)).

Fig. 2.8 Temperature dependence of (a) electron drift mobility μ_D (b) conductivity σ in a glow discharge α-Si:H film deposited at 500K (85).

FIGURE CAPTIONS

Chapter 2 (cont)

Fig. 2.9 Room temperature conductivity of n- and p-type α-Si:H plotted as a function of the gaseous composition from which the films were deposited (10).

Fig. 2.10 Temperature dependence of Hall mobility for four n-type samples (1, 2, 5 and 7) and three p-type samples of glow discharge α-Si:H. The samples were prepared from silane containing the following p.p.m. of B_2H_6 (for the p-type films) and of PH_3 (for the n-type films): 0, 2.3 x 10^4; ∇Δ, 5 x 10^4; 1, 98; 2, 304; 5, 2 x 10^3; 7, 3 x 10^4. The solid curves are theoretical (88).

Fig. 2.11 Observed thermoelectric power S plotted as a function of reciprocal temperature for five n-type α-Si:H specimens. The sample numbers increase with increasing phosphorous content. The solid curves are theoretical (6).

Fig. 2.12 A.C. conductivity at 10^4Hz and 80K for various films of glow discharge deposited α-Si:H and α-Ge:H plotted against the density of states at the Fermi level ($N(E_F)$) determined from field effect data (95).

Fig. 2.13 Optical absorption edges in amorphous silicon prepared by different methods: (a) glow discharge films deposited from 500 to 600K; (b) glow-discharge films deposited at ∿300K; (c) and (f) sputtered films; (d) and (c) evaporated films; (g) annealed sputtered film (h) extrapolated edge for 'ideal' film (67).

Fig. 2.14 Spectral dependence of photoconductivity in glow-discharge films of α-Si:H deposited at the temperatures indicated. The ordinate represents the number of charge carriers flowing around the circuit per absorbed photon. α is the absorption of a film with T_d = 500K (67).

Fig. 2.15 Composite luminescence spectra of α-Si:H showing the four peaks which have been well characterised (103)

FIGURE CAPTIONS

Chapter 3

Fig. 3.1 Energy band diagram for metal - (n-type) semiconductor contact at thermal equilibrium.

Fig. 3.2 Spatial variation of (i) charge density (ii) electric field strength and (iii) electrostatic potential in a Schottky barrier. For an n-type semiconductor, ψ is negative and the electron potential energy ($-q\psi$) is positive.

Fig. 3.3 Transport processes in a forward-biased Schottky barrier.

Fig. 3.4 Typical J-V curve (schematic) showing the various bias regimes.

Fig. 3.5 Energy band diagram for a metal - n -α-Si:H Schottky barrier. The desnity of states is also shown. The hatched area represents the region of energy and space occupied by states that have been pulled above E_F at the barrier.

Fig. 3.6 The equivalent circuit for a Schottky barrier for capacitance-frequency measurements.

Fig. 3.7 C-w, G-w data as reported by Snell et al[19]. The solid curves are theoretical, the points are experimental.

Fig. 3.8 Theoretical and experimental capacitance-voltage data (denoted by solid lines and points respectively) see ref. (19).

Fig. 3.9 Frequency dependence of the capacitance for differently doped Schottky diodes (after Beichler et al (22)).

Fig. 3.10 C-V characteristics of an undoped α-Si:H Schottky diode at different frequencies (see ref. (22)).

Fig. 3.11 General equivalent circuit for an MIS device. In the case of a Schottky dioe C_I is infinite. Interaction between the states at the Fermi level and the conduction band is illustrated by the arrows in the partial energy-band schematic representation below the circuit diagram (after Viktorovitch (25)).

Fig. 3.12 Schematic representations of (a) the Schottky emission process and (b) the Poole-Frenkel emission process. CB denotes the bottom of the conduction band.

Fig. 3.13 Current-voltage characteristics (schematic) of a solar cell in the dark and under illumination.

Fig. 3.14 The equivalent circuit of a solar cell.

FIGURE CAPTIONS

Chapter 4

Fig. 4.1 Metal-insulator-semiconductor (MIS) diode (n-type)

Fig. 4.2 Energy-band diagram of an ideal MIS (n-type) diode at zero bias voltage.

Fig. 4.3 Energy-band diagrams for an MIS structure depicting (a) accumulation, (b) depletion, (c) inversion

Fig. 4.4 Band diagram of MIS diode in inversion showing the surface potential ψs.

Fig. 4.5 (a) Band diagram of MIS diode (inversion)
(b) Charge distribution
(c) Electric field
(d) Potential

Fig. 4.6 Idealised MIS Capacitance-voltage curves (n-type semiconductor).

Fig. 4.7 Device equivalent circuits incorporating surface state components (R_{ss}, C_{ss})

Fig. 4.8 Effect of fixed surface charge on MIS diode

Fig. 4.9 Hysteresis effects in an n-type MIS device (a) due to positive ion movement (b) negative ion movement.

Fig. 4.10 The effect of temperature variation on C-V curves

Fig. 4.11 Device equivalent circuit showing additional components to allow for substrate resistance.

Fig. 4.12 (a) Lateral a.c. flow pattern (b) Equivalent circuit (after ref. (13)).

Fig. 4.13 High and low frequency capacitance curves illustrating the effect of surface states.

Fig. 4.14 Comparison of MIS capacitance and conductance measurements at two frequencies (after ref (9)).

Fig. 4.15 Admittance characteristics of MIS structure and the corresponding equivalent circuits.

Fig. 4.16 Schematic diagram of a IGFET.

Fig. 4.17 Operating regions of an IGFET (a) linear region, (b) onset of saturation (c) pinch-off.

Fig. 4.18 Output characteristics of an n-channel enhancement mode IGFET.

Fig. 4.19 Output characteristics of an n-channel depletion mode IGFET

FIGURE CAPTIONS

Chapter 4 (cont)

Fig. 4.20 Typical TFT structure and drain characteristics

Fig. 4.21 Electrode configurations for TFT's.

FIGURE CAPTIONS

CHAPTER 5

Fig. 5.1 Dispersed molecules on a water surface (a) scattered molecules with their hydrophilic terminations in the aqueous subphase (b) the aligned molecules after compression.

Fig. 5.2 Representation of the chemical structure of stearic acid and its cadmium salt.

Fig. 5.3 Idealised compression isotherm for stearic acid

Fig. 5.4 Y-type monolayer deposition.

Fig. 5.5 Schematic diagram of a Langmuir Trough

Fig. 5.6 Photo of Durham trough

A : constant perimeter barrier system

B : glass trough

C : metal beams supporting barrier

D : toothed belt driving the barrier

E : dipping head

Fig. 5.7 Schematic diagram showing the relationship between the diacetylene fatty acid monolayer (left) and the corresponding polymer produced on u.v. irradiation (right)

Fig. 5.8 Variation of a.c. conductance with frequency for good quality film. Inset shows a typical capacitance plot for CdStearate/ stearic acid thick films.

FIGURE CAPTIONS

CHAPTER 6

Fig. 6.1 Schematic diagram of a sample chamber custom-built in the Departmental workshops.

Fig. 6.2 Schematic diagram of Oxford Instruments DN704 liquid nitrogen cryostat.

Fig. 6.3 Experimental arrangement for d.c. conductivity measurements

Fig. 6.4 Block diagram of admittance measurement system.

Fig. 6.5 Block diagram of Ortholoc 9502 p.s.d.

Fig. 6.6 Mixing circuit for a.c. and d.c. signals

Fig. 6.7 Circuit diagram of virtual earth amplifier.

Fig. 6.8 Virtual earth amplifier measurement configuration.

Fig. 6.9 Schematic diagram of FET measurement set-up.

Fig. 6.10 Energy band diagram illustrating the processes involved in Auger spectroscopy. The levels E_k etc. correspond to the binding energies of electrons measured from the vacuum level. The graph below indicates the number N(E) of electrons with kinetic energies betwen E and E + dE which will be measured in the electron energy distribution leaving the solid. The horizontal scale corresponds approximately to those commonly found in practical cases (after ref. (3)).

Fig. 6.11 Contact angle photographs.

(a) α-Si:H after refluxing in I.P.A.
(b) Single crystal Si after I.P.A. reflux + buffered HF.
(c) α-Si:H after I.P.A. reflux + buffered HF.
(d) α-Si:H after ultrasonic cleaning in Decon 90.

Fig. 6.12 Scanning Auger analysis on samples with three different preparation procedures.

(a) refluxed in I.P.A.
(b) refluxed in I.P.A. and etched in buffered HF.
(c) refluxed in I.P.A. and etched in buffered HF, then treated with chlorine water.

Fig. 6.13 RHEED micrographs

(a) α-Si:H substrate
(b) α-Si:H with 11 monolayers CdStearate
(c) single crystal InP with 11 monolayers CdStearate ({100} surface).

Fig. 6.14 Photograph of a completed sample showing α-Si:H/LB film MIS devices of varying insulator thicknesses.

FIGURE CAPTIONS

CHAPTER 7

Fig. 7.1 Forward and reverse current characteristics for Pd - n -αSi:H Schottky barrier measured in the dark at room temperature. Inset shows linear J-V plot for forward bias.

Fig. 7.2 Forward I-V curves at different temperatures for an Au-n-α - Si:H Schottky diode

Fig. 7.3 Graph showing the linear dependence of I on the forward bias at various temperatures for the device whose ln I-V characteristics were shown in Fig. 7.2.

Fig. 7.4 The capacitance and conductance as a function of frequency for the device whose J-V characteristics were shown in Fig. 7.1. Measurements taken in the dark, at room temperature. Inset shows equivalent circuit.

Fig. 7.5 Capacitance-frequency and conductance-frequency curves for a gold/α-Si:H Schottky barrier (after Snell et al, ref (6)).

Fig. 7.6 Capacitance-bias data at several frequencies for Pd-n αSi Schottky diode (Device 1, see Table 7.1) at room temperature in the dark.

Fig. 7.7 C(V) dependence of a metal/undoped α-Si:H diode (after Beichler et al, ref (19)).

Fig. 7.8 C(V) characteristics of a gold/undoped α-Si:H diode (after Viktorovitch and Jousee, ref (23)).

Fig. 7.9 $1/C^2$ v V_{bias} plotted for Device 1 at room temperature in the dark showing the departure from the theory applicable to single crystal Schottky barriers.

Fig. 7.10 Conductance-bias data corresponding to that shown in Fig. 7.6.

Fig. 7.11 Forward and reverse current-voltage characteristics for 'treated' and 'untreated' Au Schottky contacts measured in the dark at room temperature.

FIGURE CAPTIONS

Chapter 8

Fig. 8.1 Typical C-V characteristics for devices incorporating different numbers of LB film monolayers. Measurements taken in the dark. The bias was scanned from negative to positive at 10 m V sec^{-1}.

Fig. 8.2 Reciprocal capacitance v no. of monolayers for devices in accumulation under white light illumination. Error bars show the spread in measured capacitance over ten different contacts.

Fig. 8.3 Typical forward current-voltage characteristics for MIS devices with different thickness insulators. Readings taken in the dark under a low pressure of dry nitrogen. A typical reverse characteristic for a zero layer device is also shown for comparison.

Fig. 8.4 Capacitance-voltage characteristics of an α-Si:H MIS device incorporating 1 monolayer of diacetylene. The dark C-V curve appeared in Fig. 8.1. Measuring frequency 4Hz, illumination intensity 5 x 10^{-4} W cm^{-2}.

Fig. 8.5 Typical C-V characteristics under illumination for those devices whose dark C-V curves were shown in Fig. 8.1. The bias was scanned from negative to positive at 10 m V sec^{-1}. Illumination intensity 5 x 10^{-4} W cm^{-2}.

Fig. 8.6 Illuminated G-V curves corresponding to the C-V data shown in Fig. 8.5.

Fig. 8.7 Open circuit voltage and short circuit current measurements as a function of number of monolayers. Illumination intensity approximately 5 x 10^{-4} m W cm^{-2}.

Fig. 8.8 Illuminated I-V curves (15 m W cm^{-2} white light) for devices incorporating zero layers and two layers of diacetylene polymer. The two-layer device shows degraded solar cell operation.

Fig. 8.9 Variation in V_{oc} and I_{sc} with insulator thickness for MIS devices on single crystal CdTe. Data for two different substrates under AM1 illumination (after Roberts et al (38)).

Fig. 8.10 Variation in V_{oc} and I_{sc} with insulator thickness for MIS devices on Dundee α-Si:H, in ∿60 m W cm^{-2} simulated sunlight (after Wilson and McGill (12)).

FIGURE CAPTIONS

Chapter 9

Fig. 9.1 Measured values of capacitance and conductance at 29Hz for an undoped α-Si:H/$CdSt_2$ capacitor (31 monolayers of $CdSt_2$; device area 1.5 x 10^{-6} m^2; voltage sweep rate 5 m V sec^{-1})

Fig. 9.2 Capacitance and conductance data as in Fig. 9.1 but showing the effects of hysteresis. Direction of voltage sweep as shown by arrows.

Fig. 9.3 Effect of bias voltage sweep rate on the observed hysteresis in the capacitance and conductance. Sweep rates and directions as shown : measuring frequency 29 Hz.

Fig. 9.4 Effect of bias voltage scan width on the magnitude of the hysteresis in the capacitance. Single arrows: +2V → +1V → +2V sweep. Double arrows: +2V →0V→ +2V sweep. Triple arrows: +2V→ -1V→ +2V sweep. The dotted curve shows the corresponding conductance-voltage characteristic.

Fig. 9.5 Schematic diagrams showing the ionic movement which could lead to hysteresis with positive ions (a and b) or negative ions (c and d).

Fig. 9.6 Typical C-V curves for Au/$CdSt_2$/α-Si:H MIS devices incorporating 11, 15 and 23 monolayers of cadmium stearate. Measurements taken at 4Hz, in the dark.

Fig. 9.7 Illuminated C-V curves corresponding to those shown in Fig. 9.6.

Fig. 9.8 Reciprocal capacitance versus number of monolayers for devices on the same substrate as those who C-V characteristics were shown in Figs. 9.6 and 9.7.

Fig. 9.9 Flatband voltage versus number of monolayers for the devices whose characteristics were shown earlier.

Fig. 9.10 Admittance-voltage data for an α-Si:H MIS device incorporating 12 monolayers of diacetylene polymer. Measuring frequency 11 Hz; voltage sweep rate 5 m V sec^{-1}.

Fig. 9.11 The effect of frequency on the C-V curve of the device whose admittance characteristics were shown in Fig. 9.1.

Fig. 9.12 The effect of frequency on the observed conductance peak. Data measured simultaneously with those shown in Fig. 9.11.

Fig. 9.13 The accumulation capacitance and conductance of the device whose admittance data were shown in Figs. 9.11 and 9.12. Measurements taken in the dark.

Fig. 9.15 Current density versus (bias voltage)$^{\frac{1}{4}}$ for devices containing two different LB film thicknesses (15 and 31 layers) on the same α-Si:H substrate. Device area 2 x 10^{-7} m^2. The lower set of curves is for negative bias on the metal top contact; for the upper set the polarity is reversed.

FIGURE CAPTIONS

Chapter 9 (Cont.)

Fig. 9.16 The data as shown in Fig. 9.15 replotted as ln J v $V^{\frac{1}{2}}$.

Fig. 9.17 Output characteristics of an α-Si:H FET with a 31-layer $CdSt_2$ LB film insulator. The device structure is shown schematically in the inset.

Fig. 9.18 Transfer characteristics of the FET whose output characteristics were shown in Fig. 9.17. The inset shows the transconductance of the device as a function of the gate voltage.

Fig. 9.19 Schematic diagram of the FET structure used by most researchers.

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