Operation of Grid-Connected Inverter under Unbalanced Grid Conditions Using Indirect Voltage Sensoring

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Declaration

No part of this thesis has been submitted elsewhere for any other degree or qualification and it is all my own work unless referenced to the contrary in the text.

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Abstract

The grid connected voltage source inverter is now the most widely used interface for connecting renewable power generation to the grid. Control of this device is a key aspect to ensure the performance, reliability and life span of the renewable power generation system.

Conventionally, the current control of the grid connected inverter is based on the measured grid side voltage. The power and the power factor at the receiving end, which is usually defined as the point of common coupling, can be controlled accurately. This controller topology has been widely used and many control methods have been developed aiming at objectives such as increasing system stability, decreasing harmonic injection, and improving transient response of the system. However, in case of the voltage measurement is not available, i.e. a faulty voltage sensor, the conventional current control topology will be disabled for lack of information of the grid voltage. This would decrease the reliability and efficiency of the system thus should be improved.

voltage-sensor-less In this research, a current control system for the grid connected inverter system not relying on the information provided by the a.c. side voltage sensors will be developed with compliance to the recommendations issued to the performances of the distribution generations such as the harmonic limitations and the fault-ride-through capabilities. Three problem will be addressed and solved.

Firstly, the a.c. side voltage should be acquired without the use of a.c. side voltage sensors. This is achieved by adopting an a.c. side voltage estimation algorithm. Secondly, the grid connected inverter should be able to start-up without synchronising to the grid while keep the current injected in a safe range. This is achieved by the newly designed start-up process. Thirdly, the grid connected inverter should be able to ride-through grid faults and providing

support to the grid. The transient response of the grid connected inverter is the key measure to define the performance. In this study, a faster symmetrical component decomposition method is proposed to improve the transient response of the current control, without relying on grid voltage sensors.

The proposed system is verified by both simulation and experimental tests, with analyses and insight aiming at general applications of the proposed method and algorithms.

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Nomenclature

f	Frequency
i	Current
P	Real power
Q	Reactive power
R	Resistance
v	Voltage
ξ	Damping-ratio
ω	Angular velocity

List of Abbreviation

a.c.	Alternating Current
d.c.	Direct Current
dq	Direct-Quadrature
DD SRF-PLL	Decoupled-Double Synchronous-Frame-Phase-Locked-Loop
IAE	Integral of Absolute Error
IGBT	Insulated-Gate Bipolar Transistor
MPPT	Maximum Power Point Tracking
PCC	Point of Common Coupling
PI	Proportional-Integral
PR	Proportional-Resonant
PLL	Phase-Locked-Loop
PWM	Pulse-Width-Modulation
VAR	Volt-Ampere Reactive
HVDC	High Voltage Direct Current

Chapter 1 Introduction

1.1 Motivation of the research

It is a relatively familiar but still on-going topic that human activities are changing the global climate particularly due to the emission of carbine-dioxide (CO_2) associated with the large scale energy production using fossil fuels [1, 2]. The traditional electrical power systems are largely dependent on centralized power generation stations using systems such as gas turbines and steam turbines which contribute majority of the green-house gas emissions [3]. Arguably cleaner, but also large hydro power stations and nuclear power plants are used but this is not always possible and they can still cause different kinds of environmental and social-economic issues. Strictly speaking, none of the commercial electrical power generation technologies is carbon free because of the carbon footprint associated with the manufacturing and maintenance of the technical system, but given the expected lifetime of a system in 20-50 years the systems using renewable rather than fossil fuel resources are of much lower carbon footprint [4]. Figure 1.1 shows the typical values of CO_2 emission for different types of technologies for generating 1 kWhr electricity levellized over their respective lifetimes [5].

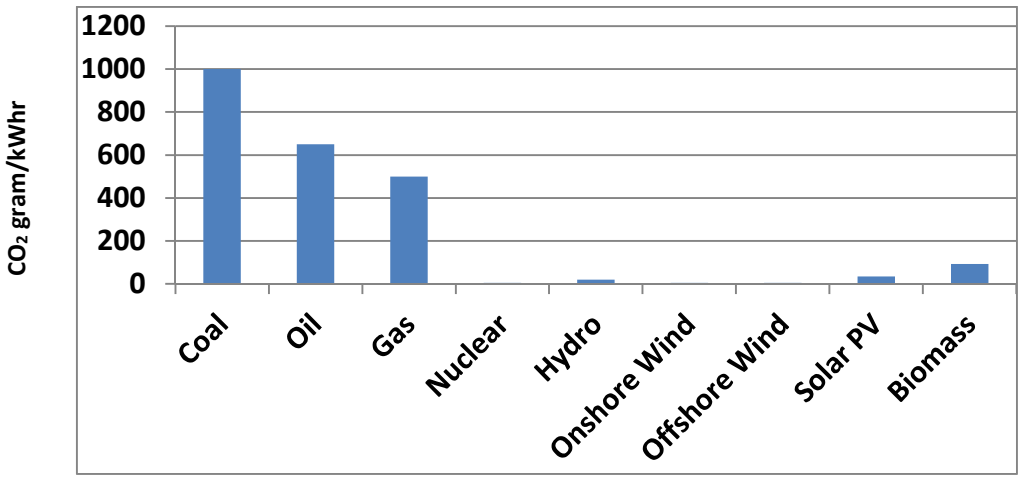


Figure 1.1 Carbon footprint of electricity generation

The power generated from the relatively large and dispatch-able power sources is transmitted and then distributed through the power networks or grids. This is regarded as the conventional configuration of the power systems before the rise of the cleaner generation technologies which are usually less dispatch-able because of the random variations of the primary resources. Wind turbines, solar panels and tidal energy devices as well as CHPs (combined heat and power) using biomass fuels are reshaping the electrical power industry in terms of the grid configurations and the relationships between the energy providers and consumers [6-10].

To constrain the emissions, more and more generation is now provided by renewable generators which are directly connected to the grid including the distribution networks. It attracts investment because of the environmental protection and economic reasons which have influenced the government policies as exemplified by numerous subsidy schemes all over the world [11]. Many clean energy generation systems could be installed domestically, such as solar panels and small scale wind turbines to harvest the locally available resources. This situation allows the microgrid operation mode in which the generated power can be utilized locally to give direct economic incentive and the customers are less likely to suffer from a loss of supply caused by outages in the traditionally upstream systems. Also the owners of the generators are usually interested in selling the additional power or energy generated to the grid to make a direct income. The grid interfaces are usually through a power electronics stage. However, the rise of distributed generation not only brings about opportunities but also presents challenges to the management and stability of the existing power systems. Stringent requirements are being proposed by the transmission and distribution network operators as will be illustrated in the following sections.

Partially because of the random variation of the primary resources, renewable power generation systems are usually interfaced to the grid through power electronic converters as shown in Figure 1.2. Power electronics which uses power semiconductors to convert electrical power

from one form to another can establish a variable condition for the generator and also suit the more fixed frequency and voltage of the a.c. grid. Until recently, power electronics has been predominantly used for loads such as motor drives, lighting a switched mode power supplies (SMPS). In pure grid applications, power electronics has been mainly used for HVDC (high voltage d.c.) transmission [12-15], static VAr compensation (SVC) [16], active filtering [17-19] and some presently miscellaneous applications including solid state fault current limiting [20], on-load transformer tap changing and seamless supply transferring [21].

Although the system configuration shown in Figure 2 is apparently a reverse of a typical load system, the requirements would inherently be different for a generation technology to a load technology. In addition to the technical challenges which are to be discussed in the following sections, reliability and cost are also important issues given that the investors would naturally expect short payback times and the power electronic converters are expected to work for a long time in environments which are not easily accessible to professional engineers. These are some of the key issues and the study of this thesis was planned in such a context.

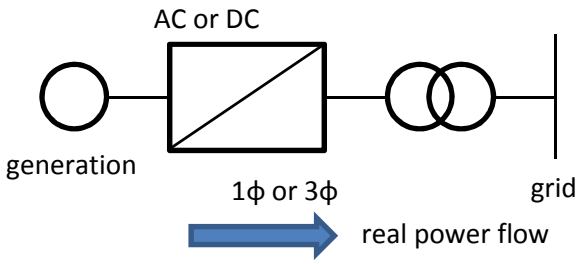


Figure 1.2 General layout of renewable generation system

1.2 Technical challenges

Increasing Increasing the penetration level of distributed generation is one of the top interests among researchers and the power industry. As implied before, the rise is driven by, firstly the interest of increasing the power generation from non-fossil fuels such as renewable resources,

which is desirable from an environment protection point of view; secondly, the benefit from the changed role of the consumers to participators, which injects dynamism into the market; thirdly, increasing the overall efficiency of the existing power system, which could potentially benefit the network owners and operators. However, the power distribution network is a relatively weak system where voltage fluctuation and frequency variation (when in a microgid operating mode) can happen easily [22]. Fault level contribution of distributed generation has recently become another issue in some systems particularly urban distribution networks where the power density in MW/km^2 is high [23]. Furthermore, the concerns about the availability and reliability of distributed generation never fade away in the mind of all players involved in the power industry. Apart from the numerous methods that aim at increasing the distribution network robustness, the quality of the control of the distributed generation devices directly affects the stability of the system.

It was a quite simple role that the renewable generation used to play in the distant past: to generate and providing power to the utility grid. When the penetration level was low, they were usually regarded as 'negative loads'. During grid faults, the distributed generation were allowed to disconnect in order to protect the equipment from being damaged. However, with more and more renewable generation connected to the grid, such a pure negative power source operation could cause problems. The generation systems would naturally be required to provide grid support in terms of voltage and frequency control during normal operation. Another stringent requirement which has presented challenges to most manufacturers is grid fault ride-through or low voltage ride-through [24]. When a fault happens in an adjacent area of where a considerable amount of renewable or embedded generators are providing power, which could cause the generators to quit, the loss of power provided by the generators could make the utility voltage drops even more and cause further problems. Reconnection after fault clearance would take time. The situation has generally changed nowadays. The renewable and/or distributed

generation is now generally required to remain connected during the fault to provide support to the grid immediately after the fault clearance. This brought challenges to the control system design, particularly associated with grid connected inverters. These requirements are special to generation rather than load technologies.

Three-phase inverters are often used to interface the renewable or distributed generation devices to the grid in order to cope with inherent variability of the sources. For large wind turbines, sometimes the generator is directly connected to the grid but not always. For off shore wind farm, the connection to the main grid is usually via a HVDC where an inverter is necessary to covert the power from d.c. to a.c.. For small wind power generators, a grid interfacing inverter is often required as the power from the generator is usually converted to d.c. for power quality control and maximum power tracking purposes etc. The solar panels will necessarily require a grid interfacing inverter as their power output is in term of d.c.. Among many situations that would cause the grid connection of the inverter to trip, the unbalanced faults are some of the most challenging and important because the commonly used voltage source converters (VSC) are very sensitive to a.c. side voltage unbalances; a commercial drive system with an active front-end rectifier (which is a VSC) would usually trip upon detecting a 2% content of negative sequence voltage [24]. The conventional control schemes designed for operation under balanced utility voltage, e.g. the voltage oriented current control with simple synchronised reference frame phase-locked-loop, are not able to yield satisfactory results during the unbalanced grid fault ride-through. The consequences include low order and even order harmonic injections and even damage to the power modules as well as capacitors in the inverter due to excessive currents. Apart from the gird faults, unbalanced loads and unbalanced generation on the three phases can also cause sustained voltage unbalance at the point of common coupling (PCC) with respect to the converter connection. As the grid operators are always aiming at balancing the network, the level of unbalance due to the unbalanced load or

generation is usually very small but could last much longer than the fault. Therefore, a control strategy with unbalanced utility voltage tolerance is necessary for grid connected inverter systems. Many researches have addressed this issue and several solutions have been reported [25-28]. However, previous studies usually focused on the steady-state performance while fast response with adequate transient stability needs further investigation; the key is to quickly identify the positive and negative sequences in the reference voltage for control. This defines part of the context of this study.

As analysed above, there is the need to reduce the system cost and improve reliability. This has given rise to the incentive to develop control techniques without using some of the sensors in a standard system which is shown in Figure 1.3. This study concentrates on achieving the above control objective without using the sensors to measure the grid voltage at the PCC. The current sensors are retained because the semiconductor devices require that the converter currents are always under strict control to avoid overloading. A brief analysis on the performance of the voltage-sensor-less control will be provided in Section 1.3.5.

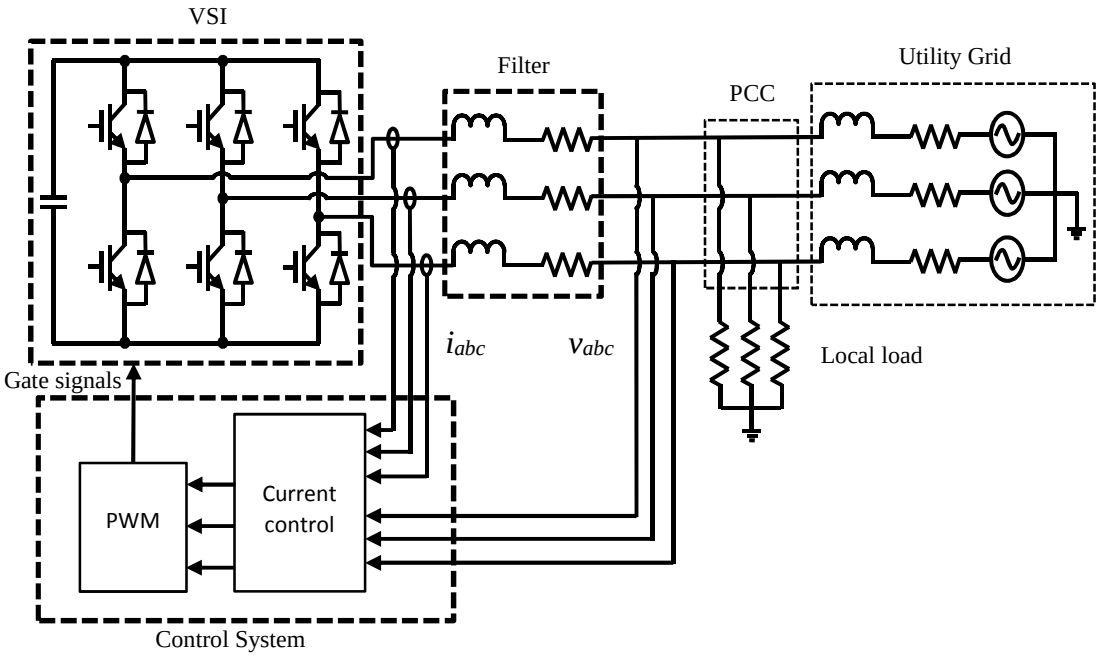


Figure 1.3. Controller block diagram of a grid connected VSC with internal current control

1.3 Compliance to grid code

When renewable power was only a small part of power generation in the system, the renewable generating units were treated just as negative, passive loads which took little responsibility towards the reliable and stable operation of the power system. As the penetration of renewables increases, grid codes are modified to specify the requirements on their performance and functionalities during normal operation and system abnormalities, such as faults. Requirements are imposed on renewable generation connected to both transmission and distribution networks [29]. In this section, the requirements issued by grid codes and technical recommendations are introduced. For large scale generations, some of the functions required by the grid code such as frequency adjustment and reactive power compensation will be done by adding additional control loop to the control system, which are not included in this research. Further research should be done in the future. For the small scale generations, it is not possible to affect the grid frequency or dealing large impact on the grid voltage. These grid code requirements are only mentioned to clarify the different situations that an inverter could encounter during on-line operation.

Traditional synchronous generators are connected to the grids directly while many renewable power generation systems are connected through a power electronics conversion stage. Therefore, the control capability and limitations of the converters are of serious importance in terms of grid code compliance. Nowadays, voltage source converters (VSCs) are used as standard in most systems, and this thesis will focus on the standard 2-level VSCs which are commonly found in wind turbines and PV systems. The study further focuses on the grid side converter. The relevant aspects of grid codes are harmonics, restrictions on the variation of power generated and grid fault ride-through capabilities. This section briefly reviews the main points of these aspects.

1.3.1 Harmonic limits

It is the responsibility of the utilities to make sure that the voltage at the connection point of the generation, which is usually also the point of common coupling (PCC) other circuits, is phase-balanced and the harmonic content is below certain level. Current harmonic injection into the grid by the inverters should follow the requirements to the general load [30]. The harmonic requirements provided by IEEE Std 519-1992 is generally accepted and followed by many grid codes of different countries. Table 1.1 summarizes these requirements, taken from IEEE Std 519-1992.

The harmonic content in the current produced by the grid connected inverter is usually regarded as low because of the high switching frequency of modern PWM (pulse-width modulation) processes, >2 kHz. Multiple level inverters are increasingly used for high power applications. The equivalent switching frequency is high although the actual switching frequency of individual devices is kept low to constrain the switching losses [24]. However for the reason to be shown in Chapter 2, there is the risk that some unusual harmonics, such as even order harmonics, injected into the grid could exceed the limit in poorly designed converters due to incomplete understanding of the physical phenomena in the converter and its control system. The non-ideal characteristics of the devices can also cause harmonics as shown in [32]. The main objective of this study is about control of the grid interfaced inverters under abnormal grid conditions, harmonics are not a major concern and the main purpose of harmonic analysis in this thesis is to guide the controller design and identify the cause of the harmonics that have not been eliminated in the test results.

Maximum Harmonic Current Distortion in Percent of I_L						
Individual Harmonic Order (Odd Harmonics)						
I_{SC}/I_L	<11	11≤h<17	17≤h<23	23≤h<35	35≤h	TDD
<20*	4.0	2.0	1.5	0.6	0.3	5.0
20<50	7.0	3.5	2.5	1.0	0.5	8.0
50<100	10.0	4.5	4.0	1.5	0.7	12.0
100<1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0
Even harmonics are limited to 25% of the odd harmonic limits above.						
Current distortions that result in a dc offset, e.g. half-wave converters, are not allowed.						
***All power generation equipment is limited to these values of current distortion, regardless of actual I_{SC}/I_L.**						
Where						
I_{SC} **= maximum short-circuit current at PCC**						
I_L **= Maximum demand load current (fundamental frequency component) at PCC.**						
TDD = Total demand distortion (RSS), harmonic current distortion in % of maximum demand load current (15 to 30 min demand)						
PCC = Point of common coupling.						

Table 1.1 Customer current harmonic limits, taken from [30]

1.3.2 Requirements during normal operation

A feature of renewable power generation, particularly wind and solar PV, is the unpredictability of the input power. For economic reasons a power system is designed to withstand a limited amount of sudden power change and in practice this is usually set as the loss of a maximum power plant [33]. The way to provide the support is traditional spinning reserve although energy storage is being actively developed as a more efficient alternative.

As wind power become a significant part of the overall generation, it has been required to share the duty of frequency regulation in the power system. Figure 1.4, taken from Irish grid code [34], shows the requirement to wind farms during grid frequency deviation. About 5% headroom is kept during normal operation so that the wind farm can produce more real power

when called upon. This can be wasteful as on average for every 20 turbines built, 1 is kept as reserve which is not generating power. Figure 1.5 shows that as the grid frequency reduces by 2 Hz, the wind farm output would increase by 5% of the initial power. Even assume that the wind farm was initially operating near its maximum power, this is about 25 times weaker than the frequency response of a traditional thermal or hydropower plant with a typical 4% power-frequency droop, suggesting that other means of frequency regulation such as energy storage and spinning reserves would still be needed.

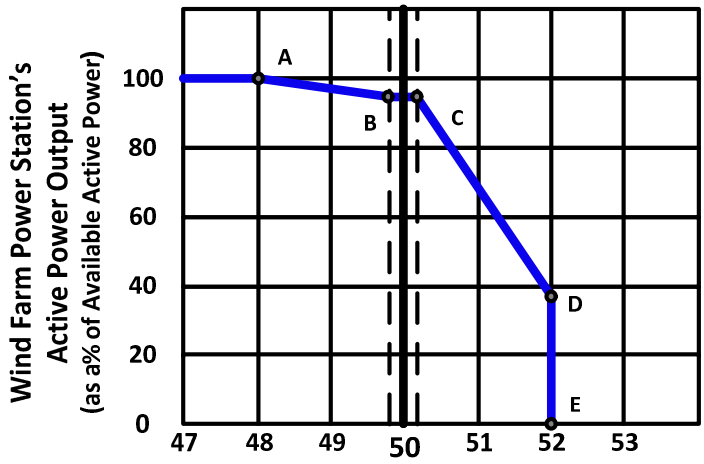


Figure 1.4. Grid code requirement for wind farm output during frequency variation, taken from [34]

However the power output of a modern turbine can respond very quickly owing to the modern power electronic converters included in the system. It is partially for this reason that recently in some countries, it has been seriously considered to require renewable power generation systems to provide fast and aggressive response to small deviations of system frequency. This is typically implemented through the concept of synthetic inertia emulating the change of kinetic energy in a synchronous generator [35]:

$$\Delta P = -2H\frac{df_{pu}}{dt} \qquad 1.1$$

where H is the H-inertia constant of the emulated power plant, typically 4-5 seconds, f_{pu} the per unit frequency of the a.c. system and ΔP the per unit power increment of the wind or renewable power plant. t is the time.

The wind farms are now also responsible to the voltage and reactive power control of the power system. This is usually specified as the range of lead to lagging power factor to be provided by the farm at different real power levels.

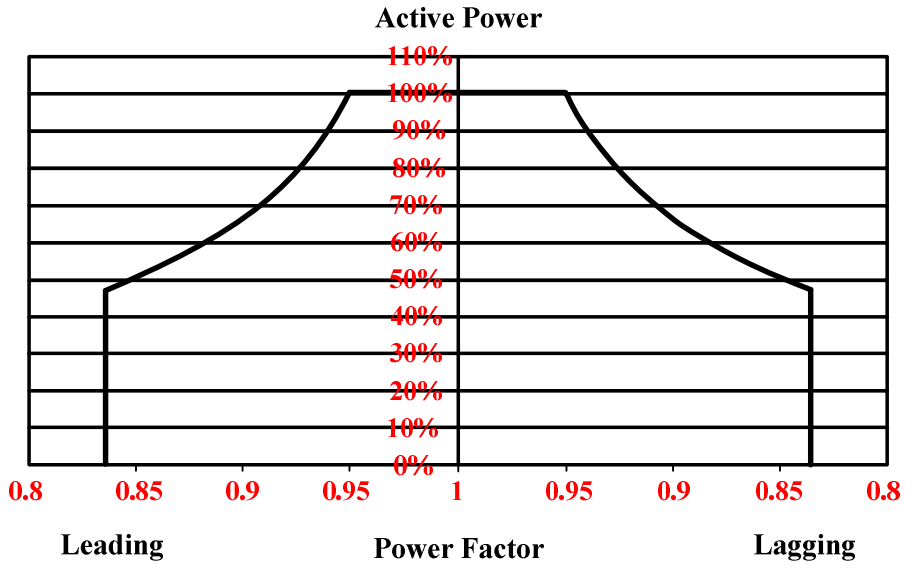


Figure 1.5. Wind farm active power output under frequency variation, taken from [34]

1.3.3 Fault-ride-through capability

Large synchronous generators can usually remain connected during a short circuit fault in the transmission network lasting for about 100-200 ms. The generators will feed current into the fault and the protection relays of the power network are based on this. A couple of reasons contribute to the capability of the synchronous generators: 1) the relatively rugged diodes and thyristors used in the brushless excitation system [33], and 2) the damper windings in modern machines which to some extent screens the rotor circuit from the effect of the stator side fault current [35]. The main concern is whether the synchronous machines can maintain synchronism with the rest of the grid after the fault clearance.

In the past when renewable power generation was treated as a negative load, there was no specific requirement to it but this situation has dramatically changed in the last 15 years. Stringent requirements are now included in the grid codes of almost all countries to ensure secure operation of the power system [36]. When renewable generation is now integrated or embedded into the transmission or distribution networks, the general expectation is that the new type of generation should behave like traditional synchronous machines. The generation units should possess the capability to ride through grid abnormalities. For instance, the UK National Grid Code requires that all wind turbine generators should remain connected to support the network and assist fault recovery if the transmission network voltage (any phase) undergoes the profile as shown in Figure 1.6 [34].

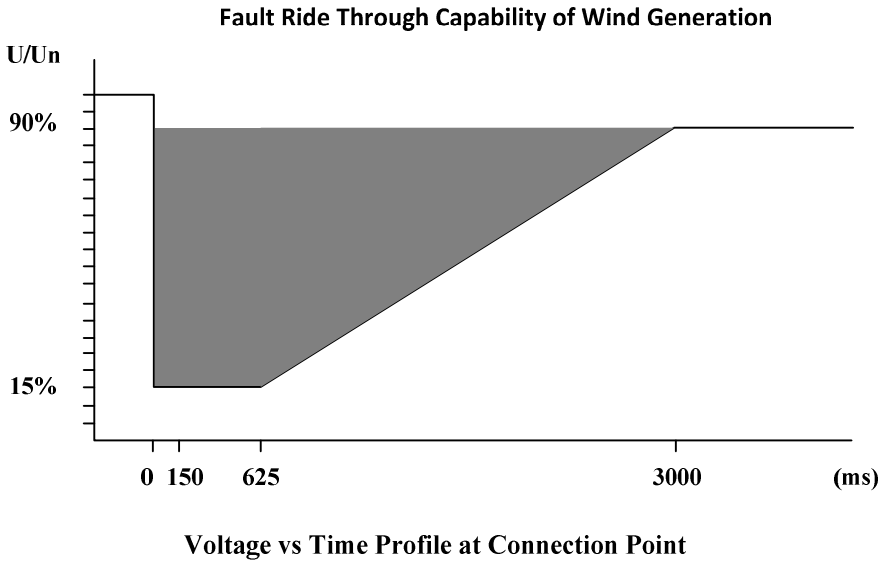


Figure 1.6 Grid code requirement for wind generation supporting the grid during grid faults, taken from [34]

A renewable power generation unit is interfaced to the grid fully [38-41] or partially (like a doubly fed induction generator [36, 42-44]) through a power electronic converter. The difficulty for a grid interfaced converter is to ride through unbalanced grid conditions including faults. Previous studies have considered control algorithms to smooth the d.c. side power [24,

45] or eliminate a.c. side negative sequence current injection [46-48]. But the algorithms proposed usually assumed that the grid pcc voltage is measured as the reference for current control, and the control transients were usually ignored.

There has been the desire to avoid grid voltage measurement in converter current and hence power control. Reliability is a major concern particularly in the case when multiple generation units are connected to the same point of common coupling. A shared voltage measurement point could then become a single weak link in the design. In [37], Parker proposed a voltage-sensor-less controller for a single phase, multilevel converter. But for a three-phase converter where the phases should not be independently treated, further studies are needed to develop the corresponding controllers.

Immediately following the occurrence of severe unbalanced grid conditions, it is important to quickly capture the grid voltage condition and control the converter current correspondingly. Many control strategies are based on the decomposition of the fundamental components into positive and negative sequences. It was shown that [24], large d.c. link voltage transients appear if the phase sequence decomposition process is slightly slowed down. Therefore it would be more challenging to achieve smooth control in the overall system with voltage-sensor-less control, and this is the main challenge to be addressed in the present study.

1.3.4 Standalone mode

Standalone or microgrid mode of operation is enabled by distributed generation. Many units indeed possess a power electronic interface stage. Control for grid voltage stability is a topic that is currently under intensive study [49]. There has not been attempt to achieve robust voltage control in the voltage-sensor-less mode because the duty of voltage stability control is usually assigned to a single master voltage source converter in the system with voltage sensors

[50]. Sensor-less control is still a desired feature for both the master and more distributed converters in the microgrid.

Although the grid voltage in the mains-connected mode is usually balanced with less than 1% of negative sequence [51], voltage unbalance is likely to occur in microgrid due to the reduced effect of load or generation aggregation [52]. Therefore three-phase converters may be required to operate with sustained voltage unbalance.

1.3.5 Cost effectiveness and reliability issue of distributed generation

The distributed generator are predominantly provided by small business owners with locally installed units such as small wind turbines with permanent magnet generators and domestic users of solar PV. Many of such applications require a grid interfacing inverter at the output terminals. The reliability of the grid interfacing inverter contributes a great proportion of the overall reliability of the generation. Driven by desire of reducing the loss both from energy and economic points of view, the methods to improve the reliability of the grid connected inverter were investigated in [53]. Figure 1.7 shows the failure rate of the components of a wind-turbine and it can be seen that the grid interfacing VSI and its sensors contribute a great potion of the total failures.

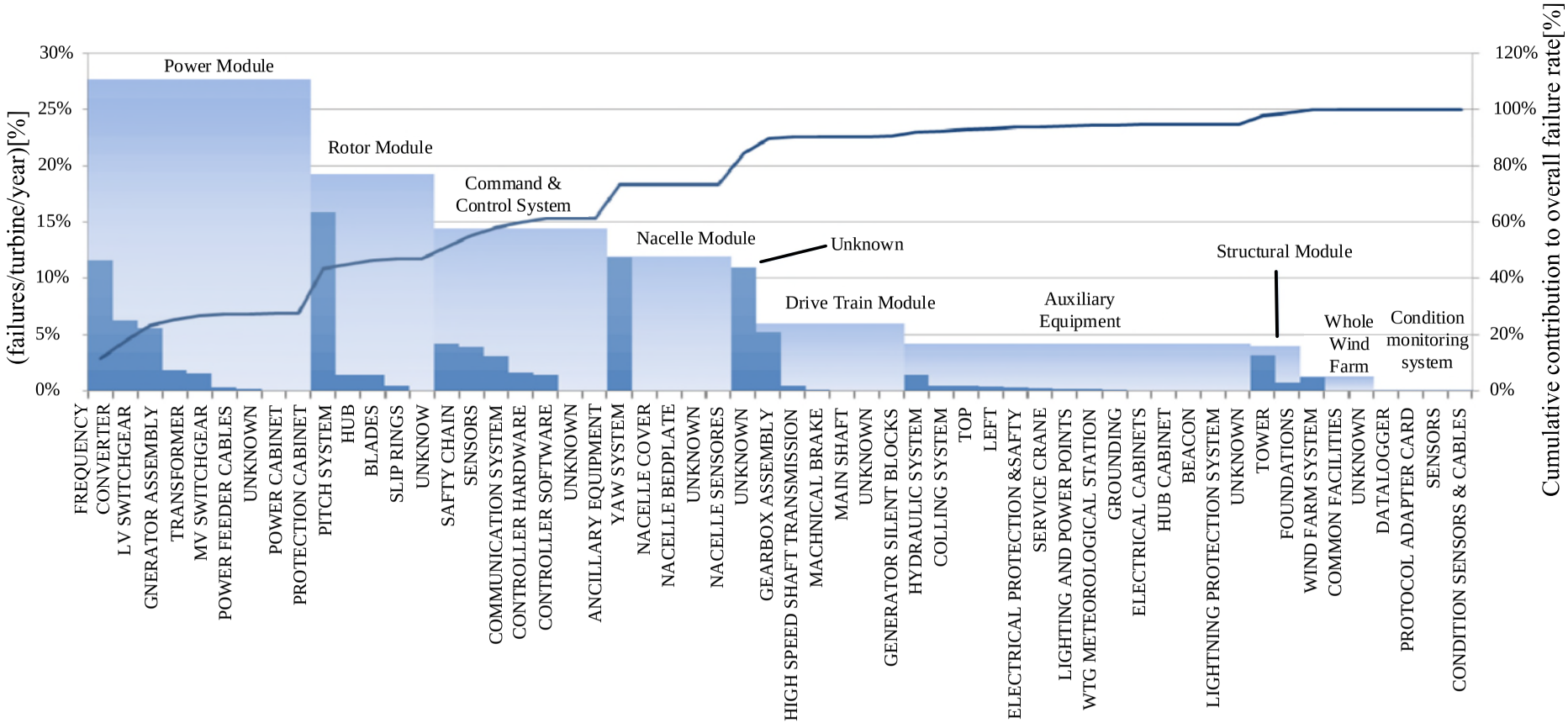


Figure 1.7 Normalised overall failure rates of sub-systems and assemblies of wind turbines of multiple manufacturers, taken from [51].

Apart from the reliability issue, the owners of these generators are surely concerned about the cost effectiveness of their facilities. A competitive product in this market should be cheap enough to provide a reasonably short pay-back time.

To satisfy both interests illustrated above, an idea of reducing the sensors used in the grid connected inverter would be attractive. On one hand, the grid interfacing inverter is less likely to be affected by the failure of the sensors. On the other hand, the manufacturing cost is reduced through less sensors used. Among many sensor reduction methods, the voltage-sensor-less control is especially attractive for that it enables the system to eliminate the use of the a.c.-line voltage sensors, which reduces not only the number of sensor components, but also the number of types of the components. This shortens the supply chain behind the manufacturing and facilitate the modular design of such equipment, both reducing the cost.

1.4 Project Objectives

The previous discussion showed a clear future picture that an unbalanced three-phase voltage will becoming a more frequent situation at the interface between the renewable power generation and the main grid. The capability of dealing with the unbalanced grid-side voltage is an important aspect for those small scaled renewable power generators e.g. wind and solar power generators rated at 5 to 10KW, which are connected to the three-phase grid to optimise their performance. The three phase a.c. side or grid in this research refers to a three-phase three-wire configuration and as will be shown in the following chapters unless specified.

The previous research has shown discussed several different methods to achieve a.c. voltage-sensor-less current control, some of them have the ability to ride-through an unbalanced grid fault. These details will be discussed in the later chapters. However, firstly, none of them has achieved unbalanced fault-ride-through based on a dq reference frame control scheme without

using a.c. side voltage sensors. Secondly, the transient response of the control system should be further improved due to large delay introduced by conventional symmetrical component decomposition method. Thirdly, steady state operation of the a.c. voltage-sensor-less control system were the main focus of these previous researches. But how the system is going to synchronise to the grid voltage when start-up is not made clear.

This research aims at the development of a dq reference frame based a.c. voltage-sensor-less control algorithm which is able to reduce the cost of the generation equipment either by improving its reliability or reducing the manufacturing cost. The proposed a.c. voltage-sensor-less control system will be able to ride through the unbalanced grid side voltage. This requires the output power of the inverter can be controlled during unbalanced grid fault:

- to provide support to the grid under unbalanced grid side voltage;
- to compensate the unbalanced three-phase power output.

To overcome the potential threat of over-current when the inverter is not synchronised to the grid voltage, a start-up process is proposed in this research with direct current controllability. The power during this period should also be controlled for protecting other components on the circuit board.

The delay introduced by the symmetrical component decomposition system will deteriorat the performance of the current control. A faster symmetrical component decomposition method will be proposed to improve the transient response of the control system.

It is essential to this research to make understanding on the stability issue of a grid connected inverter system. The knowledge of a general design approach of an observer based voltage-sensor-less control system is proposed based on the analysis of the control parameters which affect the system stability against different source of the disturbances.

The following aspects will be clarified in the rest of the thesis:

- the structure of a voltage-sensor-less controller;
- the parameters and their effect on the system performance;
- the disturbances with respect to the system stability margin;
- the design objective and its physical necessities;
- the general design approach of the parameters for tuning the controller.

1.5 Main Contributions of the Thesis

Initial synchronisation without a.c. voltage sensors: Several previous research studies have discussed the voltage-sensor-less control of a grid connected VSC for normal operation as well as the system performance under distorted grid voltage conditions [54-57]. However one important step for operation of the grid connected inverter, , the initial grid synchronisation, has been largely ignored. In this research, the initial synchronisation to the grid voltage before start-up is proposed. This is achieved from estimation/calculations based on the system response to the switch control commands without voltage sensors. An initial synchronisation method is developed to ensure the safety of both the power modules and the d.c. link capacitor. This provided a safe method to synchronise to the grid voltage without using voltage sensors. This also provides an alternative way to achieve grid synchronisation for 2 level grid connected inverters with a.c. voltage sensors, improving the reliability of the conventional system through redundancy.

Faster PLL system design for unbalanced utility voltage: As an important part of the control objective, the unbalanced operation of the grid connected VSCs is a focus of this study. A new PLL system is proposed and tested to solve the problem of oscillation and slow transient response of conventional PLL systems for decomposing the fundamental frequency

components of the positive and negative sequence from the total. The proposed PLL system enhanced the transient response of the proposed voltage-sensor-less VSC against utility voltage disturbances.

A generalized control method for the grid connected inverter for wind and solar power generation where a grid interfacing inverter is needed is presented by this research. As the rated power of the model being developed in this research is between 5-10 Kw, the inverter will be obliged to connect to the distribution network. The three-phase four-wire topology is typically used for modelling the grid side. But this generalized control method is also expandable to be of higher rated power. By adopting inverter with its topology suitable for high power applications, the control method can also be used in the applications connecting to the transmission network but it requires more research. By summarizing the design procedure of the proposed voltage-sensor-less system, stability analysis was carefully carried out and is presented in the thesis.

Chapter 2 Current Control of Voltage Source Converter

2.1 Introduction

The current controller of a grid connected inverter is responsible for determining the switching duty of the power modules to produce the desired current waveform. A well designed current controller should be able to track the reference current without any steady state error. And the response of the controller should be swift when the command changes and the controller should also be robust in different network conditions so that the system is protected from being tripped out or damaged by the utility voltage variations. As required by various grid codes [34], the low order harmonic output is restricted and the controller should be designed without any oscillation modes with any residual harmonics in the output. The current controllers can be roughly categorised into linear and none-linear current control methods.

The select of the current control technique varies with the aims of applications. For instance, the current control of a shunt connected active filter requires a high band width tracking ability to compensate the harmonic current injected into the grid by other none-linear loads, while others such as the current control for a grid connected inverter for renewable power generation requires minimum harmonic injection. In this chapter, different current control techniques are introduced and compared. The select of the current control of the voltage-sensor-less control system are made based on this comparison.

Differing from linear current control method, a distinct characteristic of the none-linear current control method is that the switching duty is directly generated by the controller to drive the power modules. On one hand, this characteristic often comes with none constant switching frequency which could result in the low order harmonic injection which is not desirable. On the other hand, the none-linear current control methods are often free from controller

bandwidth restriction as the switching duty is directly controllable which lead to a faster response and robustness. As the linear current control method has the output of the current error compensation algorithm feeding into a separate gate signal generator, which is often a PWM signal generator, a constant switch frequency can be achieved to prevent the low order harmonic injection. In this research, the full control scheme proposed benefits from both the linear and none-linear current control. A summary of different types of current controllers is provided in this chapter for overviewing the existing techniques and explaining the selection for the current controller in this research.

2.2 None-linear current control: hysteresis control

Hysteresis current control is classified as a none-linear current control method. It directly controls the switching duty of the power electronic modules to force the current output to track a desired value or waveform. Several advantages such as a higher stability margin and the better tracking ability over other current control methods have been reported in [58, 59]. Moreover, fixed-band hysteresis current control has a very simple controller algorithm and small computational burden yet it has another advantage. This control method does not introduce any voltage feed-forward to minimise the transient response. During normal operation, the grid voltage is only sampled for generating correct current reference to achieve a desired power. Therefore, it is potentially very useful in cases when the grid voltage is not available while the current should be limited in order to protect the power electronic devices e.g. start-up of the a.c. voltage-sensor-less control of the VSI.

The principle of hysteresis current control is simple, applying the assumption that the d.c. link voltage are sufficiently higher than the peak to peak value of the utility a.c. voltage (line-line) so that the switching action always achieves its desired effect. This is shown in Figure 2.1. The

sampled current values are compared with the current reference. When the sampled current is shown to be smaller than the current reference, a signal to turn on the upper switch (after turning off the lower switch) of the phase-leg is given to raise the current. Similarly a signal to turn on the lower switch of the phase-leg (after turning off the upper switch) is given for bringing down the current when it is above the current reference. It is obvious that the update of the switching state is synchronised to the sampling process. Ideally, with an infinite sampling and switching rate, this mechanism is able to control the current to track its reference value without error. However, in practical applications this is hardly achievable. Firstly, the state of conduction or blocking of power electronics devices will not change instantly due to the physical nature of the devices. Secondly a dead-band is introduced to protect the upper and lower arms from shorting-through the d.c. link. Therefore a delay of turning on the in-coming device is introduced. Thirdly, the switching frequency of the power modules cannot be infinitely high by considering the switching losses. For analogue controllers, the noise problem would degrade their performance and hence they are not considered. Due to these reasons, the current reference usually sits within a tolerance range for finite switching rate [60]. This is known as the hysteresis band, and the control strategy is illustrated in Figure 2.2.

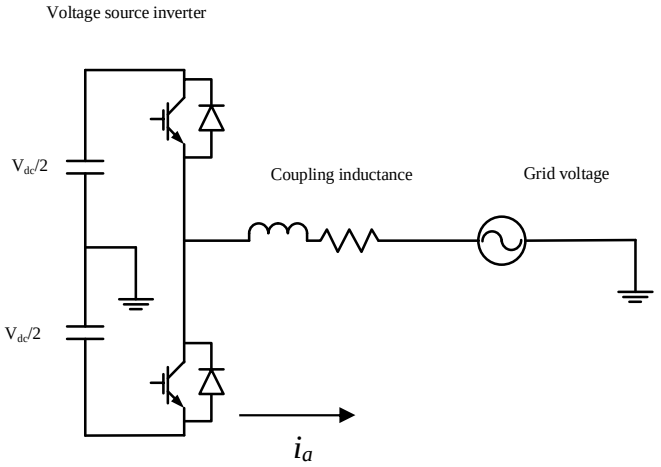


Figure 2.1 Circuit diagram of a two-level single-phase inverter

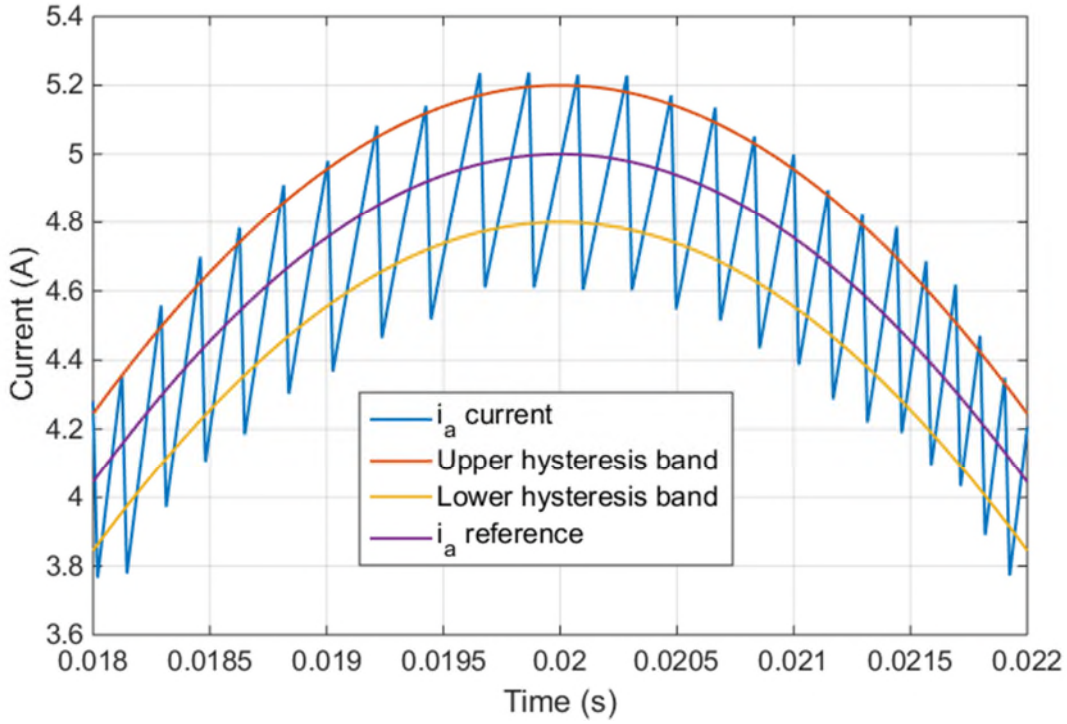


Figure 2.2 Illustration of current hysteresis control

The draw-back of fixed-band hysteresis current control is well known as the production of a wide range of harmonic frequency components, which makes the filter design difficult. For the fixed band hysteresis control, due to change of the grid voltage within a fundamental cycle, the voltage drop across the coupling impedance is not constant and this makes the current rise/drop to have different rates at different time points. The sample will not be naturally locked to the event that the current value passes the hysteresis band. During the time that the current value is between the upper and lower hysteresis band, the states of the switching devices are held. The hysteresis band should be designed taking the coupling impedance, the sampling rate on the control board and the d.c. as well as a.c. side voltage into consideration to minimise the difference of the number of samples among the switch duty updates so that the switching frequency is approximately constant.

Given the 2-level converter topology, the output voltage at the input terminal of the filter should be either $+V_{dc}/2$ or $-V_{dc}/2$, with respect to the d.c. neutral. As the switching frequency of the

hysteresis control is not constant but dependent on the operating conditions, the terminal voltage cannot be ensured to be zero sequence free. This results in the interference between phases. The current flow through each phase is no longer decided by the load and the phase voltage in this phase but is also subjective to the effect of the line voltage. In [61], the effect of the phase interference is evaluated and improvement to the hysteresis switching aiming at constant switching frequency is made. However, for many control systems, the load or grid parameters could be essential but are usually hard to be obtained; the methods increase the complexity of the control system configuration.

The well-known drawback of the fixed-band hysteresis current control, i.e. the unpredictable harmonic content which makes the filter design difficult, is due to the unequal duration of each switching duty update and this is caused by voltage drop variation as illustrated above. Ideally, switching duty updates should be made on a regular basis. Although many methods were proposed to provide some the harmonic rejection features for current hysteresis control [58, 62, 63], these methods are mostly trying to adjust the hysteresis band by a.c. source voltage or prediction from the VSI output. By adjusting the hysteresis band, a more constant switching frequency can be achieved. The methods rely on the voltage measured at the PCC which is not desired in this research because the use of the voltage sensors will be eliminated. Some of the methods above aim at working out a predictive scheme to minimise the switching frequency variation at a cost of increasing the sampling frequency instantaneously to as high as 300 kHz [58], which is not realistic in many high power applications. Such controllers may increase the cost of building the power control system hardware and therefore they are not considered any further.

2.3 Linear current control methods

The linear current control methods have been widely used for better performance in terms of reduced low order harmonic injection as compared to the non-linear current control methods, such as the current hysteresis control described above. The current control algorithms to generate the voltage command signals have been developed based on many different models. The performance of the current control algorithm directly affects the control quality of the VSI system and thus needs to be examined. In this chapter, the current control algorithms are compared and discussed in terms of their stability, speed and accuracy.

2.3.1 Ramp comparison current control

The PI controllers are widely used in many control tasks and the simplest way to use such a controller for VSI current control purpose is the method known as ramp comparison current control. The error between the phase current and its reference is directly feed into the PI controller to generate the voltage command signals, aiming at driving the error towards zero. A voltage feed-forward term is often applied to the command signals in order to minimise the transients in response. Then the gate signals are generated depending on the method selected such as SVPWM and SPWM. However, this technique is usually insufficient due to the inherent tracking error associated with the PI regulator tracking a sinusoidal signal, unless a controller structure of a higher rank is designed [64]. The structure of a PI controller for current control, in the phase or *abc* reference frame, is shown in Figure 2.3.

As the error between the current reference and the phase current feedback can be sinusoidal in the natural *abc* reference frame, the output of the PI controller has a phase delay compareing to the original error. The output of the PI controller as a voltage compensation will result in the current compensation further being delayed due to the coupling inductance. In the steady state,

an inherent tracking error will be clearly visible in the ramp comparison current control. Furthermore, the ramp comparison current control is seemingly simple but comparing to the *dq*-decoupled control (to be explained next) and the proportional-resonance (PR) current controller on the alpha-beta reference frame, more control actions are needed. Thus the cost effectiveness of such a simple PI controller in term of the computational power is not attractive. This conclusion has been verified by several different studies. Figure 2.4 shows the simulation results of a PI based ramp comparison current control, with significant tacking errors.

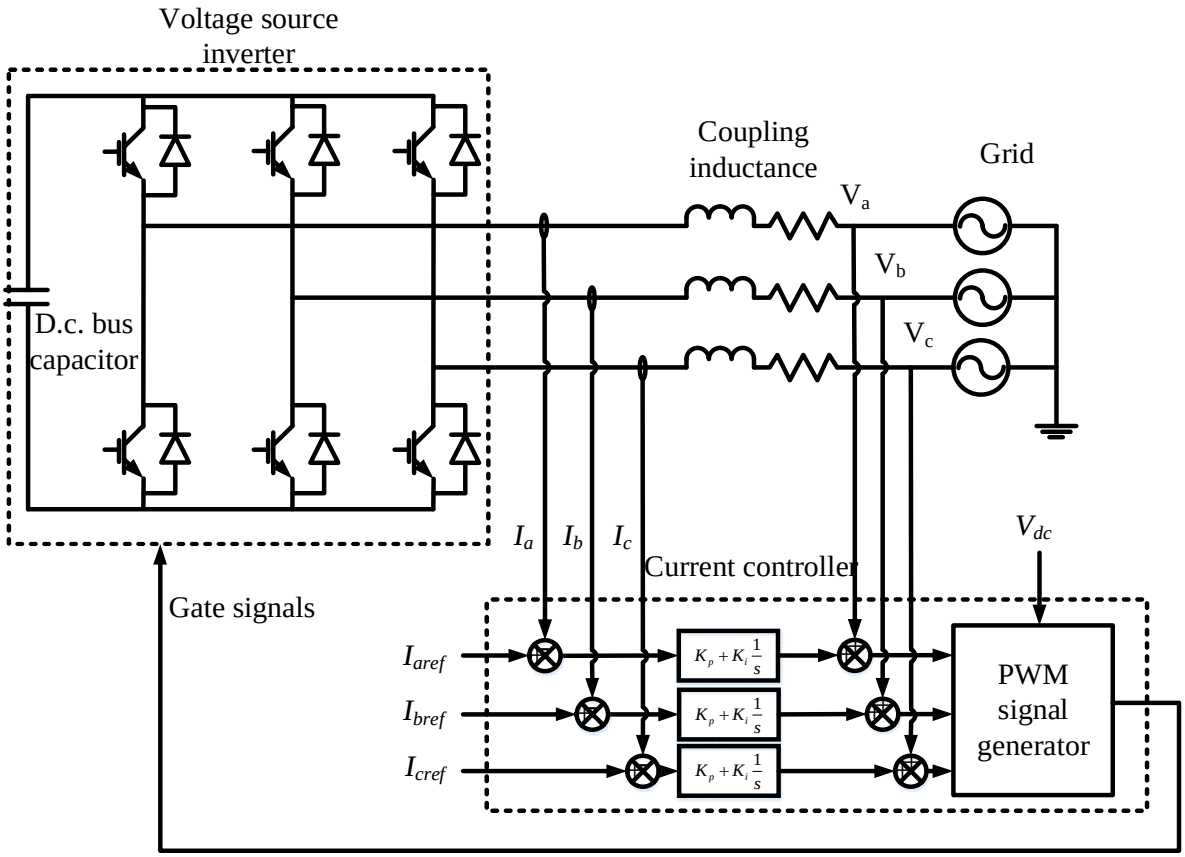


Figure 2.3 System diagram of ramp comparison current control

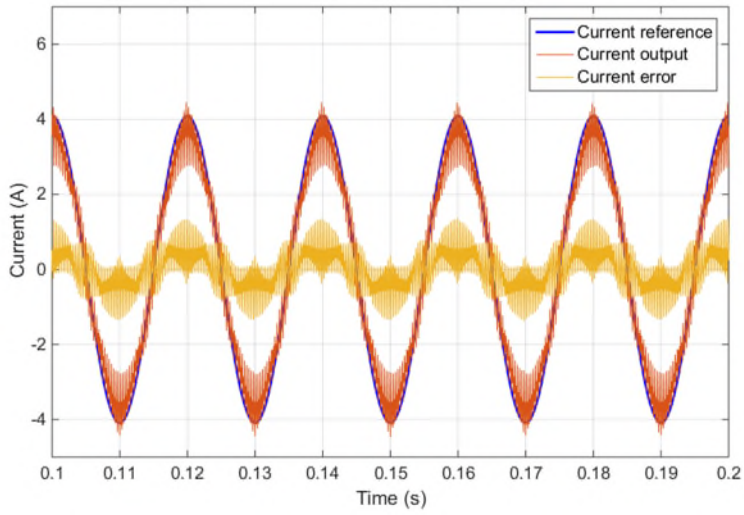


Figure 2.4 Tracking error of the ramp comparison current control

2.3.2 Dq-decoupled current control

The *dq*-decoupled control is the most widely used current controller structure. It also utilizes the PI algorithm in the control scheme but it has several advantages over the ramp comparison current control. Conventionally, the balanced three phase voltage signals are transformed into the direct and quadrature axes using the *dq* transformation. Through this transformation, all three phase sinusoidal signals are represented by the corresponding direct and quadrature axes components. For an ideally balanced three-phase utility grid voltage, the direct and quadrature components are constant or d.c. values, while the *dq* reference frame rotates at the synchronous speed with respect to the *abc* reference frame. A synchronous reference frame based phase locked loop (SRF-PLL) [65-67] can be utilized to track the necessary phase angle and amplitude as well as the frequency for the downstream control stages. By applying the SRF-PLL, the *dq* rotating reference frame is defined according to the grid voltage vector. The *dq* transformation is also applied to the current signals. The direct and quadrature components of the current are the vector projections to the *dq* reference frame defined by the reference grid

voltage vector. The controller stricture is shown in Figure 2.5. In the steady state, the current signals i_d and i_q are also d.c. values. As the control signals (commands) for the PI controller in the *dq*-decoupled current control scheme are d.c. values, the current control can be done accurately using a PI algorithm without steady state error. The current references for i_d and i_q could be generated from the desired real and reactive power by the power control algorithm based on the input condition and the utility voltage [68-71]. By changing the i_d and i_q references, the real and reactive power at the receiving end can be controlled independently.

In this way, the VSI system can be usually regarded as a second order system and the optimisation of such a system is well established in control theory [64]. The optimum response can be achieved by adjusting the proportional and integral control gains. The detailed discussion of the tuning procedure of the current controller, as applied in this study, will be provided in Chapter 5. Figures 2.6 and 2.7 show the simulation results of the *dq*-decoupled current control tracking different reference. Figure 2.8 shows the sinusoidal reference under which, the current response is shown as in Figure 2.7.

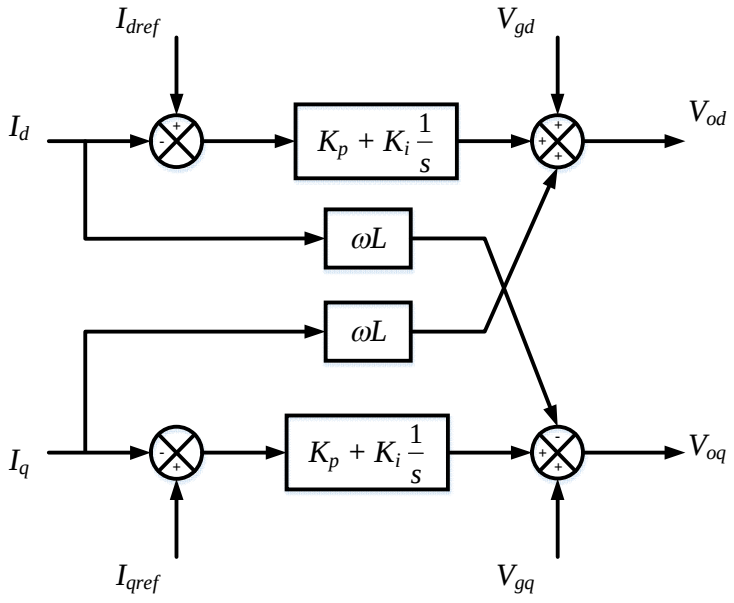


Figure 2.5 *Dq*-decoupled current controller structure

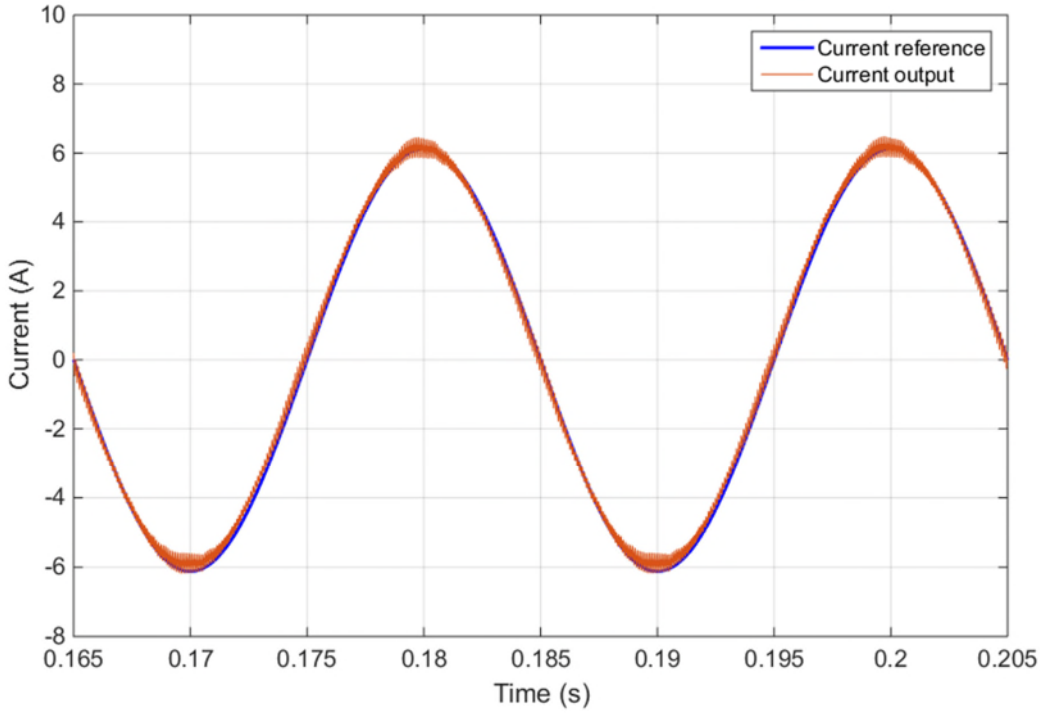


Figure 2.6 Simulation result of *dq*-decoupled current control tracking constant *dq* reference

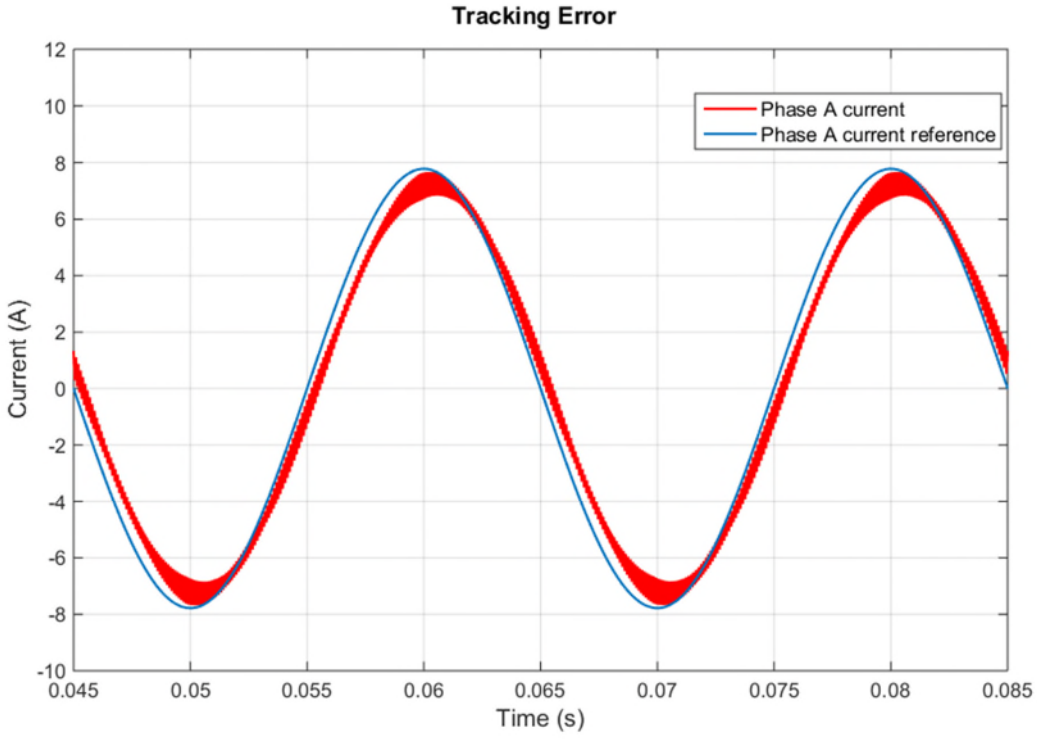


Figure 2.7 Tracking error of *dq*-decoupled current control tracking sinusoidal *dq* reference

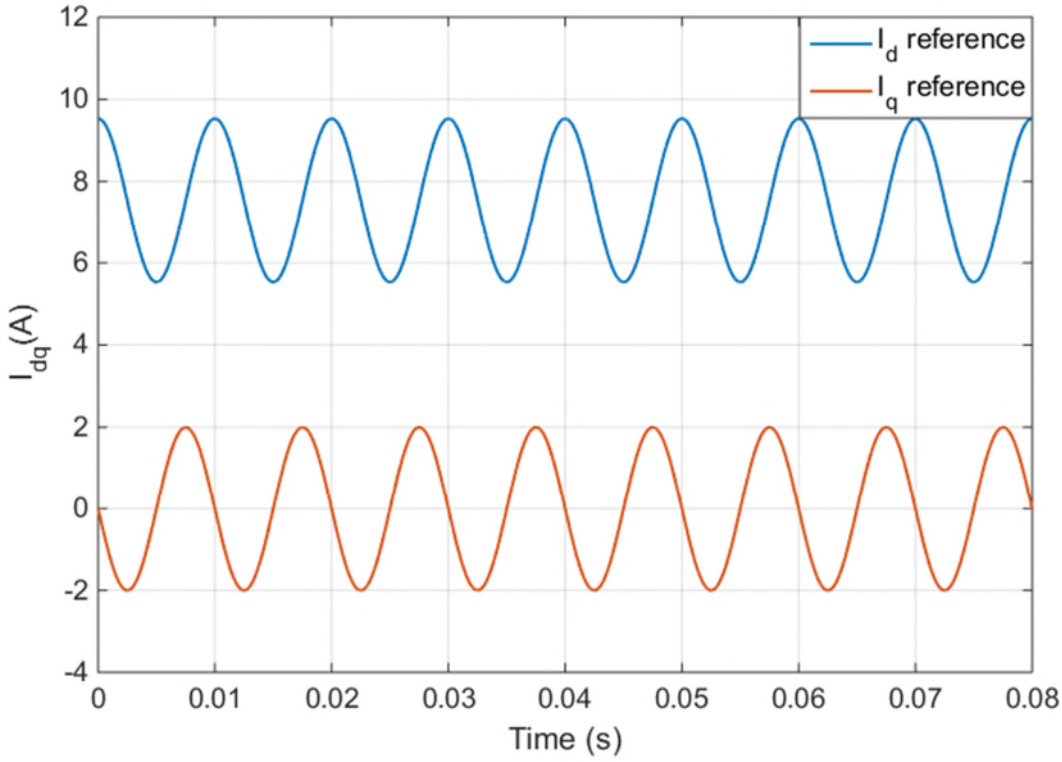


Figure 2.8 Sinusoidal *dq* reference

As can be seen from the simulation results, the *dq*-decoupled current control yields satisfactory result in term of the control accuracy. However, with non-ideal utility voltage e.g. with unbalanced utility voltage, as the negative sequence component will become 100 Hz oscillation in the positive sequence *dq* reference frame as discussed previously, the PI controller will not be sufficient for tracking sinusoidal control reference. The current control will suffer from inherent tracking error because of the limited bandwidth of the PI controller. Besides, as the 100 Hz oscillation of the *dq* reference frame will be transformed to *abc* natural reference frame, not only the negative sequence component but also a 3rd harmonic will appear in the voltage command signal which results in the undesired harmonic injection. To overcome these drawbacks, the input to the *dq*-decoupled control needs to be oscillation free. The improved PLL system are going to be utilized for this purpose, as will be discussed in the following chapter.

2.3.3 Proportional-resonant current control

The proportional resonant controller has a good performance on regulating sinusoidal control signal. The characteristic of this controller gained its attention for the potential to improve the ramp comparison current control by replacing the PI controllers.

The PR controller has a frequency selective property.

The transfer function of the PR controller is given by:

$$G(s) = K_p + \frac{K_r}{s^2 + \omega^2} \qquad 2.1$$

where proportional gain K_p and resonance gain K_r are equivalent to the proportional and integral gains of the PI controllers respectively and ω is the resonant frequency.

Harmonic rejection is one of the advantages of the proportional-resonance control technique. Because the control feedback of the system is the sinusoidal signal which could be the measured three phase signals in the natural three-phase reference frame, simpler controller structure can also be used, e.g. the reference frame transformation is eliminated. As the control system is designed to control the sinusoidal signals at a certain frequency, the non-resonance frequency component are rejected in the output. This leads to a simpler control system structure without the decoupling of *dq* axes interactions, which often presents in PI-SRF based current controllers. However, apart from the advantages mentioned above, a few aspects could potentially decrease the system performance. The grid frequency as the key controller parameter, which is not directly available from the measurements, may need to be obtained via an additional stage to achieve accurate control. Given that the frequency may deviate from 50Hz, additional algorithms such as PLL or FLL are still required and the control system can still be complex. Considering the noises and harmonics in real applications, the frequency estimation will need further filtering to prevent causing oscillations in the control system.

Therefore the drawback of requiring the frequency parameter from an additional stage reduces the overall system responsiveness. Also, the PLL and FLL systems are often integrated with coordinate transformation between the stationary and synchronously rotating reference frames. This leads to natural reference frame control becoming meaningless. Alternatively, reducing the quality factor of the PR controller to enlarge the passing band of the controller could make the system more adaptive to frequency deviation but at the cost of the reduction of the frequency selectivity [72, 73].

2.3.4 Harmonic reduction

One common source of low order harmonics e.g. the 5^{th} and 7^{th} harmonic is the voltage drops across the semiconductor devices particularly unipolar devices such as IGBTs and diodes, which are not fully compensated. In [74-77], the cause of the 5^{th} and 7^{th} harmonics also known as characteristic harmonics, injection is reported. The first source of these characteristic harmonic injection is the dead-time effect. The dead-time is introduced to protect the VSI from short circuiting due to the turn off delay of the semiconductors. If it is not critically designed, the unnecessary dead-time would bring non-linearity into the output, causing harmonic injection. As the conduction of the semiconductors will apply a fixed voltage drop between the input and the output depending on the material used for the semiconductors and the device design, this non-linearity characteristic results in the second source of the 5^{th} and 7^{th} harmonic injection as suggested in [75, 78]. The on-state resistance of the semiconductors is also a source of the conduction loss which also causes voltage drop across the devices. However, as the voltage drop associated with the resistance has a proportional relationship to the current output, it is not considered as the source of the harmonics. Based on the understanding of the cause of the mutual relationship between the harmonic injection and the non-linear characteristics of the

semiconductors, the controller design should avoid resonance at any of these harmonic frequencies.

In [66], compensation to the voltage reference of the PWM pulse generator is made based on the measured voltage drop. In the conventional control scheme, the power electronic devices are assumed to be ideal and the error between the output reference voltage and the actual output is generated in real application. By taking the voltage drop across the semiconductors into account, this method aims at achieving accurate output of the desired voltage at the converter terminals. As the compensation is a fixed value applied to the output reference positively or negatively based on the sign of the reference and irrelevant to the system feedback, this approach is regarded as the open-loop approach in the harmonic rejection associated with the non-linearity of the semiconductors.

Considering the harmonics can be separated by PLL systems as discussed in Chapter 3, the closed-loop control can be utilised to compensate the harmonics. The commonly appeared characteristic harmonics will be on the as 6^{th} and 12^{th} harmonic on the *dq* axis. A simple solution would be cascading a PR controller in parallel with the PI regulator of the *dq*-decouple current control as introduced in [77].

2.4 Chapter Summary

In this chapter, the advantage and disadvantage of different current control techniques are discussed. The hysteresis current control has the advantage of the fast transient response and easy current limiting mechanism. It can be utilized to ride-through large variation of the system e.g. initial synchronisation to the grid when start-up detailed in the later chapters. However it is not feasible for long term operation of the VSI for its poor performance in term of harmonic injection. For steady state operation of the VSI, the linear current control method should be

selected. Among linear current control methods discussed, the ramp-comparison current control is not considered as a satisfactory solution for the steady state error caused by its limited controller band-width. Between the rest two control methods, the PI-SRF based current control is preferred for the following reasons: Firstly, compared with that of the SRF-PI based current control, the performance of the PR controller is heavily dependent to the accurate information of the grid frequency. The robustness of the SRF-PI based current control to the grid voltage variation is advantage. Secondly, the SRF-PI based current control has been used in control practice of the motor drives for a long period of time and proved to be mature and satisfactory. It will be easier to put the proposed current control method in this research into practice as the coding of the SRF-PI based current control algorithm will be easily available.

Chapter 3 Grid Synchronisation Techniques for Grid Connected Inverter

3.1 Introduction

The operation of a voltage source inverter requires the information of grid voltage as a reference to achieve a desired power [79]. Considering that renewable power generation is usually connected to weak points in the a.c. grid where voltage unbalance and harmonic distortion can often be presented, the phase-locking and symmetrical components decomposition of the grid voltage is crucial to the performance of the VSI control. The symmetrical components decomposition is also required for deriving the current command signals therefore it is also an important factor for defining the performance of the current controller [31, 79]. In this chapter, the techniques required for achieving the desired current control is introduced.

Traditionally, the development of the control strategy for the grid connected inverter is based on the measured grid source-voltage and this strategy has been widely adopted in various applications including harmonic filtering, reactive power compensation and grid fault ride-through. Sensor-less control without measuring the grid source voltage is gaining attention in recent years [80]. Compared to the control models with the grid source-voltage measured, the a.c. voltage-sensor-less control has several advantages. First, the cost of hardware is reduced as less components are required. Second, the level of modularity of the system is increased in both hardware and software to facilitate the mass production. Third, the reliability of the system is increased, as shown in Figure 1.7 by the failure rates and downtimes caused by sensors in the control system of a wind turbine system. It is clear that power electronic

converters, which are the major part of the electrical and control systems, contribute significantly to both.

3.2 Grid synchronisation methods

For converters used in a.c. power systems, one aspect of control is always to maintain the target power factor. The target power factor is set along with other control objectives. For instance, a domestic solar panel is most likely to output power through a grid interface inverter with unity power factor for maximise the usage of the current rating of the power modules and economic benefit, while a VAR compensator is going to operate at very low power factor as it is deployed to support the grid with reactive power rather than real power [10]. The grid synchronisation is a very important piece in the controller of the grid connected inverter, and for the reason to become clearer later, this depends on the converter operation mode.

The PLL is included in the control system for processing the measured signals in order to acquire the angle reference to define the rotational reference frame as well as the grid frequency. It is a key component in the voltage oriented current control system as well as many other control functionalities synchronised to the utility voltage [81-84]. The control of real and reactive power flow is achieved with correct synchronisation to the grid. Among the schemes of PLL, the synchronised-reference-frame phase-locked-loop is the most widely used.

The PLL system is also a key component in the a.c. voltage-sensor-less control studied in this project. In addition to the reasons described above, the system stability is also highly dependent on the performance of the PLL.

The basic phase-locked-loop consists of a phase detector, a loop filter and a voltage-controlled oscillator [85-88] as shown in Figure 3.1. For practical PLLs used in converter control systems, especially those connected to three-phase grid systems, the algorithm representing the phase detector can be different but the basic structure remains the same, as shown in Figure 3.2. A

detailed review of the phase detector of the three-phase PLL will be provided later.

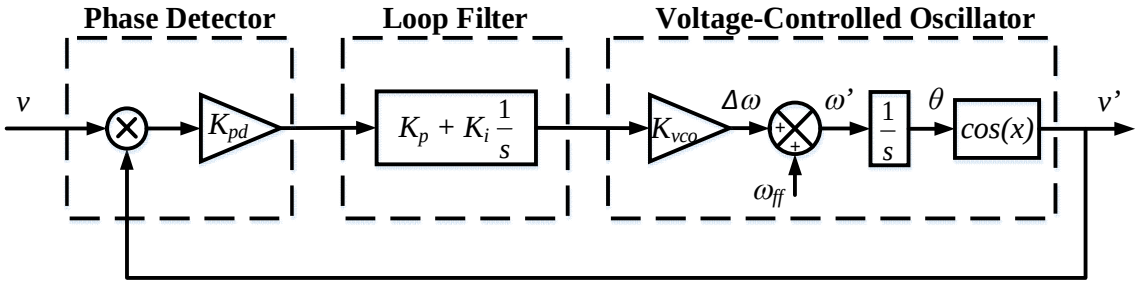


Figure 3.1 Block diagram of a basic phase-locked-loop

The phase detector is used to determine the phase angle of the input signal. The main functionality of the loop filter which has a low-pass filtering characteristic and is usually realized based on a PI controller is to suppress the high-frequency noises of the output of the phase detector [87-90]. Also, the system performance e.g. the damping effect and bandwidth can be adjusted by tuning the loop filter gains [89, 90]. The voltage controlled oscillator VCO translates the output of the loop filter into the frequency variation which is needed for tracking the phase of the input signal.

The conventional SRF PLL is widely used in control system of three-phase voltage source converters [81,91]. The input to the SRF-PLL is assumed to be balanced and sinusoidal. Therefore the inputs can be redefined in a synchronised rotational reference frame as direct and quadrature signals which are constant values through an *abc-dq* transformation, as shown in Figure 3.3. The PLL system provides the phase angle to the *abc-dq* transformation so that the voltage vector is aligned to the d-axis of the synchronised reference frame. The value of the quadrature signal scaled by the amplitude of the voltage vector, which equals *sin(θ)*, can be viewed as the phase angle difference in the small signal model. In this case, the *abc-dq* transformation can be viewed as a phase detector. The phase difference is then passing through the loop filter to generate the frequency error. A feedforward term of the grid frequency, which

is ω_{ff}=2π50rad/s, is added to improve the system dynamics. The phase angle which is fed back to the *abc-dq* transformation is the integration of the estimated grid frequency. In the steady state, the quadrature component will be derived to zero and the information of the amplitude is contained in the direct component.

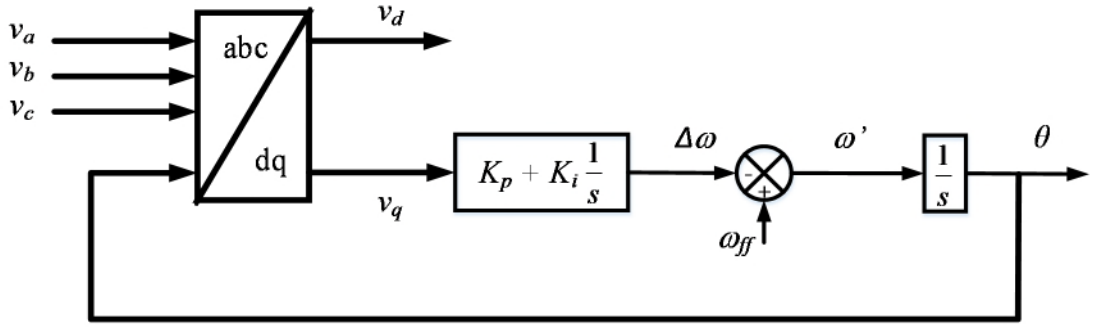


Figure 3.2 Block diagram of the SRF-PLL for three phase system

In practice, v_q is usually normalized by the amplitude of the voltage vector and it will be 0 when the SRF-PLL reaches the steady state. Knowing that for very small θ, this phase angle equals $sin(\theta)$ which is v_q divided by the voltage amplitude. The diagram above can be redrawn using a small signal model as shown in Figure 3.4, where the input and output are the quadrature signals (neglecting the variation of the amplitude).

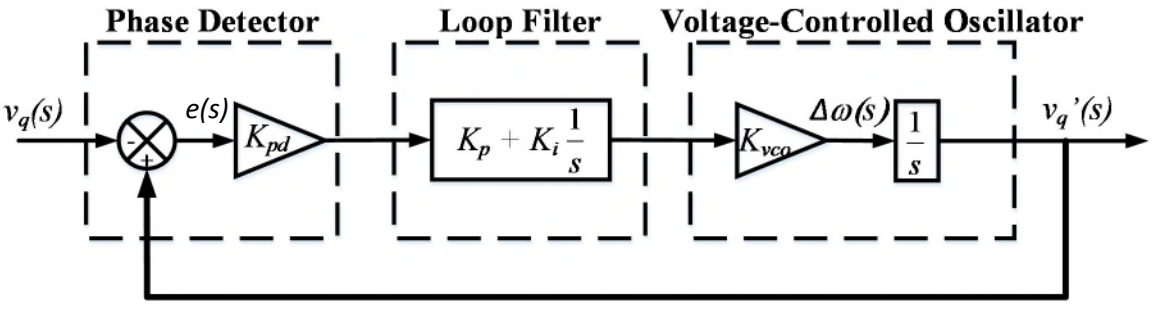


Figure 3.3 Block diagram of SRF-PLL small signal model

Since the input signal is small and θ equals $sin(\theta)$, the output will be small as well. Therefore θ' equals $sin(\theta)$. In this case, $K_{pd} = K_{vco} = 1$ where K_{pd} is the gain introduced by phase detector

It is clear that with the closed loop diagram given above, the SRF-PLL system can be analysed by the transfer function below:

$$H(s) = \frac{v_q(s)}{v_q'(s)} = \frac{K_p s + K_i}{s^2 + K_p s + K_i} \tag{3.1}$$

The closed-loop error transfer function is:

$$E(s) = 1 - H(s) = \frac{s^2}{s^2 + K_p s + K_i} \tag{3.2}$$

It is clear that the system closed-loop transfer function shows a typical second order system characteristic. The equation can be rewritten into a generalized second order transfer function format:

$$H(s) = \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{3.3}$$

$$E(s) = \frac{s^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{3.4}$$

where

$$\omega_n = \sqrt{K_i} \tag{3.5}$$

$$\xi = \frac{K_p}{2\sqrt{K_i}} \tag{3.6}$$

where ω_n is the undamped natural frequency and ξ is the damping ratio.

It is usually desired that the damping ratio of a second order system to be around $\sqrt{2}/2$ for the optimum response. The undamped natural frequency thus the integral gain K_i of the PI controller and the damping ratio ξ together decide the response time of the system. The settling time of the system is proportional to the time constant under certain damping ratio. With the

settling time defined by the design specification, the gains of the PI controller can be decided accordingly. Generally, the settling time is defined as the time from the start of the unit step input to the time when the error decreases to 1% of the step input. An approximate mathematic relationship between the settling time of the system and the time constant is given below.

$$t_s = 4.6\tau \tag{3.7}$$

where

$$\tau = \frac{1}{\xi\omega_n} \tag{3.8}$$

If the desired settling time of the PLL system is given as t_s, the optimum K_p and K_i are:

$$K_p = 2\xi\omega_n = \frac{9.2}{t_s} \tag{3.9}$$

$$K_i = \omega_n{}^2 = \frac{21.16}{\xi^2 t_s^2} \tag{3.10}$$

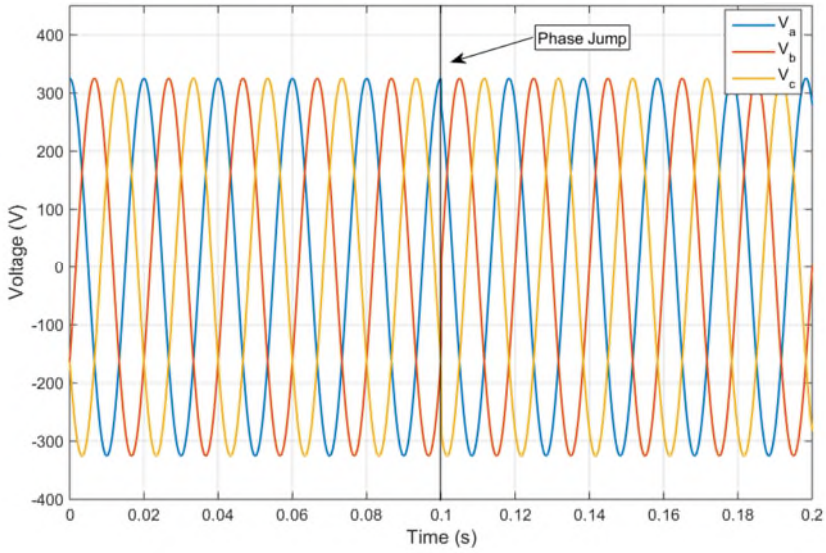
where

$$\xi = \frac{\sqrt{2}}{2} \tag{3.11}$$

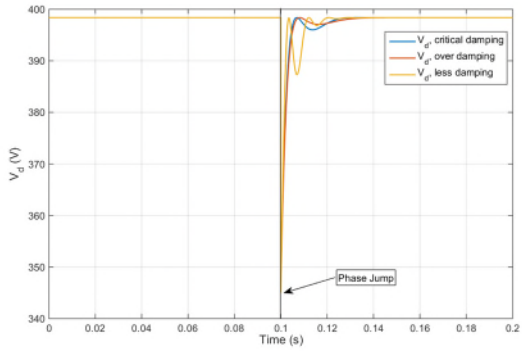
It is worth noting that the transfer function and the PI tuning technique discussed above are built on the small signal model where the deviation of the input is assumed relatively small. If the variation is significantly bigger and is not negligible when compared to the direct signal, the above transfer function is no longer valid. The approximation $sin(\theta)$ equals θ is not acceptable and linearization around a larger θ leads to a smaller K_{pd}. This indicates that the PLL system tends to react slower for a bigger input signal and the system dynamics should also be redefined as the damping ratio changes. Therefore the equations above can be used as a

guidance for tuning the system but not to be used to predict the global response of the SRF-PLL system.

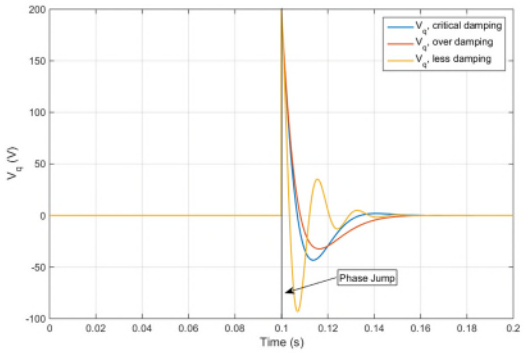
The following diagram, Figure 3.4, shows the SRF-PLL response with different parameter settings to achieve settling time 0.04s with different damping ratios guided by the Equation 3.7. The input signal is the voltage of a three-phase, 230V system. A 30 degree phase jump is applied at t=0.1 second.



(a)



(b)



(c)

Figure 3.4 Transient response of the SRF-PLL to phase jump with parameters set to produce critical-damping, over-damping and under-damping following a small signal model

(a) three-phase voltage waveform; (b) response of V_d estimation; (c) response of V_q estimation

As mentioned above, the PI controller which acts as the loop filter in the SRF-PLL system has a low-pass filtering characteristic and this results in tracking errors when the PLL input is not constant. For the original purpose of deploying the SRF-PLL, the signals of interest are the phase angle and amplitude of the three phase input. During an unbalanced grid fault, the symmetrical components in the positive and negative sequences have their unique characteristics on the *dq* reference frame. The positive sequence signal will appear on the dq reference frame defined by the PLL system as d.c. signals, the same as the balanced inputs when the grid is in the normal condition. However, the negative sequence will appear as second harmonic oscillation in the same *dq* reference frame; this will actually deteriorate the performance of the system. For voltage oriented control and other control methods utilizing PI controllers based on the *dq* reference frame, which will be introduced in the later sections, the oscillating input will cause tracking problems and sometimes, stability problem of the current controller. This is highly undesirable. There are a few research studies [88, 89] to show that the problems brought about by the oscillation of the *dq* signal inputs to the PLL system can be resolved by reducing the band width of the loop filter, however the background of the these discussions are usually the oscillation caused by high order harmonics. For oscillation brought about by the negative sequence, it is at the second harmonic frequency in the reference frame which is much lower than that caused by the common harmonics e.g. the sixth harmonic frequency oscillation caused by the 5^{th} and 7^{th} harmonics in the a.c. input signal. The bandwidth of the loop filter should be tuned really low for attenuating the oscillation at the second harmonic frequency, which severely harms the dynamic performance. For conventional voltage oriented current control with voltage sensors installed, the current reference generated from the utility voltage in order to achieve the desired control objective such as following the power references, the poor dynamic response of the PLL system would result in slow power control against the utility voltage variation. For the a.c. voltage-sensor-less control, the PLL system is

applied to the estimated voltage signals which are coupled to the current measurements. The current control stage following the PLL system needs to be tuned accordingly, but this can result in very poor dynamic response. The poor dynamic response of the PLL system would also harm the overall system performance including stability. The need for controlling the negative phase sequence will not be satisfied without additional system to extract relevant phase sequence information. SRF-PLL alone is not a solution to the control system if considering the unbalanced utility voltage. Figure 3.5 shows a typical unbalanced a.c. side voltage waveform and Figure 3.6 shows the simulation results of the PLL output under such an unbalanced grid voltage condition.

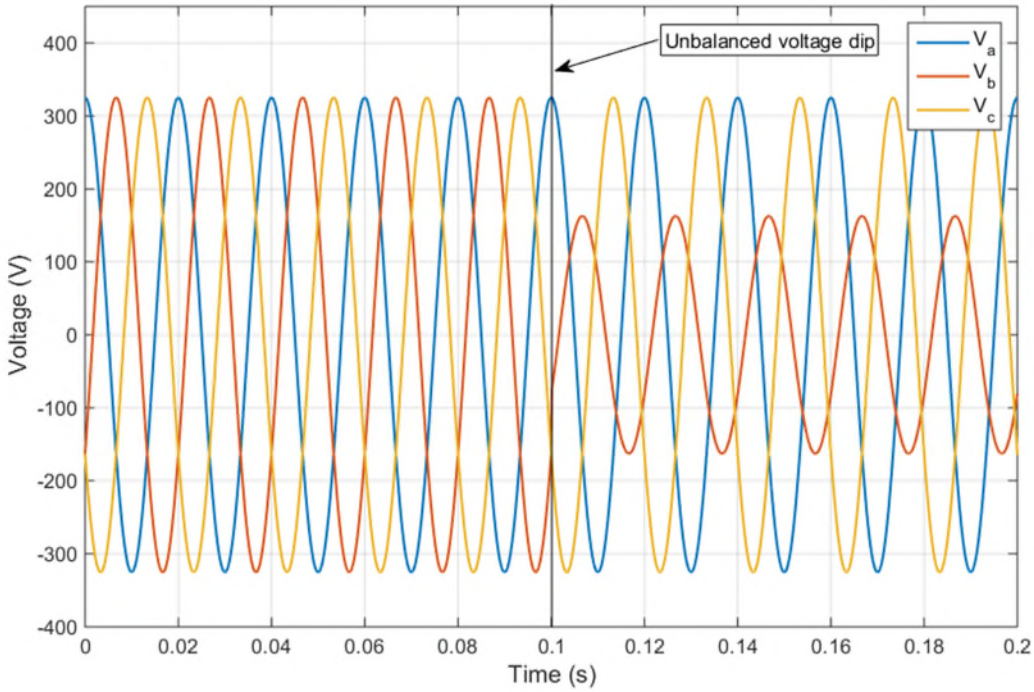


Figure 3.5 Three phase voltage during single phase voltage dip

The above discussion has shown the cause of SRF-PLL performance deterioration under unbalanced grid voltage condition. The input signals to the SRF-PLL system need to be symmetrical; in other words they should result in constant values when transformed into the *dq* reference frame. To achieve this, the original signals should be decomposed into

symmetrical components so that signals in each phase sequence are balanced and hence can be used to drive the relevant SRF-PLL system. Because of that, this study proposes a sequence decomposition mechanism prior to the SRF-PLL stage. This can be viewed as a modified version of the original SRF-PLL system. Two versions of implementing the concept are detailed in the following sections.

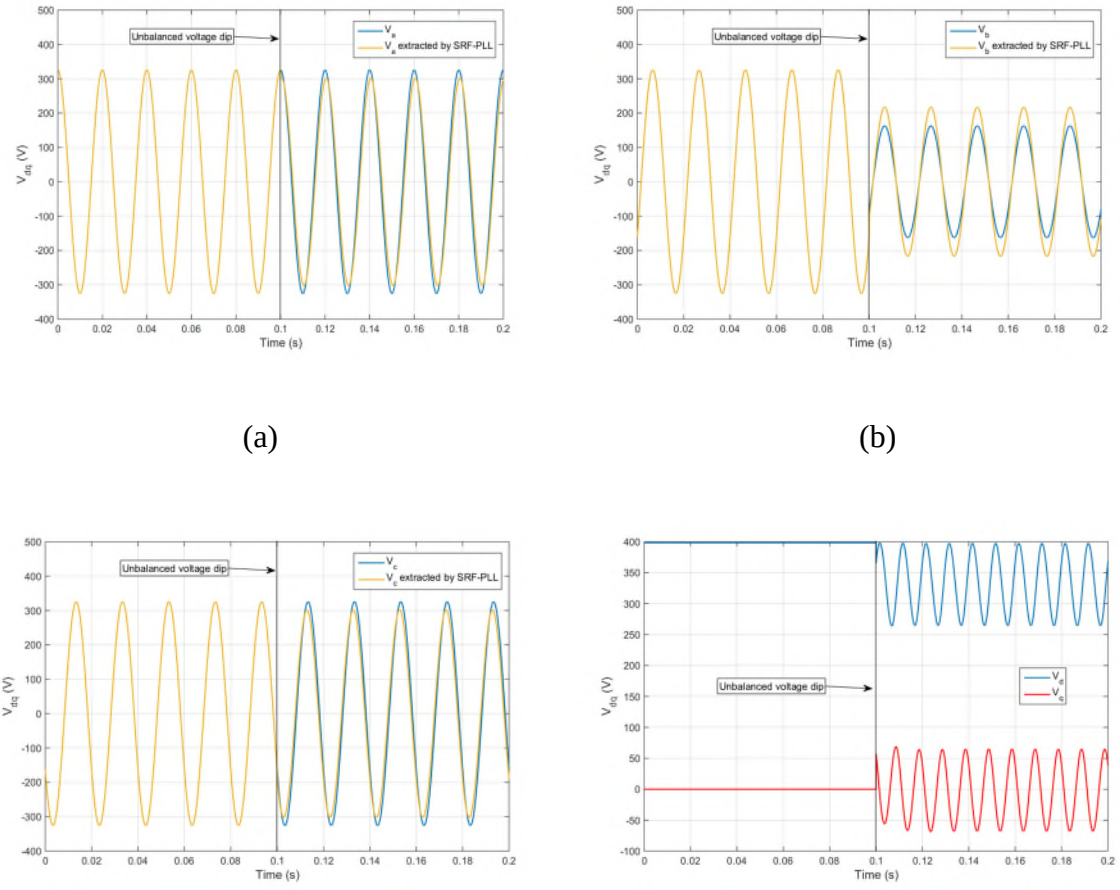


Figure 3.6 Output of the SRF-PLL during single-phase voltage dip and tracking error

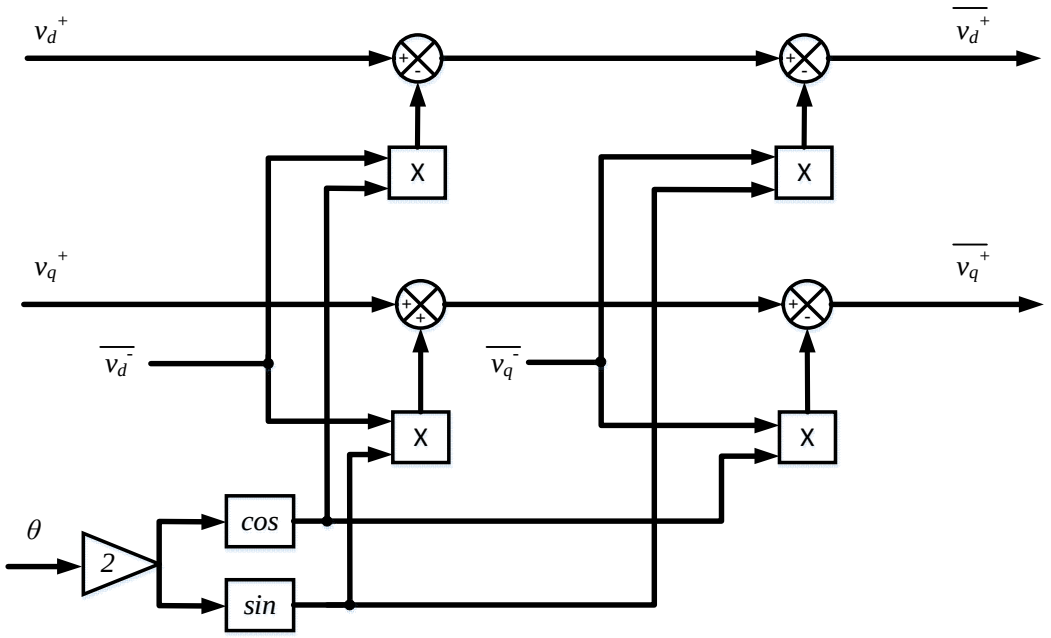
(a) Phase A output and actual value; (b) Phase B output and actual value

(c) Phase C output and actual value; (d) *dq* values

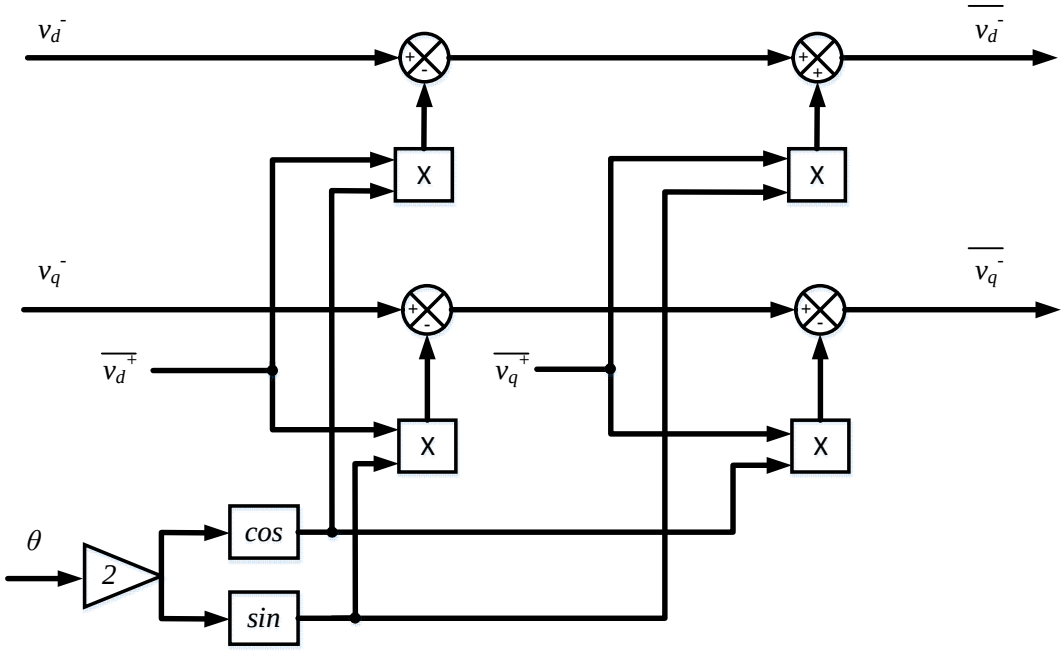
3.3 Decoupled double synchronous reference frame phase locked loop

It is clear that the SRF-PLL alone is not a proper solution for extracting information from unbalanced three-phase signals due to the effect of the negative sequence and the inability of the SRF-PLL to track a none constant reference. Therefore, a mechanism that can remove the oscillating components under unbalanced three-phase inputs becomes a necessity to cope with unbalanced utility voltages.

The DD (decoupled double reference frame) SRF-PLL [92-94] is a modified version of the original SRF-PLL which decomposes the positive and negative sequences by analytical calculation. Utilizing the characteristic of the symmetrical components on the synchronised rotational reference frame, the DD-SRF-PLL has two synchronous reference frames rotating in opposite directions to lock the phase of the positive and negative sequences respectively. As discussed in the previous section, for a 50Hz system, the negative sequence component will appear in the positive sequence reference frame as a 100 Hz oscillation and vice versa. To extract the positive sequence from the total, the negative sequence values are fed to the positive one through a decoupling network where the reference frame is changed to cancel out the effect of the oscillation. The negative sequence is extracted in the same way. As the rotational direction of the positive and negative sequence are opposite, the direction of the q-axis are different in the two cases. Therefore the feedback signal has different signs in each decomposition network. Since the symmetrical components are extracted and the direct and quadrature signals of the positive or negative sequence are now ripple free, the conventional SRF-PLL can be employed for driving the quadrature signal to zero. Figure 3.7 shows the configuration of the decoupling network for the positive and negative sequences.



(a) Positive sequence



(b) Negative sequence

Figure 3.7 Decomposition network of DD PLL: (a) positive sequence; (b) Negative sequence

The output of the decoupling network for each phase sequence are then filtered using a first order low-pass filter in order to stabilize the system by removing the high frequency oscillation during transient. The complete system is shown in Figure 3.8. The low-pass filter is tuned with a cut-off frequency of $1/\sqrt{2}$ time of the fundamental frequency as suggested by [92].

However, such a low-pass filter will introduce a significant delay, and hence poor transient response. Therefore the system response will be largely limited by the time constant of the low-pass filter. Since the symmetrical components are extracted by the decoupling network, the positive sequence v_q can be used to drive the conventional SRF-PLL for the phase angle as well as the grid frequency.

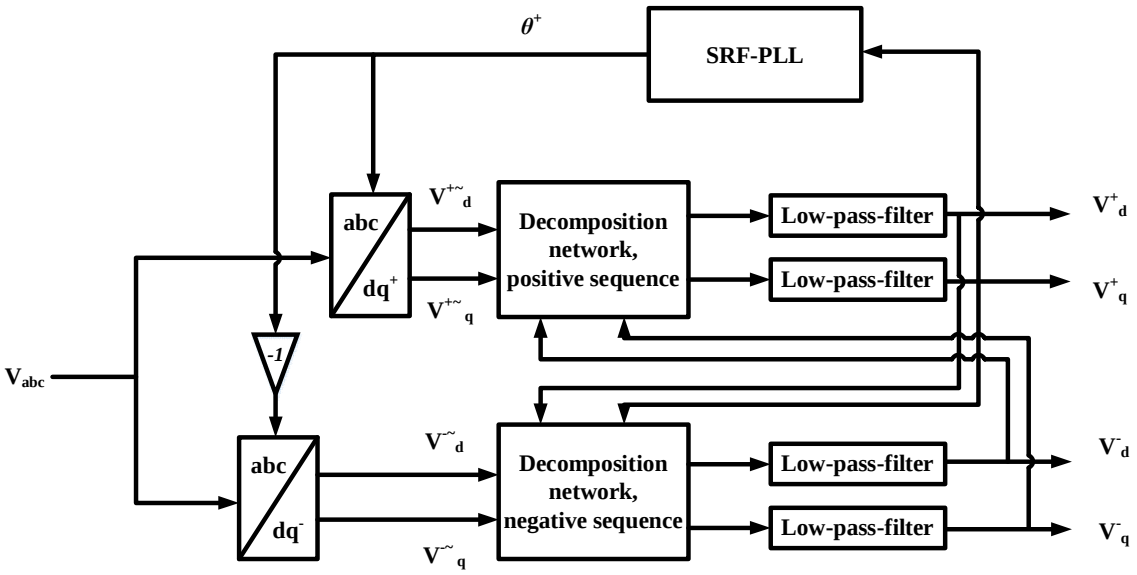


Figure 3.8 Close loop diagram of DD PLL

In summary, the DDSRF-PLL utilizes two *abc-dq* transformations, eight adding computations and four low-pass-filters in the symmetrical components decomposition stage which clearly shows a higher computational burden comparing to other methods. Therefor the system response will be largely limited by this value.

3.4 Cascaded delay method

This method has not yet been used elsewhere for converter grid synchronisation, but the idea has been widely used in power system relaying for extracting the negative sequence component during abnormalities. The values of the measured utility voltage are delayed by 1/6 of the

fundamental period. As the positive sequence and the negative sequence voltages are rotating in the opposite directions, the positive (or negative) sequence in the delayed signals will have the negative value of the original. E.g. the delayed positive sequence voltage value of phase A will be the negative value of the original of phase C. The diagram below (Figure 3.9) demonstrates the placement of the original and delayed phasors.

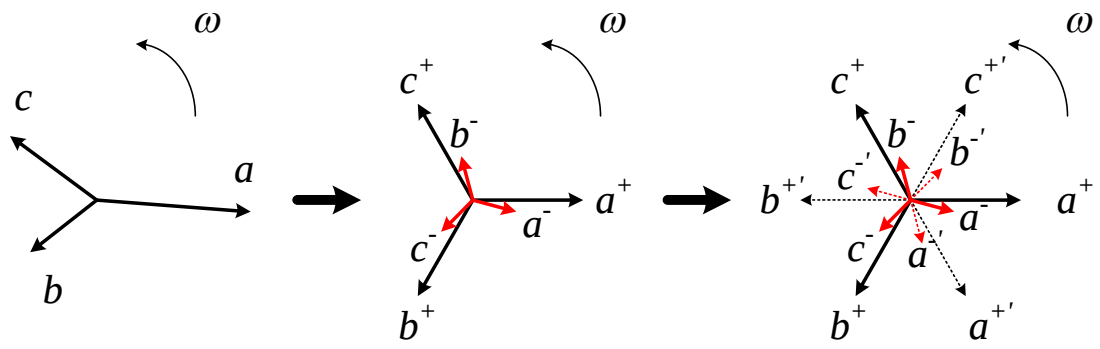


Figure 3.9 Unbalanced three phase signals and the vector placement of the symmetrical components before and after applying 1/6 fundamental period delay

It is clear that the combined phasor has one of the sequence components removed but the remaining one is both amplified and phase shifted. Therefore the combined phasor needs to be compensated. The original positive sequence and negative sequence signals can be reconstructed by calculations using the original and the delayed signals. For example, the positive sequence value of phase A is calculated by:

$$a_{real-time} + c_{delayed} = a^{+}\angle\theta + a^{+}\angle(\theta - \frac{\pi}{3}) + a^{-}\angle\varphi + a^{-}\angle(\varphi - \pi) = \sqrt{3}\cdot a^{+}\angle(\theta + \frac{\pi}{6}) \qquad 3.12$$

Thus

$$a^{+} = \frac{\sqrt{3}}{3}\cdot(a_{real-tiem} + c_{delayed})\angle(\phi - \frac{\pi}{6}) \qquad 3.13$$

where the $a_{real\text{-}time}$ and $c_{delayed}$ are the measured signals; a^+ and a^- are the values of positive and negative sequence respectively; θ, φ and ϕ are the phase angle of the positive sequence and negative sequence of phase A and the combined phasor.

The values of the positive and negative sequences of other phases can be similarly calculated. The expressions for the values of positive and negative sequence of all phases are listed below:

$$a^+ = \frac{\sqrt{3}}{3} \cdot (a_{real-tiem} + c_{delayed}) \angle (\phi_{ac} - \frac{\pi}{6}) \quad 3.14$$

$$b^+ = \frac{\sqrt{3}}{3} \cdot (b_{real-tiem} + a_{delayed}) \angle (\phi_{ba} - \frac{\pi}{6}) \quad 3.15$$

$$c^+ = \frac{\sqrt{3}}{3} \cdot (c_{real-tiem} + b_{delayed}) \angle (\phi_{cb} - \frac{\pi}{6}) \quad 3.16$$

$$a^- = \frac{\sqrt{3}}{3} \cdot (a_{real-tiem} + b_{delayed}) \angle (\phi_{ab} + \frac{\pi}{6}) \quad 3.17$$

$$b^- = \frac{\sqrt{3}}{3} \cdot (b_{real-tiem} + c_{delayed}) \angle (\phi_{bc} + \frac{\pi}{6}) \quad 3.18$$

$$c^- = \frac{\sqrt{3}}{3} \cdot (c_{real-tiem} + a_{delayed}) \angle (\phi_{ca} + \frac{\pi}{6}) \quad 3.19$$

With the signals of positive and negative sequence decomposed, again a standard SRF-PLL can be used to carry out *dq* transformation needed for control purposes. One thing worth mentioning is that similar methods can be used on harmonic detection, as reviewed in [95-101]. In this study, a fast symmetrical component decomposition method is proposed only for decomposing positive and negative sequence, these methods will be useful to expand the proposed symmetrical component decomposition algorithm to be adaptive to even more harmonic-polluted grid conditions.

3.5 Notch-filtering method

By applying Park Transformation, we can transfer the a.c. values on three-phase reference frame to d.c. values on the synchronised reference frame. The input signals containing both positive and negative sequence signals can be expressed as:

$$x_a = A\sin(\omega t + \phi^+) + B\sin(-\omega t + \phi^-) \tag{3.20}$$

$$x_b = A\sin(\omega t + \phi^+ - \frac{2\pi}{3}) + B\sin(-\omega t + \phi^- - \frac{2\pi}{3}) \tag{3.21}$$

$$x_c = A\sin(\omega t + \phi^+ + \frac{2\pi}{3}) + B\sin(-\omega t + \phi^- + \frac{2\pi}{3}) \tag{3.22}$$

where A and B are the amplitudes and ϕ^+ and ϕ^- are the phase angles of positive and negative sequence signals respectively, and ω is the rotational speed of the vectors in rads/s.

Given the transformation matrix of Park Transformation:

$$\begin{pmatrix} x_d \\ x_q \\ x_0 \end{pmatrix} = \frac{2}{3}\begin{pmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin(\theta) & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{pmatrix} \cdot \begin{pmatrix} x_a \\ x_b \\ x_c \end{pmatrix} \tag{3.23}$$

Let the transformation be synchronised to the direction of the positive sequence by defining the angle of the d-axis as:

$$\theta = \omega t \tag{3.24}$$

The d and q components on the synchronised reference frame after applying the transformation are: $x_d = A\cdot\cos(\phi^+) - B\cdot\sin(2\omega t - \phi^-)$ (3.25)

$$x_q = -A \cdot \sin(\phi^+) - B \cdot \sin(\omega t - \phi^- - \frac{\pi}{2}) \quad 3.26$$

The expression of x_d and x_q shows that by applying the Park transformation to an unbalanced three phase signals by defining the rotational direction of the *dq* reference frame by the direction of the positive sequence, the *d* and *q* components of the positive sequence are d.c. values while the effect of the negative sequence becomes an oscillation with the same amplitude of the negative sequence signals. Thus we can extract the positive sequence signals by filtering out the oscillation cause by negative sequence signals. Different types of filters are used to carry out such a function proposed in [96, 102-105]. As the frequency of the oscillation is known as twice of the fundamental frequency from the expressions above, a notch-filter is an ideal solution to carry out the filtering for its high rejection ratio to a certain frequency component [106-109].

The transfer function of the notch filter is given below:

$$G(\mathrm{s}) = \frac{s^2 + \omega_c^2}{s^2 + 2 \cdot \varepsilon \cdot \omega_c + \omega_c^2} \quad 3.27$$

where ω_c is the central frequency of the notch filter and ε is the quality factor which affect the frequency selectivity of the notch filter.

By applying the notch filter with the central frequency designed the same frequency to oscillation of the x_d and x_q, the negative component will be eliminated from the *d* and *q* components of the transformation. Thus the information of the positive sequence is extracted.

However, in reality, the fundamental frequency will not stay at its nominal value e.g. 50Hz. The frequency variation in the distribution network is especially frequent. For conventional use of the notch filter whose central frequency is fixed, the high frequency selectivity will cause the very limited attenuation to the none-central frequency components. As the target frequency would be two times of the fundamental frequency, the attenuation rate of the target frequency

component will be reduced if the grid frequency is not its nominal value. Therefore the notch filter should be designed to be adaptive to frequency deviation.

In order to achieve frequency adaption, a simple method could be considered. In spired by the experience from when using PR controller for current control purposes, the quality factor of the notch filter can be reduced in order to reduce the frequency selectivity [108]. The ideal PR controller is not practical in reality. A damping factor will be added to the denominator of the transfer function. So that the PR controller is immune to the problems, which will be discussed in the later section in detail, caused by difference between the set resonance frequency and the real frequency. Similarly, if the frequency selectivity of the notch filter is reduced, the none-central frequency components therefore will also fall into the suspension frequency range. Depending on the damping factor selected, the range of frequency that will be rejected in the output varies. It can be verified in Figure 3.11 that rejection band gets wider for higher damping factor. This method is regarded as the passive adaptive approach. However, two drawbacks of this solution are identified. Firstly, the reduction of the quality factor would also reduce the gain at the central frequency. As a result the steady state error will increase. Secondly, although a wider range of frequency components are attenuated, the attenuation rate of the none-central frequency components will not be as high as the central frequency which would cause higher steady state error under fundamental frequency deviation.

An alternative solution for achieving frequency adaptive would be adjusting the central frequency according to the fundamental frequency [109] as shown in Figure 3.10. The value of the fundamental frequency is fed into the notch filter from frequency tracking mechanism such as the phase-locked-loop or the frequency-lock-loop so that the central frequency can be adjusted in real time. However, this method requires careful tuning of the system providing the value of the fundamental frequency which increases the difficulty for designing the control

parameters. The band-width of the PLL system should be reduced in order to stabilize the system which further harms the dynamic response as shown in Figure 3.12.

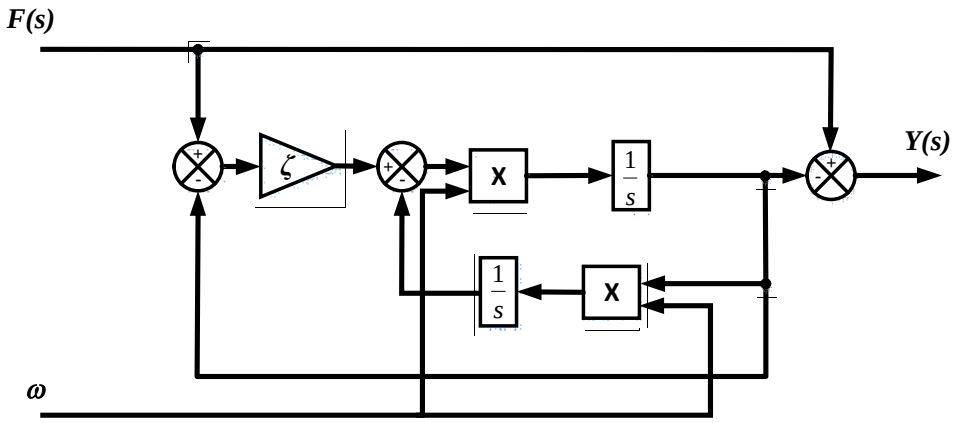


Figure 3.10 Block diagram of frequency adaptive notch filter

Similarly, the information of negative sequence component can be extracted by filtering x_d and x_q acquired from the same transformation matrix but defining the angle θ of the d-axes as:

$$\theta = -\omega t \qquad 3.28$$

The reference frame will be synchronised to negative sequence in this way, thus the positive sequence become the oscillation and can be removed by the notch filter.

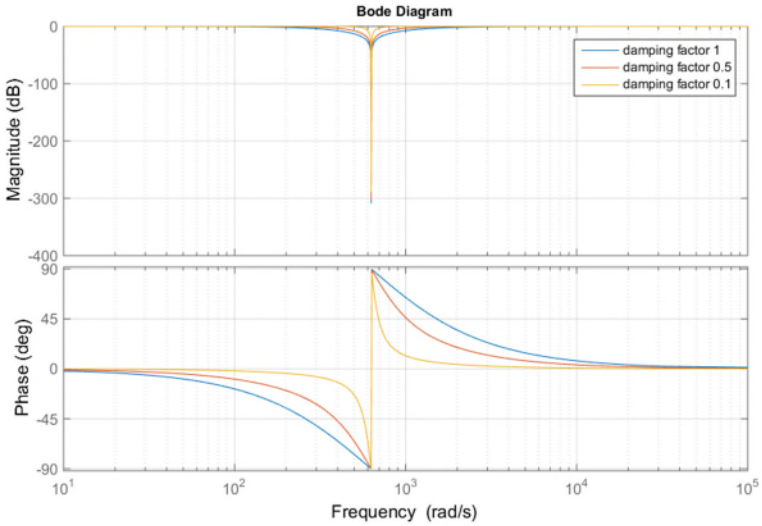


Figure 3.11 Bode diagram of the notch filter

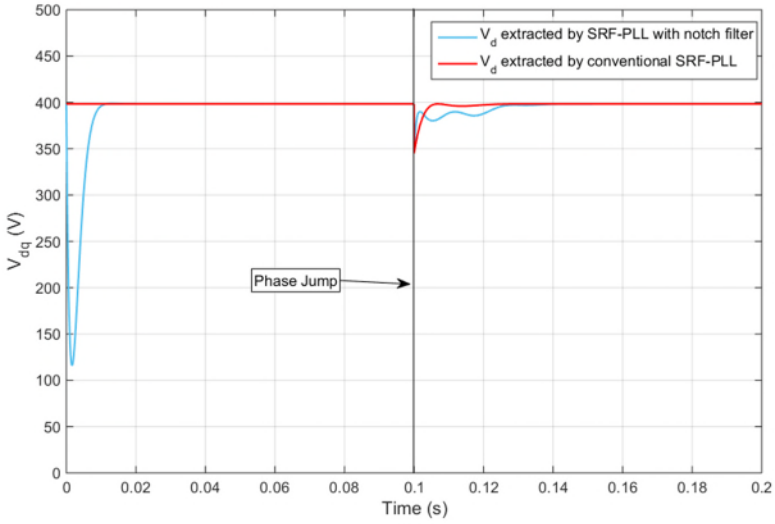


Figure 3.12 Effect of delay caused by notch filter responding to a phase jump

One thing worth noting is that the frequency component rejected shown in the diagram is the frequency component on the *dq* reference frame which means the origin of the frequency-axis is actually the frequency of the reference frame on the natural reference frame in a general case (during both transient and steady state). Therefore, specifying that the PLL system is in its steady state, the 100 Hz component is not only caused by the negative sequence also can be result of a third order harmonic [110]. Thus this technique rejects the negative sequence components as well as the third order harmonics. In the real power systems, the unbalanced utility usually contains even order harmonics e.g. 5^{th} and 7^{th} harmonics as well, where the 5^{th} harmonic is a negative sequence frequency component and 7^{th} is a positive sequence one. On the synchronised rotational reference frame, they will appear in form of a 6^{th} order harmonic which can be also rejected using a single notch filter. Thus the use of this technique can be also expanded by cascading several notch filters for harmonic rejection. However, the additional notch filter further harms the dynamic response of the system which is a side effect should be taken into consideration when applying this technique to a control system.

3.6 A new decomposing method proposed in this study

The idea of using cascaded delay to reject one phase sequence from the total was usually based on how the specific sequence could be cancelled out in the fundamental waveform e.g. applying a 1/6 cycle delay to cancel out the specific sequence signal of the adjacent phase or the SOGI-QSG method which achieved decoupling in the stationary $\alpha\beta$ reference frame. The filtering method of utilizing notch filter to extract positive/negative sequence signals has the advantage of robustness. However, each method introduces delay which is not negligible as compared to the fundamental period. Such delay is highly undesirable in the control system that relies on fast estimation of the symmetrical components. It can be seen from the *dq* signal filtering method that by applying *abc-dq* transformation with the reference frame rotating in the positive sequence, the negative sequence will appear in the output as oscillation with frequency at the sum of the negative sequence frequency and the *dq* reference frame rotational frequency, and vice versa. The property of frequency increase for a certain sequence can be further extended by defining a rotational reference frame which has a higher frequency than the fundamental frequency. The new decoupling method utilizes this property by introducing the cascaded signal delay to carry out positive and negative sequence decoupling. By defining a reference frame rotating faster than the fundamental frequency, the time delay needed for removing the signal of the targeted sequence in the opposite direction can be reduced.

The proposed decoupling scheme is driven by an angular reference which has the same frequency as the input signal. This frequency is estimated by an additional system such as a Phase-Locked-Loop (PLL) or a Frequency-Locked-Loop (FLL) which is regarded as the angular reference generator to set the fundamental angular reference θ^{+}. The generated angular reference is multiplied by an integer gain N_{res} to define the rotational reference frame dq_{res} where the positive and negative sequence signals are going to be decomposed. Then another reference frame transformation is introduced to transform the purified positive or negative

sequence signals back to the synchronised reference frame (dq_{res}) at the fundamental frequency. The diagram shown below in Figure 3.13 provides an overview to the decomposing system for extracting the positive sequence signals.

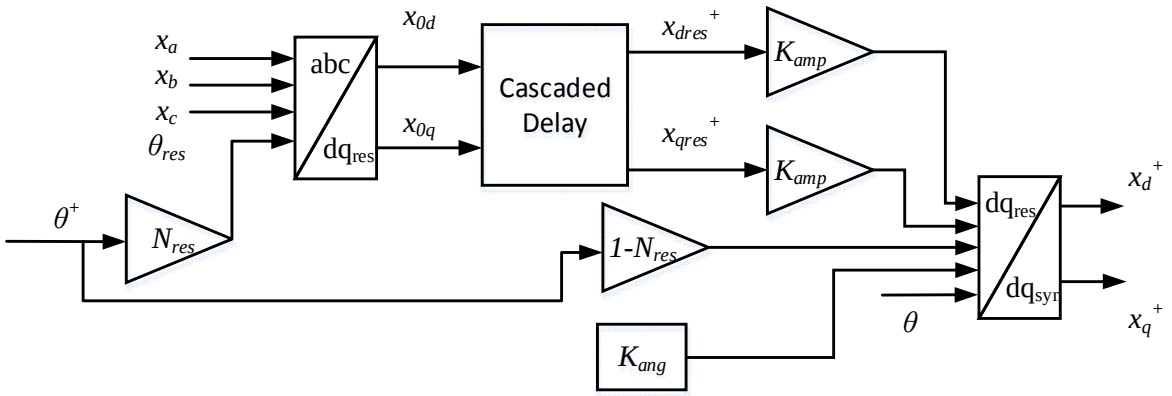


Figure 3.13 Proposed decomposing system for extracting the positive sequence signal

The time delay needed depends on the relationship between the control parameter N_{res} and the component to be removed, which in this case is the negative sequence component at the fundamental frequency. The time delay is applied to the components in the *dq* reference frame as to be shown later in this section. Because the cascaded time delay will have its effects on both the positive and the negative sequences, while the negative sequence is rejected, the positive sequence needs to be compensated. The compensations of the amplitude and the phase angle both depend on the value of the time delay introduced and thus also depend on N_{res}.

The cascaded delay structure is shown in Figure 3.14:

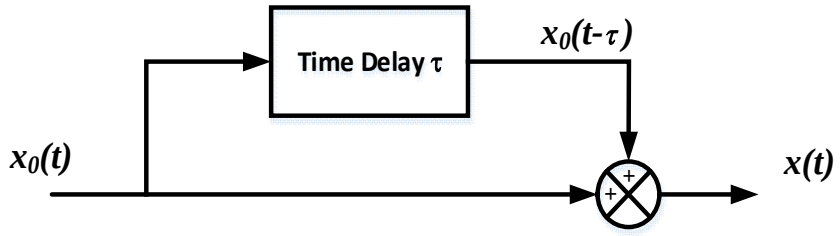


Figure 3.14 Structure of cascaded delay unit

Let the input signal $x_0(t)$ be:

$$x_0(t) = A \cdot \sin(\omega t + \varphi) \tag{3.29}$$

where A and ω are the amplitude and angular frequency of the input signal, and φ its initial angle.

The delayed signal $x_0(t-\tau)$ can be expressed as:

$$x_0(t-\tau) = A \cdot \sin(\omega t + \varphi - \gamma) \tag{3.30}$$

where γ is the phase shift introduced by the delay and hence

$$\gamma = \tau \cdot \omega \tag{3.31}$$

Thus the output *x(t)* is:

$$x(t) = x_0(t) + x_0(t-\tau) = 2 \cdot A \cdot \cos(\frac{\gamma}{2}) \cdot \sin(\omega t + \varphi - \frac{\gamma}{2}) \tag{3.32}$$

The Bode plot is shown in Figure 3.15 where f_{fund} is the normal gird frequency e.g. 50Hz.

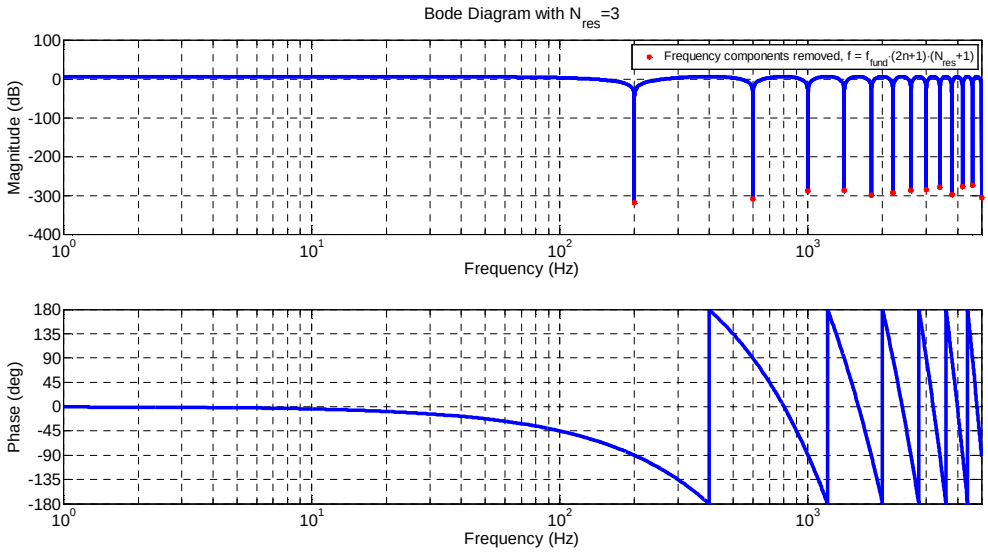


Figure 3.15 Bode diagram of cascaded delay unit

It is clear from the expression above that for a given τ, a frequency component will be removed (or significantly suppressed) from the input due to the cascaded delay if its angular frequency is:

$$\omega = \frac{(2n-1)\cdot\pi}{2\tau} \tag{3.33}$$

where *n* is a positive integer.

As mentioned before, with a reference frame rotating in the same direction as the positive sequence, the negative sequence will appear in the output as an oscillation with frequency as the sum of the negative sequence frequency and the frequency of the reference frame. Knowing that N_{res} is the control parameter which defines the frequency of the rotation of the reference frame, it is possible to calculate τ needed for rejecting the negative sequence signals in the *dq* reference frame.

$$\tau = \frac{\pi}{(N_{res}+1)\cdot\omega_f} \tag{3.34}$$

where ω_f is the fundamental frequency.

The compensation for amplitude and angle (rad) of the positive sequence signal can also be calculated as:

$$K_{amp} = \frac{1}{2\cdot\cos(\frac{N_{res}-1}{N_{res}+1}\cdot\frac{\pi}{2})} \tag{3.35}$$

$$K_{ang} = \frac{N_{res}-1}{N_{res}+1}\cdot\frac{\pi}{2} \tag{3.36}$$

It is worth mentioning that while some of the frequency components are removed from the signal, some others are amplified. Thus the control parameter N_{res} needs to be carefully selected to avoid introducing harmful harmonics into the system.

Like in any other control systems, the error between the reference value and output will appear during the transient. It is useful to quantify this error in order to evaluate the quality of the algorithm. The transient error of this symmetrical components decomposition algorithm is introduced by the miss-match between the information of the past time held by the cascaded delay unit and the real time signal when a step change (e.g. a balanced signal change or the signals became unbalanced) appears. Based on this understanding, the following section aims to derive the equation to quantify the transient error caused by a certain type of input change.

Considering a three-wire grid system where zero sequence voltage does not exist, the three phase input signals before the negative phase sequence component is added in are:

$$\begin{pmatrix} x_{0a} \\ x_{0b} \\ x_{0c} \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} \cos\theta_{syn} & -\sin\theta_{syn} \\ \cos(\theta_{syn} - \frac{2}{3}\cdot\pi) & -\sin(\theta_{syn} - \frac{2}{3}\cdot\pi) \\ \cos(\theta_{syn} - \frac{2}{3}\cdot\pi) & -\sin(\theta_{syn} + \frac{2}{3}\cdot\pi) \end{pmatrix} \cdot \begin{pmatrix} x_d \\ x_q \end{pmatrix} \qquad 3.37$$

where, θ_{syn} is the angle reference that defines the synchronous reference frame.

After the step change, assuming that the fundamental frequency of the input signals is not changed, the three phase input signals become:

$$\begin{pmatrix} x_a \\ x_b \\ x_c \end{pmatrix} = \underbrace{\sqrt{\frac{2}{3}} \begin{pmatrix} \cos\theta_{syn} & -\sin\theta_{syn} \\ \cos(\theta_{syn} - \frac{2}{3}\cdot\pi) & -\sin(\theta_{syn} - \frac{2}{3}\cdot\pi) \\ \cos(\theta_{syn} - \frac{2}{3}\cdot\pi) & -\sin(\theta_{syn} + \frac{2}{3}\cdot\pi) \end{pmatrix} \cdot \begin{pmatrix} x_d^+ \\ x_q^+ \end{pmatrix}}_{Positive\ Sequence} + \underbrace{\sqrt{\frac{2}{3}} \begin{pmatrix} \cos(-\theta_{syn}) & -\sin(-\theta_{syn}) \\ \cos(-\theta_{syn} - \frac{2}{3}\cdot\pi) & -\sin(-\theta_{syn} - \frac{2}{3}\cdot\pi) \\ \cos(-\theta_{syn} - \frac{2}{3}\cdot\pi) & -\sin(-\theta_{syn} + \frac{2}{3}\cdot\pi) \end{pmatrix} \cdot \begin{pmatrix} x_d^- \\ x_q^- \end{pmatrix}}_{Negative\ Sequence} \qquad 3.38$$

Where x_d^+, x_q^+, x_d^- and x_q^- are the direct and quadrature signals of the positive and negative sequence components respectively.

Assuming that the frequency input to the decomposing unit is always locked to the positive sequence component of the input signal and the dynamics of the PLL is ignored, applying *abc-dq* transformation to the input signals results in the outputs of the cascaded delay unit as:

$$\begin{pmatrix} x_{dres}^+ \\ x_{qres}^+ \end{pmatrix} = \sqrt{\frac{2}{3}} \cdot K_{amp} \begin{pmatrix} \cos(\theta_{res}) & \cos(\theta_{res} - \frac{2}{3}\cdot\pi) & \cos(\theta_{res} + \frac{2}{3}\cdot\pi) \\ -\sin(\theta_{res}) & -\sin(\theta_{res} - \frac{2}{3}\cdot\pi) & -\sin(\theta_{res} + \frac{2}{3}\cdot\pi) \end{pmatrix} \begin{pmatrix} x_a + x_{0a} \\ x_b + x_{0b} \\ x_c + x_{0c} \end{pmatrix} \qquad 3.39$$

where θ_{res} is the angle to define the rotational reference frame $dq_{res.}$

As mentioned above, the rotational reference frame where the delay is made on, rotates faster than the fundamental frequency components, the output needs to be transformed back to the synchronised reference frame. The final output of the decomposing system is:

$$\begin{pmatrix} x_d^+ \\ x_q^+ \end{pmatrix} = \begin{pmatrix} \cos(\theta_{rev} + K_{ang}) & -\sin(\theta_{rev} + K_{ang}) \\ \cos(\theta_{rev} + K_{ang} - \frac{\pi}{2}) & -\sin(\theta_{rev} + K_{ang} - \frac{\pi}{2}) \end{pmatrix} \begin{pmatrix} x_{dres}^+ \\ x_{qres}^+ \end{pmatrix} \qquad 3.40$$

where θ_{rev} is the angle difference between the decomposed synchronised reference and the faster rotational reference frames dq_{res}.

$$\theta_{rev} = (1 - N_{res}) \cdot \theta_{syn} \qquad 3.41$$

Knowing the original positive sequence signal (x_{dref}^+, x_{qref}^+ as in Equation 3.39) and the positive sequence signal obtained using the algorithm after introducing the negative sequence as a step change (x_d^+ , x_q^+ from Equation 3.40), the following indices can be used to measure the performance of the algorithm.

$$e_{IAEd} = \int_0^{\tau} \left| x_d^+ - x_{dref}^+ \right| dt \qquad 3.42$$

$$e_{IAEq} = \int_0^{\tau} \left| x_q^+ - x_{qref}^+ \right| dt \qquad 3.43$$

The integral of absolute error (IAE) of the transient stage based on the error between the output of x^+ and x^- and their actual values will be used as a reference to demonstrate the quality of the decomposing units under different conditions. A plot of IAE during the transient stage of a particular case will be provided in the Chapter 7.

3.7 Chapter Summary

In this chapter, the grid synchronisation methods especially those capable of working under the unbalanced three phase signals are reviewed. A new symmetrical component decomposition method is developed in this research and its mechanism has been introduced in this chapter. It is developed to reduce the delay introduced comparing to the conventional methods. The detailed comparison are shown in the simulation results placed in Chapter 7. As introduced in the previous sections, the grid synchronisation and the symmetrical component decomposition are very important to the performance of the current control system. The transient response directly affect the transient performance of the a.c. voltage-sensor-less current control system. As for the a.c. voltage-sensor-less system, the symmetrical component decomposition method is especially important because of the topology of the proposed current control system: the only feed-back from the a.c. side are the phase current signals where the symmetrical components are decomposed and grid voltage are estimated based on each phase sequence. This will be detailed in Chapter 5. The delay introduced by the symmetrical component decomposition system should be reduced to improve the transient performance of the whole control system.

Chapter 4 Technical challenges to the grid connected converter system

4.1 Voltage dips and phase jump

A voltage dip describes the situation where the grid voltage deviates considerably below its nominal value. It is most often caused by electrical faults and sudden change of the load somewhere in the grid and has different forms depending on the nature of the fault.

In a three phase system, the phase voltage of phase *A*, *B* and *C* could drop simultaneously and equally. This is regarded as a balanced voltage dip which is a rare case of the voltage dip. More frequently, the unbalanced voltage dip can be caused by unbalanced loads between phases or by a fault on one or two of the three phases.[111,112] The unbalanced voltage will have different amplitudes on each phase or the phase angle between phases are no longer balanced, or both. Conventionally, the positive and negative sequence voltages are the components of particular interests for the VSI controllers as the d.c. side capacitor in many of these applications is a floating capacitor which is not affected by the zero sequence component. Recently, some research studies have addressed the need for controlling the zero sequence from a micro-grid operation point of view.[113-115] However, this control objective is out of the scope of this research.

Before discussing the importance of the fault-ride-through and its related control objectives, the instantaneous power theory [116-119] should be introduced and expanded taking the negative sequence components into consideration. For a three phase system, the instantaneous real and reactive power can be expressed as:

$$P = v_a \cdot i_a + v_b \cdot i_b + v_c \cdot i_c \tag{4.1}$$

$$Q = (v_a - v_b) \cdot i_a + (v_b - v_c) \cdot i_b + (v_c - v_a) \cdot i_c \tag{4.2}$$

where v_a, v_b and v_c are the phase voltages and i_a, i_b and i_c are the currents and, if the system is balanced, can be expressed as:

$$\begin{cases} v_a = V \sin(\omega t + \varphi) \\ v_b = V \sin(\omega t + \varphi - \frac{2\pi}{3}) \\ v_c = V \sin(\omega t + \varphi + \frac{2\pi}{3}) \end{cases} \tag{4.3}$$

$$\begin{cases} i_a = I \sin(\omega t + \phi) \\ i_b = I \sin(\omega t + \phi - \frac{2\pi}{3}) \\ i_c = I \sin(\omega t + \phi + \frac{2\pi}{3}) \end{cases} \tag{4.4}$$

And the real and reactive power (*P* and *Q*) are:

$$P = \frac{3 \cdot V \cdot I \cdot \cos(\varphi - \phi)}{2} \tag{4.5}$$

$$Q = \frac{3 \cdot V \cdot I \cdot \sin(\varphi - \phi)}{2} \tag{4.6}$$

It can be verified that the real and reactive power outputs are constant in the balanced situation. Expanding Equation 4.1 and 4.2 through a power invariant *dq* transformation [120], it is found that the power may be expressed by the *dq* values of the voltage and the current:

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \begin{bmatrix} V_d & V_q \\ V_q & -V_d \end{bmatrix} \begin{bmatrix} I_d \\ I_q \end{bmatrix} \tag{4.7}$$

where:

$$\begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix} = \frac{\sqrt{3}}{2} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2}{3}\pi) & \cos(\theta + \frac{2}{3}\pi) \\ -\sin(\theta) & -\sin(\theta - \frac{2}{3}\pi) & -\sin(\theta + \frac{2}{3}\pi) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad 4.8$$

$$\begin{bmatrix} I_d \\ I_q \\ I_0 \end{bmatrix} = \frac{\sqrt{3}}{2} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2}{3}\pi) & \cos(\theta + \frac{2}{3}\pi) \\ -\sin(\theta) & -\sin(\theta - \frac{2}{3}\pi) & -\sin(\theta + \frac{2}{3}\pi) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad 4.9$$

and θ is the instantaneous angle of the rotating reference frame.

Now considering the unbalanced voltage and current, the instantaneous real and reactive power are still given by Equation 4.1 and 4.2. However the voltage and current are no longer balanced but have a negative sequence component added in shown in Equation 4.10 and 4.11. The zero sequence is ignored due to the reasons discussed previously.

$$\begin{cases} v_a = V^+ \sin(\omega t + \varphi^+) + V^- \sin(-\omega t + \varphi^-) \\ v_b = V^+ \sin(\omega t + \varphi^+ - \frac{2\pi}{3}) + V^- \sin(-\omega t + \varphi^- - \frac{2\pi}{3}) \\ v_c = V^+ \sin(\omega t + \varphi^+ + \frac{2\pi}{3}) + V^- \sin(-\omega t + \varphi^- + \frac{2\pi}{3}) \end{cases} \quad 4.10$$

$$\begin{cases} i_a = I^+ \sin(\omega t + \phi^+) + I^- \sin(-\omega t + \phi^-) \\ i_b = I^+ \sin(\omega t + \phi^+ - \frac{2\pi}{3}) + I^- \sin(-\omega t + \phi^- - \frac{2\pi}{3}) \\ i_c = I^+ \sin(\omega t + \phi^+ + \frac{2\pi}{3}) + I^- \sin(-\omega t + \phi^- + \frac{2\pi}{3}) \end{cases} \quad 4.11$$

The total instantaneous real and reactive power under the unbalanced grid voltage and current in this case may be expressed through four separate terms as shown in Equations 4.12-4.15. Each of these is the product of voltage and current with different combination of the two sequences.

$$\begin{cases} P_0^+ = \dfrac{3 \cdot V^+ \cdot I^+ \cdot \cos(\varphi^+ - \phi^+)}{2} \\ Q_0^+ = \dfrac{3 \cdot V^+ \cdot I^+ \cdot \sin(\varphi^+ - \phi^+)}{2} \end{cases} \quad 4.12$$

$$\begin{cases} P_{2nd}^+ = \dfrac{3 \cdot V^+ \cdot I^- \cdot \cos(2\omega t + \varphi^+ - \phi^-)}{2} \\ Q_{2nd}^+ = \dfrac{3 \cdot V^+ \cdot I^- \cdot \sin(2\omega t + \varphi^+ - \phi^-)}{2} \end{cases} \quad 4.13$$

$$\begin{cases} P_0^- = \dfrac{3 \cdot V^- \cdot I^- \cdot \cos(\varphi^- - \phi^-)}{2} \\ Q_0^- = \dfrac{3 \cdot V^- \cdot I^- \cdot \sin(\varphi^- - \phi^-)}{2} \end{cases} \quad 4.14$$

$$\begin{cases} P_{2nd}^- = \dfrac{3 \cdot V^- \cdot I^+ \cdot \cos(2\omega t + \varphi^- - \phi^+)}{2} \\ Q_{2nd}^- = \dfrac{3 \cdot V^- \cdot I^+ \cdot \sin(2\omega t + \varphi^- - \phi^+)}{2} \end{cases} \quad 4.15$$

$$\begin{cases} P_{total} = \underbrace{P_0^+ + P_0^-}_{\text{Constant}} + \underbrace{P_{2nd}^+ + P_{2nd}^-}_{\text{Oscillating}} \\ Q_{total} = \underbrace{Q_0^+ + Q_0^-}_{\text{Constant}} + \underbrace{Q_{2nd}^+ + Q_{2nd}^-}_{\text{Osillating}} \end{cases} \quad 4.16$$

The instantaneous real and reactive power expressions show that the adding in of the negative sequence components brings an oscillating term into the total power. The magnitude of the power and the power factor can be calculated from the amplitude and phase angle of the symmetrical voltage and current components. These equations can also be expressed in *dq* form through a power invariant *dq* transformation, noting that the *dq* transformation for negative sequence is performed with reference to the frame rotating in the opposite direction to the positive one, shown in Equation 4.17 [31].

$$\begin{bmatrix} P_0 \\ P_{2nd} \\ Q_0 \\ Q_{2nd} \end{bmatrix} = \begin{bmatrix} V_d^+ & V_q^+ & V_d^- & V_q^- \\ V_d^- & V_q^- & V_d^+ & V_q^+ \\ -V_q^+ & V_d^+ & -V_q^- & V_d^- \\ -V_q^- & V_d^- & V_q^+ & -V_d^+ \end{bmatrix} \begin{bmatrix} I_d^+ \\ I_q^+ \\ I_d^- \\ I_q^- \end{bmatrix} \quad 4.17$$

Several problems are considered if the VSI with conventional control system is connected to an unbalanced utility. The associated harmful effects of the unbalanced utility voltage are addressed in a relatively large number of publications [120-124]. Essentially, if the switching of the inverter is controlled to generate only the positive sequence voltage by adjusting the modulation depth taking the possible d.c. bus voltage variation into consideration, the impedance between the negative phase sequence voltage of the grid side and the VSI will be comprised solely of the reactance of the filter [121]. This will cause current of the negative phase sequence to flow into the grid connected inverter. Depending on the level of unbalance and the size of the filter, this current is potentially able to be high enough to cause damage to the power modules. The output voltage of the VSI can be controlled to be unbalanced to avoid this problem.

4.2 Current control objectives of VSI under different constraints

The 2^{nd} order harmonic active power consists of two parts as shown in Equations 4.13 and 4.15. It can be eliminated if the magnitude and phase angle of the positive and negative sequences are adjust properly according to the voltage symmetrical components. It is clear that the d.c. voltage variation rate is proportional to the variation of the output active power. This ensures the d.c. voltage is kept constant under unbalanced grid conditions. In addition to the 2^{nd} order harmonic active power, it is always desirable to achieve unity power factor, which requires the reactive power and 2^{nd} order harmonic reactive power to be zero. [125-128]

In the proposed current control system in this study, the current reference in the *dq* axis reference frame can be obtained, given the desired power and *dq* components of the symmetrical components of the grid voltage. Therefore the current reference is calculated based on the equation below:

$$\begin{bmatrix} I_d^+ \\ I_q^+ \\ I_d^- \\ I_q^- \end{bmatrix} = T_{4\times4} \begin{bmatrix} P_{ref} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{4.18}$$

where:

$$T_{4\times4}^{-1} = \begin{bmatrix} V_d^+ & V_q^+ & V_d^- & V_q^- \\ V_d^- & V_q^- & V_d^+ & V_q^+ \\ -V_q^+ & V_d^+ & -V_q^- & V_d^- \\ -V_q^- & V_d^- & V_q^+ & -V_d^+ \end{bmatrix} \tag{4.19}$$

Also, if the reactive power is required in some specific situation. The reactive power term can be added in to generate the corresponding current reference.

The shortcoming of such a control objective is that the current output of the three phases will be unbalanced which brings unequal current stress among the power modules of different phases. In some cases, depending on the severity of the voltage unbalance, the desired current output for a specific phase could exceed its safety limit. To avoid damaging the power module while keeping the original control objective, the current references of the three phases should be limited simultaneously. Therefore, the output power is limited. This requires two additional aspects to be taken into consideration if the balanced power strategy is used. Firstly, the VSI should have an additional way to restrict the power flowing into the d.c. bus. Otherwise the system would eventually fail due to the VSI not being able to dissipate the incoming power. Secondly, an additional algorithm is needed to find out if any of the phase current references exceed the limits, this will however, introduce some additional computational burden.

The current can also be controlled for injecting the fundamental positive sequence current only [127]. Thus the problem of unevenly stressed power modules can be avoided. However, the negative phase sequence voltage will cause unbalanced three phase power. The active power

oscillation will appear if only the current of the positive sequence is injected, verified by Equation 4.15. In this case the grid voltage and the current injected are expressed as:

$$\begin{cases} v_a = V^+ \sin(\omega t + \varphi^+) + V^- \sin(-\omega t + \varphi^-) \\ v_b = V^+ \sin(\omega t + \varphi^+ - \frac{2\pi}{3}) + V^- \sin(-\omega t + \varphi^- - \frac{2\pi}{3}) \\ v_c = V^+ \sin(\omega t + \varphi^+ + \frac{2\pi}{3}) + V^- \sin(-\omega t + \varphi^- + \frac{2\pi}{3}) \end{cases} \quad 4.20$$

$$\begin{cases} i_a = I \sin(\omega t + \phi) \\ i_b = I \sin(\omega t + \phi - \frac{2\pi}{3}) \\ i_c = I \sin(\omega t + \phi + \frac{2\pi}{3}) \end{cases} \quad 4.21$$

The power output in this case will be:

$$\begin{aligned} P_{total} &= \frac{3 \cdot V^+ \cdot I \cdot \cos(\varphi^+ - \phi)}{2} + \frac{3 \cdot V^- \cdot I \cdot \cos(2\omega t + \varphi^- - \phi)}{2} \\ Q_{total} &= \underbrace{\frac{3 \cdot V^+ \cdot I \cdot \sin(\varphi^+ - \phi)}{2}}_{\text{Constant}} + \underbrace{\frac{3 \cdot V^- \cdot I \cdot \sin(2\omega t + \varphi^- - \phi)}{2}}_{\text{Osillating}} \end{aligned} \quad 4.22$$

It can be verified that, as with the balanced case, the positive sequence voltage and the current will generate a constant power output. However, the negative sequence voltage and the current which is of positive phase sequence will generate an oscillating power whose frequency is two times of the fundamental frequency. The active power which determines the amount of energy exchange is of particular interest in this problem as the d.c. link voltage is directly linked to the energy exchange between the d.c. side and the a.c. side of the VSI. The oscillating real power due to the negative phase sequence voltage will cause the d.c. bus capacitor to be charged and discharged periodically. As a result, the d.c. bus voltage fluctuates.

The d.c. bus capacitor usually consume a significant amount of space in the inverter module design. A higher utilisation rate of the d.c. bus capacitor is desired for reducing the size of the equipment. But from the control point of view, the fully utilized d.c. bus capacitor, which is

designed to absorb the high frequency switching harmonics during balanced operation, left very limited margin for it against voltage variation especially the voltage rise. Generally, the d.c. bus voltage should be controlled within a safe range of 110% of its voltage rating. The current and d.c. bus voltage control should be swift enough to regulate variation of the d.c. bus voltage. The d.c. bus voltage oscillation can also be harmful mainly for three other reasons. Firstly, the oscillating d.c. voltage could results in harmonic injection in the current output if the d.c. bus voltage is not properly sampled [129]. Secondly, the renewable power such as PV generation system will be heavily affected by the oscillation of the d.c. voltage, additional control effort should be made to keep the generation connected [130, 131]. Thirdly, with many maximum power point tracking algorithms at the front end, especially for small scale wind turbines comprising a permanent magnet generator and a passive rectifier, the d.c. side voltage plays a vital row. The oscillating d.c. voltage certainly brought in undesirable effects [132].

In Figure 4.1, an unbalanced voltage is shown. The phase B voltage is at 50% of its normal value. Using Equation 4.18, the current reference generated to output balanced power is shown in Figure 4.2 (a). Figure 4.2 (b) shows the references for the balanced three phase current. If the current outputs are correctly tracking these current references, the power outputs for the two control objectives are compared, as shown in Figure 4.3

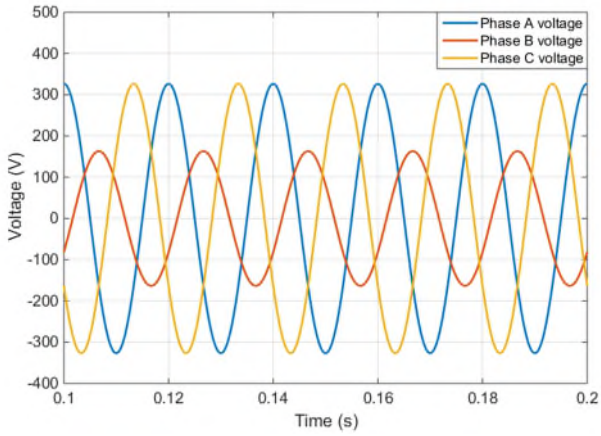
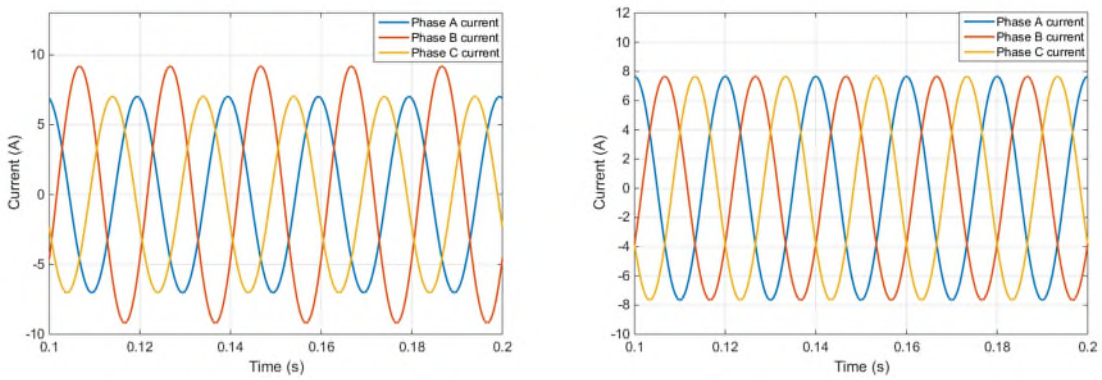


Figure 4.1 Unbalanced three phase voltage



(a) (b)

Figure 4.2 Current waveform of (a) balanced power, (b) balanced current

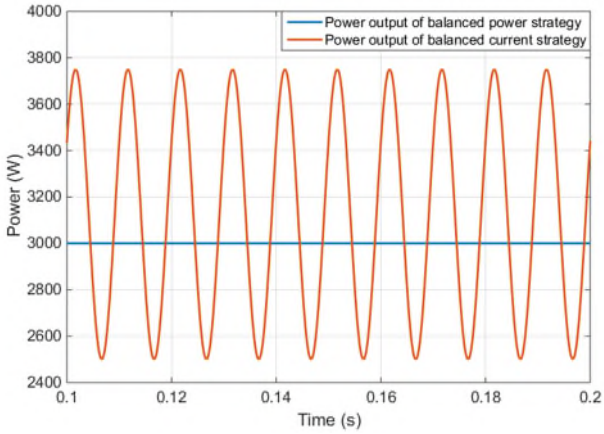


Figure 4.3 Comparison of power output of different current control strategies

Based on the discussion above, the control objective for unbalanced fault-ride should be different to satisfy different requirements according to the specific circumstance. The output current can be controlled to be balanced if the negative phase sequence voltage is not to be compensated. The balanced current output as one of the current control strategy, has the advantage of high utilisation of the inverter current rating. It is also considered a simpler solution for riding-through the unbalanced grid fault compared to the current control strategy aiming at balanced power output because: firstly, the current reference of the negative sequence doesn't need to be adjusted through on-line calculation but pre-set to be zero; secondly, the

power output doesn't need to be regulated to avoid over-current as in the second control strategy. However, the d.c. bus voltage will oscillate in the balanced current output strategy. In case of high d.c. capacitor utilisation, the constant power strategy will be beneficiary.

4.3 Voltage oriented current control and comparison

Voltage oriented current control is adopted in most of the conventional current controllers. The PLL system plays a vital role in aligning the d-axis of *dq* reference frame with the voltage vector which is the global reference for the whole system.

In this control method, the grid voltage consists of the d-axis component which will have a positive value, whilst the *q*-axis component is zero. According to Equation 4.18 the real power output is proportional to output i_d while the reactive power can be controlled by adjusting i_q. For unit power factor, which is most popular among the control objectives, the value of i_q will be zero. This characteristic has the advantage of reducing the size of the matrix for calculating current references according to desired power output.

The use of the a.c. side voltage sensors and the PLL system tuned with high bandwidth offered good performance for tracking the voltage variation especially if the grid side is considered stiff enough. However, in a weak grid where the voltage measured at the point of common coupling (PCC) is able to be affected by the VSI output. The delay introduced by the PLL could reduce the performance during the transient stage. If a symmetrical component decomposition mechanism is adopted for riding-through the unbalanced fault, additional delay will be added to the original delay of signal feed-forward, resulting in further degraded transient performance. The PLL and current control system should be carefully tuned considering this kind of situation.

The active and reactive power control can also be achieved without using the PLL system. However the matrix for calculating the current reference is larger than when the *dq* reference frame is synchronised to the grid voltage vector. In this case the frequency of the grid voltage becomes very important reference to the system as will be discussed in Section 4.5. Considering the case for riding-through the unbalanced grid fault, the complex calculation is not a drawback but becomes necessary. Usually the voltage oriented current control only adopts one PLL system which is going to lock the phase angle to the voltage vector of the positive sequence. The reference frame of the negative sequence is defined by the output of the PLL multiplied by -1, as the unbalanced grid faults have different forms.

It can be concluded that the grid frequency is a more important reference to the system compared to the phase angle. The phase angle may be calculated from the *dq* components without adopting the PLL system. It is an advantage as sometimes, the PLL system introduces some tricky transient if the input variation is large. If the grid frequency is assumed to be varying in a limited range and comparatively slow compared to the fundamental period (which is likely the case), then the PLL system is only needed for frequency tracking and the bandwidth is not necessarily high which avoids the transient problem.

4.4 Weak grid characteristic

Grid impedance of a strong grid is usually around 10% of a necessary coupling impedance and 20% if the grid is weak. In this research, the proposed grid connected inverter system can be used in many different applications. The grid which the inverter under control will be connected to is assume to be weak, where changes of the grid voltage can happen frequently due to various resources e.g. change of load and newly connected generations. Analysis will be carried out

using the character of a weak grid to investigate the current control behaviour affected by the grid impedance. This will be discussed in Chapter 5.

4.5 Sensor reduction and sensor-less control

An analysis in [53] shows that in the offshore wind farm, the failure rate of the sensors involved in the control system is around 5% which is considered to be significant. Although in this research, the model is developed based on small scale generation, the general idea can be expended to be used in the current control system of different scale of generators. For a system configured to rely on sensors will naturally be disabled for lack of control feedback if the sensors malfunction. Therefore, the need for developing techniques to reduce the dependence on sensors is rising. The conventional idea aims at reducing the number of the sensors used. For a three-phase three-wire system, the sum of line to line voltages is zero, so is the sum of the currents. Therefore, with two measurements for the voltages and currents respectively, the third one is easily determined. However, this approach still requires four sensors on the a.c. side in total. Further, this method is not expandable to three-phase four-wire systems as the neutral current will cause the sum of the three phase currents to be non-zero.

As for the current control system of the VSI, as well as of many other pieces of equipment, the current sensor is necessary for system protection. The further reduction of the number of sensors can be achieved by reducing the number of voltage sensors used. The voltage-sensor-less control of a VSI is reported in[54-57, 80, 133]. In [55], the conventional SRF-PLL is used to lock the angle of the reference frame to the reference angle generated based on the line impedance and the desired current output using an offline method. The desired active power is controlled based on balancing the incoming and outgoing d.c. power which is achieved by measuring the d.c. side voltage. This allows the VSI to be controlled without a.c. side voltage

sensors but it is not a flexible and accurate method for controlling the power factor. If the nominal grid voltage is not achieved, the *dq* reference frame will not be correctly aligned with the voltage vector of the grid voltage, not to say the capability of riding through the unbalanced grid fault. In [133], the grid synchronisation can be achieved simultaneously with the power control by emulating the behaviour of a synchronous generator. However, the initial synchronisation to the grid still requires the a.c. voltage sensors and the related PLL system. In [54], a low computational burden grid voltage estimation method with fast dynamic response is reported. This method improves the dynamic response of the voltage-sensor-less current control but the capability of riding through the unbalanced grid fault is not discussed. In [80], the current sensor-less control is expanded and capable of riding-through the unbalanced grid fault. The current controller is a proportional-resonance based controller. However, the virtual-flux based grid voltage estimation and controller are believed to have a slower dynamic response in [57]. Other researches based on different control model also proved that a grid connected inverter system is able to be controlled without the a.c. voltage sensors based on the small signal models. However none of them has mentioned how to acquire the initial synchronisation and what the system response will be in case of the large system variation. The reliable start-up method for solving this problem will be developed in this study. Among these reported methods, none has achieved voltage-sensor-less current control during an unbalanced grid conditions based on an SRF-PI based current controller. However, the a.c. voltage-sensor-less current control based on SRF-PI based current control is potentially beneficial on the other hand. Because many conventional control systems use SRF-PI based current control, the technique is believed to be mature and the coding for the hardware is easily available. A voltage-sensor-less current control method based on the SRF-PI based current controller, such as the proposed method detailed in the next chapter, will facilitate the application of the proposed control method as well as provide an easy upgrading to the existing systems.

4.6 Chapter summary

The grid connected VSI needs to deal with various grid voltage variations. The controller should be adaptive to the grid voltage variations possible to happen with the ability to achieve different control objectives to satisfy different requirements. In Section 4.1, the possible scenarios of the grid variation are illustrated. The consequence of such grid variations are illustrated in Section 4.2. The power control objectives need to be adjusted for different purposes. Through instantaneous real and reactive power theory, the current required for generating a certain power can be calculated. This provides essential control inputs to the control system as the proper current references. The SRF-PI based current control relies on the *dq* transformation to convert the coordinate frame from natural to synchronous. This requires the proper phase-locking or frequency-locking mechanism to be adopted. The voltage oriented current control using PLL is compared with SRF-PI based current control and is shown to be able to track the grid frequency in Section 4.3. The tricky transient response of SRF-PLL is a draw-back thus the second method is more preferred in this study. The benefits for deploying a.c. voltage-sensor-less current control is discussed in Section 4.5. To design such a system is the main challenge of this study. The a.c. voltage-sensor-less current control will be designed, then tested under different types of grid faults illustrated in this chapter to verify the suitability of the proposed techniques in applications.

Chapter 5 Control System Design

5.1 Introduction

The vital information for grid synchronisation is usually obtained from the voltage measured by the a.c. voltage sensors. Conventional voltage oriented current control requires the measured voltage signals to be further processed by a PLL stage to calculate the magnitude and the phase angle of the grid voltage, which are used in later current control stage. In the SRF-PI based current control systems, the measured current signals need to be transferred to the direct and quadrature axis values according to the synchronous reference frame defined by phase angle of the grid voltage detected. In this control scheme, accurate tracking of the phase angle of the grid voltage plays a vital role to keep the system operate correctly. The a.c. voltage sensors are highly important in order to ensure that such requirement is full-filled. However, the importance of the voltage sensors in turn, makes the system vulnerable to the voltage sensor failure.

This research proposes an a.c. voltage-sensor-less current control method to overcome this shortage. It utilises a grid voltage observer to replace the voltage sensors. The current control function of the proposed system is carried out by an SRF-PI based *dq*-decoupled current control. The required information of the grid voltage is obtained from the output of the grid voltage observer. As discussed previously in Section 4.5, the initial grid synchronisation is obtained from an additional start-up process which utilised the advantage of the current hysteresis control in order to avoid large current transient might happen. In this chapter, the proposed a.c. voltage-sensor-less current control method will be detailed and analysed.

5.2 Current controller

The a.c. voltage-sensor-less control was reported as a direct power control method described in [134]. The feedback signals in a current control method, which are usually the instantaneous current values (or i_α and i_β or i_d and i_q in corresponding reference frames), are replaced by the real and reactive power. This gives the name of direct power control. As the measurement of the utility voltage is eliminated from the control scheme, the output power cannot be calculated as introduced in Section 4.1. The main feature of direct power control is utilizing the virtual flux estimated from the measured current and the switching duty of the power modules to generate a power estimation. The current is then controlled by the switching duty generated by a look-up table where the input variables are the error between the estimated real or reactive power and their references respectively which are decided by the d.c. voltage as well as the control objective of the power factor. This control method has improved the control system by allowing a lower sample rate and a reduced filter size of requirement. Also, due to the swiftness of the current control associated with the hysteresis control, the transient response is improved. However, the well-known side effect of non-constant switching frequency associated with the hysteresis control results in the unpredictable harmonic injection which could actually deteriorate the overall performance of the system. Further, the operation during the unbalanced grid fault are not taken into consideration which could potentially limit the availability of this technique. Finally, the start-up of such a system is not made clear as for the operation of the system, power must be acquired and estimated based on output which is not available before system is activated.

Another reported approach for ride-through the unbalanced grid faults is the virtual-flux based current control. It has advantage for utilizing the mutual relationship between the current and flux in the inductive filter which is useful for calculating the power.

Based on the review of the previous control methods, the following aspects are considered as improvable:

- The need of the a.c. voltage sensors;
- The harmonic injection associated with methods using non-linear current control;
- The limited transient response associated with the linear current control method;
- The lack of the proper initial synchronisation for a.c. voltage-sensor-less control.

To improve the a.c. voltage-sensor-less control in terms of the harmonic performance as compared to the direct power control method, the PWM switching scheme and a linear current control system are used to replace the non-linear current control. The slower response associated with the linear current control method will be improved by adopting a higher performance symmetrical component decomposition system which has a dominant effect on the overall performance of the control system as discussed in Section 5.1.2.

5.2.1 SRF-PI based dq decoupled current control

A grid connected VSI is usually coupled with an inductive filter for filtering the high order harmonics caused by switching. The impedance of the filter is considered much greater than the grid impedance in many cases. The control parameters are designed regarding the performance of the VSI with specified filter parameters. Figure 5.1 shows the overall system diagram.

The voltage source inverter is modelled as a two-level inverter and the d.c. neutral is floating. The switching harmonics are filtered by an L type filter which denotes first order characteristic. This is an appropriate approximation from a control design point of view although in reality an

LCL filter could be used [84, 135, 136]. The local loads are connected to the PCC. The parameters of the filter and local loads on each phase are assumed well balanced.

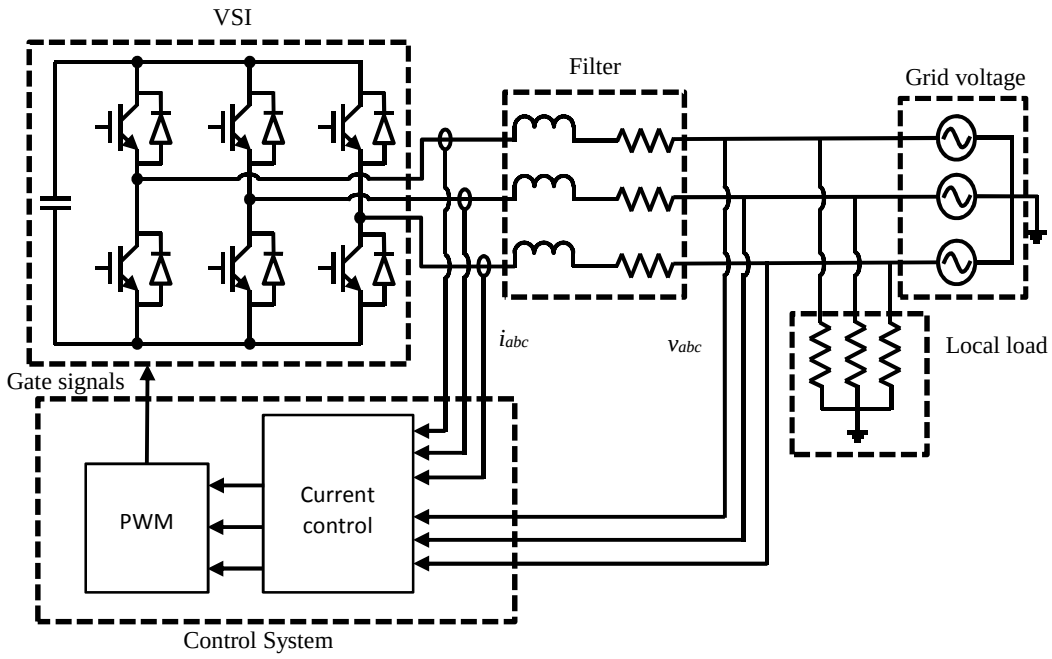


Figure 5.1. Three phase VSI under study

For the dynamics between the input voltage and the output current based on a simple RL filter, the voltage applied at the inverter terminal is modelled as its fundamental frequency component assuming that the switching harmonics can be well filtered out. The current output for each phase is the voltage drop across the filtering inductor divided by the reactance of the filter, neglecting the grid impedance.

$$\begin{cases} L\dfrac{d}{dt}i_a(t) = v_{oa}(t) - v_{ga}(t) - R\cdot i_a(t) \\ L\dfrac{d}{dt}i_b(t) = v_{ob}(t) - v_{gb}(t) - R\cdot i_b(t) \\ L\dfrac{d}{dt}i_c(t) = v_{oc}(t) - v_{gc}(t) - R\cdot i_c(t) \end{cases} \quad 5.1$$

where the v_o denotes the output voltage at the inverter terminal and v_g denotes the voltage at the receiving end grid, i_{abc} are the phase currents.

By applying *dq* transformation, equation 5.1 became:

$$\begin{cases} L\dfrac{d}{dt}i_d(t) = v_{od}(t) - v_{gd}(t) - R\cdot i_d(t) + \omega\cdot L\cdot i_q(t) \\ L\dfrac{d}{dt}i_q(t) = v_{oq}(t) - v_{gq}(t) - R\cdot i_q(t) - \omega\cdot L\cdot i_d(t) \end{cases} \qquad 5.2$$

where ω is the frequency of the a.c. side grid in rad/s.

When the grid voltage and the filtering inductor are assumed well balanced, the dynamics of the grid-side in the *dq* reference frame can be further transformed into frequency domain through Laplace transform. The *dq* frame based a.c. side dynamic model of the inverter has cross-coupling terms between the two axes. The output voltage V_d will have its effect on the I_q injected and vice versa. Based on this understanding, the block diagram representing the inverter grid side dynamics can be drawn as shown in Figure 5.2.

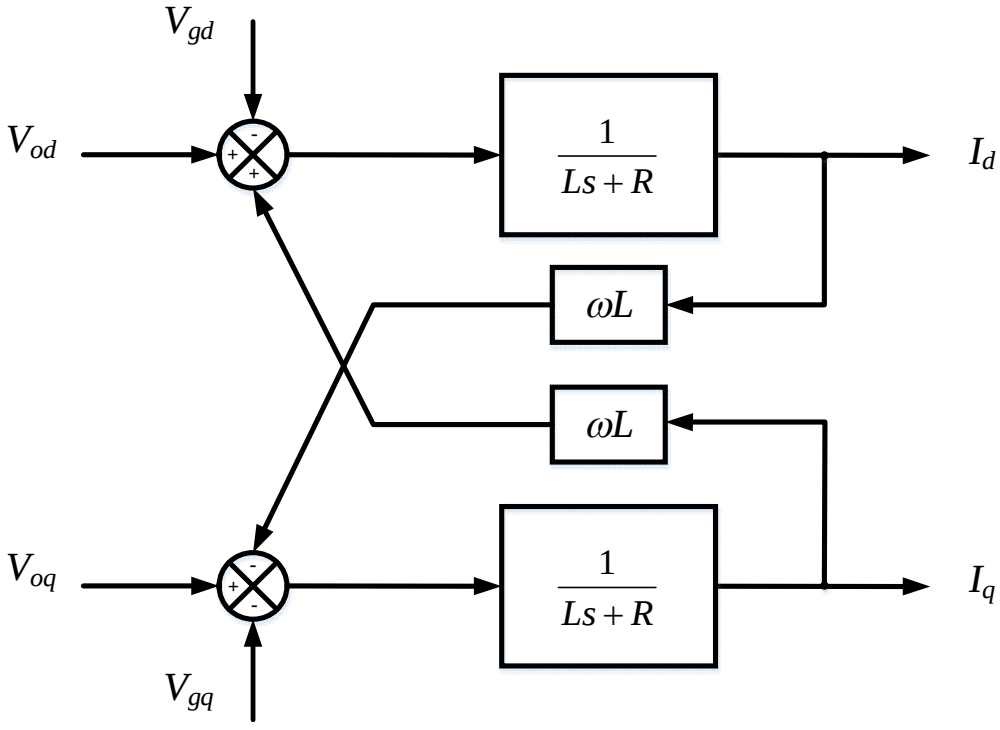


Figure 5.2. Equivalent model of filtering inductor on *dq* reference frame

With balanced grid side voltage and reactance, the current injected into the grid can be controlled to be balanced and sinusoidal as well. The I_d and I_q of the balanced three phase currents obtained through *abc-dq* transformation will be constant values as discussed in the previous sections. The relevant current control can be done using a PI controller. The primary SRF-PI based current control structure is shown below in Figure 5.3.

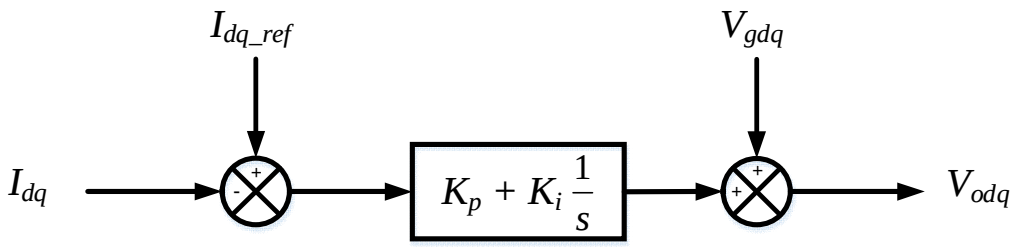


Figure 5.3 Primary SRF-PI based current control

The current control using PI regulator is a working plan for the current control however it may not be sufficiently good in terms of transient response. The output voltage reference of the current controller is zero when the current injected is zero and the grid side voltage is unknown, referred to as the zero state of the controller. The instantaneous voltage drop across the filtering inductor is considerably high at the time point zero and a short while after, which causes undesirable high current flowing through the power modules. Also, the cross coupling terms of *dq* component on the a.c. side will cause interference between the control efforts on the two axes, causing a prolonged the transient process.

The primary SRF-PI based current control can be improved by adding a voltage feed-forward term of the grid side voltage to the output of the controller, as shown in Figure 5.4. By doing this, the output voltage reference at the time point zero will be the grid voltage and the voltage drop across the filtering inductor will be zero. The control effort will be trying to increase the current injected towards its reference value during the transient stage which ensures the safety

of the power modules. Another improvement is to add a decoupling loop to decouple the interaction of the control effect on the two axes to shorten the duration of transient.

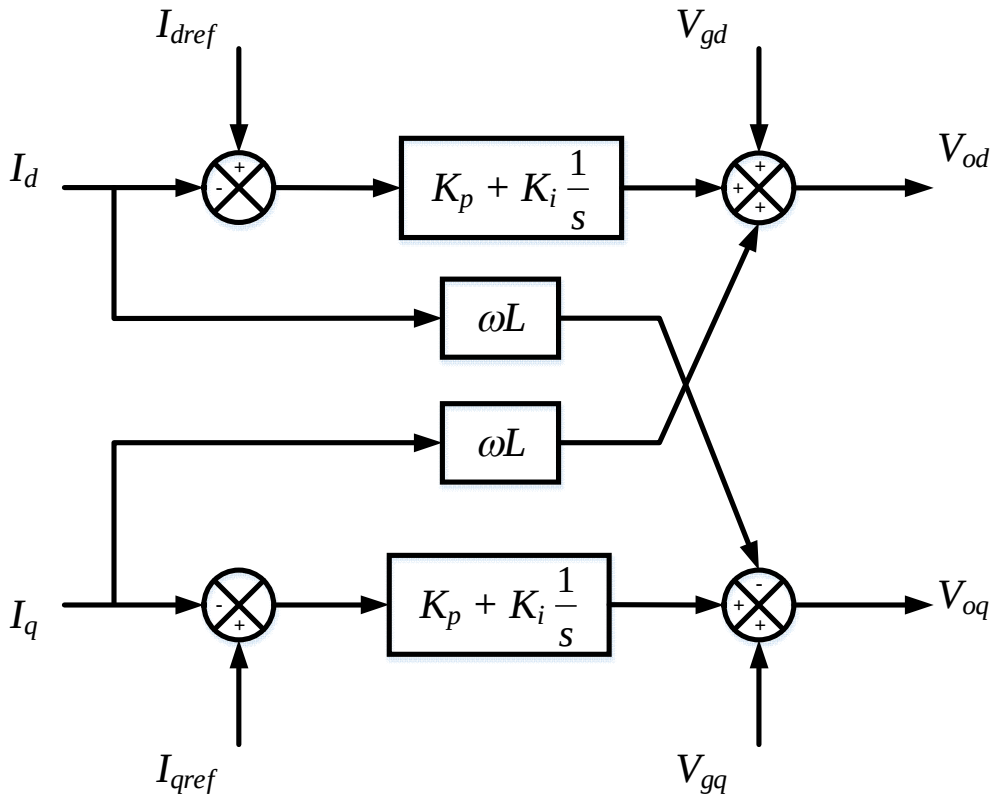


Figure 5.4 SRF-PI based *dq*-decoupled current control.

The a.c. grid side and controller side of the inverter together defines the scope of the whole grid connected inverter system, as shown in Figure 5.5. The output of the current controller is the voltage reference which will be feed into the PWM signal generator. The action of the power electronic switches will be controlled accordingly. The PWM signal aims at producing an average voltage in a switching cycle equal to the reference voltage. This process introduces delay of half of the switching period. However, the switching frequency as in the low power applications is usually significantly higher than the fundamental grid frequency. This delay can be effectively neglected. Therefore, there is no need of further compensation, such as for the

voltage drop of the semiconductors and also the resistance of the power electronic switches. The PWM process can be viewed as a unity gain and neglected in the system diagram.

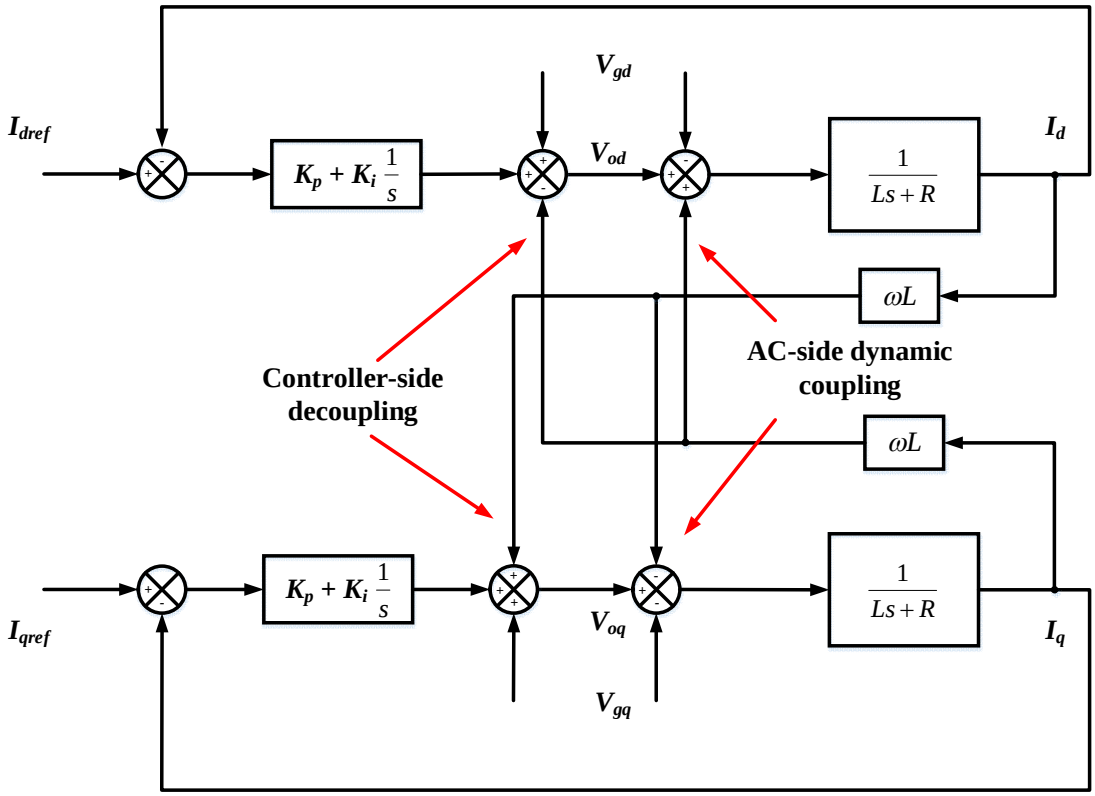


Figure 5.5. Block diagram of VSI control system and the grid side

In a conventional current control system, the voltage of the grid is measured using voltage sensors. The dynamic change of the grid side voltage is cancelled out by the grid voltage feed-forward in the controller. The variation of the grid voltage will only affect the current control by changing the current reference to maintain the power reference. Then the system responding to a balanced grid voltage dip can be predicted by the step response of the system to the input current change as shown in Figure 5.6. It is clear from Figure 5.5 that the decoupling network of the *dq* axes on the controller side removes the interaction of the *dq* signals. The voltage command signals of V_d and V_q are then only subjected to the current of their own axes. Therefore the system can be analysed based on the two parallel loop of the same structure and parameters separately [137, 138], shown in Figure 5.6.

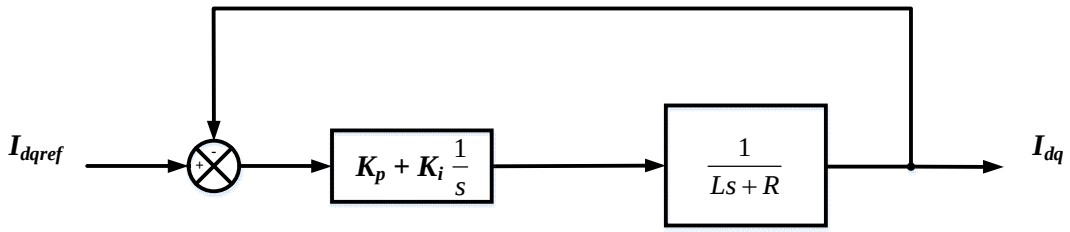


Figure 5.6. Simplified block diagram of the system under study

The step change of the system input which is the current reference could be caused in two ways. First, the change of the grid voltage will not have impact on the system output as a disturbance as mentioned above. But for the power control purpose, the current reference is adjusted according to the grid voltage. Therefore, the grid voltage step change is one of the reasons causing the input to change. The second cause of the input change comes from the varying power flow into the d.c. bus changes. The d.c. bus will be charged up if the output real power is less than the power input, and discharged vice versa. To protect the d.c. bus capacitor, the reference of the power output is directly linked to the voltage drop between the d.c. terminals, which also determines the current reference.

Since the PI control gains are set the same on the two control loops (*d* and *q* axes), the system can be considered as a single-input single-output system as the two loops are of the same dynamic characteristics. The system response on both axes can be expressed using the transfer functions below.

Open-loop transfer function:

$$H(s) = \frac{\frac{K_p}{L}s + \frac{K_i}{L}}{s^2 + \frac{R}{L}s} \qquad 5.3$$

Closed-loop transfer function:

$$G(s) = \frac{H(s)}{1 + H(s)} = \frac{\frac{K_p}{L}s + \frac{K_i}{L}}{s^2 + \frac{R + K_p}{L}s + \frac{K_i}{L}} \quad 5.4$$

Error transfer function:

$$E(s) = 1 - G(s) = \frac{s^2 + \frac{R}{L}s}{s^2 + \frac{R + K_p}{L}s + \frac{K_i}{L}} \quad 5.5$$

The transfer function verifies that the grid connected inverter under SRF-PI based *dq*-decoupled current control is a second order system and the system performance can be easily defined. The un-damped natural frequency is:

$$\omega_n = \sqrt{\frac{K_i}{L}} \quad 5.6$$

And the damping ratio is given by:

$$\xi = \frac{(R + K_p)}{2 \cdot \sqrt{L \cdot K_i}} \quad 5.7$$

As mentioned in many literatures that the damping ration should be set around half of square root two (0.707). The series resistance and the inductance are constant defined by the harmonic rejection requirement and the actual equipment. Thus the damping ration of the system is defined by the mathematical relation between the proportional and integral gains. The integral gain is selected for adjusting the rise time of the system. A simulation study has been carried out to verify the design of the current controller guided by the analysis above.

As the size of the filter is defined by the requirement of the harmonic rejection, the parameters of the RL filter are independent of the design of the control system. For a VSI system on a 400V grid, the inductance is selected to be 6mH which meets the requirement for switching

harmonic attenuation, and by using measured series resistance of a practical iron-cored inductor, the series resistance is 0.08Ω. The step response of the system under different control parameter designs based on the mathematic model are plotted in Figure 5.7. A simulation model taking the actual VSI module into consideration is built with the same RL filter to verify the current response. For the current reference stepping up, the grid voltage is going to drop.

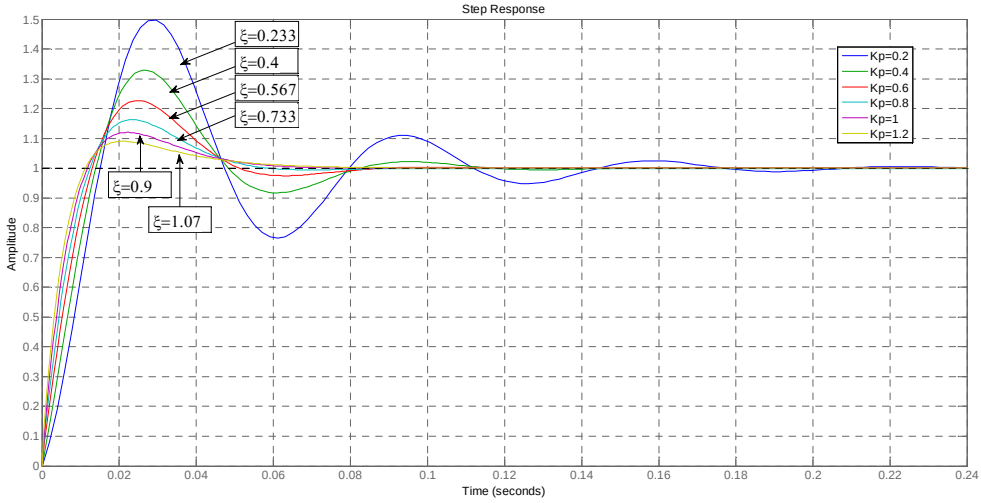


Figure 5.7 Unit step response of the *dq*-decoupled current control

The diagram shows the unit step response of the system under setting of *Ki* to be 60. The damping ratio of the system increases with the increasing *Kp*. The optimised response is reached around *Kp*= 0.8.

It has been made clear that by the analysis given above, it is important to apply *dq* decoupling as well as grid voltage feed-forward in the control loop in order to achieve better system response. The tuning of the controller is an important step towards the system design which should be guided by the parameter of the filter. Noting that assumptions are made for isolating the problem under investigation from other factors could cause disturbances to obtain the conclusion above. They are summarised as follows.

- The grid voltage is measured and the sampling of the voltage is ideal;

- The current sampling is ideal where no delay is introduced;
- The grid voltage is well balanced;
- The parameters of the filtering inductor are well balanced and acquired accurately;
- The grid frequency is at its nominal value;
- The grid impedance is insignificant and can be neglected;
- The PWM process delay is neglected.

The analysis above was made based on an elementary grid model, which has the frequency variation and the grid impedance neglected. In reality, the grid variation is a common phenomenon and the level of deviation varies in different systems. In general, the mains network is a relatively stiff system where frequency deviation is limited in a very small range for its importance of such a system while a micro-grid system can be a harsher environment where frequency deviation could happen more frequently with higher level, affected by the dynamic change of the load. Also, the mains system has a small grid impedance compared to the filtering inductor while the grid impedance is not negligible in some weaker distribution networks. Therefore, the VSI and its control system performance should be analysed taken the frequency deviation and grid impedance into consideration.

5.2.2 Effect of symmetrical component decomposition of the current signals to the current control

Based on the discussion in Chapter 3, several symmetrical components decomposition algorithms capable of working under unbalanced utility voltage are potentially feasible for the applications of the voltage-sensor-less VSI systems dealing with unbalanced system conditions. However, the different performances of these algorithms will affect the selection of the system band-width as will be discussed in this section.

Conventional current control system equipped with a.c. side voltage sensors is usually to apply the symmetrical components decomposition algorithm to both the measured voltage and the current. The selection of the symmetrical decomposition and the corresponding PLL system is a crucial step in the control system design for achieving high dynamic performance. A slow PLL for processing the voltage signals would results in a reduced dynamic response for the power control as the current reference is generated based on the voltage symmetrical components while the bandwidth of the current controller would be heavily affected by the symmetrical decomposition of the current measurement. For the ac-side voltage-sensor-less control proposed in this research, the grid voltage of a specific phase sequence is estimated based on the voltage output of the VSI and the current of the same phase sequence. Therefore the symmetrical component decomposition for voltage is not needed. The analysis will focus on the delay effect of the feed-back current on the system performance.

The symmetrical components decomposition algorithm can be simplified as a delay when analysing its interference to the system. By analysis of the system response under different input delays, the PLL interference can be predicted from its time constant. A simulation study is carried out to investigate the performance of a current control system against the current measurement input delay, as shown in Figure 5.8. The current system under examine is a *dq*-decoupled current control in which the utility voltage is measured. To isolate the problem, the PLL for voltage measurement is assumed ideal. The switching of the inverter power modules is also ignored.

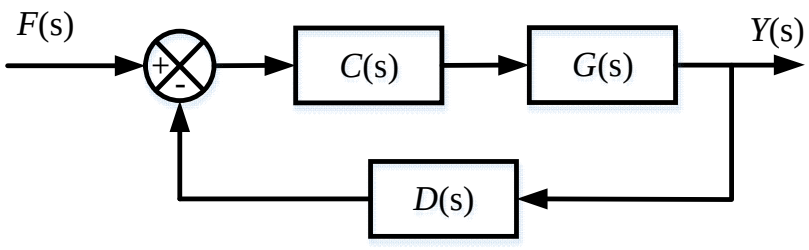


Figure 5.8 Block diagram of the current control system with feed-back delay

The following diagram, Figure 5.9, is the step response of a current control system. The control parameters *Kp* and *Ki* as well as the coupling impedance are set the same in different tests which has different time constant of *D(s)* shown in the figure above. The delay stage *D(s)* is used to represent the delay introduced by symmetrical components decomposition which is modelled as a first-order low-pass delay in this test. It can be verified from Figure 5.9 that the system damping reduces with the increasing time constant of the *D(s)*. Table 5.1 shows the parameters of the filter and control coefficients. The parameters of the a.c. side including the inductance of an L type filter and the grid is the typical value is taken from the measurement of such parameters of the experimental test rig and will be used in the other analysis in this chapter as well as simulations. Some of these parameters are going to be made different artificially in order to demonstrate a particular circumstance in some of the analysis.

Filter parameters	Control parameters
R_f = 100mΩ	K_p=0.8
L_f =10mH	K_i=60
R_g=5mΩ	
L_g=1mH	

Table 5.1 Parameters of the system under study

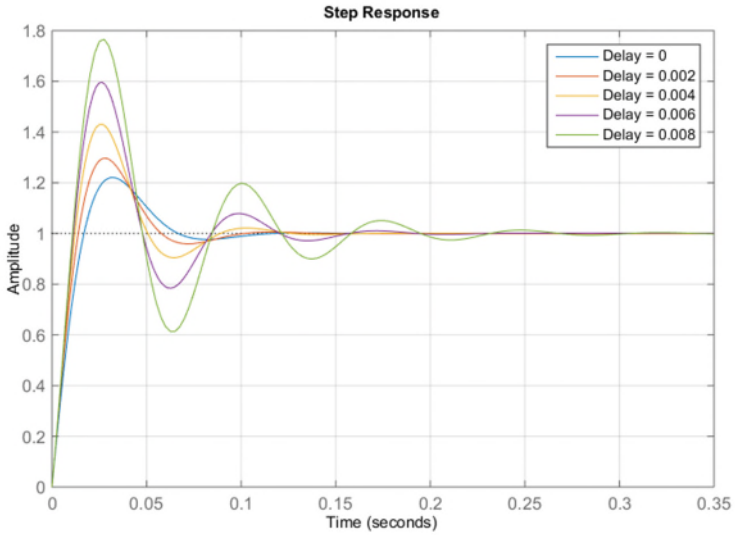


Figure 5.9. Unit step response of the system under different feedback delay

From the simulation study, it is clear that by adding delay to the feed-back, which is the symmetrical components decomposition in this research, the system damping is reduced and settling time increased. It can be concluded that when the system damping further reduces by increasing the input delay, the system will finally get into an unstable state. To compensate the oscillation brought about by higher delay, the control system band-width should be reduced so that the control can be kept stable.

This is exactly the same case for voltage-sensor-less control and the system discussed above regarding to the input delay problem as the symmetrical components decomposition algorithm is applied to the current measurement.

5.2.3 Performance of SRF-PI based dq-decoupled current control under variation of grid impedance

The analysis above provides a typical tuning procedure of the SRF-PI based *dq*-decoupled current control. However, the grid impedance is neglected in the analysis in the last section.

The effect of the grid impedance on the stability of the inverter control system is significant if it is not negligible compared to that of the filter. The analysis in this section will investigate the how the grid inductance affects the behaviour of the system. The grid impedance is modelled as a Thevenin series RL connected between the filtering inductor and the original a.c. voltage source. As shown in the analysis above, if the impedance of the grid is not negligible compared to that of the filter, the equivalent series resistance and inductance will change which in turn changes the behaviour of the system. As mentioned above, in the system model shown as the transfer function of a second order system it is assumed that the inductance L in the decoupling term is accurate when the grid impedance is negligible, so that the a.c. side dynamic coupling between dq axes is decoupled by the decoupling terms. Under the situation that the inductance L in the decoupling calculation is not accurate when taking the grid impedance into consideration, the transfer function is no longer valid. The error between the actual coupling and the decoupling will transform the system analysed above into a multi-input and multi-output (mimo) system, as shown in Figure 5.10. It will be hard to identify the transfer function of a mimo system. Such a system should be analysed using state space method.

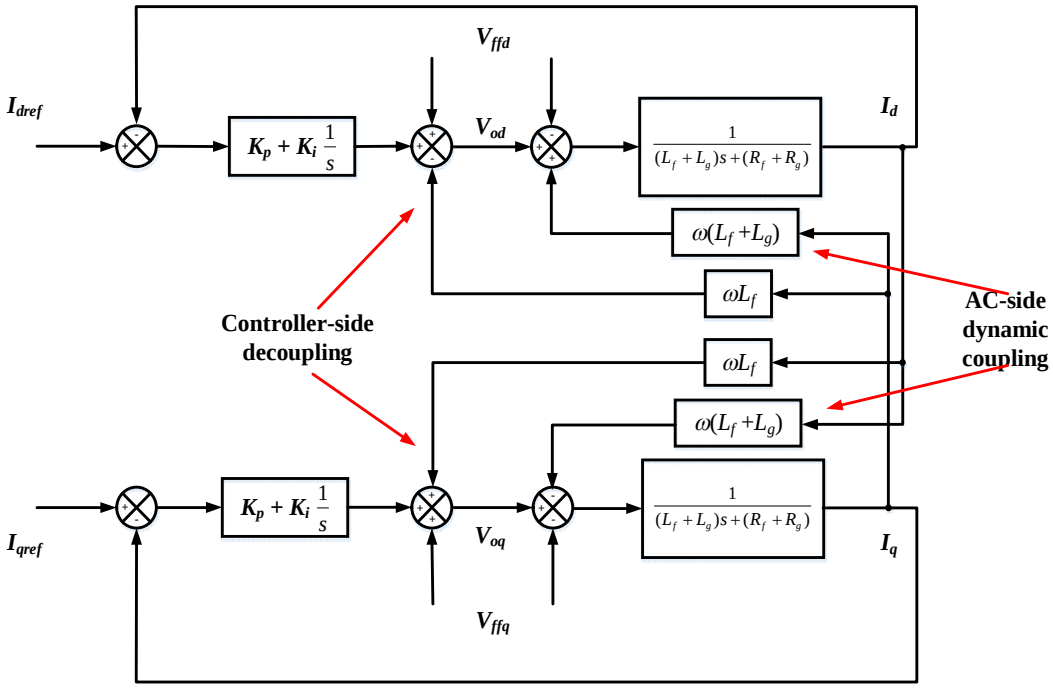


Figure 5.10 System under inaccurate *dq* decoupling

Starting from the a.c. side of the VSI, the inductance of each phase becomes the sum of the inductance of the filter and the inductance of the grid. Therefore the dynamic coupling coefficient of a three-phase system becomes the grid frequency ω multiplied by the total inductance of the system $L_f + L_g$ which is expressed as L_t in Figure 5.10. Also, the line resistance changes as well. The dynamics of the a.c. side can be expressed as follows.

$$\begin{bmatrix} v_{gp}(t) \\ v_{gp}(t) \end{bmatrix} = \begin{bmatrix} v_{od}(t) \\ v_{oq}(t) \end{bmatrix} + \begin{bmatrix} -(R_f + R_g) & \omega(L_f + L_g) \\ -\omega(L_f + L_g) & -(R_f + R_g) \end{bmatrix} \begin{bmatrix} i_d(t) \\ i_q(t) \end{bmatrix} + (L_f + L_g)\frac{d}{dt}\begin{bmatrix} i_d(t) \\ i_q(t) \end{bmatrix} \qquad 5.8$$

Rearranging the equation above gives:

$$\begin{bmatrix} v_{od}(t) \\ v_{oq}(t) \end{bmatrix} - \begin{bmatrix} v_{gd}(t) \\ v_{gq}(t) \end{bmatrix} = \begin{bmatrix} (R_f + R_g) & -\omega(L_f + L_g) \\ \omega(L_f + L_g) & (R_f + R_g) \end{bmatrix} \begin{bmatrix} i_d(t) \\ i_q(t) \end{bmatrix} - (L_f + L_g)\frac{d}{dt}\begin{bmatrix} i_d(t) \\ i_q(t) \end{bmatrix} \qquad 5.9$$

The output of the current controller is the sum of the output of PI regulator, the decoupling term and the voltage feed-forward term. Assuming there is no delay introduced to the voltage sampling, the feed-forward term cancels the voltage dynamic of the measure voltage. The

current controller is configured with decoupling coefficient using the filtering inductance.

Taking the grid impedance into account, the voltage at PCC becomes affected by the output of the VSI. The grid connected VSI is able to measure the grid voltage at the PCC which will be the voltage feed-forward to the current controller. The voltage at PCC can be expressed as:

$$\begin{bmatrix} v_{pccd}(t) \\ v_{pccq}(t) \end{bmatrix} - \begin{bmatrix} v_{gd}(t) \\ v_{gq}(t) \end{bmatrix} = \begin{bmatrix} R_g & -\omega L_g \\ L_g & R_g \end{bmatrix} \begin{bmatrix} i_d(t) \\ i_q(t) \end{bmatrix} - L_g \frac{d}{dt} \begin{bmatrix} i_d(t) \\ i_q(t) \end{bmatrix} \tag{5.10}$$

The output of the PI regulator is given as:

$$\begin{cases} v_d^{'}(t) = K_p \cdot i_{de}(t) + K_i \int i_{de}(t) \cdot dt \\ v_q^{'}(t) = K_p \cdot i_{qe}(t) + K_i \int i_{qe}(t) \cdot dt \end{cases} \tag{5.11}$$

where $i_{de}(t)$ and $i_{qe}(t)$ are the errors between the current dq components and their references respectively. The current controller is redrawn to indicate the state space variables as shown in Figure 5.11.

The decoupling terms are given as:

$$\begin{cases} v_d^{''}(t) = -\omega \cdot L_f \cdot i_q(t) \\ v_q^{''}(t) = \omega \cdot L_f \cdot i_d(t) \end{cases} \tag{5.12}$$

Therefore the differential equations of the current controller without the voltage feed-forward can be expressed as follows:

$$\frac{d}{dt} \begin{bmatrix} \Delta v_d(t) \\ \Delta v_q(t) \end{bmatrix} = \begin{bmatrix} K_i & -\omega L_f \\ \omega L_f & K_i \end{bmatrix} \begin{bmatrix} i_{de}(t) \\ i_{qe}(t) \end{bmatrix} + \begin{bmatrix} K_p & -\omega L_f \\ \omega L_f & K_p \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{de}(t) \\ i_{qe}(t) \end{bmatrix} \tag{5.13}$$

where $\Delta v_d(t)$ and $\Delta v_q(t)$ are

$$\begin{cases} \Delta v_d(t) = v_d^{'}(t) + v_d^{''}(t) \\ \Delta v_q(t) = v_q^{'}(t) + v_q^{''}(t) \end{cases} \quad 5.14$$

As a linear system, it is possible that the system equations be rewritten into a standard format of the state space matrix.

$$\dot{p} = Ap + Bu \quad 5.15$$

$$y = Cp + Du \quad 5.16$$

where u, p and y are input, state variable and output matrices (vectors) respectively, A is the state space vector which is of particular interest for determining the stability as well as system performance. The Eigen value of matrix A shows the pole placement of the system. Let the I_{dref} and I_{qref} be the system input and the actual current be the output. The state space variables are selected to be x_1, x_2, x_3 and x_4 marked on Figure 5.10 and Figure 5.11. The system differential equations are listed below:

$$\begin{cases} \dot{x}_1 = [x_3 + (u_1 - x_1) \cdot K_p - R \cdot x_1 - x_2 \cdot \omega L_g] \cdot \dfrac{1}{L_f + L_g} \\ \dot{x}_2 = [x_4 + (u_2 - x_2) \cdot K_p - R \cdot x_2 + x_1 \cdot \omega L_g] \cdot \dfrac{1}{L_f + L_g} \\ \dot{x}_3 = (u_1 - x_1) \cdot K_i \\ \dot{x}_4 = (u_2 - x_2) \cdot K_i \end{cases} \quad 5.17$$

In order to clearly show the parameters selected as the state space variables, the system diagram is drawn and the location of the state variables are marked in Figure 5.11.

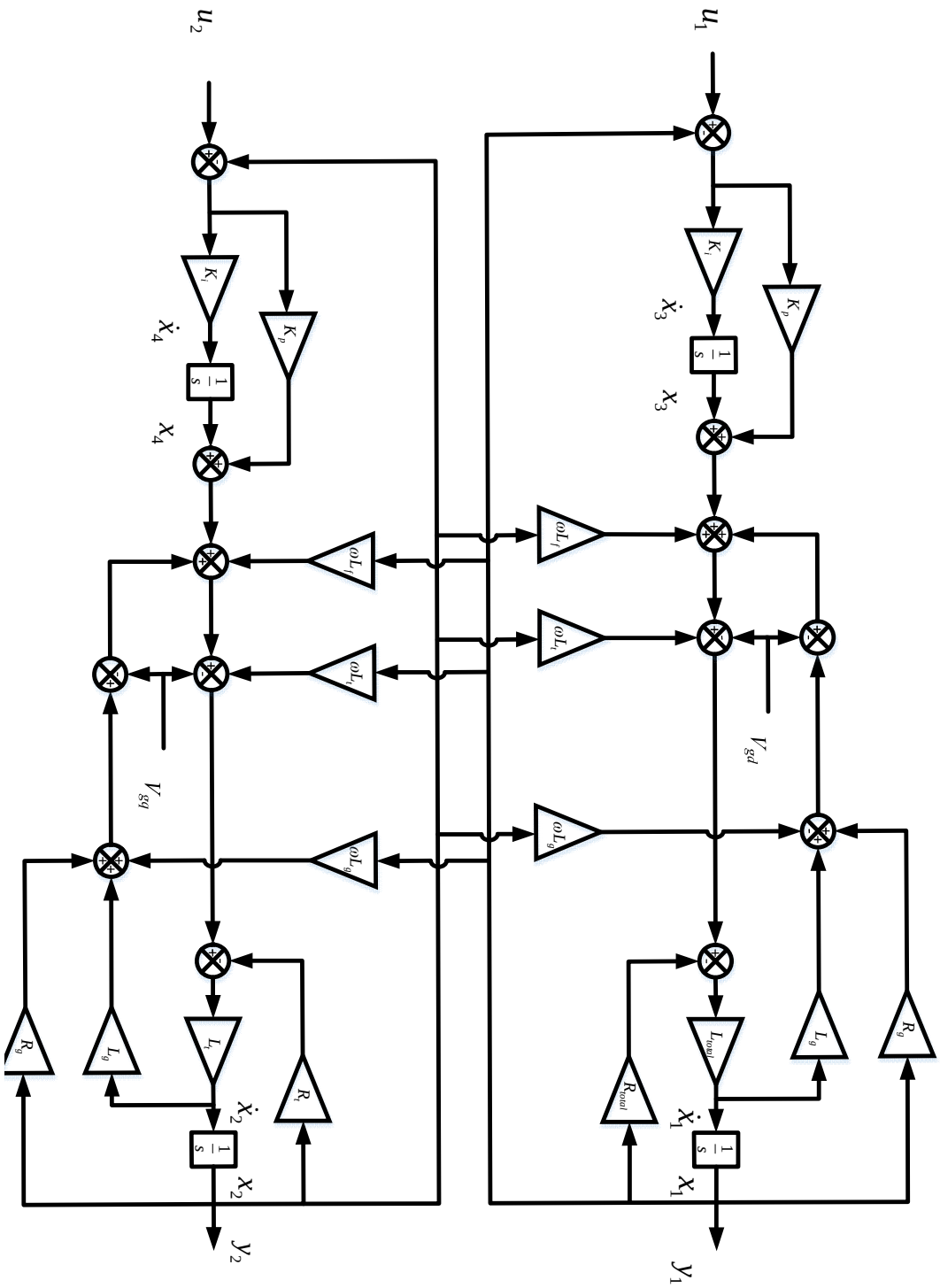


Figure 5.11. Placement of state variables

Reorganise the equations into the standard canonical format:

$$\underbrace{\begin{bmatrix}\dot{x}_1\\ \dot{x}_2\\ \dot{x}_3\\ \dot{x}_4\end{bmatrix}}_{\dot{p}} = \underbrace{\begin{bmatrix} -\frac{R_f+R_g+K_p}{L_f+L_g} & -\frac{\omega L_g}{L_f+L_g} & \frac{1}{L_f+L_g} & 0\\ \frac{\omega L_g}{L_f+L_g} & -\frac{R_f+R_g+K_p}{L_f+L_g} & 0 & \frac{1}{L_f+L_g}\\ -K_i & 0 & 0 & 0\\ 0 & -K_i & 0 & 0\end{bmatrix}}_{A} \underbrace{\begin{bmatrix}x_1\\ x_2\\ x_3\\ x_4\end{bmatrix}}_{p} + \underbrace{\begin{bmatrix}K_p & 0\\ 0 & K_p\\ K_i & 0\\ 0 & K_i\end{bmatrix}}_{B} \underbrace{\begin{bmatrix}u_1\\ u_2\end{bmatrix}}_{u} \qquad 5.18$$

The outputs are the *dq* currents which are actually among the state variables. The output matrix is constructed as following:

$$\underbrace{\begin{bmatrix}y_1\\ y_2\end{bmatrix}}_{y} = \underbrace{\begin{bmatrix}1 & 0 & 0 & 0\\ 0 & 1 & 0 & 0\end{bmatrix}}_{C} \underbrace{\begin{bmatrix}x_1\\ x_2\\ x_3\\ x_4\end{bmatrix}}_{p} + \underbrace{\begin{bmatrix}0 & 0\\ 0 & 0\end{bmatrix}}_{D} \underbrace{\begin{bmatrix}u_1\\ u_2\end{bmatrix}}_{u} \qquad 5.19$$

Assume that the parameter design of the current controller are the optimised values e.g. the case discussed in Section 5.2.1. The parameters of the filtering inductor and the current controller are listed in Table 5.2 below. The poles are plotted with increasing grid inductance and resistance separately using Matlab.

Grid resistance varying (Fig. 5.2. (a))	Grid inductance varying (Fig. 5.2. (b))	Control parameters
R_f = 80mΩ	R_f = 80mΩ	K_p=0.8
L_f =10mH	L_f =10mH	K_i=60
R_g=5~25mΩ (5mΩ step)	R_g=5mΩ	
L_g=1mH	L_g=1~5mH (1mH step)	

Table 5.2 System parameters.

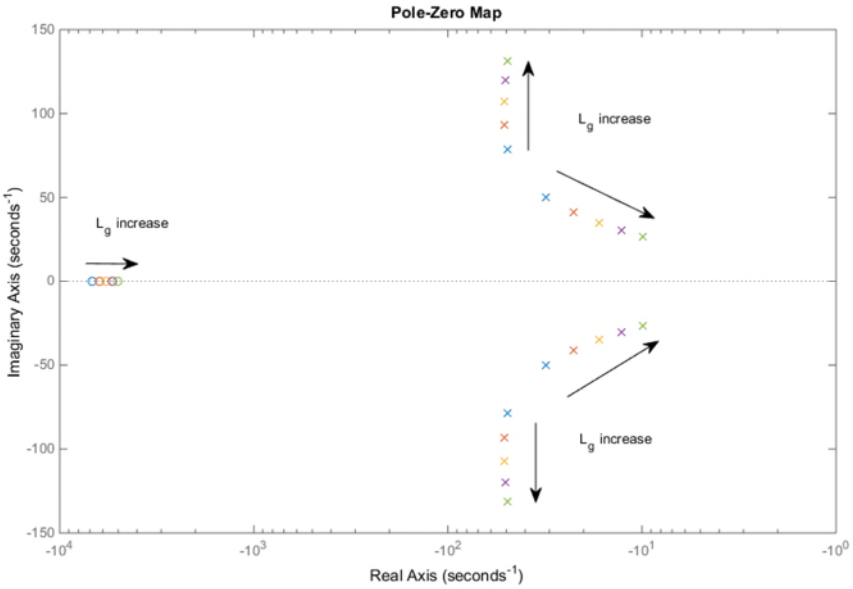


Figure 5.12. Pole-zero map of the system under study with increasing L_g.

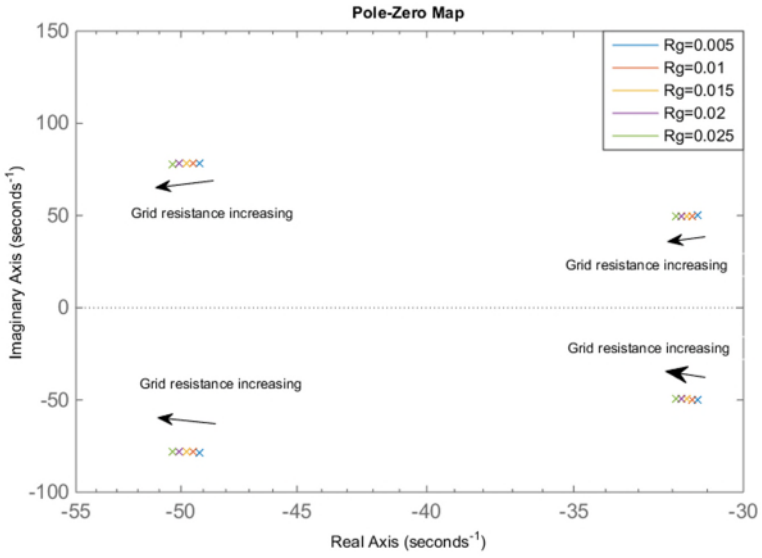


Figure 5.13 Pole-zero map of the system under study with increasing R_g

It can be seen that with the increase of the grid inductance, a second pair of poles (the pole pairs on the left hand side of the graph) are present and the damping of the second pair of poles is reduced. The reduction of the system damping ratio will cause oscillation in the output and

the system settling time is to be increased accordingly. In the case that the grid side inductance is much greater than the filtering inductance, the grid side dynamic coupling coefficient will be much greater than the controller side decoupling coefficient making the decoupling effect insignificant. The controller behaviour then approaches the elementary SRF-PI based current control without decoupling term. The idealised model of the system doesn't show that the second pair of poles falling into the right hand side of the imaginary axis of the s-plain. But considering a more complex model e.g. with dynamic of the PLL system or resonance of LCL filter if used, the lower damping ration indicates that the system is under risk of resonance which means the stability of the system is harmed. It can also be verified from Figure 5.12 that the first pair of poles are moving towards the zero point of s-plain showing that the system settling time increases. Viewing from the current response wave form, it can be seen that the first pair of poles represents the behaviour of average value of the output under oscillation dominated by the second pair of poles.

The solution to the problem illustrated above would be focus on the oscillation problem whose behaviour is represented by the second pair of poles. The reduced system response represented by the first pair of poles could be solved by increasing the controller bandwidth. However the controller bandwidth is subjected to not only the goal of optimising the system response under a certain a.c. side impedance but also factors including PWM switching frequency, sampling frequency and PLL dynamics. Therefore, the increase of the controller bandwidth will not be modelled here as it may cause additional problems. If the bandwidth is large enough, e.g. higher than half of the sampling frequency, then the system will lose stability due to insufficient sampling. Similar case will happen for a controller bandwidth higher than half of the PWM frequency, the output voltage determined by the duty ration of the PWM waveform is simply not fast enough to track the reference and lose stability. In real applications, if the grid side impedance is significant enough, and the output of the inverter will cause a voltage change at

the PCC where the grid voltage is measured. If the voltage change has a higher bandwidth than the PLL, the system is also at the risk of losing stability. The best counter action to the oscillation problem caused by the variation of the grid impedance would be acquiring parameters of accurate line inductance for decoupling the *dq* axes. The second pair of poles will disappear if the decoupling is ideal. However, the impedance of the grid can hardly be measured and moreover, it is not always the same over time. A closed-loop approach of observation to the grid impedance is a solution but it consumes additional computational power of the computing unit. Further, it is not easily achievable in voltage-sensor-less control thus it is not considered in this research. A passive adaptive method which will be used in the system design is to tune the controller off-line, taking the possibility of the grid impedance variation thus the reduction of the system damping into consideration. A compromise will be made between the system response and stability in the case of grid impedance variation. The system is tuned for a higher damping ratio by increasing the proportional gain for an assumed average grid inductance. Then if the grid inductance varies, the system has redundant damping to stabilise the system. The cost would be as discussed above, for a higher damping ratio, the system will take some additional time to clear out the error.

5.2.4 Performance of SRF-PI based dq-decoupled current control under variation of the grid frequency

The grid frequency deviation should be taken into consideration as the conventional *dq* decoupled control tuning was often made based on the assumption of the nominal grid frequency. The *dq* axis decoupling feed-forward in the current control system will not be accurate if the actual frequency is different from the assumed frequency. Therefore errors will occur between the actual coupling and decoupling terms. The frequency deviation could cause

the system behaviour change from the original design. As by the effect of the error in the decoupling term, the system can no longer be analysed based on the transfer functions provided in Section 5.2.1. The case is similar to the analysis in 5.2.2 as the decoupling accuracy is harmed by a different ω. However, the error of the decoupling term is different from the error caused by grid impedance. The grid frequency can be different from the nominal value, e.g. 50Hz. This could result in the change of system from two aspects. Firstly, the system will generate a steady state erro ifthe frequency locking mechanism, usually provided by a PLL, is not used. Considering this particular model, the *dq* signals obtained after applying *abc-dq0* transformation without correct grid frequency will no longer be constant but a sinusoidal waveform with its frequency being the difference between the actual frequency and the reference frequency for *abc-dq* transformation. In this case, the PI based controller is not able to track the reference signals without steady state error. This is already shown in Section 2.3. The second aspect of the change of the system response is due to the deficiency of the decoupling term in the current controller for the error between the assumed grid frequency and actual grid frequency. This change of system response will happen regardless if the *abc-dq0* is done at the correct frequency or not, as long as the parameter of the grid frequency in the decoupling term is not on-line adjusted. The analysis in this section will focus on the second aspect of change in the system's dynamic behaviour assuming that the *abc-dq0* is done at a correct frequency of the reference frame. A system block diagram is drawn and as shown in Figure 5.14, where the error of the decoupling of the *dq*-axis occurred due to the mismatch of the assumed nominal grid frequency ω and the actual grid frequency ω' is shown

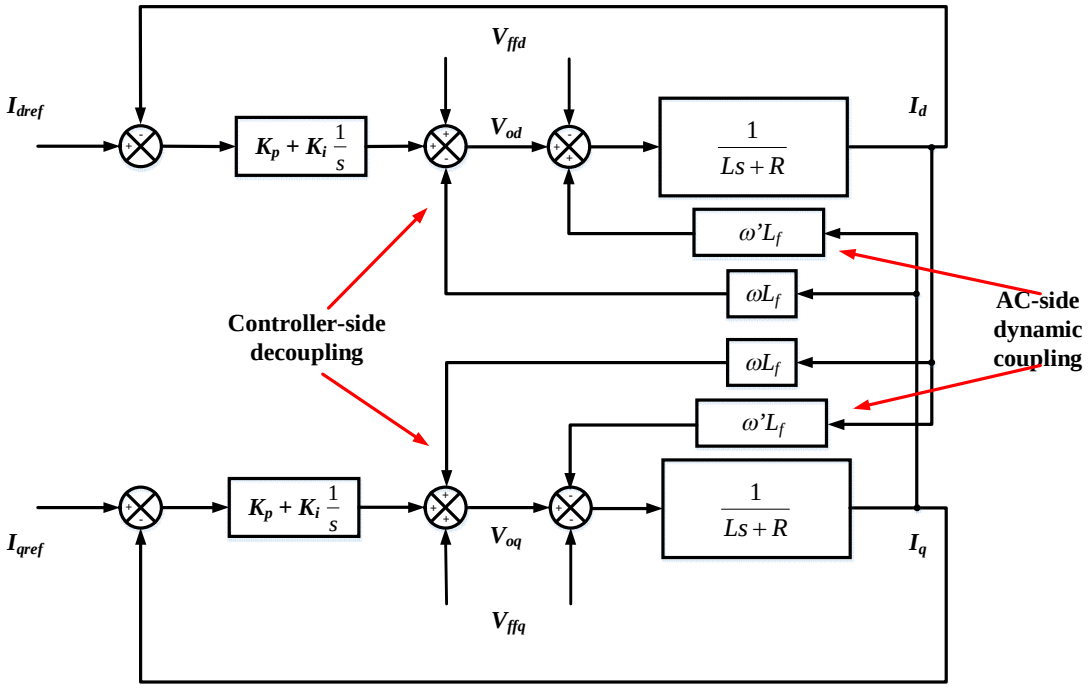


Figure 5.14 Pole and zero placing under different grid frequency

The influence of the change of the grid frequency on the dynamic behaviour of the controller is similar to that of the inductance mismatch as they both affect the accuracy of the *dq* decoupling. The following state space equations are obtained for the system shown in Figure 5.15.

$$\underbrace{\begin{bmatrix}\dot{x}_1\\ \dot{x}_2\\ \dot{x}_3\\ \dot{x}_4\end{bmatrix}}_{\dot{p}} = \underbrace{\begin{bmatrix}-\frac{R+K_p}{L} & -(\omega_{ff}-\omega_g) & \frac{1}{L} & 0\\ \omega_{ff}-\omega_g & -\frac{R+K_p}{L} & 0 & \frac{1}{L}\\ -K_i & 0 & 0 & 0\\ 0 & -K_i & 0 & 0\end{bmatrix}}_{A} \underbrace{\begin{bmatrix}x_1\\ x_2\\ x_3\\ x_4\end{bmatrix}}_{p} + \underbrace{\begin{bmatrix}K_p & 0\\ 0 & K_p\\ K_i & 0\\ 0 & K_i\end{bmatrix}}_{B} \underbrace{\begin{bmatrix}u_1\\ u_2\end{bmatrix}}_{u} \tag{5.20}$$

$$\underbrace{\begin{bmatrix}y_1\\ y_2\end{bmatrix}}_{y} = \underbrace{\begin{bmatrix}1 & 0 & 0 & 0\\ 0 & 1 & 0 & 0\end{bmatrix}}_{C} \underbrace{\begin{bmatrix}x_1\\ x_2\\ x_3\\ x_4\end{bmatrix}}_{p} + \underbrace{\begin{bmatrix}0 & 0\\ 0 & 0\end{bmatrix}}_{D} \underbrace{\begin{bmatrix}u_1\\ u_2\end{bmatrix}}_{u} \tag{5.21}$$

The pole and zero placement of the system is shown in Figure 5.15. The current control system can be expressed by a second order system if there is no error between the grid frequency used in the *dq* decoupling and the actual grid frequency. In that case, there will be only one pair of poles. The frequency deviation affects the accuracy of the *dq* decoupling and will result in extra oscillation. It has a more significant effect compared to the other parameters investigated in Section 5.23. Besides, if the frequency for defining the *dq* reference frame of the current controller is different from the real grid frequency, the controller will yield steady state error as introduced in Chapter 2. This proves a frequency locking mechanism is necessary. The decoupling coefficient could be adjusted in real time to solve the problem, but the band-width of the frequency parameter variation should be restricted for stability reason.

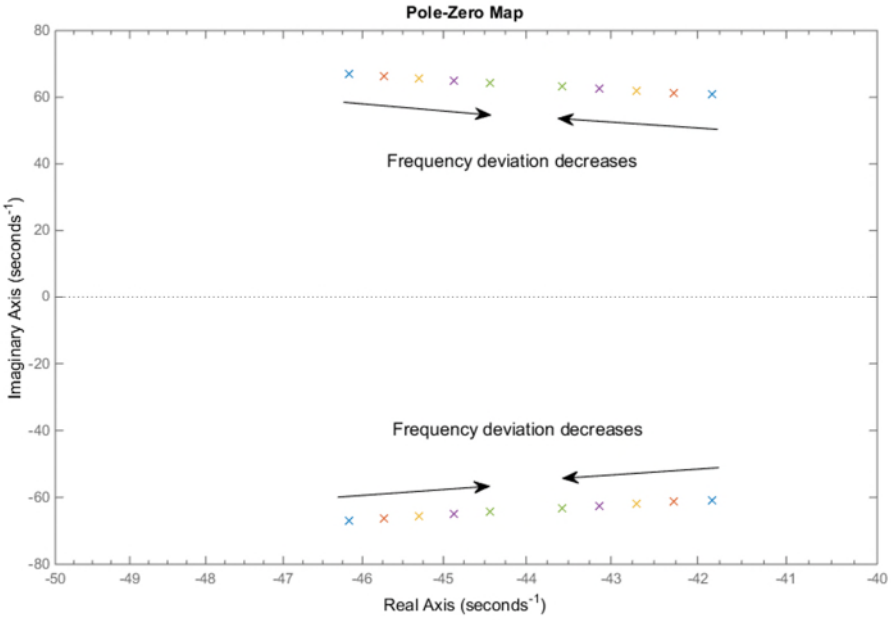


Figure 5.15 Pole and zero placing under different grid frequency

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5.2.5 Performance of the SRF-PI based dq-decoupled current control with voltage feed-forward delay

The above investigated the performance of the primary system design under different grid conditions. The ideal case is that the variation of the grid voltage is fully cancelled by the voltage feed-forward term. However in the case that the grid voltage is estimated where a delay is introduced, the system response to a change of the grid voltage will not be as ideal as shown in the analysis above. It is a similar case to those conventional systems which has non-ideal feed-forward voltage signals. One example is the voltage oriented current control especially considering its performance in the reality. The voltage feed-forward term will not be an ideal match to the exact grid voltage. The error of the grid voltage feed-forward can be caused by several facts. Firstly, the sampling of the grid voltage will not be ideal in reality for the errors between the desired parameters and rated parameters commonly existing in the components used for building a sampling board. Secondly, most of the automatic control actions are done by digital controllers nowadays. The sampling and signal processing introduces delay. Thirdly, the error can be created from a PLL transient. Fourthly, the symmetrical component decomposition system will also introduces delay. Among these factors, the PLL system and symmetrical component decomposition usually cause longer transient and larger errors. Thus

the effect of these dominating factors is modelled in the analysis below. In case of this system would introduce delay when tracking the dynamics of the measured signal, the voltage feed-forward terms in the controller will have error with respect to the actual grid voltage. The change of the grid voltage should be taken as disturbances and analysed. The disturbance transfer function should be included.

The dynamic response of the PLL is complex as it does not only introduce delay but also overshoot and high order oscillations. The PLL can be reduced to a second order system using small signal model. To simplify the problem, the PLL is assumed to be critically tuned so that the over shoot can be ignored. Then symmetrical component decomposition system using filtering method has a similar delay effect as the PLL. It will be valid for modelling the effect of these delays using a first order delay as shown in Figure 5.14.

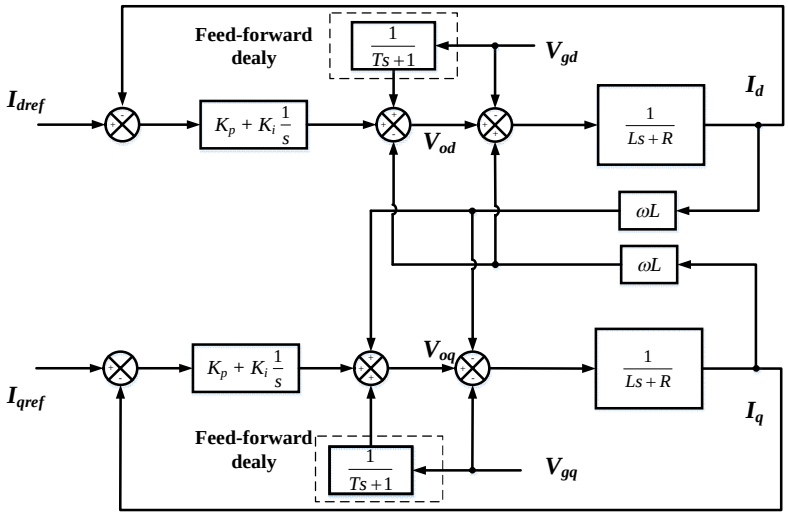


Figure 5.14. Block diagram of the system under grid voltage feed-forward delay

For a linear system, the system response should be the sum of the response against input change and the response against disturbance. Assuming the decoupling of the *dq* axis is ideally done, the system can be simplified as a SISO system as discussed in Section 5.2.1. The disturbance to the system will be the current response caused by the error between the real grid voltage and the inaccurate grid voltage feed-forward.

The simplified system is shown below in Figure 5.15:

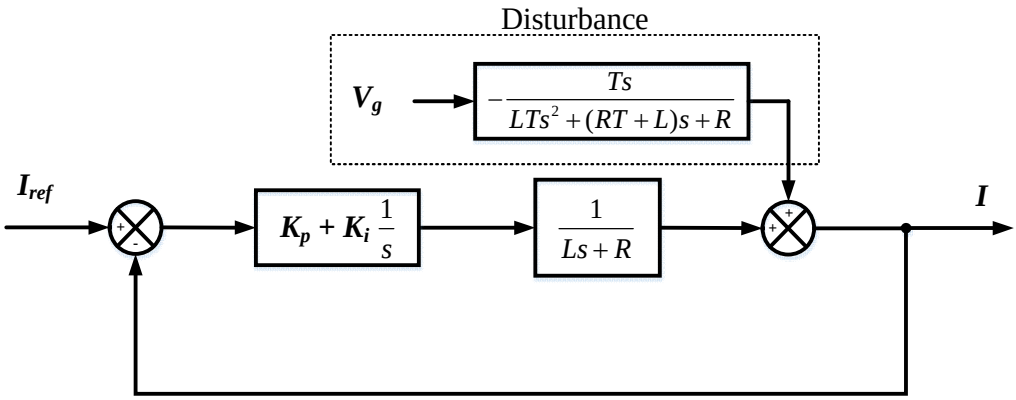


Figure 5.15. Small signal model of the system under study

The disturbance transfer function is:

$$D(s) = \left(\frac{1}{Ts+1} - 1\right)\frac{1}{Ls+R} \qquad 5.22$$

The delay introduced to the voltage feed-forward under changes of the grid does not only affect the rejection of disturbance but also causes the power tracking to take a longer transient stage. It can be verified from Equation 4.18 and 4.19 that the current reference is an inverse function of the grid voltage. In the previous discussion, the voltage disturbance is fully cancelled out by voltage feed-forward, the correct current reference for a desired power will be generated instantaneously. The speed of power tracking is subjected to the time constant of the current controller. But if the delay introduced to the voltage feed-forward which is also used to generate the current reference is significantly larger than the time constant of the current controller, the speed of power tracking will be subjected to the voltage feed-forward delay instead.

5.3 Grid voltage observer

Given the dynamic model of the grid side circuit and ignoring the delay and the none-linearity of the PWM stage, the line voltage is observable if the current and output voltage are known and the filter reactance given. The a.c. side dynamics of the VSI is given by:

$$\begin{bmatrix} v_{pccd} \\ v_{pccq} \end{bmatrix} = \begin{bmatrix} v_{od} \\ v_{oq} \end{bmatrix} + \begin{bmatrix} -R & \omega L \\ -\omega L & -R \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + L \frac{d}{dt} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \quad 5.23$$

The difference between the voltage at the PCC and the voltage output of the VSI is the voltage drop across the RL filter branch. For a given current output, the voltage drop is subjected to the RL filter parameters. Verified by the pole placement of such a system as stated in Figure 5.12, there is no poles and zeroes cancelling each other. Therefore the voltage drop across the RL filter is observable from the current injected with the parameter of the RL filter known.

The grid voltage observer utilises the current output of the VSI as a reference. A virtual filter model is built inside the controller based on the real parameters of the filter. An estimated voltage drop is fed into the virtual filter model to generate a virtual current response which is then compared to the actual current injected into the grid. The error between the actual current and virtual current during the transient stage is used to adjust the estimated voltage drop. As the relationship between the voltage drop and the current is fixed by the given RL parameter, the virtual current will equal the actual current in the steady state. PI decoupled current control is adopted as the controller to minimise the error until the system reaching steady state. Based on the analysis of the SRF-PI based *dq*-decoupled current control in Section 5.2.1, the bandwidth of the observer can be easily defined and adjusted. The grid voltage thus can be calculated based on the voltage output of the VSI and the estimated voltage drop. The block diagram of the proposed grid voltage observer is shown in Figure 5.16.

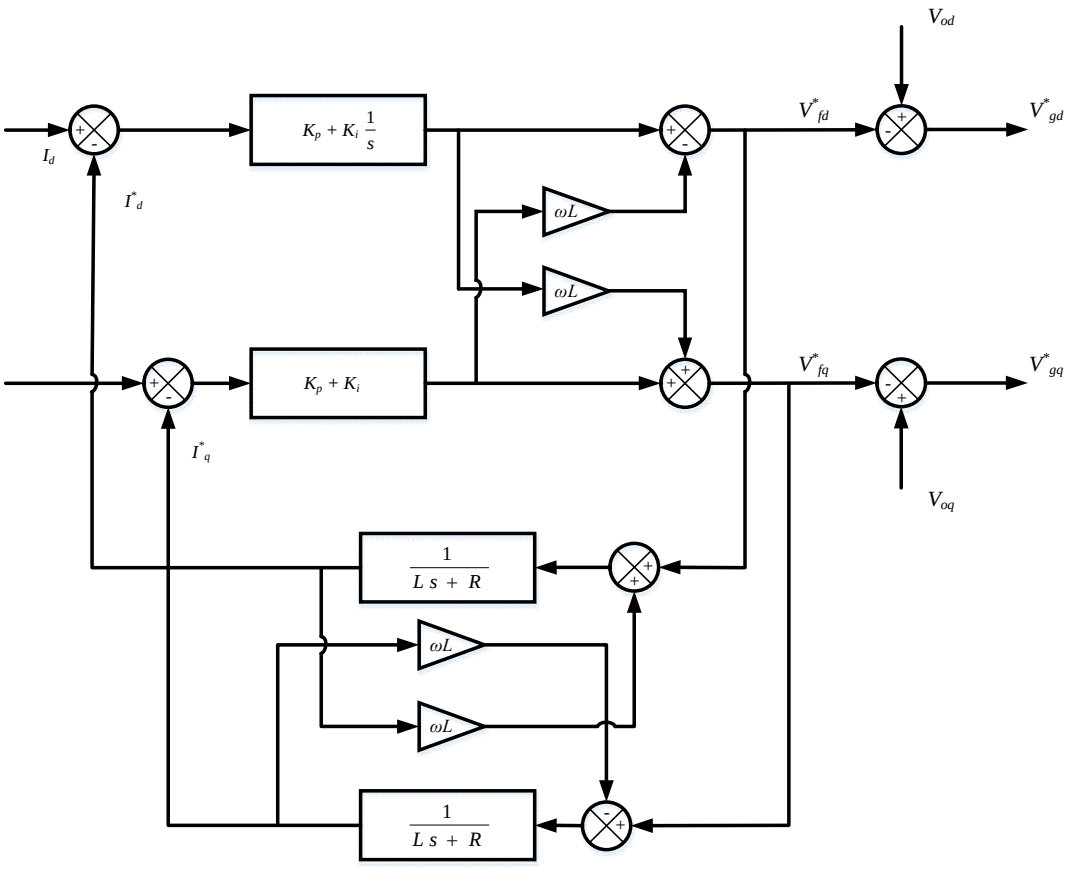


Figure 5.16. Block diagram of proposed voltage observer

As the reference to the observer is the current output whose dynamics are subjected to the bandwidth of the current controller, the current control loop should be viewed as the outer loop of the voltage observer.

The tuning procedure of the grid voltage observer is the same as that of the SRF-PI based current control analysed in Section 5.2.1. It is worth clarifying that for the case if the grid impedance is not negligible, this design is still valid. The observer is actually to estimate the voltage at the PCC where the voltage is measured for the conventional current control system. The voltage observer satisfied the design purpose as a replacement of the voltage measurements.

As the grid voltage observer has its own bandwidth thus delay between the actual voltage and the estimated voltage will occur during the dynamic stage. In Section 5.2.4, the non-ideal

voltage feed-forward is analysed based on the model which has a delay introduced to the V_d and I_d caused by the PLL . The delay of the estimated voltage of the observer is considered to have the same origin as the case discussed in this section. This effect could be analysed using a similar model. Therefore, the over-all performance of the a.c. voltage-sensor-less current control is expected to have similar behaviour to the VSI controlled by conventional controller with voltage sensor equipped but has voltage feed-forward delayed.

The grid voltage estimation can be simplified based on the ideal current control model discussed in Section 5.2.1 as the non-ideal situation such as feed-forward delay and current measurement delay will not exist in this virtual system. The *dq* axis decoupling can also be done ideally as the parameters of the virtual load and the parameters used in the decoupling terms can exactly match each other. Therefore the model is reduced to a SISO system. The following diagram, Figure 5.17, shows the small signal model of the grid voltage estimation system.

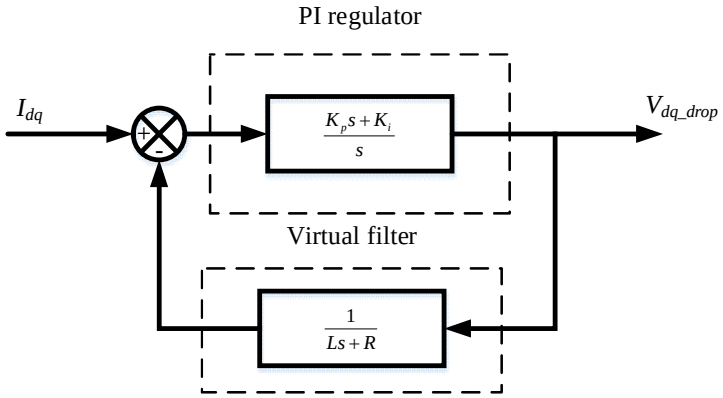


Figure 5.17 Small signal model of the voltage estimation system

The closed-loop transfer function can be drawn from the diagram as:

$$G(s) = \frac{K_p s + K_i}{Ls^2 + (R + K_p)s + K_i} \qquad 5.24$$

As generally applied when designing the control parameters, the input to a system should have a lower bandwidth comparing to the control system to ensure the stability. To keep the system stable, the band-width of the inner-loop should be at least three times larger than the outer loop. Further, in this system design, the bandwidth of the voltage observer is selected to be five times of the current control to avoid any undesired oscillation. This is because the current control system will not be good enough if it is stable, but the output of the controller in term of V_d and V_q need to be oscillation free to ensure the power quality. The low-pass-filtering characteristic of the PI controller also provided the harmonic rejection ability where the irrelevant noise and harmonic are attenuated so that a clean voltage signal with the fundamental component of the control interest.

5.4 A.c. voltage-sensor-less current control

The *dq* decoupled current control needs the information of the grid voltage in order to control the power output as well as minimise the transient current overshoot in the case of the grid voltage variation. With the grid voltage estimated by the observer discussed in Section 5.3, this piece of information is acquired without using voltage sensors. As a main concern in all sorts of control system designs is that the stability issue should be discussed.

As discussed in Section 5.3, the d.c. bus voltage control loop is considered to be the outer loop of the controller and should have the slowest dynamic to ensure stability. It is tuned to be significantly slower than the current control stage in this research, so its dynamics can be ignored in some analyses. The stability of the system is defined by the current control and the grid voltage estimation. In the voltage-sensor-less control, the voltage for generating the current reference is the output of the grid voltage observer whose dynamics is coupled to that of the current controller. As the observer is tuned with a wider bandwidth compared to the

current control as discussed in Section 5.3, the high frequency components in the current reference need to be restricted to ensure the stability of the system. A low pass filtering stage is deployed to serve this function. It breaks the dynamic coupling between the grid voltage estimation and the current controller, as shown in Figure 5.18, therefore will be referred to as the dynamic decoupling stage in the discussion below.

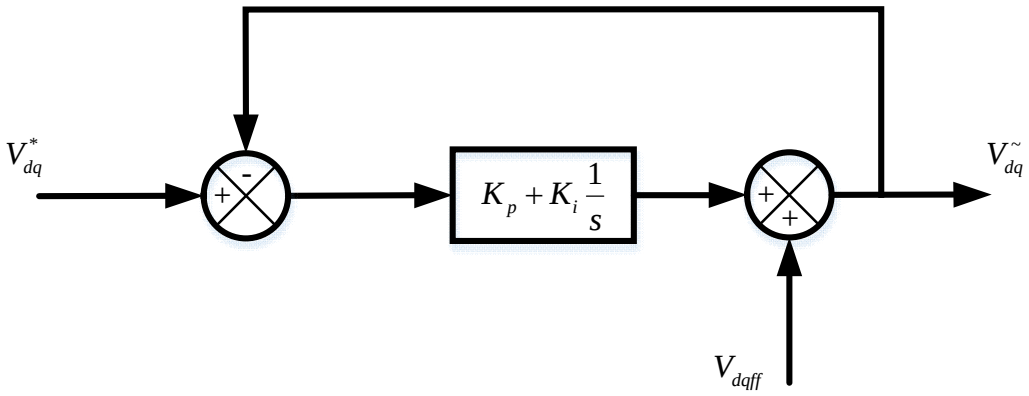


Figure 5.18 Diagram of the dynamic decoupling stage

The close loop transfer function is:

$$D(s) = \frac{K_p s + K_i}{(K_p + 1)s + K_i} \qquad 5.25$$

The bode plot below (Figure 5.19) shows the magnitude-frequency and phase-frequency characteristics of the dynamic decoupling stage under a selected set of PI coefficient are 0.1 for proportional gain and 40 for integral gain.

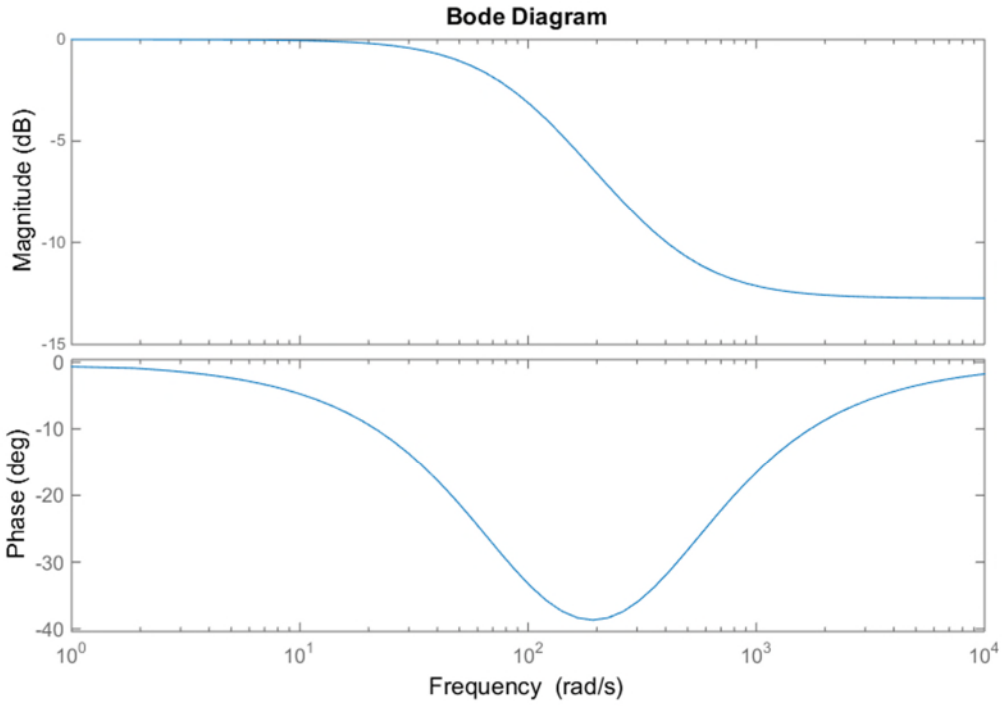


Figure 5.19 Bode diagram showing the low-pass character of dynamic decoupling stage

The PI controller is tuned to have a bandwidth of 1/5 of the current controller so that the current controller is swift enough to track the input signal and avoid undesired oscillation. The overall block diagram is shown in Figure 5.20.

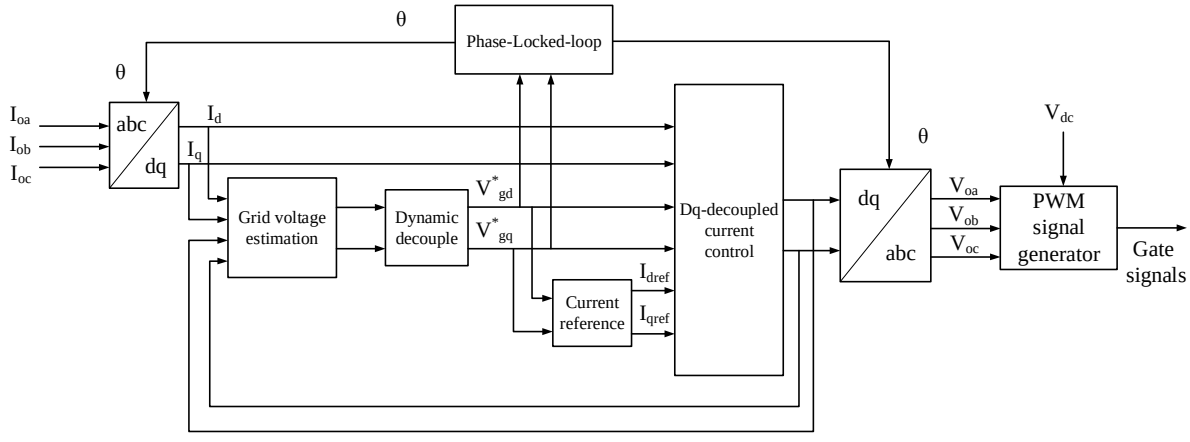


Figure 5.20 Block diagram of the basic a.c. voltage-sensor-less current controller

The stability of this a.c. voltage-sensor-less controller can be found based on a simplified model with the dynamics of the power control stage and PLL ignored. Assuming that the grid

frequency is tracked and the coupling impedance is accurately acquired, the system can be further simplified as a SISO system. The transfer functions of the current controller, grid voltage observer and the dynamic decoupling stage has been derived in the previous sections under the same assumptions. The diagram of the system is shown below in Figure 5.21. The whole system closed-loop transfer function then can be drawn as:

$$G(s)=\frac{I}{I_{ref}}=\frac{H_1(s)H_3(s)}{1+H_1(s)H_3(s)-D(s)H_2(s)H_3(s)} \qquad 5.26$$

where $H_1(s)$ is the transfer function of the PI regulator in the current controller, $H_2(s)$ (Equation 5.24) is the closed-loop transfer function of the grid voltage estimation, $H_3(s)$ is the transfer function of the RL filter and $D(s)$ (Equation 5.32) is the closed-loop transfer function of the dynamic decoupling stage.

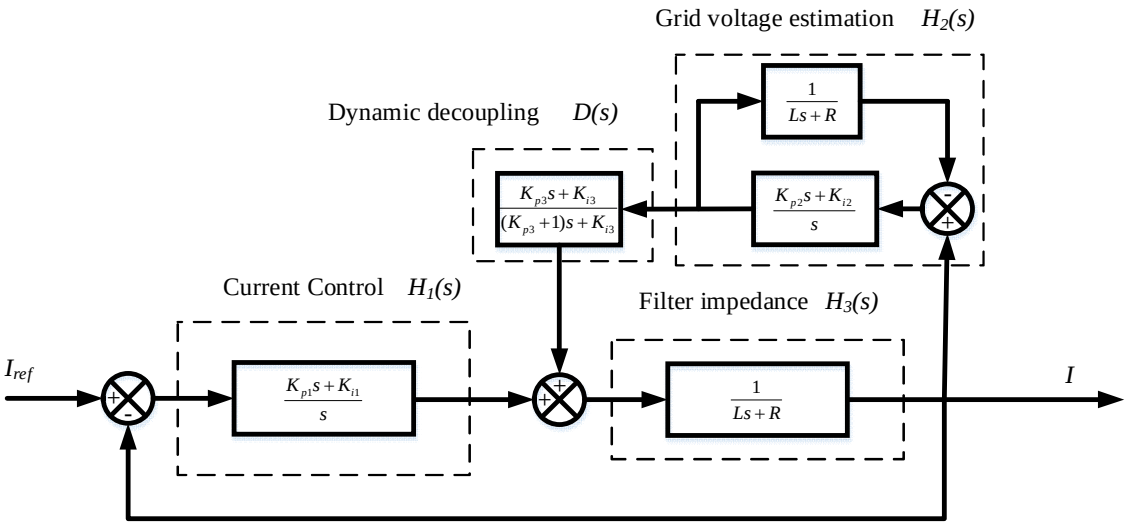


Figure 5.21 Block diagram of small signal model of the a.c. voltage-sensor-less controller

For a given set of control parameters listed below in Table 5.3, the system stability can be analysed using its bode plot, Figure 5.22. The phase margin is 70 degrees which is close enough

to the optimum design objective of 60 degrees. In Table 5.3, the parameters of the system are listed. The PI coefficient of the grid voltage observer is selected for enough bandwidth to track the change of the a.c. side voltage caused by the control effort done by current controller. As mentioned earlier in this section, the PI coefficient of the dynamic decoupling stage is selected for reducing the bandwidth of the reference signals to the current controller to stabilize the system.

Design parameters of the closed-loop system	
K_{p1}	0.8
K_{i1}	60
K_{p2}	4
K_{i2}	300
K_{p3}	0.1
K_{i3}	40
R	0.1Ω
L	10mH

Table 5.3 Design parameters of the a.c. voltage-sensor-less system

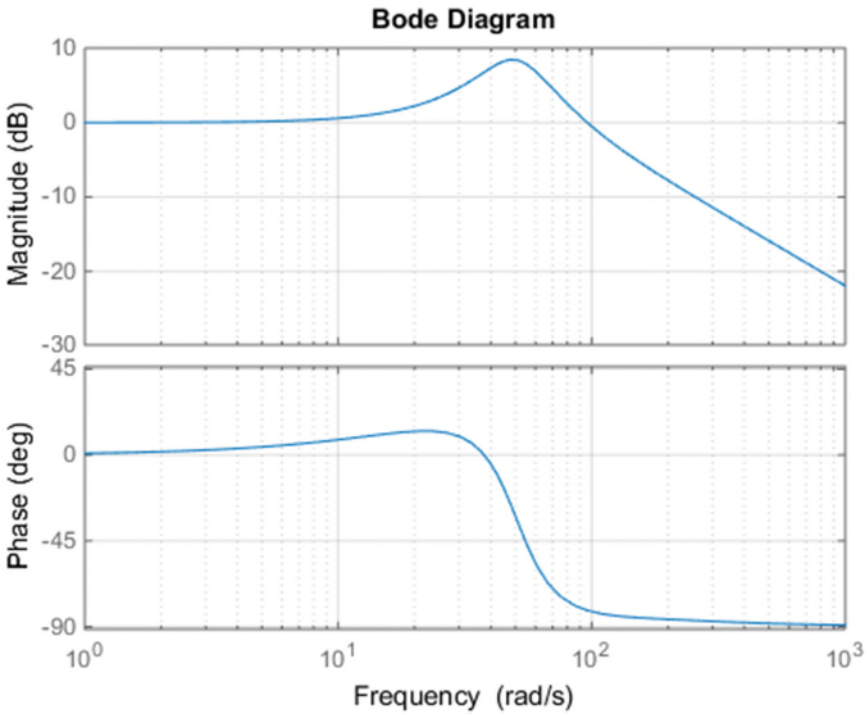


Figure 5.22 Bode diagram of the closed-loop system

The current control and the grid voltage estimation necessary for generating the current reference to regulate the power has been designed as discussed above. The basic a.c. voltage-sensor-less current control structure is made clear and shown in Figure 5.20. As briefed in Chapter 2, the *dq*-decoupled current control is not sufficient for tracking a sinusoidal current reference. The negative sequence current needed for compensating the 2nd harmonic power is not controllable through a single *dq*-decoupled current controller for the positive sequence, due to the reason illustrated above. Therefore, two current controllers in the two different reference frames are needed for controlling the positive and negative phase sequence separately and simultaneously, as shown in Figure 5.23. The steady state error is eliminated in this arrangement [120].

A conventional SRF-PLL system is used to track the phase angle and the frequency of the system. The estimated V_q of the positive sequence is used to drive the PLL system. The current reference is generated through Equation 4.18 in Chapter 4. The grid frequency is an important

reference for operation of the control system as well as the symmetrical component decomposition algorithm. The main objective of adopting this PLL is for tracking the grid frequency. The power can be controlled through the current reference generated from Equation 4.18 as long as the grid frequency is correctly tracked. As the symmetrical components of the current measurements are decomposed and grid voltage are estimated by each phase sequence, the conventional SRF-PLL system will be sufficient to operate even if the grid voltage is unbalanced.

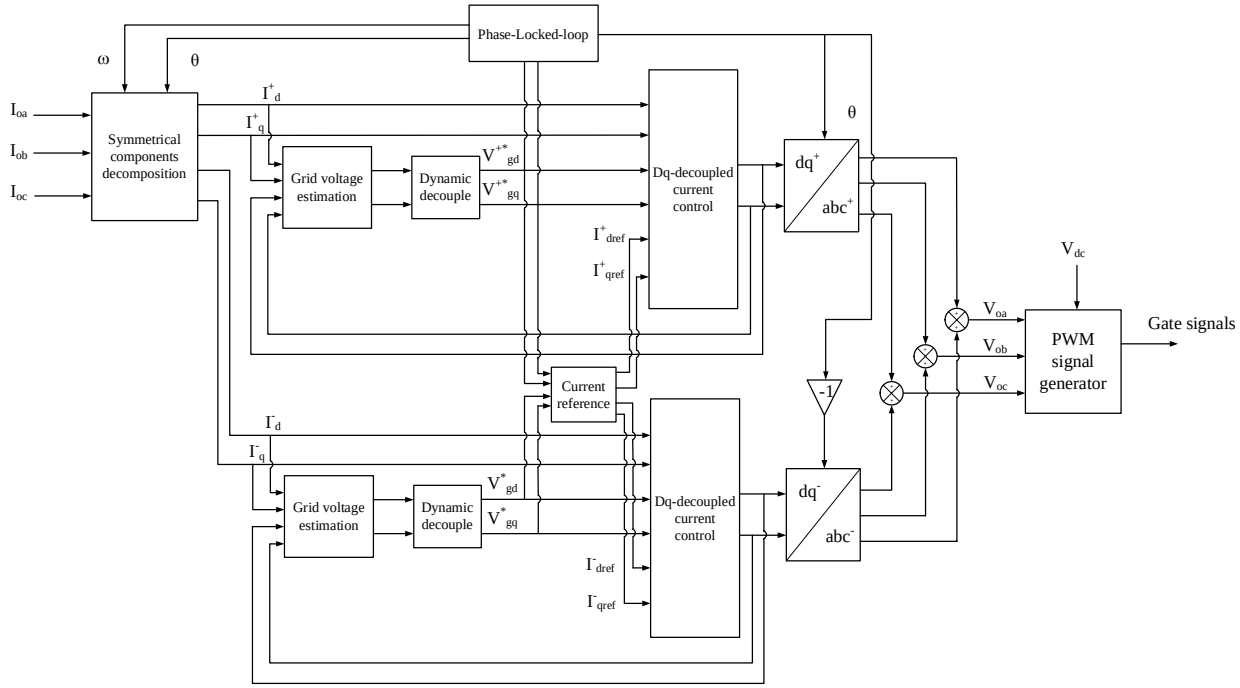


Figure 5.23 Diagram of a.c. voltage-sensor-less current controller for riding through unbalanced grid fault

5.5 Chapter summary

First of all, the highest frequency component that is possible to control in the current is half of the switching frequency or the sampling frequency. The bandwidth of the current controller

should not exceed the limit set by these value otherwise the control will not be stable. The upper limit of the current controller is further limited by the delay introduced by the symmetrical component decomposition algorithm which is usually the dominant factor to consider.

The sampled current is decomposed into positive and negative phase sequences using the decomposition algorithm design discussed in Section 3.2.5. The decomposition of the phase sequence introduces delay which has a harmful effect on the current control stage as shown in the analysis of Section 5.2.4. The decomposition should be proposed with less delay to improve the performance of the current controller. The proposed symmetrical component decomposition algorithm has transformed the signals of a lower frequency to a higher frequency. This action could cause the sampling to become insufficient and cause alias. In the application, the delay used in the decomposition algorithm should be maintained above a certain limit, restricted by the sample rate. The parameter N_{res} which affects the delay is selected to be 5 to in the later sections to improve the performance.

A conventional SRF-PLL is deployed with the input to be the estimated grid voltage of the positive sequence to track the angle and grid frequency of the system. The grid voltage is proposed to be estimated by the voltage observer introduced in section 5.3. Then it will be used to generate the current reference using instantaneous PQ theory under *dq* reference frame. The use of the SRF-PLL system is valid for the proposed control system to ride-through the unbalanced grid fault as the symmetrical components is decoupled before the grid voltage of the positive and negative sequence voltage are estimated. So that the SRF-PLL system has the input of only the positive sequence voltage.

Chapter 6 D.C. Bus Voltage Control and Initial Synchronisation to the Grid

6.1 Introduction

Apart from the design of the a.c. voltage-sensor-less controller, there are other two aspects which need to be investigated to ensure the safe operation of the VSI. Firstly, the d.c. bus voltage should be regulated in order to provide high enough voltage to avoid the PWM process falling into the non-linear over modulation mode of operation, or being over charged to threaten its own safety at the same time. Secondly, due to the lack of information about the grid voltage before starting-up the VSI, large transient over current may occur which could damage the inverter power modules. Therefore the start-up process should be specially designed to avoid the problem.

6.2 D.c. bus voltage control and capacitor design

The d.c. bus capacitor should be designed to withstand the voltage fluctuations caused by the variations from either the generated power or the disturbance from ac-side grid. The d.c. bus voltage should be controlled to serve the control purposes of protecting the capacitor from over charging or falling into the non-linear over modulation range. In this section, the selection of the capacitance of the d.c. bus and the controller design are discussed with regarding to the current control objectives.

6.2.1 D.c. natural voltage variation

In VSI operation, the output voltage at the power electronic terminals should be at least equal to the grid voltage in order to control the output current and hence the power into the grid. The commonly used PWM switching with a three leg inverter is only able to produce am equivalent a.c. voltage with its amplitude equal to half of the d.c. link voltage. Therefore, the d.c. bus voltage should be higher than peak-to-peak value of the grid line voltage. This is the ideal case for the minimum requirement to the d.c. bus voltage. In reality, the d.c. bus voltage capable of supporting the VSI with power output is significantly higher than the amplitude of the nominal grid voltage due to the following reasons. Firstly, the power modules introduces a voltage drop. The size of the voltage drop is dependent on the material used in the power electronic devices. Also, the semiconductors will introduce resistance which causes further voltage drop depending on the current flow. The d.c. bus voltage should be high enough to compensate these voltage drops. Secondly, depending on the size of the coupling impedance between the VSI and the grid, the actual terminal voltage may need to be higher than the grid voltage which varies in the ±10% statutory limits to drive a current flow. In a case when the VSI is supporting the grid by injecting lagging reactive power, the output voltage at the VSI terminal should be even higher for the same amount of real power output. This requires sufficiently high d.c. bus voltage. Thirdly, the modulation depth for generating the PWM signal is usually controlled between 0.8 and 1. With higher modulation depth, the performance of the VSI in term of the harmonic injection improves. But a margin is needed for anticipating the grid voltage variation. In case of providing such a margin by reducing the modulation depth, the d.c. bus voltage should be increased.

Assuming a VSI is connecting to the 230V three-phase system and providing power to the grid. The first constrain for selecting the d.c. bus capacitor is that the rated voltage level of the capacitor should be at least twice as high as the tip of a required output voltage. If the d.c.

voltage drops below two times of the output voltage amplitude, the switching scheme regardless its nature e.g. PWM, hysteresis and etc., will not be able to produce the desired voltage in a linear manner thus performance of the VSI is affected. A typical consequence would be harmonic injection and for voltage-sensor-less control and it is further added with oscillation in the control effects.

The amplitude of the output voltage varies with the output power factor under the same real power output. Unity power factor is typical for most of the small renewable generation units. The phasor diagram in Figure 6.1 below shows the output voltage regarding to the current output and the grid voltage. In this research, the rated power of the VSI is considered around a few kW and regarded as small generation. Thus the capacitor design will only take the requirement for the VSIs working as power source other than some other equipment responsible of injecting reactive power to support the voltage.

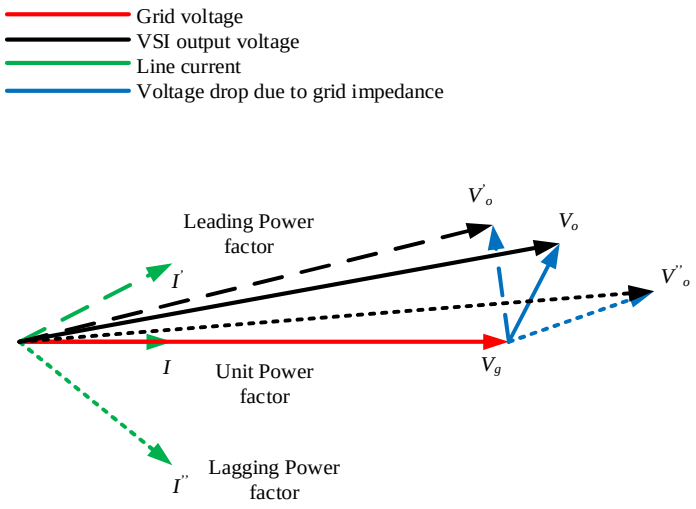


Figure 6.1. Phasor diagram, output voltage under different power factors

Another aspect for selecting the voltage rating of the d.c. bus capacitor is the modulation depth. A typical modulation depth is around 0.8 for practical applications. This modulation depth is selected for a balance between the harmonic restriction and the transient tolerance. Therefore,

the rated voltage level of the d.c. bus capacitor can be selected according to the two constrains discussed above.

The physical size of d.c. bus capacitor is another issue when designing the d.c. side capacitor. The capacitor is a space consuming component of a VSI module. In the accepted range, the capacitor should be designed as small as possible. This facilitate the modular design of the VSI board in term of spacing efficiency. However, as an energy storage component, the d.c. bus capacitor determines the physical inertia of the VSI system response. With larger inertia, the VSI system becomes stiffer against impact brought about by grid voltage dip and sudden upper stream changes. It is pointed out in some other researches that for tuning the behaviour of a VSI to emulate a synchronous generator, the physical inertia plays a vital role [141]. In this case, the capacitance of the d.c. bus is desired to be higher which results in a larger capacitor design. Because of this conflict, compromise should be made. Further, the capacitor can usually tolerant the voltage exceeding its rated voltage within 10% range. This property should be considered so that the size of the capacitor can be further restricted.

Without losses, the grid connected VSI should output power equal to the d.c. side power. The power flowing into the d.c. bus is determined by the upper stream devices such as rectifiers or d.c. boosters. In renewable power generation, the power acquired from the environment varies over time. Therefore the power generated is not a constant but dynamically changes. The change of the power generated will be reflected on the d.c. bus voltage as overshoot/undershoot during the charge/discharge process. For the upper stream devices of a passive nature e.g. a diode rectifier, the power output of the VSI should be adjusted accordingly to balance the power flowing through the d.c. bus. As the voltage fluctuation of the d.c. bus is subjected to the energy exchange between the d.c. side and a.c. grid, in the case when the VSI plays a role in controlling the d.c. voltage, power output is specifically refer to the real power.

6.2.2 D.c. natured voltage controller design

The d.c. bus capacitor has its dynamics modelled from the relationship between the energy stored in the capacitor and its terminal voltage. The energy stored in the capacitor is:

$$E = \frac{1}{2} C V^2 \qquad 6.1$$

It is clear that the energy stored in the capacitor is proportional to the voltage square. The voltage square therefore is used as the input to the controller, expressed as $W(s)$ in the transfer function. The d.c. side resistance is neglected as it is usually very small. Knowing that the energy is power integrated by time, through Laplace transformation, the transfer function for the d.c. bus can be derived from:

$$P(s) = \frac{1}{2} s \cdot C \cdot W(\mathrm{s}) \qquad 6.2$$

The error between the reference voltage square and the actual voltage square will be feed into a PI regulator and the output will be used to adjust the power reference on the ac-side, as shown in Figure 6.2. The voltage exceeding the reference value will drive the PI controller to output a higher power reference for the a.c. side so that the additional energy stored in the d.c. bus capacitor can be dispatched. A feed-forward term of the power reference is added, usually calculated by the measured d.c. bus voltage and current on the input side, to improve the dynamic response of the d.c. voltage control. The power variation due to the change of the generator side will be decoupled by this term under ideal conditions. In this case, the d.c. voltage control is dealing with the d.c. voltage variation caused by disturbance from the a.c. side.

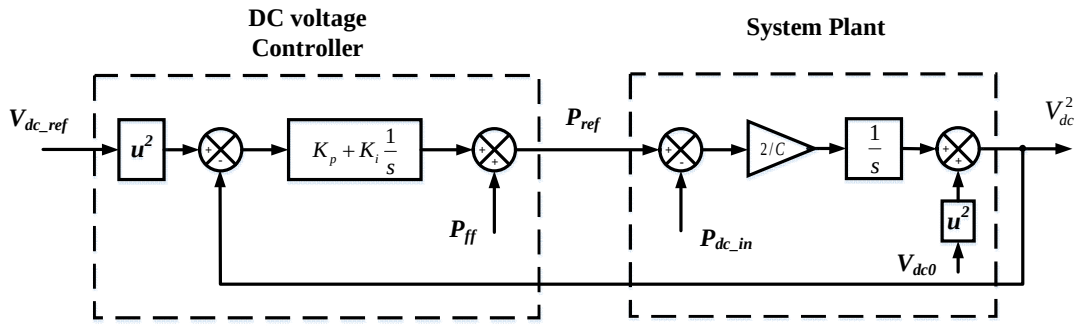


Figure 6.2 D.c. voltage control, open-loop approach, closed-loop diagram

The ideal model of the d.c. voltage control and the controlled system shown above can be used to describe the fundamental concept of the d.c. bus voltage control. It expresses the dynamics of the d.c. voltage control as an outer-loop of the control system. However, the current control stage will not be able to reach unlimited band-width in reality. The power output of the VSI will not be able to immediately follow the reference power in this case. Before the current controller could reach a new steady state, the d.c. capacitor will continue to be charged or discharged depending on the actual situation. Then the original design of the d.c. voltage controller will not work as desired. Therefore the transient delay of the current controller should be taken into consideration, as shown in Figure 6.3. Assuming that the system is operating at the grid frequency and the parameters of the a.c. side impedance is known to the system controller, the current controller can be modelled using the simplified current control model provided in Section 5.2.1 without considering the complex current controller behaviour. The system under discussion is shown in Figure 5.20.

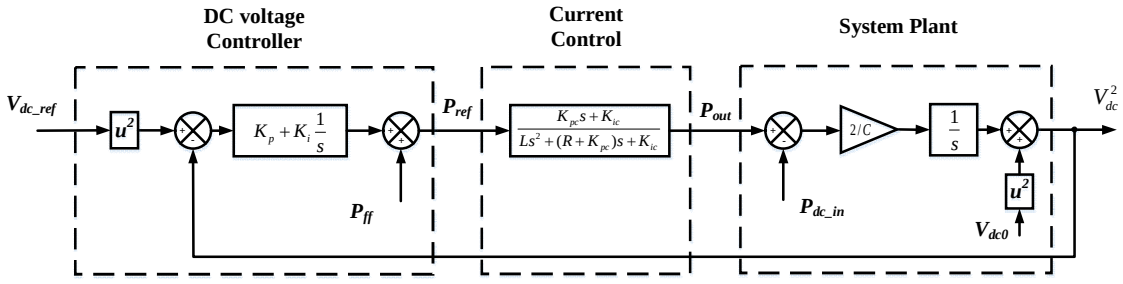


Figure 6.3. d.c. voltage control loop taken dynamic of the current control into consideration

The closed-loop transfer function can be derived:

$$G(s)=\frac{Y(s)}{F(s)}=\frac{2\cdot K_{p1}\cdot K_{p2}\cdot s^2+2\cdot(K_{p1}\cdot K_{i2}+K_{p2}\cdot K_{i1})\cdot s+2\cdot K_{i1}\cdot K_{i2}}{L\cdot C\cdot s^4+C\cdot(R+K_{p1})\cdot s^3+(C\cdot K_{p1}+2\cdot K_{p1}\cdot K_{p2})\cdot s^2+2\cdot(K_{p1}\cdot K_{i2}+K_{p2}\cdot K_{i1})\cdot s+2\cdot K_{i1}\cdot K_{i2}} \qquad 6.3$$

where K_{p1} and K_{i1} are the gains of the PI regulator of the d.c. voltage controller; K_{p2} and K_{i2} are the gains of the PI regulator of the current controller; L and R are the inductance and resistance of the a.c. side and C is the capacitance of the d.c. capacitor.

The boundary of the design of the PI gains of the d.c. voltage controller for a specific system can be found by inspecting the location of the poles. The parameters of the system is listed in Table 6.1 below. The pole-zero map and bode plot are plotted accordingly in Figures 6.4 and 6.5. The capacitance is decided for an original design of the converter board before putting into test rig which is changed in the later research stage for handling power fluctuation which will be discussed in the next section.

Design parameters of the d.c. voltage control system	
K_{p1}	2~10
K_{i1}	300
K_{p2}	8
K_{i2}	200
C	460μF
R	0.2Ω
L	10mH

Table 6.1: Parameters of the d.c. voltage control and the system

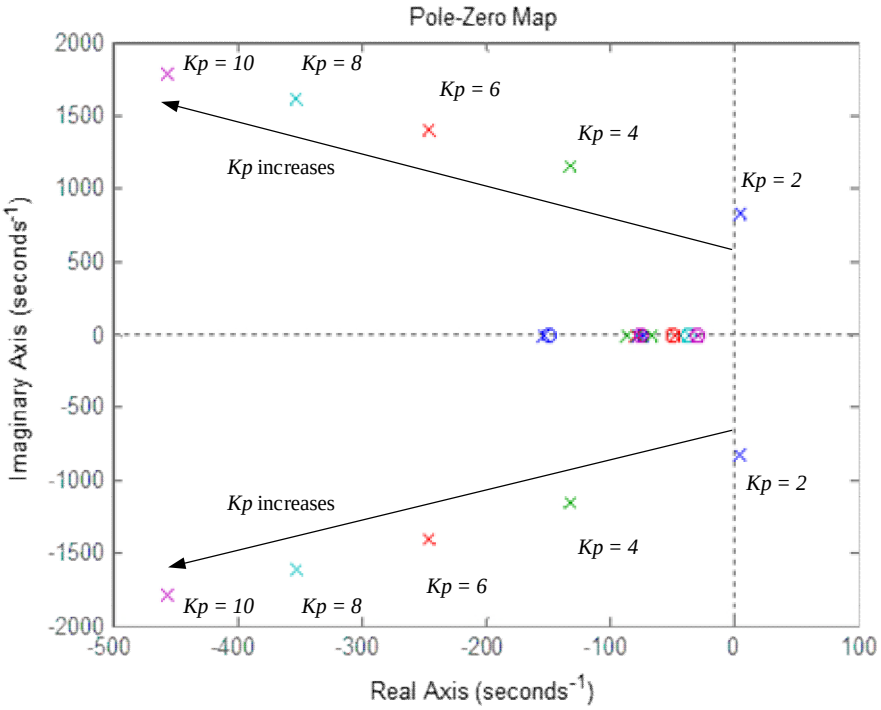


Figure 6.4: Pole-zero map of the system under study

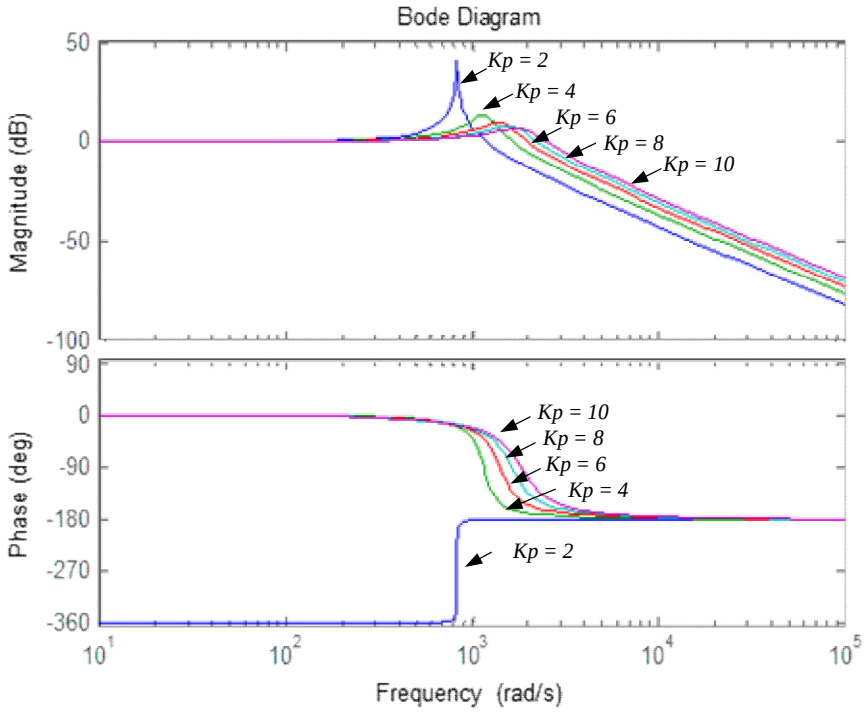


Figure 6.5: Bode plot of the system under study

It is clear from the pole-zero map that with the given parameters, the system start to be unstable when K_{p1} is around 2 and less. K_{p1} should be increased to ensure the stability of the system. The damping ration of the system increases with increasing K_{p1}. The desired damping ratio of 0.707 is reached when K_{p1} equals 69.

The performance of the d.c. voltage control is affected by the parameters of the current controller, the a.c. side impedance and the size of the capacitor. The tuning of the controller needs to take these factors into consideration. In the design process, the response of the current controller is defined by factors independent of other parts of the control system. The design of the size of the d.c. bus capacitor can be guided by the requirement of absorbing negative sequence power which is detailed later. In the design process, the response of the current controller is defined by factors independent of other parts of the control system. So with other parameters defined by the grid side, its controller should be done under guidance provided by the current controller design.

6.2.3 A.c. natural voltage variation

The d.c. bus capacitor design could vary from the design discussed above due to different control strategies of the VSI. The voltage fluctuation has two distinctive features. The design method above considered a problem of d.c. voltage rise/fall of a d.c. nature caused by a slowly varying power mismatch. The fluctuation resulted from an a.c. side harmonic or unbalanced phase output is regarded as of an a.c. nature, in which case the d.c. voltage will be shaped with high frequency ripples. The frequency of the ripple could be roughly verified by the oscillation frequency of the relevant harmonic on a fundamental *dq* reference frame e.g. for a typical 5^{th} and 7^{th} harmonic injection on the a.c. side, the d.c. voltage ripples will be the 6^{th} harmonic. The uncompensated output power during an unbalanced voltage dip will also cause the d.c. side

voltage oscillation as the negative sequence is the -1st order harmonic in another sense. If the voltage control is utilised to generate the current reference to compensate the unbalanced power, two problems can be addressed. Firstly, the use of the PI regulator in the d.c. voltage control system will introduce delay, therefore the power reference generated will not change in an accurate manner to compensate the power unbalance on three phases. Secondly, even if the power reference is ideally tracking the desired trajectory to compensate the power, it will cause the current reference oscillating in a sinusoidal pattern. As discussed above, the SRF-PI based current control is not capable of tracking a sinusoidal reference without error. Therefore, it is not feasible to integrate the unbalanced power control into the d.c. voltage control loop.

The voltage ripples on the d.c. side caused by harmonic power is neglected in this research as even for the capacitor design considering only the d.c. natured voltage change, the power oscillation caused by harmonic is usually very small as the higher order harmonics are restricted on the grid side. For the d.c. voltage fluctuation due to unbalanced phase power, it usually causes bigger problem due to the negative sequence voltage being much higher than those harmonics. This oscillation is rejected from the current controller side. Also the control strategies vary with different applications during unbalanced fault-ride-through. Some of them intended to stabilize the power system by absorbing the negative sequence current/voltage which naturally results in a d.c. voltage oscillation. The design of the size of the capacitor should take a different approach as discussed later. For a system designed without the duty of absorbing the negative sequence components, the d.c. capacitor design could take the approach discussed above.

Considering the case of an unbalanced voltage dip and assuming that the output power is not compensated accordingly, the capacitor size can be selected from an energy absorbing point of view. The oscillating instantaneous power can be expressed as:

$$p_o(t) = \Delta P_{amp} \sin(2\omega t + \varphi) \tag{6.4}$$

where ΔP_{peak} is the amplitude of the oscillating power, given by:

$$\Delta P_{peak} = (V_d^+ \cdot I_d^- + V_q^+ \cdot I_q^- + V_d^- \cdot I_d^+ + V_q^- \cdot I_q^+) + (-V_q^+ \cdot I_d^- + V_d^+ \cdot I_q^- + V_q^- \cdot I_d^+ - V_d^- \cdot I_q^-) \tag{6.5}$$

Noting the *dq* term in the equation is obtained via a power invariant *dq* transformation. Otherwise a coefficient of 3/2 should be multiplied.

The energy exchange due to this power oscillation is also a sine function with its peak calculated to be:

$$\Delta E_{peak} = \int_0^{\frac{1}{2}T} \Delta P_{amp} \sin(2\omega t) dt \tag{6.6}$$

where *T* is the fundamental period.

In this research, the system is modelled as a 50Hz system. Applying the grid frequency and its fundamental period, the energy peak is:

$$\Delta E_{peak} = \frac{\Delta P_{amp}}{100\pi} \tag{6.7}$$

For a given d.c. bus capacitor with its capacitance being *C*, the peak voltage variation is:

$$\Delta V_{peak} = 2\sqrt{\frac{\Delta E_{peak}}{2C}} \tag{6.8}$$

This voltage variation should not cause the d.c. voltage rise above 10% of the rated voltage. If it is calculated to be higher than the limit under a possible assumption of the unbalanced voltage dip, the d.c. bus capacitance should be increased, either by selecting larger capacitor or connecting more in parallel. Guided by this equation, the d.c. side capacitor is selected to be 1380μF with rated voltage of 800V.

To summarise the discussion in this section, the capacitor design has different approaches considering two possible kinds of disturbances. The VSI designed to absorb the unbalanced current should have a larger d.c. bus capacitor to support the system. In this research, different power control objectives are equally considered. Therefore the capacitor design will follow the second approach for riding-through the unbalanced fault with power of negative sequence flowing into the d.c. side. The design of the d.c. voltage control should follow the guidance provided by analysing the current control system bandwidth. The d.c. voltage control should be deactivated when the VSI is operating for absorbing negative sequence power.

6.3 Initial transient ride through with ensured safety of the power modules

6.3.1 Current hysteresis control

In addition to the techniques involved in the voltage-sensor-less control introduced in the last section, a VSI start up process needs to be considered. The initial synchronisation to the grid is a very important step that all the grid connected VSI systems should carry out. For conventional VSI control systems, the phase-locked-loop used for extraction of the direct and quadrature signals as well as the frequency of the grid voltage is usually activated before the rest of the control system. By taking this step, the information of the grid synchronisation is acquired. A failed initial synchronisation may cause a large transient current when the power module is activated. A test result is shown below to demonstrate the seriousness of the failed initial synchronisation.

For the proposed voltage-sensor-less control, it is also very important to acquire grid synchronisation before activating the inverter. However, it is now impossible to carry out the

conventional procedure due to the nature of the voltage-sensor-less control. It is a new and yet important task for the a.c. side voltage-sensor-less system as no direct measurement is available. In this research as well as some other researches, the method for synchronising the VSI to the grid has been established for steady state operation [54-57, 80, 133]. The system start-up is a different case. Firstly, the initial transient currents needs to be controlled to avoid damaging the components. Secondly, the power flow should be controlled to avoid undesired charge/discharge of the d.c. bus capacitor.

Based on the discussion above, an initial synchronisation operation stage should be introduced. The initial synchronisation operation will have the following two distinct features: first, the current should be controlled within the safety range of the power modules and without a severe transient stage; second, the power flow during the initial synchronisation operation should be controlled so that the d.c. bus capacitor is protected from over charging. Due to the limited bandwidth associated with the linearized current control methods, the initial transient current is not able to be controlled within the safe rang quickly. Further, for a considerably large error between the estimated grid voltage and the actual voltage. The stability and performance of the voltage-sensor-less control system determined above using small signal model is no longer valid. There is a risk of prolonged transient stage or even loss of stability. The current hysteresis control on the other hand, offers an ideal solution with its “unconditional stability” and fast current transient [58, 62]. Therefore, a start-up is proposed under current hysteresis control.

6.3.2 Tuning of the hysteresis control, hysteresis band design

The correlation of several factors decided the switching action of the power modules. Control system wise, the set of hysteresis band and the sampling frequency of the computing device has opposite effect on the average switching frequency e.g. larger hysteresis band will cause

the average switching frequency to reduce [61]. From the VSI and a.c. grid side point of view, the voltage drop between the coupling inductor and the desired current dynamic should be analysed based on different situations. Firstly, the voltage drop across the coupling/filtering inductor is not constant due to the a.c. voltage at the receiving grid end. For a given coupling inductance, the voltage drop decided the current variation rate in time. So the current dynamics is different at different time point along one quarter of the fundamental cycle, resulting in different switching duty-ratios. Secondly, the current reference could be changing subjected to the power control purposes. The change of the current reference could either accelerate the approaching of the actual current to the hysteresis band or decelerate the process. The switching will be affected accordingly.

From regulating the switching loss point of view, the maximum switching frequency should be restricted [58, 60-63]. The recent micro-computing units usually have a relatively high sample rate compare to the maximum switching frequency of the IGBT. Ideally if the d.c. voltage is high enough regarding to the a.c. side peak to peak voltage, the current can be controlled to rise/fall so fast that it can always catch up with its reference within one sampling period. The switching of the IGBT dominated by current hysteresis control therefore will be commanded to be equally fast as the sampling frequency e.g. high above 10 kHz. It may be obviously too high for an IGBT to handle. Therefore the number of samples between two switching state changes should be analysed if the sampling frequency of the computing unit is significantly higher than the desired switching frequency.

From harmonic injection regulation point of view, an important factor that should be taken into consideration when designing the hysteresis band is to regulate the average switching frequency. The range of the average switching frequency can be provided by the prediction of the maximum and minimum switching frequency.

The switching state change will be triggered by the sampled current exceeding the hysteresis band. The switching cycle will be an integer of the sampling period in a digital current hysteresis control. One switching cycle should be the period defined by three such switching state changes, which is during the actual current waveform passing the inner sector between the hysteresis bands twice [61]. For this condition to be satisfied, the current variation rate times the number of sampling periods between two switching state changes should be larger than the sum of two times of the hysteresis band and the current reference variation during the mean time. One key factor to predict the switching period is the possible rate of the current variation. The switching period along the desired current trajectory will be analysed in the following section.

Assume that the d.c. side voltage and a.c. side voltage can be given as:

$$v_{ac}(t) = \frac{V_{dc}}{2} \cdot m \cdot \sin \omega t \qquad 6.9$$

where m is the modulation depth and the d.c. side voltage is assumed to be kept constant.

The voltage drop across an L filter will cause the current to rise/fall at the rate of:

$$\frac{d}{dt}\Delta i(t) = \frac{\Delta v(t)}{L} \qquad 6.10$$

where ΔV is the voltage drop which is the difference between the d.c. side voltage and a.c. side voltage.

In a two level VSI topology, the output voltage at the terminal of the VSI output will be either $+\frac{V_{dc}}{2}$ or $-\frac{V_{dc}}{2}$ regarding to the a.c. side neutral point for two different switching states on one leg. The upper switch will be switched on for driving the current to rise and lower switch on for driving the current to fall. The voltage drop across the L filter is given by:

$$\begin{cases} \Delta v_r(t) = \dfrac{V_{dc}}{2} - v_{ac}(t) \\ \Delta v_f(t) = -\dfrac{V_{dc}}{2} - v_{ac}(t) \end{cases} \tag{6.11}$$

Applying the conditions of the state change of the hysteresis control, the number of samples during the current rise and fall are subjected to the limits below:

$$\begin{cases} \Delta i_r(t) + i_0 \geq i_{ref}(t) + B \\ \Delta i_f(t) + i_0^{'} \geq i_{ref}(t) - B \end{cases} \tag{6.12}$$

where B is the hysteresis band and i_0 is the initial current value. The initial current value should be the first sampling that detects the current is getting out of the hysteresis band thus the switching state changes. The current variation term of Δi is the rise/fall rate of the actual current integrated by the rise/fall time.

$$\begin{cases} \Delta i_r(t) = \dfrac{1}{L} \cdot \int_{\varphi/\omega}^{\varphi/\omega + n_r T_s} \Delta v_r(t) \cdot dt = \dfrac{1}{L} \cdot \{ \dfrac{V_{dc}}{2} \cdot n \cdot T_s + \dfrac{V_{dc} \cdot m \cdot [\cos\varphi - \cos(\omega \cdot n \cdot T_s + \varphi)]}{2 \cdot \omega} \} \\ \Delta i_f(t) = \dfrac{1}{L} \cdot \int_{\varphi/\omega}^{\varphi/\omega + n_f T_s} \Delta v_f(t) \cdot dt = \dfrac{1}{L} \cdot \{ -\dfrac{V_{dc}}{2} \cdot n \cdot T_s + \dfrac{V_{dc} \cdot m \cdot [\cos\varphi - \cos(\omega \cdot n \cdot T_s + \varphi)]}{2 \cdot \omega} \} \end{cases} \tag{6.13}$$

where φ is the initial angle of the voltage, T_s is the sampling period and n is the number of sampling between switching state changes.

The current reference will be in-phase with the ac-side voltage if the unity power factor is achieved. Assuming this is the case for the switching actions under analysis, Equation 5.31 should be rewritten as:

$$\begin{cases} \dfrac{V_{dc}}{2 \cdot L} \cdot n_r \cdot T_s + \dfrac{V_{dc} \cdot m \cdot [\cos\varphi - \cos(\omega \cdot n \cdot T_s + \varphi)]}{2 \cdot \omega \cdot L} + i_0 \geq I_{ref} \sin(\omega \cdot n_r \cdot T_s + \varphi) + B \\ -\dfrac{V_{dc}}{2 \cdot L} \cdot n_f \cdot T_s + \dfrac{V_{dc} \cdot m \cdot [\cos\varphi - \cos(\omega \cdot n \cdot T_s + \varphi)]}{2 \cdot \omega \cdot L} + i_0^{'} \geq I_{ref} \sin(\omega \cdot n_f \cdot T_s + \varphi) - B \end{cases} \tag{6.14}$$

A further analysis on the maximum frequency existence of the fixed-band hysteresis current control regarding to the location along the ac-side voltage waveform in the proposed system

proved that at the zero-crossing of the ac-side voltage, the switching frequency reaches its maximum value. In these equations, the inductance of the L filter, sampling period and grid frequency are fixed with given conditions of the system and considered as constants. The initial current value term in the equations under steady state will be close to the hysteresis band from outside with maximum error no larger than the possible current change in one sampling period. The number of sampling periods between the switching on and off are restricted by the desired maximum switching frequency with given sampling frequency. The hysteresis band therefore can be set accordingly.

For the maximum switching frequency occurring, one switching period is the sum of the time of current rising and falling. Assuming that the hysteresis band is critically set to achieve

$$\begin{cases} i_0 = I_{ref} - B \\ i_0^{'} = I_{ref} + B \end{cases} \qquad 6.15$$

The following equation expressing the maximum switching frequency can be derived from Equaion 6.15, with the effect of a.c. side voltage ignored as during a switching period, the variation of the a.c. voltage is insignificant.

$$f_{switching} = \frac{1}{(n_r + n_f) \cdot T_s} \leq \frac{V_{dc}}{8 \cdot B \cdot L} \qquad 6.16$$

Therefore the maximum switching frequency can be adjusted by changing the value of the hysteresis band. Noting that the expression of the switching frequency is also restricted by the sampling frequency. As mentioned in the previous section, the switching state change will only happen after a sampling is taking. For the maximum switching frequency allowed that is above half of the sampling frequency, the hysteresis controller could be tuned to be switching once every sampling. In that case, the hysteresis band is zero.

6.3.3 Voltage estimation

The performance of current hysteresis control varies with different system topologies. For the system with a clamped d.c. neutral and grounded as neutral, the current on each phase could have a free access by controlling the current flowing into the neutral without interfering the other phases. Therefore, the voltage ripple is considered small as for no interference occurs [140]. However if the a.c. side and d.c. bus neutral points are assumed floating, currents will need the access to flow back to the negative side of the d.c. bus. Note that the switching of the power modules are not synchronised in a fixed-band hysteresis control in many cases; therefore the access is largely provided by the free-wheeling diodes in the power modules of the other phases, which is passive and uncontrollable, causes interference between phases. The current rise/fall time will be subject to the line to line voltage and the coupling impedance other than the phase voltage. This could results in larger current ripples. In this research, a two level VSI with a floating neutral is assumed. Therefore the case with large current ripples discussed above is expected. These current ripples need to be filtered out when using the current to analyse the grid voltage. Filters with lower cut-off frequency will be utilized for the system with larger current ripples.

To cancel the effect of the interference between phases, the gate signals are filtered and transformed into line-to-line voltages. Knowing that the amplitude of the phase voltage is $1/\sqrt{3}$ of that of the line-to-line voltage and the phase is shifted by 30 degrees, the phase voltage can be extract.

The voltage at the PCC can be estimated by the current, output voltage and the parameter of the coupling inductor based on a synchronous reference frame. The same voltage estimation algorithm as introduced in Section 5.3 will be utilized. The current sampling in the PWM operation stage will be same as the switching frequency known as the synchronised sampling.

The current ripples as a result of the switching will not exist in the sampled waveform. However, the hysteresis current control will have a variable switching frequency. This makes the synchronised sampling impossible to deploy. Anti-aliasing filter will be used on the sampled current to attenuate the high order harmonics.

6.4 Chapter summary

The design of the d.c. bus capacitor and the d.c. voltage control are proposed taking the two aspects into consideration in the overall control system design. The variation of the d.c. voltage due to generated power mismatching the output power is handled by the d.c. voltage controller. The output power of the VSI is adjusted accordingly. In the case of an unbalanced grid fault, the negative sequence power may be absorbed by the d.c. bus capacitor. The capacitor should be large enough to handle the power oscillation and maintain at a necessary voltage level to ensure that the modulation stays in the linear range.

An initial synchronisation to the grid is necessary and a solution is proposed with the use of the hysteresis current control to avoid large transient current damaging the power electronic devices. The grid voltage can be estimated during this operation. The proposed grid voltage estimation method provides good performance for its low-pass-filtering characteristic. This is particularly important to ensure the quality of the control as the hysteresis current control has a wide range of harmonic content.

Chapter 7 Simulation Study of A.C. Voltage-sensor-less Control System and Simulation Results

7.1 Proposed symmetrical component decomposition

Simulation is carried out to examine the transient of the decomposing algorithm used to deal with a sudden unbalanced grid voltage change. The disturbance is that the voltage dip will reduce the positive sequence voltage while a negative sequence voltage will be added in. N_{res} is set to 21 in this simulation study. It can be calculated from Equation 3.34 that the duration of the detection transient will be approximately 0.95ms and this is verified in Figure 7.1. The comparison of the duration of the transient of different algorithms is provided in Figure 7.2 (a) and (b), where a clear reduction of the duration of the transient is observable.

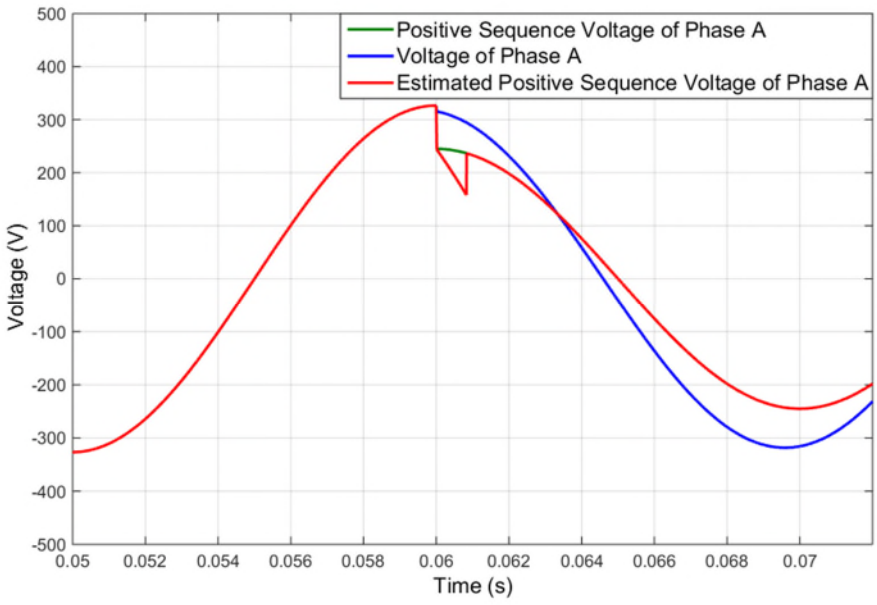
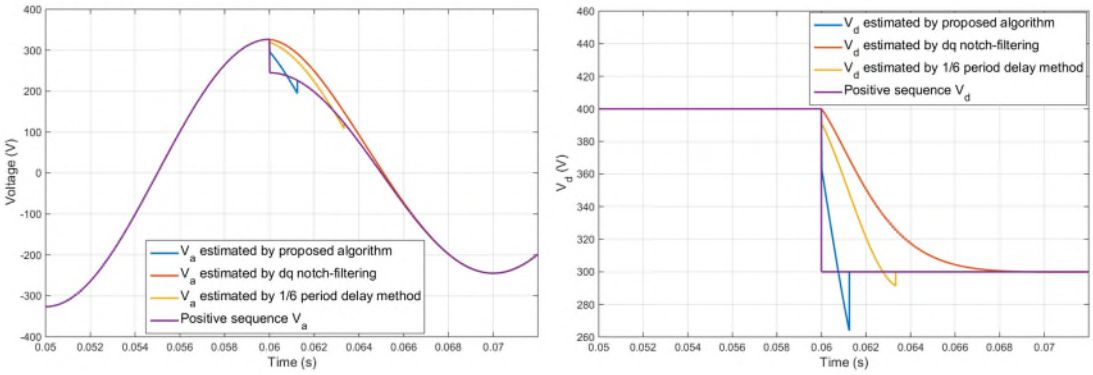


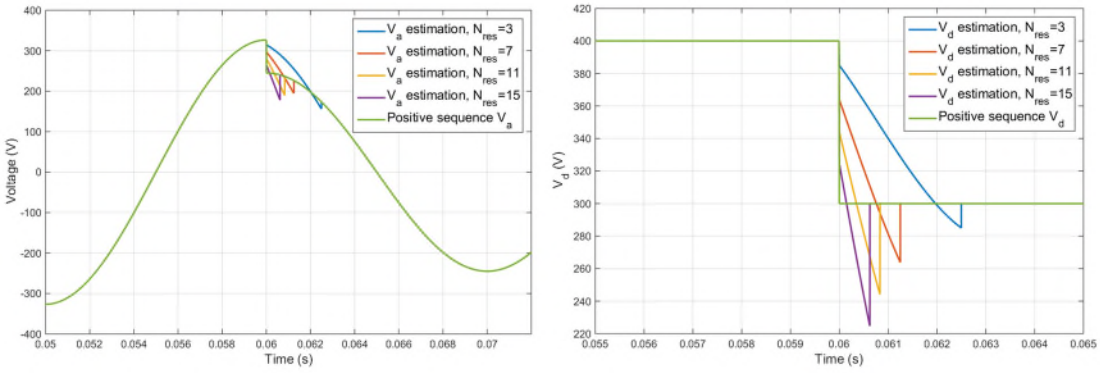
Figure 7.1 Sinusoidal signal of positive sequence extracted by proposed symmetrical components decomposition network with N_{res}=21



(a) (b)

Figure 7.2 Comparison of transient between the proposed and other algorithms

Figure 7.3 also shows that the overshot will increase with increasing N_{res} under a certain input change. Following the transient error analysis in Chapter 5, one per unit step change in d-axis or q-axis value of the positive sequence or negative sequence are made to the input signal one by one for checking the error. The per unit IAE error indices of the estimated V_d and V_q of the positive sequence voltage during the transient are plotted in Figure 7.4. It can be seen from the plots, especially from Figures 7.4 (c) and (d), that the overall performance of the decomposition algorithm is improved by increasing N_{res}.



(a) (b)

Figure 7.3 Comparison of transient of the estimated positive sequence between different N_{res}

(a) a.c. value, (b) dq value

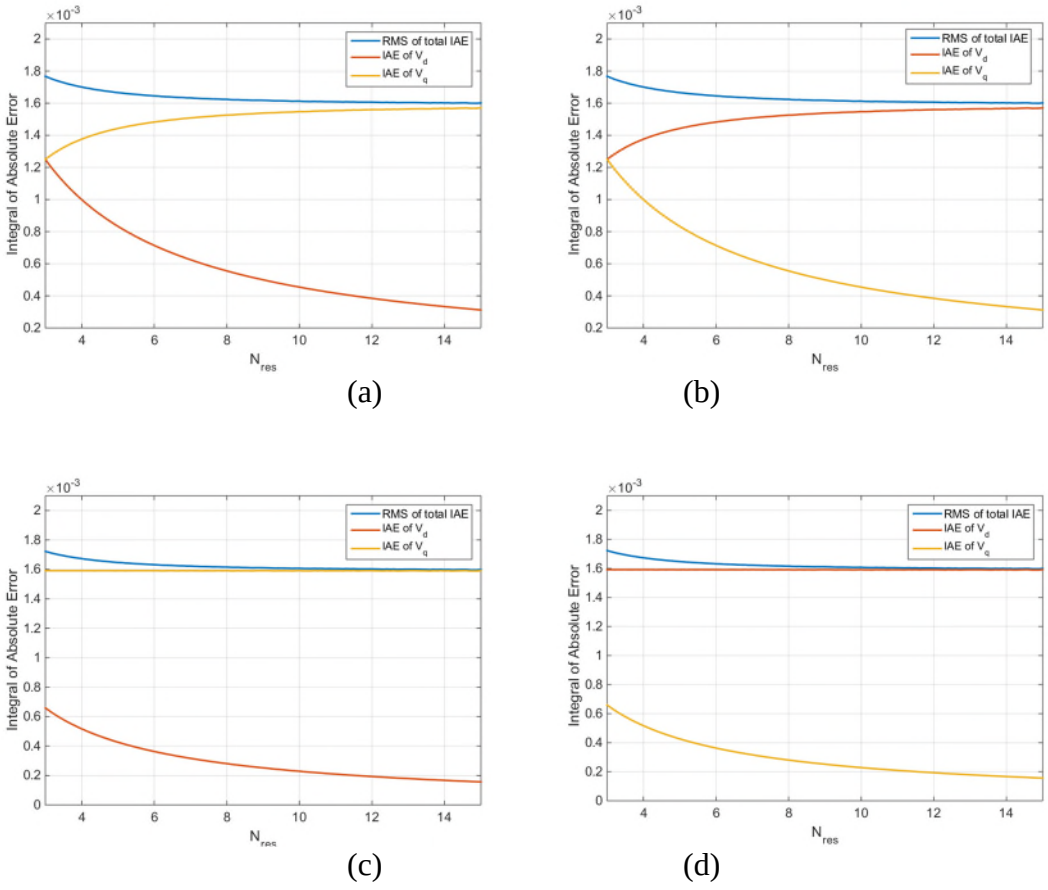
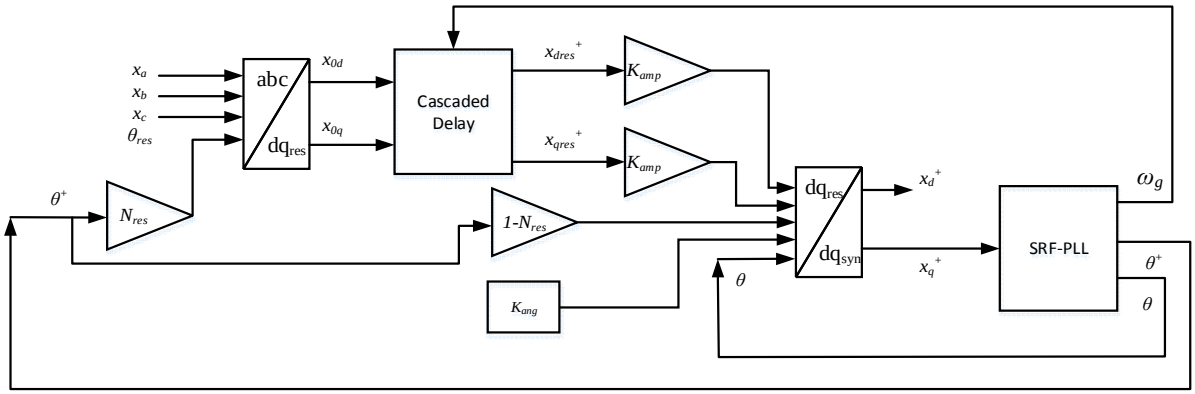


Figure. 7.4 IAE of V_d and V_q during transient caused by 1 p.u. step change of:

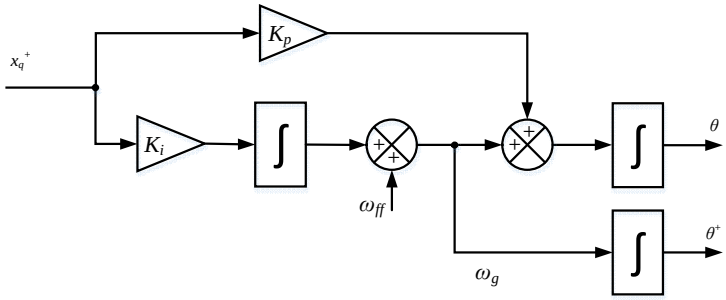
(a) V_d of positive sequence; (b) V_q of positive sequence;

(c) V_d of negative sequence; (d) V_q of negative sequence.

The dynamics of an SRF-PLL system are taken into consideration for further verifying the suitability of the algorithm as part of the PLL system, which is always needed in the downstream (inner loop) control for providing the information for grid synchronisation such as the grid frequency and voltage phase angle. This is shown in Figure 7.5 (a). As shown in Figure 7.5 (b), the information about the grid frequency is acquired from the integral output of the PI controller working as the loop filter in the SRF-PLL. The SRF-PLL is set to track the positive sequence in the simulation.



(a)



(b)

Figure 7.5 (a) Structure of symmetrical component decomposition system with PLL to track positive sequence signal; (b) structure of SRF-PLL

By acquiring V_d and V_q of the positive sequence voltage, the SRF-PLL is sufficiently functional to track the grid voltage. Also, as the PLL system is able to track the frequency of the input signals, the system is frequency-adaptive. Proper tuning of the SRF-PLL should be considered to avoid causing oscillations. Due to the dynamics of the SRF-PLL, a slightly longer transient is expected and shown in Figure 7.6.

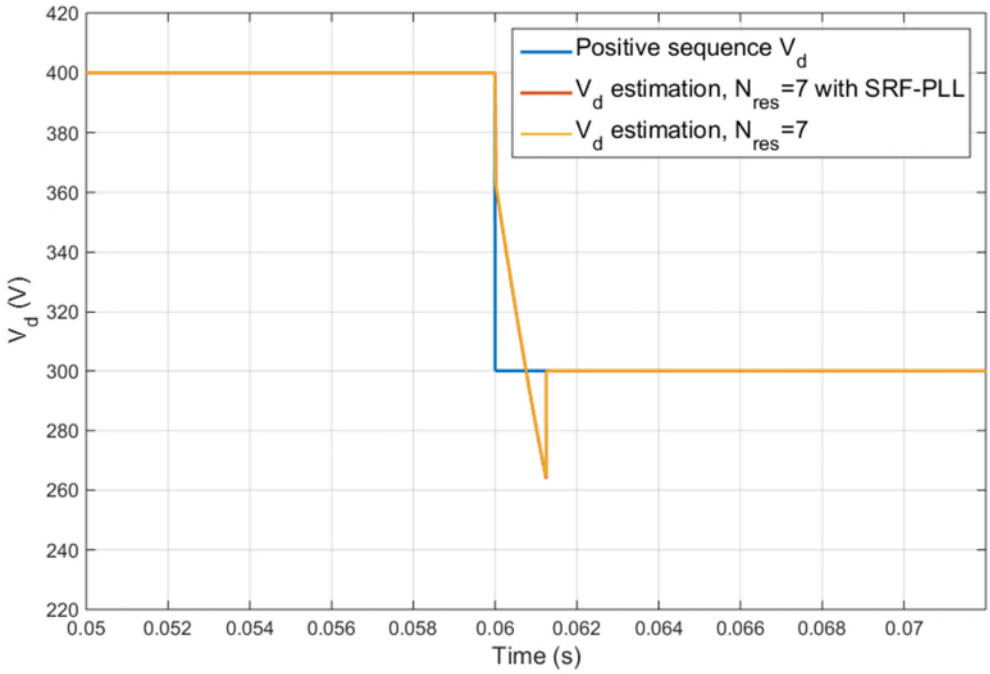


Figure 7.6 Effect of SRF-PLL dynamics on decomposition output

7.2 System initialization and start up

The system initialization is carried out with current hysteresis control discussed in Section 6.1. The simulation study is carried out to verify the current tracking ability and the accuracy of the grid voltage estimation. Also, different a.c. side topology e.g. three-phase three-wire or three-phase four-wire system is simulated to verify the filter design and system response in different environments.

The three-phase four-wire a.c. topology is first used to verify the performance using simulation. The coupling inductance is 10mH. The average switching frequency should not exceed a limit of 10kHz. The sampling frequency is set to be 20kHz which would be the same sampling frequency applied later in the experiments. d.c. voltage is set to be 413V for achieving a modulation depth of 0.8 assuming the a.c. side is a 230V grid system. Guided by the design procedure provided in Section 6.3.2, the small hysteresis band is set to be ±0.2A.

The purpose of deploying the initial start-up procedure is to ride-through the initial current transient prior to synchronising to the grid voltage. The VSI system could be started with phase error between the referenced voltage output and the desired one. The initial start-up procedure should be able to control the current within a safety range of the power modules even if this error is the worst case i.e. 180 degrees. The power should be controlled simultaneously according to an estimated grid voltage. A simulation is carried out to verify the performance of the design especially the accuracy and speed of the grid voltage estimation which is most important to the success of the rest of the control stage.

The parameters of the system under study is listed in Table 7.1:

Parameters	Values
Grid voltage	230V (RMS)
Coupling inductance	10mH
Series resistance	0.1Ω
D.c. link voltage	800V
Hysteresis band	0.2A
Power reference	2000W
Sampling frequency	20kHz

Table 7.1 Parameters of the system under study

The current output waveform and is shown in the figure below. The current ripples are controlled within the designed range to ensure that the harmonic injection is below the limit. The system starts without observable current overshoot. However, a small transient response is found when the PLL system is activated. This is due to the initial angle of the PLL system

being very different from the actual angle of the grid voltage. This effect can be reduced by feed-forward the angle estimated before the PLL system kicks in. The initial grid frequency is assumed to be 50 Hz at the time point when the system simulation is started. The PLL system is activated to adjust the feed-forward term of the grid frequency. It is worth mentioning that the PLL system here is not activated for power control purpose as during the start-up, the desired output power is guaranteed by the current reference generated using calculation matrix derived from the instantaneous power theory. But if the grid frequency varies, the *dq* components of the grid voltage become sinusoidal. This would introduce error to the voltage estimation because of insufficient bandwidth of the PI controller involved in the algorithm. In this case, the PLL system becomes necessary. It can be seen in the simulation result that the current reference I_{dref} is negative due to the phase error being 180 degrees. After the activation of the PLL, the d-axis is aligned with the estimated grid voltage. The current reference becomes grid voltage oriented thus it jumps from negative to positive value. It is also essential to synchronise the PLL system during the start-up process to minimise the transient response when the current control mode is switched to *dq* decoupled current control.

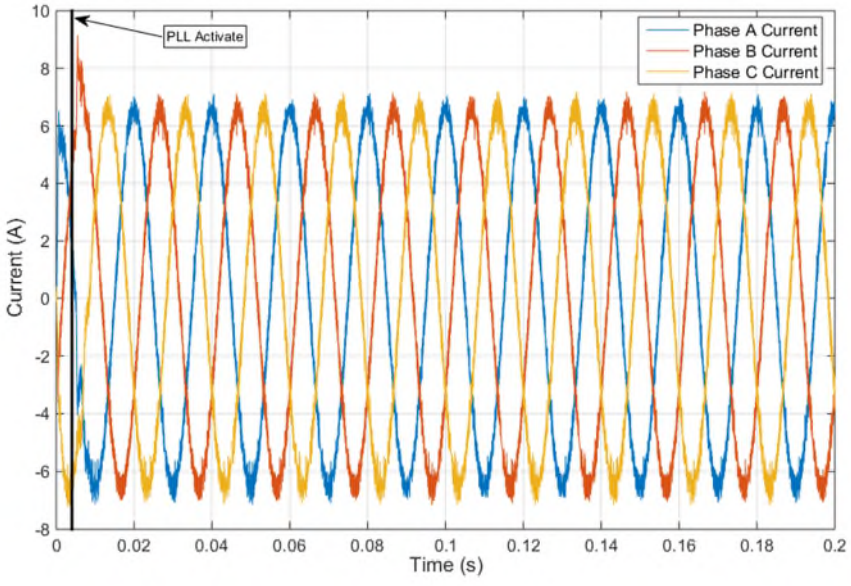


Figure 7.7 Current waveform during the initial start-up process.

To evaluate the impact brought to the system when activating the SRF-PLL system, an extended analysis is provided here from d.c. bus capacitor voltage point of view. The mismatch of the input and output energy across the d.c. capacitor will be the error between the output power and its reference, which is generated according to the input power, integrated by time. This energy variation is calculated to be approximately 8.7J (the accuracy is affected by the switching harmonics and definition of the steady state) causing the d.c. bus voltage variation of 3.2V if using the value of the capacitance of the experimental test rig. The impact on the d.c. link capacitor will be very small. As introduced in Section 6.2, the a.c. side power output needs to be controlled to balance the power generated from the generator side prior to synchronisation to the grid as one of the important control objectives during the initial start-up of the a.c. voltage-sensor-less system. The simulation results proved that this design objective is well satisfied as shown in Figure 7.8. As for the current overshoot, it is well below the limit of the IGBT rating and the duration is very short.

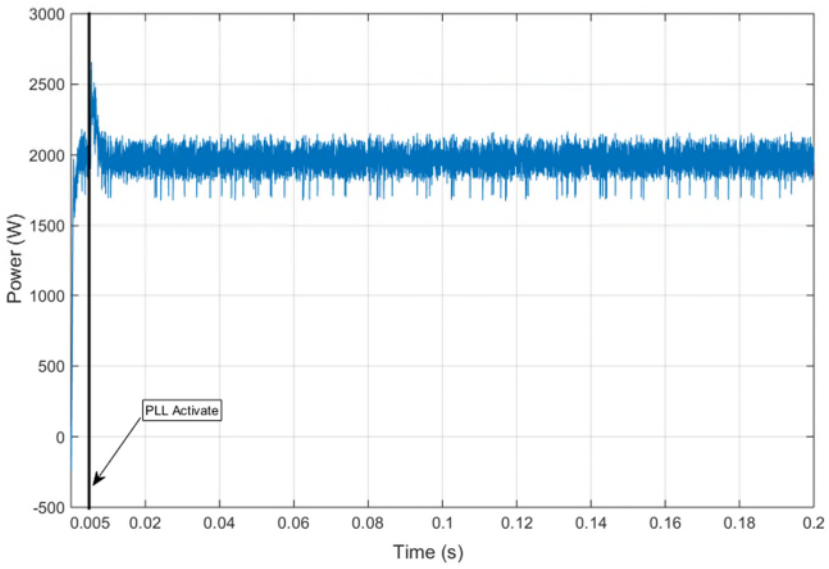


Figure 7.8 Power output during the initial synchronisation process

It can be verified from Figure 7.9, that with estimated voltage shown in Figure 7.10, the current reference can be generated to achieve unity power factor in less than a quarter of a fundamental

cycle and the reference output power can be reached. The effectiveness of the low-passing characteristic of the grid voltage estimation is obvious in Figure 7.11. The estimated grid voltage waveform is almost ripple free and exactly matches the actual grid voltage. This ensures the quality of the control especially when the current control mode is switched from hysteresis current control to *dq* decoupled current control as the error of the feed-forward grid voltage is not desirable.

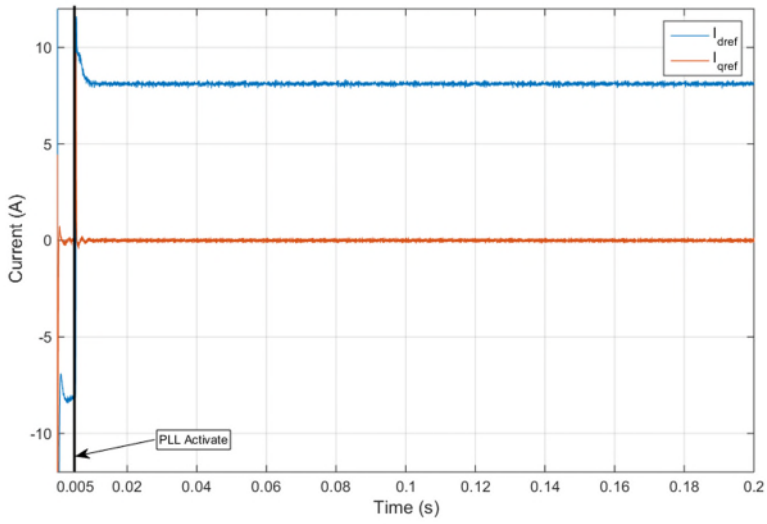


Figure 7.9 Current reference during the initial start-up

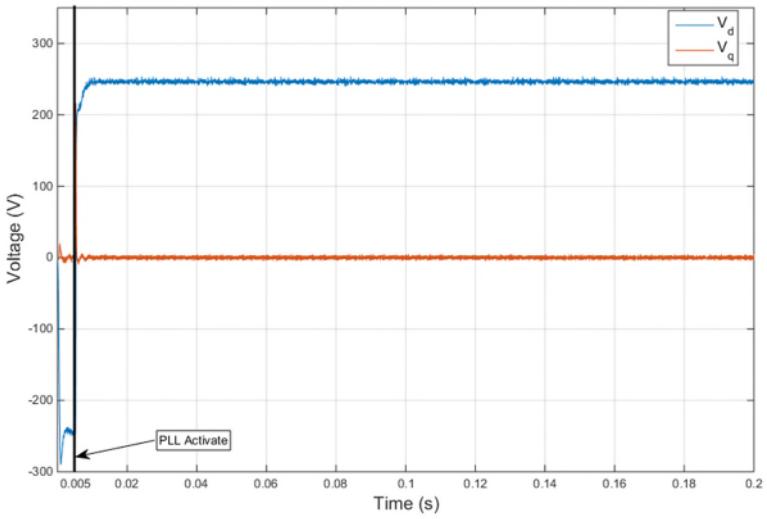


Figure 7.10 The estimated voltage *dq* components

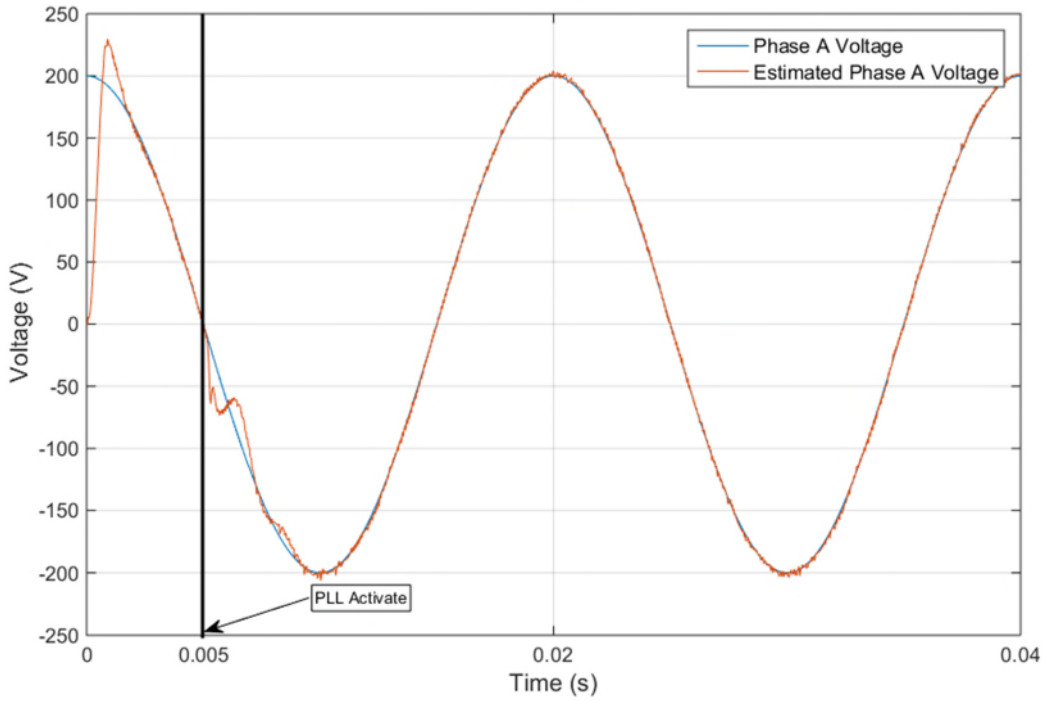
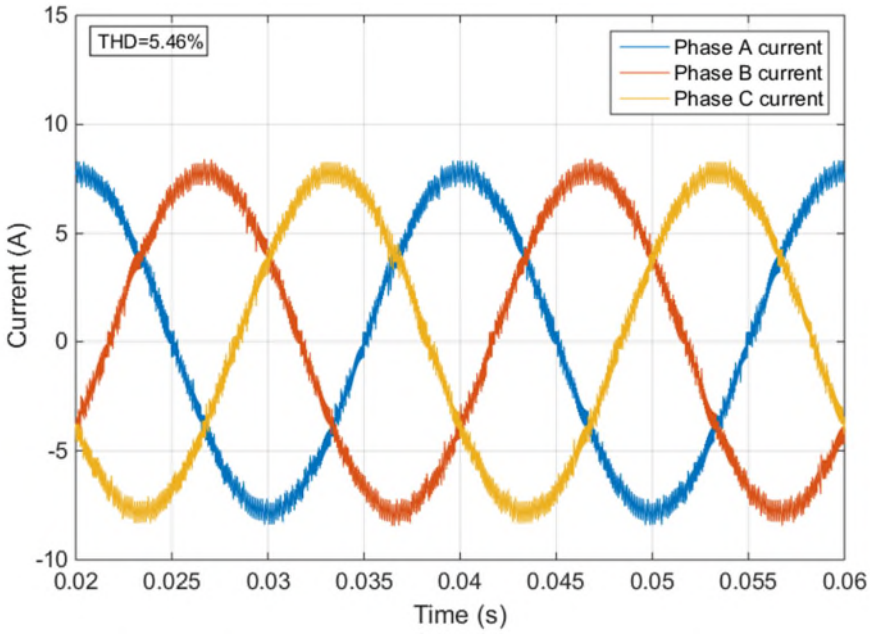
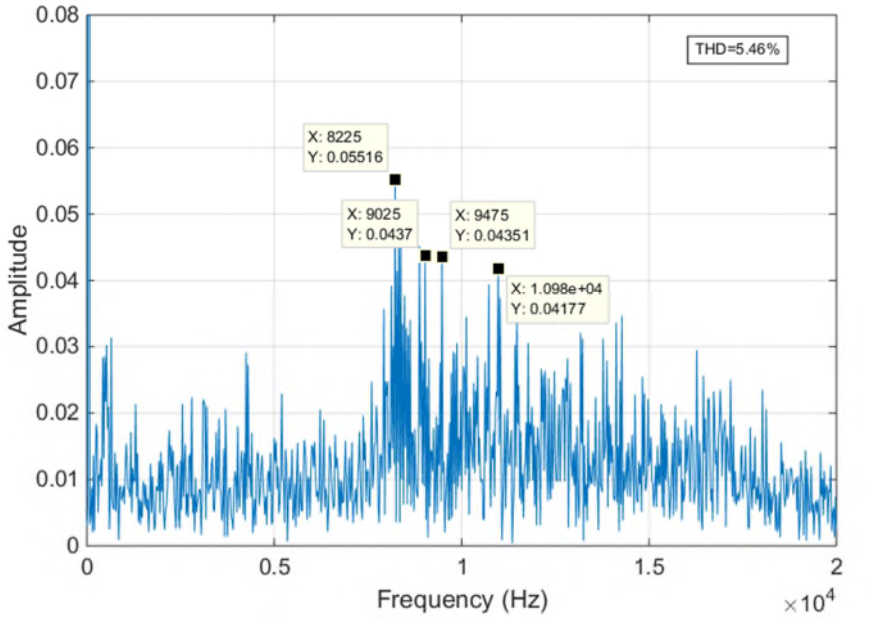


Figure 7.11 The estimated grid voltage waveform

An FFT is carried out using Matlab to verify the actual switching frequency during the hysteresis control, as shown in Figure 7.12. The spectrum shows that the highest peaks are located around 9kHz which indicates the possible average switching frequency. This proves that the hysteresis-band is well designed to regulate the switching frequency within the permitted range. The THD is also complied with the requirement of the grid code as illustrated in Section 1.3. However, the harmonic content is barely below the permitted range. This is the most important reason why the current control mode needs to be switched from hysteresis current control to the proposed a.c. voltage-sensor-less current control with PWM to generate the gate signals.



(a)

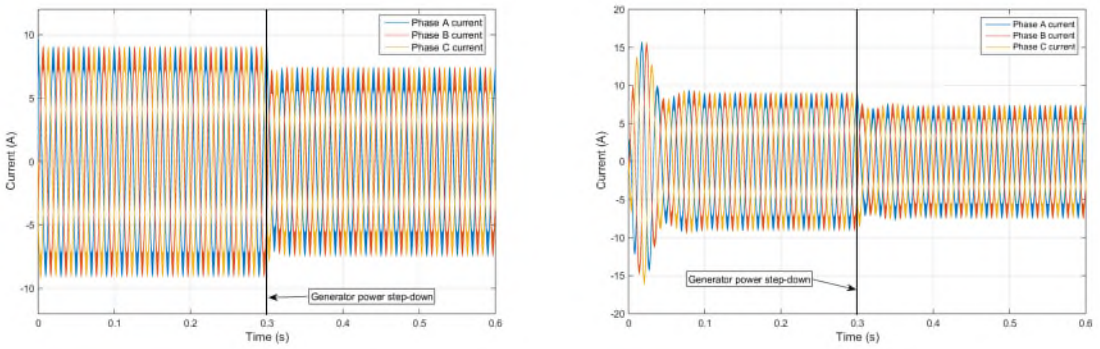


(b)

Figure 7.12 Results of (a) the current waveform and (b) the FFT spectrum

7.3 d.c. bus voltage control simulation

Verified by the simulation results shown above, the response of the active power output is mainly subject to the bandwidth of the controller. As the d.c. bus voltage variation is a result of the energy exchange happened between the d.c. and a.c. side of the VSI, the ability to track the desired active power determines the ability to stabilize the d.c. bus voltage. A simulation study is carried based on the discussion provided in Section 6.2 to provide comparison between the response of the system under same d.c. bus voltage controller but with different current control bandwidth. The results are shown in Figures 7.13 and 7.14.



(a) (b)

Figure 7.13 Current injected when the system starts and the power flowing into the d.c. side steps down with: (a) faster current control; (b) slower current control

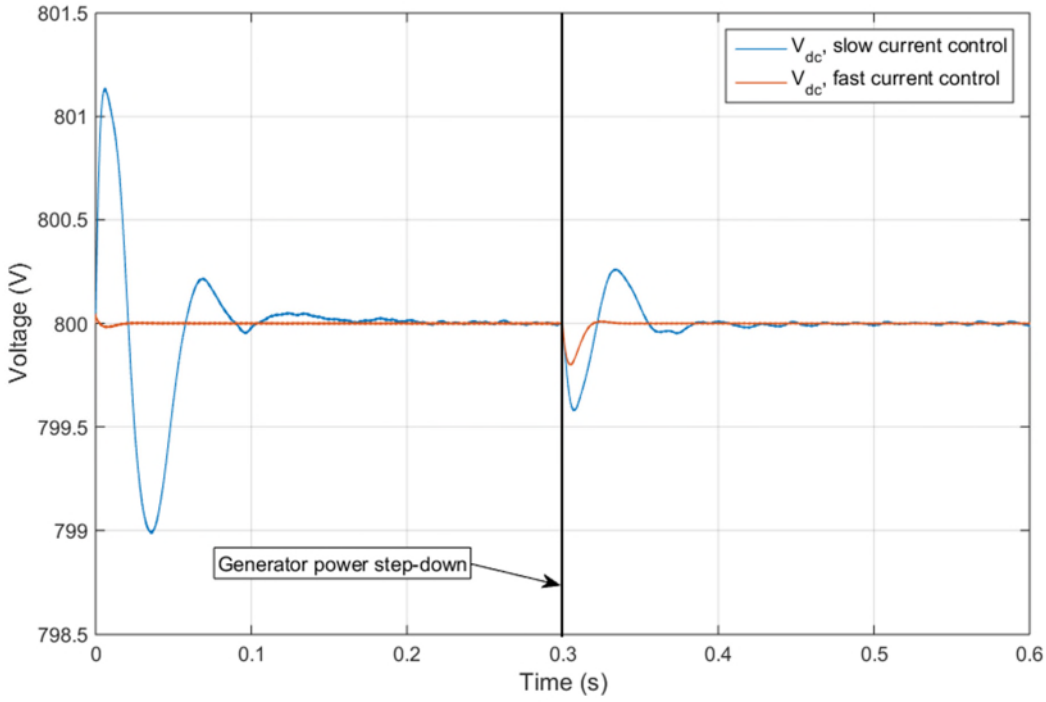


Figure 7.14 The d.c. bus voltage response

7.4 Power control behaviour and transient of the a.c. voltage-sensor-less control

The simulation results for the initial grid voltage estimation show that the fixed-band hysteresis current control and the proposed grid voltage estimation system are able to control the current thus the power without ac-side voltage sensors. The advantage of a fast transient response of the hysteresis current control is well presented. However, it also shows a high harmonic content which is approaching the limit of the grid code regulation. Considering it is only going to operate for a few fundamental cycles, this side effect can be accepted but should be improved by using linear current control as introduced in the previous sections.

After acquiring accurate grid voltage via the initialization procedure, the ac-side voltage-sensor-less control under PWM switching scheme can be started safely. The control algorithm

will be tested under balanced grid conditions. But before verifying the final system design, a few situations related to failed initial synchronisation is illustrated to provide comparison.

The initial feed-forward V_d and V_q are set different to the actual grid side to simulate the error of the initial synchronisation. Firstly an error of V_d is made to be 50% of the nominal value while V_q is set to be same as the grid side in order to simulate the case under an mismatch between the amplitudes of the feed-forward and the actual grid voltage. The simulation results are shown in Figures 7.15 and 7.16. Then the case V_d is set to be 86.6% of the actual value while V_q 57.7% of the value of V_d is tested to simulate a correct estimation of the voltage amplitude but 30 degrees of phase error. The power output during the transient stage is also provided in the results shown in Figure 7.17. Finally the case of an accurate initial synchronisation is provided in Figure 7.18. The parameters of the system under study is listed in the table below, Table 7.2.

Parameters	Values
Grid voltage	230V (RMS)
Grid frequency	50Hz
Coupling inductance	10mH
Series resistance	0.1Ω
Target modulation depth	0.8
D.c. link voltage	800V
Power reference	3000W
Switching Frequency	10kHz

Table 7.2 Parameters of the system under study

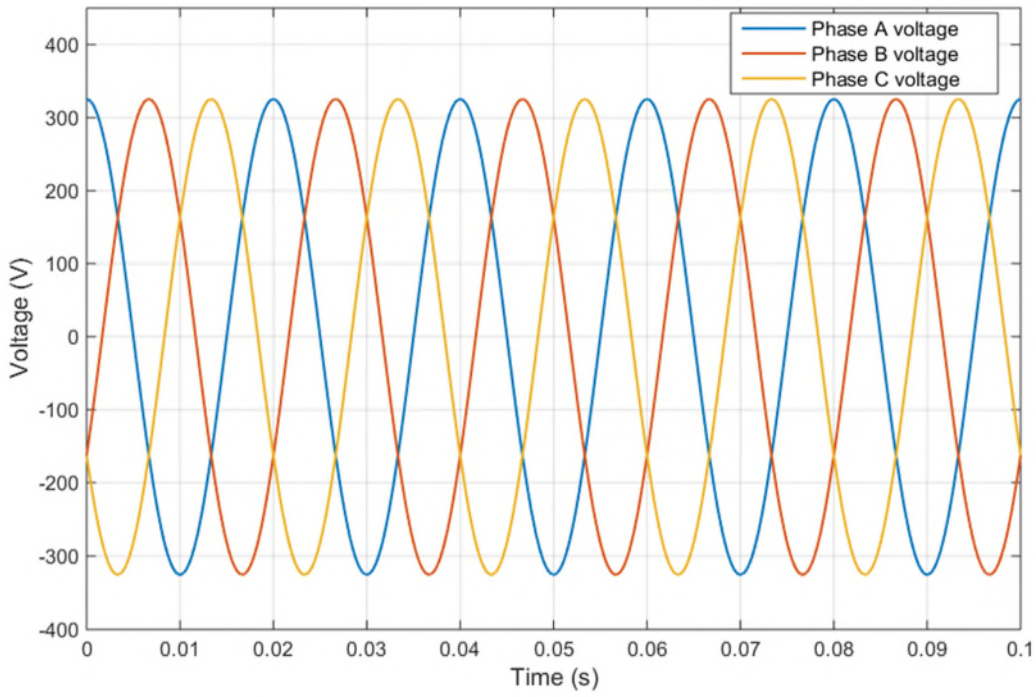
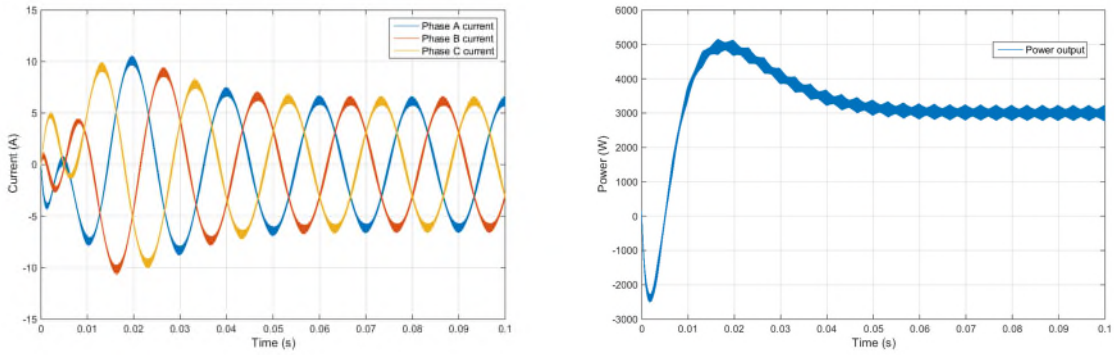
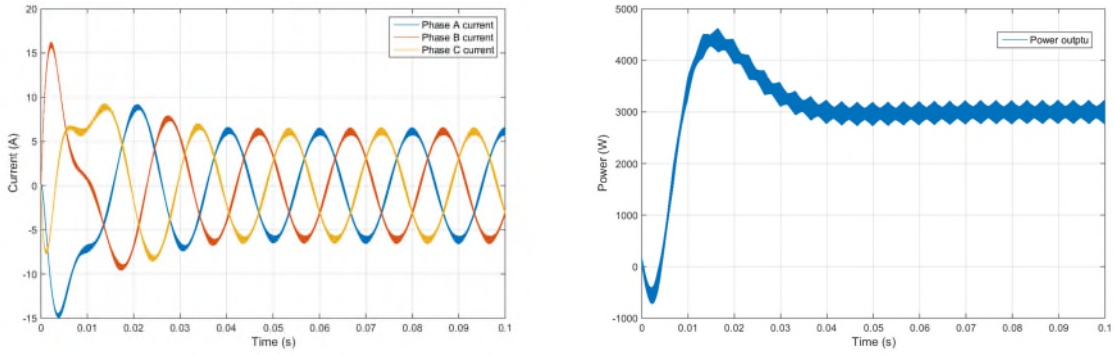


Figure 7.15 Waveform of the grid voltage



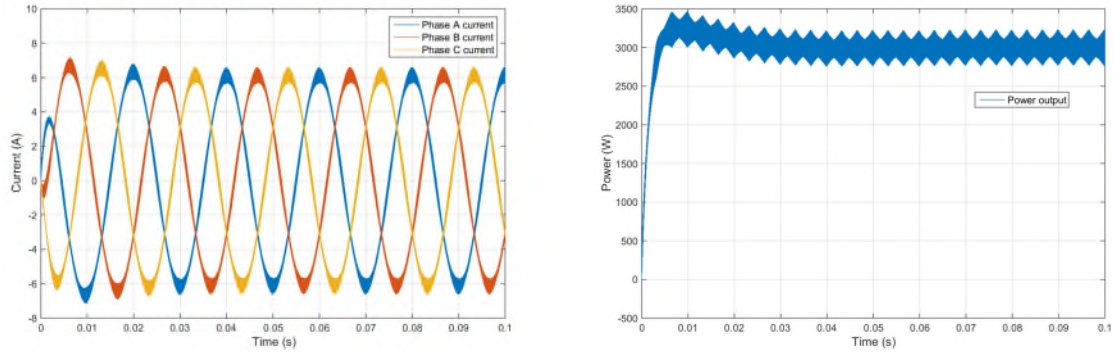
(a) (b)

Figure 7.16 Initial current (a) and power (b) transient response of the a.c. voltage-sensor-less current control with 50% of grid voltage amplitude feed-forward error



(a) (b)

Figure 7.17 Initial current (a) and power (b) transient response of the a.c. voltage-sensor-less current control with 30 degree of grid voltage phase angle feed-forward error



(a) (b)

Figure 7.18 Initial current (a) and power (b) transient response of the a.c. voltage-sensor-less current control with accurate feed-forward grid voltage

It can be verified that the system could reach steady state without very accurate initial synchronisation to the grid. However, the simulation results shown in Figure 7.16 and Figure 7.17 have a significant current overshoot during the first few cycles. The power modules are at a risk of being damaged by this high current. As a consequence, the power output has yielded large transient error during the start up. The power during the transient stage undergoes some reverse power flow which is not desirable at the first point. The d.c. bus voltage will be affected and at the risk of being over charged. Then the over-shoot of the power above the power reference may be too high that it could cause the d.c. bus voltage to drop below the minimum

required value if the output power is not regulated by the d.c. bus voltage control, then the SPWM will be sent into the range of non-linear modulation which means the modulation depth is above 1.0. Low order harmonics in this case will be significant. And the accuracy of the grid voltage estimation will be affected, bringing uncertainty to the stability of the controller. The comparison provided above suggests that initial synchronisation to the grid is important for avoiding these situations thus very necessary.

In practice, the grid voltage could deviate from its nominal value while the power flowing into the d.c. bus could vary. Therefore, the simulation study should take these situations into consideration. The a.c. side voltage-sensor-less control is further tested for its power tracking ability and voltage tracking ability.

A balanced voltage dip of the a.c. side is introduced to test the algorithm. In reality a voltage dip below 70% will allow the connected generation to quit in 1.25 seconds according to Figure 1.6. Therefore it is important to know if the controller could reach steady state within the required remaining connection time range otherwise it could be meaningless to control the power as the error will not be cleared effectively. In the simulation study a 50% voltage dip is provided so that the availability of the control scheme under smaller voltage dip can be verified.

In the following simulation results, a balanced grid voltage dip of 50% of its nominal value is applied at t=0.1 second after the control is active. In Figure 7.19, the voltage waveform is provided. The response of the basic a.c. voltage-sensor-less control system is shown in Figure 7.20. It is clear that the controller is well capable of tracking such a variation of the grid voltage as shown in Figure 7.21. In this case, the current reference generated based on the estimated voltage therefore is able to represent the desired power output. The current response is well damped and swift enough to track the desired power output. The current overshoot visible in Figure 7.20 is caused by the current control error due to the feed-forward voltage discussed in

Section 5.2.5, a similar case to the current overshoot of a current system equipped with voltage sensors and a slow PLL under the same grid conditions. The size of error is determined by the parameter design of the voltage estimation stage together with dynamic decoupling stage. As the voltage estimation stage naturally has a wider bandwidth than the current control stage while the dynamic decoupling is aiming at restricting the high frequency components in the estimated voltage signals, the grid voltage tracking ability thus the power tracking ability is mainly restricted by the dynamic decoupling. However it is small enough to be neglected.

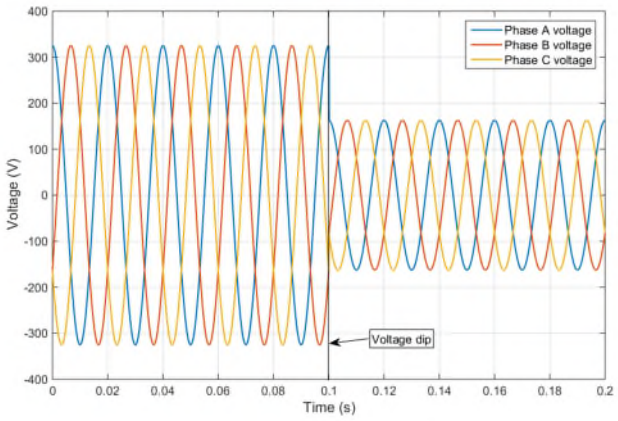
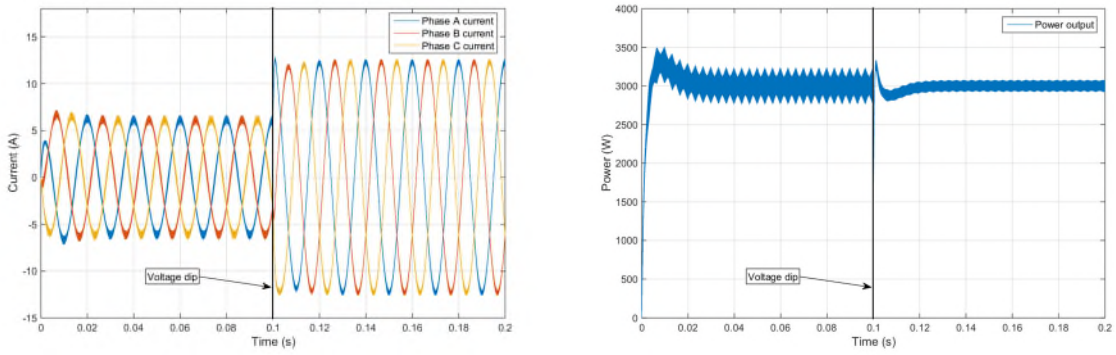


Figure 7.19 Waveform of the grid voltage



(a) (b)

Figure 7.20 Current (a) and power (b) response to the a.c. voltage dip

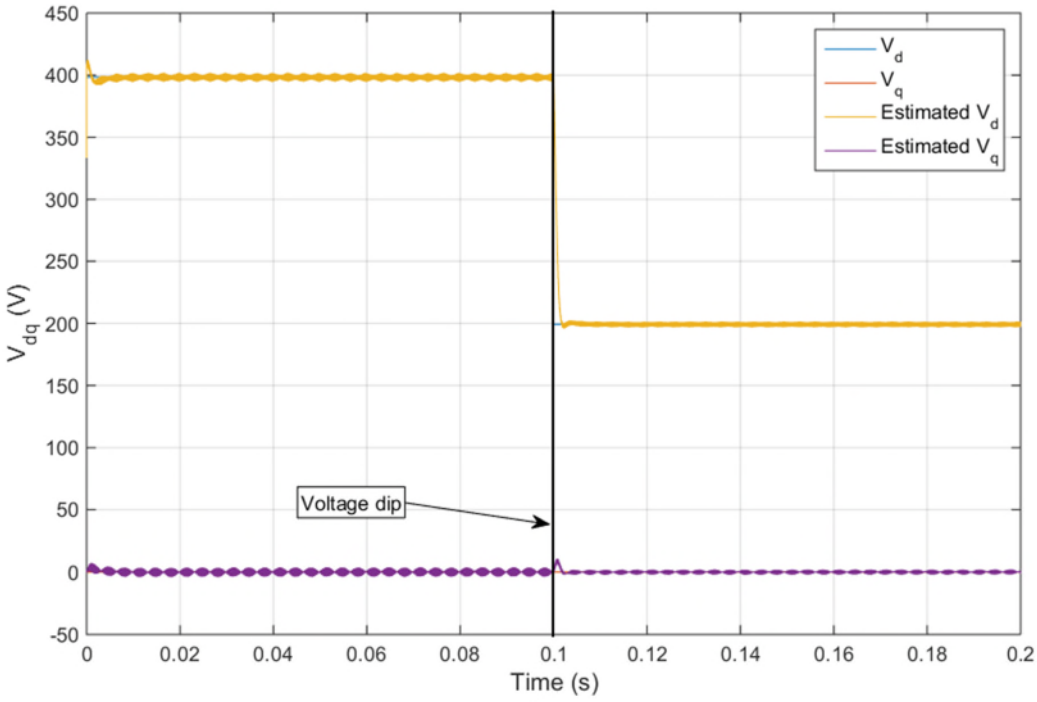
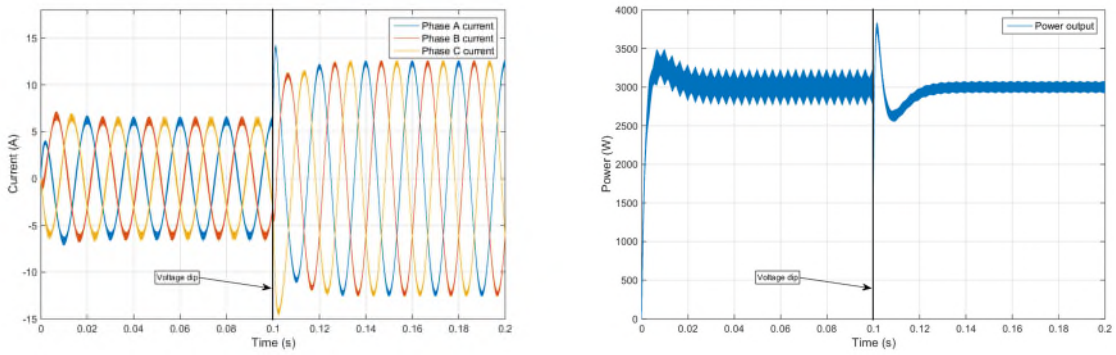


Figure 7.21 Estimated grid voltage V_d and V_q

The system response with slower voltage estimations is shown in Figure 7.22 to provide some comparison. It is obvious that the system response slows down with the decreasing PI coefficients of the dynamic decoupling stage.



(a) (b)

Figure 7.22 Current (a) and power (b) response with a slow grid voltage estimation system

Another situation could bring challenge to the performance of the system is the phase jump of the grid side voltage. In the simulation study, a forward phase jump of 30 degree is applied to the grid voltage at 0.1 second after the system been activated as shown in Figure 7.23. To

isolate the response of the proposed a.c. sensor-less current control from the response of its outer loops, e.g. the d.c. bus voltage control and PLL, the system is simplified without activating these controllers. Therefore this system became a linear system as described in Section 5.4.

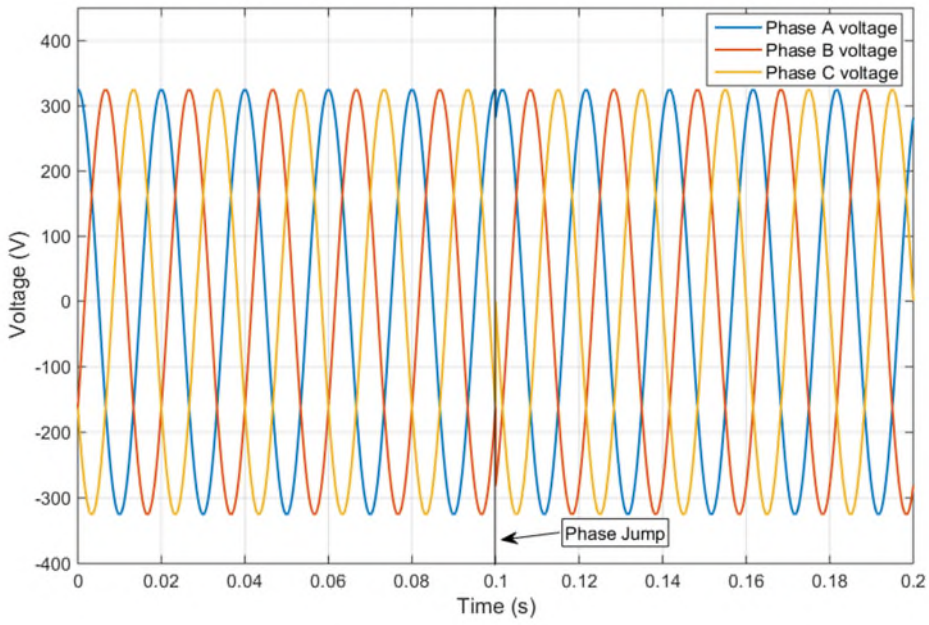
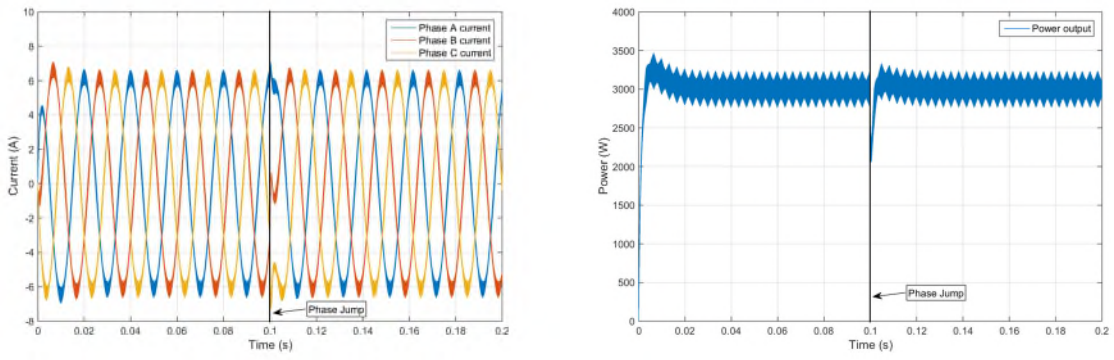


Figure 7.23 Waveform of the grid voltage with 30 degree phase jump

As the current control in this simulation study is not voltage oriented without PLL where the angle of the reference frame of the control system is not locked to the grid angle. To maintain unity power factor, the current should respond to the change of the phase angle of the grid voltage, and its angle should be adjusted accordingly by changing the reference of I_q. The reference for I_d should also be adjusted to maintain the total active power output to be the desired value. The current and power response are shown in Figure 7.24.



(a) (b)

Figure 7.24 Current (a) and power (b) response under 30 degree grid voltage phase jump

The simulation results have now verified the validity of the proposed voltage-sensor-less current control under grid voltage phase jump. The current injected is adjusted according to the estimated grid voltage which is accurately tracking the actual grid voltage. The current response to the voltage phase jump is within a desired range of current values without visible current overshoot. This ensures the safety of the power modules. With accurate estimation of the grid voltage, the power is able to be recover to its reference value. In Figure 7.25, the V_d and V_q are referred to the angle of the angular reference of the system reference frame before the phase jump. It can be verified that the voltage estimation is swift which ensures the smooth current response and the fast power output recovery. The current is in phase with its phase voltage at steady state which is shown in Figure 7.26. These simulation results suggest that without physical inertia, the VSI system is more capable of dealing with phase jump of the mains voltage compared to the actual generators.

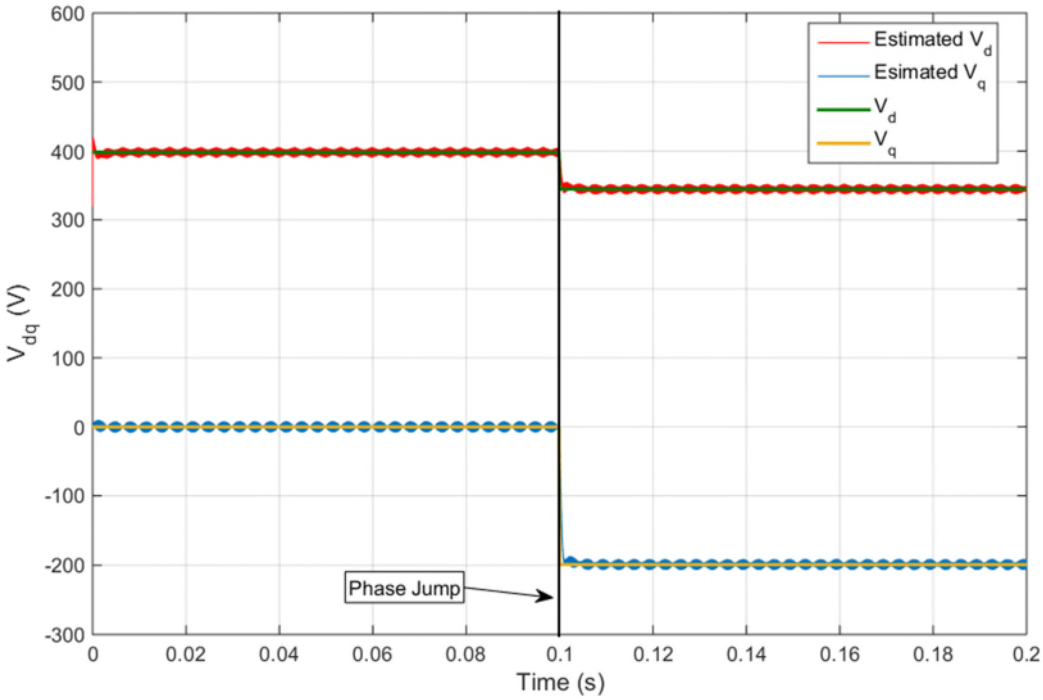


Figure 7.25 Estimated grid *dq* components comparing to the actual values

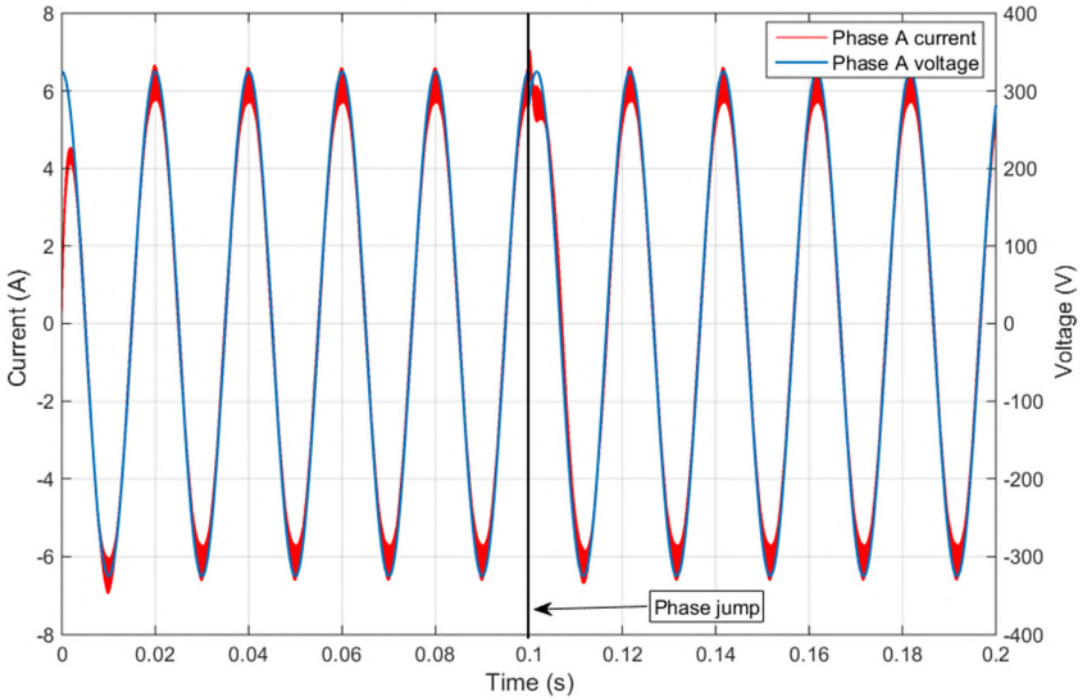
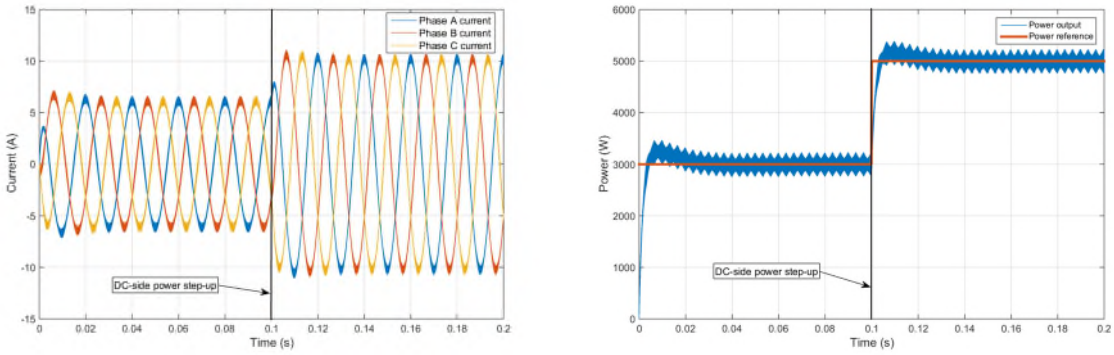


Figure 7.26 Phase A current and the phase voltage before and after phase jump

To test the power tracking ability, a step change of the power reference is applied. The system starts with a reference power output of 3kW. At 0.1 second, the output power reference rises

to 5kW. The current response and the real power at the PCC is recorded and plotted as shown in Figure 7.27.

Two points should be verified by this simulation study. Firstly, is the stability of the system guaranteed if the power reference which determines the working point of the system step-changes? Secondly, is the system able to track the changed power reference in a reasonable amount of time? Thirdly, will error be introduced to the grid voltage estimation if the current injected which is the input to the grid voltage estimation system changes while the grid voltage remain the same?



(a) (b)

Figure 7.27 Current (a) and power (b) response to a reference power step change

The results show that although the grid voltage is estimated based on the output voltage of the VSI and the current response, the wider bandwidth of the grid voltage estimation allows the grid voltage to be tracked accurately without being interfered by the change of the working point of the system. The system performance therefore is subjective to the performance of the current control stage. A settling time of 30ms is approximately achieving which is a good match to the design objective.

7.5 Inverter operation under unbalanced grid voltage

The proposed a.c. side voltage-sensor-less control operating under unbalanced grid voltage is then tested. The effectiveness of the new symmetrical component decomposition method on the current control is evaluated in this section.

The new symmetrical component decomposition method has its advantage in term of faster response. It is proposed to shorten the time spent on generating accurate current reference for power control if it is applied to a conventional current control system during unbalanced grid conditions. This effect is firstly verified. The comparison is made between the proposed symmetrical component decomposition method and other methods in the *dq* reference frame. The parameters of the L filter and other components are listed in Table 7.3:

Parameters	Values
Grid voltage	230V (RMS)
Grid frequency	50Hz
Coupling inductance	10mH
Series resistance	0.1Ω
Target modulation depth	0.8
Power reference	3000W
Switching Frequency	10kHz

Table 7.3 Parameters of system under study

The waveform of the a.c. side voltage is shown in Figure 7.28. The single phase voltage dip is applied and Phase C voltage is dropped to 50% of its nominal value. The control objective is to inject negative sequence current to balanced the power output on three phases. The current response is shown in Figure 7.29 (a). The output power is constant, verified by Figure 7.29 (b).

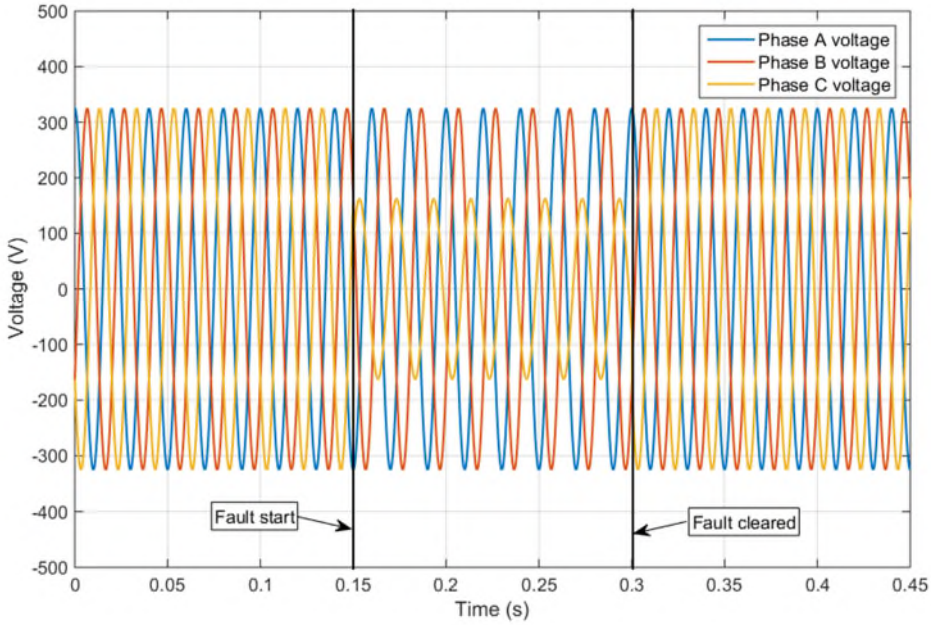
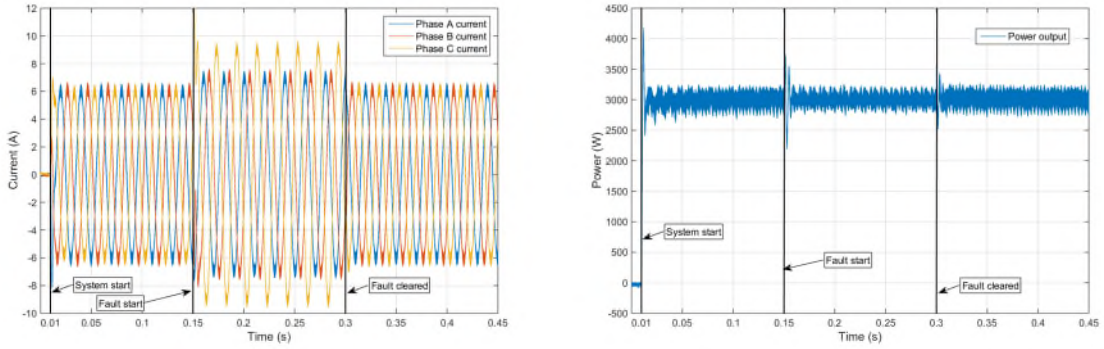


Figure 7.28 Grid voltage with single phase voltage dip

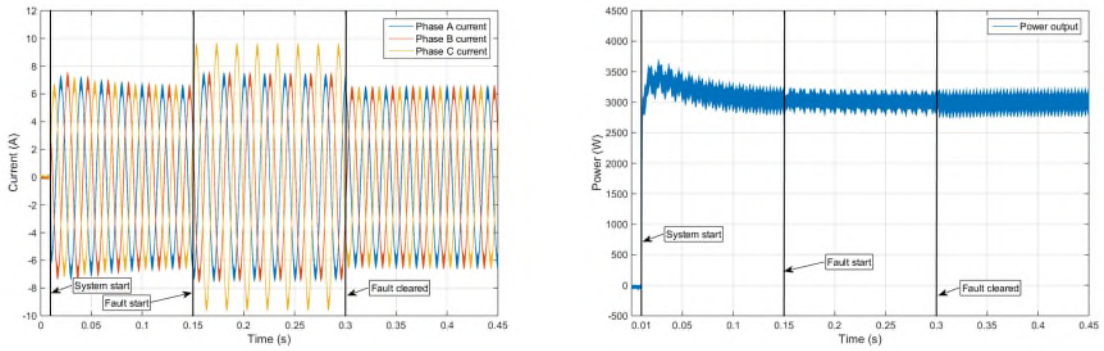


(a) (b)

Figure 7.29 Response of the current control equipped with voltage sensors and using new proposed symmetrical components decomposition method against single phase voltage dip: (a) current waveform; (b) output power at PCC

Another simulation is carried out to provide comparison using conventional notch-filtering method to decompose symmetrical components. Same current control parameters, grid voltage and single phase voltage dip are applied. The current and power response is shown in Figure 7.30. By comparing response shown in Figure 7.29 and Figure 7.30. The symmetrical component decomposition method proposed in this research has little effect on system damping

as the delay introduced in much smaller than the conventional method thus more suitable to be applied to the a.c. voltage-sensor-less control system.



(a) (b)

Figure 7.30 Response of the current control equipped with voltage sensors and using notch filter to decompose symmetrical components against single phase voltage dip:

(a) current waveform; (b) power output at PCC

The simulation of the proposed a.c. voltage-sensor-less control is carried out. The control strategy is first select to be the balanced current strategy. The a.c. side voltage is still the same as shown in Figure 7.28. The three phase current during the voltage dip is shown in Figure 7.31. As introduced in Chapter 4, the current control objective could vary depending on the configuration and roll of the VSI. The constant current strategy aims at a balanced utilization of the power modules on each phase. The negative sequence current is not desired for causing unbalanced current output on different phases. Therefore, the current reference for positive sequence is generated based on the estimated grid-side voltage to keep the desired average power output shown in Figure 7.32 (a), while the current reference for negative sequence is kept 0 regardless what the negative sequence voltage is as shown in Figure 7.32 (b). The power of negative sequence will be absorbed by the d.c. link capacitor. The relevant voltage control therefore is disabled.

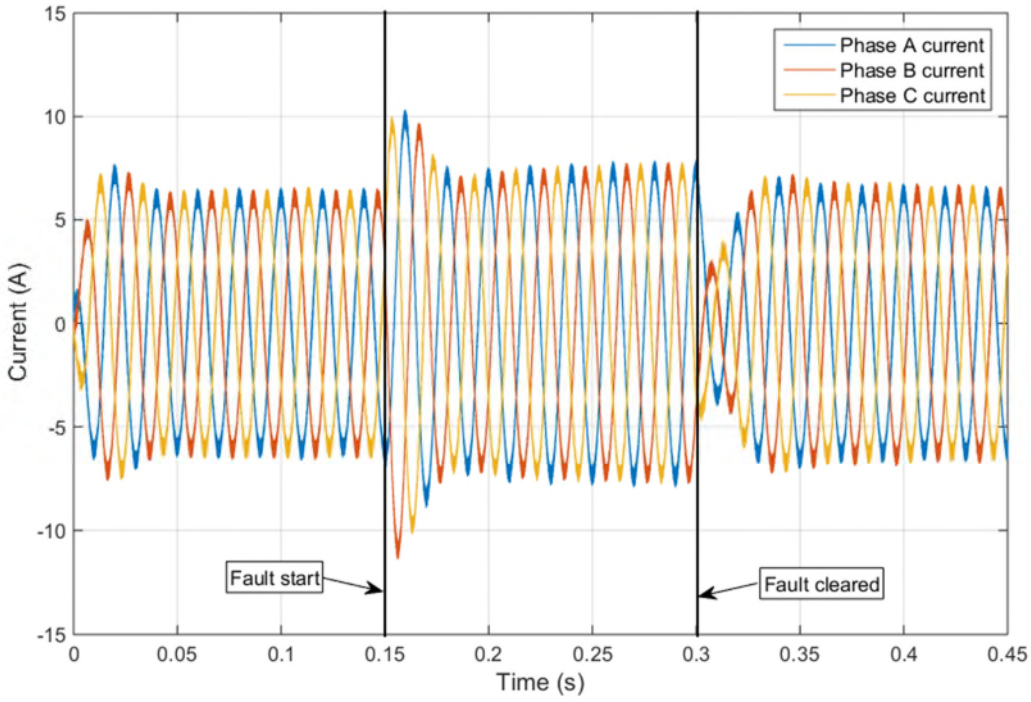
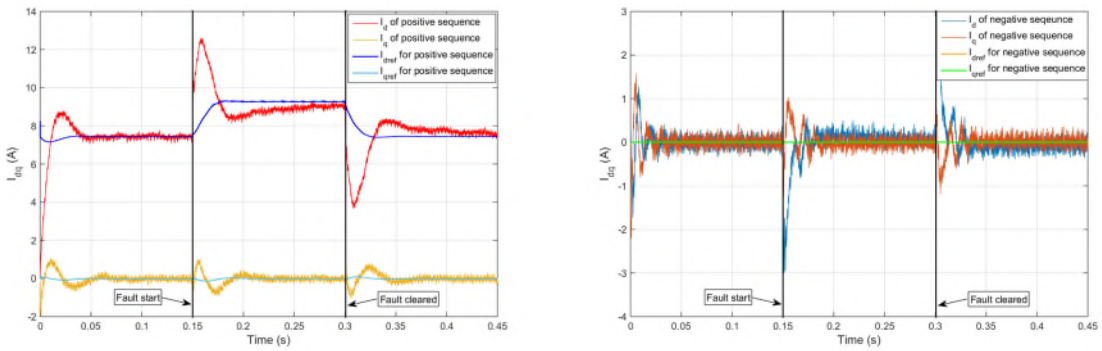


Figure 7.31 Current response to single phase voltage dip aiming at balanced current

The system is assumed to be starting up with accurate initial grid synchronisation achieved. The current response reaches its steady state with in three fundamental cycles after start. It is slower than the simulation result shown in 6.25 due to the band-width of the system is restricted for avoiding interference between controllers of the positive and negative sequence. The current response in term of I_d and I_q shown in Figure 6.32 indicates that the slower response is mainly caused by the reduced bandwidth of the current control stage. The voltage estimation is swift enough to reach steady state within one fundamental period which can be verified by inspecting the curves of the current reference while the actual current takes time to settle. As the current reference for negative sequence is set to zero, the current is still balanced during the single phase voltage dip.



(a) (b)

Figure 7.32 I_d and I_q responding to the single phase voltage dip,

(a) positive sequence; (b) negative sequence

It can be verified from Figure 7.33 that the power of the negative sequence during the unbalanced fault causes a 100Hz oscillation on the output power which will affect the d.c. link voltage. The amplitude of the oscillation is related to the current output of the positive sequence and the voltage of the negative sequence as introduced in Chapter 4. The average power output is kept 3kW as its reference.

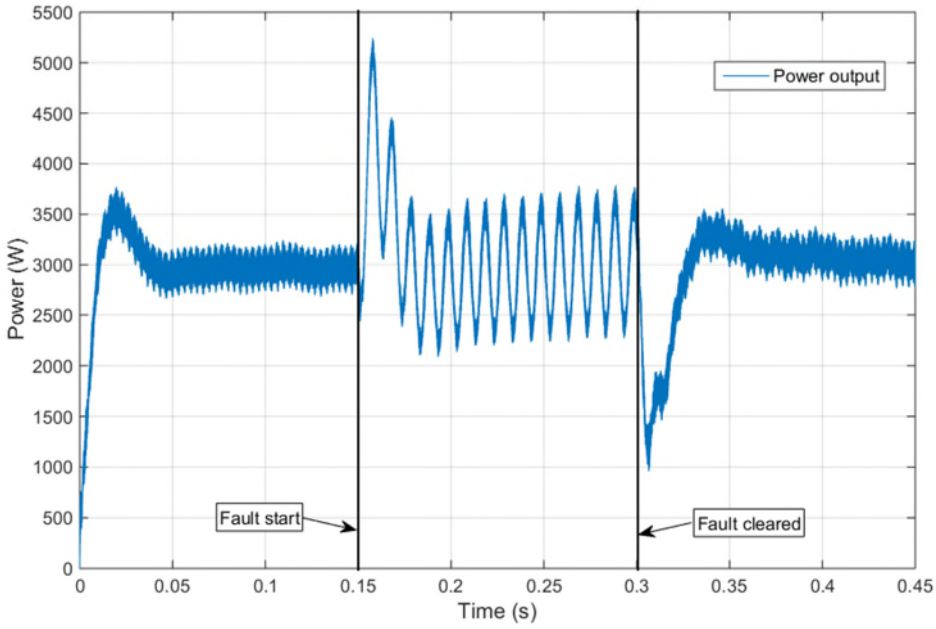


Figure 7.33 Active power output measured at PCC

Another control objective associated with unbalanced grid fault-ride-through is to compensate the active power oscillation by injecting negative sequence current. The current reference can be generated using Equation 4.18 with Q_0, P_{2nd} and Q_{2nd} to be 0. During the single phase voltage dip, the current is also unbalanced. The current references are generated according to the voltage of positive and negative sequence respectively as shown in Figure 7.35. After the fault cleared, the current returns to balance as normal. The three phase current waveform is shown in Figure 7.34. The power output is plotted and shown in Figure 7.36. It can be verified that after a short transient stage of approximate two and half fundamental cycles, the power output is returned to its reference value and constant. The d.c. bus voltage will not be affected active power oscillation in this case.

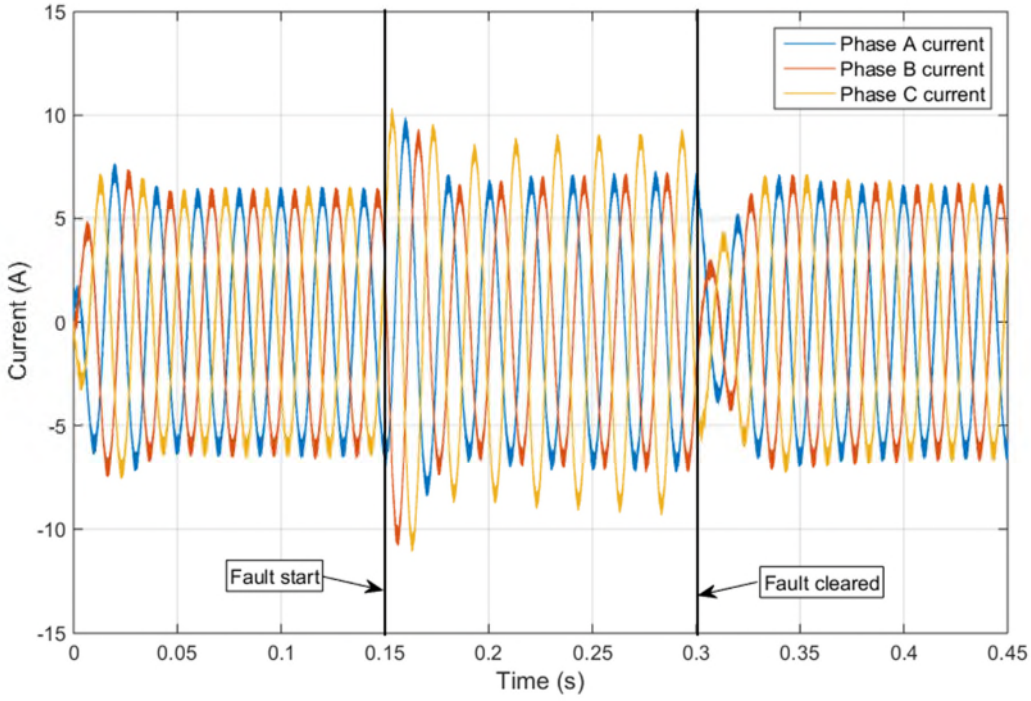
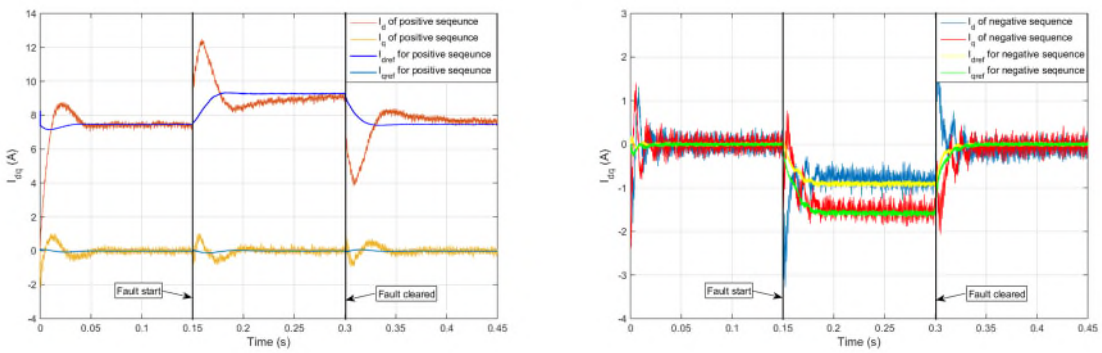


Figure 7.34 Current response to the single phase voltage dip aiming at constant power



(a) (b)

Figure 7.35 I_d and I_q response to the single phase voltage dip,

(a) positive sequence; (b) negative sequence

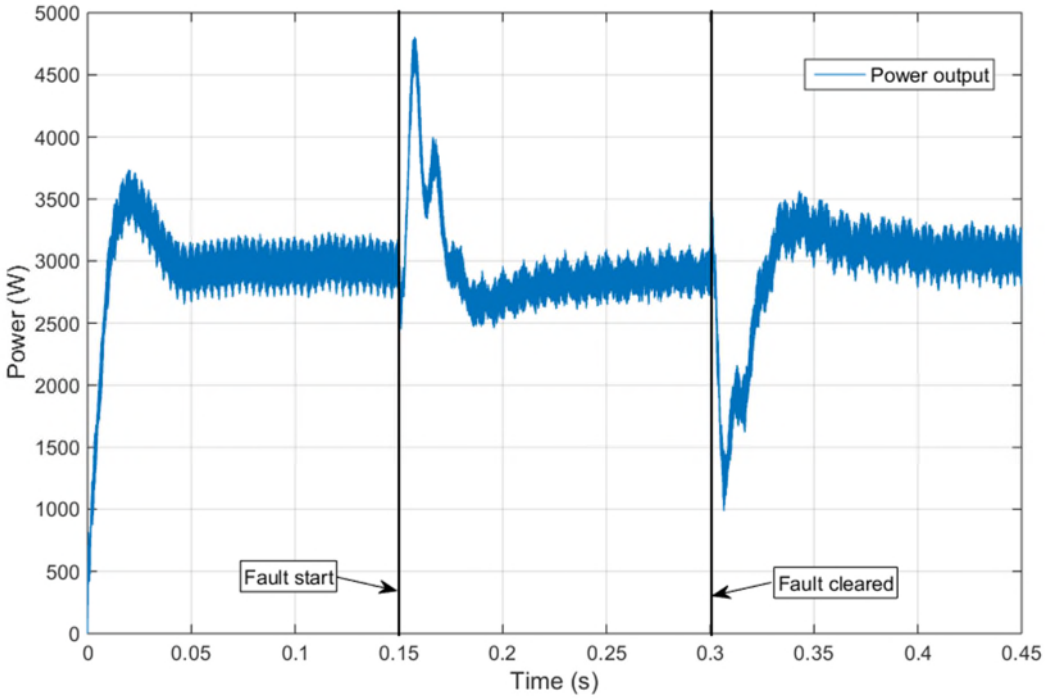


Figure 7.36 Active power measured at PCC

7.6 Chapter summary

This chapter presents simulated case studies to check or verify the proposed control scheme and controller design. The initial start-up and synchronisation to the grid, the steady state operation under balanced grid voltage and the system performance during an unbalanced voltage dip are investigated. The initial start-up process is able to regulate the current injected without synchronisation to the grid. This feature is highly desirable to ensure the safety of the power modules. The transient response of the grid voltage estimation during the start-up process is swift enough to minimise the use of the hysteresis current control and its harmful effect of harmonic injection. The steady-state operation of the a.c. voltage-sensor-less current control with PWM output is proved to be able to track the grid voltage variation while keeping the desired power output in a swift manner. The newly design symmetrical component decomposition algorithm is able to be adopted by the a.c. voltage-sensor-less controller, and plays a vital role in riding-through unbalanced grid fault.

The simulation results has verified the design objective is able to be reached, given the suitable conditions such as sufficient d.c. bus voltage, and well-tuned control parameters. The system can be further verified by experiments.

Chapter 8 Experiment Set-up and Experimental Result Analysis

8.1 Experimental test rig set up

An experimental test rig is built to validate the proposed system design and simulation studies. The performance of the proposed system under unbalanced grid voltage is tested based on different power control objectives and the the newly designed symmetrical component decomposition algorithm in the real application is validated in closed-loop.

A Cinergia GE grid emulator shown in Figure 8.1 is utilized for its four quadrant power control capability. With an isolation transformer, the power can be fed into the GE from the inverter under test.

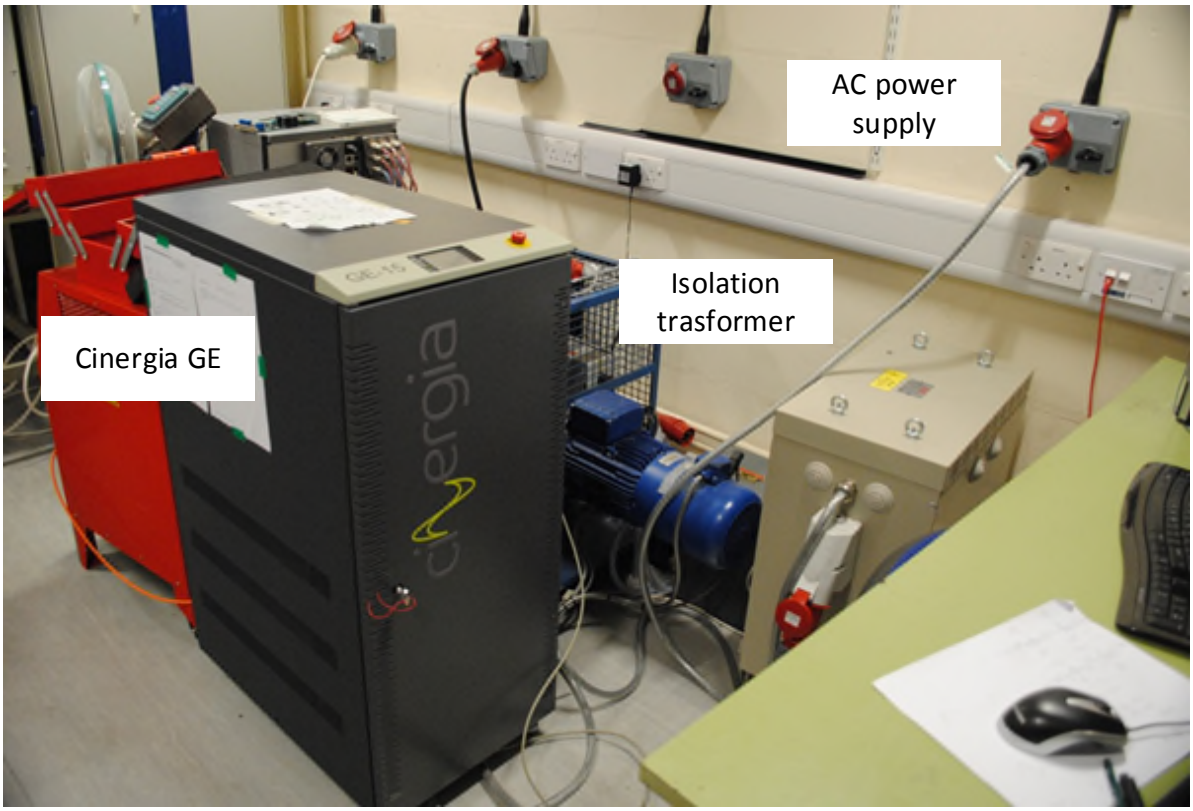


Figure 8.1 A.c. side power voltage source of experiment test rig

The VSI under test is powered from a controllable d.c. voltage source as shown in Figure 8.2 The d.c. voltage is set by this device and due to this reason, the d.c. voltage control discussed in the Chapter 6 is not actually deployed in the experiment.

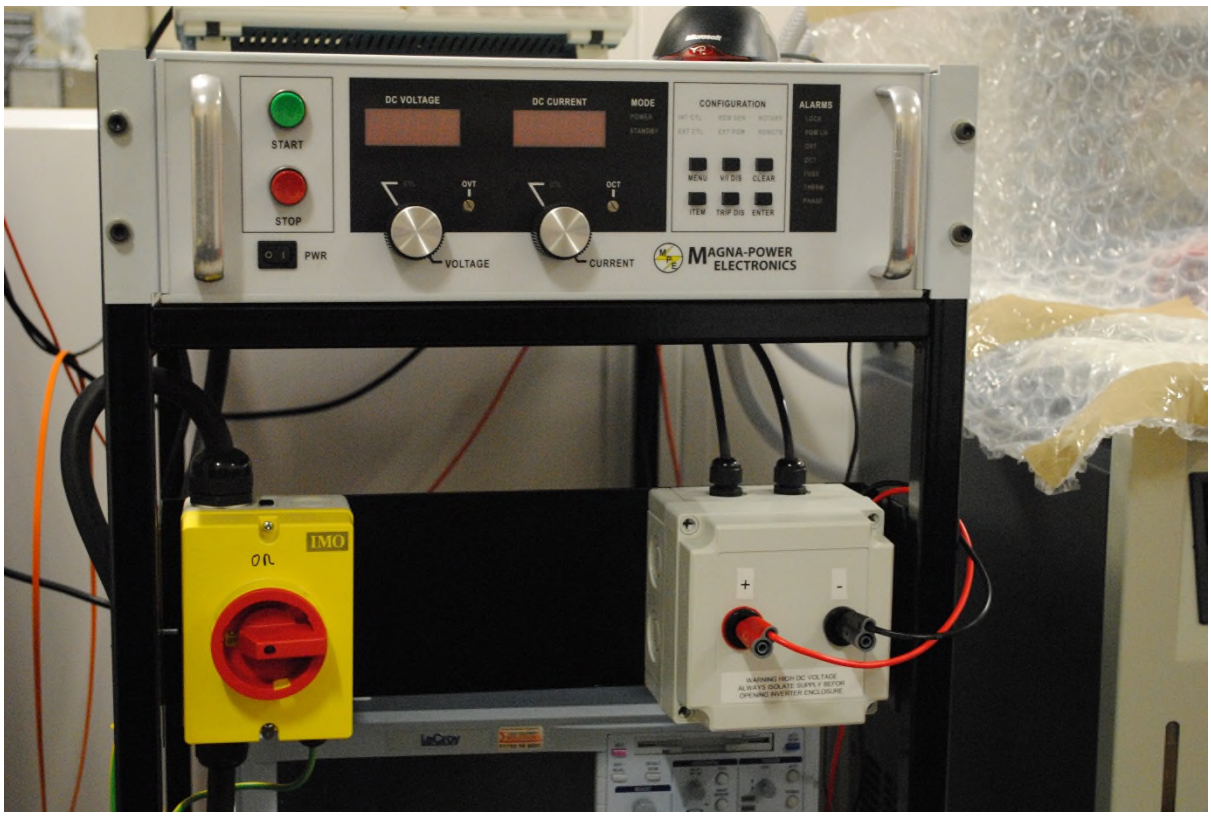


Figure 8.2 D.c. power source

The inverter board shown in Figure 8.3 is contained in a protective casing as shown in Figure 8.4 to isolate the high voltage and power circuit from the outside environment. The filtering inductor and dSpace interface component is also placed in the protective casing as shown in Figure 8.4.

Figure 8.3 Inverter board

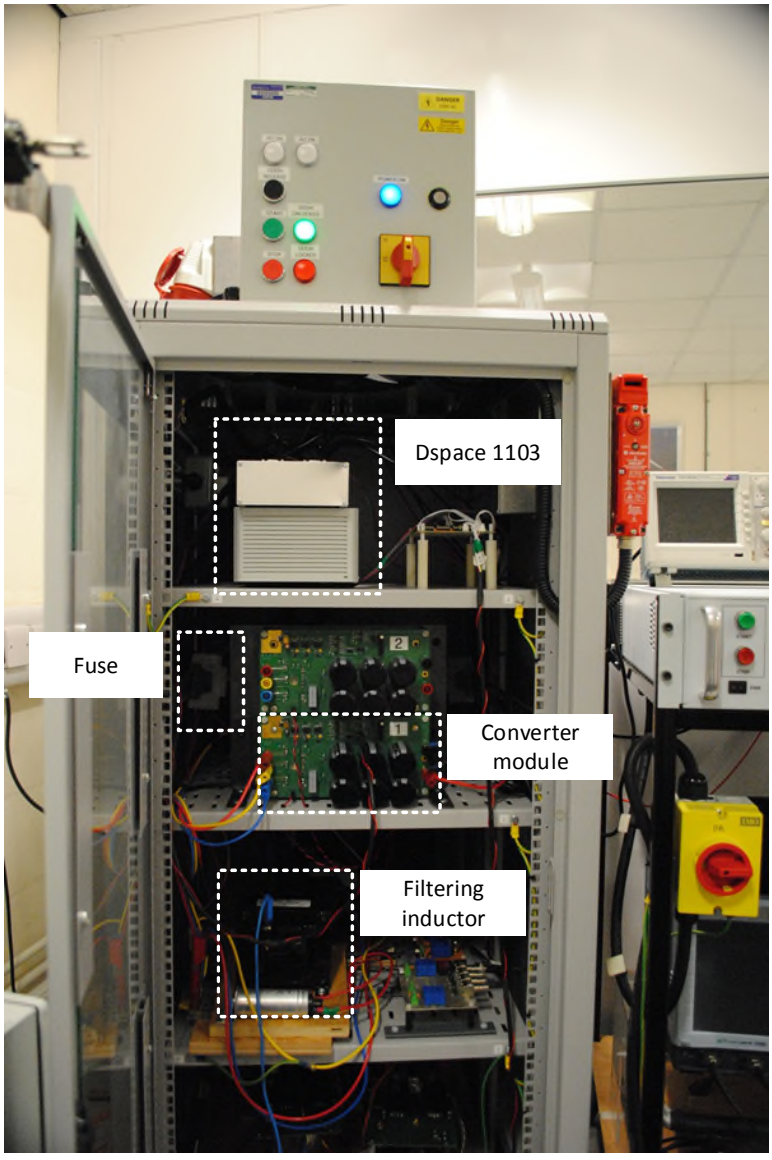


Figure 8.4 Converter Board mounting and casing

8.2 Experiment results

8.2.1 Start-up and initial synchronisation

The capability of the VSI to start-up from zero condition and get synchronised to the grid is first tested and verified. As introduced in Chapter 6, the current control during start-up is carried out by a hysteresis current controller to restrict the current overshoot. The grid voltage should be estimated during this process in order to provide feed-forward signal to the a.c. voltage-sensor-less current control discussed in Chapter 5. The power is controlled during the process to avoid reversed power flow to ensure the safety of the d.c. voltage source. The unity power factor should be achieved, the same as in steady state operation. The relevant experimental results are presented below.

The control starts at a random time point to emulate what is going to happen in reality. Also, the a.c. grid voltage is set to be 49.9Hz but not ideally 50Hz to emulate the case in reality considering a frequency variation. The a.c. voltage contains harmonics as shown in Figure 8.8, which is good for emulating the real environment. The a.c. side voltage is sampled for providing comparison but not used in any of the control stage. As shown in Figures 8.5~8.10, the system starts at time 7.44s. The measured *dq* value of the a.c. side voltage shown in Figure 8.5 is obtained through a *dq* transformation using the output angle of the PLL system. The PLL system has no input to track the phase angle and frequency of the a.c. voltage before the system starts. Therefore the *dq* values of the a.c. voltage are changing over time before the system starts due to the mismatch between the PLL frequency and actual a.c. frequency. After the current control is activated, the grid voltage is estimated based on the output voltage and the current injected. It can be verified from Figure 8.6 that the grid voltage is quickly reaching its true value. The duration of the transient is less than three fundamental cycles which is a good match to the simulation result provided in Section 7.2.

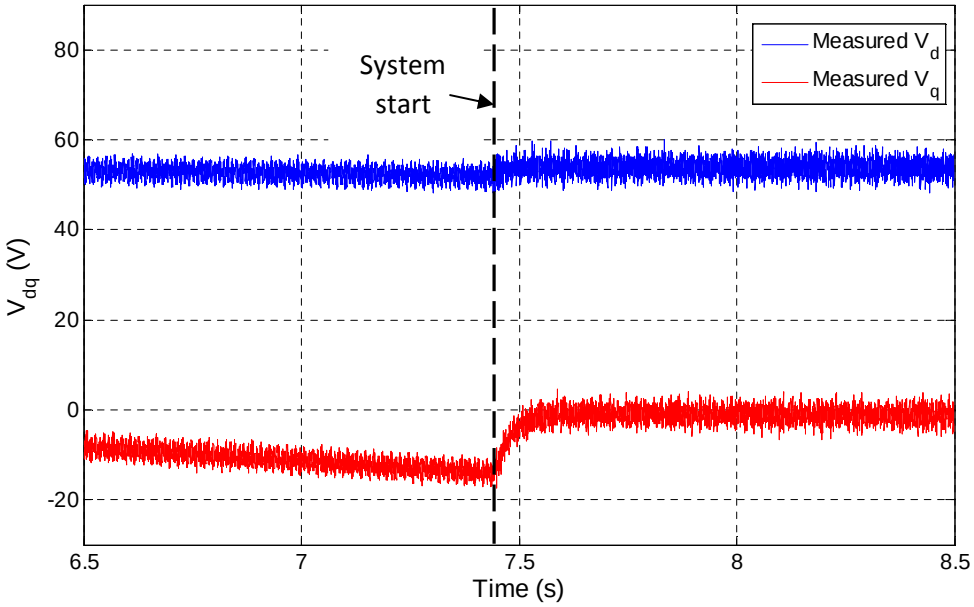


Figure 8.5 Measured grid voltage *dq* components

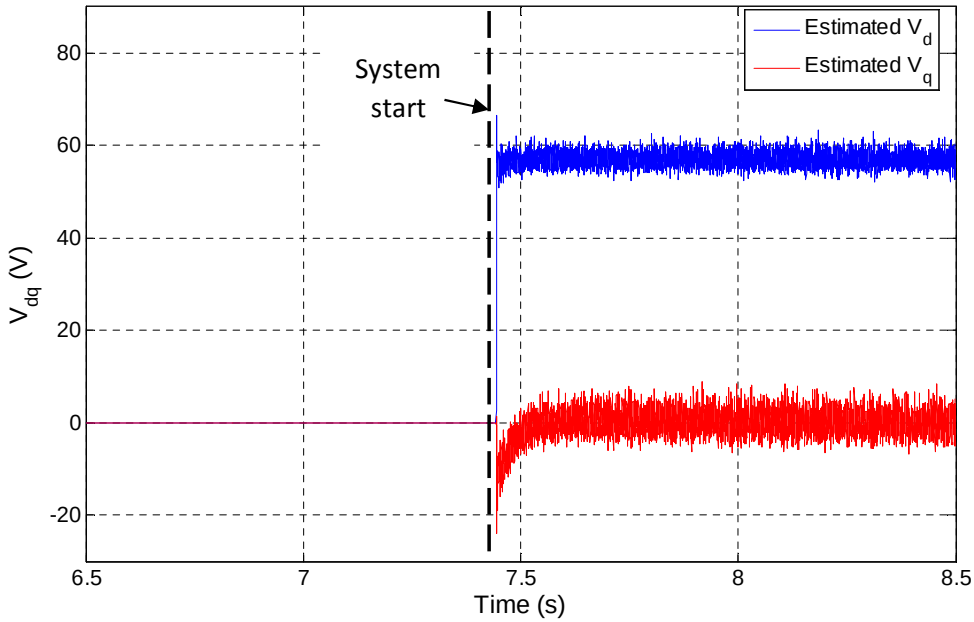


Figure 8.6 Estimated grid voltage *dq* components

As the PLL system will be locking the phase angle of the grid voltage, in the steady state, V_q will be zero and this is shown in Figure 8.5 and Figure 8.6 for both the measured and estimated *dq* values of the a.c. voltage. The accuracy of the voltage estimation is mainly presented by V_d.

A scaled view of the measured and estimated V_d are shown in Figure 8.7 to provide detailed comparison. It is found that the estimated V_d is slightly larger than the real value. This is due to the parameter change of the filter associated with the temperature rise during operation. The error of the estimation is found to be small enough comparing to the value of the signal. It can also be verified from later results that such a small error in the feed-forward signal will not cause big problem. Further, as the power is controlled by I_d whose reference is generated by the desired power and V_d, the error will only causing the output power mismatching the desired power output which should be automatically corrected by the closed-loop d.c. voltage control. Thus this error is accepted.

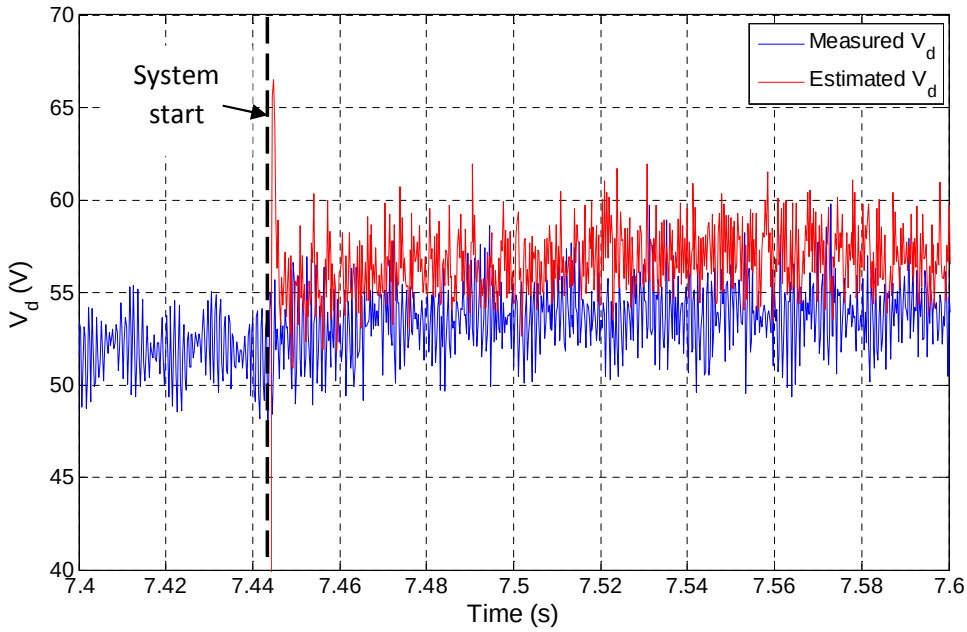


Figure 8.7 Comparison between measured and estimated grid voltage

The current response during the start-up process is shown in Figure 8.9. It can be verified that the current response is smooth without any overshoot, which is desired for protecting the devices from damaging. In Figure 8.10, the phase current and a.c. voltage are plotted together to show that the current is indeed in phase with the voltage, proving that the unity power factor is reached.

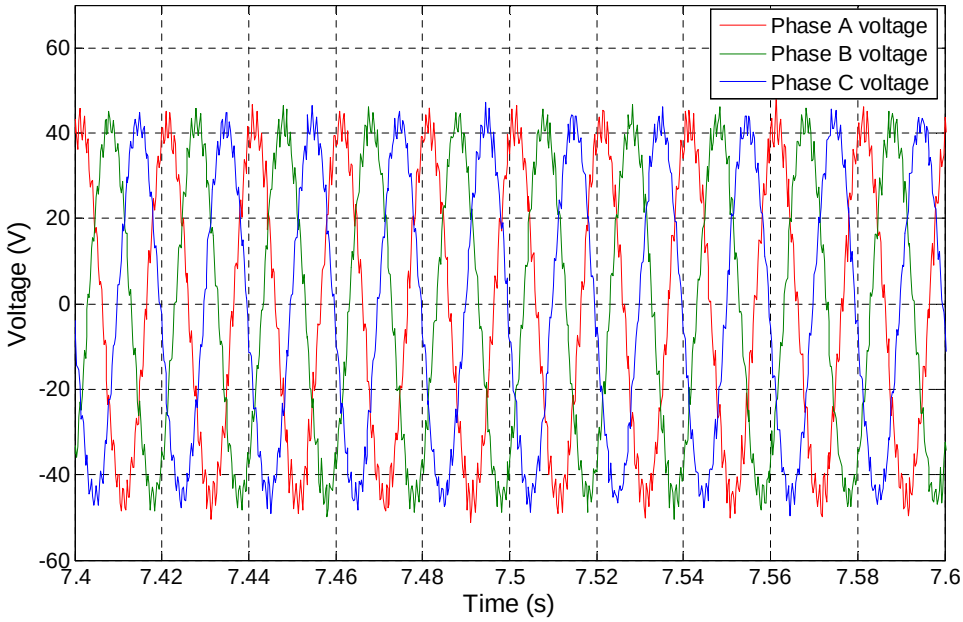


Figure 8.8 Three phase voltage of the grid

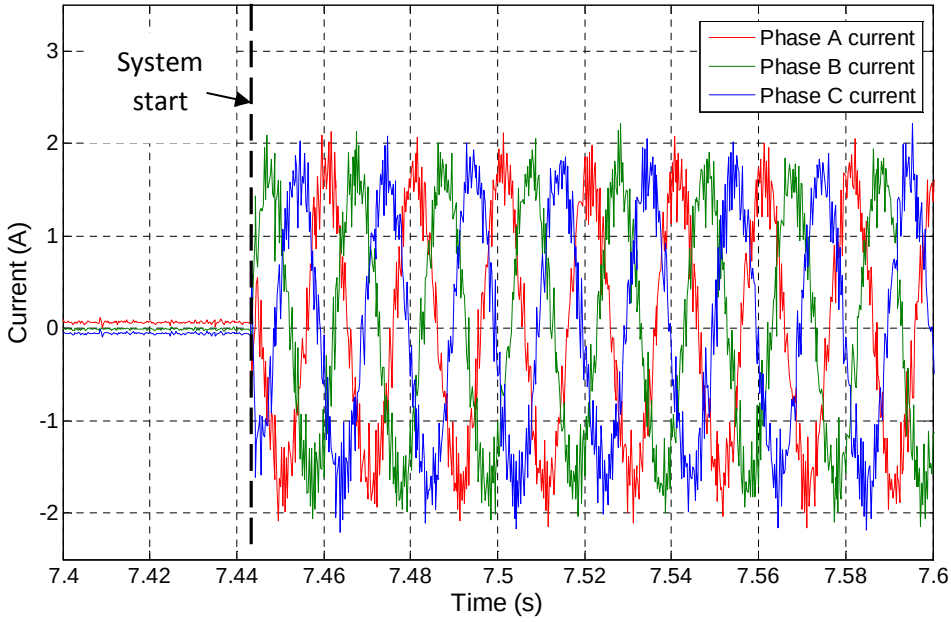


Figure 8.9 Current injected

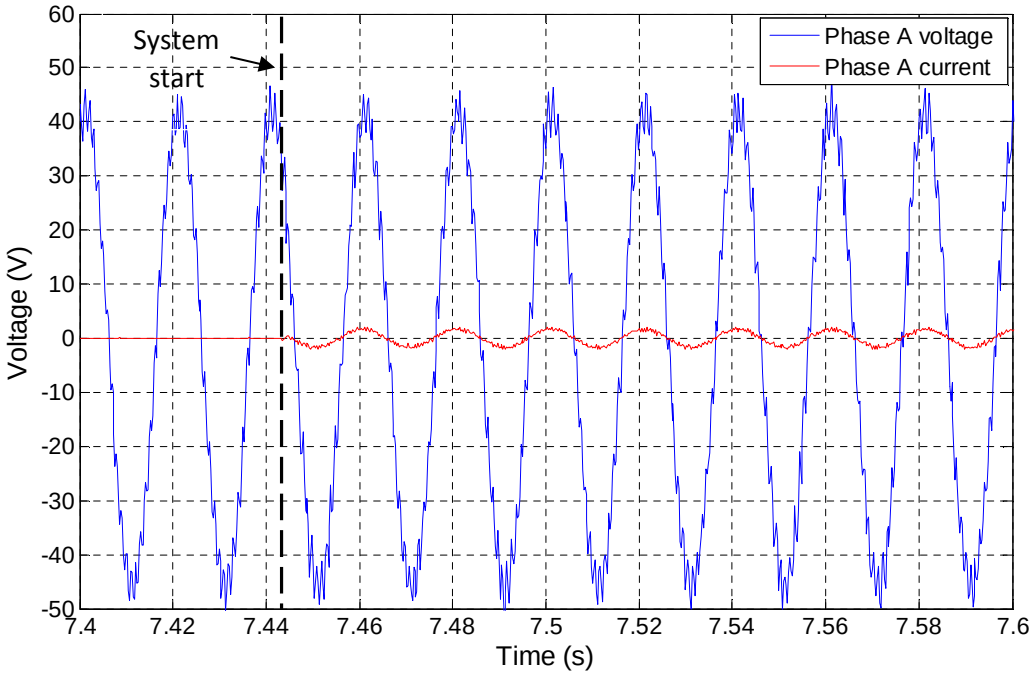


Figure 8.10 Scaled view of the phase current and voltage

The objectives of designing the start-up process are all reached, verified by the experimental results provided in this section. The a.c. voltage-sensor-less current control therefore can be deployed safely utilizing the initial synchronisation acquired by the start-up.

8.2.2 A.c. voltage-sensor-less current control under balanced grid voltage

The a.c. side voltage-sensor-less current control is able to be deployed after obtaining accurate grid synchronisation. To further verify the necessity of deploying the initial start-up procedure, a scaled experiment is carried out to show the effect of incorrect initial grid synchronisation. Figure 8.11 shows the initial current response with good grid synchronisation and Figure 8.12 provides comparison with the case of incorrect grid synchronisation. It can be verified the current overshoot shown is Figure 8.12 is almost twice the amplitude of the steady state current. It can be very hazardous to the power modules in high voltage/power situation.

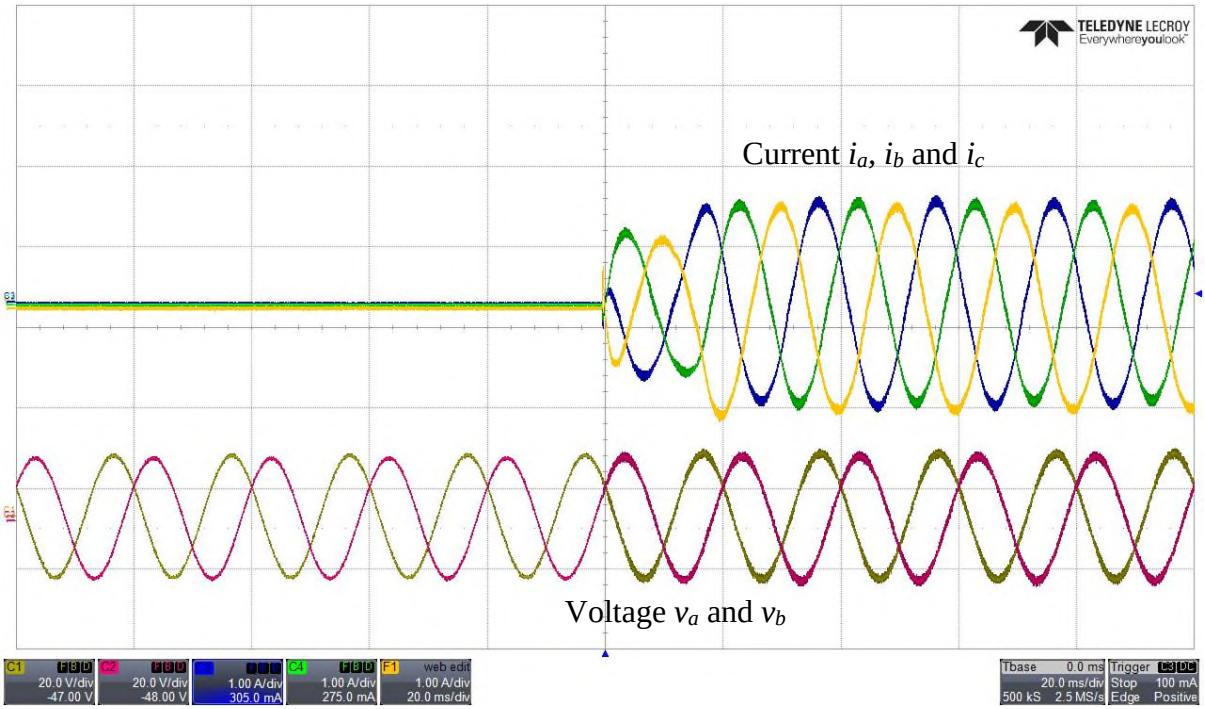


Figure 8.11 Initial current response with accurate grid synchronisation

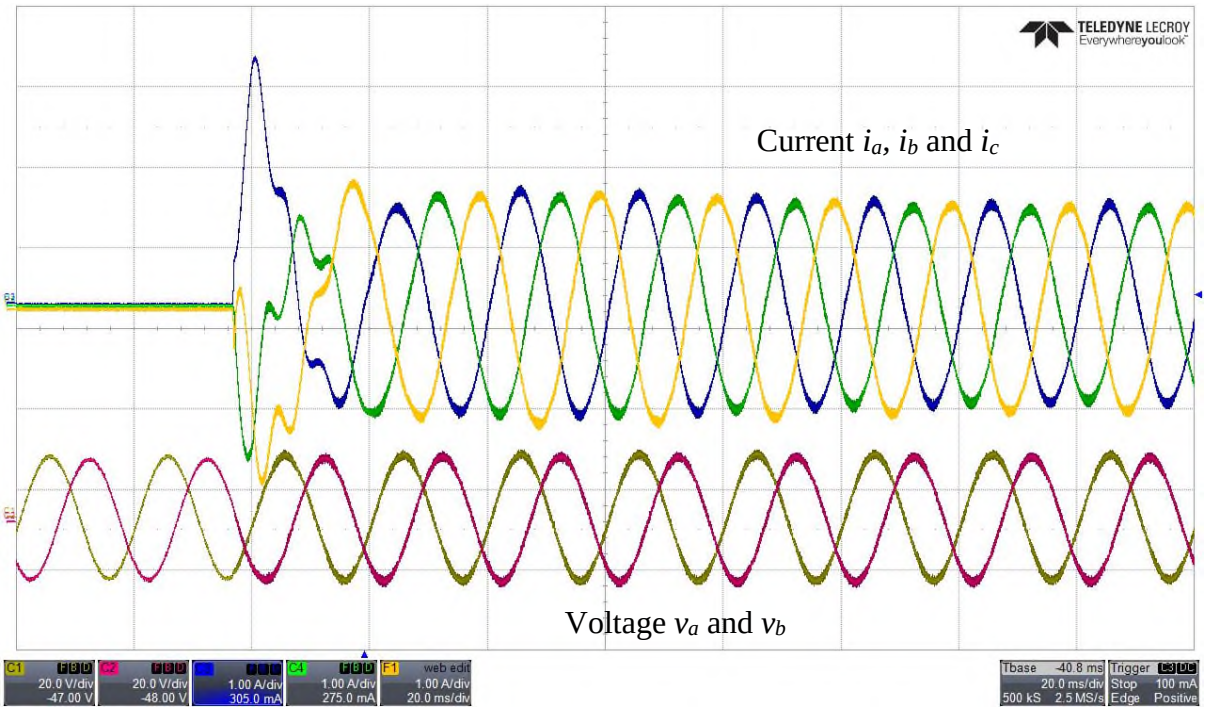


Figure 8.12 Initial current response without accurate grid synchronisation

The fundamental part of the control system as shown in Figure 8.13, including the current controller, grid voltage observer and the dynamic decouple stage needs to be verified for its basic current controllability e.g. balanced grid. The symmetrical components decomposition

system as well as the controller for negative phase sequence are excluded at this moment as they are not necessary for controlling the current under balanced grid voltage. The relevant test will be reported later.

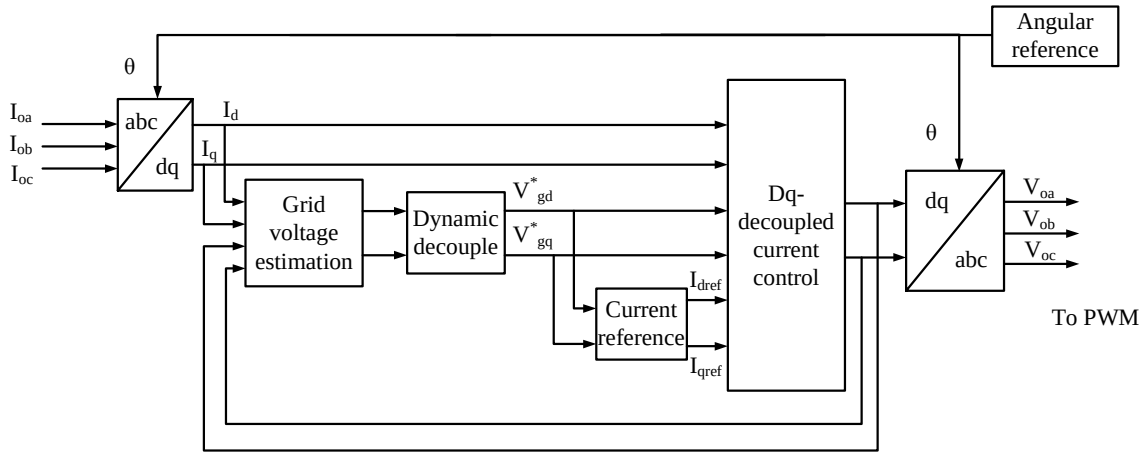


Figure 8.13: The control system put into experiment

The proposed a.c. voltage-sensor-less system is firstly verified with a low power experiment to ensure the stability under the parameter design. The voltage of the a.c. side is also reduced from the nominal value for system protection. As a linear system, the proposed control system should have the same performance regardless the different scale of input, therefore it is valid to predict the system performance under higher power and voltage levels. The system parameters are listed in Table 8.1.

The steady state current is shown in Figure 8.14. Two aspects should be addressed and explained. Firstly, the switching of the power electronic devices should cause harmonic ripples in the current waveform but the shown current waveform is apparently ripple free. This is due to that the data is sampled at the same frequency as the switching frequency. According to Nyquist theory, the switching harmonics are of too high frequency to be sampled thus not visible in the waveform. Secondly, there is a noticeable level of unbalance in the current waveform. This is due to the three phase filtering inductors actually have somewhat different parameters. For a balanced output voltage at the VSI terminals and an equally balanced a.c.

side voltage, the unbalanced phase impedance would cause such an unbalanced current waveform. The unbalanced current can be compensated by activating the negative sequence current controller as what is to be used in the experiment described in Section 8.2.3. In that case, the estimated voltage of the positive sequence will be different from the a.c. voltage that the grid emulator provides, which affects the accuracy of the power control.

Parameters	Values
Grid voltage	30V (Peak Value)
Coupling inductance	10mH
Series resistance	0.1Ω
d.c. voltage	60V
d.c. capacitance	800μF
Power reference	100W
Sampling frequency	10kHz

Table 8.1: System parameters for scaled low power test

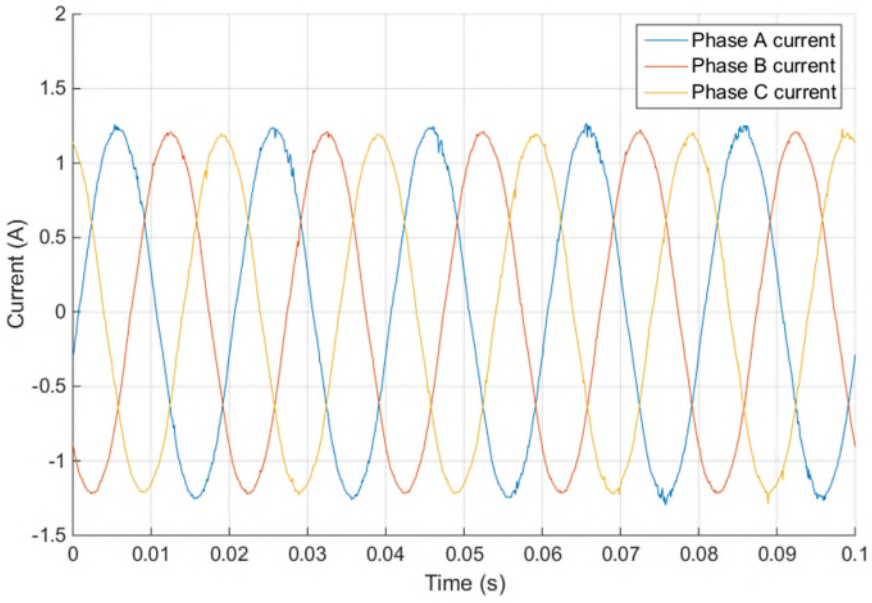


Figure 8.14 Steady state current

The system stability is further verified by the system response under a step change of the a.c. side voltage. The a.c. side voltage is reduced to half of its original value, the controller should be able to track the step change of the a.c. voltage. The current is expected to respond without high overshoot in order to ensure the safety of the power modules and keep the power output at the same time.

In Figure 8.15, the voltage dip is clearly visible around t=0.06s. The current response shown in Figure 8.16 has a small overshoot and reaches steady state in one cycle. The current reference rises as shown in Figure 8.17 to compensate the effect of voltage dip on the power output and the current is controlled to track the current reference. The a.c. voltage estimated shown in Figure 8.18 is following the actual voltage. To clarify, the distorted a.c. side voltage waveform shown in Figure 8.15 is caused by noises affecting the voltage sensors, the actual a.c. voltage does not contain the large spikes shown in the waveform, and the quality of the a.c. side voltage is similar to the voltage waveform shown in Figure 8.8.

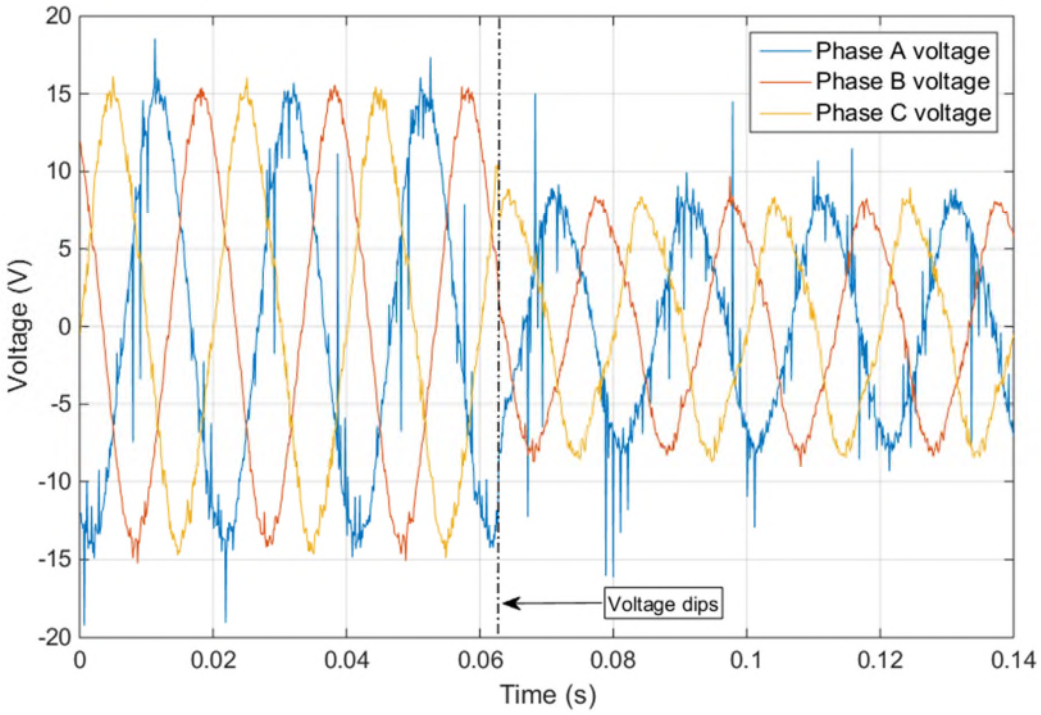


Figure 8.15 Measured three phase voltage of the a.c. side

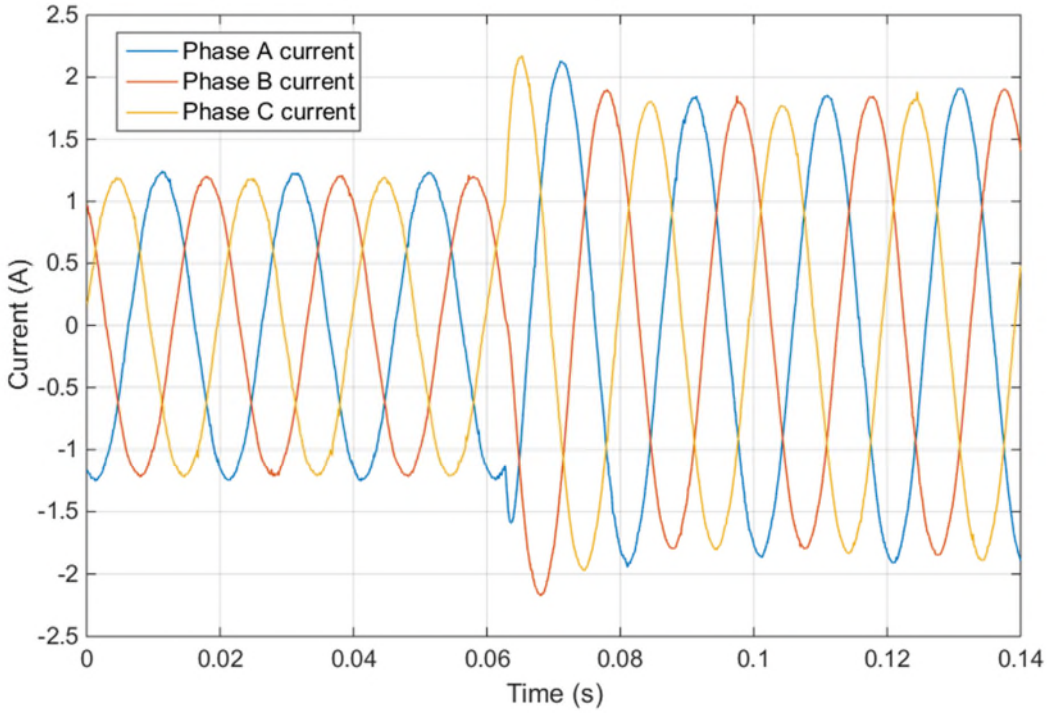


Figure 8.16 Three phase currents

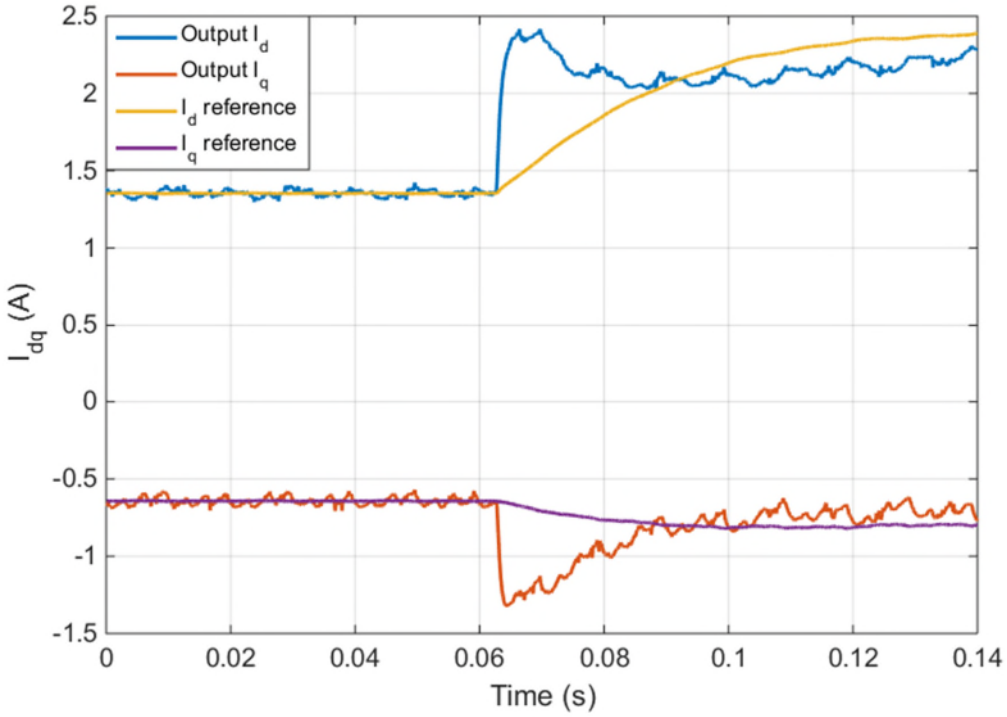


Figure 8.17 Current *dq* components tracking their reference

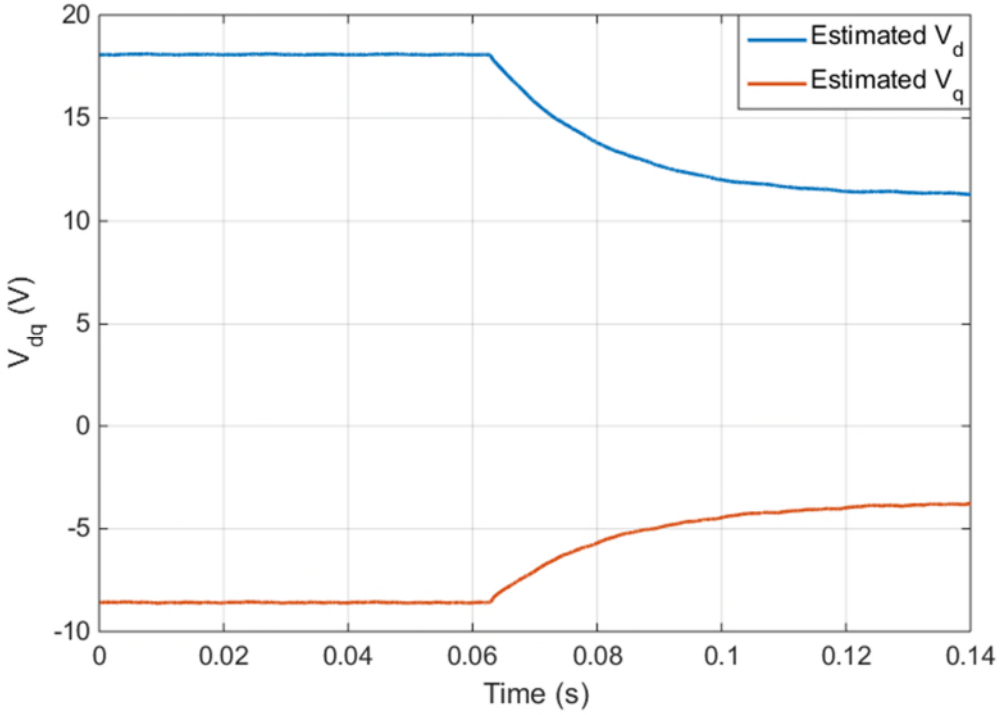


Figure 8.18 Estimated a.c. side voltage *dq* components

The output power is calculated at the PCC. From Figure 8.19, it can be found that the output power is not reaching the reference value of 30W; the power is not directly subject to closed-loop control. There are four possible causes of this result. Firstly, the actual parameters of the filtering inductor can be different from its rated value due to manufacturing. The accuracy of the estimation of the a.c. voltage relies on the accurate parameters of the filter. If the parameters are inaccurate, the current reference will not be generated correctly for the desired power. Secondly, during operation, the heat loss will cause the resistance of the inductor to rise. This can also cause the parameter of the filtering inductor to change from the value used to estimate a.c. voltage. Third, the non-ideal characteristic of the power electronic devices, especially the internal resistance and voltage drop across the semiconductors could cause such an error as they are not modelled in the grid voltage estimation algorithm. The non-ideal characteristic will cause a voltage drop across the semiconductors and the consequence is that the actual output voltage deviate from the voltage reference that the controller yields. Fourth, as discussed

earlier in this section, the filter of the three phases are not ideally balanced. Therefore, the estimation of the grid voltage could contain error.

The first, second and fourth reason to cause the power output error can be solved by carefully selecting components and introduce better cooling. For the third cause of the problem, it is known that the output voltage of the VSI will be smaller than the one used for calculating the grid side voltage which results in the estimated grid voltage larger than its true value. This effect will decrease if higher a.c. side voltage levels is applied as the output voltage of the VSI will increase with the grid voltage for the same power output. The voltage drop will count for a smaller proportion of the total output voltage which reduces its effect on the error of the output power. To totally eliminate the error caused by the conduction loss, a solution would be compensating the voltage drop from the controller side to make the actual output match the voltage reference generated by the controller. As the simulation result with a parameter mismatch shows a smaller error than in the experiment, the experiment result shown should have the power output error being caused by several of the factors discussed above. And due to the fact that the error increases with the current output, the dominant reason would be the reasons associated with heat loss thus the second and fourth reasons.

In real applications, the d.c. bus voltage should have been controlled by an additional controller. The error of the real power output would be reflected from the d.c. side power thus the voltage as discussed in Section 6.2. The power reference will be adjusted accordingly to balance the input and output power of the VSI however this process is not presented in the experimental result due to that the d.c. side voltage is controlled by the d.c. power source other than the VSI.

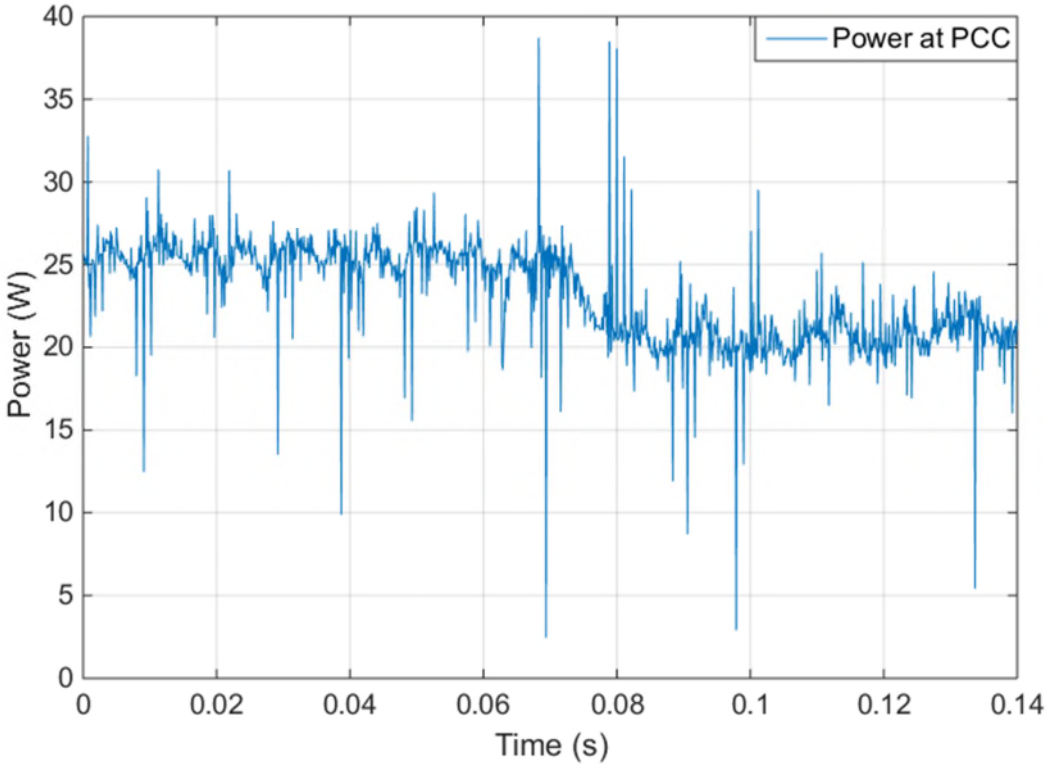


Figure 8.19 Output power at PCC

The high voltage test of the proposed sensor-less current control will be deployed together with the unbalanced voltage dip and detailed in the next section.

8.2.3 Unbalanced grid voltage

The proposed system will be tested under unbalanced grid voltage. The symmetrical component decomposition system as well as the controller for the negative phase sequence is active in this test. The experiment is carried out to verify the capability of the proposed control system to reach the control objective of injecting balanced (smooth) three phase power under unbalanced grid voltage. The current reference for the positive and negative sequence is generated using Equation 4.20. The structure of the control system is shown in Figure 8.18.

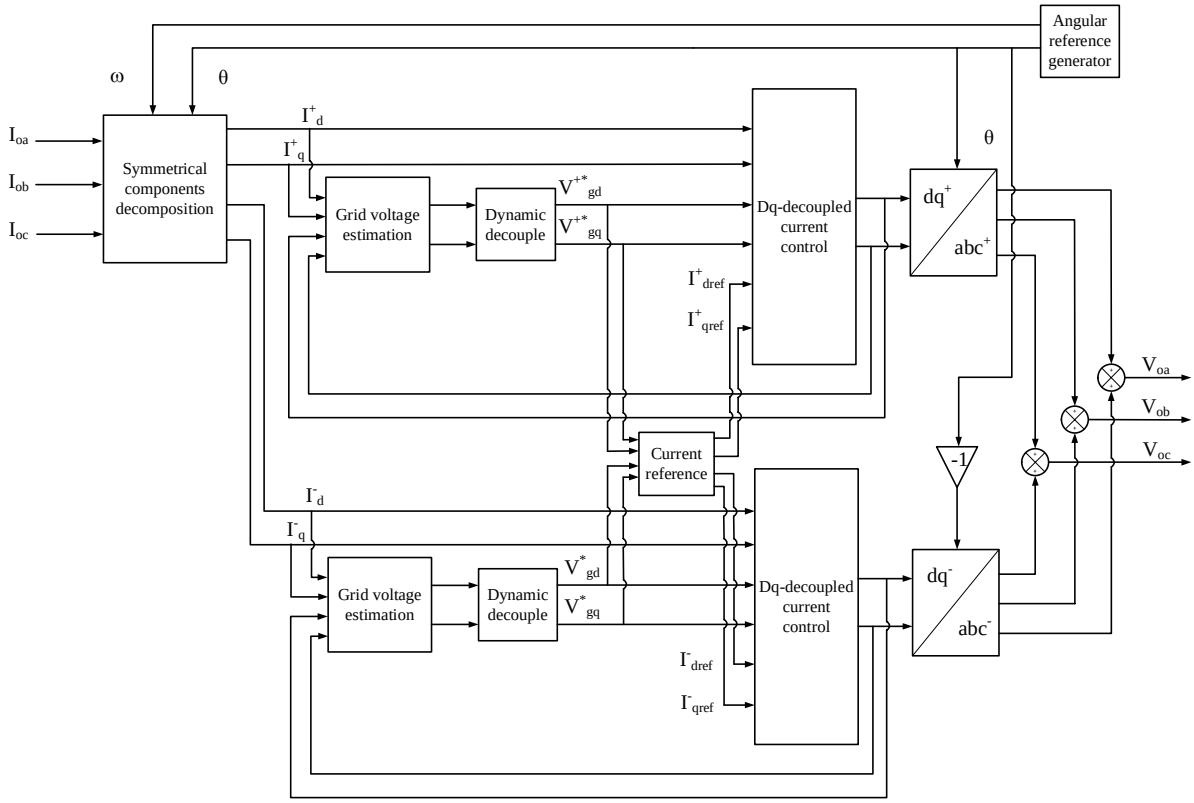


Figure 8.20 Control system structure under test

A voltage dip on phase A is applied and the current response and key parameters during the transient is recorded as follows. The current response shown in Figure 8.21 is compared with the simulation results shown in 8.22. The results shows good agreement between each other. The detailed control actions are shown in Figure 8.23, 8.24 and 8.25. At the time point when the single phase voltage dip is applied, the positive sequence voltage drops while the negative sequence is built up. The voltage-sensor-less current control is able to track such variation. An accurate estimation of the symmetrical components of the grid voltage is acquired with in two fundamental cycles. The current reference is adjusted accordingly to compensate the reduction in the power output. In Figure 8.24 and 8.25, the current reference for positive sequence is rising while a negative sequence current is calculated to achieve a constant power output.

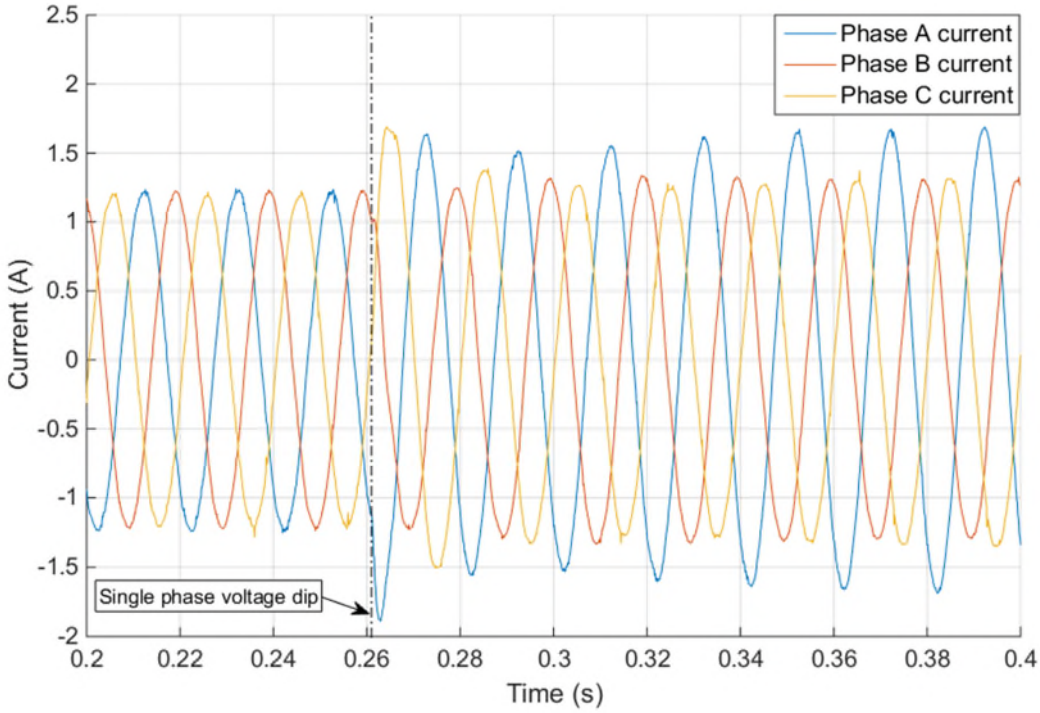


Figure 8.21 Current sampled during experiment

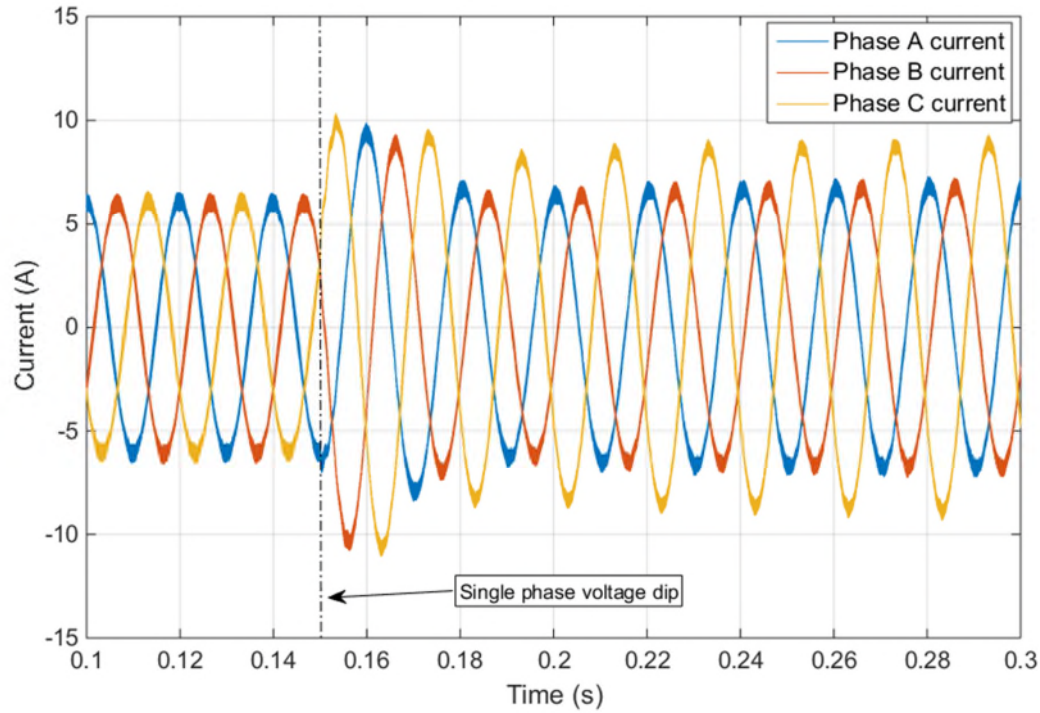


Figure 8.22 Current response during unbalanced fault from simulation

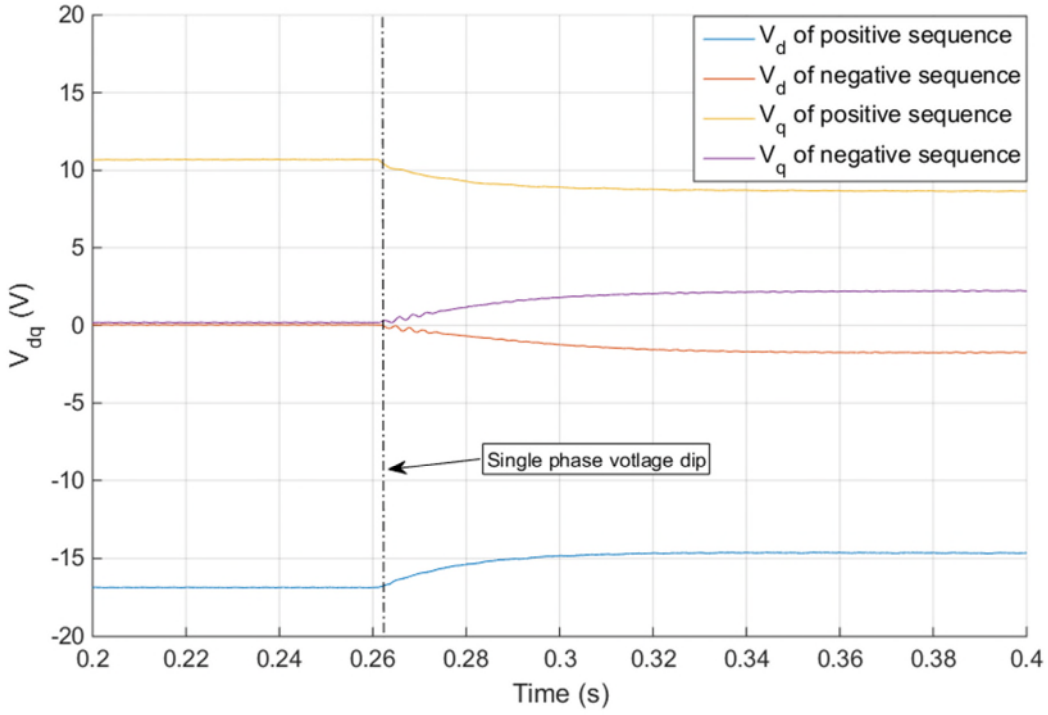


Figure 8.23 Estimated symmetrical components of the grid voltage

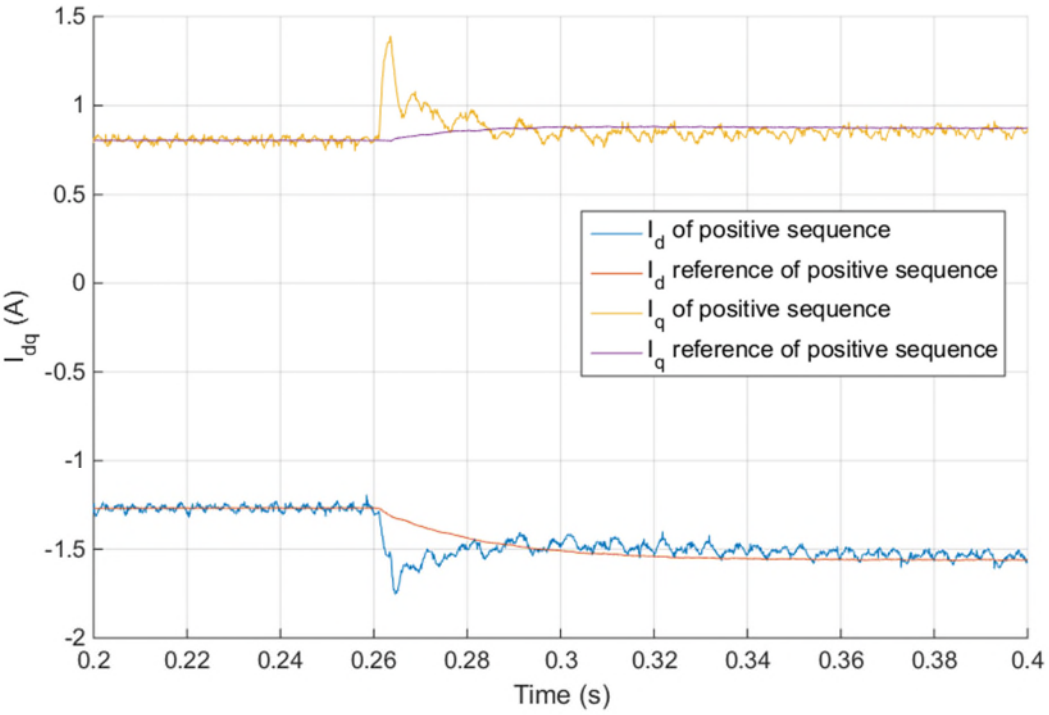


Figure 8.24 The positive sequence current dq-components tracking their reference

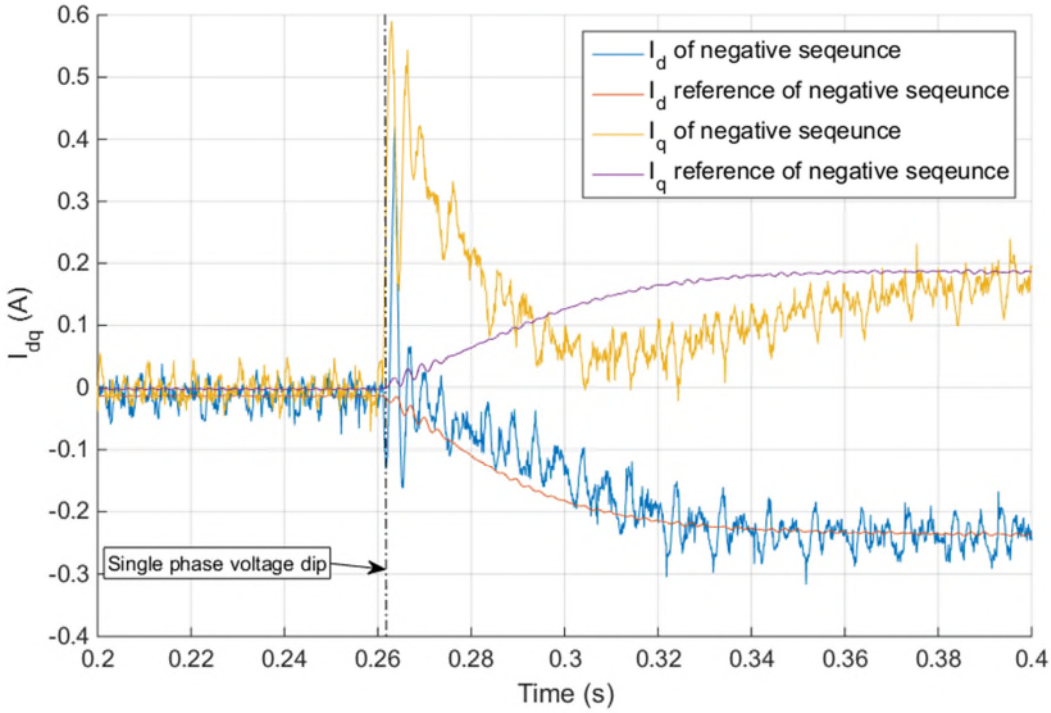


Figure 8.25 The negative sequence current *dq*-components tracking their reference

Another experiment is carried out to verify the capability of the proposed control system to reach the control objective of injecting balanced three phase current. The negative sequence current is not desired thus its references are kept at zero. From Figure 8.26, the output current waveform of this control strategy is well balanced. The unbalanced current output shown in Figure 8.14 of the previous experiment due to unbalanced line impedance is eliminated.

The system structure of this control strategy and tuning are the same as the one for injecting balanced three phase power. The only difference is that only the positive sequence current is adjusted with the a.c. voltage while negative sequence current is kept zero. The system response should show the same pattern as in the scaled experiment described above. A 110V high a.c. voltage test is put into practice and the transient current response is shown in Figure 8.27. The current response when the voltage is back to normal is shown in Figure 8.28. The balanced power strategy is also tested in the high voltage test, the transient current response is shown in Figure 8.29.

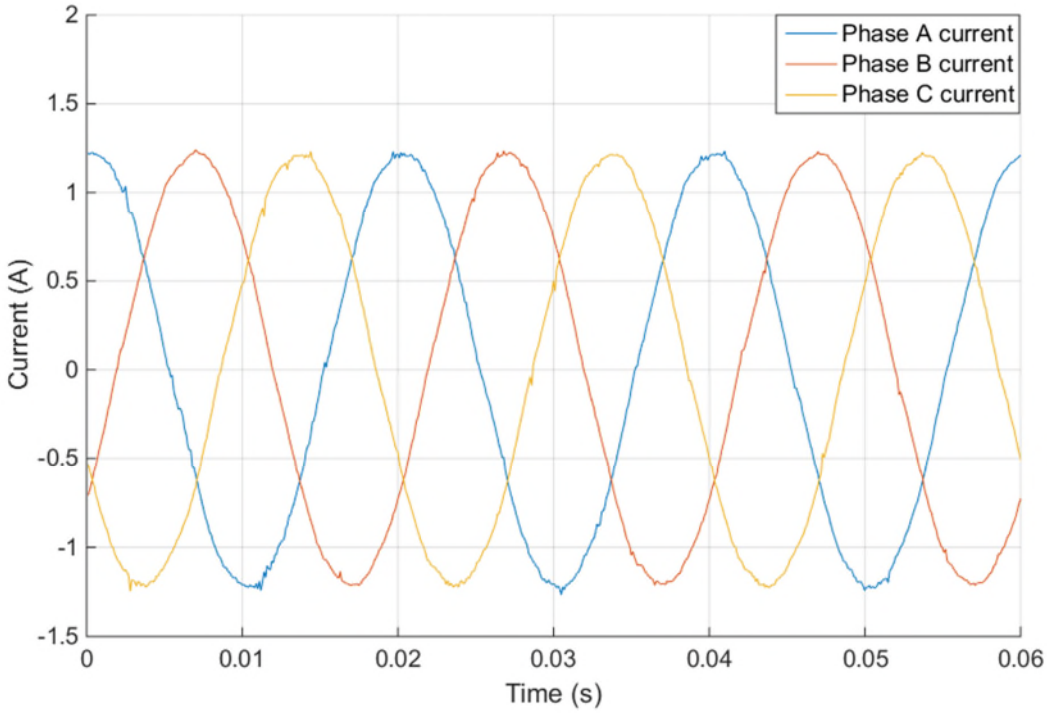


Figure 8.26 Steady state current of proposed system

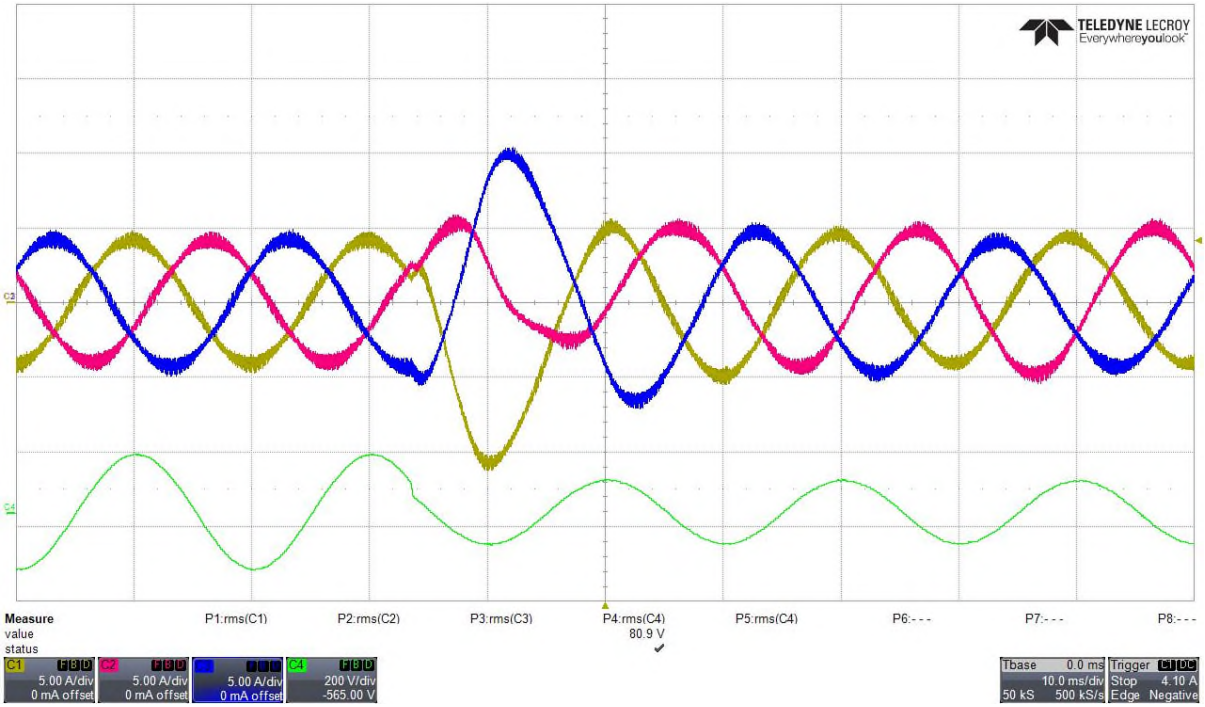


Figure 8.27 Current control transient response at a single phase voltage dip and injecting balanced three phase current

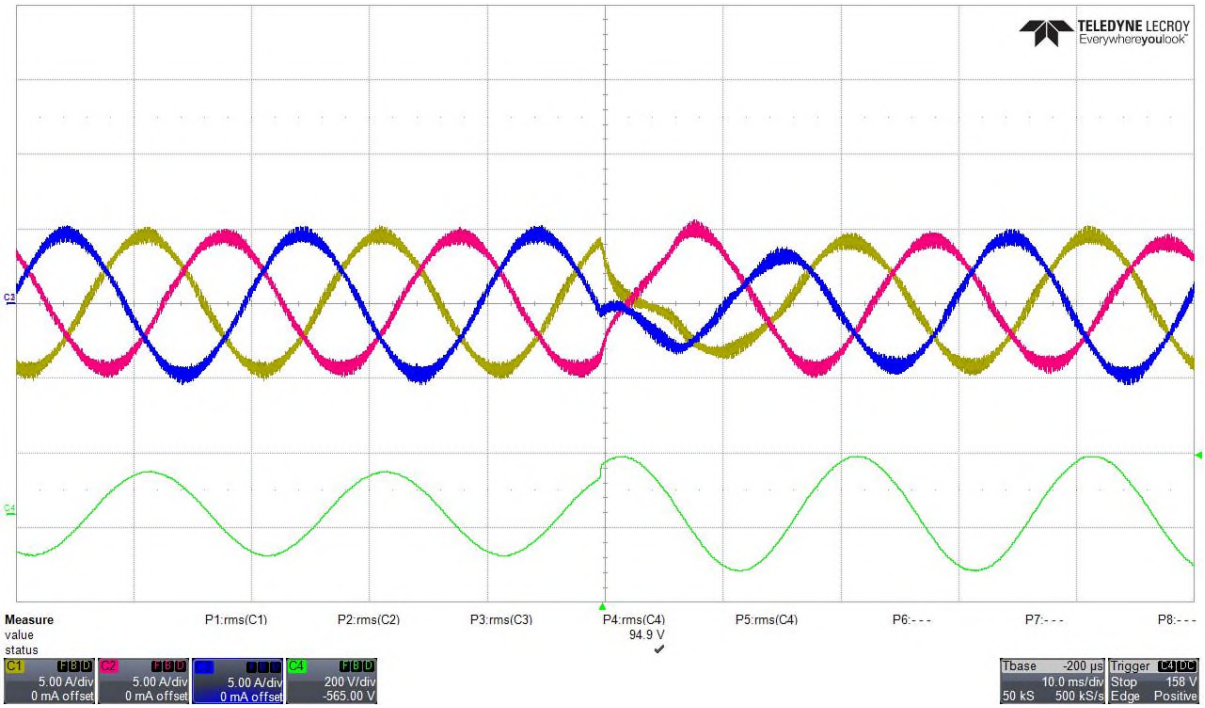


Figure 8.28 Current control transient response when the single phase voltage dip is cleared

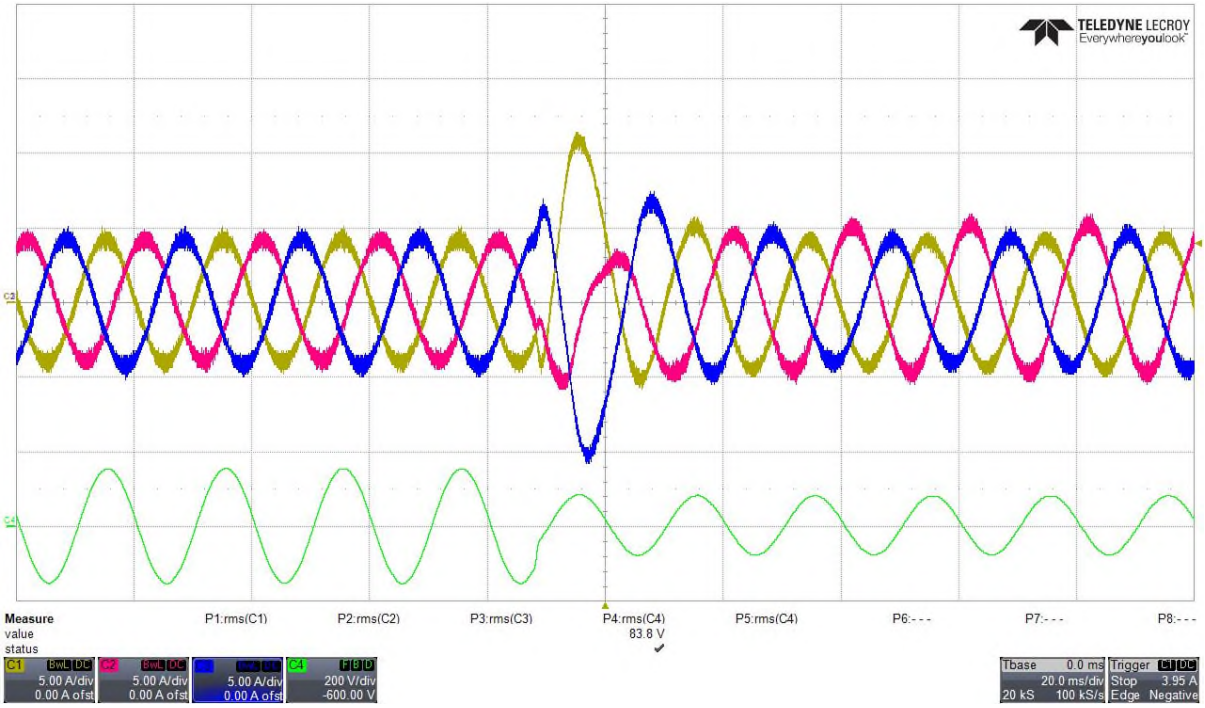


Figure 8.29 Current transient response at single phase voltage dip and injection balanced three phase power

8.3 Chapter summary

A test rig is built with necessary safety measures to carry out the experimental test. The following aspects of the proposed current control system is verified through the data obtained from the experiments:

- The ability of start from zero state and obtain grid synchronisation safely;
- The ability to track the voltage variation of the a.c. side;
- The ability to control the power and maintain stability during grid voltage dips;
- The performance on restricting the harmonic injection.

The start-up process is firstly tested and shown to yield satisfactory results. The information of the a.c. side voltage is acquired and the system response is swift. The system response in the experiment is a good match to the simulation results. Due to the nature of the hysteresis current control, relatively large harmonic injection is visible. However it can be verified the grid synchronisation can be acquired within two fundamental cycles. Then the hysteresis control will stop and PWM kicks in so that the harmonic injection won't cause big problems.

The harmful effect of starting the a.c. voltage-sensor-less control without synchronising to the grid is verified using scaled experiments. The current overshoot is large enough to damage the power modules if the voltage and power is at its normal scale. This shows the importance of carrying out the start-up procedure.

The grid voltage tracking ability of the a.c. voltage-sensor-less control is tested for different types of voltage dips. The results show, with the aid from the symmetrical component decomposition system, both the balanced and unbalanced voltage dips can be tracked. The current reference can be generated according to the grid voltage to reach desired power output under different control objectives. Also, the experimental results show good match to the

simulation results. Since the simulation result shows an improved transient performance after adopting the symmetrical component decomposition algorithm, it is reasonable to believe that the performance of VSIs in real world be improved by the proposed algorithms.

Chapter 9 Conclusion and Future Work

The proposed a.c. voltage-sensor-less current control for the grid connected VSI is presented and verified by the results provided in Chapters 7 and 8. The current control assisted by the newly designed symmetrical component decomposition method is a generic control system with some desirable features. The important rationales behind the design procedure are summarized in this chapter to conclude the research.

9.1 Conclusions

Before tuning the controller, the limits on the operation of the grid connected VSI and its available digital controller are common issues when designing the system. Firstly, the PWM process should be considered. The switching frequency should be selected based on the acceptable power loss due to switching and capability of the heat dispatching. This should require to limit the maximum switching frequency. On contrast, for small applications located domestically, the switching frequency should be high enough to exceed the audible frequency range to avoid being heard. Therefore the selection varies with different applications. The maximum sampling frequency is decided by the digital processor and the complexity of the control algorithm. In some research, high sampling frequency is required which is highly undesirable in designing a practical system. To reduce the cost of the digital processor applied, a low computational burden is always favoured.

The *dq*-decoupled current control is selected to carry out the current control because the maturity of this control method. The analysis and performance are well established in the

research and applications during the last few years. This facilitates the coding when the proposed control algorithm is to be considered in practical applications.

For tuning the *dq*-decoupled current control, although the swift control response is always desirable as a control objective, several aspects in reality influence the applicable decisions. The band-width of the controller should not exceed half of the switching frequency at most constrained by the PWM process that is incapable to control the higher frequency component beyond half of its switching frequency. The sampling frequency is a similar factor which should be treated equally but usually ignored as it is at least equal to or higher than the switching frequency in most of the cases. Then the current controller should be tuned according to the symmetrical component decomposition available to ensure the system performance and stability. These factors are all independent from the current control system design and being well defined by their own restrictions. Once these restrictions are clear, the current controller can be tuned and should be tuned as swift as possible.

The symmetrical component decomposition algorithm is needed in the case of the unbalanced grid voltage. Otherwise the current and power control loops will be affected by the unbalanced voltage and cause many undesired interaction and even instability of the system. The symmetrical component decomposition algorithm will introduce delay into the control system and this is modelled in Chapter 5, whose effect could affect the selection of the current control bandwidth. To minimise the delay introduced by the symmetrical component decomposition algorithm, a newly designed algorithm with accelerated response is put into use. The delay introduced is obviously smaller than that introduced by other decomposition methods and the simulation and experimental results verified the robustness of the current control system. By using the new decomposition method, the current controller is tuned with a bigger bandwidth which improves the performance of the overall system. The integral of the absolute error is

used to evaluate the performance. The control error during the transient response is directly linked to this error thus smaller error means better control accuracy.

The signals needed to operate the conventional *dq*-decoupled current control, such as the current reference, *dq* axis current feedback and grid voltage are still needed but the measurement of the grid voltage is replaced by a voltage estimation system proposed in this study. The current reference is generated using the estimated grid voltage. The effectiveness has been proven to be similar to the conventional *dq*-decoupled control with a delay in the voltage measurement. Considering that if the unbalanced grid fault-ride-through is required, the symmetrical component decomposition algorithm will also introduce such a delay. In the voltage-sensor-less current control, the symmetrical components of the grid voltage are estimated independently and thus no additional symmetrical component decomposition is needed for the grid voltage. Therefore the response of the voltage-sensor-less system doesn't deteriorate from those equipped with voltage sensors. Even better, the low-pass filtering characteristic of the grid voltage estimation system reduced the high order harmonic components which need to be filtered out, using anti-aliasing filters, in conventional current control systems. Another benefit from this arrangement is that a conventional SRF-PLL can be used to track the phase angle of the positive sequence grid voltage component without adding any other algorithms to deal with unbalanced signals. Therefore the tuning process for optimisation of the response of the PLL system together with the symmetrical component decomposition algorithm is not necessary and the design is consequently simplified.

In summary, the presented research achieved several improvement comparing to the conventional system, listed as following:

- The current overshoot at start-up is eliminated while output power is controlled.

- A dq reference frame based a.c. voltage-sensor-less current control system capable of riding-through unbalanced grid fault is developed.
- The transient response is improved using the newly designed symmetrical component decomposition system.

9.2 Future work

Although the newly designed symmetrical components decomposition method has the advantage of introducing less delays, there is still the need to expand it in order to deal with more harmonic components in the voltage. The utilisation of the mechanism would also allow other harmonics to be separated with reduced delays. The mutual relationship of the characteristic harmonics, i.e. the 5^{th} and 7^{th} harmonic usually form 6^{th} harmonic on *dq* axes, should be utilised to optimise the performance and reduce the complexity of the method.

The a.c. voltage-sensor-less current controller can be improved by developing methods to decouple the transient response of the controller of the positive and negative sequences. Then oscillation will be reduced and the steady state can be reached more quickly.

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