Non-equilibrium generation lifetime measurements on MOS devices

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NON-EQUILIBRIUM GENERATION LIFETIME MEASUREMENTS ON MOS DEVICES

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A thesis submitted in accordance with the regulations for the degree of Master of Science in the University of Durham

1982

ABSTRACT

This thesis is concerned with the study of the interface and bulk properties of n-type and p-type silicon MOS devices.

The widely used quasi-static technique has been applied to the interface state analysis. The method (due to Kuhn) consists of applying a linear voltage ramp to the sample at a sufficiently low sweep rate so as to maintain the device in quasi-equilibrium.

The non-equilibrium characteristics of the device were measured by the fast ramp technique. From such characteristics, the bulk trap density and the generation lifetime were obtained.

An analogue circuit was built to give a direct plot of surface potential versus gate voltage in equilibrium as well as in non-equilibrium conditions. Such plots were compared with those generated theoretically and with those obtained using graphical integration of the I-V curves. There was a close agreement between all these results.

The transient charge due to small voltage steps applied to an MOS capacitor in inversion was measured. The results were analysed to give the generation lifetime which was compared with that obtained from the fast ramp non-equilibrium analysis. The values agreed well for an n-type sample, but they differed by a factor of three for a p-type one. Further experimental and theoretical work will be needed to find the reason for this discrepancy.

ACKNOWLEDGEMENTS

I would like to thank my supervisors, Dr. M.J.Morant and Dr. P.G.C.Allman, who created the unique atmosphere which made this work possible. Their guidance during the course of the work and help in the preparation of this thesis are most appreciated.

Many thanks are due to Dr. A.G.Nassibian of Western Australia University and to the University of Edinburgh for providing the devices used in this work. It is certainly a pleasure to acknowledge Mr. Z.A.Ibrahim who provided assistance and his apparatus for the measurement of Q-t. I would also like to thank all the technicians who have helped me in various ways. My gratitude also goes to Mrs. S.Mellanby for her invaluable work in typing this thesis.

I wish to express my appreciation to the Universiti Sains Malaysia for the award of a fellowship and also the Public Services Department of Malaysia for granting financial assistance.

Finally, my particular gratitude goes to my parents for their endless advice and encouragement during my study in Durham.

LIST OF SYMBOLS

C	Small signal capacitance, F/cm^2
C_d	Depletion capacitance, F/cm^2
C_{FB}	Capacitance at flat-band, F/cm^2
C_i	Inversion capacitance, F/cm^2
C_m	Minimum high frequency capacitance, F/cm^2
C_{ox}	Oxide capacitance, F/cm^2
C_{sc}	Semiconductor space-charge capacitance, F/cm^2
C_{ss}	Interface state capacitance, F/cm^2
d_{ox}	Oxide thickness, cm.
E_c	Bottom of conduction band, eV
E_F	Fermi level in semiconductor bulk, eV
E_{Fm}	Fermi level in metal, eV
E_{Fs}	Fermi level at oxide-semiconductor interface, eV
E_g	Energy gap, eV
E_i	Midgap energy level, eV
E_t	Trap energy level in bulk, eV
E_T	Trap energy level at the oxide-semiconductor interface, eV
E_v	Top of valence band, eV
I	Current, A/cm^2
ΔI	Drop in current at sweep reversal, A/cm^2
I_d	Depletion current, A/cm^2
I_f	Total forward current, A/cm^2
I_g	Generation current, A/cm^2
I_o	Current at strong accumulation condition, A
I_r	Total reverse current, A/cm^2
k	Boltzmann's constant, $eV/^oK$
L_D	Extrinsic Debye length, cm
L_E	Normalized steady-state depletion width, cm
n	Density of free electrons, cm^{-3}

n_i	Intrinsic carrier concentration, cm^{-3}
n_{po}	Minority carrier density, in equilibrium, cm^{-3}
N_A	Acceptor concentration of substrate, cm^{-3}
N_D	Donor concentration of substrate, cm^{-3}
N_{ss}	Interface state density, cm^{-2} eV^{-1}
N_t	Bulk trap density in semiconductor, cm^{-3}
p	Density of free holes, cm^{-3}
p_{po}	Majority carrier density, in equilibrium, cm^{-3}
q	Electronic charge, Coul
Q_B	Charge within the surface depletion region at the onset of strong inversion, $Coul/cm^2$
Q_{fc}	Interface fixed charge, $Coul/cm^2$
Q_g	Gate charge, $Coul/cm^2$
Q_m	Initial charge at the beginning of charge transient, Coul
Q_n	Charge in inversion region, $Coul/cm^2$
Q_o	Total charge stored in MOS system, Coul
Q_s	Space-charge in semiconductor, $Coul/cm^2$
Q_{ss}	Interface state charge, $Coul/cm^2$
R_t	Resistance associated with the generation-recombination processes, ohms
t	Time, sec
T	Absolute temperature, ^oK
U	Bulk generation-recombination rate, cm^{-3} sec^{-1}
U_g	Bulk generation rate, cm^{-3} sec^{-1}
v_{th}	Thermal velocity, cm/s
V	Gate voltage above V_o, Volts
V_d	Voltage dropped across the depletion region, Volts
V_{FB}	Flatband voltage, Volts
V_g	Gate voltage, Volts
V_o	Gate voltage at onset of generation, Volts

V_{ox}	Oxide voltage, Volts
V_R	Gate voltage at the dropback to equilibrium on reverse sweep, Volts
ΔV_g	Voltage step, Volts
x	Distance into semiconductor from interface, cm
x_d	Depletion width, cm
x_{dm}	Maximum depletion width in equilibrium, cm
x_o	Depletion width at start of generation, cm
z	Normalised depletion width
z_B	Normalised depletion width at instant of sweep reversal
α	Voltage sweep rate, Volts/sec
β	q/kT, $Volts^{-1}$
ψ	Electrostatic potential, Volts
ψ_s	Surface potential, Volts
ψ_F	Fermi potential, Volts
$\mathcal{E}$	Electric field strength, Volts/cm
$\mathcal{E}_s$	Electric field strength at surface of semiconductor, Volts/cm
σ	Capture cross section, cm^2
ϵ_{ox}	Oxide permittivity, F/cm
ϵ_s	Silicon permittivity, F/cm
ρ	Charge density, $Coul/cm^3$
ϕ_{ms}	Metal-semiconductor work function difference, Volts
τ_g	Generation lifetime, sec
τ_r	Time constant of the charge transient, sec

C O N T E N T S

CHAPTER 1

INTRODUCTION

1.1 Introduction

Metal-oxide-semiconductor (MOS) based electronics components account for a substantial proportion of all devices (both discrete and integrated) manufactured. Such devices cover a wide range including field-effect transistors, charge-coupled devices and memory (dynamic and static). A thorough physical understanding of such MOS structures is thus essential.

The most popular tool used for study is the MOS capacitor, thus being the most simple MOS structure. The MOS capacitor allows us to study such parameter as mobile and fixed ions within the oxide, the trapping states (interface states) which occur within the semiconductor forbidden band-gap at the semiconductor-oxide interface and trapping states within the forbidden band-gap in the bulk of the semiconductor (bulk states). All of these effects are detrimental to the operation of the aforementioned MOS based devices.

In this thesis, the work will be mainly concerned with a study of bulk traps and a brief account for every chapter is arranged as follows.

The second chapter is concerned with interface states analysis. The method made use of is that presented by Kuhn (14), in which the displacement current is measured upon application of a slow voltage ramp to the gate of the MOS capacitor. A study of bulk traps is treated in the third chapter. The method consists of applying a fast voltage ramp so as to take the device into the non-equilibrium condition. The various sections of the resulting non-equilibrium I-V curves are identified using the non-equilibrium theory proposed by Board and

Simmons (29) ; the generation lifetime can then be extracted. Surface-potential as a function of gate voltage is generated experimentally and compared with theory. The fourth chapter is concerned with the measurement of a charge transient upon application of a step voltage to the gate of the MOS capacitor. The generation lifetime is extracted from the transient curve using the simple theory presented by Hofstein (23). The results obtained from this measurement are compared with results obtained from the fast ramp setup.

1.2 Review of the Subject

The advent of the MOS structure can be considered to have heralded a new era in semiconductor device research. It was first proposed as a voltage variable capacitor by Moll (6) and Pfann and Garrett (7). The structure was then employed by Terman (8) in the study of thermally oxidised silicon surfaces after Frankl (9) and Lindner (10) analysed its characteristics.

Many experimental techniques were developed in an effort to understand the physics of the MOS system. Early experimentation was concerned mainly with the study of the interface properties of silicon-silicon dioxide. Terman (8) used the high frequency capacitance method in evaluating the interface state density. Following this, Gray and Brown (11) proposed a method of temperature variation to study interface states, while maintaining the surface potential at a fixed value.

Nicollian and Goetzberger (12) established the admittance method, again in an attempt to evaluate the density of interface states. However, this precise technique is unsuitable for a rapid evaluation of the device parameters. Furthermore, the interface state density can only be measured in a small portion of the forbidden energy gap and information concerning the bulk semiconductor properties cannot be obtained.

In 1966, Berglund (13) provided the basic theory for the quasi-static method which made use of very low frequency device excitation in order to maintain it always in electrical equilibrium. Following this, Kuhn (14) and Castagne (15) provided an easy and fast technique which allowed interface state density over large parts of the energy gap to be determined. The method consists of applying a very slow linear voltage ramp to the device whilst at the same time measuring

current response. Then, the interface state density can be determined by comparing this data with a calculated ideal low frequency (14) or high-frequency (15) curve. Values of interface state density down to $\sim 10^{10}$ cm^{-2} V^{-1} can be achieved using the former method.

As mentioned above, the traditional experimental technique has been to measure the capacitance or conductance as a function of a d.c. or slowly varying gate voltage. By operating the device in a non-d.c. equilibrium situation, it has become possible to study the generation-recombination characteristics in the bulk as well as at the interface of semiconductor. After Schockley and Read and Hall (5) proposed the model of generation-recombination process, much effort has been expanded on the verification and use of this model.

Much work has been published concerning the determination of generation and recombination lifetime (31) of excess minority carriers from measurements on an MOS capacitors. These measurement techniques involved monitoring quantities such as current or capacitance after the device is brought to a non-equilibrium condition. Some techniques cause large deviations from equilibrium whilst others involve small deviations from thermal equilibrium.

The concept of the pulsed MOS structure was first proposed by Rupprecht (16) to study the generation properties of surface states in germanium. It was later extended to the bulk properties. Jund and Poirier (17) have used this method of monitoring the capacitance as a function of time to obtain the bulk generation lifetime. The technique was further developed by Zerbst (18) to again extract the generation lifetime and the surface generation velocity. In view of the Zerbst (18) analysis, Schroder and Nathanson (19) showed that a correction must be applied when interface generation is significant so that bulk and surface-dominated generation can be separated. Further

work by Schroder and Guldberg (20) presented a detailed analysis of lifetime interpretations using this pulsed technique. The method made use of experimental aspects of the Zerbst (18) analysis and it was shown that surface generation, which is characterised by a surface generation velocity, can be eliminated if the surface is initially in the inverted condition. However, if the interface state density is very large, which would result in strong surface generation, then it is not possible to completely ignore it, even though the surface is shielded by an inversion layer.

Heiman (21) described the method of applying a large voltage step to the gate of an MOS capacitor in such a direction as to take the system from accumulation to depletion and the model of Zerbst was used to evaluate the bulk generation lifetime. Huang (22) introduced a technique of applying a large signal step voltage to MOS capacitors in strong inversion and monitoring the change of the MOS capacitance as a function of time. The lifetime can be easily extracted from the transient waveform. The advantage of this method again lies on the fact that the device is operated in heavy inversion where the surface state contribution is negligible and the use of a large-signal measurement which produced a pronounced change in observed capacitance transient.

Hofstein (23) introduced a simple method for the determination of the generation lifetime. It consists of applying a small depleting voltage step to the device biased in inversion condition and measuring the charge flow as a function of time. The generation lifetime can then be extracted from the transient response characteristics. Although this method eliminates interface state effects, it faces the problem of pick up and leakage in the measuring circuit.

Berglund (24) suggested a method by which carriers are injected from the inversion layer into the semiconductor bulk to create an excess concentration of minority carriers. This method was later employed by Tomanek (25) to evaluate recombination lifetime. The work involved applying a voltage pulse of reverse polarity to the MOS system biased in inversion, so that the space charge region will cease to exist in a very short time. This results with some of the minority carriers unable to recombine during the pulse duration. As the pulse terminated, the inversion layer is reconstituted under the influence of the d.c. bias. By measuring the capacitance after termination of a pulse of such duration, it is possible to calculate the charge carriers that being able to recombine during the pulse, which is used to obtain the recombination lifetime.

Both the methods of Heiman (21) and of Tomanek (25) include the effect of surface states, since, during the transient, the quasi-Fermi level at the surface sweeps through the major portion of the bandgap. If interface state densities are large, incorrect bulk lifetime values are therefore obtained.

Simmons and Wei (26) provide a somewhat different approach in analysing the pulsed MOS capacitor. They have studied in detail the Shockley-Hall-Read (5) generation rate equation and considered their effect on the capacitance transient of the Zerbst's analysis.

The method of Kuper and Grimbergen (27) uses a depleting linear voltage ramp applied to the gate of an MOS capacitor biased initially in inversion to cause the device to go into the non-equilibrium state. Then, the generation lifetime can be obtained from the measurement of high-frequency small signal capacitance and the gate current, at particular sweep rate. The method was shown to be very successful in measuring devices with short lifetimes as well

as for those with long lifetimes.

Trullemans and Van de Wiele (28) introduced a method of measuring the current response as a function of time upon application a step voltage ; the device being biased from inversion to stronger inversion. The bulk lifetime obtained using this method was shown to agree quite well with the capacitance-time transient method of Zerbst.

Recently, Board and Simmons (29) presented an analysis of the response of an MOS capacitor upon application of a fast linear voltage ramp. Subsequently, Board, Simmons and Allman (39) have shown experimental proof of this theory.

Allman and Simmons (40,41) introduced a constant-current rather than a constant-voltage ramp method (29) to biasing the MOS device. The method was shown to have an advantage over the constant-voltage ramp method in that the total semiconductor capacitance can be extracted directly from the curves, thus easing analysis.

CHAPTER 2

INTERFACE-STATE ANALYSIS

2.1 Introduction

This chapter is concerned with the evaluation of the density of interface states that occur within the MOS capacitor. The conditions occurring within this surface region are intimately connected to the device fabrication parameters. The most important example of the necessity for good surface control is where a semiconductor junction terminates at a surface(usually the silicon-silicon dioxide interface). Extensive studies using MOS capacitors have given a better understanding of the characteristics of this interface region. The knowledge gained has been used to control the properties of this interface, giving rise to modern fabrication techniques for high quality devices.

Since the periodicity of a crystal lattice at a surface is disturbed, it was predicted by Shockley (1) that a high density of energy states (designated interface states) will be introduced into the forbidden energy band gap. These states are found to have a measurable density of the order of 10^{10} to 10^{12} cm^{-2} eV^{-1} and are more or less uniformly distributed in energy over the centre portion of the energy gap (2).

The technique proposed by Kuhn (14) is often used to determine the interface-state density of both n-type and p-type MOS devices. It consists of applying a slow linear voltage ramp of such a rate as to maintain the device in equilibrium, the resulting instantaneous current being measured as a function of applied voltage.

2.2 The Ideal MOS Characteristics

An ideal MOS structure is defined as that which is free of work function difference mobile and fixed oxide charge and interface states.

The simple MOS structure with a p-type substrate is illustrated in Fig. 2.1. The ideal energy band diagram corresponding to zero gate voltage is shown in Fig. 2.2.

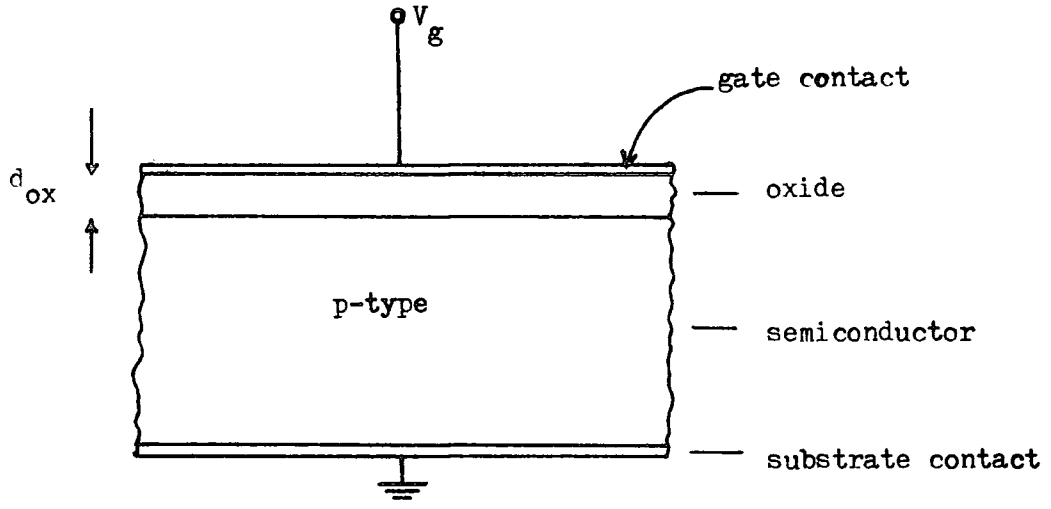


Fig. 2.1 : MOS capacitor structure.

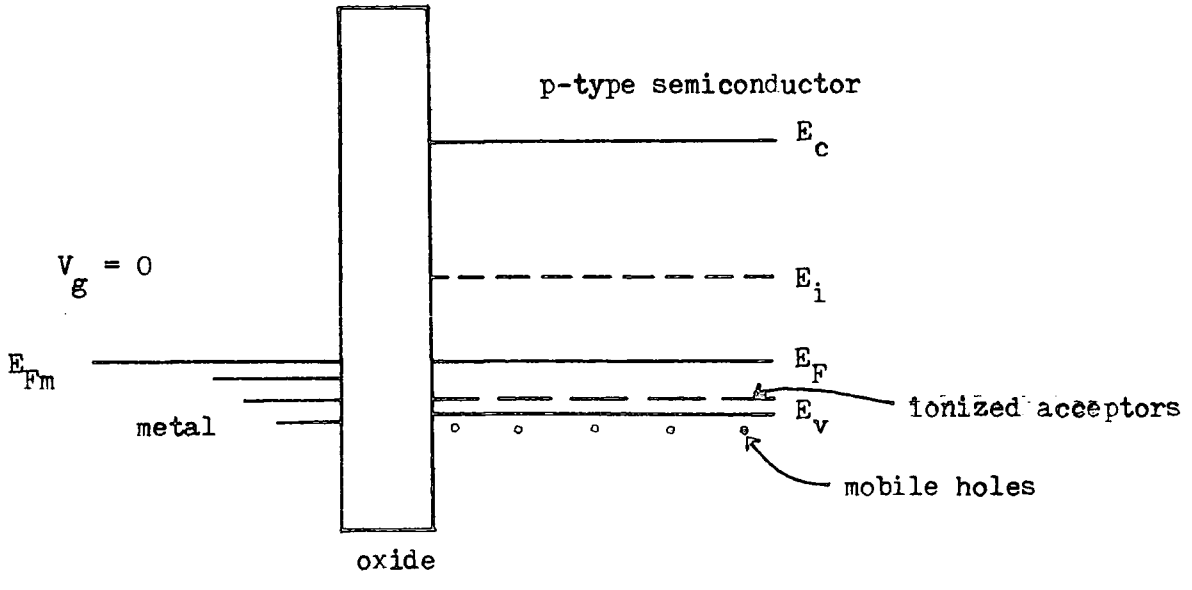


Fig. 2.2 : Ideal energy band diagram at $V_g = 0$.

The MOS capacitor can be biased with both negative and positive gate voltages. For a negative gate voltage, $V_g < 0$, the energy bands in the semiconductor will bend up and the majority carrier (holes) are attracted towards the oxide-semiconductor interface, thus creating an accumulated surface layer ; the semiconductor bulk remains effectively neutral. To compensate these accumulated charges, an equal negative electron charge forms on the gate. This is shown in Fig. 2.3(a)

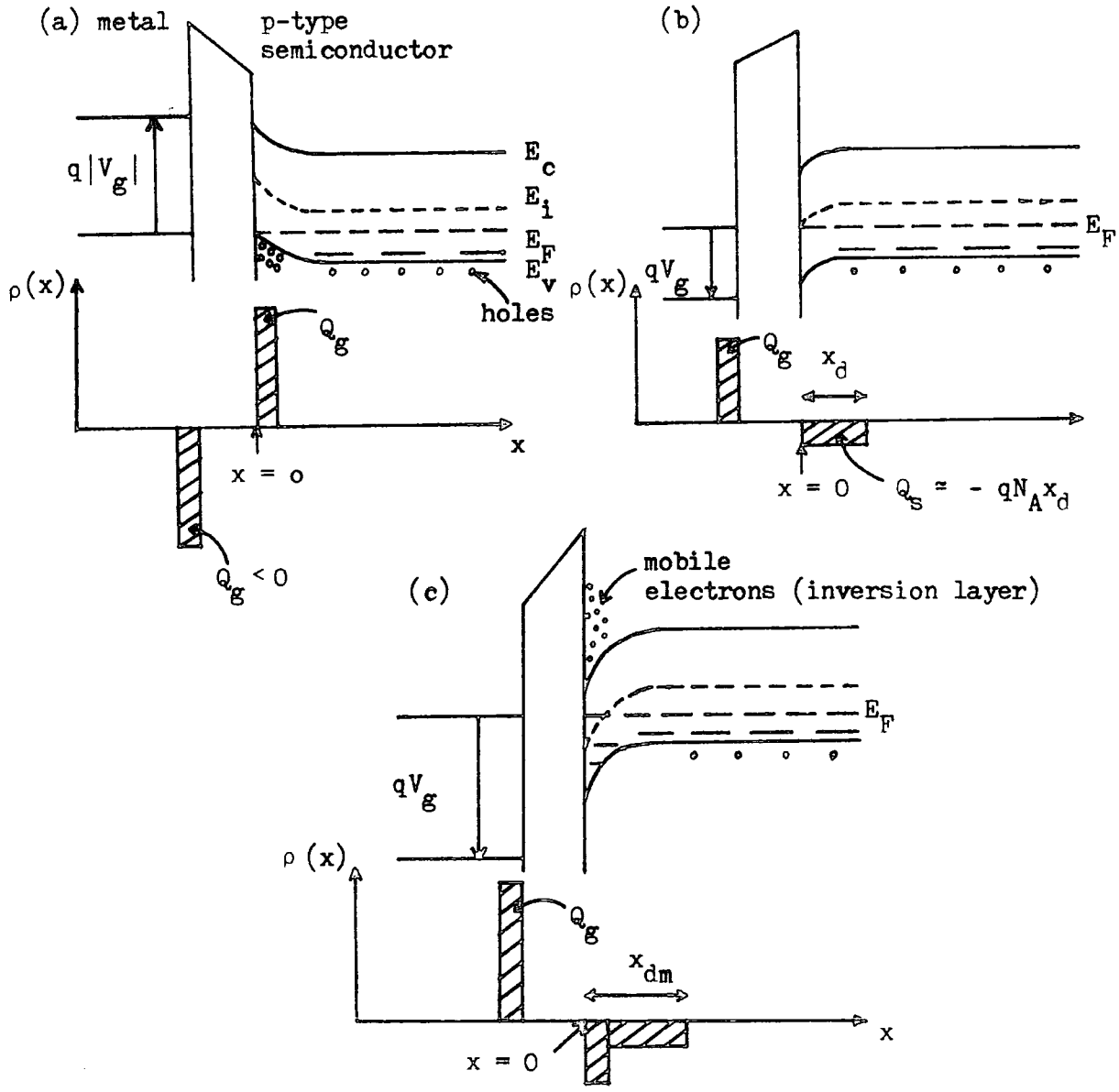


Fig 2.3 : Energy band diagram and charge distribution in an MOS structure upon applying external bias.

(a) $V_g < 0$, accumulated surface layer
(b) $V_g > 0$, depleted surface layer
(c) $V_g >> 0$, inverted layer at the semiconductor surface.

Holes will be repelled from the oxide-semiconductor interface when a positive bias is applied to the gate ($V_g \geq 0$), leaving the surface layer a region depleted of mobile charge, as shown in Fig 2.3 (b). The charge density in this depletion region is determined by the ionized donor density so that,

$$Q_s = -q N_A x_d \quad \text{C cm}^{-2} \qquad (2.1)$$

where x_d is the depletion layer width. In practice, the transition from the depleted region to the neutral bulk is not as abrupt as shown in the diagram.

If the gate voltage becomes more positive, the energy bands bend further, with the effect that the conduction band edge moves closer towards the Fermi level. Electrons will thus be caused to pile up at the oxide-semiconductor interface creating what is known as an inversion layer, shown in Fig 2.3 (c).

Assuming that Q_n is the total electron charge per unit surface area built-up in the inversion region, then from charge neutrality requirements, we obtain,

$$Q_s = -Q_n - q N_A x_d = -Q_g , \qquad (2.2)$$

where Q_g is the charge on the metal gate.

The process of accumulating electrons to form the inversion layer together with the widening of the depletion region occurs within a certain time constant which is characterized by the generation lifetime. Due to this fact, the dynamic characteristics of the MOS system is a strong function of the frequency of the measurement. At very low frequencies, the device follows the d.c. equilibrium characteristics, while at higher frequencies the behaviour will become frequency dependent.

2.2 (a) Charge in the Semiconductor Surface Layer :

For an MOS capacitor under steady-state bias, the ~~system~~ semiconductor is considered to be in equilibrium provided that there is no conduction through the oxide.

By making the assumptions that the doping concentration is uniform, the impurities are fully ionized, and the statistical function under consideration is not degenerate, it is possible to compute the electric charge in the semiconductor surface layer (31).

Using the convention defined in Fig 2.4 for the parameters, we use Poisson's equation :

$$\frac{d^2\psi}{dx^2} = -\frac{\rho(x)}{\varepsilon_s} \tag{2.3}$$

where $\rho(x)$ is the total space-charge density and ε_s is the permittivity of the semiconductor. Integrating Eq (2.3) yields :

$$\mathcal{E} = -\frac{d\psi}{dx} = \pm \frac{2kT}{q\,L_D} F\left\{\beta\psi, \frac{n_{po}}{p_{po}}\right\} \tag{2.4}$$

where $\mathcal{E}$ = electric field in s/c and L_D = extrinsic Debye length.

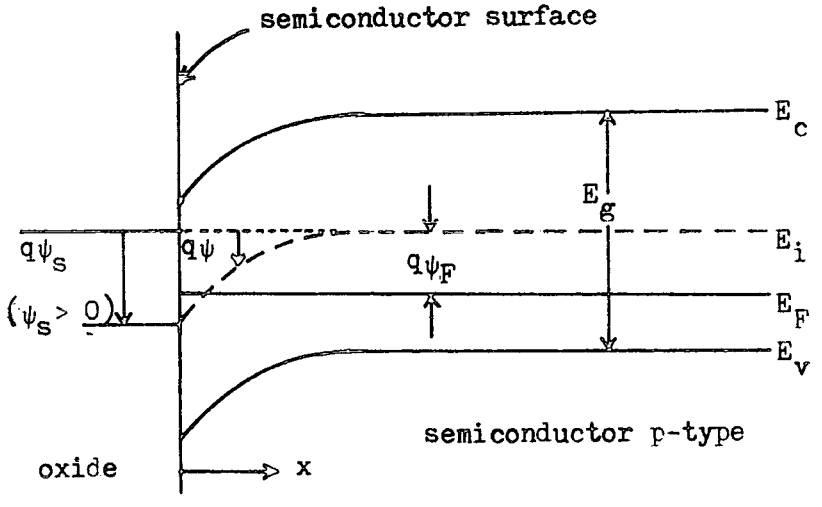


Fig 2.4 : Energy band diagram at the surface of a semiconductor. The potential ψ is measured with respect to the intrinsic Fermi level E_i (after Sze (31)).

At the surface, the electric field becomes :

$$\mathcal{E}_s = \pm \frac{2kT}{q\,L_D} \; F\left(\beta\psi_s, \frac{n_{po}}{p_{po}}\right) \tag{2.5}$$

where

$$F\left(\beta\psi_s, \frac{n_{po}}{p_{po}}\right) = \left[\left(e^{-\beta\psi_s} + \beta\psi_s - 1\right) + \frac{n_{po}}{p_{po}} \left(e^{\beta\psi_s} - \beta\psi_s - 1\right) \right]^{\frac{1}{2}} \geq 0$$

and

$$L_D = \sqrt{\frac{2E_s}{q\beta N_A}}, \quad \beta = q/kT.$$

Using the relation : $p_{po} \simeq N_A$,

and $n_{po} \cdot p_{po} = n_i^2$, where n_i is the intrinsic carrier concentration, then :

$$F\left(\beta\psi_s, \frac{n_{po}}{p_{po}}\right) = \left[\left(e^{-\beta\psi_s} + \beta\psi_s - 1\right) + \left(\frac{n_i}{N_A}\right)^2 \left(e^{\beta\psi_s} - \beta\psi_s - 1\right) \right]^{\frac{1}{2}} \tag{2.6}$$

The space-charge per unit area becomes

$$Q_s = -\epsilon_s E_s = \mp \frac{2\,\epsilon_s\,kT}{q\,L_D} \; F\left(\beta\psi_s, \frac{n_{po}}{p_{po}}\right) \tag{2.7}$$

with the convention that,

$$Q_s > 0, \quad \psi_s < 0$$

and $$Q_s < 0, \quad \psi_s > 0$$

It is possible to evaluate the mobile electron charge which constitutes the inverted surface layer, Q_n, that is ,

$$Q_n = Q_s - Q_B \tag{2.8}$$

where, $$Q_B = -q\,N_A\,x_{dm} \tag{2.9}$$

$$\text{with} \quad x_{dm} = \left(\frac{4 \varepsilon_s \psi_F}{q N_A} \right)^{\frac{1}{2}} \tag{2.10}$$

being the maximum depletion width and ψ_F the Fermi potential.

2.2 (b) Capacitance of an Ideal MOS Structure

If a voltage is applied to the gate of an MOS device with respect to the substrate, some of it will be dropped across the oxide layer and the rest across the surface space-charge layer of semiconductor, that is,

$$V_g = V_{ox} + \psi_s \tag{2.11}$$

The total differential capacitance of the MOS system is given by :

$$C = \frac{d Q_g}{d V_g} = - \frac{d Q_s}{d V_g} \tag{2.12}$$

Substituting Eq (2.11) into Eq (2.12) and re-arranging, yields :

$$C = \frac{C_{ox} C_{sc}}{C_{ox} + C_{sc}} \quad , \tag{2.13}$$

Eq (2.13) shows that the total capacitance of the system is a series combination of the insulator capacitance and the silicon space-charge capacitance, C_{sc} which can be obtained by differentiating Eq (2.7), such that,

$$C_{sc} = \frac{d Q_s}{d \psi_s} \tag{2.14}$$

The oxide capacitance is given by,

$$C_{ox} = \frac{d Q_s}{d V_{ox}} = \frac{\varepsilon_{ox}}{d_{ox}} \qquad F \text{ cm}^{-2} \tag{2.15}$$

Eqs (2.11), (2.13), (2.14) and (2.15) describe the equilibrium capacitance-voltage characteristics of an MOS structure at low frequency, thus being depicted in Fig 2.5 (a).

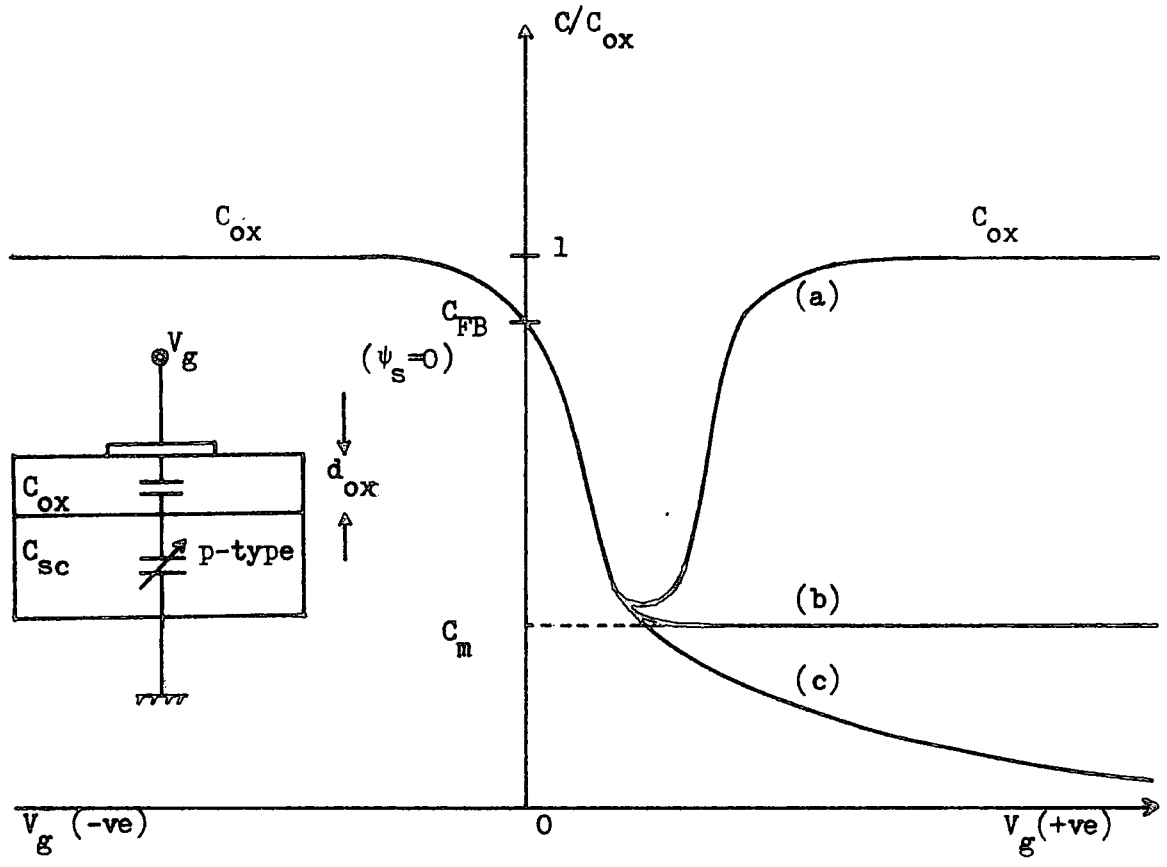


Fig 2.5 : Ideal MOS Capacitance-voltage curves (30)

(a) low-frequency curve

(b) high-frequency curve

(c) deep-depletion curve

The total capacitance at flatband condition (i.e. at $\psi_s = 0$), can be determined from :

$$C_{FB} = \frac{\varepsilon_{ox}}{d_{ox} + \left(\frac{\varepsilon_{ox}}{\varepsilon_s}\right)\left(\frac{kT\,\varepsilon_s}{N_A q^2}\right)^{\frac{1}{2}}} \qquad (2.16)$$

The small-signal capacitance-voltage behaviour of the MOS system can be briefly described as follows. Under a negative gate voltage, holes accumulated at the surface of the semiconductor give rise to a total capacitance with a value close to the oxide capacitance. When a depletion region is formed, as a result of positive voltage at the gate, the total capacitance starts to decrease and reaches a minimum value. With larger positive voltages, it starts to increase again defining the inversion region where the electrons are building up at the semiconductor surface. Again, at strong inversion, the total capacitance will be practically equal to the oxide capacitance.

If the small signal measurement frequency is sufficiently high, such that the electrons (minority carriers) in the inversion region can not follow the a.c., the total capacitance in the inversion region will be practically constant (equal to C_{min}) as shown in Fig 2.5 (b). The small signal capacitance of the space charge region under these high frequency conditions is given by

$$C_{sc} = \left(\frac{q^2\,\varepsilon_s\,N_A}{2\,kT}\right)^{\frac{1}{2}} \frac{1-e^{\beta\psi_s}}{\left(e^{-\beta\psi_s} + \beta\psi_s - 1\right)^{\frac{1}{2}}} \qquad (2.17)$$

The gate voltage is related to surface potential as in Eq (2.11). From Eqs 2.11 and 2.17, it is possible to obtain the high-frequency C-V curve (Fig 2.5 (b)).

If it is assumed that strong inversion begins at a surface potential, $\psi_s \simeq 2\psi_F$, the corresponding gate voltage is :

$$V_g = -\frac{Q_s}{C_{ox}} + 2\psi_F \qquad (2.18)$$

where $$\psi_F = \frac{kT}{q} \ln (N_A/n_i) \qquad (2.19)$$

The total capacitance which corresponds to this condition can be written as :

$$C_m = \frac{\varepsilon_{ox}}{d_{ox} + \left(\frac{\varepsilon_{ox}}{\varepsilon_s}\right) x_{dm}} \qquad (2.20)$$

where x_{dm} is given by Eq (2.10). From Eq (2.20), the doping density N_A can be determined by knowing C_m from the high frequency C-V measurement.

When the voltage sweep applied to the gate is relatively fast, the electrons (minority carriers) will not have enough time to accumulate at the surface. As a result, the total capacitance will be lower than C_m, as illustrated in Fig 2.5(c). This is due to the fact that in curve (c) the depletion layer extends further into the semiconductor and constitutes the deep depletion condition. The experimental evidence of the difference between curve (b) and curve (c) was first shown by Zaininger & Heimans(33), as the rate of sweep was varied.

2.3 Experimental MOS Characteristics

Measurements on actual MOS capacitors show that various factors or phenomena associated with the structure perturb the predicted ideal C-V characteristics. These factors include : metal-semiconductor work-function difference, surface states or interface-states at the silicon dioxide-silicon interface and also the charge within the oxide layer.

(a) Effect of work-function difference and fixed oxide charge :

It has been shown (34) that in the Al-SiO_2-Si structure at thermal equilibrium and zero gate voltage, the surface of n-type silicon is already accumulated. On the other hand, the surface of p-type silicon is inverted. This is true even for oxide and interface charges assumed to be zero. The amount of gate voltage needed to bring the energy band diagram to the flatband condition is defined as the flatband voltage, V_{FB}. In this case, it will be equal to the metal-semiconductor work-function difference, ϕ_{ms}. The different values of V_{FB} obtained experimentally by using various metals such as Mg, Ni, Cu, Au, Ag, has been considered by Deal et al (34). The dependence of work-function difference upon the doping concentration of the semiconductor has also been shown.

If a fixed charge density Q_{fc} exists at the oxide-semiconductor interface (fixed oxide charge), then :

$$V_{FB} = - \frac{Q_{fc}}{C_{ox}} + \phi_{ms} \qquad (2.21)$$

Equation (2.21) shows that the equations obtained for the ideal MOS structure can be used if V_g is replaced by an effective gate voltage V_g°, such that

$$V_g^{\circ} = V_g - V_{FB} \qquad (2.22)$$

Another effect on voltage flatband arises from distributed charge within the oxide. This will modify the voltage flatband such that :

$$V_{FB} = -\frac{Q_{fc}}{C_{ox}} + \phi_{ms} - \frac{1}{C_{ox}} \int_{o}^{d_{ox}} \frac{x'}{d_{ox}} \rho'(x') \, dx' \qquad (2.23)$$

where $\rho'(x')$ is charge density distrubuted in the oxide with x' indicating distance from the metal.

The expression given above can be simplified by considering the interface fixed charge and the distributed charge within the oxide as an equivalent interface fixed charge, so that,

$$V_{FB} = -\frac{(Q_{fc})_{equiv}}{C_{ox}} + \phi_{ms} \qquad (2.24)$$

Equation (2.24) shows that if the flatband voltage, ϕ_{ms} and C_{ox} are known, then $(Q_{fc})_{equiv}$ can be evaluated (32). Values of $(Q_{fc})_{equiv}$ of about $10^{10} - 10^{11}$ charges per cm^2 are quite common, the magnitude being strongly dependent on the final heat treatment that the device received (3).

(b) Effect of mobile charge within the oxide

During the fabrication process, the system is normally subjected to ionic contamination, particularly by sodium which is easily incorporated in SiO_2 as Na^+ (4). Upon applying a bias to the device, sodium ions will be forced to move. This means that Eq (2.24) will be a function of time. However, the drift of voltage flatband caused by this effect can be negligible, once a good controlled surface is achieved.

(c) Effect of fast surface states or interface-states

At any crystal surface, there is a discontinuity in the periodicity of the lattice. This disruption results in the introduction of energy levels or states within the semiconductor bandgap at the surface. The number of such states depends on the surface treatment during processing. Shockley (1) predicted an interface-state density of the order of 10^{15} cm^{-2} for an atomically clean surface. However, the formation of an oxide layer tends to reduce the actual interface-state density found at a clean silicon dioxide-silicon interface. The number of such states on a well prepared surface can be less than 10^{10} per cm^2 ; whereas for poorly prepared surfaces, they may reach over 10^{13} per cm^2 (32).

The important property of these states is their ability to exchange charge very readily with the valence band and conduction band of the semiconductor. The interface-states are considered to be donor-type, that is, those situated above the Fermi level are empty, and hence positively charged, whereas those below the Fermi level are full of electrons and neutral. When a gate voltage is applied, the interface state levels will move up or down with the valence and conduction band edges while the Fermi level remains fixed, as illustrated in Fig 2.6. This means that the charge condition of the interface states can be raised. This change results in a further alteration of the ideal MOS C-V curve. The early observations of this effect were made on experimental high frequency C-V curves, Fig 2.7 (32), where a distorted characteristic is very obvious.

The effect of the interface-states on the C-V curve can be understood by considering their density designated as N_{ss} per cm^2. These states are charged and discharged as the voltage is varied. For a MOS structure with oxide thickness d_{ox} of 1000 Å and interface-

state density N_{ss} of 10^{12} per cm^2, the extra voltage required to do this is :

$$V_{ss} = \frac{Q_{ss}}{C_{ox}} = \frac{q\,N_{ss}}{\varepsilon_{ox}/d_{ox}} = 4.7 \text{ volts},$$

which will result in significant displacement along the voltage axis of the C-V curve. However, if N_{ss} is reduced to as low as 10^9 per cm^2, the displacement will be almost negligible. Further consideration of the effect of interface-states on the C-V curves will be given in the next section.

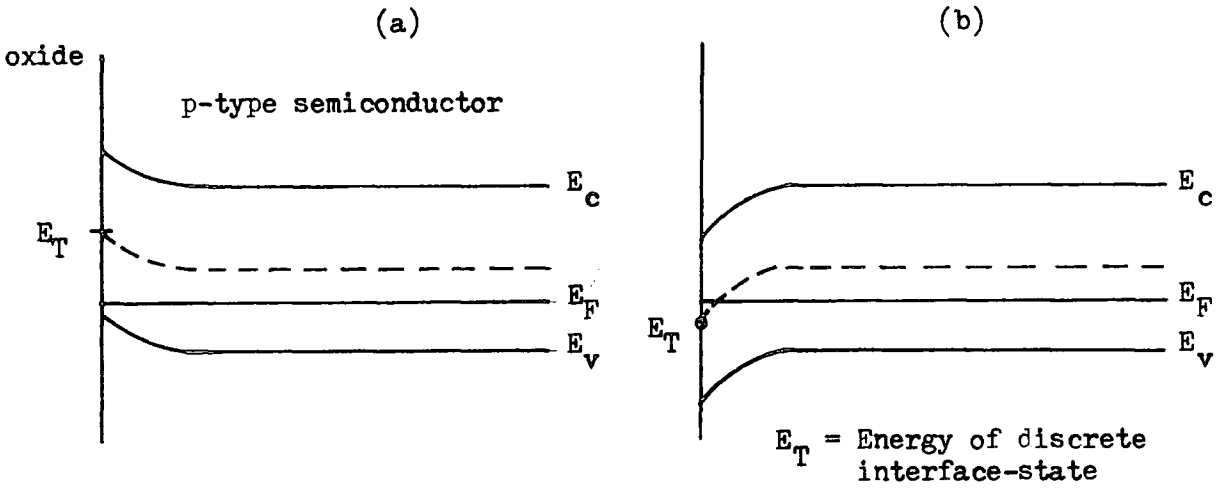


Fig 2.6 : Illustration of interface-states behaviour as surface potential is varied.

(a) surface accumulated :- state unoccupied.
(b) surface inverted :- state occupied.

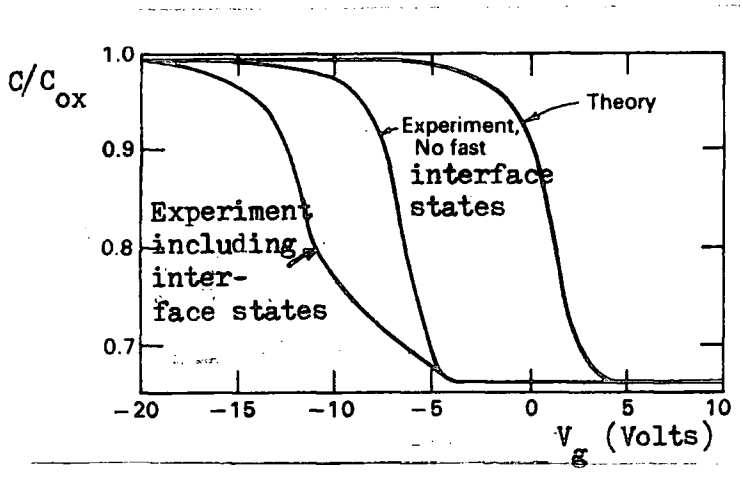


Fig 2.7 : The effect of interface-states on the h.f. capacitance-voltage characteristics of an MOS capacitor.

2.4 Interface-State Evaluation

Early methods used to evaluate the interface-states density of MOS devices utilized the high-frequency C-V characteristics (8). These methods are based on the comparison between the experimental and theoretical C-V curves. The interface-state cause a shift ΔV along the voltage axis of the C-V curve, the value of which is measured as a function of surface potential. This yields the total charge in the surface states at any particular surface potential, that is :

$$Q_{ss} = C_{ox} (\Delta V) \quad \text{Coul}/\text{cm}^2 \tag{2.25}$$

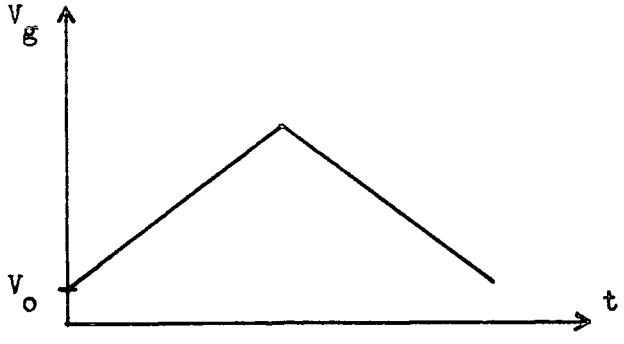
The interface-state density per unit energy is then evaluated by numerical or graphical differentiation:

$$N_{ss} = \frac{1}{q} \left(\frac{\partial Q_{ss}}{\partial \psi_s} \right) = \frac{C_{ox}}{q} \left(\frac{\partial \Delta V}{\partial \psi_s} \right) \text{ states/cm}^2\text{/eV} \tag{2.26}$$

This technique was shown to be successful for measuring very large surface state densities (greater than 10^{10} per cm^2 per eV). However, the method becomes inaccurate for lower surface state densities (35).

The low-frequency or quasi-static C-V technique provides an alternative method for evaluating interface-state densities (14,15). Basically, the method consists of applying a slow ramp voltage to the MOS capacitor, the resultant displacement current being measured using an electrometer amplifier.

By considering the applied voltage waveform to be :



$$V_g = V_o + \alpha t \tag{2.27}$$

where α = voltage sweep rate, then the instantaneous displacement current as a function of gate voltage can be written as :

$$I = \frac{dQ_g}{dt} = \frac{dQ_g}{dV_g} \cdot \frac{dV_g}{dt} = \alpha C(V_g) \tag{2.28}$$

where $C(V_g) = \frac{dQ_g}{dV_g}$ is the quasi-static total differential capacitance of the device. This provides an elegant way of measuring the device capacitance.

The total MOS capacitance obtained from the quasi-static measurement can then be expressed as (see Fig 2.8) :

$$\frac{1}{C(V_g)} = \frac{1}{C_{ox}} + \frac{1}{C_{sc}(\psi_s) + C_{ss}(\psi_s)} \tag{2.29}$$

where $C_{ss}(\psi_s)$ is the interface-state capacitance (a function of surface potential). Using Eq (2.29), the interface-state density can be evaluated from :

$$N_{ss}(\psi_s) = \frac{C_{ss}(\psi_s)}{q} = \frac{1}{q}\left[\frac{C(V_g)}{1 - \frac{C(V_g)}{C_{ox}}} - C_{sc}(\psi_s)\right] \tag{2.30}$$

From Eq (2.30) it is obvious that in order to evaluate N_{ss}, it is necessary to know the relationship between gate voltage V_g and surface potential ψ_s. The overall procedure for obtaining the distribution of the interface-state density is therefore as follows :

(a) The ideal $C(\psi_s)$ curves are generated using the known gate area, oxide capacitance and doping density of the MOS device.

(b) The experimental $\frac{C}{C_{ox}}$ vs. V_g curve is integrated to determine the surface potential as a function of gate voltage, using Berglund's integration :

$$\psi_s(V_g) = \int_{V_a}^{V_g} \left[1 - \frac{C(V_g)}{C_{ox}}\right] dV_g + \Delta \tag{2.31}$$

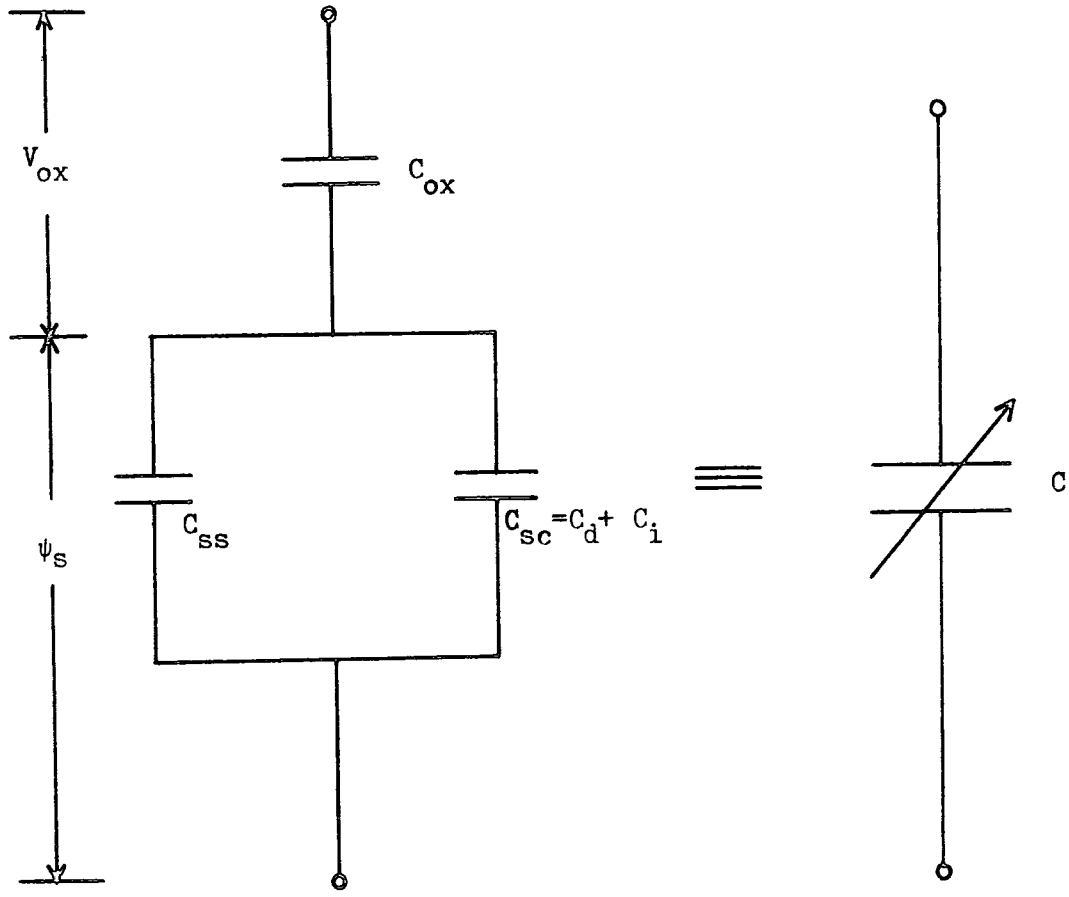


Fig 2.8 : Simplified equivalent circuit of the MOS capacitor showing the capacitance due to interface-states, C_{ss}.

where V_a is the chosen gate voltage at the initial limit of integration, and Δ is an additive constant, which can be determined either by comparison with the ideal curve or by use of a suitably chosen value of V_a (usually the flat-band voltage, V_{FB}, in which case $\Delta = 0$). A plot of $\psi_s - V_g$ can in fact be obtained directly by using special circuits which will be described in detail in the next chapter.

(c) The experimental normalized capacitance (C/C_{ox}) as a function of the experimentally determined surface potential can then be plotted. Comparison can be made with theoretically generated curves obtained from the ideal MOS structure.

(d) A plot of semiconductor surface capacitance at each value of surface potential can be constructed for both the experimental and theoretical cases. Using Eq (2.30), the surface state density can then be determined directly.

As mentioned earlier, the valence and conduction bands move up or down as determined by the gate voltage. By assuming that the interface states are confined to a continuum of discrete levels in the band gap, it is possible to determine the distribution of interface-states within the energy gap. From Fig 2.9 the interface state levels can be written with respect to the conduction band edge as :

$$E_T - E_c = \frac{E_g}{2} + q\psi_F - q\left|\psi_s\right| \qquad (2.32)$$

where $E_g = 1.11$ eV and ψ_F is given by Eq (2.19).

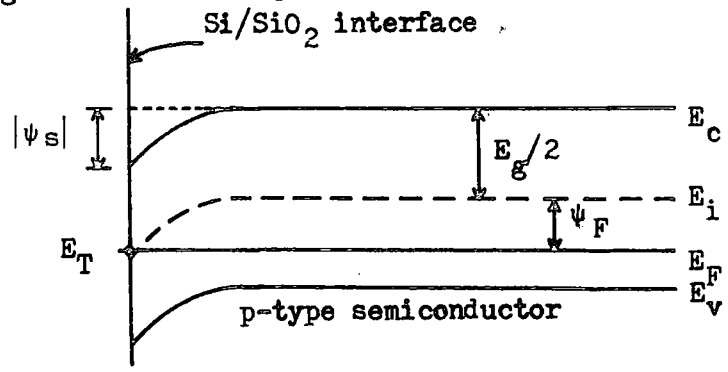


Fig 2.9 : Position of a single discrete interface-state level within the band gap as a function of surface potential.

2.5 Experimental Measurements of Interface-State Density

The method described in the previous section has been used to determine the interface state density from experimental measurements. Two types of MOS capacitor were used in these experiments, with the following specification :

(i) n-type substrate : [☆]

< 100> orientation, oxide thickness ~ 1000 Å ,

gate diameter of Al ~ 1 mm, gold substrate contact.

(ii)p-type substrate : [☆ ☆]

< 100> orientation, oxide thickness ~ 745 Å ,

gate diameter of Al ~ 1.54 mm, aluminium substrate contact.

2.5 (a) Experimental details :

The experimental set-up used for these measurements is shown in Fig. 2.10. The high-frequency C-V measurements were made using an analogue C-V plotter which had been built in the department (37). This instrument allows an a.c. signal of 100 mV (rms) to be superimposed on a d.c. bias which is then applied to the sample. The output from this bridge, proportional to capacitance, is directly connected to a Bryans X-Y plotter. The instrument was calibrated using standard capacitors. The lowest voltage sweep rate (26 mV/sec) which can be derived from the triangle generator (supplying the d.c. bais to the bridge) was found to be slow enough to maintain equilibrium in the devices used.

The sample was housed in an electrically and optically shielded probe chamber. The vacuum chuck (plinth) supporting the sample was made of stainless steel ensuring a good electrical contact between the substrate contact of the device and the plinth itself. The probe contact to the metal gate of the device was adjusted manually with the help of a binocular microscope.

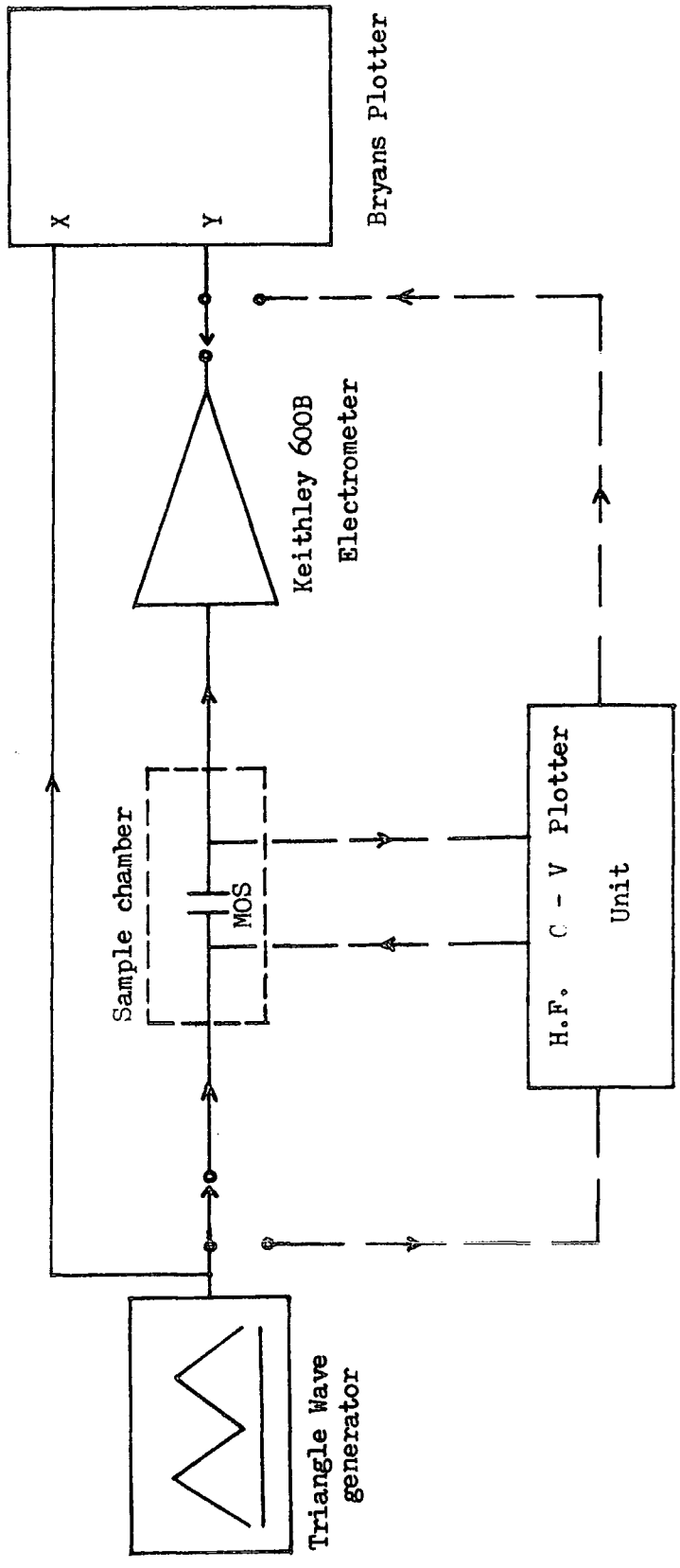


Fig 2.10 : Measurement set-up for slow ramp I-V and high frequency C-V.

The method of Kuhn (14) has been used in order to obtain the low-frequency quasi-static I-V measurements. A very low frequency triangular voltage waveform was applied to the sample and the displacement current measured using a Keithley 600B Electrometer. Typical current magnitudes for this kind of measurement lies in the range 10^{-12} - 10^{-11} Amp. The output voltage (which is proportional to the input current) from the electrometer together with the voltage sweep from the triangle generator were fed to the X-Y plotter as vertical and horizontal inputs, respectively.

2.5 (b) Experimental precautions :

Since the magnitude of the measured current is very low, several precautions have to be taken. All of the connecting leads are well shielded against electrical and mechanical disturbance (usually short screened cables and 'BNC' connectors). The triangular voltage waveform generator and electrometer were battery driven in order to avoid mains frequency pick-up problems.

The chamber containing the device was flushed with dry nitrogen in order to avoid condensation of water on the surface of the sample. The sample plinth was regularly cleaned with iso-prophyl alcohol in order to remove grease, etc, and ensure a low resistance substrate connection.

[*], [* *] Supplied by Dr. A.G.Nassibian from the University of Western Australia and by the University of Edinburgh.

2.6 N-type MOS Results and Analysis

The high-frequency C-V and quasi-static I-V measurements made using the technique described above, were analysed to give the interface-state density by the method given in section 2.4. This section describes the results and analysis for the n-type sample.

2.6 (a) High-frequency C-V curve

Fig 2.11 shows the high-frequency C-V curve obtained for the n-type MOS device. The oxide capacitance can be determined from the strong accumulation region (since for $V_g >> 0$ the semiconductor capacitance, C_{sc} is much greater than oxide capacitance, C_{ox}), the value being measured as 268 pF. From Eq (2.15), the oxide thickness is calculated to be 1009 Å.

The same curve, gives a value of minimum capacitance of 60 pF. Using the equations which relate the minimum capacitance to doping density (as presented in section 2.2), yields the value of the doping density N_D of 6×10^{14} cm^{-3}.

The flatband voltage, V_{FB} was determined as -0.72 V using Eq 2.16 for C_{FB} , and the experimental C-V curve. From Sze (31), the metal-semiconductor work-function difference, ϕ_{ms} of the device considered is -0.36 volts. Thus, the total shift of V_{FB} due to oxide and interface charges is $(-0.72 + 0.36) = -0.36$ volts, which yields the equivalent interface charge of only $0.36.C_{ox}/q = 7.5 \times 10^{10} cm^{-2}$.

The ~~ideal~~ theoretical high-frequency C-V characteristics was generated using the values of V_{FB}, N_D, area A and oxide capacitance, C_{ox} as obtained from the experimental data. The theoretical curve is shown dotted in Fig 2.11 and the computer data used to generate this curve is tabulated in Appendix A.

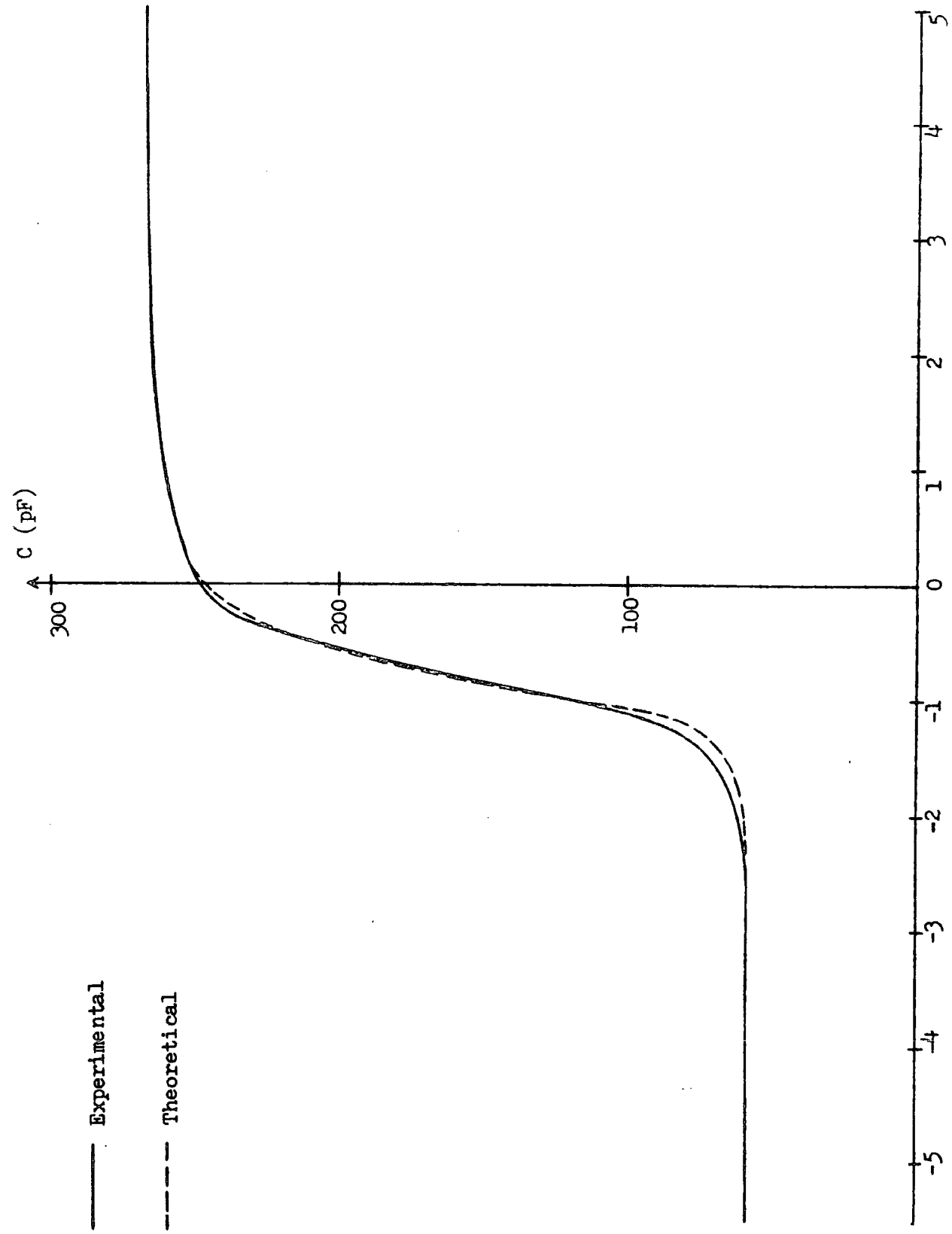


Fig 2.11 : High-frequency C-V curves of n-type MOS Capacitor

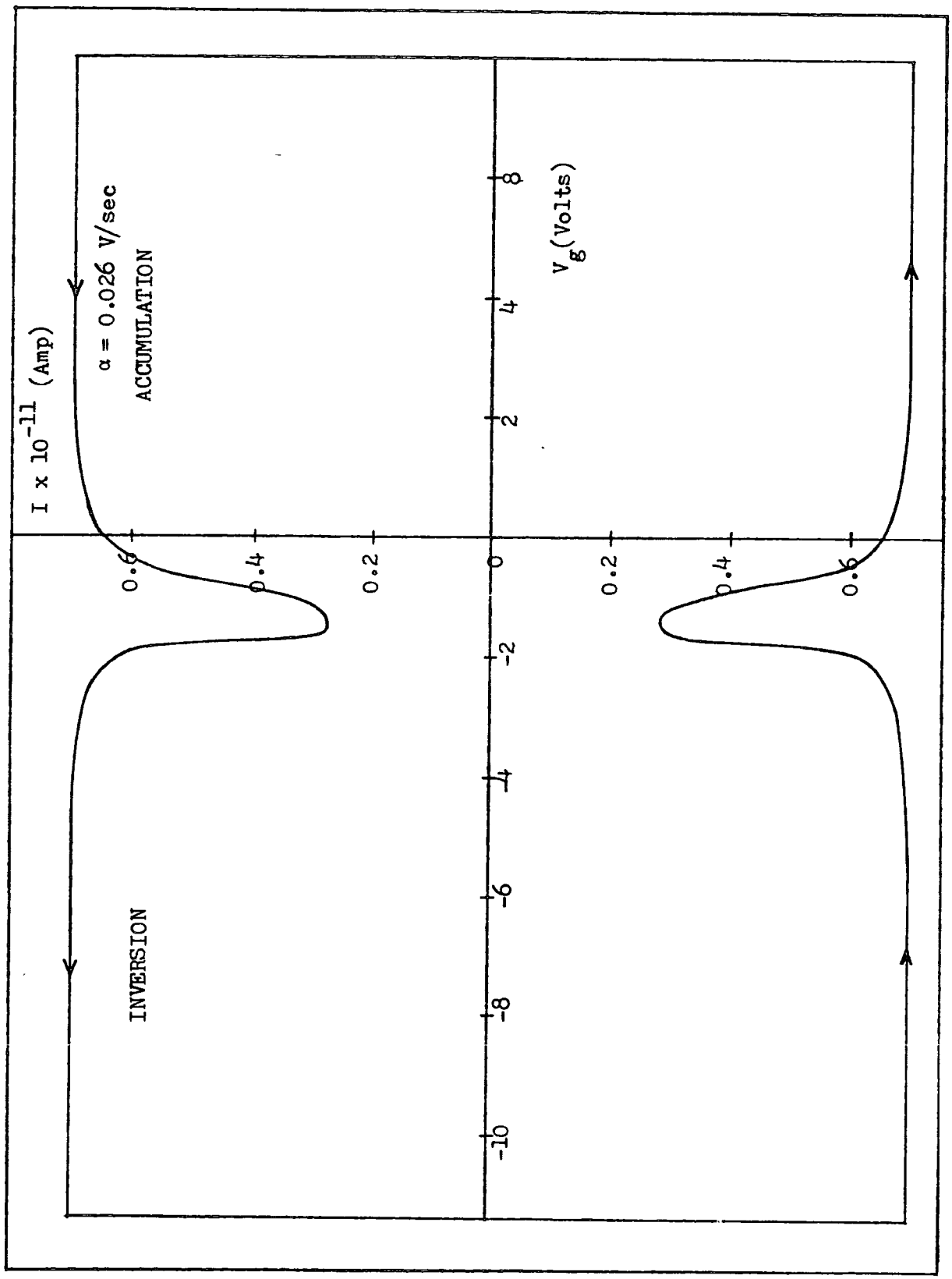


Fig 2.12 : Quasi-static I-V curve of n-type MOS Capacitor

2.6 (b) Quasi-static I-V curve

Fig 2.12 shows the quasi-static curve obtained for the device under consideration. We can be sure that we have equilibrium maintained throughout the entire voltage sweep because of the symmetry of the characteristics about the voltage axis. The curve was generated at room temperature using a voltage sweep rate, α = 0.026 V/sec. The oxide capacitance, C_{ox} was determined to be 269 pF from the current obtained in strong accumulation, that is, $C_{ox} = I_o/\alpha$, where I_o is the current measured in strong accumulation. This value of C_{ox} is in very good agreement with the value of 268 pF obtained from the high frequency measurement .

The experimental surface potential-gate voltage relationship was obtained using the direct plotting instrumentation developed which will be described in the next chapter. This enables the total normalised capacitance and the surface capacitance, Figures 2.13 and 2.14 to be generated from the experimental quasi-equilibrium I-V curve as a function of surface potential. The theoretical curves in the figures were generated using the equations given in section 2.2. The data obtained from a computer program is shown in Appendix A.

The interface state density was extracted from Fig 2.14 (i.e. the difference between the two curves, divided by the electronic charge). The plot of interface state density as a function of position in the band gap is shown in Fig 2.15. It shows that the density is of the order of 4.5×10^{10} cm^{-2} eV^{-1} near midgap and rising toward the band-edges.

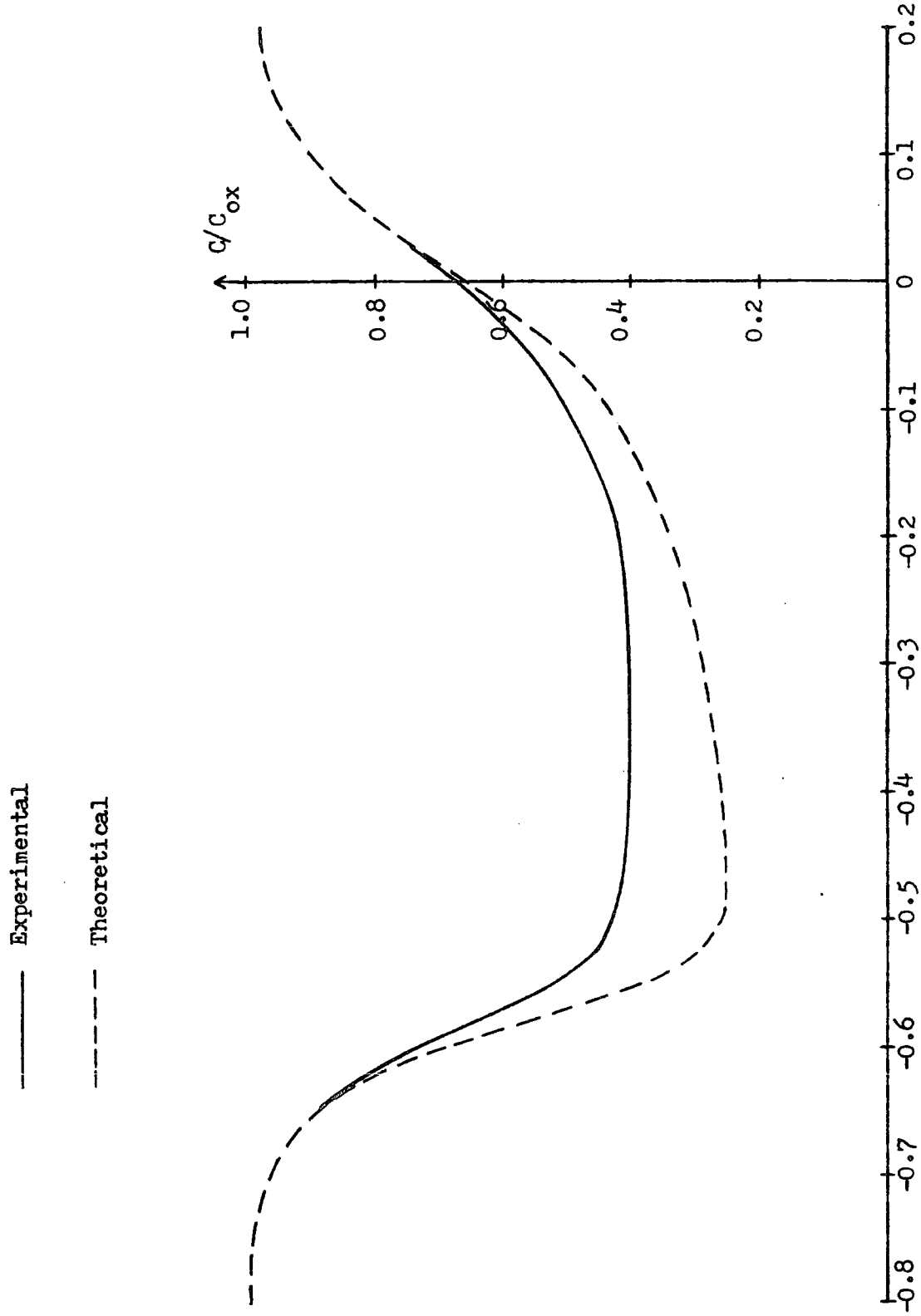


Fig 2.13 : Normalized capacitance as a function of surface potential.

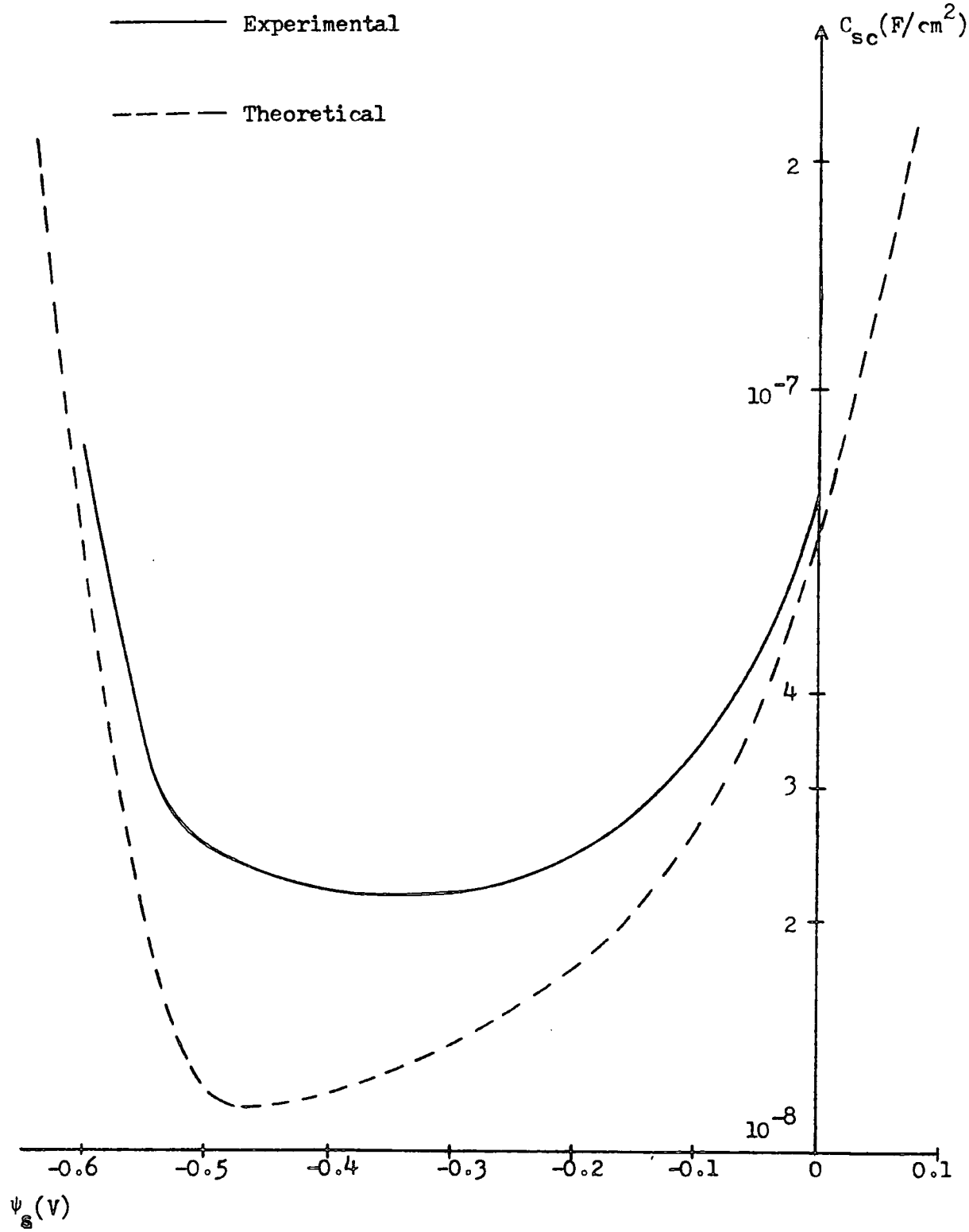


Fig 2.14 : Surface capacitance as a function of surface potential.

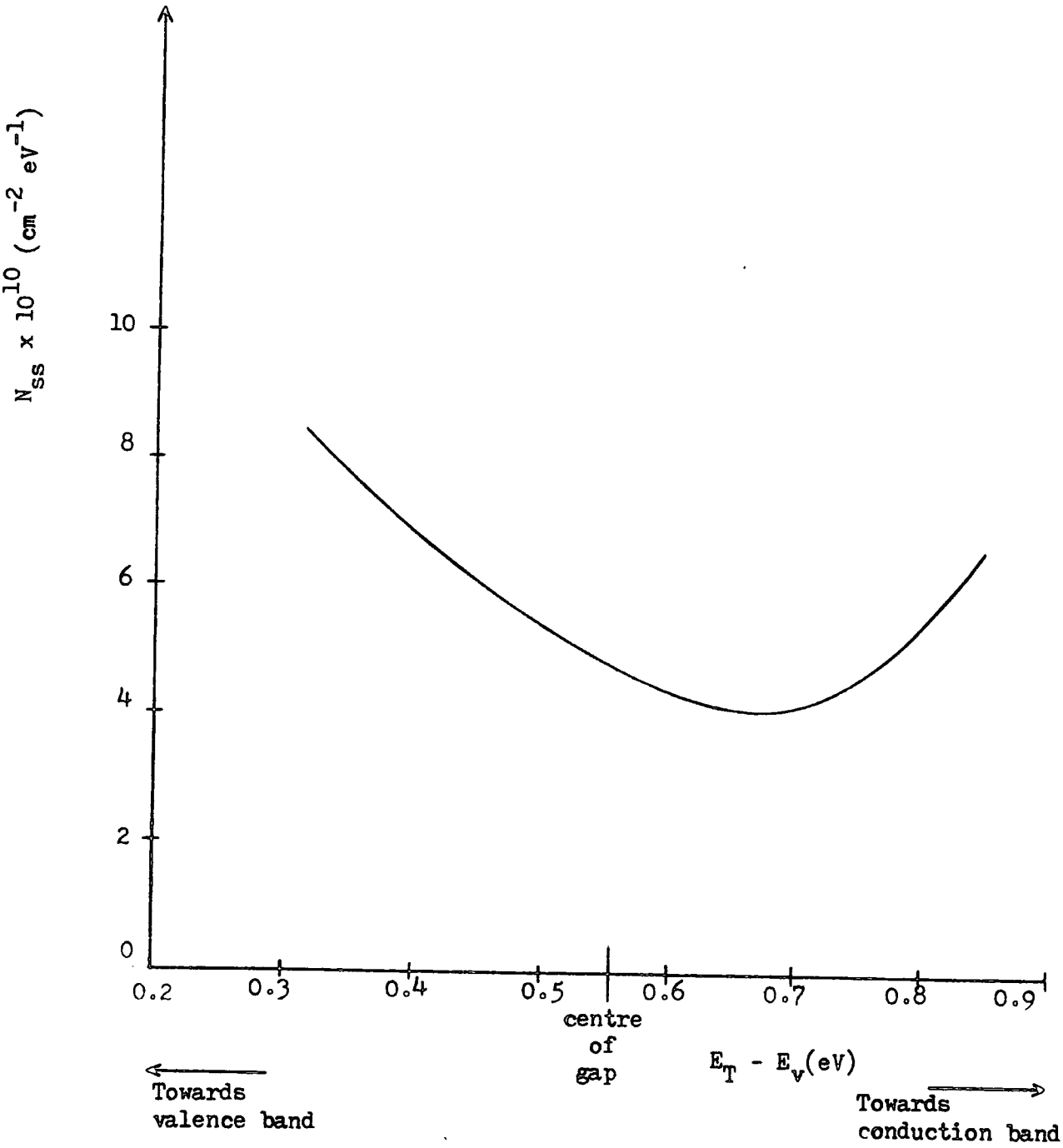


Fig 2.15 : Interface states density distribution obtained for n-type MOS capacitor.

2.7 P-Type MOS Results and Analysis

The high frequency C-V curve obtained for the p-type sample is shown in Fig 2.16. The oxide capacitance is seen to be 850 pF, yielding an oxide thickness of 745 Å . The minimum capacitance is 153 pF, giving a doping density N_A of 7.0×10^{14} cm^{-3}.

From the experimental curve the flatband voltage was determined to be equal to -0.96 volts using Eq (2.16). Using the metal-semiconductor work-function difference, ϕ_{ms} = -0.86 volts, the effective total interface charge density at flatband is found to be 2.8×10^{10} cm^{-2}, which is very low. It is therefore not surprising that there is a close correlation between the experimental and theoretical curve (dotted curve in Fig 2.16) is seen. The data for the theoretical curve is tabulated in Appendix B.

Fig 2.17 shows the experimental I-V curve obtained using the quasi-static method. The curve shows symmetry about the voltage axis, indicating again that the device is in equilibrium. The curve was generated at room temperature with a voltage sweep rate, α of 0.026 V/sec. The current was 2.25×10^{-11} Amp at strong accumulation and strong inversion, yielding an oxide capacitance of 865.4 pF. This value is found to be in quite good agreement with the value of 850 pF obtained from the high-frequency C-V measurement. Figure 2.18 shows the normalised total capacitance as a function of surface potential for both experiment and theory, (the data for the theoretical curve is tabulated in Appendix B). The capacitance of the semiconductor surface is plotted against surface potential in Fig.2.19.

The interface-state density distribution is obtained from Fig 2.19 by noting the difference between the experimental and theoretical curves. Fig 2.20 shows the resulting interface-state density as a function of position in the band gap. The minimum value of interface-state density of the order of 2.5×10^{10} cm^{-2} eV^{-1} is again observed to be near midgap.

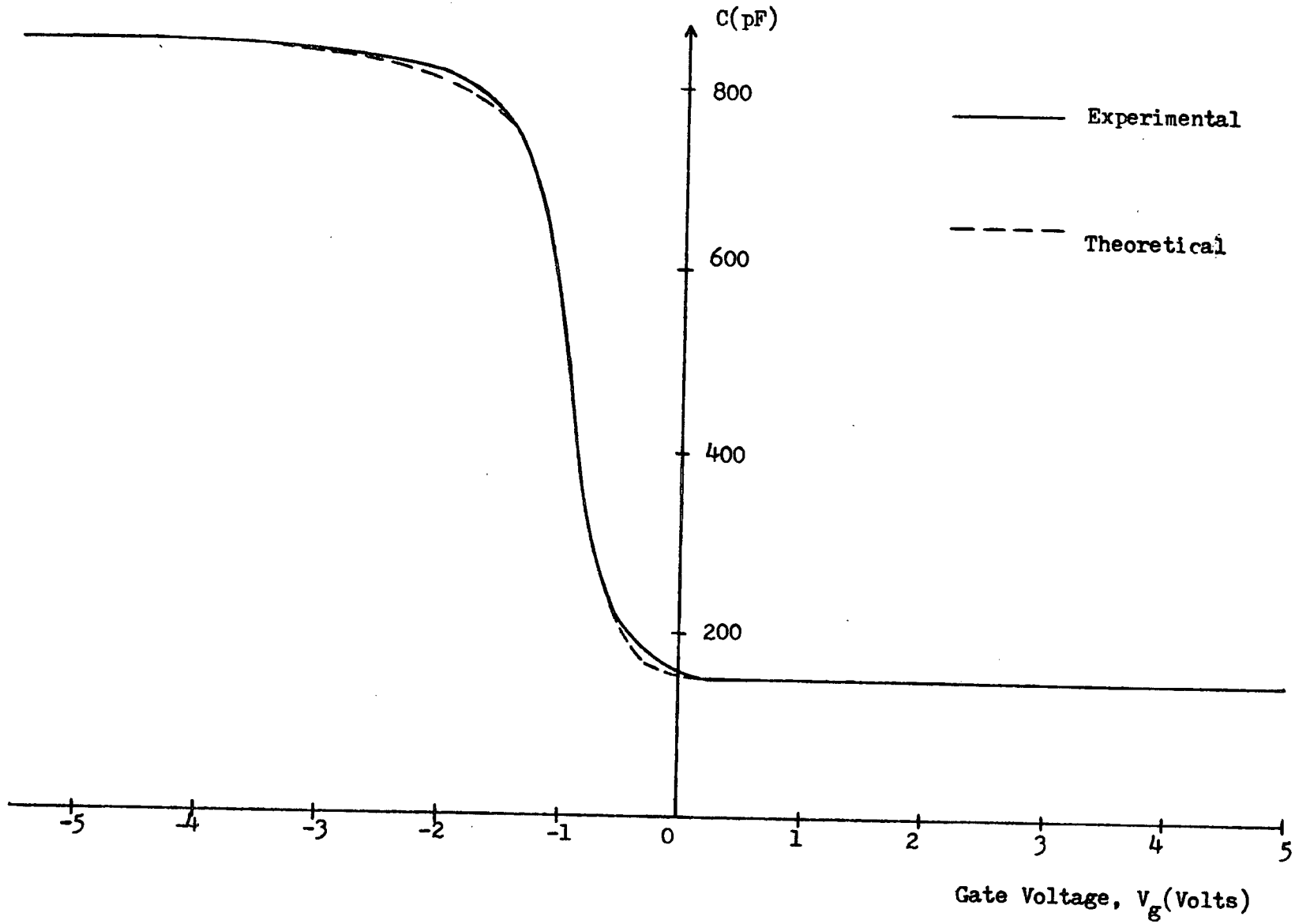


Fig 2.16 : High-frequency C-V curves of p-type MOS capacitor

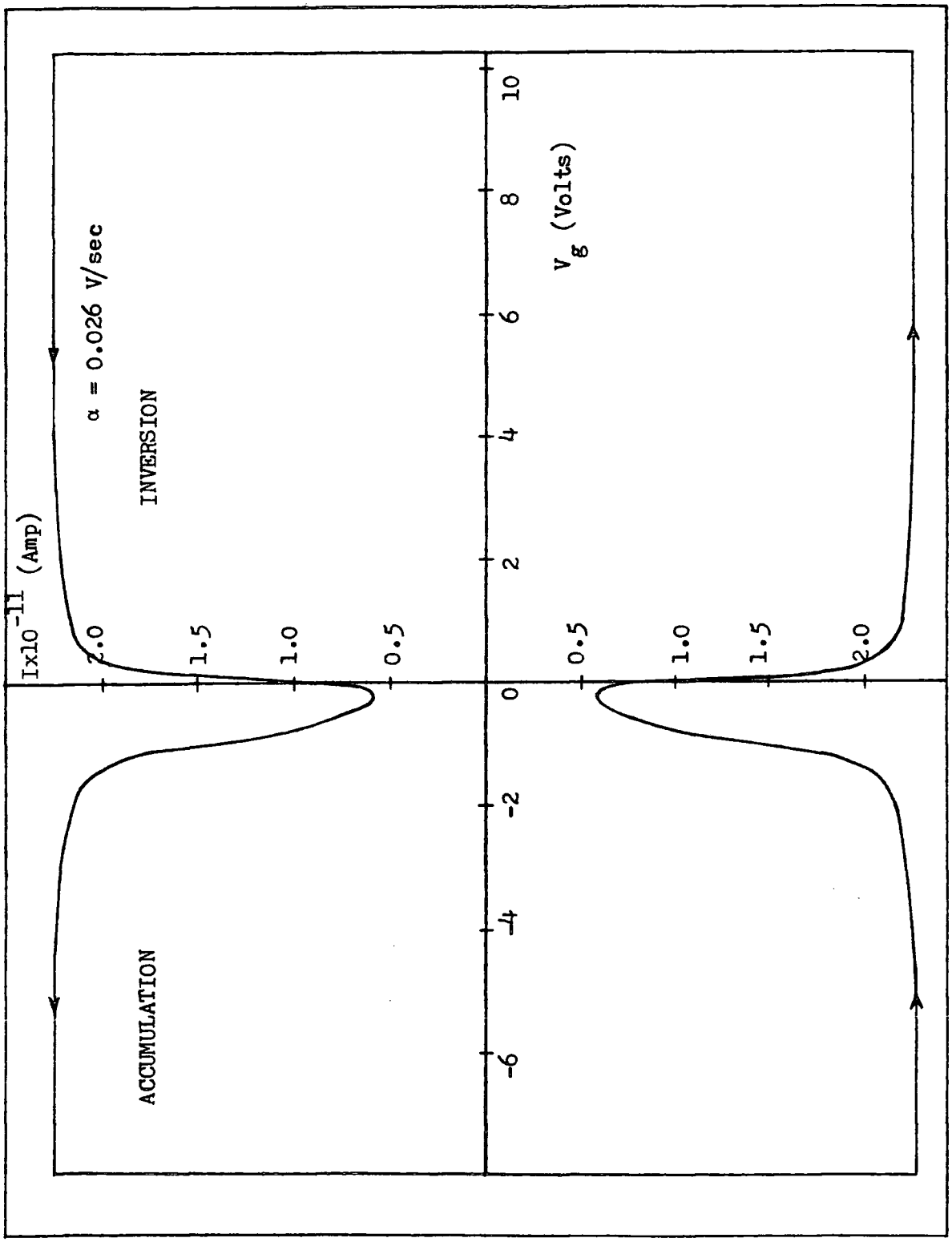


Fig 2.17 : Quasi-static I-V curve of p-type MOS capacitor

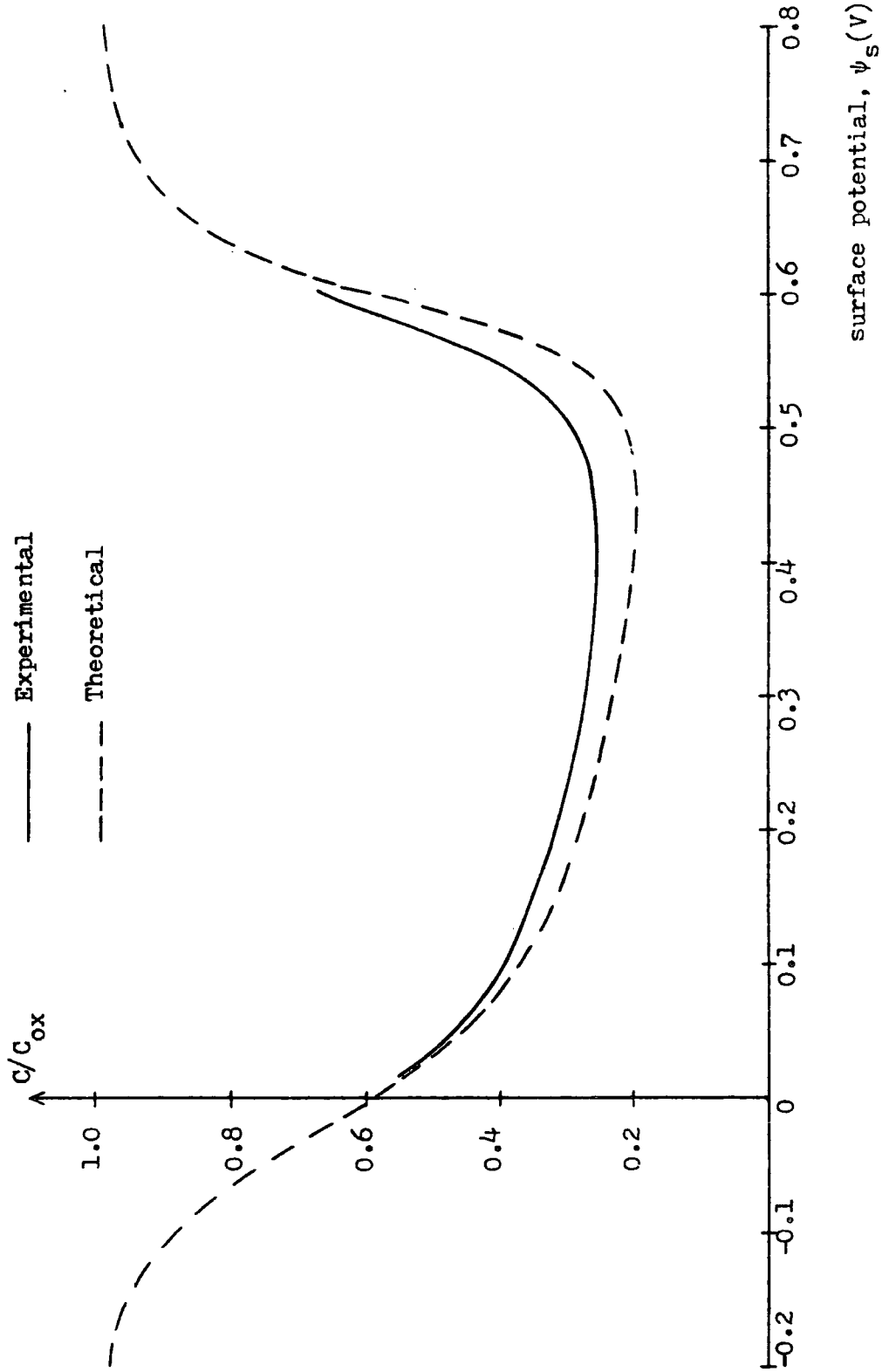


Fig 2.18 : Normalized capacitance as a function of surface potential.

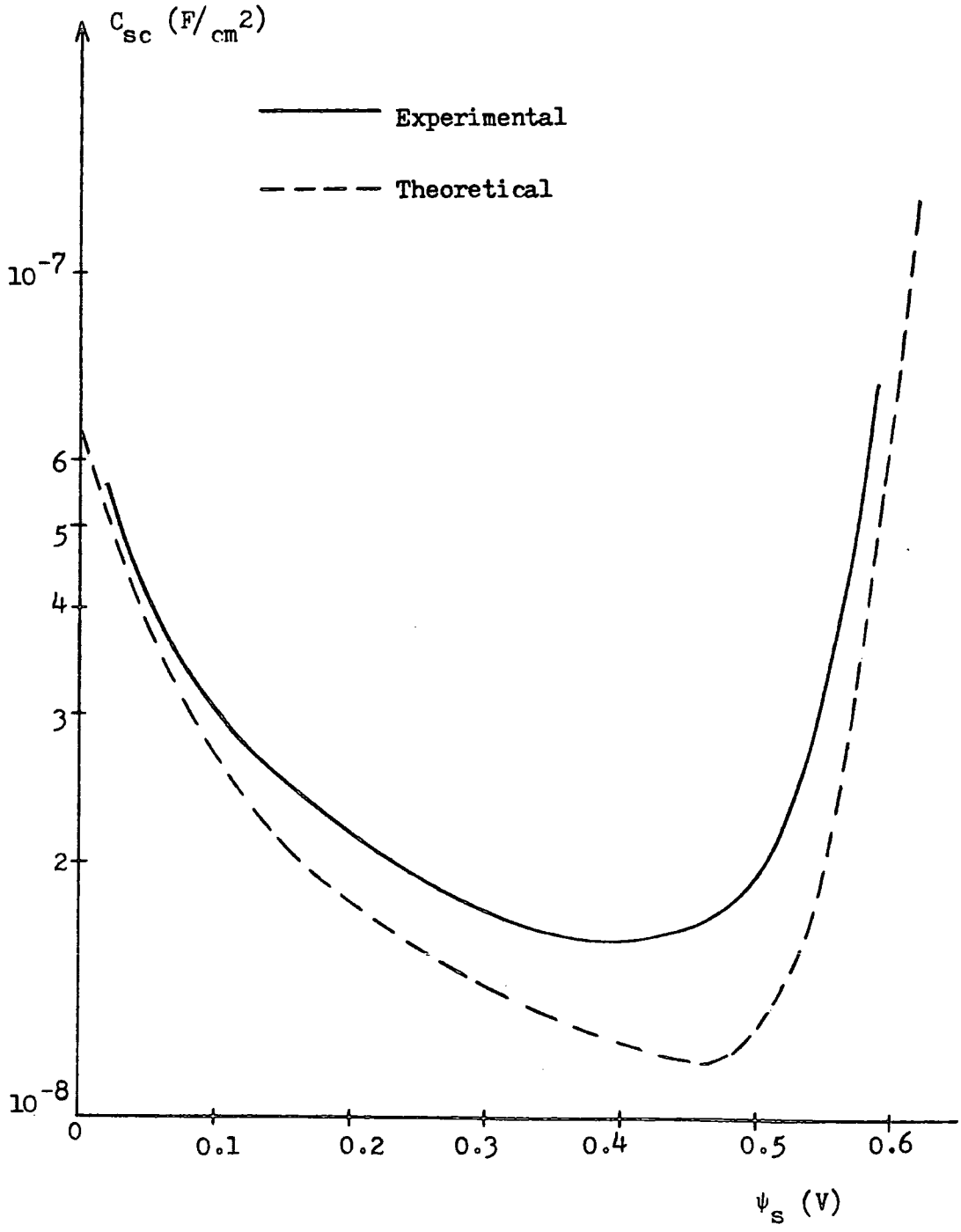


Fig 2.19 : Surface capacitance as a function of surface potential.

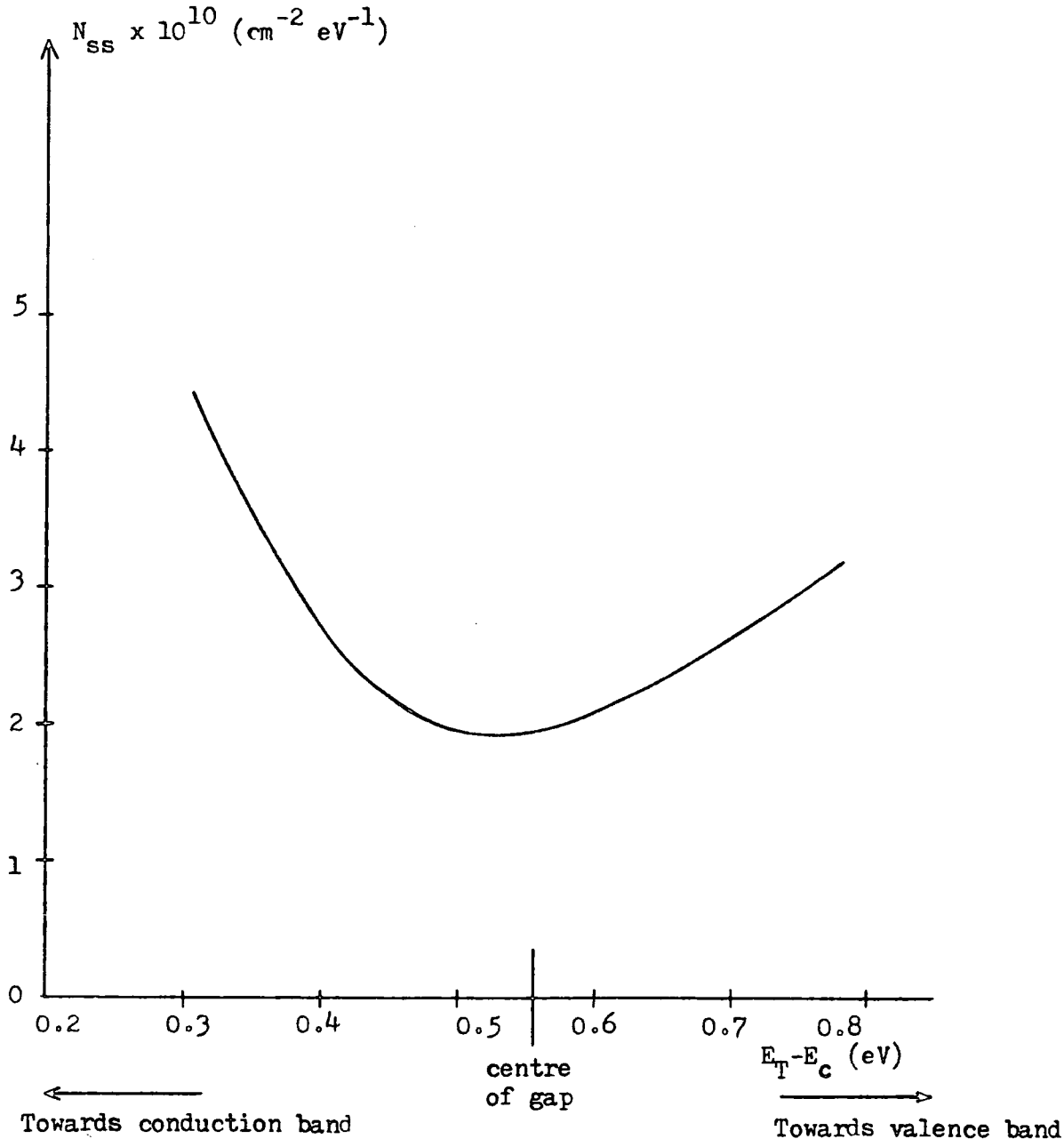


Fig 2.20 : Interface states density distribution obtained for p-type MOS capacitor.

2.8 Discussion

The experimental section of this chapter has been concerned with the calculation of the interface-state density distribution for both n and p-type MOS capacitors. One of the major sources of error which would affect the interface-state density calculation is the determination of surface potential as a function of gate voltage. This effect can be understood by realising that, in strong inversion at least a small change in surface potential will cause a substantial change in gate voltage. Thus, it would be possible to obtain a value of surface capacitance at a grossly incorrect gate voltage. The non-uniform nature of surface potential can also influence the calculation of N_{ss} (35).

The minimum interface-state densities obtained for the capacitors used are quite low, of the order of 4.5×10^{10} cm^{-2} eV^{-1} (n-type) and 2.5×10^{10} cm^{-2} eV^{-1} (p-type). At such values the differences between experimental and ideal curves are very small (e.g. Fig 2.11 and 2.16) and this limits the accuracy of this method of measurement. In the present case the values may have an absolute accuracy at only $\pm$ 50%, although this does not invalidate the method. On the contrary, it can be argued that low values of interface-state density are of limited practical importance and that accuracy is not then required. The method used has the advantages of simplicity and low cost compared with more sensitive methods (e.g. G-f-V, DLTS) which have been developed more recently.

CHAPTER 3

NON-EQUILIBRIUM MEASUREMENTS AND ANALYSIS

3.1 Introduction

In contrast to the subject of the second chapter, where the device is maintained in quasi-equilibrium conditions with the bias voltage,here, we shall consider the non-equilibrium case. In this condition the carrier densities are well above or below the thermal equilibrium values corresponding to the instantaneous bias voltage. The necessity for understanding non-equilibrium behaviour is due to the fact that charge coupled devices are operated in this manner.

The method used here to study the non-equilibrium behaviour is based on work performed by Board and Simmons (29). It consists of applying a triangular gate voltage to an MOS capacitor of sufficiently high frequency to drive the device into non-equilibrium. The various sections of the experimental current-voltage curves obtained in these conditions were found to fit well with the proposed theory. The results obtained were then analysed to give the generation lifetime of the silicon.

An experimental circuit was built to measure the surface potential as required for analysing the non-equilibrium results. The circuit which was first described by Tonner and Simmons(36) can be used to obtain directly the surface potential-gate voltage relationship under either quasi-equilibrium or non-equilibrium conditions. The resulting curves were compared with those obtained by graphical integration.

3.2 Theory of the MOS Capacitor in Non-Equilibrium

3.2 (a) Generation-recombination centres (traps)

The conditions for non-equilibrium phenomena to occur in a semiconductor can be realised by applying an external energy source for example, radiation or electric field. In the case of applying a light source, some electrons are raised to the conduction band and excess carriers are generated. As the source is turned off, carrier generation ceases and the excess concentration decays back to the original equilibrium conditions by means of recombinations. From observed values of lifetime of these carriers in silicon it becomes clear that direct recombination from band to band is insignificant in practice. Schokley and Read and Hall (5) proposed that the generation/recombination mechanism involve transitions via intermediate energy levels lying within the forbidden energy gap. These energy levels may arise from a variety of causes, including the existence of unwanted impurities in the crystal or the presence of lattice imperfections. Using Schockley-Hall-Read statistics (5) , the bulk generation-recombination rate of a single level trap at an energy E_t above the valence band is given by

$$U = \frac{\sigma v_{th} N_t (pn - n_i^2)}{n + p + 2n_i \cosh\left(\frac{E_t - E_i}{kT}\right)} \qquad (3.1)$$

where N_t is the bulk trap density, v_{th} is the thermal velocity of carriers and σ is the capture cross-section (which is taken to be the same for holes and electrons). Under thermal equilibrium $pn = n_i^2$ resulting in $U = 0$ (no net rate of generation-recombination). Also U can be interpreted as the recombination rate when it is positive and as the generation rate when it is negative in value.

Equation (3.1) provides the most important aspect of the Schokley-Hall-Read generation-recombination analysis. It relates the

net generation-recombination rate to the free carrier densities as well as the specific properties of the generation-recombination centre. In either generation or recombination the most effective centres will have E_t close to E_i, the intrinsic energy level. For example, gold and copper give rise to two very effective trapping centres with values of (E_t-E_i) in silicon of 0.03 and 0.01 eV respectively (31) . Furthermore, Eq. (3.1) can be simplified for a particular problem. In the case of a depleted region, such as exists in MOS structures when a deep-depleting voltage step or fast voltage ramp is applied, the electron (n) and hole (p) carrier concentrations are reduced below their equilibrium concentrations such that :

$$n, p \ll n_i \tag{3.2}$$

where n_i is the intrinsic concentration of carriers. Then the generation rate is given by ,

$$U_g = -\frac{\sigma v_{th} N_t n_i}{2 \cosh\left(\frac{E_t-E_i}{kT}\right)} = -\frac{n_i}{2\tau_g} \tag{3.3}$$

where $$\tau_g = \frac{\cosh\left(\frac{E_t-E_i}{kT}\right)}{\sigma v_{th} N_t} \tag{3.4}$$

is defined as the generation lifetime. Eq (3.3) states that U_g has a maximum value when the trap is located at midgap, ie. : $E_t = E_i$.

3.2 (b) Theory of non-equilibrium fast ramp I-V :

Following the treatment presented by Board and Simmons (29), the trapping level is considered to be a generation centre only. Consider an n-type MOS device with generation centres (or trap energy levels) lying very close to the intrinsic energy level, as illustrated

in Fig 3.1. Above the Fermi level the traps are essentially empty of electrons and below it they are essentially full of electrons. When a depleting voltage is applied to the metal gate electrode the generation of electron-hole pairs will not be fast enough to maintain the device in quasi-equilibrium for a sufficiently high voltage sweep rate. As a result, the depletion region extends into the bulk, far beyond the maximum depletion width of quasi-equilibrium.

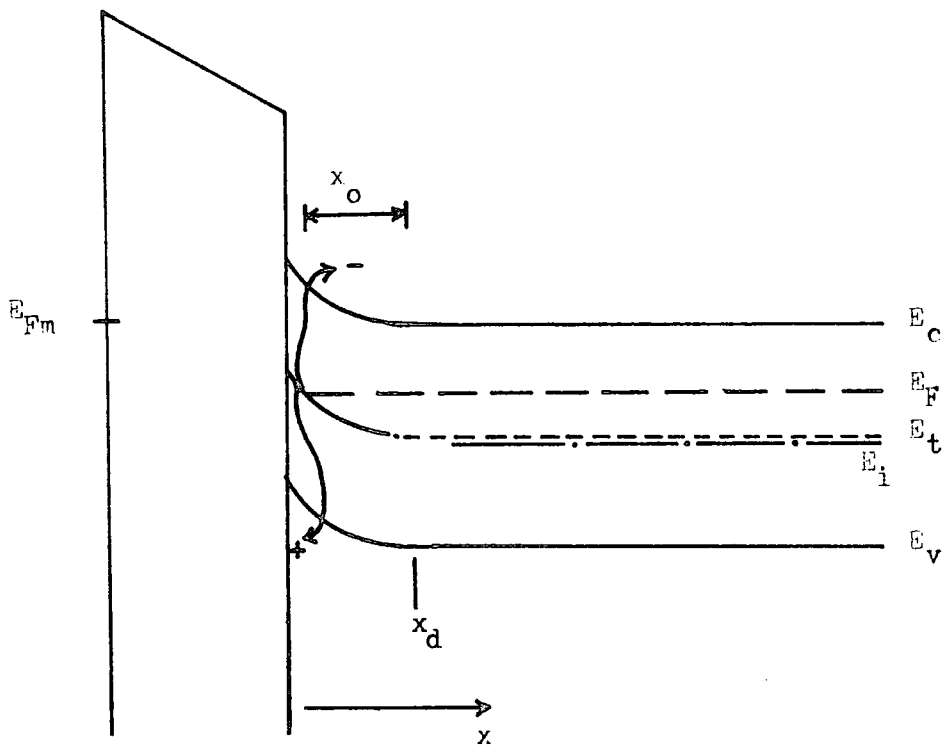


Fig 3.1 : Band diagram of n-type MOS structure with a discrete bulk trap at energy E_t biased into inversion.

In the region $(x_d-x_o) < x < x_d$, where x_o is the depletion width up to the onset of generation, the net generation rate is negligible (26). This is because the number of holes in this region is very small and the traps are essentially full. However, in the region $o< x < (x_d-x_o)$ the generation rate is very high compared to the recombination rate, so that the net generation rate is effectively given by Eq (3.3). The holes which are generated will be swept to the interface (due to high field in the depletion region) to accumulate and form the inversion charge. Thus, the process by which a MOS capacitor subjected to a depleting voltage relaxes to equilibrium is characterised by the generation lifetime. The inversion charge built up at the interface is given by,

$$Q_i = q\, U_g \int (x_d-x_o)\, dt \qquad (3.5)$$

where (x_d-x_o) represents the depletion width contributing to carrier generation. The total gate charge, Q_g, is given by,

$$Q_g = Q_{ox} + Q_d + Q_i \qquad (3.6)$$

where Q_{ox} is the fixed oxide charge and Q_d and Q_i are the depletion charge and inversion charge, respectively.

The current can be obtained by differentiating Eq (3.6),

$$I = \dot{Q}_g = q\, U_g\, (x_d-x_o) + q\, N_D\, \frac{dx_d}{dt}\,. \qquad (3.7)$$

The gate voltage is related to the depletion width by :

$$V_g = -\frac{Q_s}{C_{ox}} + \frac{q\, N_D\, x_d^{\,2}}{2\,\varepsilon_s} + V_{FB} \qquad (3.8)$$

Fig 3.2 shows typical current-voltage characteristics together with the

voltage waveform that is applied to the n-type MOS device. Section a-b of the curve shows the quasi-equilibrium part of the characteristic. In section b-c the current-voltage characteristic is in the non-equilibrium condition (i.e. the bulk silicon is being depleted). The current magnitude is reduced below that of the quasi-equilibrium value due to the reduced generation of electron-hole pairs in the depletion region. This results in the depletion layer extending further into the bulk. Hence, the current I flowing in the device consists of the current I_d (due to the discharging of the donor centres at the edge of the depletion region) and the generation current I_g as illustrated in Fig 3.3 (a) :

$$I = |I_d| + |I_g|$$

On reversal of the voltage sweep, at gate voltage V_B, the depletion layer is progressively reduced with time, the generation current continuing to flow in the same direction. The resulting current is given by,

$$I = -|I_d| + |I_g| \ ,$$

the sign of I_d is changed because the donor centres at the edge of the depletion region have to be filled (Fig 3.3 (b)).

Section c-d of the curve shows the current dropping abruptly at the instant of sweep reversal, and then following the form as indicated by section d-e. For $|I_g| > |I_d|$ the current is positive in magnitude but when $|I_g| < |I_d|$ the current becomes negative. The return to equilibrium occurs when the Fermi level in the bulk lines up with the Fermi level at the interface (Fig 3.3 (c)), at which point the current decreases abruptly as depicted by section e-f of the characteristic. The system is then in quasi-equilibrium, as

indicated by section f-g, with the current being given by

$$I = - I_d - I_q ,$$

where I_q is the current due to the flow of inversion charge (holes) from the interface.

Extraction of various parameters such as generation rate and generation lifetime can be made by the equation appropriate to the particular section of the non-equilibrium I-V characteristic (see below).

(a) Forward voltage sweep :

The voltage waveform that is applied to an n-type MOS device is shown in Fig 3.2. The forward sweep corresponds to the interval $o < t < t_B$ where the gate voltage can be represented as :

$$V_g = V_o - \alpha t = V_o - V \qquad (3.9)$$

Differentiating, with respect to time, equations (3.8) and (3.9) (second term of RHS in Eq (3.8) will be negative in this case) we obtain,

$$\frac{dV_g}{dt} = - \alpha = \frac{- I_f}{C_{ox}} - \frac{q N_D x_d}{\varepsilon_s} \frac{dx_d}{dt} \qquad (3.10)$$

Substituting I_f from Eq. (3.7) gives :

$$\left(1 + \frac{C_{ox} x_d}{\varepsilon_s} \right) \frac{dx_d}{dt} = \frac{U_g}{N_D} (L_E + x_o - x_d) \qquad (3.11)$$

where $L_E = \frac{\alpha C_{ox}}{q U_g}$ and C_{ox} is the oxide capacitance per unit area.

Using the boundary condition $x_d = x_o$ at $t = o$ the solution to the

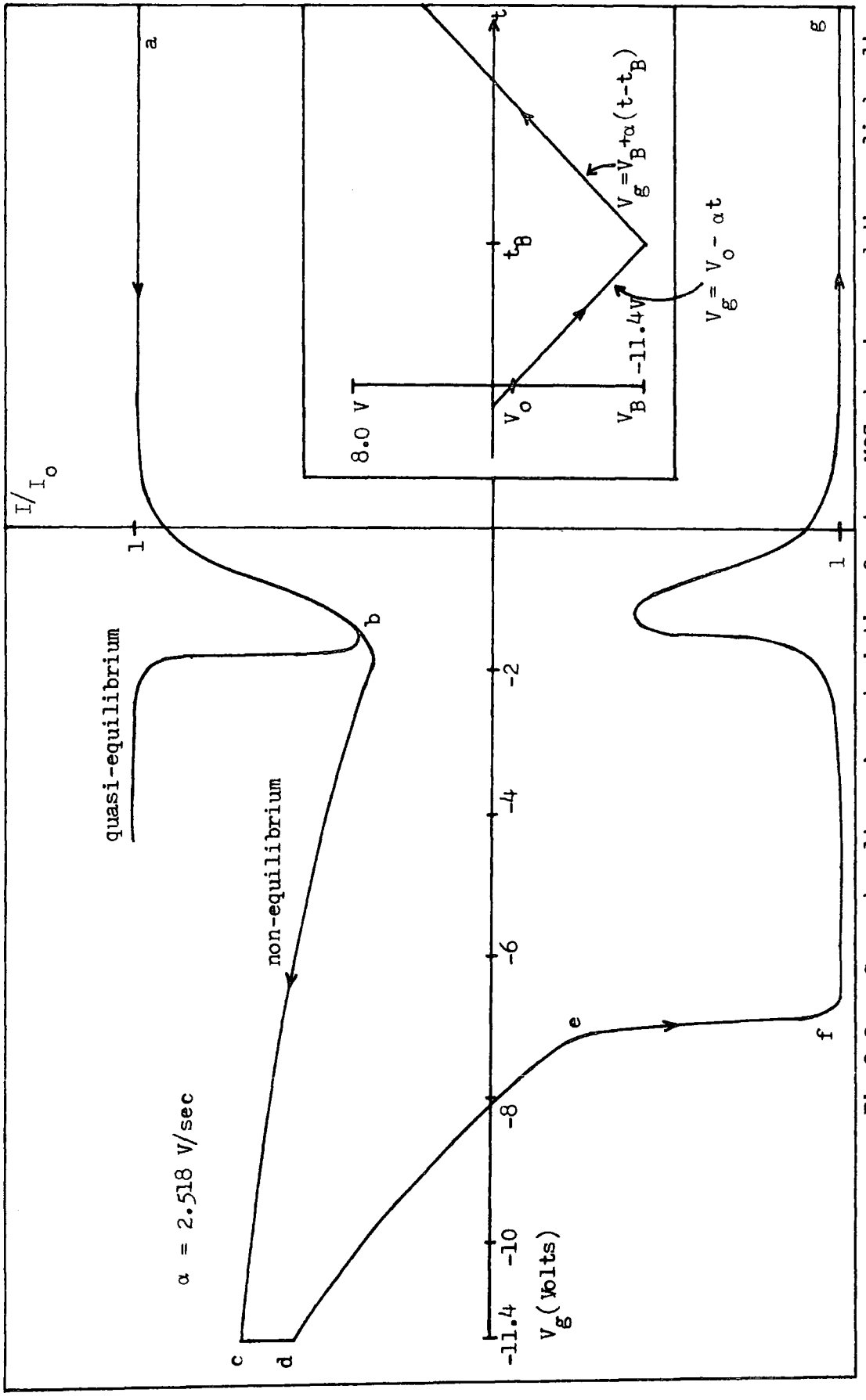


Fig 3.2 : Current-voltage characteristic of n-type MOS structure and the applied voltage waveform.

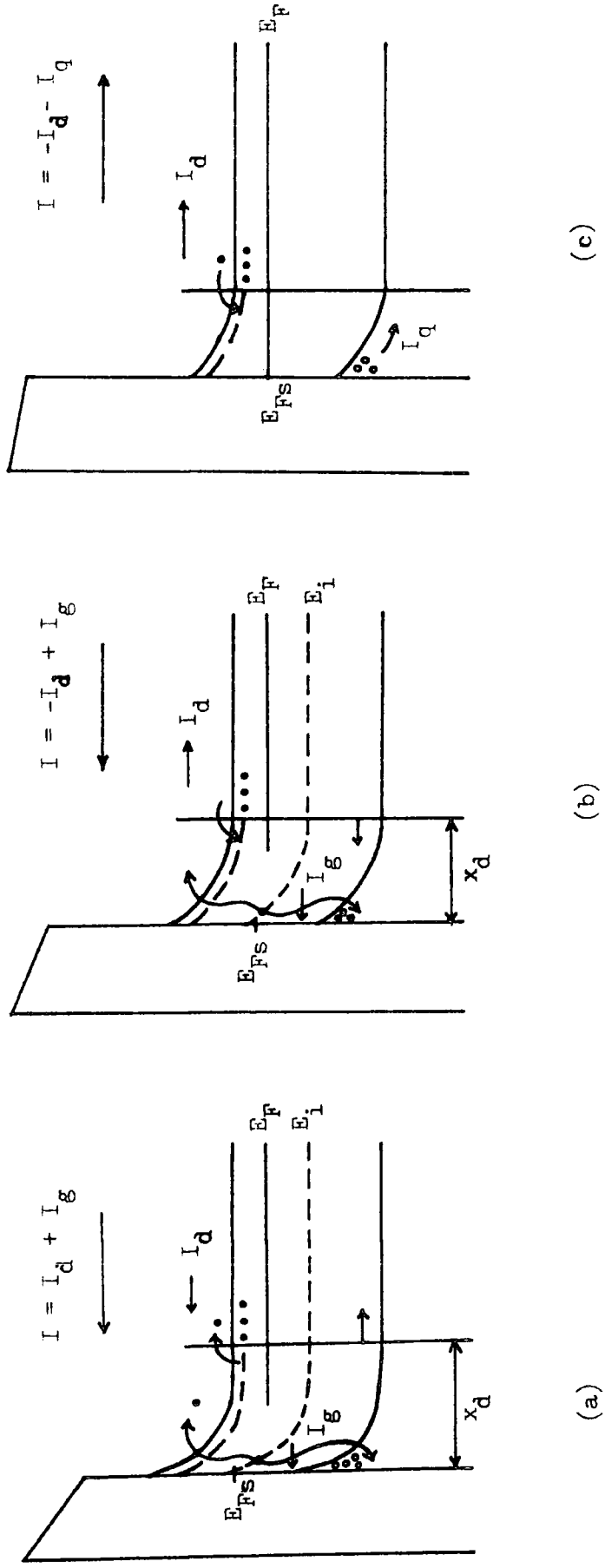


Fig 3.3 : Band diagram of MOS device with linear voltage sweep.
(a) end of depleting sweep, (b) start of reverse sweep (c) return to equilibrium.

above equation is

$$\left[1 + \frac{C_{ox}}{\varepsilon_s}(x_o + L_E)\right] \ln(1-z) + \frac{L_E C_{ox} z}{\varepsilon_s} = \frac{-C_{ox} V}{q N_D L_E} \qquad (3.12)$$

where $z = (x_d - x_o)/L_E$ is the normalized depletion width. Eq.(3.12) relates the depletion width to time (or voltage).

An expression for the current can be obtained by differentiating Eq. (3.12) with respect to z, so that

$$\frac{dz}{dV} = \frac{C_{ox}(1 - z)}{q N_D L_E \left(1 + \frac{C_{ox}}{\varepsilon_s}(x_o + z L_E)\right)} \qquad (3.13)$$

Substituting Eq.(3.13) into Eq. (3.7), then,

$$I_f = \alpha C_{ox} z + q N_D L_E \alpha \frac{dz}{dV}$$

or

$$I_f = \alpha C_{ox}\left[z + \frac{1 - z}{1 + \frac{C_{ox}}{\varepsilon_s}(x_o + z L_E)}\right] \qquad (3.14)$$

The parameter x_o, the depletion width at the start of generation, is given by,

$$x_o = \left(\frac{2 \varepsilon_s (E_F - E_t)}{q^2 N_D}\right)^{\frac{1}{2}} \qquad (3.15)$$

where E_t is the energy level of the bulk traps. The gate voltage at the onset of generation, V_o, occurs at a surface potential ψ_o such that,

$$\psi_o = -\frac{(E_F - E_t)}{q} \qquad (3.16)$$

Then,

$$V_o = - \frac{Q_s}{C_{ox}} + \psi_o + V_{FB} \qquad (3.17)$$

where Q_{sc} is the equilibrium semiconductor charge (an expression for which is given in Chapter 2).

Equations (3.9), (3.12) and (3.14) completely described the form of the non-equilibrium I-V curve as indicated by section b-c of Fig.3.2.

(b) Reverse voltage sweep :

The reverse voltage sweep corresponds to $t_B < t < t_c$, where t_c is the time at the end of the reverse sweep. The gate voltage at any time is then given by:

$$V_g = V_B + \alpha (t-t_B) = V_B + V \qquad (3.18)$$

where V_B is the gate voltage at $t = t_B$.

From equations (3.8) and (3.18),

$$\frac{dV_g}{dt} = \alpha = - \frac{I_r}{C_{ox}} - \frac{q N_D x_d}{\varepsilon_s} \frac{dx_d}{dt} \qquad (3.19)$$

Substituting I_r (from Eq. (3.7)) yields :

$$\left(1 + \frac{C_{ox} x_d}{\varepsilon_s} \right) \frac{dx_d}{dt} = - \frac{U_g}{N_D} (L_E + x_d - x_o) \qquad (3.20)$$

By using the boundary condition $z = z_B$ at $t = t_B$, separating the variables and then integrating, results in :

$$\left[1 + \frac{C_{ox}}{\varepsilon_s} (x_o - L_E) \right] \ln \frac{1+z}{1+z_B} + \frac{L_E C_{ox}}{\varepsilon_s} (z - z_B) = - \frac{C_{ox}}{q N_D L_E} .V \qquad (3.21)$$

Similarly, the expression for reverse current can be obtained by differentiating Eq.(3.20) and using Eq. (3.7),

$$I_r = \alpha C_{ox} \left[z - \frac{1 + z}{1 + \frac{C_{ox}}{\varepsilon_s} (x_o + z L_E)} \right] \qquad (3.22)$$

Combining equations (3.18), (3.21) and (3.22) will allow us to generate the non-equilibrium reverse sweep I-V characteristic (section d-e of Fig 3.2).

(c) Instant of sweep reversal

The change of current ΔI at the voltage sweep reversal can be calculated from equations (3.14) and (3.22) resulting in,

$$\Delta I = \frac{2 \alpha C_{ox}}{1 + \frac{C_{ox}}{\varepsilon_s} (x_o + z_B L_E)} \qquad (3.23)$$

where z_B is the normalized depletion width at V_B. In Fig. 3.2, ΔI is represented by section c-d of the characteristic.

(d) The return to equilibrium on reverse sweep

This occurs when the inversion charge being generated by the bulk traps is equal to the inversion charge for quasi-equilibrium at the same gate voltage. The gate voltage which corresponds to this condition, say V_R, can be obtained by substituting $z = z_o$ in Eq. (3.21),

$$V_R = V_B - \frac{q N_D L_E}{C_{ox}} \left[\left(1 + \frac{C_{ox}}{\varepsilon_s} (x_o - L_E)\right) \ln \frac{1+z_o}{1+z_B} + \frac{L_E C_{ox}}{\varepsilon_s} (z_o - z_B) \right] \qquad (3.24)$$

with $$z_o = \frac{x_m - x_o}{L_E} \qquad (3.25)$$

where x_m is the depletion region width under quasi-equilibrium strong

inversion conditions. By assuming a surface potential of $2\psi_F$ we can say,

$$x_m = \left(\frac{4 \varepsilon_s \, kT \, \ln (N_D/n_i)}{q^2 N_D} \right)^{\frac{1}{2}} \qquad (3.26)$$

(e) Equilibrium section

Sections f-g and a-b represent the quasi-equilibrium part of the characteristic and can be generated using the theory presented in Chapter 2.

In the analysis presented above, the current I is related to gate voltage V_g through the normalized depletion width, z. It can also be expressed in terms of small signal capacitance, using the relation

$$C = \frac{dQ_g}{dV_g} = \frac{dQ_g}{dt} \cdot \frac{dt}{dV_g} = I/\alpha$$

where C is the small signal capacitance.

3.3 Surface Potential-Gate Voltage Relationship

In the Kuhn analysis of interface state density evaluation (described in Chapter 2), it is necessary to obtain the semiconductor surface potential as a function of gate voltage. This can be achieved by graphical integration of the I-V curve using Berglund's (13) integration. However, this method is very tedious and time consuming when performed by hand. As an alternative, Tonner and Simmons (36) describe a method of using a single analogue circuit to provide direct plots of ψ_s vs. V_g.

Considering an n-type MOS device, the gate voltage is related to the surface potential by

$$V_g = V_{ox} + \psi_s = \frac{Q_g}{C_{ox}} + \psi_s \tag{3.27}$$

or

$$\psi_s = V_g - \frac{Q_g}{C_{ox}} \tag{3.28}$$

where Q_g is the gate charge per unit area. (The flatband voltage is not included here because it can be easily accommodated by an appropriate gate voltage translation). From Eq. (3.28), the surface potential can be obtained by subtracting Q_g/C_{ox} from the gate voltage, V_g ; this evaluation can be easily performed using analogue circuitry.

From Eq. (3.28),

$$d\psi_s (V_g) = dV_g - \frac{dQ_g}{C_{ox}} ,$$

or

$$\frac{d\psi_s(V_g)}{dV_g} = 1 - \frac{C(V_g)}{C_{ox}} \tag{3.29}$$

where $C(V_g) = dQ_g/dV_g$ is the small signal capacitance as a function of gate voltage. Integrating Eq. (3.29), the change in surface potential

for a change of gate voltage from V_i to V_g is given by :

$$\psi_s(V_g) - \psi_s(V_i) = \int_{V_i}^{V_g} \left[1 - \frac{C(V_g)}{C_{ox}} \right] dV_g \qquad (3.30)$$

where $C(V_g) = I(V_g)/\alpha$.

Berglund (13) was the first to use this equation to determine the surface potential as a function of gate voltage from the experimental quasi-equilibrium I-V curve.

For simplicity let $V_i = V_{FB}$.

Then, using the fact that $\psi_s(V_{FB}) = 0$, Eq. (3.30) reduces to :

$$\psi_s(V_g) = \int_{V_{FB}}^{V_g} \left(1 - \frac{C(V_g)}{C_{ox}}\right) dV_g \qquad (3.31)$$

By evaluating the appropriate area from the I/I_o-V_g curve, the ψ_s vs. V_g relationship for either quasi-equilibrium or non-equilibrium can be determined.

In generating the ψ_s-V_g relationship for the case of the non-equilibrium I-V curve, the various sections of the curve can be manipulated as follows :

Integrating the equation from voltage flatband, V_{FB} to the end of forward sweep, V_B, yields the surface potential at V_B as

$$\psi_s(V_B) = \int_{V_{FB}}^{V_B} \left(1 - \frac{I(V_g)}{I_o}\right) dV_g \qquad (3.32)$$

where $I_o = \alpha C_{ox}$. The integral in Eq. (3.32) will be the area marked as A in Fig. 3.4. The value is negative because dV_g is negative.

During the reverse sweep, the surface potential at any gate

voltage, V_g is given by :

$$\psi_s(V_g) = \psi_s(V_B) + \int_{V_B}^{V_g} \left(1 - \frac{I(V_g)}{I_o}\right) dV_g \qquad (3.33)$$

where $\psi_s(V_B)$ is given by Eq. (3.32). The value of $\psi_s(V_g)$ will become less negative because dV_g is positive, in other words, the surface potential begins to decrease after the voltage sweep reversal. If the integration for the reverse sweep is carried out up to the voltage flatband, then,

$$\psi_s(V_{FB}) = \psi_s(V_B) + \int_{V_B}^{V_{FB}} \left(1 - \frac{I(V_g)}{I_o}\right) dV_g \qquad (3.34)$$

where the integral term is represented by area B + C in Fig. 3.4. Since the surface potential at voltage flatband is zero, the area of A must be equal to the area of (B + C).

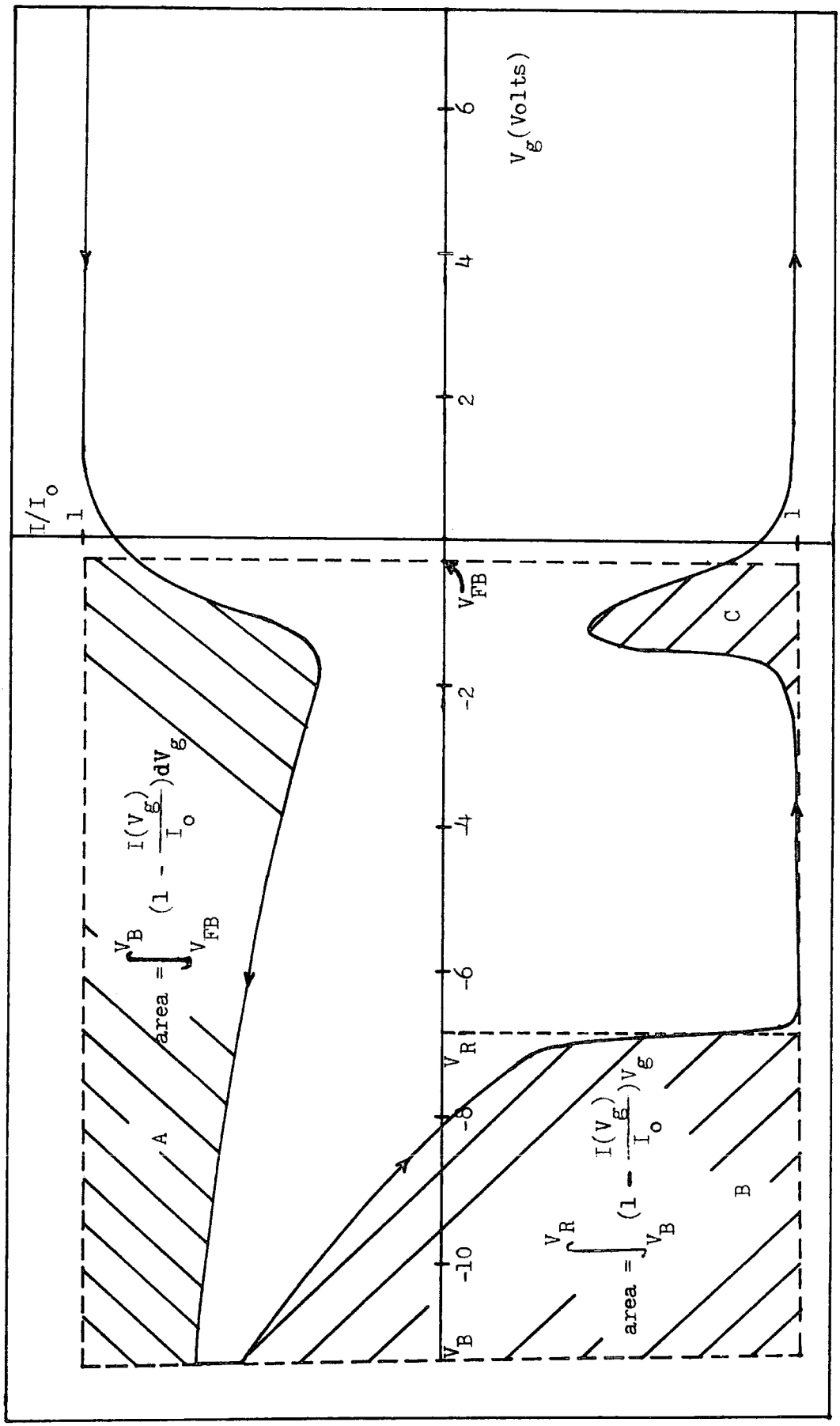


Fig 3.4 : Graphical integration of the I-V curve.

3.4 Experimental Techniques for Non-Equilibrium Measurements

The samples used for the measurements were those used for the quasi-equilibrium evaluation in Chapter 2.

3.4 (a) Non-equilibrium I-V

The experimental set-up for obtaining the non-equilibrium I-V characteristic was the same as used for the quasi-equilibrium I-V measurements. In the case of fast ramp excitation, the I-V curve was displayed on a storage oscilloscope since the speed of response of an analogue X-Y plotter is insufficient. A permanent copy of the form of the I-V characteristics was obtained by photographing the oscilloscope screen.

3.4 (b) Surface potential versus gate voltage curve

The form of equation (3.28) is very simple. Such a ~~single~~ simple expression can be realised in analogue circuit form. The schematic diagram of such a circuit is illustrated in Fig 3.5. The method is based on a measurement of MOS capacitor gate charge in response to a linear voltage ramp. The resulting charging current from the MOS device is fed into the input of the Keithley electrometer (Model 600B), this being operated on the charge range.

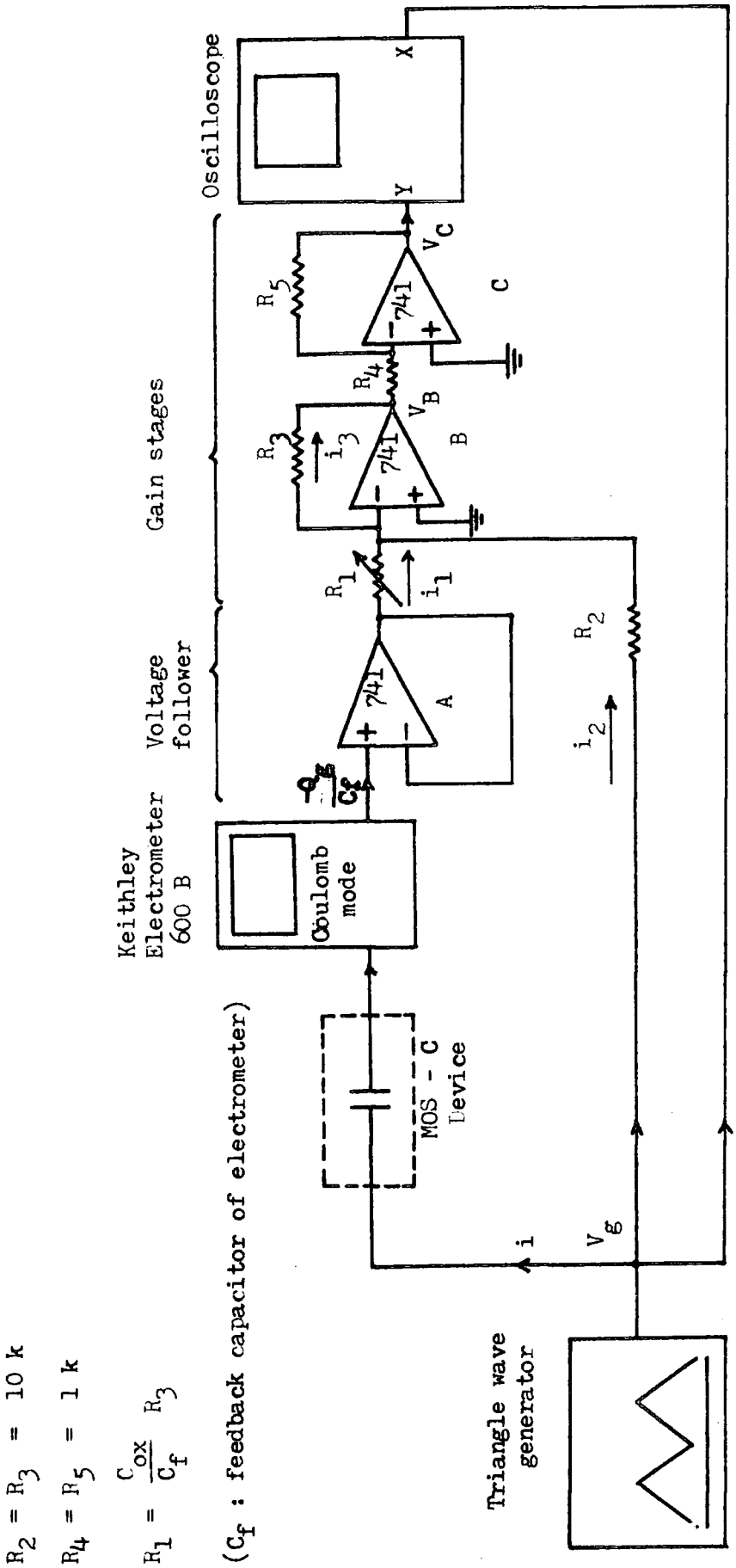
The electrometer is operated in the 'fast' mode and the output voltage is a measure of the gate charge, Q_g :

$$V = \frac{1}{C_f} \int_0^t i \, dt = - \frac{Q_g}{C_f} \qquad (3.35)$$

where C_f is the feedback capacitor in the electrometer. The operational amplifier A acts as a voltage follower, so its output will be equal to $- Q_g/C_f$. The current flowing into the input terminal of amplifier B is given by

$$i_3 = i_1 + i_2 \qquad (3.36)$$

where $i_1 = V/R_1 = - Q_g/CR_1$ and $i_2 = V_g/R_2$.



$R_2 = R_3 = 10\ k$

$R_4 = R_5 = 1\ k$

$R_1 = \frac{C_{ox}}{C_f} R_3$

(C_f : feedback capacitor of electrometer)

Fig 3.5 : Schematic diagram of the experimental set-up used to measure the $\psi_s - V_g$ relationship of an MOS capacitor.

The output V_B of amplifer B is thus :

$$- V_B = i_3 R_3 = R_3 \left(\frac{V_g}{R_2} - \frac{Q_g}{CR_1} \right) \tag{3.37}$$

selecting $R_2 = R_3$ and $R_1 = \frac{C_{ox}}{C_f} R_3$, yields

$$- V_B = V_g - \frac{Q_g}{C_{ox}} \tag{3.38}$$

The output V_C of amplifier C is the inversion of V_B, thus :

$$V_C = V_g - \frac{Q_g}{C_{ox}} \tag{3.39}$$

Comparing equations (3.28) and (3.39), the surface potential ψ_s is simply given by the output V_C. The output V_C and the gate voltage V_g are fed into the oscilloscope, allowing us to display the ψ_s vs. V_g characteristic directly.

All of the amplifiers and components, except resistor R_1, are mounted in a screened box. The value of external resistor R_1 (variable) depends on the oxide capacitance of the MOS sample through the relation :

$$R_1 = \frac{C_{ox}}{C_f} R_3$$

The system was assessed using a constant capacitor of the polystyrene type (measured as 224 pF and with insulation resistance greater than 10^{12} ohms). Measurements were taken for different voltage sweep rates, each time the value of R_1 being compared with the expected theoretical value. It was observed that the difference was 2% or less, which is acceptable.

3.5 Analysis of Results for an n-type MOS Device

3.5 (a) Non-equilibrium I-V characteristic

Fig 3.6 shows experimental non-equilibrium I-V curves as a function of voltage sweep rates measured at room temperature. The non-symmetrical nature of the curves about the voltage axis is due to the fact that the net generation rate of electron-hole pairs is insufficient to maintain the device in quasi-equilibrium. Consequently, as the voltage sweep rate is increased the depletion layer extends further into the semiconductor bulk. The current at strong accumulation, I_o, is measured for every voltage sweep-rate allowing us to determine the oxide capacitance, C_{ox}, from the relationship $C = I_o/\alpha$

α (V/sec)	I_o (Amp)	C_{ox} (pF)
1.257	3.4×10^{-10}	270.5
2.518	6.8×10^{-10}	270
4.419	1.2×10^{-9}	271
6.941	1.85×10^{-9}	266.5

The values of C_{ox} obtained here are very close to those obtained from high-frequency C-V measurements (i.e. : 268 pF) as described in Chapter 2. The differences are well within experimental error.

For ease of analysis the normalized current rather than the absolute value is plotted against gate voltage in Fig 3.6. The dashed curves in Fig 3.6 are the theoretical non-equilibrium I-V characteristics, generated using the theory presented by Board and Simmons (29) . To obtain the form of the characteristic at any particular voltage sweep rate, α , the normalized steady-state depletion width, L_E (in this case the parametric variable) is first chosen and then the current-voltage relationship calculated. A value of L_E can then be selected to give the optimum fit to the experimental I-V curve. The

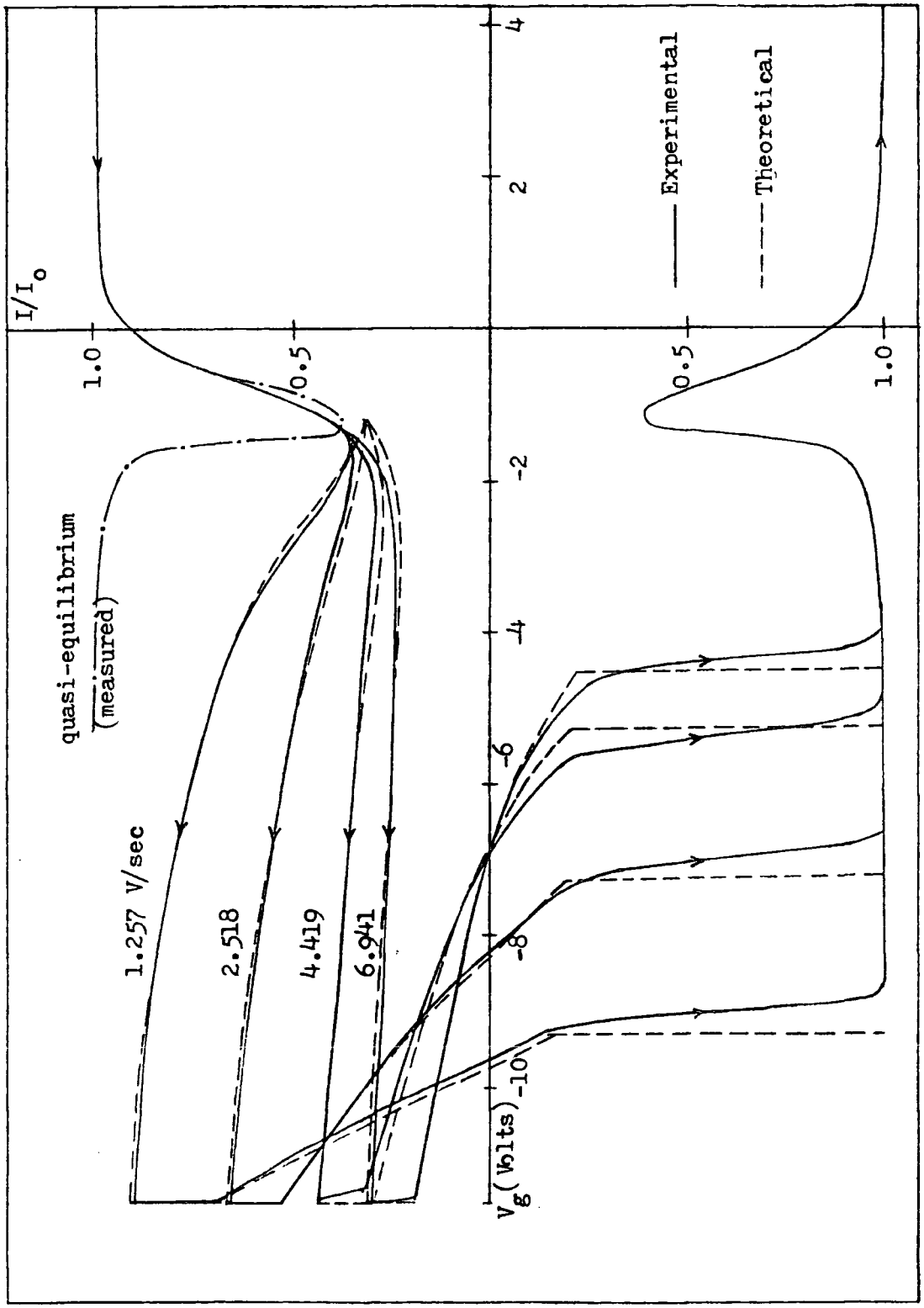


Fig 3.6: Non-equilibrium I-V characteristics of n-type MOS device for various voltage sweep rates.

value of x_o, the depletion layer width at the start of generation, is calculated using Eq. (3.15) by assuming that the traps are located at, or very near to, mid-gap. From the relationship $L_E = \frac{\alpha C_{ox}}{q U_g}$ the generation rate, U_g, can be determined. The process of obtaining the generation rate is repeated for the other curves taken at different voltage sweep rates. This means that the value of L_E, and thus U_g, is determined independently for every different voltage sweep rate characteristic. It can be seen from Fig 3.6 that the theoretical curves are in close agreement with the experimental I-V curves over most of the sweep range. The theoretical normalized current at the onset of generation is seen to be lower than the measured current. This difference may be attributed to the effect of interface states. The differences between the measured I-V curves and the generated theoretical curves is very obvious at the early portion of the forward sweep. As the gate voltage is increased, and thus the depletion region width extended further into the bulk, the difference seems to be reduced.

Assuming that the bulk traps are at midgap it is possible to calculate the generation rate and hence the generation lifetime. The average generation rate obtained is of the order of 1.3×10^{15} cm^{-3} sec^{-1}. The generation lifetime, τ_g (where $\tau_g = n_i/2U_g$)is then calculated for every I-V curve and is found to have values of 6.05, 5.92, 5.97, 6.03 μsec at voltage sweep rates, α, of 1.257, 2.518, 4.419 and 6.941 V/sec, respectively. These values can give an average of 6.0 μsec. Furthermore, if it is assumed that thermal velocity, $v_{th} = 10^7$ cm/sec and capture cross-section, $\sigma = 1.0 \times 10^{-15}$ cm^2, then the bulk trap density is 1.7×10^{13} cm^{-3}.

3.5 (b) $\psi_s - V_g$ curves

The solid curve shown in Fig 3.7 is the quasi-equilibrium surface potential versus gate voltage characteristic obtained using the experimental

circuit as of Fig 3.5. The experimental curve was obtained by using a value of external variable resistor, R_1 of 270 ohms and feedback capacitor, C_f of 10^4 pF, resulting in a value of C_{ox} of 270 pF. Again this is very close to the value of C_{ox} obtained from the high frequency measurement (268 pF). The dashed line shows the result obtained using the Berglund graphical integration method. Graphical integration is obtained by calculating the appropriate area for a small increment of gate voltage using Simpson's approximation. The agreement between these two curves is quite good although some deviation at strong accumulation and strong inversion is apparent.

Fig 3.8 shows the ψ_s-V_g characteristic obtained as the voltage sweep rate is increased. The solid lines are the experimental curves while the theoretical curves are represented by the dashed lines. The theoretical curves are generated using the relation

$$\psi_s (V_g) = - \frac{q N_D x_d^2}{2 \varepsilon_s}$$

where x_d is related to the gate voltage, V_g, through the parameter z by :

$$x_d = z L_E + x_o,$$

with the parameter z being already defined (section 3.2 (b)). The two sets of curves, experimental and theoretical, are so close as to be indistinguishable. The curves presented correspond to the I-V characteristics of Fig 3.6, with the same voltage sweep rates. The surface potential, ψ_s becomes increasing negatively as the gate voltage is increased more negative. This is a consequence of the depletion layer width expanding further into the semiconductor bulk during the forward sweep. During the reverse voltage sweep the surface potential decreases due to the decreasing depletion layer width. The reduction in ψ_s continues to be appreciable until we reach a particular gate

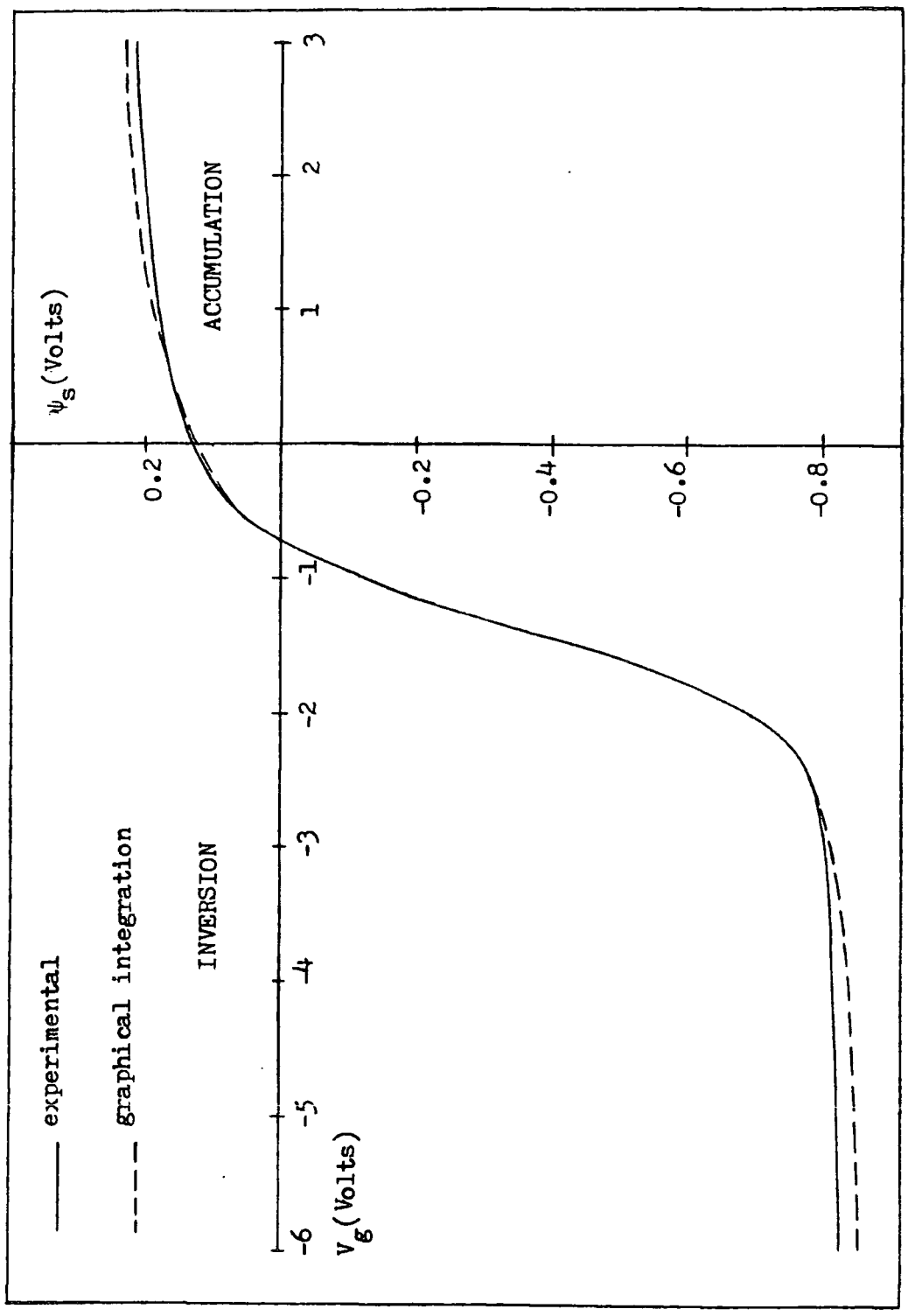


Fig 3.7 : Quasi-equilibrium $\psi_s - V_g$ characteristics of n-type MOS device.

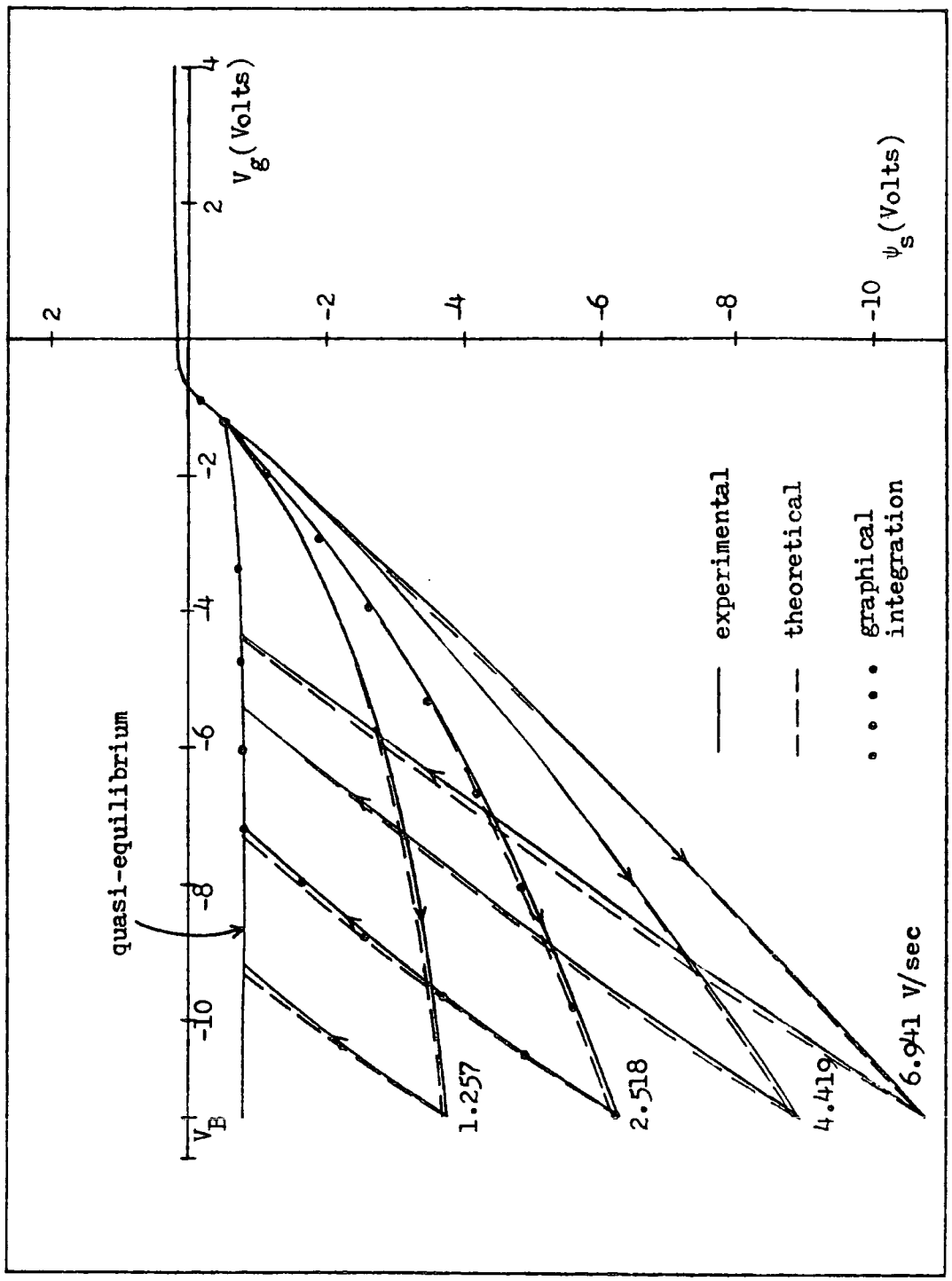


Fig 3.8 : Non-equilibrium $\psi_s - V_g$ characteristics corresponding to the I-V curves of Fig 3.6.

voltage whereby the system returns to quasi-equilibrium ; the surface potential then follows the quasi-equilibrium characteristics.

The quasi-equilibrium $\psi_s - V_g$ is included in Fig 3.8. It is observed that the surface potential is essentially constant at strong inversion and that the characteristic displays no hysteresis. On the other hand, under non-equilibrium, hysteresis in the characteristics is observed.

The dotted curve in Fig 3.8 (for a voltage sweep rate, α = 2.518 V/sec) was obtained by graphical integration of the I-V characteristic. Again, close agreement with the theoretical curve is demonstrated.

3.6 Analysis of Results for a p-type MOS Device

3.6 (a) Non-equilibrium I-V characteristic

The experimental non-equilibrium I-V characteristics are shown in Fig 3.9. The measurements were taken at room temperature for different voltage sweep rates. The current at strong accumulation, I_o was measured for every voltage sweep rate and the oxide capacitance C_{ox} determined.

α (V/sec)	I_o (Amp)	C_{ox} (pF)
0.292	2.5×10^{-10}	856.2
0.588	0.5×10^{-9}	850.3
1.281	1.1×10^{-9}	858.7
1.667	1.45×10^{-9}	869.8

These values of C_{ox} are found to be in good agreement with the value of 850 ~~868~~ pF obtained from the high frequency measurement (2 percent difference or less).

The dashed lines in Fig 3.9 are the theoretical I-V curves. In generating these theoretical curves the normalized steady-state depletion width, L_E, is first chosen and then the current and voltage values can be determined. The value of L_E is selected to give the best fit to the experimental curve. If the bulk traps are assumed to be positioned at midgap the generation rate, U_g, can be calculated. The value of x_o is calculated using Eq (3.15). The process of obtaining the generation rate, U_g, is repeated for other curves with different voltage sweep rates. The close agreement between the experimental and theoretical curves is demonstrated over most of the characteristic. It can be observed that the characteristics first follow the quasi-equilibrium curve and then deviate on to the non-equilibrium portion. This is due to the fact that the generation rate of electron-hole pairs is not fast enough to cope with the changing gate voltage ; as a result, the current is lower than the quasi-equilibrium value. The calculated

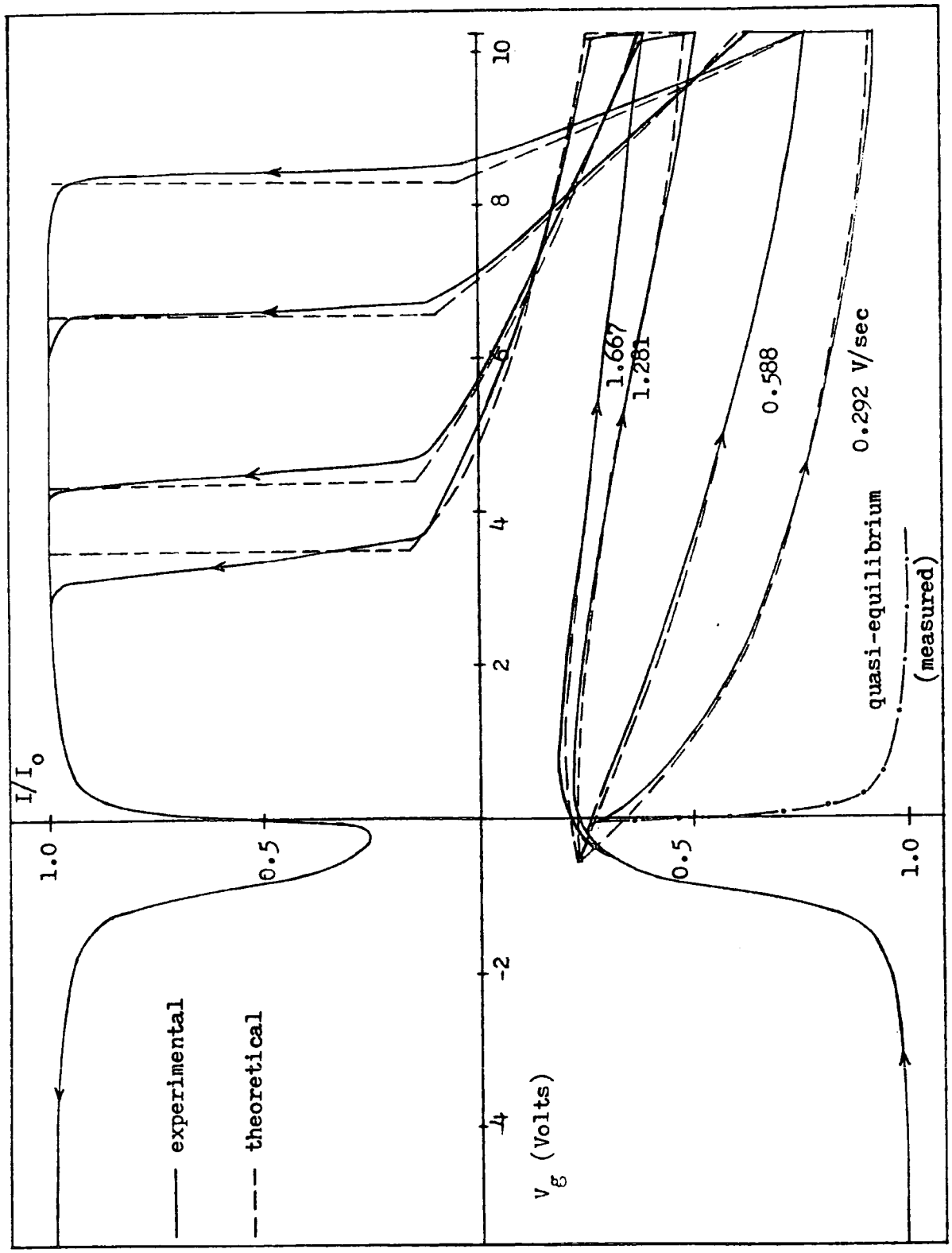


Fig 3.9 : Non-equilibrium I-V characteristics of p-type MOS device.

current at the onset of generation is found to be lower than obtained experimentally. The difference is thought to be due to the emission from interface states (36) . However, for increasing gate voltage the difference between the two curves becomes very small.

Using the theory presented in section 3.2 (b), it is possible to calculate the voltage sweep rate which must not be exceeded if the system is to remain in quasi-equilibrium. This condition is when

$$x_{dm} - x_o = L_E$$

where x_{dm} is the depletion width at strong inversion under equilibrium conditions and is given by,

$$x_{dm} = \left(\frac{4 \varepsilon_s \psi_F}{q N_A} \right)^{\frac{1}{2}}$$

Using the relation $L_E = \alpha C_{ox} / q U_g$, the voltage sweep rate for the condition to occur is :

$$\alpha = \frac{q U_g}{C_{ox}} \left(x_{dm} - x_o \right) = 0.05 \text{ V/sec},$$

which lies between 0.026 (for the quasi-equilibrium curve) and 0.292 V/sec (for the non-equilibrium curve).

The generation lifetime can be evaluated by assuming the bulk traps are at midgap. The values obtained are 18.5, 16.3, 16.0, 16.0 μsec for the curves with voltage sweep rates of 0.292, 0.588, 1.281, 1.667 volts/sec, respectively. If we assume the thermal velocity, $v_{th} = 1 \times 10^7$ cm/sec and the capture cross-section, $\sigma = 1.0 \times 10^{-15}$ cm^2, the average bulk trap density is 6.3×10^{12} cm^{-3}.

3.6 (b) $\psi_s - V_g$ curves

The quasi-equilibrium ψ_s-V_g relationship obtained using the circuit described earlier is shown by the solid line in Fig 3.10. The dashed line is the curve obtained by graphical integration. The experimental curve was obtained using an external variable resistor, R_1, of value 858 ohm and feedback capacitor, C_f, of 10^4 pF. Using the equations given in section 3.4 (b) the oxide capacitance, C_{ox}, is 858 pF, which again is in good agreement with the result obtained from the high frequency measurement.

Fig 3.11 shows the experimental non-equilibrium ψ_s-V_g characteristics obtained as the voltage sweep rate is increased. These curves correspond to the set of experimental non-equilibrium I-V curves in Fig 3.9.

The quasi-equilibrium ψ_s-V_g curve is included in Fig 3.11 and shows no hysteresis. The approximately constant surface potential is observed in the strong inversion region.

The result obtained using a graphical integration method is shown by the dotted curve in Fig 3.11 (for a voltage sweep rate, α , of 0.588 V/sec.

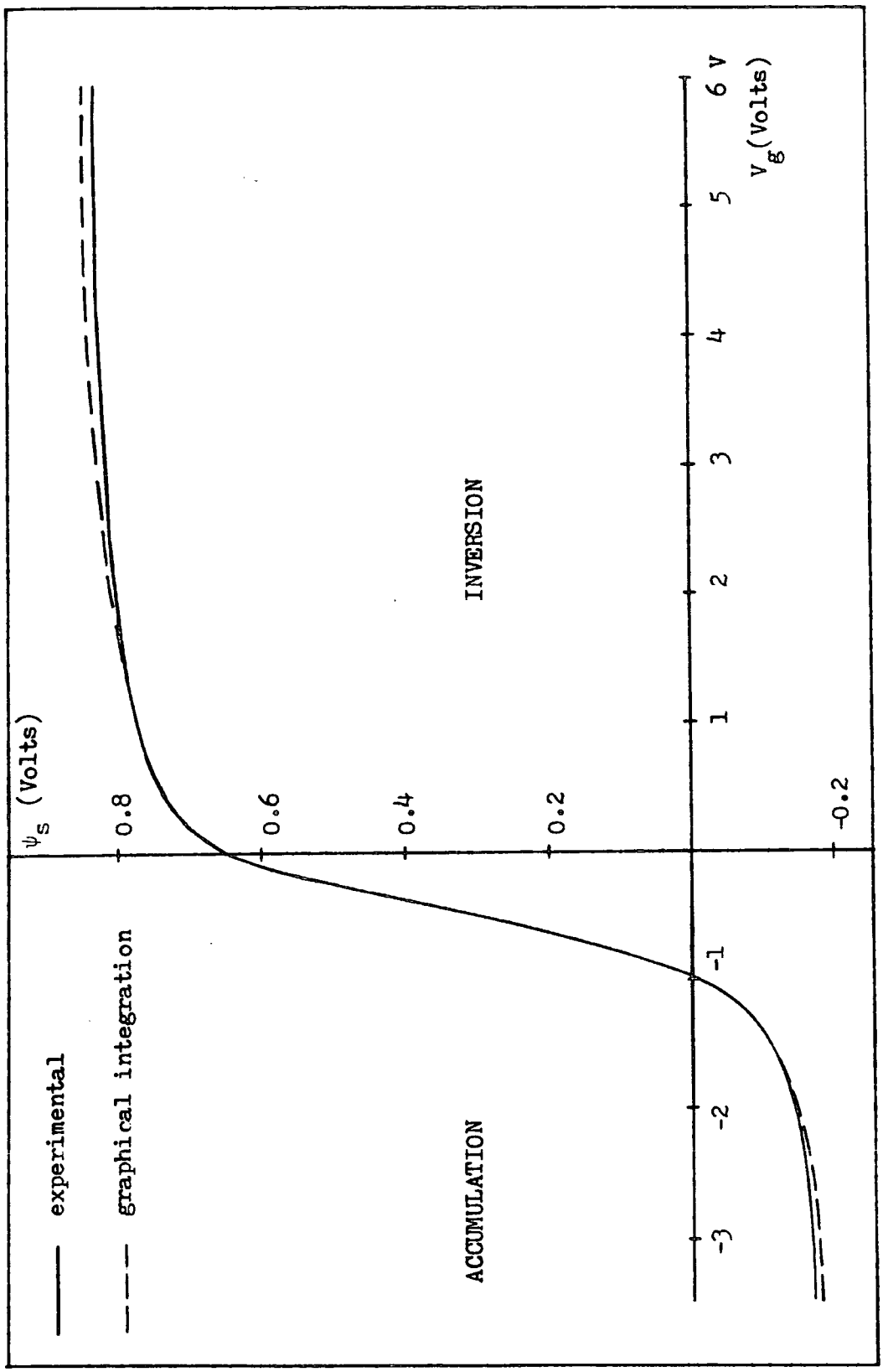


Fig 3.10 : Quasi-equilibrium ψ_s-V_g characteristics of p-type MOS device

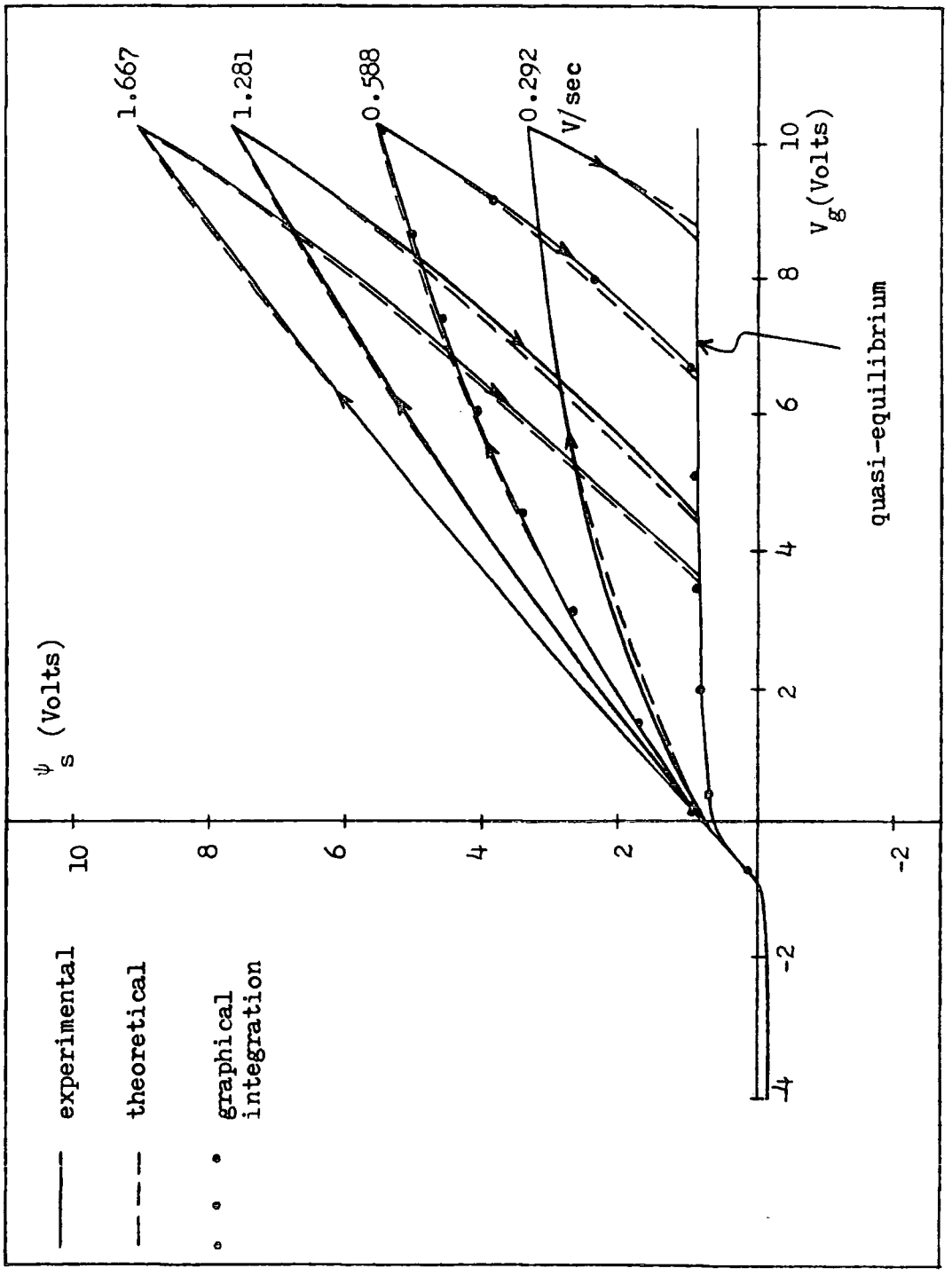


Fig 3.11 : Non-equilibrium ψ_s-V_g characteristics corresponding to the I-V curves of Fig 3.9.

3.7 Discussion

The non-equilibrium I-V characteristics of an MOS system (n-type and p-type) in response to a linear voltage ramp has been investigated. The experimental results were shown to have a close correlation with the theory presented. Assuming that the bulk traps are located at midgap (as the most efficacious generation centres) allowed us to determine the generation rate and generation lifetime. Values of generation lifetime were determined for each of the different voltage sweep rates and the results were shown to be consistent. Interface states were observed to have an effect on the early portion of the forward sweep characteristic.

A simple analogue circuit was found to be useful in directly generating a plot of surface potential versus gate voltage. The quasi-equilibrium ψ_s vs. V_g curve generated using the circuit is in reasonably good agreement with the tedious graphical integration method. Furthermore, the circuit can be used to generate the non-equilibrium ψ_s vs. V_g curves. Again, such curves are shown to be in close agreement with those obtained by graphical integration.

CHAPTER 4

TRANSIENT CHARGE MEASUREMENTS AND COMPARISON WITH FAST RAMP

4.1 Introduction

This chapter presents the results obtained for the generation lifetime measured using the Q-t method of Hofstein (23). These results are later compared with those from the fast ramp measurements in Chapter 3.

The Q-t method consists of measuring the charge response following the application of small step voltages to the gate of an MOS capacitor biased initially in strong inversion. The present measurement makes use of automated computer controlled-digital instrumentation developed in the Department (38).

Since the device is initially biased in inversion the effect of interface states is minimal. It is not the purpose of this work to discuss the Q-t theory in detail and, as such, only the simple model presented by Hofstein (23) is considered. The transient response of the inversion charges is assumed to follow a simple exponential law and the generation lifetime is computed from the time constant of the transient characteristic. Because the observed transient time is very much larger than the generation lifetime (of the order of 10^5 to 10^6 times), the method can be used to measure lifetimes as low as 10^{-10} second.

The results obtained will be compared with the values computed from the fast ramp measurements.

4.2 Theory of Inversion Charge Transient Response

The theoretical considerations are developed here for an n-type MOS capacitor biased by a sufficiently large negative gate voltage, V_g, so that an inversion layer is created at the silicon-silicon dioxide interface. Upon the application of a negative voltage step ΔV_g, towards stronger inversion, the depletion width expands further into the bulk. Simultaneously, electron-hole pairs start to be generated within part of the depletion layer. As a result, the minority carriers (holes) are swept to the silicon-silicon dioxide interface reinforcing the inversion layer while the depletion width relaxes back to its equilibrium value. The energy band diagram corresponding to this relaxation process is shown in Fig. 4.1.

The electrical response is thus determined by a dynamic equilibrium between the depleting voltage step tending to increase the depletion layer width, and the generation of carriers tending to collapse it and restore equilibrium. There are some other mechanisms of inversion layer formation (not included in the analysis here), such as thermal generation at the silicon-silicon dioxide interface, thermal generation in the neutral semiconductor bulk and surface generation around the edge of the capacitor which is discussed by Schroder (42).

The simplified small-signal equivalent circuit of an MOS capacitor biased in strong inversion is illustrated in Fig. 4.2 (23). C_{ox} is the oxide capacitance, C_d the depletion layer capacitance and R_t a resistance associated with the generation-recombination processes. Assuming that the generation-recombination centres are at midgap, Sah et al (43) have shown that,

$$R_t = \frac{\tau_g \cdot V_d}{q\, n_i\, x_d} \qquad (4.1)$$

where τ_g is the generation lifetime, V_d is the voltage dropped across the depletion region, and x_d the width of the depletion region.

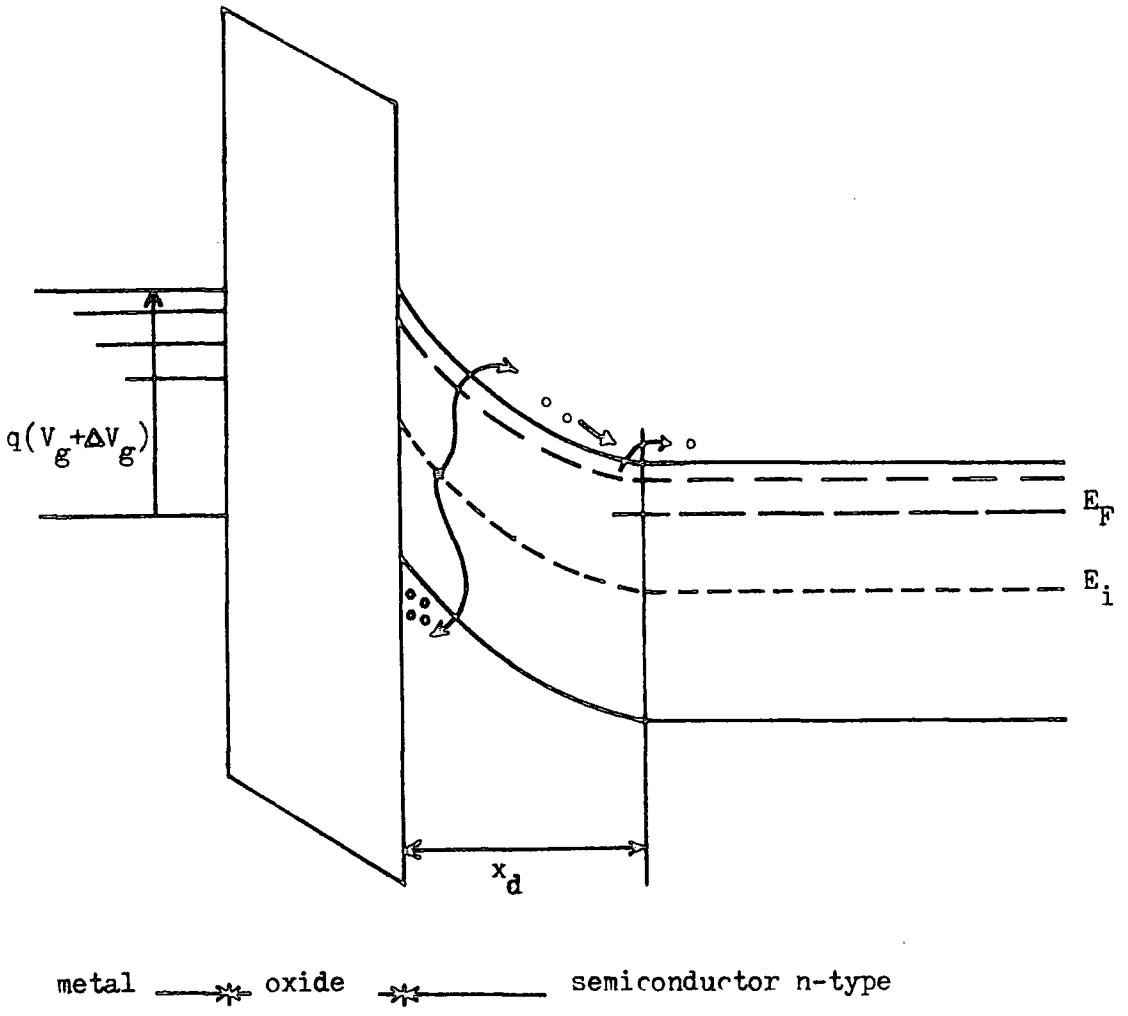


Fig 4.1 : Relaxation of depletion region due to generation of electron-hole pairs in the depletion region of an MOS capacitor.

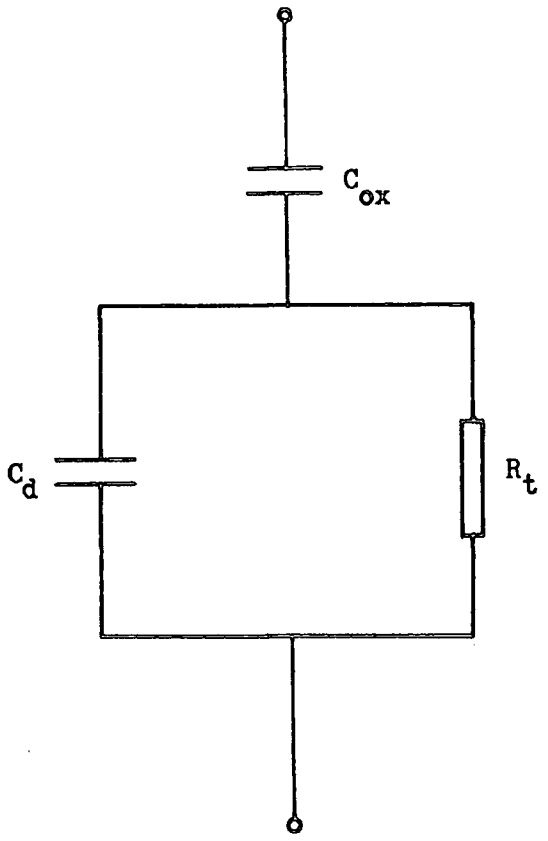


Fig 4.2 : Equivalent circuit of the MOS structure in strong inversion.

The generation lifetime can therefore be deduced from a measurement of R_t. As proposed by Hofstein (23), the response time of the MOS structure to a small-signal perturbation is measured. From the equivalent circuit of Fig. 4.2, the dynamic behaviour is characterised by a time constant :

$$\tau_r = R_t \cdot (C_{ox} + C_d) \tag{4.2}$$

Using the relations

$$C_d = \frac{\varepsilon_s}{x_d} \tag{4.3}$$

and

$$C_m = \frac{C_{ox}\ C_d}{C_{ox} + C_d} \tag{4.4}$$

where C_m is the high frequency strong-inversion capacitance, the generation lifetime from Eq (4.1) is given by :

$$\tau_g = \tau_r \cdot \frac{q\, n_i\, \varepsilon_s \left(1 - C_{m/C_{ox}}\right)^2}{V_d\, C_{ox}^2 \cdot C_{m/C_{ox}}} \qquad (4.5)$$

Fig. 4.3 shows the transient behaviour of the total charge after a small voltage step is applied to the gate of an MOS capacitor. The ratio of $C_{m/C_{ox}}$, which appears in Eq. (4.5), can be obtained directly from such a transient curve. The rapid initial step, ΔQ_m, is due to the very fast change of depletion region width in the beginning of the transient. The initial charge step is given by

$$\Delta Q_m = C_m \cdot \Delta V_g \qquad (4.6)$$

where ΔV_g is the small voltage step and C_m is the high frequency capacitance at inversion. The total change of charge stored in the MOS system is determined by the oxide capacitance, C_{ox} as :

$$\Delta Q_o = C_{ox} \cdot \Delta V_g \qquad (4.7)$$

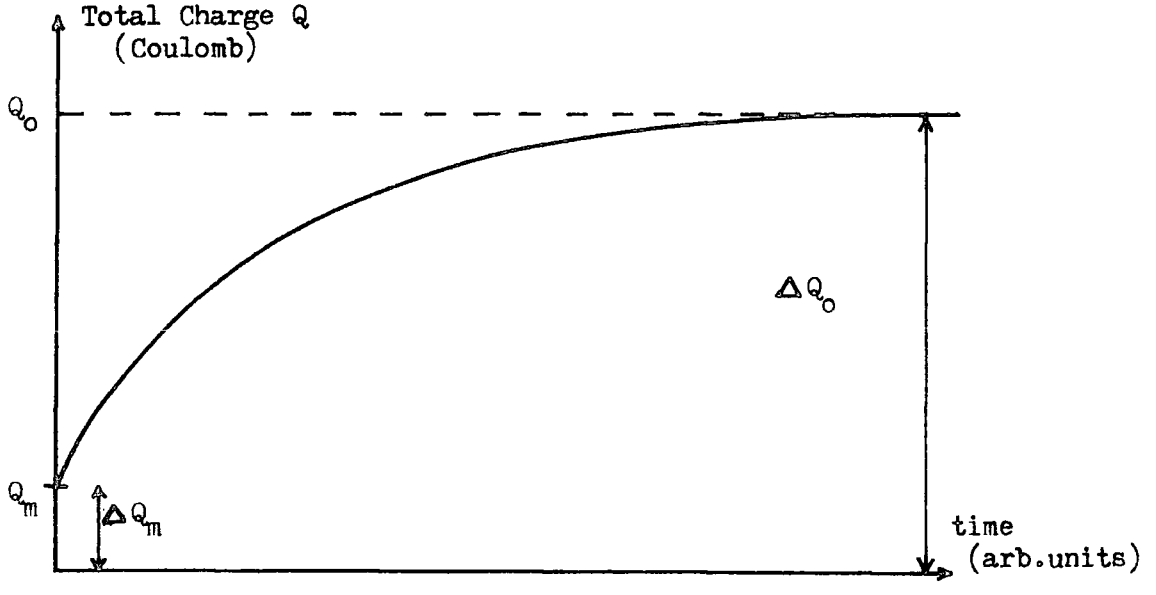


Fig. 4.3 : Schematic diagram of the transient characteristic of the total charge in an MOS capacitor after a small depleting voltage step.

The capacitance ratio C_m/C_{ox} can therefore be obtained by measuring the changes ΔQ_m and ΔQ_o ; so that from Equations (4.6) and (4.7)

$$C_m/C_{ox} = \Delta Q_m/\Delta Q_o \tag{4.8}$$

The time constant, τ_r can be computed from the Q-t transient, assuming that the characteristics follow the simple exponential law.

$$Q - Q_m = (Q_o - Q_m)\left(1 - e^{-t/\tau_r}\right) \tag{4.9}$$

The slope of a semilogarithmic plot of $1 - \frac{Q-Q_m}{Q_o-Q_m}$ against t will therefore give the value of τ_r.

4.3 Experimental Details

The equipment used for measuring the charge-time (Q-t) transient behaviour of MOS capacitors is illustrated in Fig 4.4 (38). This equipment has recently been developed in the Department by Z.A. Ibrahim whose assistance with the Q-t measurements is gratefully acknowledged.

A d.c. bias, V_g, causes the MOS system to be in strong inversion. A rectangular voltage step of amplitude $\Delta V_g = 0.025$ V (generated from the PET computer) is superimposed upon V_g. The charge flow following the application of the voltage step is measured by the electrometer which is operated in the Coulomb mode. The output voltage of the electrometer, V_{out}, is thus directly proportional to the total charge Q stored on the MOS system. The sample was housed in a screened chamber and flushed with dry nitrogen in order to reduce leakage currents across the surface.

The analogue voltage output from the electrometer, which is monitored using an oscilloscope, is converted to a digital form. A computer program was available for the computer which controls the experiment and which finally produced the Q-t transient on a digital plotter (38). The Q-t curve is plotted after averaging the data over several runs.

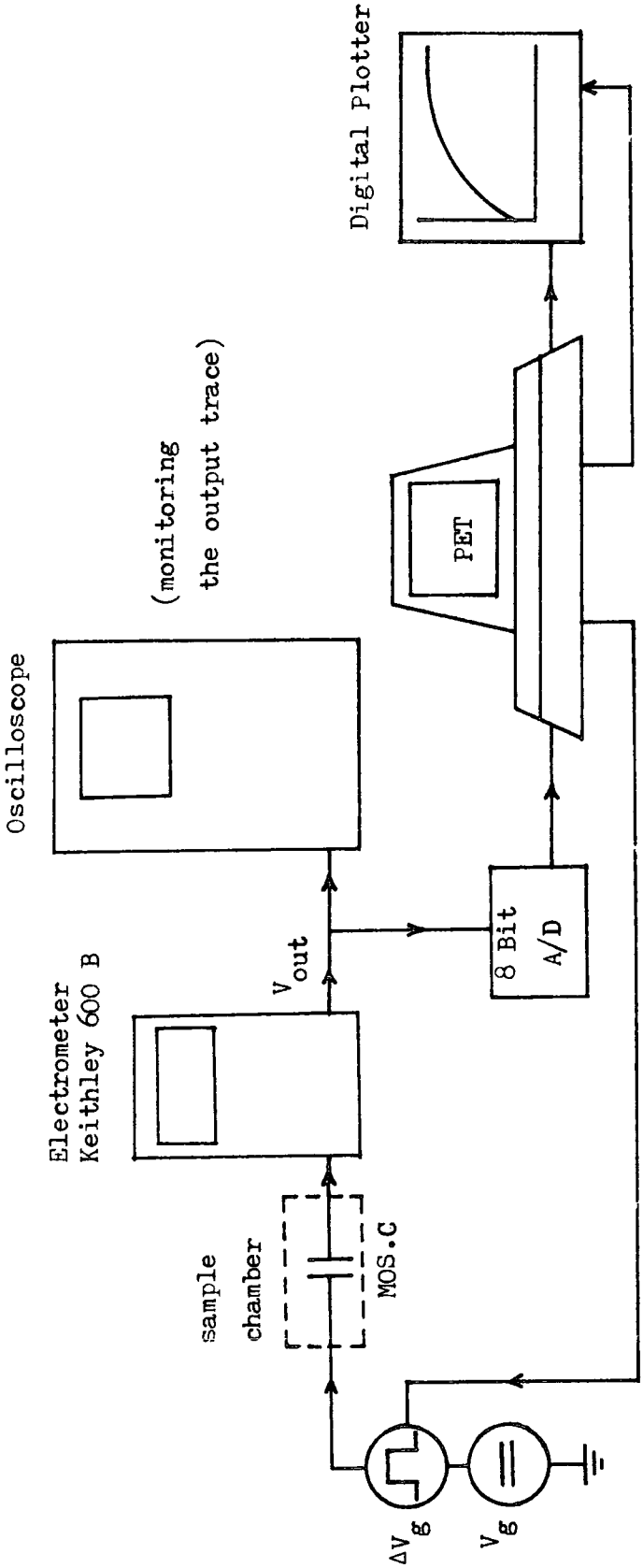


Fig 4.4 : Instrumentation used for Q-t measurement.

4.4 Results and Analysis

4.4 (a) N-type MOS sample

Fig. 4.5 shows the Q-t plot obtained for the same n-type MOS capacitor as used for measurements in previous chapters. The response is to a step voltage of 0.025 volts superimposed on a d.c. bias of -5.05 volts, so that the gate voltage finally reached a value of -5.075 volts.

Assuming that the transient behaviour follows the characteristics described by Eq. (4.9), the time constant τ_r is determined to be 0.51 sec (from the slope of curve (a) in Fig.4.6). The transient behaviour is seen to follow the exponential characteristic but deviates from it for larger times, as shown by the plot of $\ln\left[1 - \frac{Q-Q_m}{Q_o-Q_m}\right]$ vs. t in Fig 4.6 (curve a).

The ratio of C_m/C_{ox} as obtained from the high frequency measurement is 0.224. Using this value and putting $V_d = 2\psi_F$ in Eq. (4.5), the generation lifetime, τ_g, is determined to be 5.9 μsec. However the value of C_m/C_{ox} can also be obtained from the charge transient since

$$\frac{C_m}{C_{ox}} = \frac{\Delta Q_o}{\Delta Q_m}$$

The value of $\Delta Q_o/\Delta Q_m$ is 0.253 from Fig.4.5, and substituting this into Eq. (4.5) gives τ_g as 4.9 μsec. The difference in the two values is seen to be relatively small and within the limits of experimental error and theoretical assumptions.

4.4 (b) P-type MOS sample

The Q-t plot measured for the p-type sample is shown by curve (a) in Fig.4.7. The response was measured with the MOS system biased at a gate voltage of 5 Volts and a step voltage of 0.025 Volts. The transient behaviour is measured for a positive going voltage step

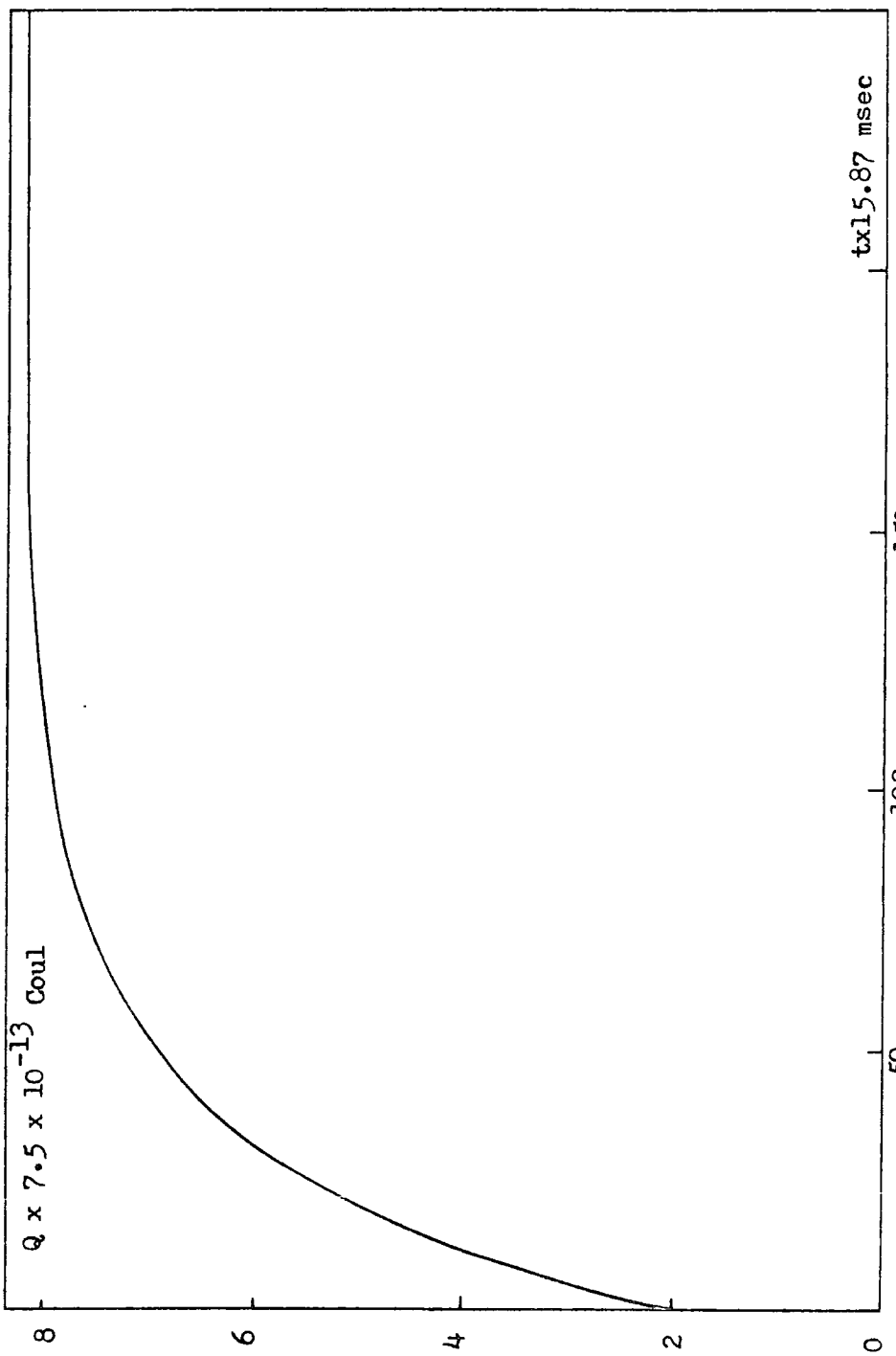


Fig 4.5 : Charge-time transient plot for the n-type MOS sample.

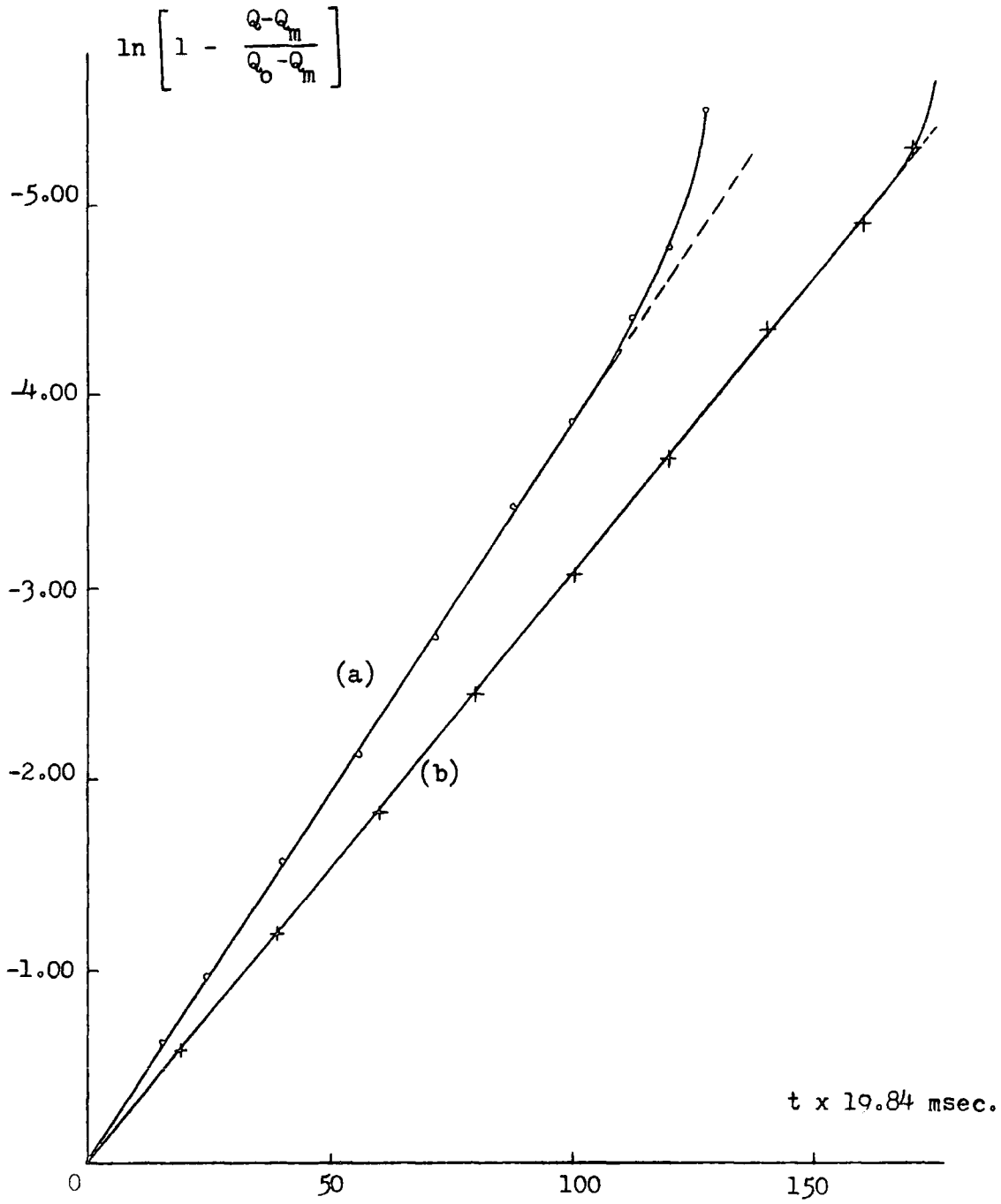


Fig 4.6 : Evaluation of charge-time plots

(a) n-type sample

(b) p-type sample.

(i.e. V_g : 5 to 5.025 volts) which corresponds to the generation characteristics.

From the straight line portion of the plot of $\ln\left[1 - \frac{Q-Q_m}{Q_o-Q_m}\right]$ against t, shown by curve (b) in Fig. 4.6, the time constant τ_r is determined to be 0.645 sec. Using the ratio of $C_{m/C_{ox}}$ = 0.180 (as determined from high frequency measurement) then from Eq.(4.5), the resulting generation lifetime, τ_g, is 5.6 μ sec. On the other hand, using $\Delta Q_{m/\Delta Q_o}$ = 0.184 (as determined from the charge-time plot of curve (a) in Fig. 4.7) yields τ_g = 5.4 μsec which is in excellent agreement.

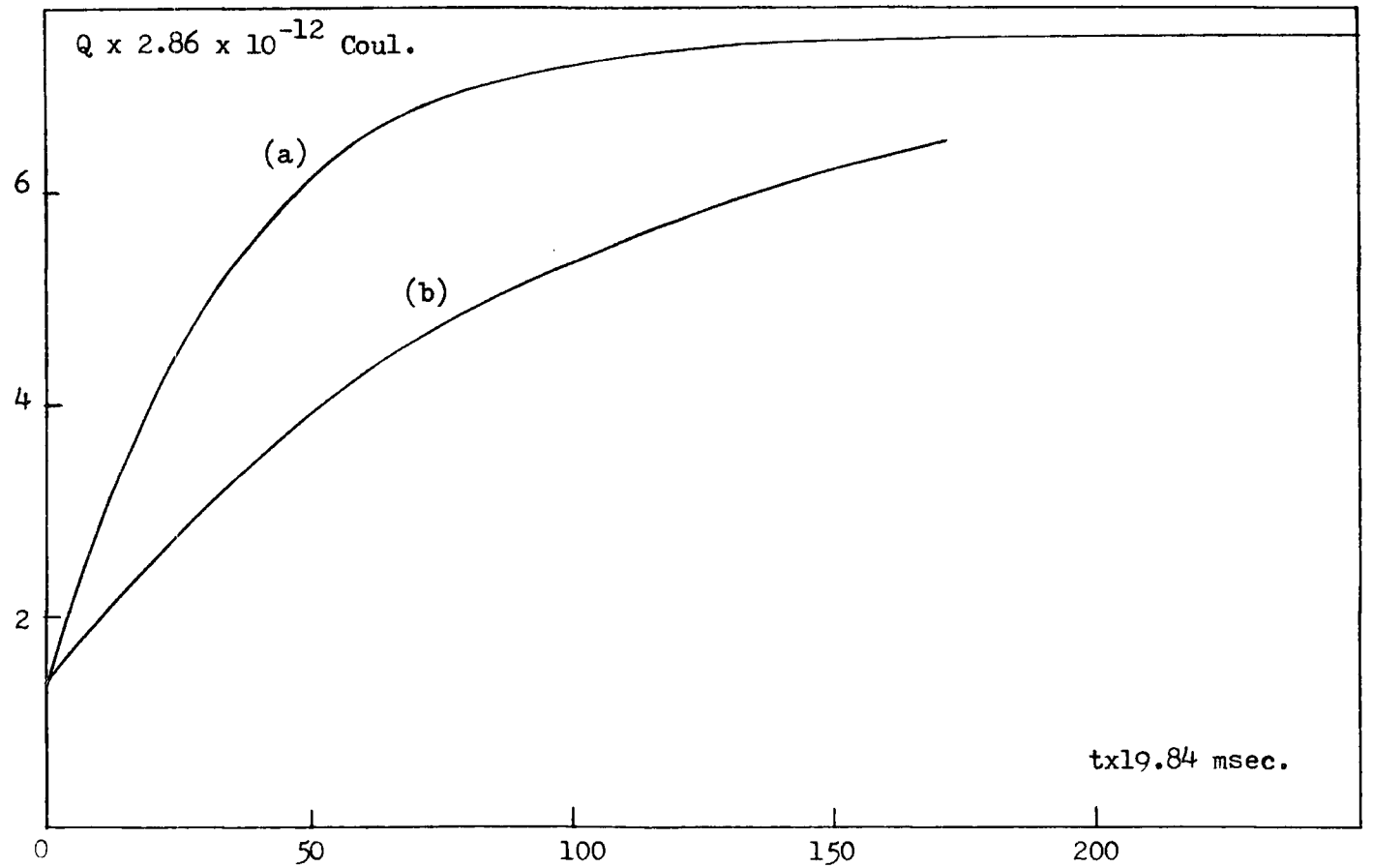


Fig 4.7 : Charge-time plot of p-type MOS sample
(a) obtained from experiment
(b) generated using Eq. (4.5) and (4.9), assuming τ_g = 16 μsec.

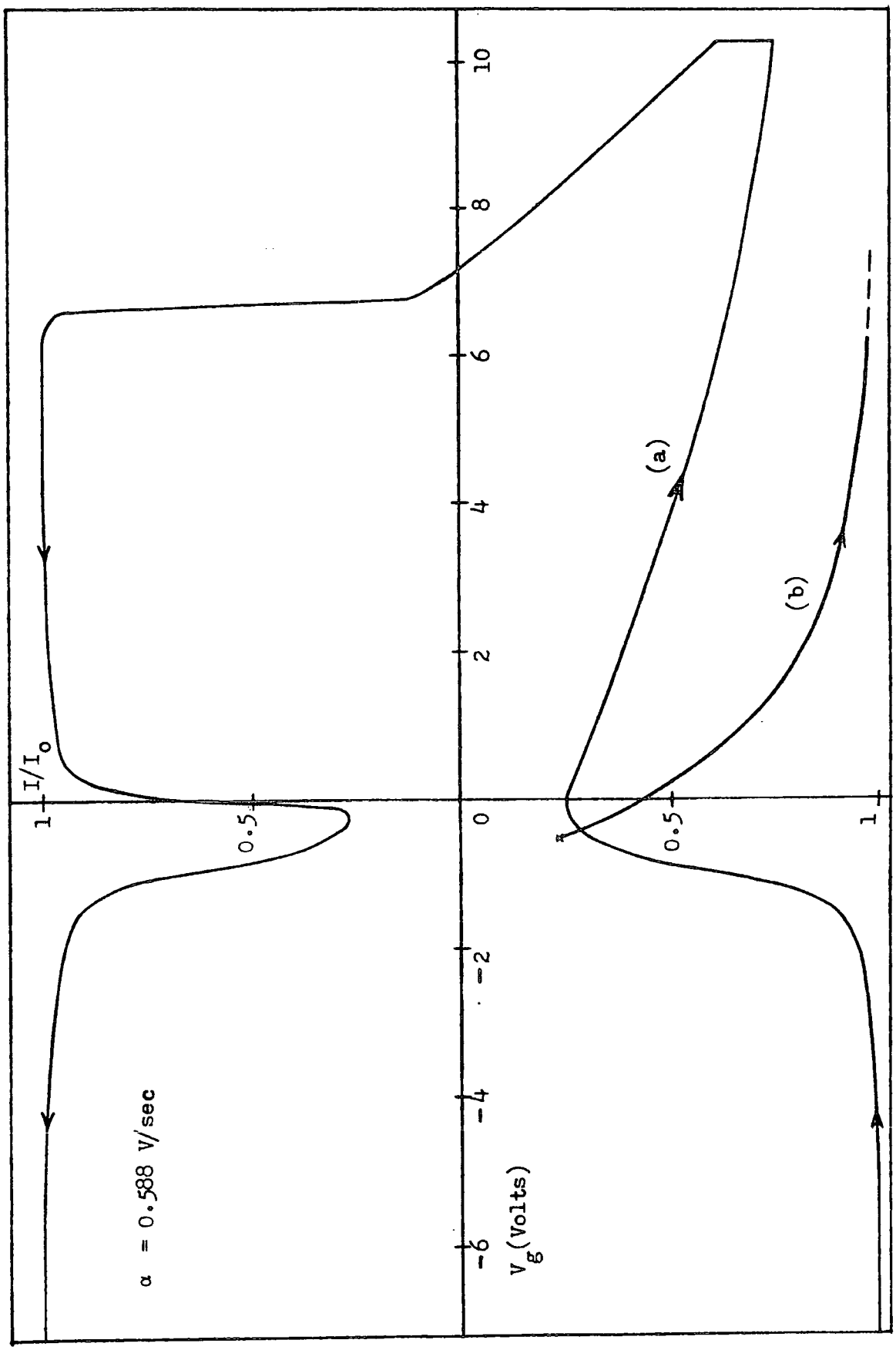


Fig 4.8 : Fast-ramp I-V curves for p-type sample
(a) measured (b) generated if τ_g is assumed to be 5.6 μsec.

4.5 Discussion

The Q-t method as applied to the MOS system allows us to determine the generation lifetime, τ_g. Using the simple theory presented by Hofstein (23), values of generation lifetime were obtained for both samples under consideration.

The generation lifetime for the n-type sample using the Q-t method is 5.9 μsec, whereas from the fast ramp technique as described in Chapter 3, τ_g = 6.0 μsec. There is seen to be excellent agreement between these values.

For the case of the p-type sample, the generation lifetime was found to be 5.6 μ sec from the Q-t method, and 16 μsec from the fast ramp technique. The measurements were checked but the difference of almost a factor of 3 times was definitely not due to an experimental error. To check the calculations further theoretical Q-t and fast ramp I-V curves were calculated using the lifetime values of 16 and 5.6 μsec respectively. In each case these are the lifetimes obtained from the opposite technique. The resulting curves were compared with the experimental ones.

Curve (b) in Fig.4.7 shows the resulting Q-t transient calculated using the simple theory of Hofstein (23) and Equations (4.5) and (4.9) with τ_g = 16 μsec. The large difference between the experimental curve (a) and curve (b) in Fig.4.7 is clearly seen. The curves show that the technique is very sensitive to the value of τ_g and that the difference in the values can not be accounted for by errors in measurement.

A similar comparison is shown for the fast ramp technique in Fig. 4.8. Curve (b) is generated from the theory of Board and Simmons (29), using a generation lifetime of 5.6 μsec. Again a significant difference is observed between curve (a) (τ_g = 16 μsec) and curve (b) (τ_g = 5.6 μsec).

A possible reason for the difference between the two techniques is that interface state generation is not considered in the Q-t analysis. However, the interface state density for these samples is moderately small, as shown by the measurements in Chapter 2, so that any possible effect due to interface states would also be expected to be small. Furthermore, investigations by Schroder and Nathanson (19) showed that the influence of interface state generation under our biasing conditions is small. It would also be difficult to explain why the techniques agree for the n-type sample but not for the p-type, since the interface state densities are very similar.

A more likely reason for the discrepancy could be the very simple model used for the Q-t analysis. Uncertainty about the analysis presented by Hofstein (23) arises from doubts about the expression used for the generation rate, this being valid only for deep depletion in the space charge region (44). The objective of the present work was to use the Q-t technique rather than being concerned with its theory which is the subject of further work in the group. Therefore the following refinements of the theory were not used in practice. Although they might influence the result it seems unlikely that they would change τ_g by as much as three times.

The first improvement in the Q-t theory was due to Zechnall and Werner (44) who obtained good agreement for measurement on many samples when compared with the Zerbst method (18). Later, Viswanathan (45) again modified the Q-t analysis and showed that the method is applicable over a large range of values of step voltage amplitude. Again, the generation lifetime was in good agreement with Zerbst's results.

The comparison between the Q-t and fast ramp methods of obtaining τ_g, in the present work, which has not been done before, shows the need for much more further work on a variety of MOS samples with different doping densities and lifetime values. It is hoped that

such investigations would clarify the cause of the discrepancy in the present results which cannot be explained with the limited data available.

Another factor that can influence MOS measurements is the state of the oxide surface outside the electrode area. For example, the surface may have a permanent inversion layer due to charges in the oxide or its interface with the silicon so increasing the effective area (31). This problem can be overcome by using a suitably-biased guard ring around the measuring electrode. The only samples available for the present work did not have such guard rings, raising the possibility that the results might be influenced by a permanent inversion layer. This would be most likely for the p-type sample due to the predominance of positive oxide charge. Fig 2.17 showed that the flat-band voltage was, in fact, negative for this sample showing that surface inversion was possible.

An independent measurement was therefore made of the effective electrode area for the p-type sample using an ellipsometer to determine the oxide thickness. The result was between 760 and 775 $\mathring{A}$ for different parts of the sample, the average being 767 $\mathring{A}$. The refractive index was 1.455. From the HF measurement of the oxide capacitance, 850 pF (page 37), the effective electrode area was thus 1.88×10^{-2} cm^2 giving a diameter of 1.55 mm. This compares well with the measured value of 1.53 mm from which the oxide thickness of 745 $\mathring{A}$ was obtained earlier. These values agree to well within experimental error so that it could be concluded that there was no permanent surface inversion with this sample.

It is important to consider whether the difference between the lifetime results obtained by the two methods could be influenced by surface inversion. The fast sweep method drives the capacitor into inversion for only a short period of time whereas the Q-t method uses a steady inversion bias. This could possibly influence the surface outside the measuring electrode in a different way but it is unlikely to account for the large difference in the values of τ_g found. Other work in the Department has been concerned with the influence of the potential of a guard ring in Q-t measurements, and it is not large. However, some further work similar to the present should be done using samples with guard rings.

CHAPTER 5

CONCLUSION

CONCLUSION

The present work is mostly concerned with the determination of generation lifetime of silicon MOS devices using the fast ramp and Q-t techniques. Since the comparison of results obtained from the two measurements has not been done before, the work is an important check on both methods.

Some subsidiary measurements were also performed on the same samples. These included the measurement of the fixed interface charge and interface state density spectrum which determined the quality of the devices. The direct measurement of the surface potential-gate voltage relationship, which was also included, provides further confirmation of the fast ramp results.

The fixed interface charge values were obtained from the experimental high frequency C-V characteristics. Both devices show a moderately low magnitude of interface charge (7.5×10^{10} cm^{-2} and 2.8×10^{10} cm^{-2} for the n-type and p-type respectively) which results in a small voltage translation of the C-V characteristics from the ideal.

Quasi-static I-V measurements have been shown by Kuhn (14) to provide an easy method for obtaining the interface state spectrum in an MOS sample. For the devices under consideration, the minimum interface state densities obtained are again quite low, of the order of 4.5×10^{10} cm^{-2} eV^{-1} and 2.5×10^{10} cm^{-2} eV^{-1} around the centre of the gap for n-type and p-type devices respectively, rising towards the band edges. A larger value might have been obtained near the band edges as a result of incorrect determination of the surface potential in this region, and this is one of the errors associated with the quasi-static technique. Although the validity of the resulting value of interface state density can be accepted only in a small region ($\pm$ 0.3 eV) around

midgap, the measurement technique can be confidently used to estimate interface state densities as low as 10^{10} cm^{-2} eV^{-1} in this region.

The experimental non-equilibrium I-V characteristics of the devices in response to a fast linear voltage ramp has been analysed using the theory presented by Board and Simmons (29). The close correlation between experimental and theoretical values for most sections of the curves is demonstrated. This verified the assumption that the most efficacious generation centres are located at midgap or very close to it. It was observed that the interface states have an effect on the initial portion of the forward sweep characteristic although this effect is diminished as the biasing voltage is increased. Every individual I-V curve (which is a function of voltage sweep rate) was analysed to extract the required parameters, thus avoiding the error due to a single measurement.

A simple analogue circuit was found to be very useful for directly generating a plot of surface potential versus gate voltage. Rather than a tedious graphical integration method, such a plot can be easily used in the interface state analysis. When used in the non-equilibrium condition, the resulting $\psi_s - V_g$ plot again showed a close agreement with the theoretically generated plot and with that obtained by graphical integration of the I-V curve. Furthermore, the trend of the non-equilibrium $\psi_s - V_g$ characteristics was observed to have a close relationship to the non-equilibrium I-V characteristics. Hence, any irregularities that appear in the I-V characteristics will also be reflected in $\psi_s - V_g$ curve. Such information could be useful for further investigations in identifying various mechanisms occurring within MOS devices.

The fast ramp analysis indicated a bulk trap density of 1.7×10^{13} cm^{-3} and a generation lifetime of 6.0 μsec for the n-type MOS device. Similar analysis for the p-type MOS device yields a bulk

trap density of 6.3×10^{12} cm^{-3} and a generation lifetime of 16.0 μsec.

Finally, the results from Q-t measurements, analysed using the simple theory of Hofstein (23), gave the value of generation lifetime for comparison with the fast ramp values, as tabulated below :

Method of Measurement	τ_g(n-type) μsec	τ_g(p-type) μsec
Fast ramp	6.0	16.0
Q-t	5.9	5.6

It is difficult to explain why the techniques should agree for the n-type sample but not for the p-type one. Any effect from interface states would be expected to be small since the values measured are quite low. The measurements were checked but the difference of almost a factor of three times (for the p-type sample) was definitely not due to an experimental error. Furthermore, the curves show that the technique is very sensitive to the value of τ_g and that the difference in the values cannot be accounted for by errors in measurement.

The objective of the present work was to use the Q-t technique rather than being concerned with its detailed theory which is the subject of further work in the group. For such reason, only a simple theory of Hofstein (23) is used and the refinements of the theory have not been considered. Although they might influence the result it seems unlikely that they would change τ_g by as much as three times.

In order to understand the cause of the discrepancy in the present results, a further investigation should be made. This should include measurements on many more samples with variable doping density

and including guard rings to ensure that the free surface of the sample is not inverted.

and lifetime values for both n-type and p-type substrates. It would also be important to check the results by using a third method for measuring τ_g (for example C-t method) which was beyond the scope of the present work. It is hoped that such measurements would clarify the discrepancy shown in the present results.

To sum up, the quasi-static and non-equilibrium linear voltage ramp techniques have shown to provide an easy and useful method for characterizing interfacial and bulk traps that occur in metal-oxide-semiconductor structures. The Q-t technique gives a value of generation lifetime which is generally in agreement with that obtained from the fast ramp technique although a far more detailed comparison with other methods should be made in the future.

APPENDIX A

Theoretical C-V Data for an n-type MOS Device

Generated Using the Equations Given in the Text

ND= 6.18E+14 CM-3
A = 7.952E-03 CM2
COX= 2.68E-10 PF
VFB=-.7175 V

LOW FREQUENCY C-V

ψ_s(V)	V_g (V)	C_{sc} (F/cm^2)	C (F/cm^2)	C/C_{ox}
-1	-432.279242	2.80132348E-04	3.36981591E-08	.999879706
-.98	-294.351572	1.90406575E-04	3.3696249E-08	.99982303
-.96	-200.595445	1.29419697E-04	3.36934392E-08	.999739657
-.94	-136.86286	8.79666988E-05	3.36893061E-08	.999617022
-.92	-93.5373958	5.97909034E-05	3.36832271E-08	.999436649
-.9	-64.0827658	4.06396188E-05	3.36742874E-08	.999171393
-.88	-44.0562663	2.76222632E-05	3.3661143E-08	.998781376
-.86	-30.4382187	1.87740778E-05	3.36418213E-08	.99820807
-.84	-21.1761945	1.27595781E-05	3.36134293E-08	.997365631
-.82	-14.675231	8.67098566E-06	3.35717274E-08	.996128269
-.8	-10.5872796	5.89121549E-06	3.35105078E-08	.994311784
-.78	-7.66810639	4.00074296E-06	3.34206779E-08	.991646382
-.76	-5.68004348	2.71429441E-06	3.32888798E-08	.987735715
-.74	-4.32590849	1.83781599E-06	3.30953059E-08	.981992046
-.72	-3.40410217	1.23924925E-06	3.28099254E-08	.973524353
-.7	-2.77807021	8.28759409E-07	3.23852397E-08	.960923231
-.68	-2.3554333	5.4553973E-07	3.1741307E-08	.941816691
-.66	-2.07348605	3.49268229E-07	3.07363469E-08	.911997874
-.64	-1.88880217	2.14483997E-07	2.91256529E-08	.864205939
-.62	-1.76987269	1.25582224E-07	2.65713272E-08	.788414902
-.6	-1.6929219	7.12180891E-08	2.28764803E-08	.678782728
-.58	-1.640615	4.08129703E-08	1.84591564E-08	.547713477
-.56	-1.6016041	2.50562075E-08	1.43715511E-08	.426427517
-.54	-1.56930684	1.73281246E-08	1.14440973E-08	.339565155
-.52	-1.54023902	1.36996549E-08	9.7403058E-09	.289010865
-.5	-1.51265521	1.20863019E-08	8.8960108E-09	.263959246
-.48	-1.48570471	1.14478981E-08	8.54526141E-09	.253551935
-.459999999	-1.45897633	1.12816764E-08	8.45230295E-09	.250793705
-.439999999	-1.43226949	1.13488712E-08	8.48996384E-09	.251911166

-.419999999	-1.40548306	1.15376571E-08	8.59517451E-09	.255032939
-.399999999	-1.37856211	1.17967612E-08	8.73815214E-09	.25927532
-.379999999	-1.35147248	1.2103855E-08	8.90551661E-09	.264241299
-.359999999	-1.32418864	1.24506692E-08	9.09185053E-09	.269770132
-.339999999	-1.2966876	1.28360813E-08	9.295664E-09	.275817612
-.319999999	-1.26894574	1.32630142E-08	9.5175294E-09	.282400723
-.299999999	-1.24093686	1.37371958E-08	9.75926789E-09	.289573501
-.279999999	-1.21263058	1.42668878E-08	1.00236545E-08	.297418286
-.259999999	-1.18399082	1.48632119E-08	1.03143983E-08	.306045131
-.239999999	-1.15497386	1.55409698E-08	1.06362961E-08	.315596369
-.219999999	-1.12552579	1.63200261E-08	1.09955293E-08	.326255408
-.199999999	-1.09557886	1.72274739E-08	1.14001093E-08	.338259959
-.179999999	-1.06504634	1.83009852E-08	1.18604956E-08	.351920377
-.159999999	-1.03381478	1.95940207E-08	1.23904039E-08	.367643625
-.139999999	-1.00173237	2.11839864E-08	1.3007773E-08	.385961982
-.119999999	-.968591273	2.31850697E-08	1.37357266E-08	.407561559
-.0999999992	-.934100194	2.57684523E-08	1.4603063E-08	.433296853
-.0799999992	-.89784188	2.91940051E-08	1.5643271E-08	.464161532
-.0599999992	-.859206936	3.38594862E-08	1.68903334E-08	.501163921
-.0399999992	-.817291228	4.03757092E-08	1.83691809E-08	.545043757
-.0199999992	-.770738243	4.96790765E-08	2.00799824E-08	.595806045
.02	-.654479979	8.30812782E-08	2.39761881E-08	.711412864
.04	-.577007718	1.12550993E-07	2.59359618E-08	.769562568
.06	-.478074029	1.56365371E-07	2.7726238E-08	.822683003
.08	-.34722286	2.21519454E-07	2.92518107E-08	.867949247
.1	-.168943001	3.18259189E-07	3.04750436E-08	.904244576
.12	.0796781841	4.61585753E-07	3.14089228E-08	.931954306
.14	.432395505	6.73487166E-07	3.20960817E-08	.95234344
.16	.938868291	9.86239861E-07	3.25885822E-08	.966956738
.18	1.67211752	1.44727747E-06	3.29352621E-08	.977243298
.2	2.73951041	2.12635684E-06	3.31763762E-08	.98439755
.22	4.29893448	3.12609746E-06	3.33427477E-08	.989334066
.24	6.58260344	4.59748149E-06	3.34569544E-08	.992722765
.26	9.93208774	6.76265184E-06	3.35350885E-08	.995041133
.28	14.849856	9.94844882E-06	3.35884263E-08	.996623752

HIGH FREQUENCY C-V

ψ_s (V)	C_{sc} (F/cm^2)	C (F/cm^2)	C/C_{ox}
-1	7.28660641E-09	5.99126213E-09	.177770584
-.98	7.36258184E-09	6.04253114E-09	.17929182
-.96	7.44098445E-09	6.09523953E-09	.180855764
-.94	7.52194631E-09	6.14945802E-09	.182464515
-.92	7.60560973E-09	6.2052624E-09	.184120323
-.9	7.69212838E-09	6.26273401E-09	.1858256
-.88	7.7816845E-09	6.32196021E-09	.187582939
-.86	7.87441E-09	6.38303509E-09	.189395131
-.84	7.97054847E-09	6.44606004E-09	.191265184
-.82	8.07029642E-09	6.5111446E-09	.19319635
-.8	8.17388553E-09	6.57840728E-09	.195192144
-.78	8.28156881E-09	6.64797654E-09	.197256378
-.76	8.39362328E-09	6.71999192E-09	.199393193
-.74	8.51035288E-09	6.79460535E-09	.201607096
-.72	8.63209206E-09	6.871982555E-09	.203903005
-.7	8.75920967E-09	6.95230475E-09	.206286296
-.68	8.89211379E-09	7.03577063E-09	.208762866
-.66	9.03125718E-09	7.12259857E-09	.211339193
-.64	9.17714383E-09	7.21302928E-09	.214022421
-.62	9.33033658E-09	7.30732886E-09	.216820444
-.6	9.49146638E-09	7.40579239E-09	.219742019
-.58	9.66124315E-09	7.50874824E-09	.222796888
-.56	9.84046903E-09	7.61656307E-09	.225995931
-.54	1.00300543E-08	7.7296479E-09	.229351344
-.52	1.02310371E-08	7.8484654E-09	.232876854
-.5	1.04446072E-08	7.97353863E-09	.236587982
-.48	1.06721356E-08	8.10546182E-09	.240502359
-.459999999	1.09152123E-08	8.24491349E-09	.24464012
-.439999999	1.11756928E-08	8.39267284E-09	.249024382
-.419999999	1.14557581E-08	8.5496409E-09	.253681858
-.399999999	1.17579917E-08	8.71686225E-09	.258643614
-.379999999	1.2085481E-08	8.89556603E-09	.263946049
-.359999999	1.24419497E-08	9.08720011E-09	.269632146
-.339999999	1.28319373E-08	9.29349051E-09	.275753121
-.319999999	1.32610414E-08	9.51651348E-09	.282370579

-.299999999	1.37362549E-08	9.75879301E-09	.28955941
-.279999999	1.42664381E-08	1.00234325E-08	.297411699
-.259999999	1.48629965E-08	1.03142945E-08	.306042053
-.239999999	1.55408663E-08	1.06362477E-08	.31559493
-.219999999	1.63199762E-08	1.09955067E-08	.326254736
-.199999999	1.72274498E-08	1.14000987E-08	.338259645
-.179999999	1.83009735E-08	1.18604907E-08	.35192023
-.159999999	1.95940149E-08	1.23904016E-08	.367643557
-.139999999	2.11839836E-08	1.3007772E-08	.385961951
-.119999999	2.31850684E-08	1.37357261E-08	.407561544
-.0999999992	2.57684515E-08	1.46030627E-08	.433296847
-.0799999992	2.91940048E-08	1.56432709E-08	.46416153
-.0599999992	3.38594861E-08	1.68903333E-08	.50116392
-.0399999992	4.03757091E-08	1.83691809E-08	.545043756
-.0199999992	4.96790765E-08	2.00799824E-08	.595806045
.02	8.30812782E-08	2.39761881E-08	.711412865
.04	1.12550993E-07	2.59359618E-08	.769562568
.06	1.56365371E-07	2.7726238E-08	.822683003
.08	2.21519454E-07	2.92518107E-08	.867949247
.1	3.18259189E-07	3.04750436E-08	.904244576
.12	4.61585753E-07	3.14089228E-08	.931954306
.14	6.73487166E-07	3.20960817E-08	.95234344
.16	9.86239861E-07	3.25885822E-08	.966956738
.18	1.44727747E-06	3.29352621E-08	.977243298
.2	2.12635684E-06	3.31763762E-08	.98439755
.22	3.12609746E-06	3.33427477E-08	.989334066
.24	4.59748149E-06	3.34569544E-08	.992722765
.26	6.76265184E-06	3.35350885E-08	.995041133
.28	9.94844882E-06	3.35884263E-08	.996623752

APPENDIX B

Theoretical C-V Data for a p-type MOS Device

Generated Using the Equations Given in the Text

NA= 6.64E+14 CM-3
A = .018626 CM2
COX= 8.5E-10 PF
VFB=-.96 V

LOW FREQUENCY C-V

ψ_s (V)	V_g (V)	C_{sc} (F/cm^2)	C (F/cm^2)	C/C_{ox}
-.3	-18.4782363	1.51706678E-05	4.54982696E-08	.997000905
-.28	-12.9425708	1.03120538E-05	4.5434069E-08	.995594081
-.26	-9.17329721	7.00981943E-06	4.53399628E-08	.993531936
-.24	-6.60455524	4.76551445E-06	4.52022714E-08	.990514713
-.22	-4.85170188	3.24035293E-06	4.50013623E-08	.986112203
-.2	-3.65326272	2.20407287E-06	4.47094289E-08	.979715086
-.18	-2.83147663	1.50017389E-06	4.42879004E-08	.970478155
-.16	-2.26547969	1.02228586E-06	4.36850218E-08	.957267313
-.14	-1.8730816	6.9810239E-07	4.28349988E-08	.938640808
-.12	-1.59838432	4.7845621E-07	4.16614649E-08	.912925229
-.0999999999	-1.40337331	3.29891217E-07	4.00894099E-08	.87847688
-.0799999999	-1.26220904	2.29615749E-07	3.80690711E-08	.8342053514
-.0599999999	-1.15735175	1.62080356E-07	3.56090859E-08	.780299804
-.0399999999	-1.0769275	1.1666461E-07	3.28035334E-08	.718821899
-.0199999999	-1.01293211	8.61178088E-08	2.98285385E-08	.653631009
.02	-.914555907	5.14947926E-08	2.41941061E-08	.530164024
.04	-.874229424	4.18513973E-08	2.18307217E-08	.47837532
.06	-.837452807	3.50970135E-08	1.98391466E-08	.434734052
.08	-.803187635	3.02610142E-08	1.81954614E-08	.398716075
.1	-.77074179	2.6710261E-08	1.6848706?E-08	.369204717
.12	-.739648774	2.40324586E-08	1.57422472E-08	.344958937
.14	-.709589178	2.19582378E-08	1.48249317E-08	.324857856
.16	-.680340019	2.031016E-08	1.40549358E-08	.307984981
.18	-.651742183	1.87698647E-08	1.3399773E-08	.293628437
.2	-.623679474	1.7857116E-08	1.28348244E-08	.281246752
.22	-.596065038	1.69164984E-08	1.23415911E-08	.27044056
.24	-.568832476	1.6108961E-08	1.19061522E-08	.260898813
.26	-.541929947	1.54064163E-08	1.15179557E-08	.252392286
.28	-.515316176	1.47882647E-08	1.11689256E-08	.244744008
.3	-.488957705	1.42391449E-08	1.08528286E-08	.237817394

.32	-.462826934	1.37474895E-08	1.05648502E-08	.231506941
.34	-.436900669	1.33046516E-08	1.03013533E-08	.22573295
.36	-.411158946	1.29045188E-08	1.00598383E-08	.220440646
.38	-.385583906	1.25436904E-08	9.83919834E-09	.215605774
.4	-.360158412	1.22225454E-08	9.64050931E-09	.211251913
.42	-.33486388	1.19479936E-08	9.46888975E-09	.207491224
.44	-.309676231	1.17396603E-08	9.33756675E-09	.204613551
.46	-.28455776	1.16432463E-08	9.27646871E-09	.203274713
.48	-.259440255	1.17589475E-08	9.3497645E-09	.204880839
.5	-.2341896	1.23012879E-08	9.68943027E-09	.212323915
.52	-.208531717	1.37231835E-08	1.05504897E-08	.23119226
.54	-.18189951	1.69656383E-08	1.23677256E-08	.271013244
.56	-.153125684	2.39296162E-08	1.56980545E-08	.343990544
.58	-.119862888	3.8253333E-08	2.08097255E-08	.456002291
.6	-.0776162683	6.62338747E-08	2.70190268E-08	.592066343
.62	-.0184740892	1.17091124E-07	3.28371658E-08	.719558882
.64	.0699471759	2.01703096E-07	3.72152245E-08	.815495026
.66	.204917515	3.3156184E-07	4.01139722E-08	.879015112
.68	.409309983	5.21579184E-07	4.19635666E-08	.919545166
.7	.714322615	7.9580862E-07	4.3160143E-08	.945765675
.72	1.16468535	1.19277924E-06	4.39534951E-08	.963150352
.74	1.82616042	1.77101357E-06	4.44887561E-08	.974879494
.76	2.79595442	2.61716746E-06	4.48530384E-08	.982861991
.78	4.21762362	3.85867568E-06	4.51017322E-08	.988311603
.800000001	6.30284134	5.68278864E-06	4.52715842E-08	.992033562
.820000001	9.3633891	8.36475437E-06	4.53875155E-08	.994573957
.840000001	13.8582344	1.23093303E-05	4.54665727E-08	.996306333
.860000001	20.4628144	1.81118612E-05	4.55204392E-08	.997486705
.880000001	30.170988	2.66481304E-05	4.55571168E-08	.99829042
.900000001	44.4450466	3.92065422E-05	4.55820777E-08	.998837386
.920000001	65.4364258	5.76825844E-05	4.55990584E-08	.999209483
.940000001	96.3104333	8.48649206E-05	4.56106071E-08	.999462551
.960000001	141.724002	1.24856295E-04	4.56184601E-08	.999634632
.980000001	208.528584	1.83692778E-04	4.56237993E-08	.99975163

HIGH FREQUENCY C-V

ψ_s (V)	C_{sc} (F/cm^2)	C (F/cm^2)	C/C_{ox}
-.3	1.51706678E-05	4.54982696E-08	.997000905
-.28	1.03120538E-05	4.5434069E-08	.995594081
-.26	7.00981943E-06	4.53399628E-08	.993531936
-.24	4.76551445E-06	4.52022714E-08	.990514714
-.22	3.24035293E-06	4.50013623E-08	.986112203
-.2	2.20407287E-06	4.4709429E-08	.979715086
-.18	1.50017389E-06	4.42879004E-08	.970478155
-.16	1.02228586E-06	4.36850218E-08	.957267313
-.14	6.9810239E-07	4.28349988E-08	.938640808
-.12	4.7845621E-07	4.16614649E-08	.912925229
-.0999999999	3.29891217E-07	4.00894099E-08	.87847688
-.0799999999	2.29615749E-07	3.80690711E-08	.834205314
-.0599999999	1.62080356E-07	3.56090859E-08	.780299804
-.0399999999	1.1666461E-07	3.28035334E-08	.718821899
-.0199999999	8.61178088E-08	2.98285385E-08	.653631009
.02	5.14947925E-08	2.41941061E-08	.530164024
.04	4.18513972E-08	2.18307217E-08	.47837532
.06	3.50970134E-08	1.98391466E-08	.434734051
.08	3.02610139E-08	1.81954613E-08	.398716072
.1	2.67102604E-08	1.68487064E-08	.369204712
.12	2.40324574E-08	1.57422467E-08	.344958926
.14	2.19582352E-08	1.48249305E-08	.324857831
.16	2.03101549E-08	1.40549333E-08	.307984927
.18	1.89698542E-08	1.33997677E-08	.293628322
.2	1.78570943E-08	1.28348132E-08	.281248507
.22	1.69164536E-08	1.23415673E-08	.270440038
.24	1.61088681E-08	1.19061014E-08	.2608977
.26	1.54062229E-08	1.15178476E-08	.252389916
.28	1.47878609E-08	1.11686952E-08	.244738961
.3	1.42383001E-08	1.08523376E-08	.237806639
.32	1.37457181E-08	1.05638041E-08	.231484017
.34	1.33009306E-08	1.02991225E-08	.225684066
.36	1.28966895E-08	1.00550797E-08	.220336371
.38	1.25271922E-08	9.82904453E-09	.215383274
.4	1.21877336E-08	9.61883901E-09	.210777053

.42	1.18744536E-08	9.42264245E-09	.20647781
.44	1.15841523E-08	9.23891884E-09	.202451885
.46	1.13141515E-08	9.06636168E-09	.19867065
.48	1.10621906E-08	8.90385133E-09	.19510957
.5	1.08263462E-08	8.75042167E-09	.191747475
.52	1.06049705E-08	8.60523379E-09	.188565982
.54	1.0396642E-08	8.46755507E-09	.185549036
.56	1.02001275E-08	8.33674228E-09	.182682543
.58	1.00143511E-08	8.21222791E-09	.179954067
.6	9.83836919E-09	8.09350897E-09	.177352586
.62	9.67135027E-09	7.98013778E-09	.17486829
.64	9.51255848E-09	7.87171432E-09	.172492413
.66	9.36133984E-09	7.76787979E-09	.170217093
.68	9.2171109E-09	7.66831133E-09	.168035255
.7	9.07934928E-09	7.57271742E-09	.165940511
.72	8.94758567E-09	7.48083409E-09	.163927077
.74	8.82139706E-09	7.3924216E-09	.1619897
.76	8.7004011E-09	7.30726161E-09	.160123594
.78	8.58425117E-09	7.22515482E-09	.158324392
.800000001	8.47263218E-09	7.14591881E-09	.156588098
.820000001	8.365257E-09	7.06938629E-09	.154911046
.840000001	8.26186338E-09	6.99540346E-09	.153289864
.860000001	8.16221115E-09	6.92382664E-09	.15172145
.880000001	8.06608E-09	6.8545311E-09	.150202937
.900000001	7.97326733E-09	6.78738992E-09	.148731676
.920000001	7.88358652E-09	6.72229312E-09	.147305214
.940000001	7.79686529E-09	6.65913678E-09	.145921273
.960000001	7.71294437E-09	6.5978243[illegible]E-09	.144577736
.980000001	7.63167623E-09	6.53[illegible]2e587E-09	.143272635

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