Gas effects on the interface state spectrum of mis devices

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GAS EFFECTS ON THE INTERFACE STATE SPECTRUM OF MIS DEVICES

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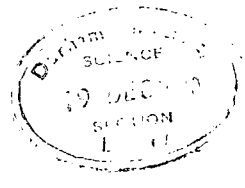

Abstract

A semiautomatic measurement system has been developed for investigating the electronic structure of the interface between an insulator and a semiconductor. The associated microcomputer possesses advanced software which leads to simple operation particularly when used in the real time mode. An attractive feature of the technique is that admittance data are evaluated in the voltage domain using a modified version of the Simonne method.

The system has been used to investigate the effects of gases on the interface state spectrum of MIS devices; the action of hydrogen upon the palladium-silicon dioxide-silicon system receiving the most attention. An alternative insulator to silicon dioxide has been considered, namely organic Langmuir films. Overall there has been little detectable change in the surface state density, although results with different semiconductors appear to be more encouraging.

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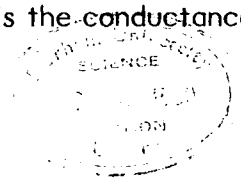
CONTENTS

Chapter I

Introduction

The electronic structure of the interface between an insulator and a semiconductor is of paramount importance in field effect devices such as the metal-oxide-semiconductor (MOS) capacitor shown in figure 1.1. The electrical properties of this type of device are dependent upon the presence of trapping centres located at the insulator-semiconductor boundary known as surface or interface states. These are able to communicate with mobile carriers in the semiconductor and make a contribution to the measured admittance characteristic. The interface state density (N_{ss}) is influenced by impurities or defects which may be introduced accidentally during the processing of the device. In this thesis, a novel development of the standard interface state density determination procedure is presented. The microprocessor-controlled instrumentation described enables not only rapid evaluation of the surface state density, but also easy location of this density with respect to the band edges which previously had required a separate measurement.

The necessary theory for the comprehension of the operation of metal-insulator-semiconductor (MIS) devices is outlined in Chapter 2. This is done by progressing from a microscopic atomic view of the system through a consideration of the role of charge in various regions of the device to a macroscopic circuit element type of approach. (As in Chapter 3, only a brief summary is given; fuller details will be found in the references.) In Chapter 3, a review is presented of the various electrical techniques that utilise MIS devices to obtain interface state density information. The technique that offers the most detail with the best accuracy is the conductance



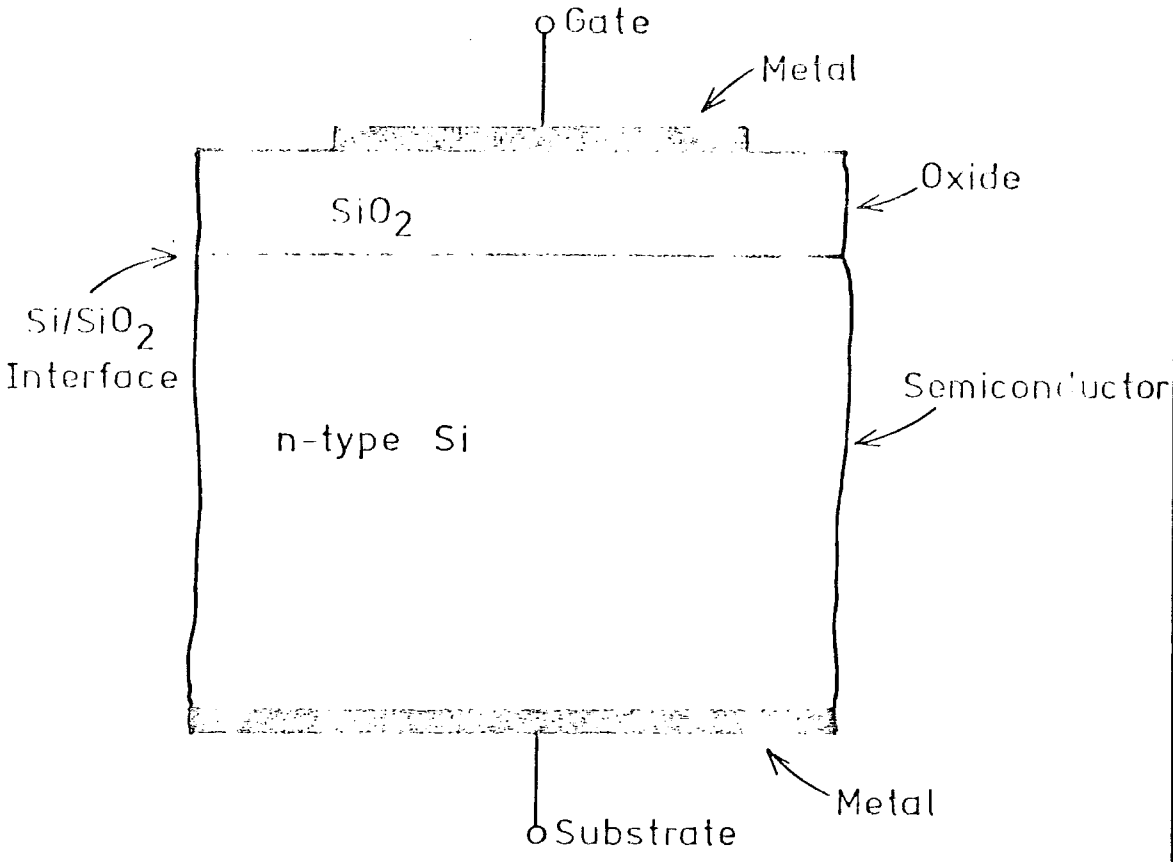


Figure 1.1 Structure of the MOS capacitor.

technique of Nicollian & Goetzberger (1). Unfortunately, however, it is extremely tedious in practice and part of this work has been spent developing a method to reduce the effort involved. This was achieved with the aid of a microprocessor used in a real time mode. This and ancillary equipment are described in Chapter 4 whilst the measurement procedure is outlined in Chapter 5.

The recent need to efficiently interface microelectronic equipment to the outside world has led to a renewed interest in comprehending the effect of the ambient on electronic device structures. We were particularly interested in the change in surface state density of MIS capacitors although, as outlined in the introduction to Chapter 6, other parts of the structure can be influenced. These effects are monitored through measurement of the electrical response. Several workers (2,3) have indicated that surface states may be influenced by the ambient surrounding the device but, owing to the lack of a fast accurate measurement technique, this subject has been little explored. One particular example is the controversy over the role of hydrogen in palladium-coated MOS devices (3,4), which we have tried to resolve using our equipment. The results that we have obtained are described in Chapter 6. We have also investigated the effect of gas on MIS devices incorporating novel Langmuir film insulators. The preparation of these organic monomolecular based films and the gas effects upon them are described in Chapter 7.

Chapter 2

Theory of the Insulator-Silicon Interface

2.1 Introduction

There are two main ways to acquire an understanding of the action of defects at the insulator-silicon interface. The first, a microscopic approach, gives an atomic view, and is obtained through a chemical consideration using optical and electron scanning techniques such as ESR (1). Alternatively the interface can be viewed in a macroscopic fashion, characterized by parameters derived from electrical measurements. Accordingly, in this chapter, a physical model is initially outlined which is then developed into an electronic consideration of the metal-insulator-semiconductor diode whose properties we have examined.

2.2 The Atomic Approach

When a collection of semiconductor atoms comes together to form a crystal, there is an interaction between the extreme orbitals with the formation of bands of permitted energy where electrons are allowed to reside. The outermost occupied bands are known as the valence and conduction bands and are separated by a forbidden band (or gap) in electron energy, which in a perfect lattice is devoid of electrons. Whenever the periodicity of the crystal matrix is interrupted by the presence of lattice defects or impurity atoms, then this arrangement will be perturbed. Generally this perturbation manifests itself as an extra amount of energy levels that may be situated in the forbidden gap. Such levels located in the bulk of the material are known as bulk traps, whereas at the surface or at an interface they are called

surface or interface states. The surface of the crystal itself also represents an interruption of this lattice and gives rise to surface states. In silicon these are thought to be due to dangling bonds formed by incompletely filled orbitals of the sp^3 hybridisation of the atoms; one per surface atom on clean cleaved silicon, except for the (111) direction (2).

The growth of silicon dioxide reduces the number of surface states by saturating dangling bonds; however, as can be seen from figure 2.1, the silicon dioxide lattice does not quite match the silicon one, and so there will always be a fraction of unsaturated bonds. As a consequence of this misfitting, there will be imperfections which will give rise to strain and other defects. In fact there is a transition region 0.5 to 1 nm wide where SiO_x ($x < 2$) occurs; thus it can be seen that there will be various unsatisfied bonds in different environments. Several models (3) have been proposed to try and correlate the chemical and electronic nature of the interface in order to explain the origin of two different types of defects that are found. These are fast states which are able to exchange charge very quickly with the silicon and fixed charge (Q_{ss}) which cannot. We shall concentrate on two of them.

(1) The Trivalent Silicon Model (4)

This model is based on the concept of trivalent silicon which can take three different forms (see figure 2.2):

$:Si_s$ bound to three silicon atoms

$:Si_o$ bound to three oxygen atoms

$:Si_{os}$ bound at the interface

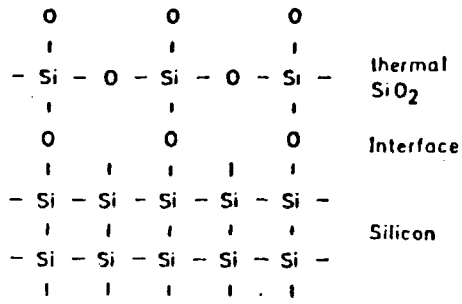


Figure 2.1 Simple schematic diagram of the silicon-silicon dioxide interface. (19)

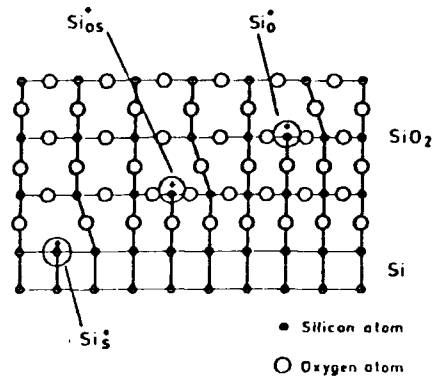


Figure 2.2 The silicon-silicon dioxide interface with three trivalent silicon defects (4)

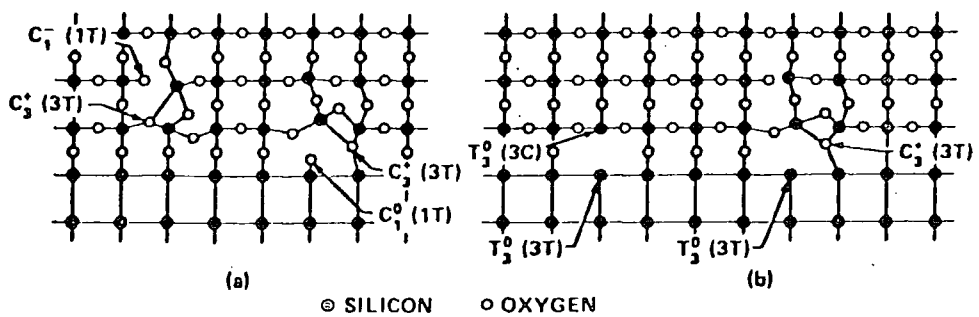


Figure 2.3 The silicon-silicon dioxide interface with various defect pair configurations. (5)

The first is considered to be a surface state whilst the second two are assumed to be hole traps; the latter much deeper energywise due to its interaction with the silicon surface. This is possibly of the image force type and leads to a lowering of the energy of the defect, so much so that it is assumed to be above the conduction band edge and therefore permanently ionized to $:Si^{+}_{os}$. It is therefore the source of the fixed oxide charge.

The above model can be used to explain several of the experimentally encountered properties. For example, it is well known that the surface state density of $Si\text{-}SiO_2$ is reduced by low temperature annealing in a hydrogen atmosphere (3). The following reaction of the $:Si_s$ centre with interstitial hydrogen (H_i) accounts for this by bond saturation:

$$:Si_s + H_i \rightleftarrows :Si_s\,H \qquad (2.1)$$

The reverse reaction represents the increase of surface state density that occurs on annealing at high temperatures and corresponds to the thermal dissociation of the SiH bond. Hydrogen annealing has no effect on oxide charge because Si^{+}_{os} is in an unreactive low energy condition. However, the concentration of the above three defects is correlated at high temperatures where the following occurs

$$:Si_o \rightleftarrows :Si_{os} \rightleftarrows :Si_s \qquad (2.2)$$

(2) The Defect Pair Model (5)

The second model is based on defect pairs rather than single ones, as above, and follows on from the Street & Mott concept (6) that two dangling bonds might be energetically more stable as two charged centres, the more positive centre lowering its energy by forming three bonds. This reaction is represented by the following equation:

$$2\ C_2^o \rightarrow C_3^+ + C_1^- \qquad (2.3)$$

The superscript refers to the charge state, C represents an oxygen atom (we shall use T for silicon), and the subscript refers to the covalent coordination (that is, the number of atomic bonds). For example, in bulk silicon dioxide, C_1^- could be a non-bridging negatively-charged oxygen atom bonded to a :Si atom, whereas C_3^+ could be an oxygen atom bonded to three silicon atoms of the network. Such a pair of defects is shown on the left of figure 2.3a.

However, the defects right at the interface are more interesting since they can be used to explain various phenomena there. If we assume that the electron associated with the C^- centre has been injected into the bulk, which is highly likely considering its location, we then have C_1^o (1T), C_3^+ (3T) - the terms in brackets specifying the atoms that are bonded to the oxygen atoms. The former, which is ESR-active, accounts for the P_c centre seen by Nishi (7), whereas the latter can be associated with the positive space charge, Q_{ss}, which again is in a low energy state and thus impervious to the action of hydrogen. If oxygen vacancies are present through imperfection then we have the situation in figure 2.3b that explains the origin of two other ESR defects P_a and P_b. The P_b

centre represents the aforementioned dangling bond which can be annealed by hydrogen action through a similar reaction to the above; indeed it has been shown by experiment (8) that the magnitude of the ESR P_b signal is reduced at the same time.

Now let us consider the influence of extrinsic impurities which may also give rise to surface states. Again there is no absolute theoretical evaluation of their effect and, to further complicate matters, some of the experiments which indicate that extrinsic impurities are the source of surface states are open to question. For example, sodium ions, well known for causing instability problems through their high mobility in silicon dioxide, have been shown to introduce a surface state 0.05 eV below the conduction band edge (9). Some workers (10), however, maintain this is a spurious result due to surface potential fluctuations (see section 2.54). Another example is that supposed surface states introduced by ion implanted impurities, previously thought to be due to those impurities (11), have been shown to be caused by the damage that the implantation produces (12). This was proved by high temperature annealing of the samples which made the above surface states disappear.

It may be the case that the location of the extrinsic impurities restrict them from contributing to the surface state density for the following two reasons. Firstly, interstitial impurities, because of their various possible interstitial spatial locations, do not give rise to identical energy level positions within the band gap and therefore do not augment each other to produce a significant state. Secondly, in general, most imperfections that lie in the oxide will have their resultant energy levels outside the bandgap (13). Since

this is where they are likely to be gettered, owing to the preferential incorporation of impurities in a disturbed region, then this might also explain their lack of effect. On the other hand though, certain elements such as gold (see section 4.24), germanium (14) and the group III & V standard dopant atoms (15) have been conclusively shown to introduce surface states, but the actual mechanism is yet to be fully explained.

The distribution of surface states in energy throughout the bandgap can have various forms: it can be a single level which could be caused by a specific impurity as has just been outlined (a in figure 2.4a); it may be spread throughout the bandgap (b in figure 2.4a); or it may be a combination of the two. In practical silicon-silicon dioxide devices, an intrinsic U-shaped distribution is obtained, upon which is superimposed structure introduced by extrinsic impurities. The intrinsic spectrum can be separated into two groups of states due to the different response of the N_{ss} distribution to physical and chemical influences across the bandgap (16). The central portion is found to be particularly influenced by technological processing and the states here may be attributed to dangling bonds. The states that compose the rise towards the band edges are insensitive to a wide range of treatments and are thought to result from bond distortion and strain.

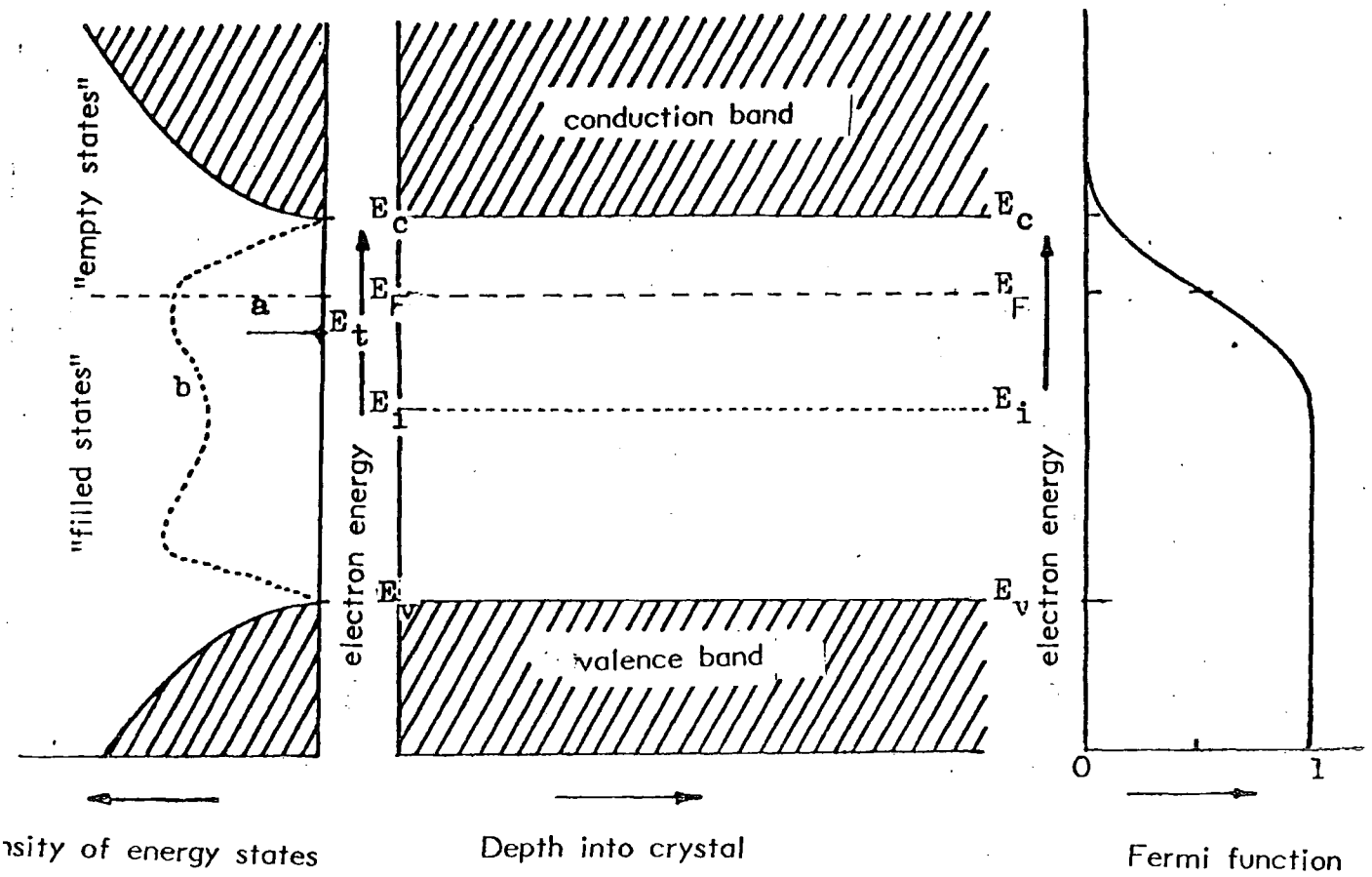


Figure 2.4 Band diagram near the interface and the degree of occupancy of electron states and surface states . (a = single level; b = continuum of states) Flat band situation.

2.3 The Charge Approach

2.31 The Fermi Function

Surface states are localized energy levels that can be occupied by electrons. The degree of occupancy of all levels, including surface and energy band states, is determined by the Fermi function, F(E), given below and shown in figure 2.4. In the expression, degeneracy factors have been ignored: normally, these are equal to 1/2 or 2, but in many situations, for example those where multivalent impurities are involved, the spin degeneracy factor can depart from these two values.

$$F(E) = 1/(1 + \exp (E - E_F)/kT) \qquad (2.4)$$

where:

E = Energy of the state

E_F =Fermi (level) energy

k = Boltzmann's constant

T = Absolute temperature

Energy levels far below the Fermi level are occupied since F(E) is approximately equal to one, whilst those far above are essentially empty. Whenever the Fermi level is shifted with respect to the band edges, the occupancies of the energy levels will alter, particularly those close to the Fermi level. It follows from the latter that the states close to the Fermi energy usually dominate the electrical response of the structure. Positive holes obey the same statistical laws as electrons and their behaviour can be described in terms of the same parameters. If F(E) is the fraction of quantum states occupied by electrons, then (1 - F(E)) is the fraction occupied by holes. Thus

the Fermi function for these particles is:

$$1 - F(E) = 1/(1 + \exp (E_F - E)/kT) \qquad (2.5)$$

The energy required to eject an electron at the Fermi energy to the vacuum level is defined as the work function, ϕ, of the material. When a metal and semiconductor are joined, it is the difference in their work function values that determines the nature of the contact between them. That is, to maintain a thermodynamic equilibrium, the two Fermi levels must coincide. In an ideal situation where there are no surface states, the flow of charge that results will give rise to a bending of the bands at the semiconductor surface. If the work function of the metal is the larger, then electrons flow from the semiconductor to the metal producing a depletion region in the semiconductor (see figure 2.5b,h). A potential barrier to electron flow from the metal to the semiconductor whose height is independent of applied potential is also formed. This is the situation normally envisaged for a Schottky barrier diode (17). Conversely, if the semiconductor has the larger work function, then electron flow is reversed and an Ohmic contact is obtained (see figure 2.5d,f). Unlike a Schottky barrier, an Ohmic contact permits current flow in both directions. However, the flow may not necessarily be Ohmic in nature, as the name implies; under certain conditions, space charge limited conduction can occur.

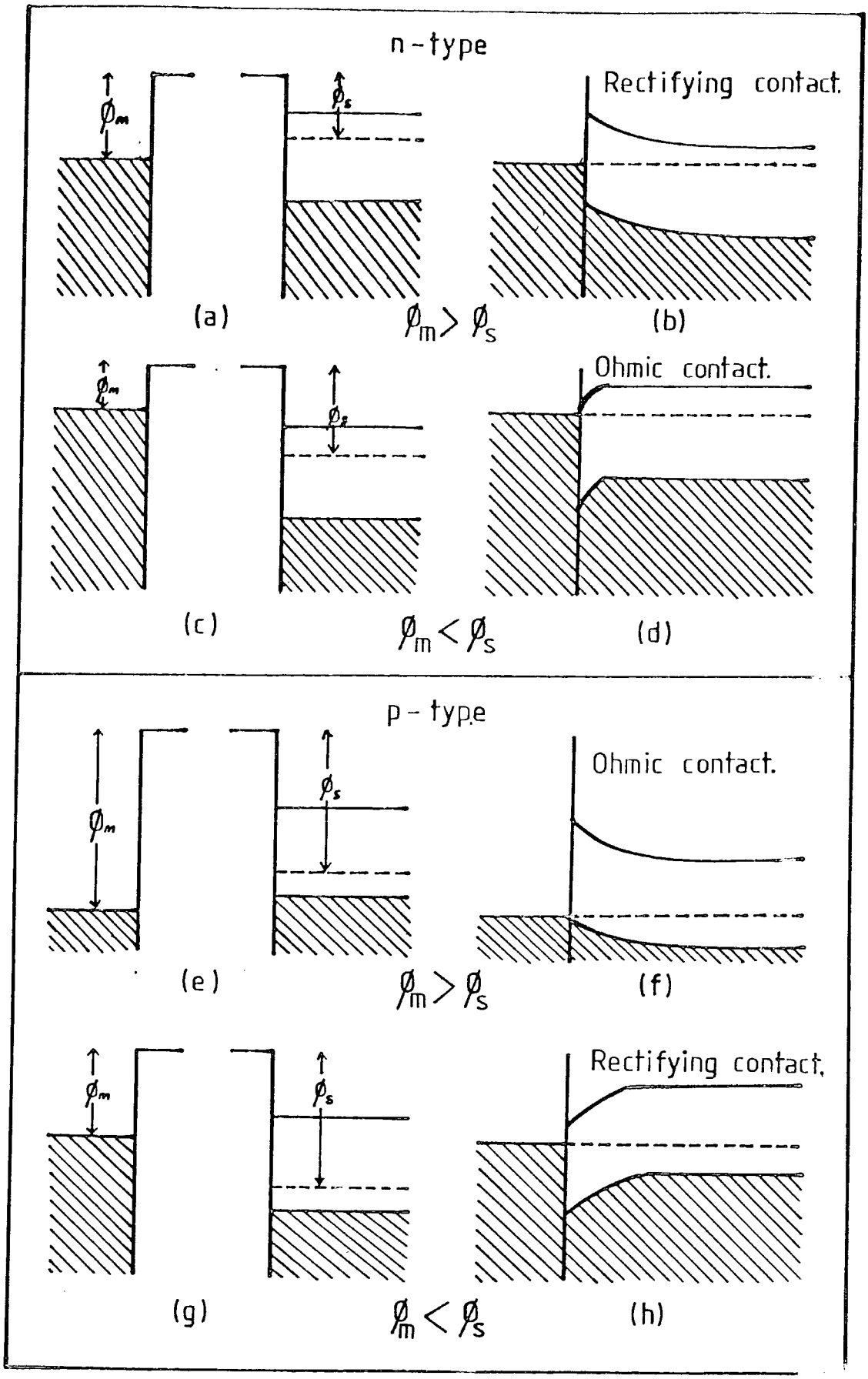


Figure 2.5 Energy band diagrams for metal/semiconductor contacts for p and n-type semiconductors. ϕ_m, ϕ_s are the work functions of the metal and semiconductor respectively.

2.32 The Surface Space Charge Region of the Semiconductor

When a bias is applied to a Schottky barrier diode, the width of the depletion region alters, which in turn affects the amount of charge stored at the semiconductor surface. The charge storage situation is complicated when an interfacial layer exists between the semiconductor and the metal for, if the layer acts as an insulator, accumulation of free carriers at the semiconductor surface is possible. This structure is known as a metal-insulator-semiconductor diode (see figure 1.1). The state of the semiconductor surface can be classified by the value and polarity of the surface potential Ψs, which corresponds to the degree of bandbending and is defined in figure 2.6. Practically, there are three possible cases for a biased surface state free diode; these are shown in figure 2.7 for an n-type semiconductor (see figure 2.8a for a p-type semiconductor):

a)ACCUMULATION, for $\Psi s<0$ for p-type and $\Psi s>0$ for n-type, majority carriers are attracted to the surface and accumulate there. The Fermi level at the surface is in the proximity of the majority carrier band edge.

b)DEPLETION, for $\Psi s>0$ for p-type and $\Psi s<0$ for n-type, majority carriers are repelled from the surface leaving uncompensated ionized (donor or acceptor) impurities.

c)INVERSION, if Ψs increases further, the minority carrier density exceeds the majority carrier bulk density and forms an inversion region. The onset of inversion corresponds to the point at which the Fermi level crosses the intrinsic Fermi level, E_i, at the surface.

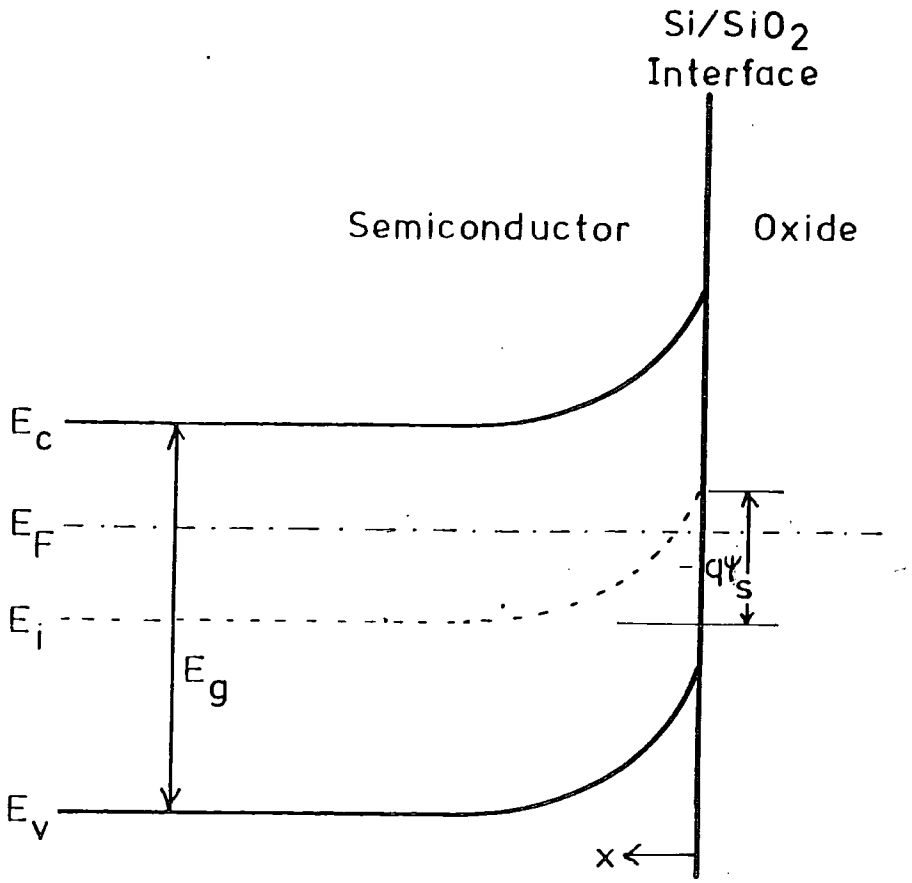


Figure 2.6 Band diagram of an MIS diode (Depletion situation).

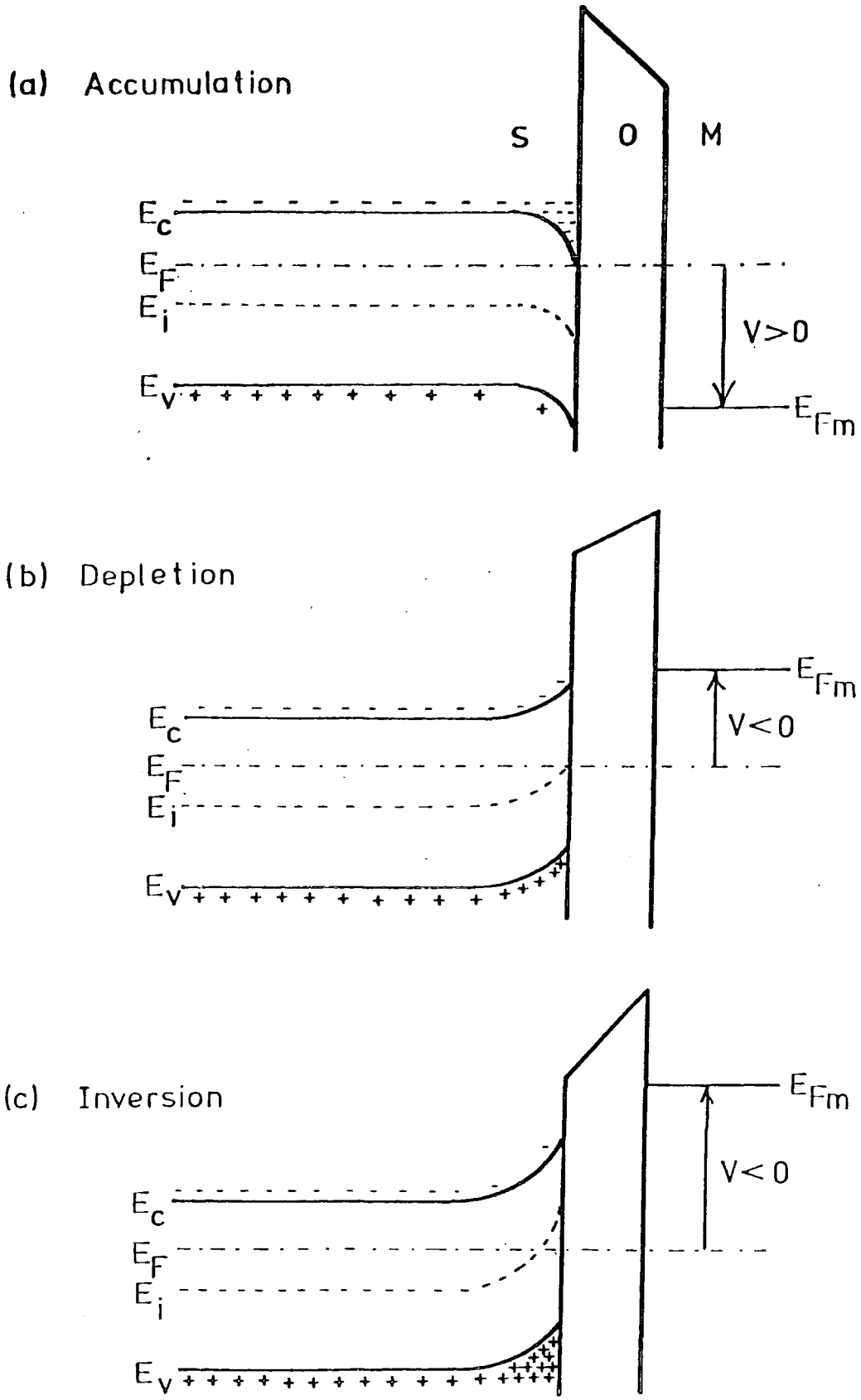


Figure 2.7 Energy band diagrams for an MOS structure depicting (a) accumulation, (b) depletion, (c) inversion.

The surface potential may be substituted into the standard expressions relating bulk potential to concentration in order to obtain the electron and hole surface densities (18).

$$n_s = n_{bulk} \exp(q\Psi s/kT) \qquad (2.6)$$

$$p_s = p_{bulk} \exp(q\Psi s/kT)$$

In addition the surface electric field, potential and charge concentration can be found by integrating Poisson's equation and by using Gauss's law (see figure 2.8).

When surface states are present, charge is distributed among these states and the silicon space charge region, such that the following charge neutrality condition holds:

$$Q_{ss} + Q_{sc} = - Q_G \qquad (2.7)$$

where these quantities correspond to charge in surface states, in the silicon space charge region and at the metal electrode respectively. These quantities represent effective charges without regard to the complexity of their distribution; charge exchange equilibria also exist between these various regions.

2.4 The Capacitance Approach

2.41 Semiconductor Surface Capacitance

Since the net charge in the semiconductor varies as the surface potential across the surface layer is changed, a differential

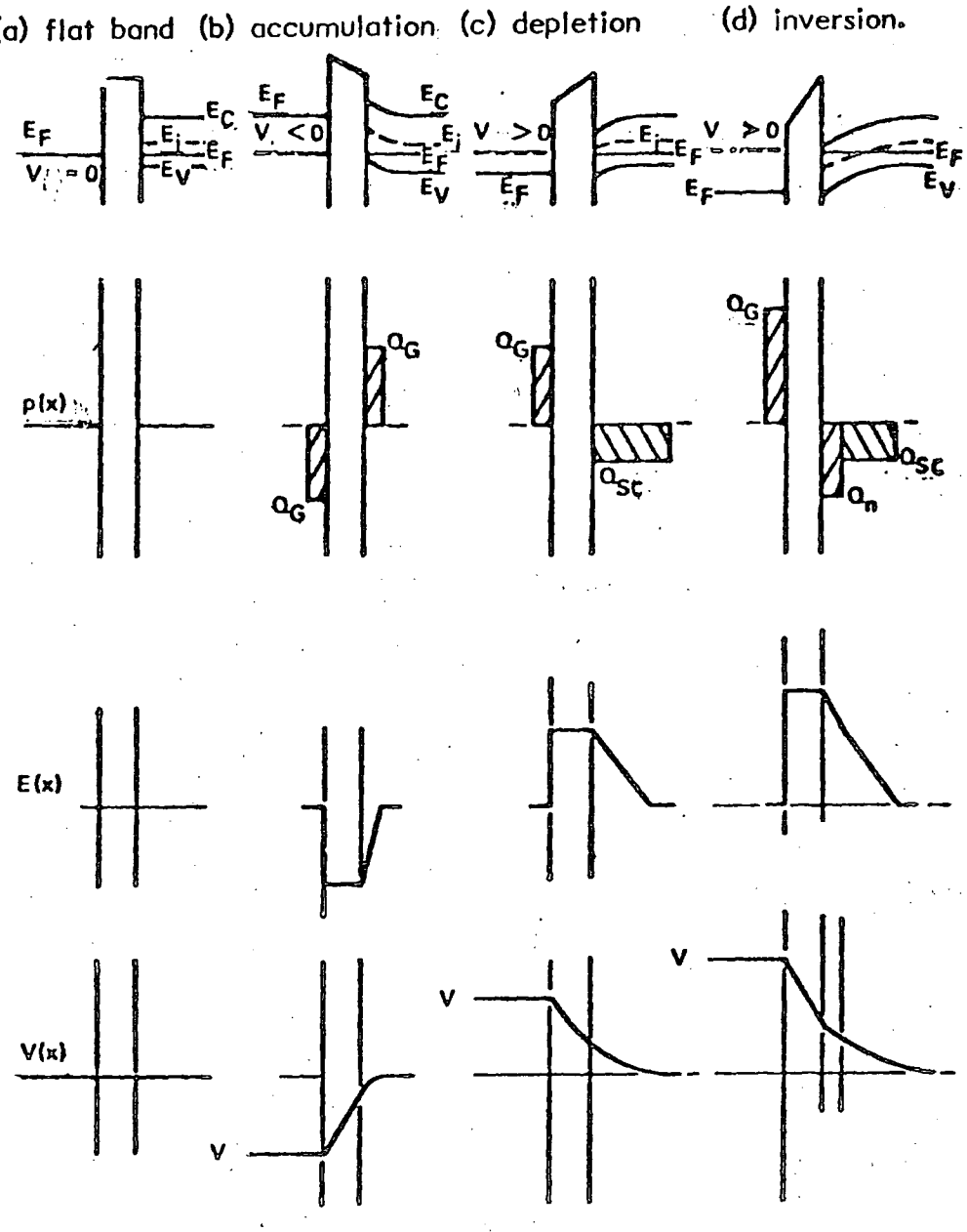


Figure 2.8 Band diagrams, charge, field, and potentials for a p-type substrate for (a) flat band, (b) accumulation, (c) depletion and (d) inversion.

capacitance, C_{sc}, can be associated with the semiconductor surface. This capacitance per unit area is defined as:

$$C_{sc} = \frac{dQ_{sc}}{d\Psi_s} \tag{2.8}$$

and it is measured by superimposing an alternating voltage upon the applied dc bias. For a Schottky barrier, the surface potential is directly related to the applied bias, V, and the semiconductor capacitance is simply:

$$C_{sc}^{-2} = \frac{2\,(V_b - V - kT/q)}{\varepsilon_s N_d q} \tag{2.9}$$

where V_b is dependent on the barrier height within the diode and N_d is assumed to be the constant doping density of the semiconductor. Experimental values for these can obviously be obtained from an appropriate plot of this expression. For an MIS diode, the relationship between capacitance and surface potential is far more complicated (19), although it does reduce to a similar expression to the above in the depletion region. In the depletion and accumulation regions, the semiconductor capacitance is independent of frequency but, in the inversion region, it depends on the ability of the minority carriers to follow the applied bias and/or ac signal.

A differential capacitance can also be associated with the charge in the surface states, when present, which is defined as:

$$C_{ss} = \frac{dQ_{ss}}{d\Psi_s} \tag{2.10}$$

Unlike C_{sc}, which is a unique function of ψ_s for a given impurity concentration and temperature, C_{ss} depends upon the particular spatial and energy distribution of surface states, their occupancy as determined by an external field and the frequency of the ac measurement signal. Since the total surface charge is the sum of Q_{sc} and Q_{ss}, the semiconductor surface capacitance, C_p, is thus:

$$C_p = C_{ss} + C_{sc} \tag{2.11}$$

Therefore, it can be seen that the semiconductor surface capacitance is a parallel combination of C_{ss} and C_{sc}.

2.42 Capacitance of an Ideal MIS Diode

An MIS capacitor is formed by the addition of an insulator in series with the semiconductor, so the capacitance, C, of the whole structure is:

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{sc} + C_{ss}} \tag{2.12}$$

where C_{ox} is the geometrical capacitance per unit area of the insulator. The voltage bias applied to an MIS diode falls partially across the insulator and partially across the semiconductor so

$$V_G = V_{ox} + \psi_s \tag{2.13}$$

where V_{ox} is the voltage dropped across the insulator given by

$$V_{ox} = \frac{Q_G}{C_{ox}} \qquad (2.14)$$

In an idealized case where the insulator is charge free, there is no work function difference between metal and silicon, and no surface charges exist; the C-V curve is called "ideal". Figure 2.9 shows such a curve with three different inversion options: (1) if the minority carriers can follow the applied ac signal; (2) if they cannot; and (3) if they cannot follow the ac signal but if they can follow the dc signal. The left of the curve corresponds to accumulation where there is a high concentration of majority carriers at the surface, holes in this case. As a result the total capacitance is close to the insulator capacitance. By increasing the applied voltage, the bands are made flat which corresponds to a surface potential of zero as indicated on the curve. Further increase produces a depletion region which acts as a dielectric in series with the insulator and therefore decreases the capacitance. Eventually inversion is reached and in equilibrium a minimum capacitance is obtained.

The shape of the capacitance-voltage characteristic varies for different insulator thicknesses and semiconductor doping densities. Goetzberger (20), has provided not only a set of ideal characteristics with respect to these two parameters, but also curves relating surface potential to applied voltage, and flat band capacitance to the above parameters.

In a real situation, the following cases can be differentiated: (1) If no surface states are present but there is a non-zero work function difference between metal and silicon, there will be a parallel shift of the C-V curve without distortion along the voltage

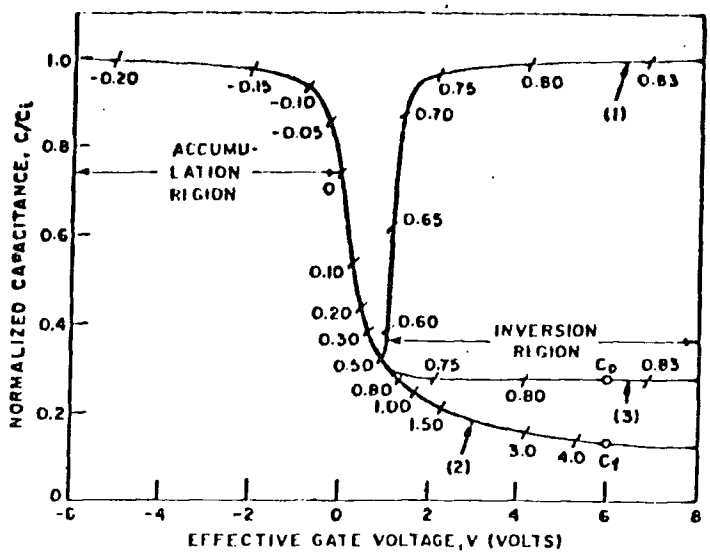


Figure 2.9 Normalised MIS capacitance vs Gate Voltage for the case of no surface states. The value of the silicon surface potential is shown for several values of capacitance. (34)

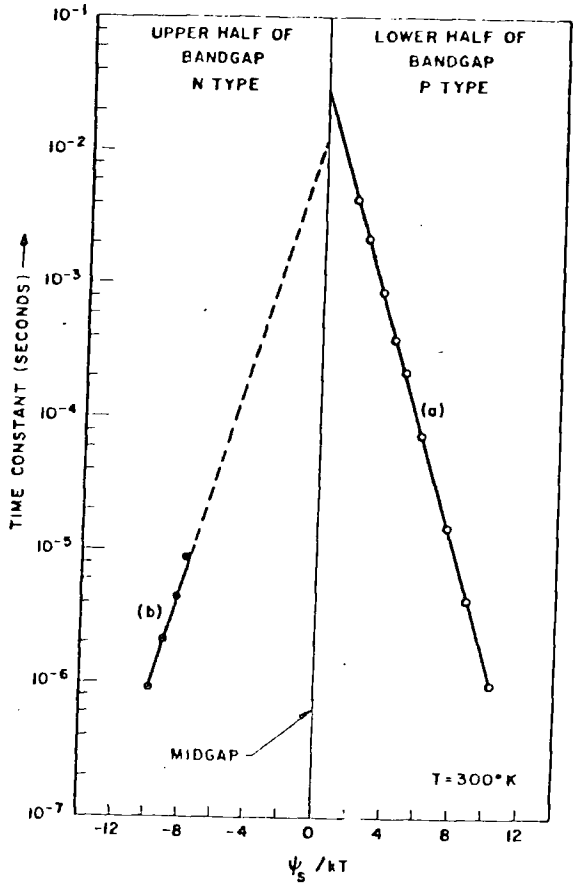


Figure 2.10 Variation of time constant with surface potential.

(ψ_s plotted with respect to midgap) (18)

axis by an amount equivalent to this difference.

(2) If surface states are present whose occupation is independent of applied bias, a similar simple lateral shift will occur which is a measure of the charge in the surface states. These states might correspond to the defects $:Si_{os}^{+}$ or C_3^{+} mentioned in section 2.3 that are either outside the band gap or too far into the oxide to respond.

(3) If surface states are present that do not follow the applied ac signal but whose occupancy depends on the dc bias (ie states that are within the silicon forbidden gap), the C-V curve will be displaced and distorted along the voltage axis, but the ratio of maximum to minimum capacitance will remain unchanged. This is the case for very high frequencies and forms the basis of the high frequency method of analysis as described in section 3.22. At lower frequencies the following situation prevails.

(4) If surface states are present that can follow the ac signal then they will displace and distort the C-V curve as well as change the ratio of minimum to maximum capacitance. Whether surface states can follow the applied signal depends on their inverse time constant as compared to the applied frequency. The variation of time constant through the band gap is given in figure 2.10 as a function of surface potential. It is important to note that the time constant is directly proportional to the surface potential: this will be used later.

2.43 Insulator Effects

The above assumes that an ideal insulator is present, but real insulators possess defects that introduce instability into the measured C-V curves. One type of instability is a hysteresis (19) in the measured response, ie the forward and reverse characteristics not overlaying one another. Particularly in early work with silicon dioxide, such hysteresis was caused by the presence of mobile sodium ions. A simple explanation of this phenomenon is that, as the applied bias is made more positive, positive sodium ions are repelled from the top contact to the semiconductor interface where they reside. Thus a larger negative bias is required to overcome their presence when the bias is reversed. If the insulator is a polarizable one, such as phosphosilicate glass, then a similar hysteresis direction will be observed; but since there is a large effective dipole layer within the insulator, the whole curve will be shifted laterally along the voltage axis.

Charge injection (21) into the insulator causes the opposite hysteresis direction. The initial bias now becomes important: a large value in accumulation causes injection from the metal whilst a large value in inversion causes injection from the semiconductor. If this biasing is done at elevated temperature, then large horizontal shifts in the measured C-V curves occur when the device is returned to room temperature. This is known as Bias Temperature Stressing and the results can be used to identify the nature of the particular instability (22).

We have also assumed that the carrier transport in the insulator is zero. However, real insulators do pass current, albeit small amounts, which can be characterized by various conduction mechanisms. Different ones exist depending on what factor dominates the current flow (18). In the case of Langmuir films, discussed in Chapter 7, the Poole-Frenkel mechanism has been found to be predominant where the current is given by

$$\ln J \propto \gamma_{PF} F^{1/2} / kT \qquad (2.15)$$

in which $\gamma_{PF} = 2(q^3/4\pi\varepsilon_i\varepsilon_o)^{1/2}$. The actual process corresponds to hopping of carriers between localized states or traps within the bulk of the insulator. The factor 2 depends on the charged state of these traps and disappears if the trap can be regarded as neutral. The mechanism then resembles the Schottky one, and distinction can only be made by further experiments investigating contact and thickness effects. If the insulator is thin, tunnelling can occur; this is considered later in this chapter.

2.5 The Conductance Approach

The surface state response to an ac signal is also characterized by a loss. This is a consequence of the complex nature of the silicon band structure: more energy is required to fill the interface states than to empty them, since electron promotion involves additional phonon interaction. Therefore each cycle of the signal requires energy to be contributed by the source, and so the diode appears to have a resistive element (conductance). This conductance combined

with the capacitance of the surface states produces a time constant effect which means that the ac current produced will lag behind the applied signal. Put another way, it can be said that the non-instantaneous nature of the charge exchange processes will cause the measured current to be out-of-phase with the applied signal. The following sections calculate the values of the capacitance and conductance of the surface states for various distributions, starting with a single level situation and finishing with the experimentally encountered continuous distribution. As previously mentioned, the surface states that respond to the signal most are those nearest the Fermi level. This is because the fluctuation of the degree of occupancy is greatest at this point.

2.51 Admittance of a single level state

Let us consider first the case of a single level of surface states in the semiconductor bandgap. Nicollian & Goetzberger (23) have shown through consideration of Shockley-Read-Hall statistics that the admittance can be given as

$$Y_s = j\omega^2 q N_s F_{to} (1-F_{to})/(kT(1+j\omega F_{to}/c_n n_{so})) \quad (2.16)$$

where

ω = period of applied ac signal (rad/s)

n_{so} = electron concentration at the surface with no ac voltage applied (cm^{-3})

F_{to} = value of the Fermi function at the trap energy E_t with no applied gate voltage

c_n = capture probability for electrons (cm^3/s), which equals $v_{th} \cdot \sigma_n$, where v_{th} is the thermal velocity of electrons and σ_n their capture cross section (cm^{-2})

N_s = number of states in E_t (cm^{-2})

Inspection of the function Y_s shows that it corresponds to a series admittance of resistance G_s^{-1} and capacitance C_s (figure 2.11) where

$$Y_s^{-1} = G_s^{-1} + 1/j\omega C_s$$

$$G_s^{-1} = kT/(q^2 N_s (1-F_{to}) c_n n_{so}) \qquad (2.17)$$

$$C_s = q^2 N_s F_{to} (1-F_{to})/kT$$

The time constant previously mentioned is defined as

$$\tau_s = G_s^{-1} C_s = F_{to}/c_n n_{so} \qquad (2.18)$$

Both C_s and G_s are independent of frequency of the applied gate voltage, since they depend only on E_F and E_t

It is found to be more convenient to express Y_s in terms of a parallel conductance G_p, and a parallel capacitance C_p (figure 2.11)

$$G_p/ = C_s \omega \tau_s / (1 + \omega^2 \tau_s^2)$$

$$C_p = C_s / (1 + \omega^2 \tau_s^2) \qquad (2.19)$$

Thus

$$Y_s = G_p + j\omega C_p \qquad (2.20)$$

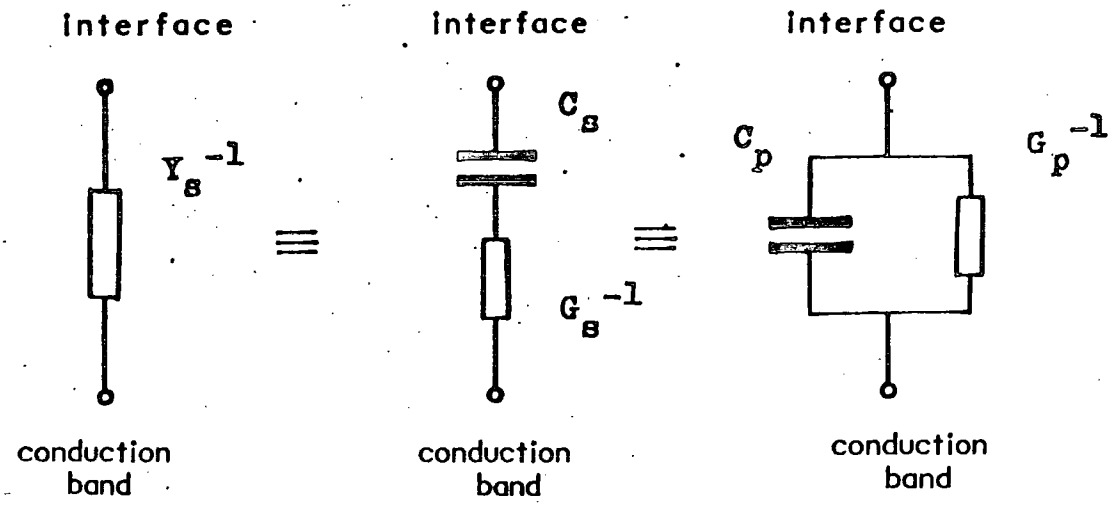


Figure 2.11 Surface state admittance in the single level model.

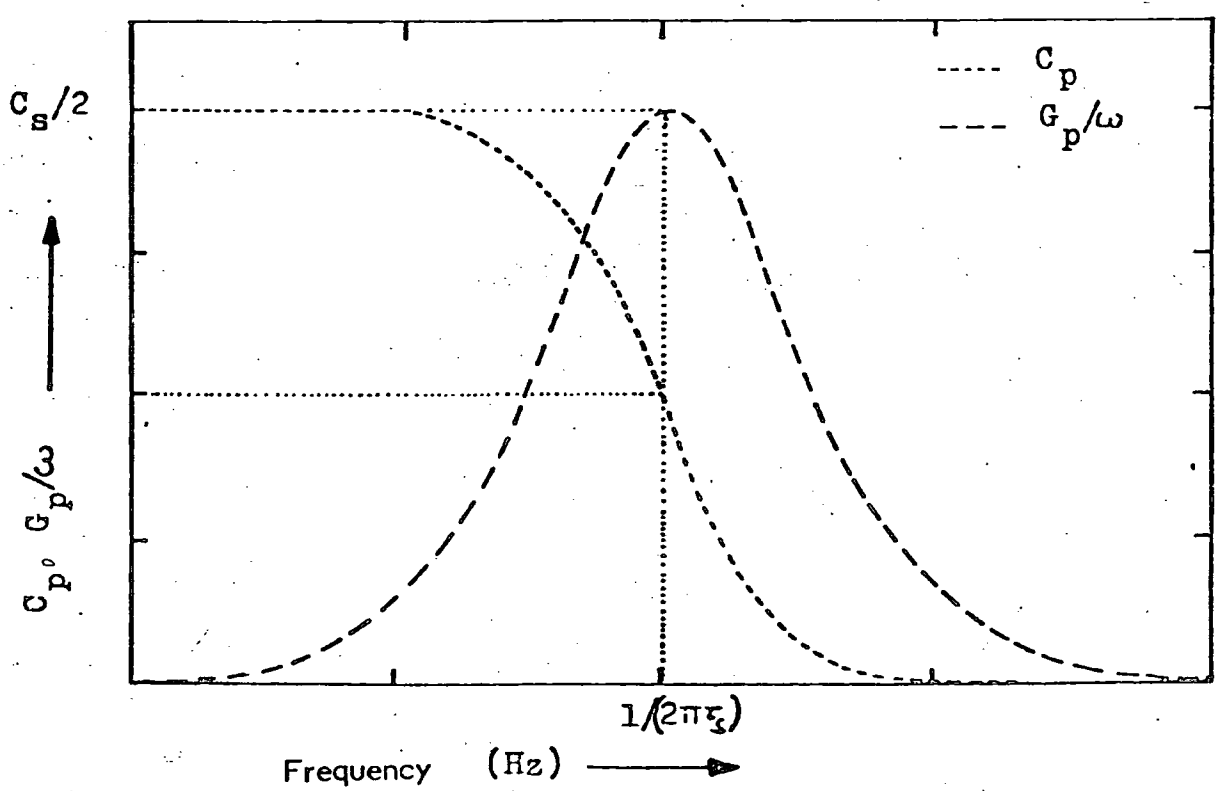


Figure 2.12 Parallel conductance and capacitance vs. frequency in the single level model.

As can be seen in figure 2.12, G_p/ω has a maximum as a function of frequency for $\omega\tau_s = 1$. The maximum of the G_p/ω versus the position of the Fermi level at the surface occurs for maximum C_s ie for $E_F = E_t$. Thus if a G_p/ω versus frequency plot is done at a bias such that the Fermi level is maintained at the trap level which gives $F_{to}(1-F_{to})=1/4$ then

$$G_p/\omega\ (max) = C_s/2 = q^2N_s/8kT \qquad (2.21)$$

Therefore it can be seen that the surface state density can be evaluated. Of course we can obtain C_s from a measurement of C_p, but in practice the extraction is difficult since a value of C_{sc} needs to be accurately known first, which can lead to error. This point will be returned to in the next chapter when various analysis methods are considered.

Unfortunately, experimental conductance curves do not display the single time constant character of the single level model (except in the inversion region which does not interest us): they are much broader. This is due to the fact that, as outlined in section 2.2, the surface state distribution in practical device is more complicated, being of a continuous nature rather than a single level. In order to account for this, Nicollian & Goetzberger (23) have extended their model, as outlined in the next section.

2.52 Admittance of a Continuum of Surface States

We can envisage a continuous distribution of surface states as a set of infinitely close single levels. In the electrical analogue, we can obtain the total admittance Y_{ss} by connecting all the single levels in parallel. Mathematically this is represented by integrating Y_s over all the trap energies in the gap:

$$Y_{ss} = \int_{E_v}^{E_c} Y_s(E_t)dE_t = \frac{j\omega q^2}{kT} \cdot \int_{E_v}^{E_c} \frac{N_{ss}F_{to}(1-F_{to})dE_t}{(1+j\omega F_{to}/c_n n_{so})} \qquad (2.22)$$

The integral when it is evaluated (23) gives

$$Y_{ss} = \frac{qN_{ss}}{2\tau_m} \ln(1+\omega^2\tau_m^2) + \frac{j\omega qN_{ss}}{\tau_m} \arctan(\omega\tau_m)$$

or $$Y_{ss} = G_p + j\omega C_p \qquad (2.23)$$

where

$$G_p/\omega = qN_{ss} \ln(1+\omega^2\tau_m^2)/2\omega\tau_m$$

$$C_p = qN_{ss} \arctan(\omega\tau_m)/\omega\tau_m \qquad (2.24)$$

with $\tau_m = 1/c_n n_{so}$

The expression for Y_{ss} is only correct if both N_{ss} and c_n are slowly varying functions of energy, because then we can treat them as constants in a limited area of energy. This is generally true for reasonable frequencies and systems.

The resulting G_p/ω versus frequency curves are wider than those for the single level case and the maximum now occurs for $\omega\tau_m = 1.98$. However, experimentally it is found that the parallel conductance curves with frequency are wider still and the maximum occurs at $\omega\tau_m = 2.5$ rather than $\omega\tau_m = 1.98$ (see figure 2.13).

2.53 The Surface Potential Fluctuation Model

Another factor is necessary to explain the discrepancy. If we assume that the built-in charges and charged interface states are randomly distributed in the plane of the interface, the electric field at the silicon surface will then fluctuate over the plane of the interface. Fluctuations in the electric field will cause corresponding fluctuations in the surface potential. There are several models (24) which take this into consideration and produce expressions for the parallel conductance of the device. Effectively, the previous expressions for parallel conductance and capacitance are integrated over the various surface potential values which means that the parallel conductance curves will have their maxima at different frequencies and will ensure that the resultant curve is broader. Unfortunately it is not possible to simplify the resulting expressions, and therefore the surface state information is found from a fitting of the theoretical curves to the experimental ones. This is accomplished accurately on a computer by adjusting the three variables c_n , N_{ss}, and σ_s which represents the variance of the surface potential. The starting values of these variables can be obtained from the experimental curves using those equations derived for the

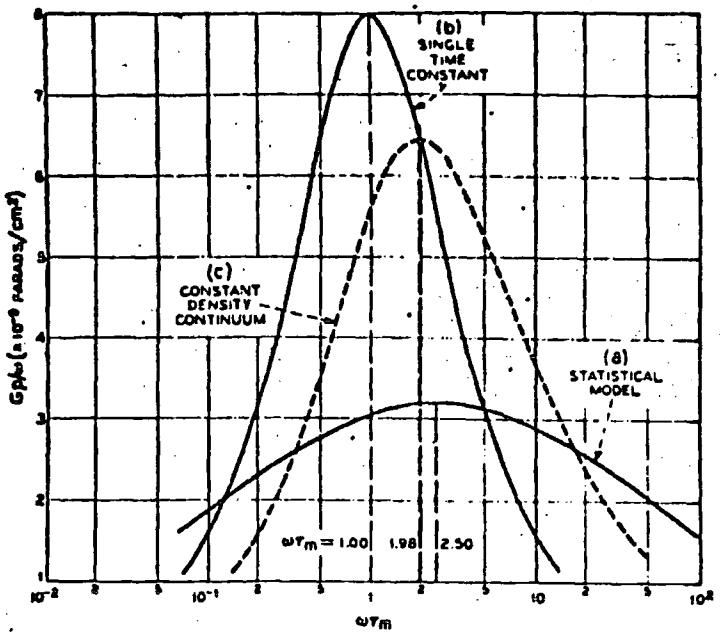


Figure 2.13 Calculated parallel conductance vs. $\log \omega\tau_m$ for the three different theoretical models. (33)

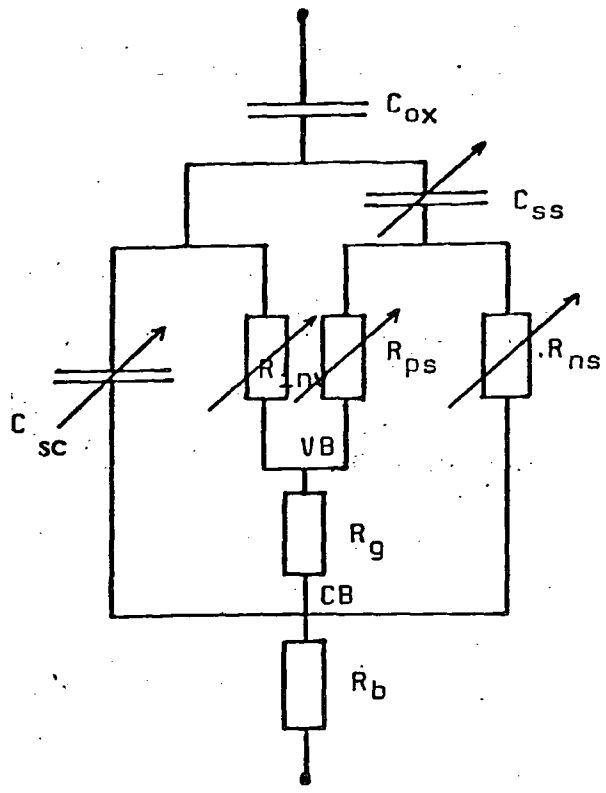


Figure 2.14 Lehovec & Slobodskoy Equivalent Circuit.

continuum model.

Alternative, more expedient, techniques that do not require computer curve fitting are outlined in the next chapter. The benefits gained by the faster analysis are offset by the requirement for an accurate determination of the experimental curve maximum. The height of this is proportional to the surface state density.

2.54 The Tunnelling Model

A different explanation for the experimental G_p/ω curve broadening was proposed by Preier (25) based on work by Heiman & Warfield (26). They assumed that the interface states were not located at the interface, but were distributed into the oxide from where they communicated with the conduction band by means of tunnelling. Preier proposed that a variable tunnelling parameter should be used to fit the theoretical curves to the data.

A modification by Warashina & Ushirokowa (27) requires only a single set of measured capacitance and conductance versus bias curves for analysis. They have derived expressions for the parallel conductance which can be used around the maximum in the voltage domain to get the value of N_{ss}. However, their expressions are complex and the results obtained for N_{ss} seem to be double-valued in certain parts of the bandgap.

The tunnelling model has not received wide acceptance because most workers (24,28) have been unable to fit their experimental data to it, and also most do not find the predicted low frequency asymmetry in the parallel conductance curve. Therefore most prefer the surface

potential fluctuation approach of Nicollian & Goetzberger (23).

2.6 More Complex Equivalent Circuits

We now have the concept of a simple admittance of two effective elements to represent the surface states. Its validity, though, is limited to the depletion region, as the initial equations only included the charge exchange processes of the majority carriers. At other potentials, the action of minority carriers may have to be considered. A full equivalent circuit describing all bias situations has been derived by Lehovec & Slobodskoy (29) by following step by step the flow of charge from the bulk of the semiconductor to the interface under an ac excitation. Each loss can be associated with a resistance, whereas charge storage can be associated with a capacitance (see figure 2.14). The positions of the valence and conduction band can be seen with associated resistances R_{ns} and R_{ps} which represent charge exchanges due to electrons and holes.

R_{inv} is a resistance representing the effects of the inversion layer and R_g is the bulk lifetime resistance. Using this model, a mathematical representation of the loss mechanisms of surface states outside the depletion region has been made (30): however, the matching of the representation to the experimental results is complicated and questionable. The analyses described in this thesis are restricted to the depletion region; even though this gives a limited range of surface potential, simplified analysis enables results to be obtained.

In the equivalent circuits so far, we have assumed that the insulator is thick and perfect; it has been shown (23) that for high accuracy the oxide must be as thin as possible. When it becomes very thin it reaches tunnelling dimensions when the carriers can pass through the insulator into either the conduction band or into the interface states themselves, depending on the insulator thickness. The latter also determines the additional components introduced into the equivalent circuit, which have been reviewed by Deneuville (31). It is possible to calculate the surface state density in spite of the added complication; for example, Kar & Dahlke (32) have obtained values for surface state density over the whole of the bandgap.

Finally, an additional complication when dealing with p-type samples is the interaction of the charge beneath the top contact with an external inversion layer that has been formed by positive charge within the insulator. The process is known as lateral ac current flow (33) and it introduces a second conductance peak into the admittance voltage characteristics. From an equivalent circuit point of view, a distributed resistance capacitance can be considered to have been introduced in parallel with the semiconductor capacitance.

2.7 Summary

In this chapter, the theoretical parameters used to describe the interface have been related to their physical origin and the electrical quantities used to measure them. This has been done by starting with a theoretical atomic perspective, developing through a

consideration of the role of charge exchange processes and finishing with an appreciation of the equivalent circuits involved. The approach has included a consideration of the effect of temperature, since its variation can be used to probe surface states close to the band edge. The same order will be preserved in the next chapter which contains a review of most of the current electrical methods that may be used to obtain surface state density information. The chapter begins with a consideration of capacitance techniques performed at room temperature and progresses through methods where temperature variation is important, finishing with the standard ac conductance method. Complications arise when temperature variation is used which, until the recent development of the DLTS technique, have meant a restricted range of measurement within the bandgap.

Chapter 3

Determination of Surface State Parameters from Measured Electrical Data

3.1 Introduction

The current electrical methods fall into two main groups: first, those which measure charge in (quasi) equilibrium with the electric field; and second, the ones based on the transient charging and discharging of surface states. The former category covers most capacitance methods and the latter group encompasses the charge pumping, transient capacitance and low temperature hysteresis methods. The choice of technique is determined not only by the information required, but also by the practical ease of obtaining that information ie the complexity of measurement including preparation and data analysis. Since MIS devices are easy to fabricate, we have concentrated upon techniques that utilize them: thus the charge pumping technique (1) and simpler I-V curve (2) measurement procedures which require the use of MOS transistor structures are precluded from this discussion. However, the data analysis is not as straightforward; the required information is obscured by the influence of competing factors which can introduce imaginary surface state density values. In order to recognise and compensate for this, more complicated measurement or analysis procedures are necessary, but the result is a limitation in the valid range of the following techniques. These are now considered in turn.

3.2 The Capacitance Techniques

The capacitance of an MIS device as a function of applied voltage may be determined under various conditions of frequency and temperature. The frequency of the ac measurement signal is important because different characteristics will be obtained, depending on whether or not the surface states are able to respond. At low frequencies, all the surface states are in equilibrium with the applied signal. However, as the frequency increases, less and less of the surface states are able to follow it and, at very high frequencies, none at all. The two methods outlined below are based at the frequency extremes.

3.21 High Frequency Method

Terman (3) suggested that even though surface states did not respond to a high frequency signal, they would still be manifest through the presence of their trapped charge, which would give rise to a lateral shift in the high frequency C-V curve as compared to an ideal theoretical one. This displacement corresponds to an additional voltage, V_{shift}, developed across the oxide depending on the amount of trapped charge, Q'_{ss}, that appears for various band bending conditions. The resultant lateral shift for several different surface state distributions are given in figure 3.1. At each energy position:

$$Q'_{ss} = C_{ox} \cdot V_{shift} \qquad (3.1)$$

Since Q'_{ss} represents the sum of the charge (integral) in the states, a graphical differentiation of Q'_{ss} versus surface potential is required to find N_{ss} as a function of energy:

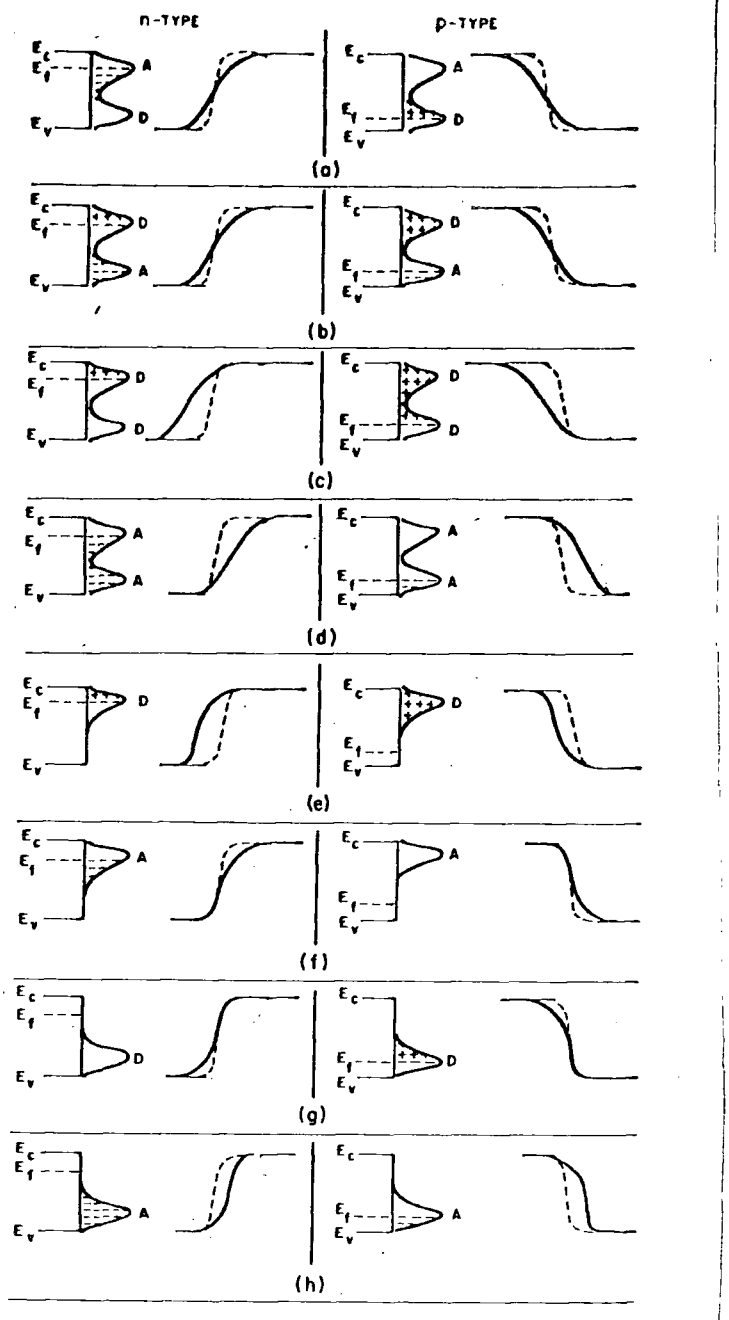


Figure 3.1 High frequency capacitance-voltage characteristics with (continuous line) and without (dashed line) interface state distributions shown. States labelled A are acceptors and states labelled D are donors.

$$N_{ss} = \frac{1}{q} \frac{dQ'_{ss}}{d\Psi_s} \qquad (eV^{-1}\ cm^{-2}) \qquad (3.2)$$

Zaininger & Warfield (4) demonstrated that the method was particularly sensitive to inaccuracies in the determined values of C_{ox} and the doping density used in the calculation of the ideal curve. These could give rise to effective surface state densities that do not really exist. Sah and co-workers (5) put forward improved formulae and curve fitting techniques for deriving these quantities thus overcoming the above problems. However, they did not take into account the effect of surface potential fluctuations which can also introduce spurious surface state densities (6,7). Finally, the measurement signal has to be very large to ensure that all the surface states do not respond; the standard frequency of 1MHz is inadequate for states near the band edges, where the reciprocal time constant is of this value, as figure 2.10 illustrates.

3.22 Low Frequency Method

At low frequencies, where the period of the measurement signal is long compared to the time constants of the surface states, there is a contribution from these states to the total capacitance. This means that simple equations, rather than graphical differentiation, can be used to determine the surface state density. Furthermore, the surface potential is easily found by integration of the experimental curve; in Terman's technique, it is found by comparison with the theoretical

one. Berglund's (8) original technique is perfected in the quasistatic approach of Kuhn (9) where the low frequency becomes equivalent to zero with a dc voltage ramp. The displacement current produced is directly proportional to the low frequency capacitance:

$$i = \frac{dQ}{dt} = \frac{dQ}{dV} \cdot \frac{dV}{dt} = C_{lf}(V) \cdot \frac{dV}{dt} \qquad (3.3)$$

Now recalling the simple representation for the MIS device capacitance (see equation 2.5):

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{sc} + C_{ss}} \qquad (3.4)$$

It can be seen by rearrangement and assuming that $C_{ss} = q.N_{ss}.A$

$$N_{ss}.q.A = \left(\frac{C_{lf}}{1 - C_{lf}/C_{ox}} - C_{sc} \right) \qquad (3.5)$$

C_{sc} can be theoretically calculated or derived experimentally from a high frequency curve. The latter is done by assuming that C_{ss} is zero in equation 3.4, thus equation 3.5 can be written as:

$$N_{ss}.q.A = \left(\frac{C_{lf}.C_{ox}}{C_{ox} - C_{lf}} - \frac{C_{hf}.C_{ox}}{C_{ox} - C_{hf}} \right) \qquad (3.6)$$

Since it is not necessary to compute a theoretical curve, this equation is far easier to use. However, whereas equation 3.5 is applicable to the whole of the bandgap, equation 3.6 has a limited range depending on the measurement frequency such that C_{ss} is zero.

The interval extends from the inversion threshold to a value of the surface potential where the surface state time constant has just become equal to the ac signal period. For an ac frequency of 500 kHz this point is 250mV from the majority carrier band edge.

Again, as with Terman's method, if surface potential fluctuations are present, the theoretically calculated value for C_{sc} will be incorrect and give rise to an apparent N_{ss} (10). It is better to compare the high and low frequency curves, using equation 3.6, since the effects of the fluctuations will be approximately the same and counteracting. The error is expected to be small for large surface state densities, small surface potential fluctuations and for energy values near midgap resulting in an accuracy in N_{ss} values of about 10^{10} cm^{-2} eV^{-1}.

The relation between surface potential and applied bias is obtained using the expression below

$$\Psi s = \int_{V_{acc}}^{V} (1 - C_{lf}/C_{ox}) \, dV + @ \qquad (3.7)$$

The integration is done either numerically on a computer or direct from the equipment using electronic modules (11). The additive constant, @, may be determined in various ways; normally it is from the horizontal intercept of the inverse capacitance squared versus applied potential curve. Another technique

was suggested by Lopez (12); it calculates the total surface potential and compares it to the theoretical value of 1.1eV. The additive constant is simply the difference between the two.

3.23 Quasistatic Measurement Configuration

The basic circuit for performing quasistatic MIS C-V measurements is given in figure 3.2. It is essentially an analog differentiator incorporating the MIS device as the capacitive element. The amplifier ideally maintains point N of the circuit at ground potential so that the output voltage can be written as

$$Vo(t) = - RC(t)\ dV(t)/dt \qquad (3.8)$$

Therefore when V(t) is a ramp of the form $V(t) = \overset{+}{-} at$, the output voltage is directly proportional to the differential capacitance,

$$Vo(t) = \overset{-}{+} aRC(t) \qquad (3.9)$$

An example of a resultant plot is shown in figure 3.3; by superimposing a high frequency curve as in figure 3.4, the surface state density of the system can be calculated using equation 3.6.

3.3 Temperature Techniques

Alternatively, variation of the sample temperature can be used as a basis for obtaining surface state density information. The simplest technique (13) is related to Terman's method, where the high frequency capacitance curve is used to monitor the charge occupancy of the surface states. Instead of altering the bias, it is held constant and temperature change is used to sweep the Fermi level. Then, using expressions very similar to Terman's, surface state densities in a range from 0.2eV to 0.05eV near the majority carrier band can be obtained when the device is cooled to liquid nitrogen temperature.

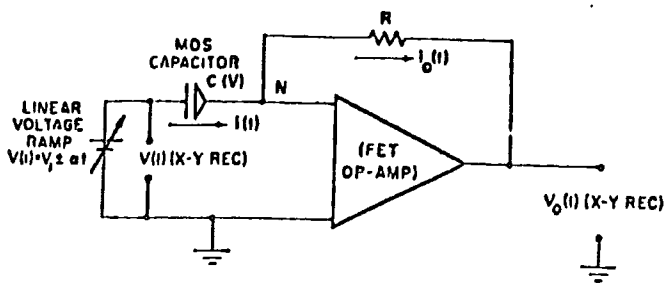


Figure 3.2 Basic circuit required for quasi-static MOS C-V method.

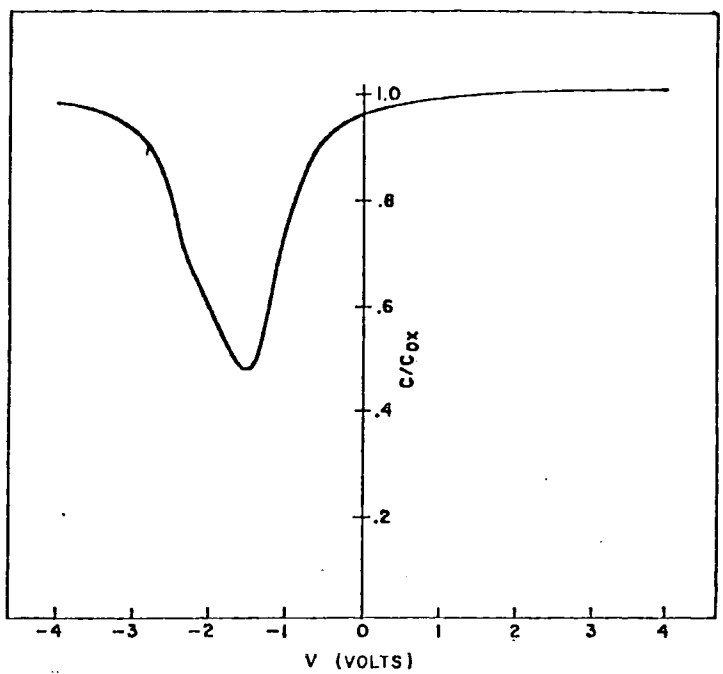


Figure 3.3 MOS C-V curve obtained with the quasi-static technique for an n-type silicon MOS capacitor. (9)

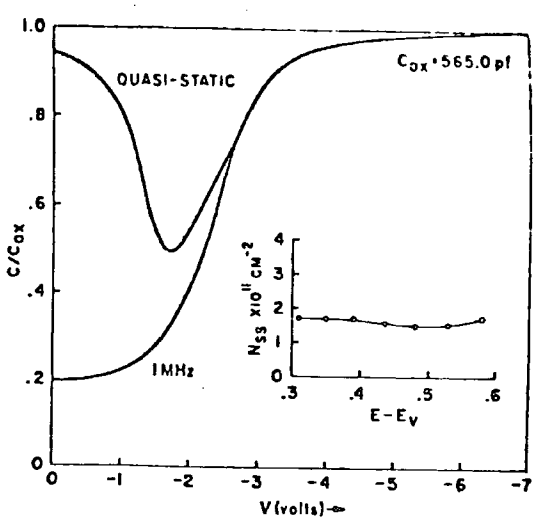


Figure 3.4 Combined low and high frequency curves and corresponding surface state density.

The technique has drawbacks though: it is difficult to interpret the results over small temperature changes, and the method also produces anomalous peaks in N_{ss} close to the band edges that do not agree with the latest data. Recent computation (14) has shown that these may be due to the combined effect of an inadequately low measurement frequency and a decreasing capture cross section value nearer to the band edge.

3.31 Low Temperature Hysteresis Method

This technique only gives N_{ss} values averaged over a large portion of the band gap rather than with respect to energy (15). It relies on the difference in capture and emission times of carriers reacting with the surface states at liquid nitrogen temperature which causes a hysteresis in the high frequency C-V curves. This can be explained by considering a voltage cycle. Starting in accumulation, with only majority carriers filling the surface states, it is only after the device has reached inversion, where there is a high concentration of minority carriers, that the occupancy will alter. On going from inversion to accumulation, the states then remain filled with minority carriers. The difference, dV, in the two curves corresponds to the charge contained by the surface states.

$$Q'_{ss} = C_{ox}.dV \qquad (3.10)$$

and

$$N_{ss} = Q'_{ss}/q.A \qquad (cm^{-2}) \qquad (3.11)$$

3.32 The Transient Capacitance Method

By actually measuring the emission processes, whilst scanning the temperature at the same time, far more information can be obtained. In the normal transient spectroscopy technique, an MIS capacitor is pulsed into accumulation and the resulting high frequency capacitance transient measured as the temperature is increased. The transient is a result of the return to equilibrium of the electron population in the depletion region which has been disturbed by majority carriers introduced by the applied voltage. The overall decay is monitored in the DLTS technique (16) through the use of a "rate window", which produces a peak in the output when the decay rate passes through a predetermined value. When the temperature is altered, the thermal emission rate and hence the capacitance decay rate change. This gives rise to such a peak, which can be used to calculate the surface state density. However, the equipment can be complicated (17), especially if it is to measure the smallest surface state emission times. The analysis, too, is not simple and there is even some doubt as to the validity of some interpretations(18).

We have not used temperature techniques because of the additional variable that would be introduced when considering gaseous interactions which could well be temperature dependent. We have concentrated upon the conductance technique, which is the standard, although a little time consuming. With the aid of a microcomputer, we have been able to cut down the effort involved in extracting the required information. Moreover, we have developed a novel technique that enables fast surface state determination; this is described in Chapter 5.

3.4 The Conductance Technique

More information on interface states can be obtained if the loss mechanisms in the system are considered and a full frequency response is measured. This involves determining the small signal admittance of the MIS device resolved as a capacitance and conductance and extracting the parallel conductance using algebraic manipulation. The parallel conductance is then examined using the theory in section 2.5 and the surface state information calculated.

3.41 Equivalent Circuits

The measured capacitance and conductance (see figure 3.5a) have to be related to the parallel conductance of the surface states through the use of equivalent circuits. This is because the total admittance of an MIS capacitor consists of several components whose effect has to be compensated for. A circuit model of the device is shown inset in figure 3.5b with a typical corresponding set of measured characteristics. The semiconductor capacitance in parallel with G_p represents the combination of the surface state and depletion layer capacitance; the increased contribution of the former produces the rise in C_p as the frequency decreases. The circuit elements C_{ox} and R_s are associated with the geometrical capacitance of the oxide and the bulk resistance of the substrate, respectively. Their values can be calculated from the measured values of C_m and G_m in strong accumulation:

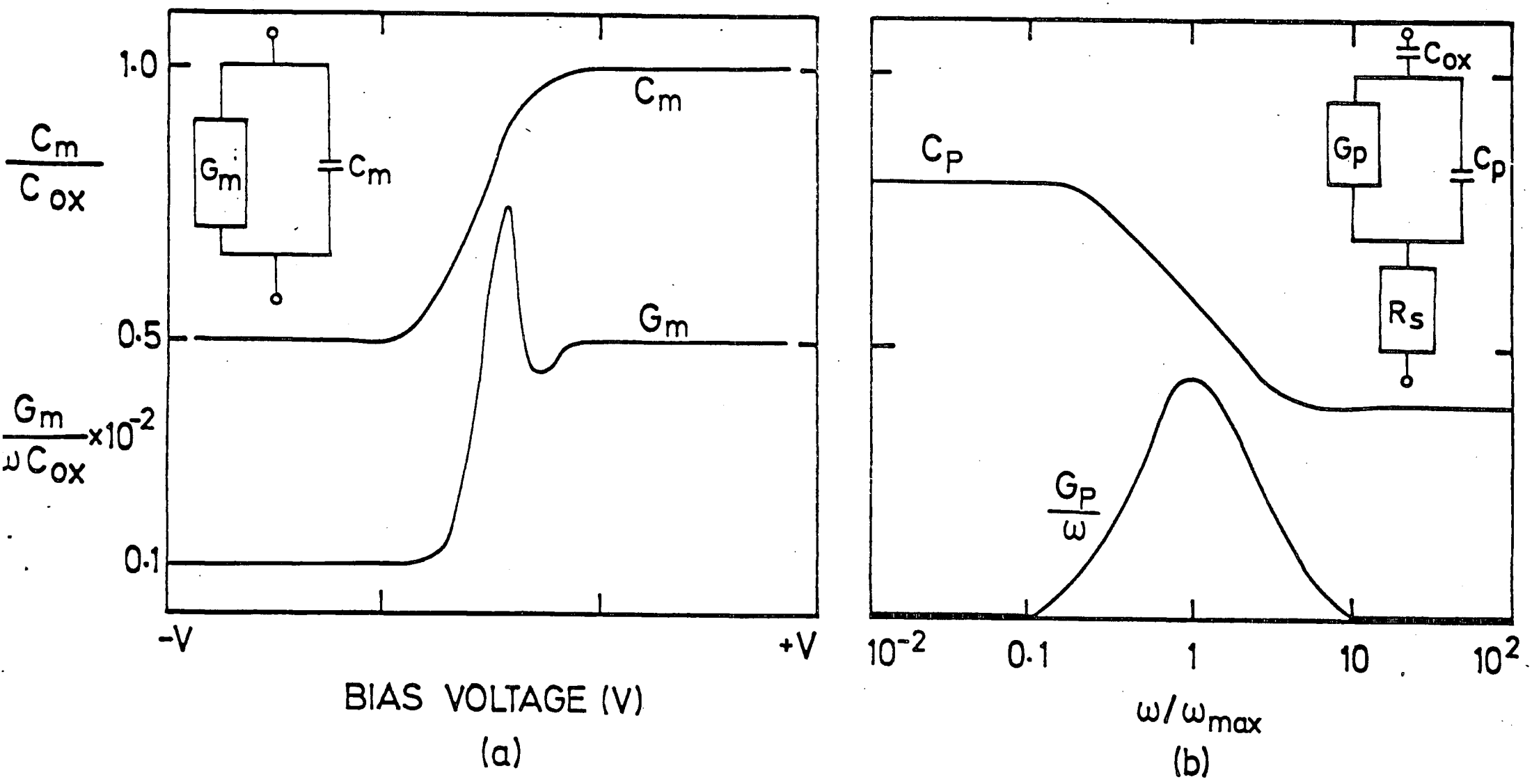


Figure 3.5 Admittance Characteristics for MIS structure, and corresponding equivalent circuits.

$$R_s = G_m/(G_m^2 + \omega^2 C_m^2) \qquad (3.12)$$

$$C_{ox} = C_m(1 + (G_m^2/\omega^2 C_m^2))$$

The terms defined by these equations are bias and frequency independent for ideal devices, but in a practical situation the insulator may, for example, have a frequency dependent permittivity. Therefore, compensation is required at each frequency. The fact that such compensation is necessary is not commonly recognised.

The interface state contribution is contained entirely in the terms C_p and G_p, which are bias and frequency dependent. These terms are extracted from the measured values using the equations below (A is the top contact area).

$$A.G_p = \frac{\omega^2 C_{ox}^2 (G_m - \omega^2 C_m^2 - R_s - R_s C_m^2)}{(\omega^2 C_{ox} R_s C_m - G_m)^2 + \omega^2 (C_{ox} - C_m - C_{ox} R_s G_m)^2}$$

$$A.C_p = \frac{\omega^2 C_{ox} C_m (C_{ox} - C_m) - C_{ox} G_m^2}{(\omega^2 C_{ox} R_s C_m - G_m)^2 + \omega^2 (C_{ox} - C_m - C_{ox} R_s G_m)^2}$$

(3.13)

As can be seen, C_p contains the same information, but to obtain N_{ss}, a theoretical value for C_{sc} would have to be assumed, leading to the same problems as suffered by the capacitance techniques previously described. It is better to use the parallel conductance to determine N_{ss} as this is directly related (see section 2.5). However, a fact not generally appreciated is that it is possible to use C_p in the depletion region to obtain a value for the surface

potential thus obviating the need to perform the integration normally carried out (equation 3.7). This is explained further in section 5.4.

If highly-doped epitaxial samples are used then R_s can be assumed equal to zero and

$$A.G_p = \omega^2 C_{ox}^2 G_m / (G_m^2 + (C_{ox} - C_m)^2) \qquad (3.14)$$

In the conventional realisation of the conductance technique, frequency response curves are not directly measured as the equipment has to be calibrated at every frequency due to the effects introduced by stray capacitances. Instead, capacitance and conductance characteristics are measured with respect to bias at several frequencies; the parallel conductance is then extracted, compensating for C_{ox} and R_s, and replotted in the frequency domain to give the peaks ready for analysis.

3.42 Surface State Evaluation

In order to obtain N_{ss} values from parallel conductance versus frequency curves, it is not necessary to go to complicated computer curve fitting procedures. Two graphical techniques have been proposed that enable desktop evaluation of N_{ss} to be performed. The first, suggested by Goetzberger et al (19), involves comparing the shape of the experimentally determined curves with standard $G_p/\omega C_{ox}$ curves that have been plotted in a normalized fashion. The shape of the latter (see figure 3.6) depends only on the variance σ_g so, by comparison, the value of the variance for the experimental curves can

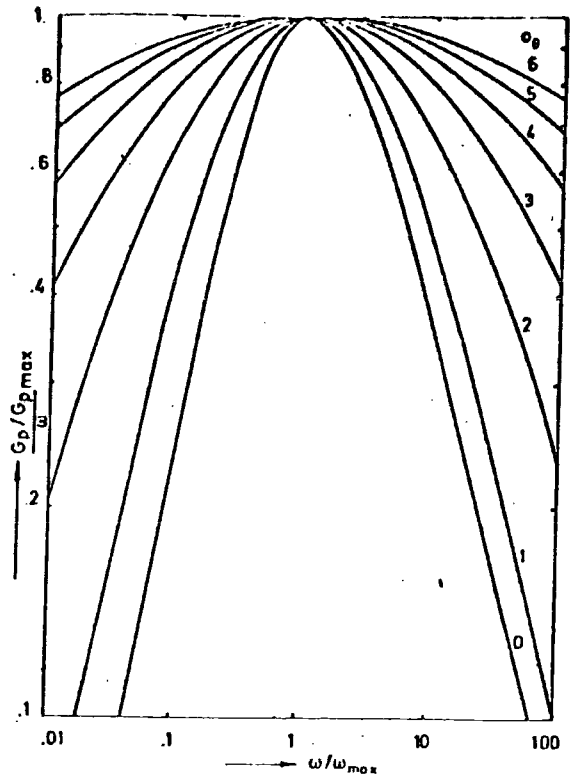


Figure 3.6 Normalized parallel conductance plots plotted with respect to the variance σ_g of the surface potential

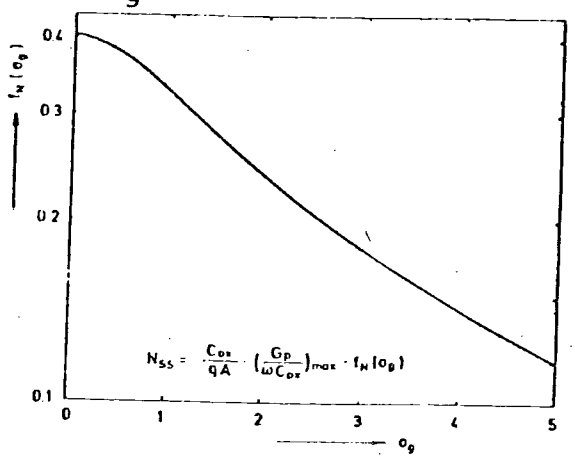


Figure 3.7 A plot of the function $f_N(\sigma_g)$ versus variance of the surface potential.

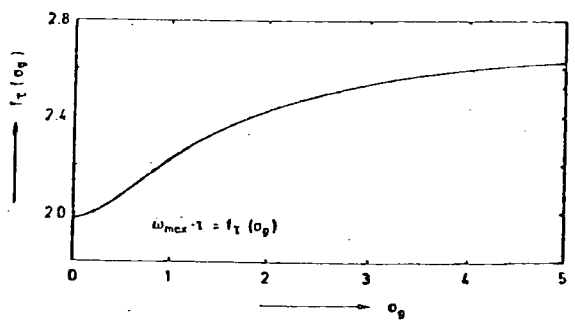


Figure 3.8 The general function $f_\tau(\sigma_g)$ plotted with respect to the variance of the surface potential.

be found. The surface state density and the relaxation time are then obtained from the following:

$$N_{ss} = (1/qA).G_p/\omega_{max} \cdot f_N(\sigma_g)$$

$$\tau = 1/\omega_{max} \cdot f_\tau (\sigma_g) \qquad (3.15)$$

The functions f_N and f_τ are given in figures 3.7 and 3.8. They are dependent only on $_g$. The capture cross section can be determined from if the surface potential is known, using equation 3.16 (v_{th} is the thermal velocity taken as 10^7 cms^{-1}).

$$_n = (v_{th} \cdot \tau \cdot n_{bulk} exp(q\Psi s/kT))^{-1} \qquad (3.16)$$

The surface state density is seen to be determined by the peak height and a variable dependent on the curve width. From inspection of figure 3.6, it can be realised that curve fitting is not absolutely necessary; for, sitting at any particular frequency, there is only one possible value of $G_p/\omega/(G_p/\omega_{max})$ for any particular variance. Thus it can be seen that only two values of the G_p/ω curve are necessary This is the essence of the Simonne technique (20) which goes one step further and combines the curves given in figures 3.6 & 3.7 into one. Practically, an approximate G_p/ω versus ω curve is first plotted; then, by taking additional data points, the peak position is precisely located. Next, the ratio of the peak parallel conductance compared to the value of G_p/ω at a frequency a factor of five different is determined and, from the curve reproduced from (17), N_{ss} is simply found. This is by far the simplest evaluation method, but it does have its drawbacks which are discussed more in Chapter 5 where they are used to justify the development of our novel technique.

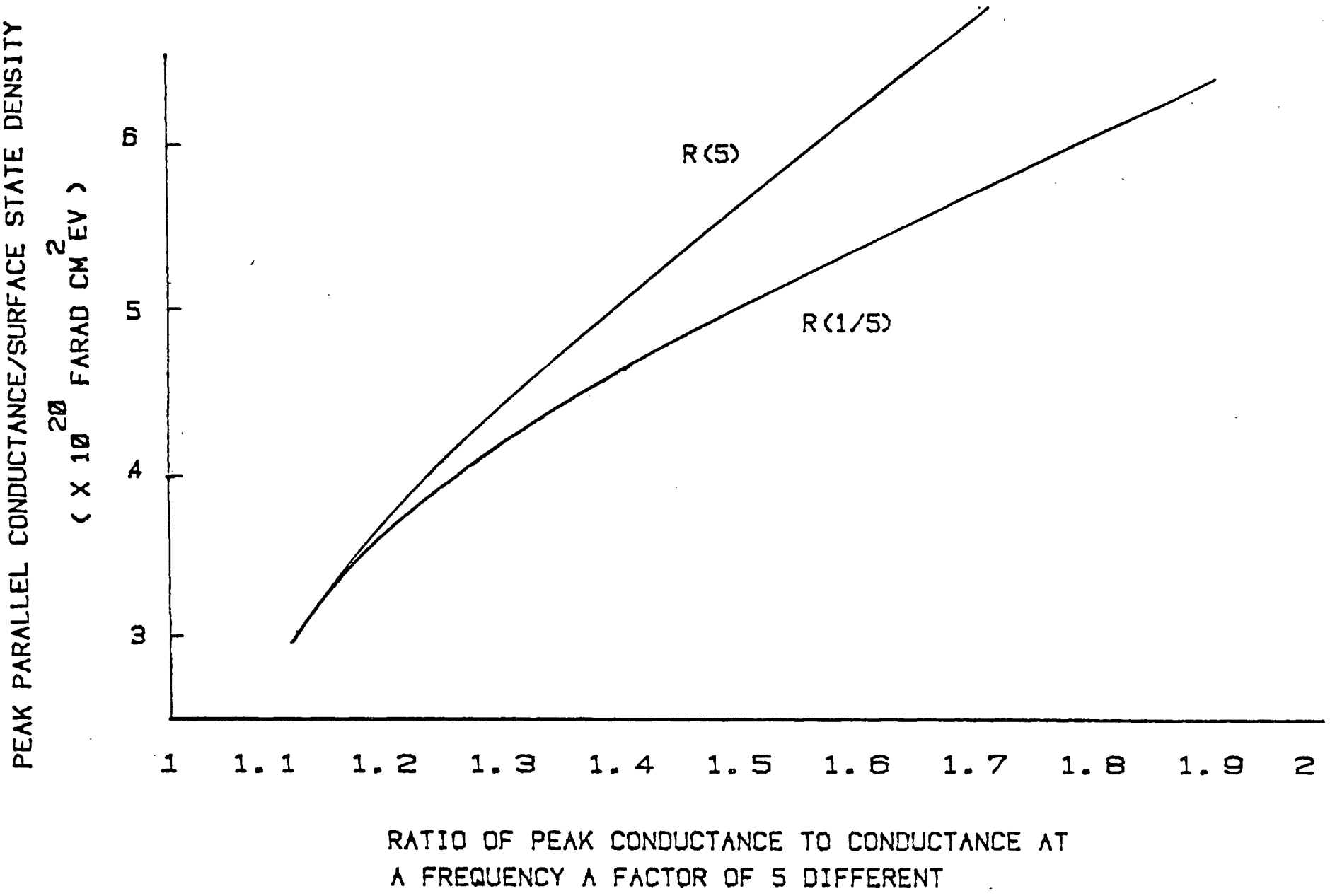


Figure 3.9 Simonne curve for surface state density extraction.

3.5 Summary

This chapter has progressed from simple capacitance techniques that are highly susceptible to error to the more accurate, but also more complicated, transient capacitance and conductance methods, where the response times of the states are measured. There are a few other techniques, such as the static (21) and photovoltage (22), but these are not widespread in use and hence were excluded from this study. A brief outline of the accuracies and valid range of the above is now given:

Method	Accuracy	Range
1) Terman's Hf C-V	5×10^{10} eV^{-1} cm^{-2}	$E_i \pm 0.3eV$
2) Quasistatic C-V	1×10^{10} eV^{-1} cm^{-2}	$E_i \pm 0.3eV$
3) Hf Temperature	1×10^{11} eV^{-1} cm^{-2}	$E_i - (E_{maj} - 0.15)$ eV
4) Low Temp. C-V	$5 \times 10^{10} eV^{-1}$ cm^{-2}	$E_i \pm 0.4eV$
5) Transient Cap	2×10^{9} eV^{-1} cm^{-2}	0.9eV
6) Conductance	10^{9} eV^{-1} cm^{-2}	$E_i - (E_{maj} - 0.1)$ eV

Chapter 4

Experimental Details

4.1 Introduction

A complete characterization of the semiconductor surface would require many different types of technique which would obviously be experimentally complex to attempt simultaneously. This work has concentrated on electrical measurements of MIS structures with a view to obtaining information on the surface state distribution. The experimental arrangements for the quasi-static and admittance techniques are described below. The microcomputer which has been added to the standard admittance measurement equipment and used to develop our novel technique is also described. In addition, this chapter contains details of sample preparation. The description of the Langmuir film deposition technique and equipment, however, is left until Chapter 7.

4.2 The Quasi-static Technique

4.21 Use of Equipment

The experimental set-up for this technique is shown in figure 4.1, corresponding to the functional layout given in figure 3.2. The MIS device was driven with a high linearity (1%) low noise ramp voltage generator whose internal circuit was based on a standard OP-AMP integrator. This unit was constructed within the University and possessed presettable start and finish points over a 200 V range, and variable sweep rate down to as low as 5 mV/s. It was connected to the shielded light-tight cryostat which held the sample through stiff cables. A gold wire probe which was ball-shaped at the end to avoid damaging the top electrode completed the contact. The current

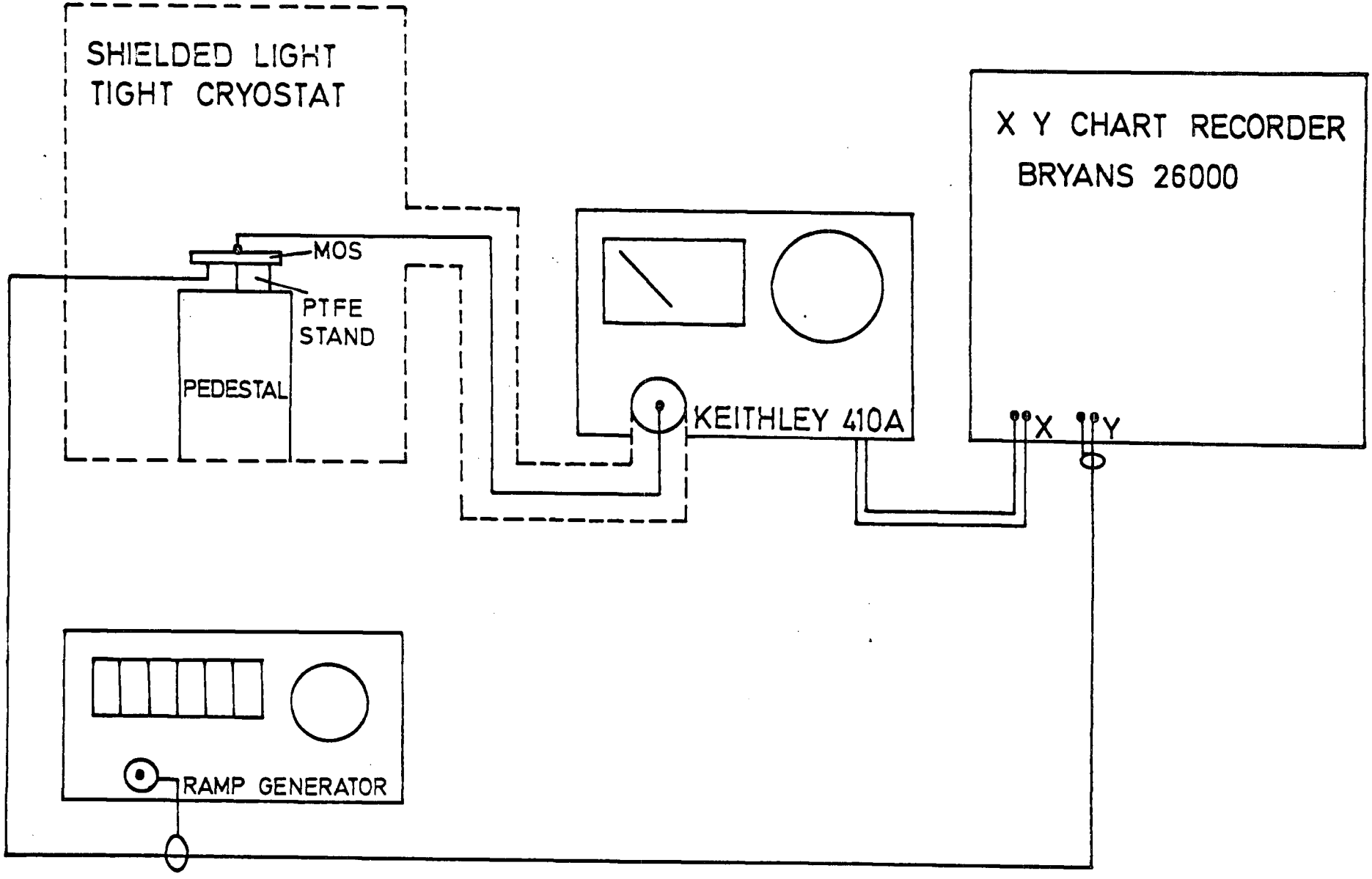


Figure 4.1 Experimental configuration for quasi-static method.

produced was monitored with a Keithley 410A picoammeter that acted as the current to voltage converter. Its output voltage, which is directly proportional to the low frequency capacitance of the device, was then displayed on a Bryans 26000 chart recorder. This not only provided additional gain to the system, but also a source of response time type distortion if any filter, eg a capacitor, was used at the input to remove noise. Such distortion is a crucial consideration in such time domain measurements since it can introduce error. The picoammeter rise time on its low ranges is 0.25s; thus, a capacitor with a value less than 0.25mF had to be used (the input impedance of the chart recorder being 1 megohm). These sources of time constant dispersion lead to a limiting of the ramp rate if distortion of the resultant curve is not to occur.

In practice, though, the requirement that the sample be in thermal equilibrium is more important: this limits the ramp rate to less than 50 mV/s. Thermal equilibrium can be seen to exist by sweeping the curve in both directions. Ideally, the two curves obtained above and below the zero line should be mirror images of each other, as shown in figure 4.2. The zero line does not represent zero capacitance because of a current contribution from the stray capacitances present in the circuit. These have to be compensated for and are evaluated by performing a second scan with the sample disconnected. Any slope in the resultant curve indicates leakage, possibly through the input connections. The cryostat used had well-insulated independent entry points to prevent such a problem. If the low frequency capacitance curve slopes, then this means that the device itself posesses a non-ideal insulator which is unsuitable for the following analysis.

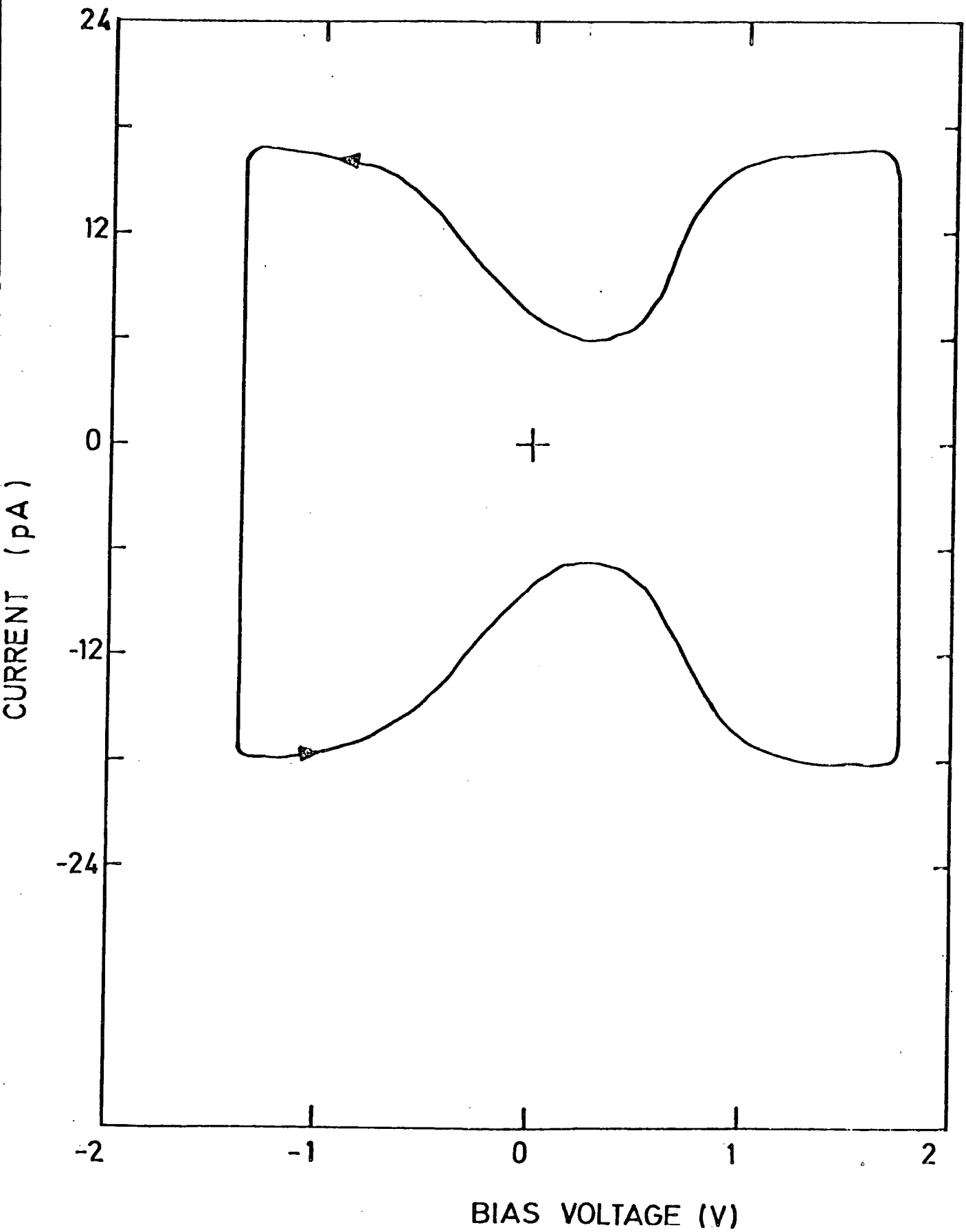


Figure 4.2 Experimental quasi-static C-V curves showing presence of thermal equilibrium.

Before the curve can be used to determine surface state density values, it has to be calibrated in terms of capacitance. This was accomplished in two ways:

(1) Comparison with the resulting structureless curve obtained by ramping with the device substituted by a standard polystyrene capacitor.

(2) Use of the high frequency capacitance curve: this requires initial matching of the two zero positions followed by a superposition of the measured characteristics in the accumulation region. C_{lf} is thus given by

$$C_{lf} = C_{ox} \text{ (Height of } C_{lf})/(\text{Height of } C_{ox}) \qquad (4.1)$$

This procedure is made easier by using the normalised version of equation 3.6 below.

$$N_{ss} = \frac{C_{ox}}{q.A} \left(\frac{C_{lf}/C_{ox}}{1 - C_{lf}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1 - C_{hf}/C_{ox}} \right) \qquad (4.2)$$

It is best to use the first method initially to ensure that the insulator capacitance is not frequency-dependent which could indicate the presence of a non-Ohmic back contact.

4.22 Experimental Difficulties

(a) The output current from the MOS device is extremely small (picoampere range) and, therefore, the technique suffers from the usual noise problems brought about by vibration and poor screening. One example of the former was the periodic hum of the the chart

recorder, caused by an internal fan, which meant that it was necessary to mount it away from the main equipment on a separate bench. The latter meant that the entry points to the cryostat had to be carefully screened and earth loops avoided.

(b) Under such low current conditions, leakage currents became obvious. In the case of the organic multilayers used, these currents gave rise to an intolerable slope in the measured characteristic making surface state determination impossible.

(c) Drift, ie vertical shift of the experimental curves, also occurred under certain experimental conditions such as gas exposure, possibly caused by the presence of water vapour.

4.3 The Admittance Measurement System

The MIS devices were mainly analysed through measurement of their small signal admittance which was done using a traditional phase sensitive detector system (1). In order to reduce the effort involved in collecting and analysing the data, a microcomputer was added to the equipment. The associated hardware and software are described after a consideration of the input circuit to the lock-in-amplifier and the calibration procedure utilized.

A Brookdeal Ortholoc, Model 9502, lock-in-amplifier was the phase sensitive detector used. It measures the magnitude and phase of an ac signal produced by a sample that has been excited by an ac source, and resolves them into the in-phase and out-of-phase component with respect to the applied signal. These can be seen to be proportional to the capacitance and conductance of the sample by a simple consideration of the circuit elements involved.

4.31 Input Circuit

For the purposes of measurement, the sample admittance may be represented as the parallel combination of a capacitance C_m and a conductance G_m thus (see figure 3.5)

$$Y_m = G_m + j\omega C_m \tag{4.3}$$

If the sample is driven with a sinusoidal voltage v_i a current i_m is generated (see figure 4.3a) which from elementary theory is given by

$$i_m = v_i \cdot Y_m \tag{4.4}$$

Therefore from equation 4.3

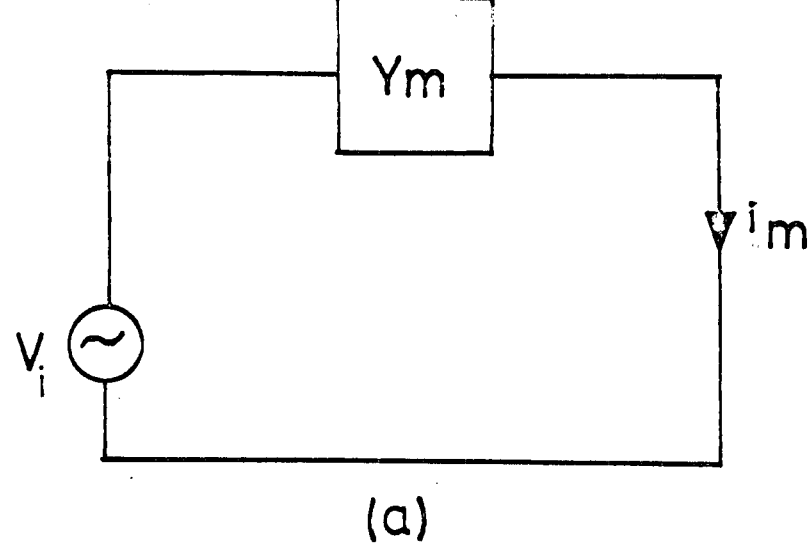
$$G_m = Re(i_m)/v_i \quad \& \omega C_m = Im(i_m)/v_i \tag{4.5}$$

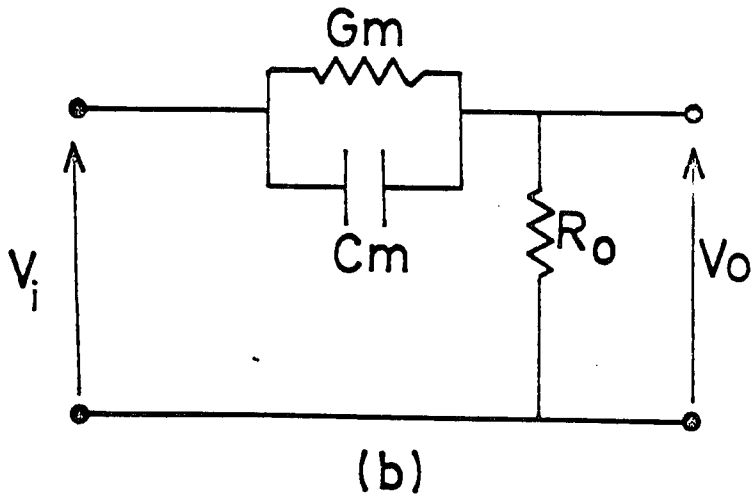
where the real and imaginary parts of i_m can be considered as the in-phase and out-of-phase components of the signal.

Commonly a sense admittance is used to determine i_m and the voltage developed across this is measured with a voltage sensitive detector. If the input impedance of the latter and that of the interconnecting cables are neglected, it can be seen how a simple sensing resistor (see figure 4.3b) or capacitor (see figure 4.3c) complicates the above analysis.

The output voltage across the sense resistor, using the principle of voltage division, is:

$$v_o = v_i R_o (G_m + j\omega C_m)/(1 + R_o G_m + j R_o \omega C_m) \tag{4.6}$$





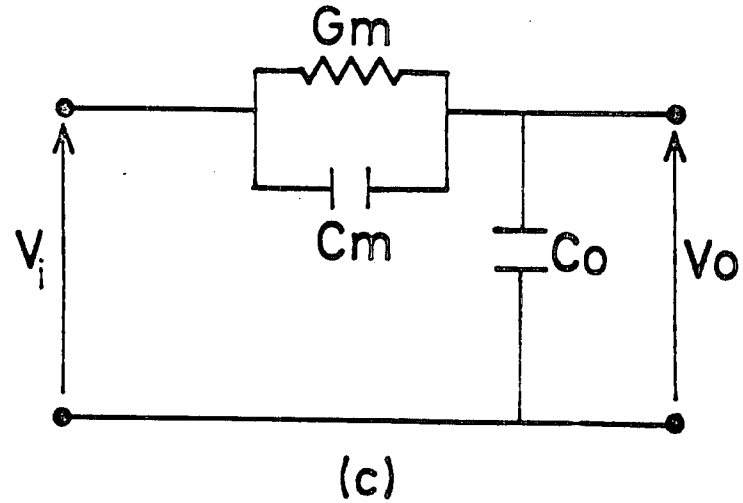


Figure 4.3 Various lock-in-amplifier input circuits. (a) Schematic, (b) Resistive and (c) Capacitive.

Supposing $R_o G_m < 1$, $(R_o \omega C_m)^2 < 1$, $R_o (C_m)^2 < G_m$ ie the impedance of the sample is much greater than that of the sense resistor, then:

$$v_o = v_i R_o (G_m + j\omega C_m) \qquad (4.7)$$

which is as required. If a capacitor is used as the sense element the output voltage is now:

$$v_o = v_i (C_m / C_o - jG_m / \omega C_o)/(1 + C_m / C_o + G_m / j\omega C_o) \qquad (4.8)$$

Similarly if $C_m / C_o < 1$, $(G_m / \omega C_o)^2 < 1$, $(G_m / \omega)^2 / C_o < C_m$ then the above reduces to:

$$v_o = v_i (C_m - jG_m / \omega) / C_o \qquad (4.9)$$

The advantage of using a capacitor as the sense admittance is that the output is frequency-independent.

In both cases, the set of conditions necessary so that the sense element does not disturb the voltage dropped across sample creates operational frequency limits. For a typical set of possible measurement values $30pF < C_m < 500pF$, $G_m < 10uS$, $G_m / \omega < 1pF$, it is found that the circuit shown in figure 4.3b can only be utilised when R_o=10 ohm at frequencies less than 1 kHz and C_o = 0.03uF for frequencies greater than 1 kHz, in figure 4.3c. In order to accommodate other frequencies, the sense impedance has to be made smaller, thereby leading to loss of resolution due to detector noise.

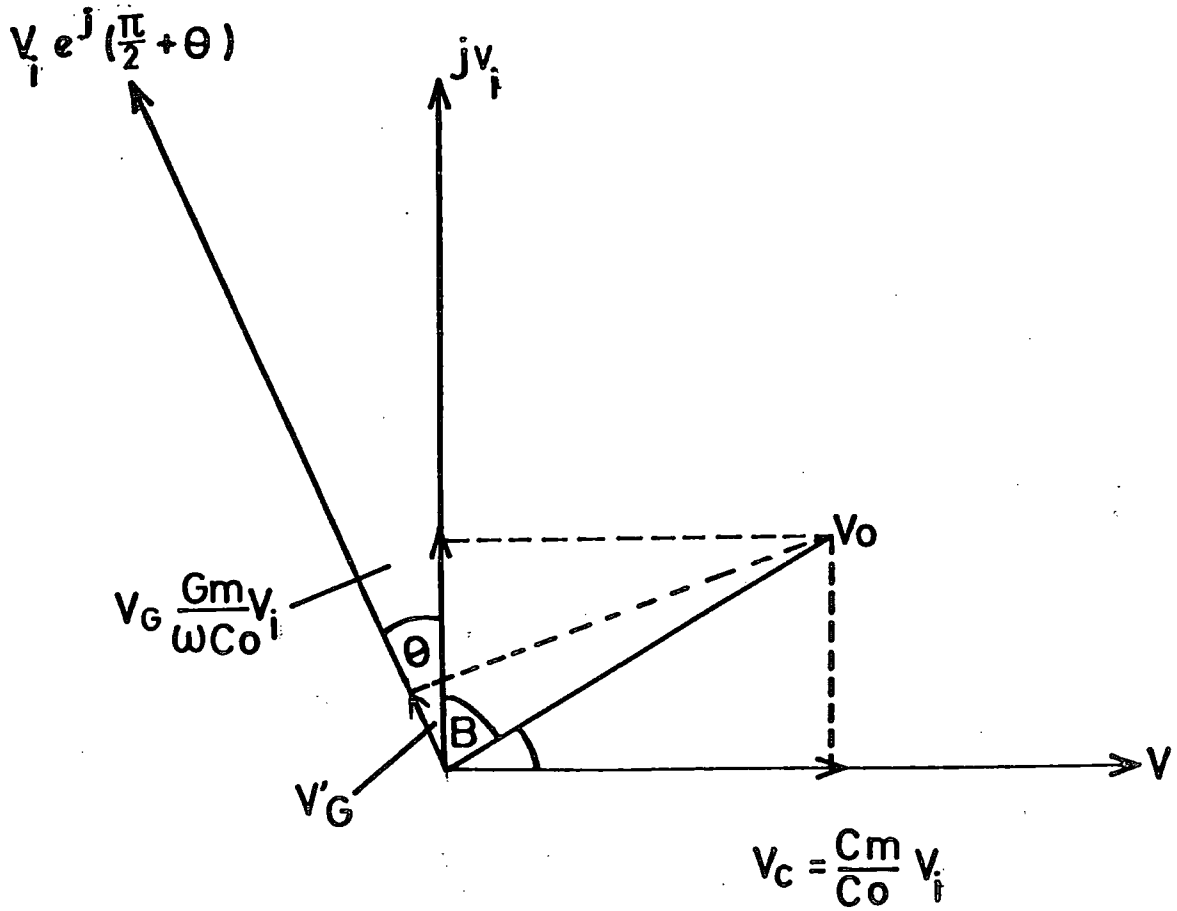


Figure 4.7 Effective rotation of admittance vectors in the presence of a parasitic capacitance.

A better approach is to use a virtual-earth amplifier (VEA) as the detector. This type of detector has a very low input impedance and measures the current directly. The cable admittance has negligible effect in this configuration as it is shunted by the very large input admittance of the detector.

4.32 Input Circuit with VEA.

A VEA can be formed from an operational amplifier with shunt feedback as in figure 4.4. It produces an output voltage:

$$v_f = - Z_F \, i_m \qquad (4.10)$$

where Z_F is the feedback impedance. By choosing this as a capacitor, the frequency dependence of the conversion factors is eliminated. Thus defining:

$$Z_F = 1 / j\omega C_F \qquad (4.11)$$

we obtain from equations 4.5 and 4.6:

$$G_m = C_F / v_0 \, \mathrm{Im}(v_f) \qquad (4.12)$$

$$C_m = - C_F / v_0 \, \mathrm{Re}(v_f)$$

The actual design is very similar to that described by Boudry (2) where a detailed appreciation is given. The circuit, shown in figure 4.5, includes an active feedback section, in addition to the

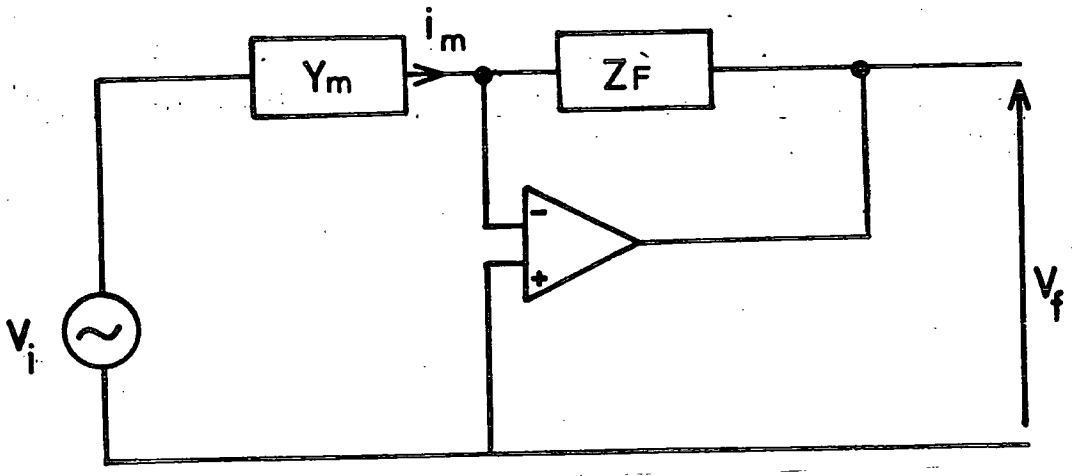


Figure 4.4 VEA measurement configuration.

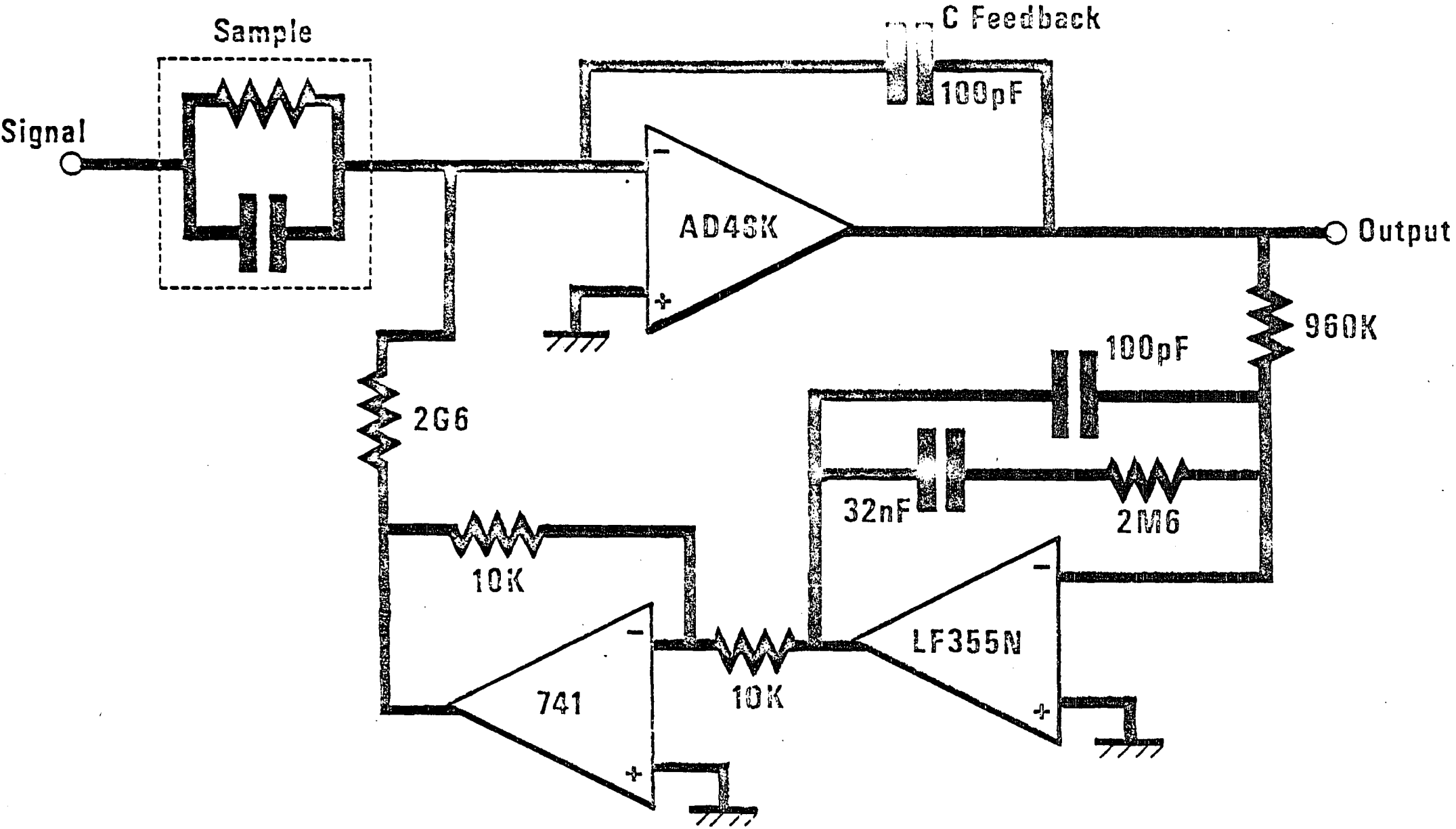


Figure 4.5 Circuit diagram of virtual earth amplifier.

capacitive one. This active feedback section acts as a dc leakage path for displacement currents that might otherwise upset the amplifier output.

4.33 Bias Injection Circuit

The circuit that mixes the dc and ac signals and applies them to the sample is also important as it is a source of phase and capacitance error. Initially the ac signal was coupled inductively into the system using an rf transformer, but in practice this was found to have a low frequency limit of 1 kHz which meant that a second mixer was required to function below this frequency. Fortunately, this coincided with a change of lock-in input preamplifiers. For high frequencies, a voltage preamplifier followed the variable sense element, whilst at low frequencies a current sensitive preamplifier was used. The actual input impedance of the latter (nominally 1 ohm at a gain of 10^{-6} A/V) acted as the sense element and thus replaced the need for a variable sense element. The mixer circuit that was used with the VEA is shown in figure 4.6 and again follows that of Boudry (2).

4.4 Calibration

Stray admittances introduce frequency-dependent error that has to be compensated for by calibration of the equipment at every frequency. The loss can be represented by an effective rotation or change in phase of the reference signal as demonstrated in figure 4.7. The resultant output voltage is altered from:

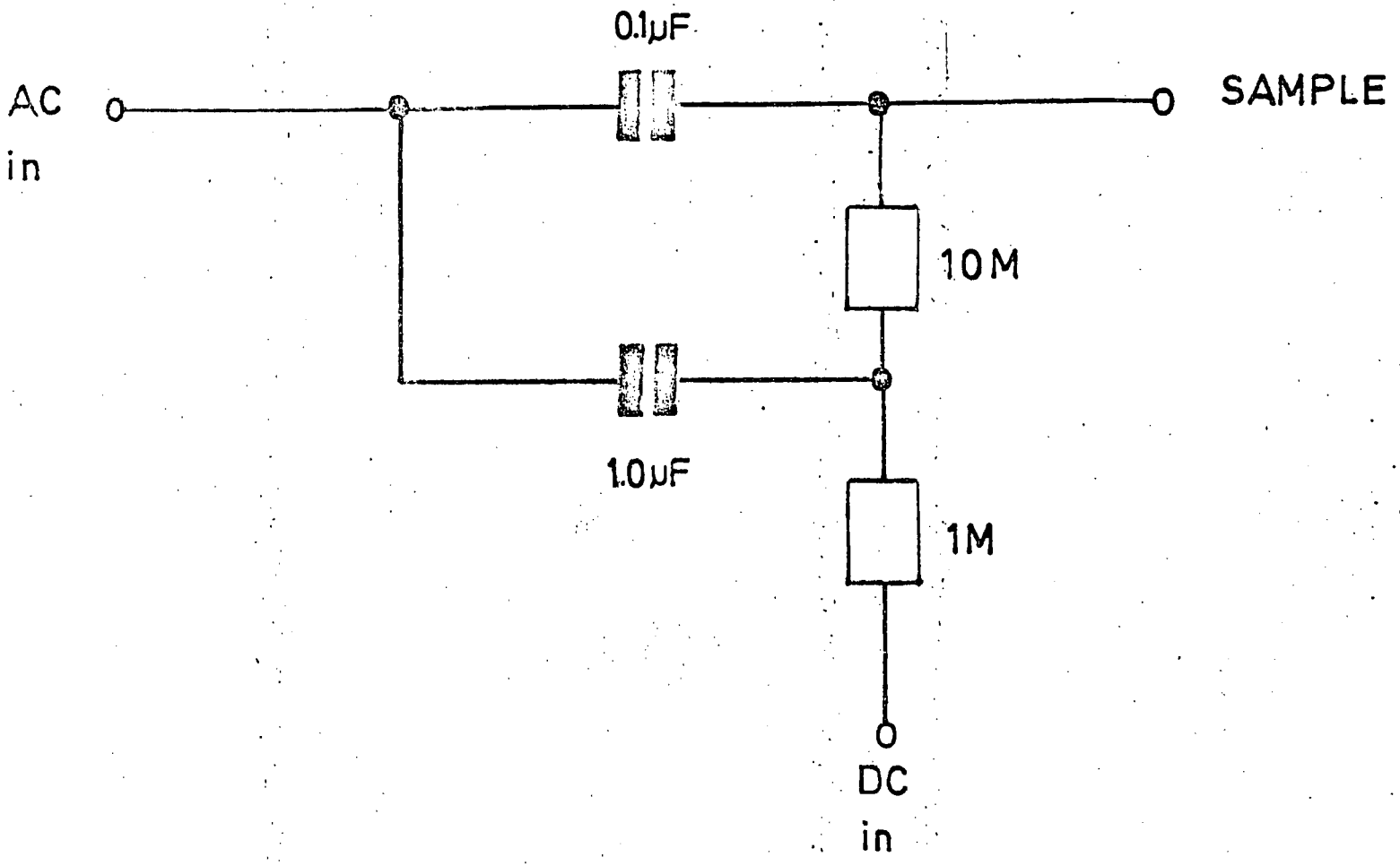


Figure 4.6 Mixer for dc and ac signals.

$$v_g = v_o \cos B = j(G_m/\omega C_o)\, v_i \qquad (4.13)$$

to

$$v_g' = v_o \cos(B + \theta) = v_i \omega (G_m/\omega - \theta C_m)/C_o \qquad (4.14)$$

where θ is the loss angle and, assuming $\cos\theta=1$, $\sin\theta=\theta$. Therefore, a phase error introduces a term C_m in the expression for G_m. If we do a rough calculation, assuming that θC_m is not greater than 5% of G_m/ω, for typical values of conductance and capacitance of 1pF and 500 pF respectively we find that $\theta<10^{-4}$. That is, the phase control on the front of the lock-in-amplifier must be adjusted to within less than a thousandth of a degree for accurate calibration; obviously this is very difficult. An attempt was made to automate this tedious procedure by connecting this control to a stepper motor and from there to the microcomputer. However, the backlash on the control and the stringent accuracy requirement meant that this attempt at automation was unsuccessful.

The actual process of calibration is done by substituting the sample with standard components. Polystyrene capacitors were found to be the best low loss capacitors; variable air-spaced ones suffered from slight variation owing to humidity changes, whilst mica ones were found to be too lossy. The capacitor is treated as ideal and the phase control adjusted until there is no deflection on the conductance meter. This is checked by inserting a known resistor in parallel and ensuring that the value registered on the conductance channel is

correct. At the same time, the chart recorder is calibrated so that an integral number of vertical divisions correspond to a particular value. Before the above is carried out, the zero offset controls of the lock-in-amplifier are used to adjust the meter deflections to zero. These are rechecked after calibration as they are found to be dependent on the position of the phase control. A summary of the above procedure is given below:

(1) With the sample disconnected, the zero offset controls on the lock-in-amplifier are used to set both capacitance and conductance meters to zero.

(2) An "ideal" capacitor is inserted and the phase control adjusted until the conductance meter registers zero.

(3) The sample is disconnected and the zero offsets checked and reset if necessary; (2) is then repeated.

(4) A resistor is then added in parallel with the capacitor. The ratio of the measured values of capacitive and conductive voltage should be equal to ωCR if the equipment is correctly calibrated. This relation is simply derived from equation 4.7.

4.5 The Microcomputer

4.51 The Hardware

In the conductance technique many admittance-voltage plots are made at different frequencies from which the parallel conductance is extracted by compensating for C_{ox} and R_s. The transfer of data from graph paper to computer for this compensation can lead to errors. It was therefore decided at an early stage in the work to incorporate a microcomputer to do the data collection and transmission to a

mainframe computer. At that time there was no "fully dressed" microcomputer such as the relatively modern Commodore PET. There were several single board computers on the market, but they lacked expandability and did not represent a complete system. An SWTPc 6800 system hobby-kit was purchased, with the limited funds available, to emulate the sophisticated university system which was used initially to demonstrate the idea. It was of modular construction where extra memory or peripheral boards could be fitted on the spare slots provided. All these were assembled by soldering the components into the bare boards supplied. A total of four 4kbyte memory boards and seven peripheral interface boards were made.

There were two different types of peripheral board, serial and parallel, based on the Motorola 6850 and 6820 integrated circuits respectively. The serial boards were for communicating with other computers or terminals and the parallel ones for interfacing with A/D, D/A converters, a digital voltmeter and a cassette recorder. The A/D, D/A converters were used to connect the microcomputer to the experimental equipment. The Ferranti ZN425E dual mode 8 bit data acquisition chip was the integrated circuit around which both A/D and D/A converters were built. Few external components were required and, therefore, it was possible to redesign one of the peripheral boards to accommodate two such units. It was found that the 1/2% accuracy of the A/D converter was insufficient when subsequent mathematical data manipulation had to be undertaken. Hence, this part of the system was upgraded with a 3½ digit DVM, with the advantage that the data acquired was visible and able to be verified. The accuracy of this has been found to be sufficient. The D/A converter can be used under

program control to provide the gate bias. Any required dc offset is derived from the same power supply that is used to run the cassette recorder. An operational amplifier is used to combine the two voltages.

The data and programs are encoded digitally on an industrial Racal P70 Digideck cassette recorder. The information is stored on the cassette tape in 1 kbyte large blocks, each of which corresponds to approximately one terminal screen full of characters. Reliable floppy disc systems were unavailable when the original system was constructed, but, nevertheless, magnetic tape is still the preferred storage medium for datalogging systems.

The most expensive item of hardware associated with the microcomputer was a Cifer Systems terminal. This particular model was chosen because it was the standard in the department and also because it was compatible with the mainframe computer that was used.

4.52 The Software

In order to run a computer system that collects data, stores and dispatches it to a mainframe computer, an operating system is required. SIXTH, developed in this department by Dr B.J. Stanier, and based on FORTH (3) is not only an operating system, but also an assembler, editor, interpreter and compiler. It is a complete package which provides the experimental physicist with a high element of control over his equipment.

SIXTH is a dictionary-based language consisting of words which correspond to certain operations. READ, for example, will transfer one block of information from the cassette to a buffer area within the main memory of the microcomputer. There are words to control peripherals and ones that do the normal programming type operations such as IF and DO. New definitions may be defined mnemonically in terms of old ones to build up a user-oriented vocabulary that carries out various tasks. An example of a short program is given below where the word DOUBLE is defined to be a program that gets a letter from the terminal, duplicates it and then prints it out on the screen.

```
: DOUBLE GET DUP SEND SEND;
```

The individual commands are separated by spaces and concatenated into the new command by the enclosing : and ;.

SIXTH is a stack oriented language manipulating numbers in a reverse Polish fashion. In this respect, it can be likened to a Hewlett Packard calculator in that, in arithmetic operations, the operator follows the operand, e.g. 2 2 * . (. prints the result). On the basic system, only integer manipulation is available; but for ease of use and intelligibility (since very small capacitance values were to be displayed), it was decided to add a floating point package to the system. This was installed at the very top of the microcomputer memory. The linking programs between it and SIXTH are given in the first section of Appendix I. Numbers on the stack in floating point format can be manipulated with commands such as X. and +.. Binary-wise, the numbers are 4 bytes wide: 1 byte for the

exponent, 3 for the mantissa. Since the stack is only two bytes wide, then a floating point number takes up two locations.

The assembler level of SIXTH makes the interfacing of peripherals very easy. The subsequent block of programs in Appendix I are used to interface to the 3½ digit DVM. The next set of programs convert the input data into a presentable exponential-type form. Various programs have been written to manipulate this data: a list of them and their corresponding actions is given in Appendix 2. Their actual use in determining surface state density values is outlined in the next chapter.

4.53 SIXTH in Detail

On a programming level, the SIXTH format, where new commands are written in terms of lower level definitions, can be seen to be pyramidal in form. (Treelike would be another description.) Structured programs are developed which consist of small easily-tested modules that are linked together to perform a desired process. When many programs are written which use the same basic routines, the above neat pyramidal analogy breaks down as the system control goes from one definition at one level to another somewhere else; on a machine code level, this gives rise to what is known as threaded code (4).

When a definition is implemented, by typing a word in at the terminal, the microcomputer system monitor passes control to that word. The latter consists of a series of branches to those definitions that constitute the word; in machine code, this appears as a series of

JSR (jump to subroutine) instructions. Besides the latter, a word also contains what is known as a header. This includes four bytes that act as a label for that word and a link address which holds the dictionary together. The same format is used for kernel words (basic system definitions that interface the language to the microcomputer) and machine code interfacing routines where the bulk of the definition is no longer a series of JSR instructions, but rather the computer's basic instruction set.

The programs are stored on cassette and compiled into the memory of the microcomputer when needed. With the above knowledge, it is possible to undertake modifications of the compiled code which saves time editing the original source text and the consequent reloading. A simple example is the accounting of the multiplier buttons on the front of the lock-in-amplifier. This is performed by substituting the JSR instruction that implements the appropriate multiplicative routine with NOP (do nothing) instructions. This is done using the microcomputer's own monitor. Another example is the ability to restore pointers using the monitor editor after a system crash. This enables data to be recovered intact.

4.6 Sample Details

4.61 Source of Samples

The silicon wafers were provided by three industrial establishments: Philips Research Laboratories, Redhill; GEC Hirst Research Centre, Wembley; and the Plessey Allen Clark Research Centre, Caswell. The first supplied a standard sample which had already been

analysed to give some information on the surface states within the bandgap. This sample was used to check our equipment and ensure that it was giving the correct results. The others provided simple substrates with various oxide thicknesses, predominantly 100 nm, but some as thin as 5 nm. Two oxides were also grown in the Department of Applied Physics at Durham - one 60 nm thick on an epitaxial substrate and another 12 nm thick on a simple bulk substrate. In addition, a silicon sample which was doped with gold, diffused in from the rear side, was used. This was supplied by Dr P.G.C. Allman and originated from Dr A.G. Nassibian.

4.62 Sample Characteristics

(1) The Philips sample was n-type, 111 orientation, with an epilayer doped with arsenic to give an electron concentration of approximately 10^{17} cm^{-3} . The oxide was wet grown at 1200 K in oxygen.

(2) The bulk GEC samples were n-type, 111 orientation, predominantly with a doping concentration of 1.3 x 10^{15} cm^{-3} . The oxides were of various thicknesses grown in dry oxygen at 1400 K. A set of p-type epitaxial samples from GEC had an epilayer with doping concentration of 5 x 10^{14} cm^{-3} oxide layer 100 nm thick.

(3) The Plessey samples were both n-type and p-type 100 orientation of 2 ohm cm and 4-6 ohm cm resistivity respectively. They possessed 5 nm dry oxides.

(4) Two wet oxides were grown in the department - one 12nm on a 3 ohm cm bulk p-type substrate and the other 60 nm on a epitaxial p-type substrate.

4.63 Sample Contacting Procedure

Before an ohmic contact could be made to the back of the samples, the oxide had to be removed. Initially this was done with a PTFE stick and diamond paste, but an etching procedure using buffered HF was found to be easier. For p-type silicon, aluminium was then evaporated and, for n-type, a gold-antimony alloy. This was followed by a high temperature anneal in nitrogen at 770 K for ten minutes for p-type, and at 730 K for fifteen minutes with n-type. The Ohmic contacts were then checked on a curve tracer; usually, a straight line was sufficient proof, but calculation of the resistivity and comparison with the bulk value would be a complete procedure. Sometimes, especially on n-type material, further anneals were found to be necessary.

Top contacts of 1mm diameter were evaporated through a brass mask using an Edwards Mk IV evaporator from a tungsten filament. Langmuir films required the substrate to be cooled by liquid nitrogen and also a very slow evaporation rate. Alternative top contacts such as mercury drops and graphite paste were used when a quick evaluation of the sample was required.

4.64 Sample Measurement

Physical contact to the top electrode was made with a gold ball-shaped probe that was controlled with a micromanipulator, whilst contact to the back was through flying lead attached to the sample with silver paste (Acheson Electrodag 915). The sample was mounted on an insulating base and measured in a stainless steel cryostat,

although sometimes a specially constructed glass sample chamber with integral heater was used. Between measurements, the samples were stored in a desiccator under dry nitrogen.

4.7 Experimental Results

The experimental layout for the admittance measurement system is shown in figure 4.8. In this section, some basic results using this system are presented. These are divided into two parts, firstly those obtained without utilising the microcomputer and those obtained with it.

4.71 Admittance-Voltage Characteristics

The low frequency (1kHz) admittance-voltage characteristics for an n-type epitaxial MOS silicon structure are shown in figure 4.9. The flat portions of the capacitance characteristic on the left and right sides of the curve indicate the presence of inversion and accumulation of the device. The depletion region, in between, exhibits a peak in the conductance characteristic produced by the action of surface states. The almost zero value of accumulation conductance denotes a very small series resistance value, which is to be expected with an epitaxial substrate. However, the influence of the series resistance increases with frequency and it was found, even on epitaxial substrates, that as the frequency increases, a plateau similar to that in figure 3.5 is observed. Thus compensation for series resistance can be seen to be necessary even for epitaxial

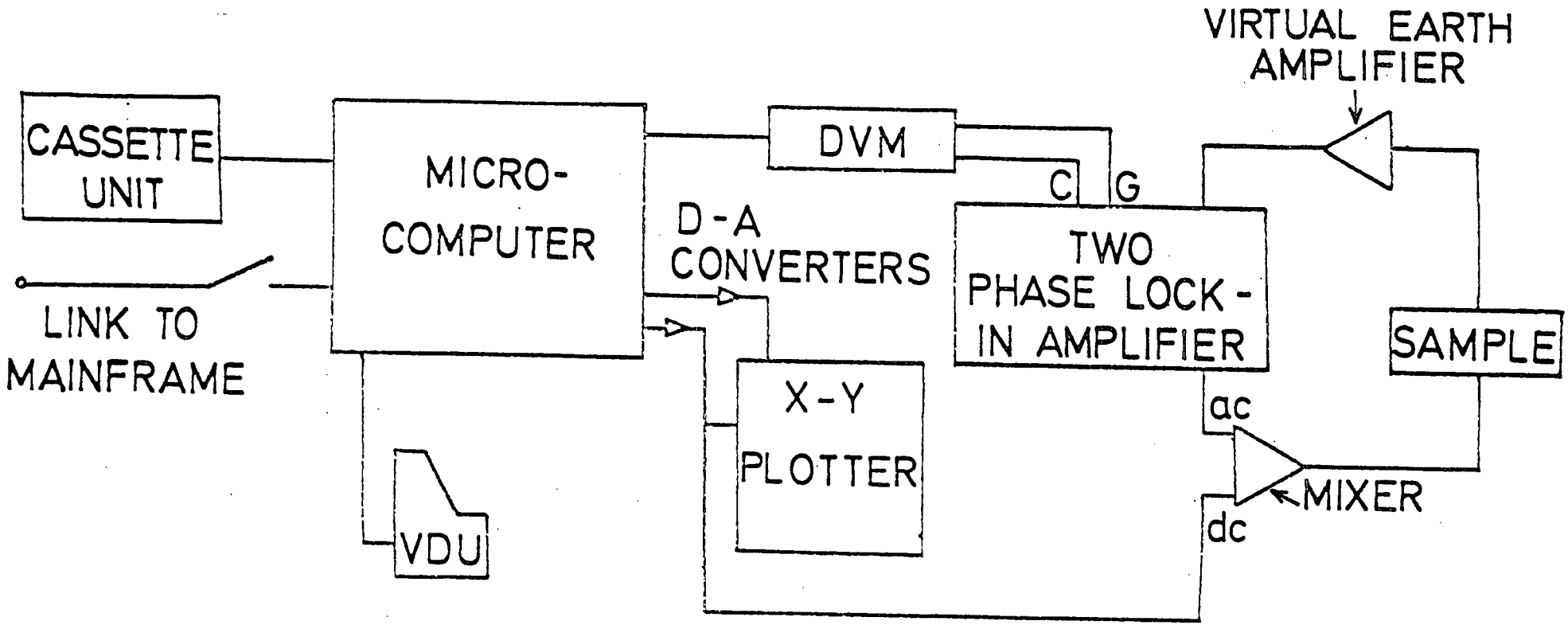


Figure 4.8 Experimental Layout for admittance measurements including microcomputer.

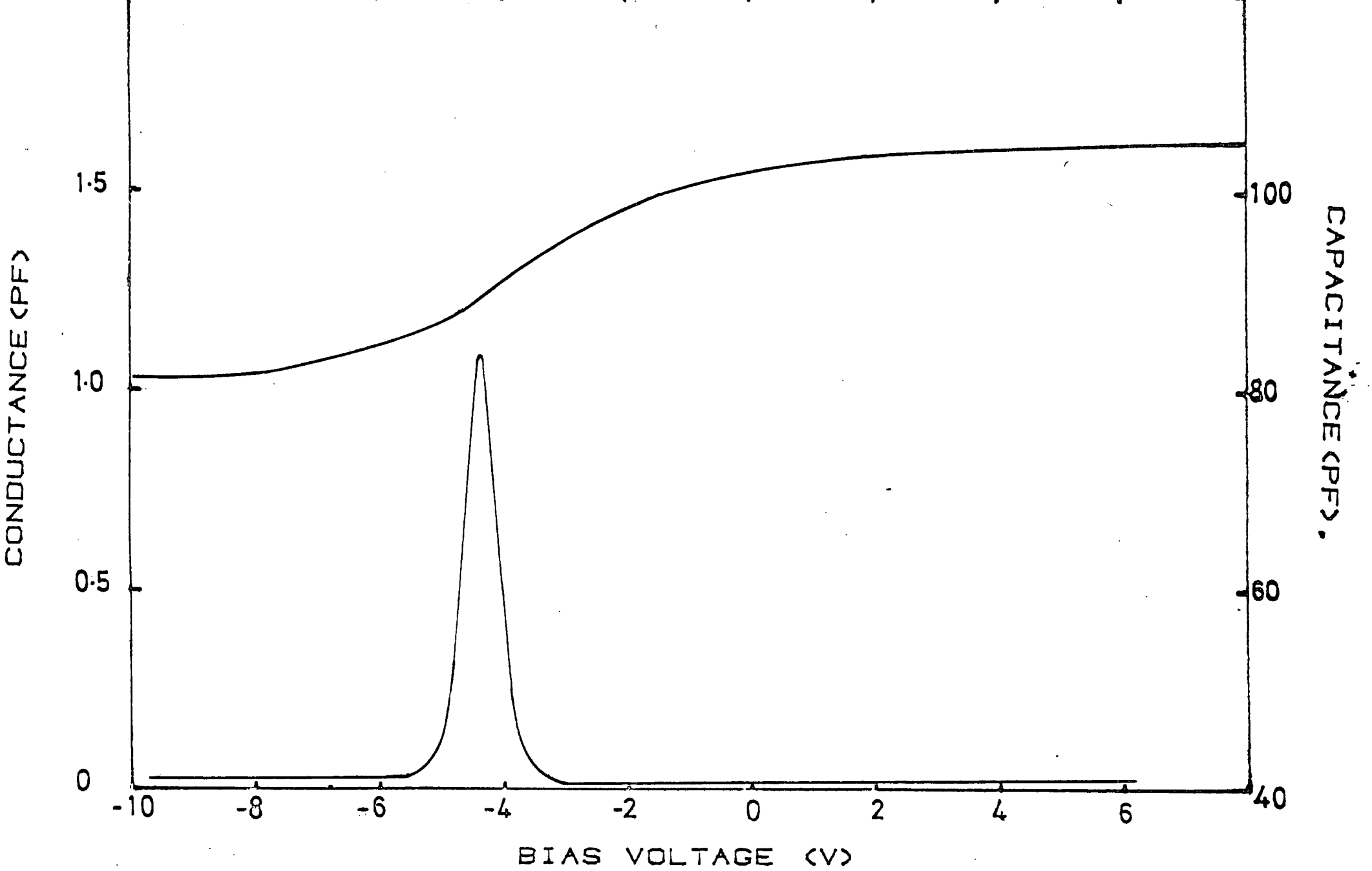


Figure 4.9 Measured admittance-voltage characteristics for epitaxial n-type silicon sample.

samples.

The admittance-voltage characteristics, measured at 10kHz, for a p-type epitaxial silicon sample are shown in figure 4.10. Accumulation now occurs at the opposite voltage value (ie left), where again an almost zero accumulation conductance can be seen. The presence of a second conductance peak and capacitance inversion (which normally does not occur until well below 100Hz) is due to the presence of an external inversion layer outside the top contact, formed by the action of positive charge within the oxide. This charge is the fixed oxide charge mentioned in section 2.2. It is also apparent through the displacement of all the MOS measured characteristics to the left of the zero voltage axis.

4.72 Results obtained with the Microcomputer

In figure 4.11, the measured characteristics (100kHz) for a p-type bulk sample are shown. It can be seen that the high accumulation conductance, caused by the larger series resistance, actually obscures the surface state induced conductance peak. The parallel conductance calculated using the microcomputer is shown for two different conditions to emphasize the importance of the series resistance compensation. That is, it is calculated using equations 3.13 and 3.14 where, in the latter case, series resistance is not taken into consideration. This may be more clear in figure 4.12, where the parallel conductance for an n-type bulk sample is shown, (a) without and (b) with series resistance compensation. A series of parallel conductance plots versus bias for an epitaxial n-type

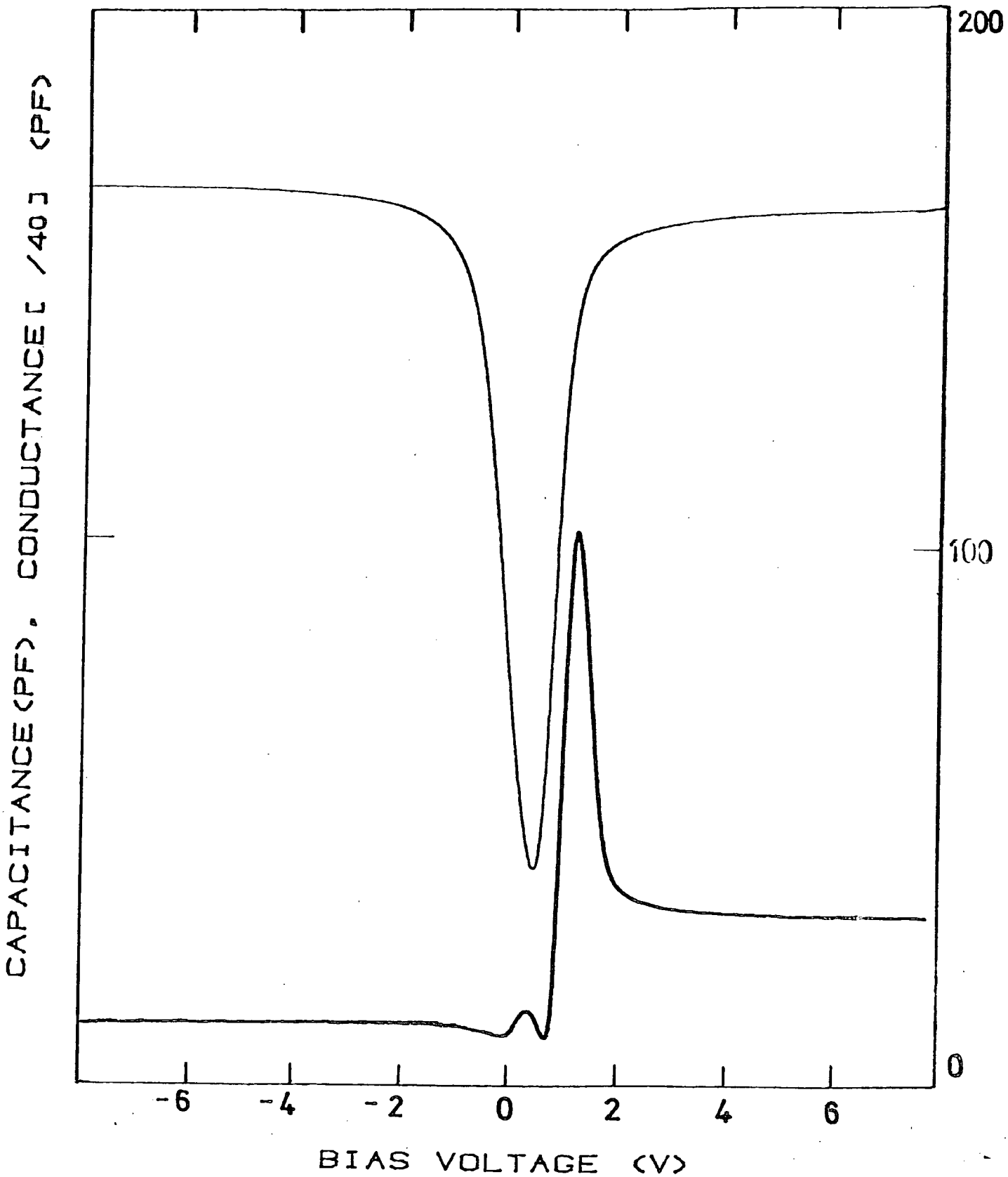


Figure 4.10 Measured admittance characteristics for epitaxial p-type sample.

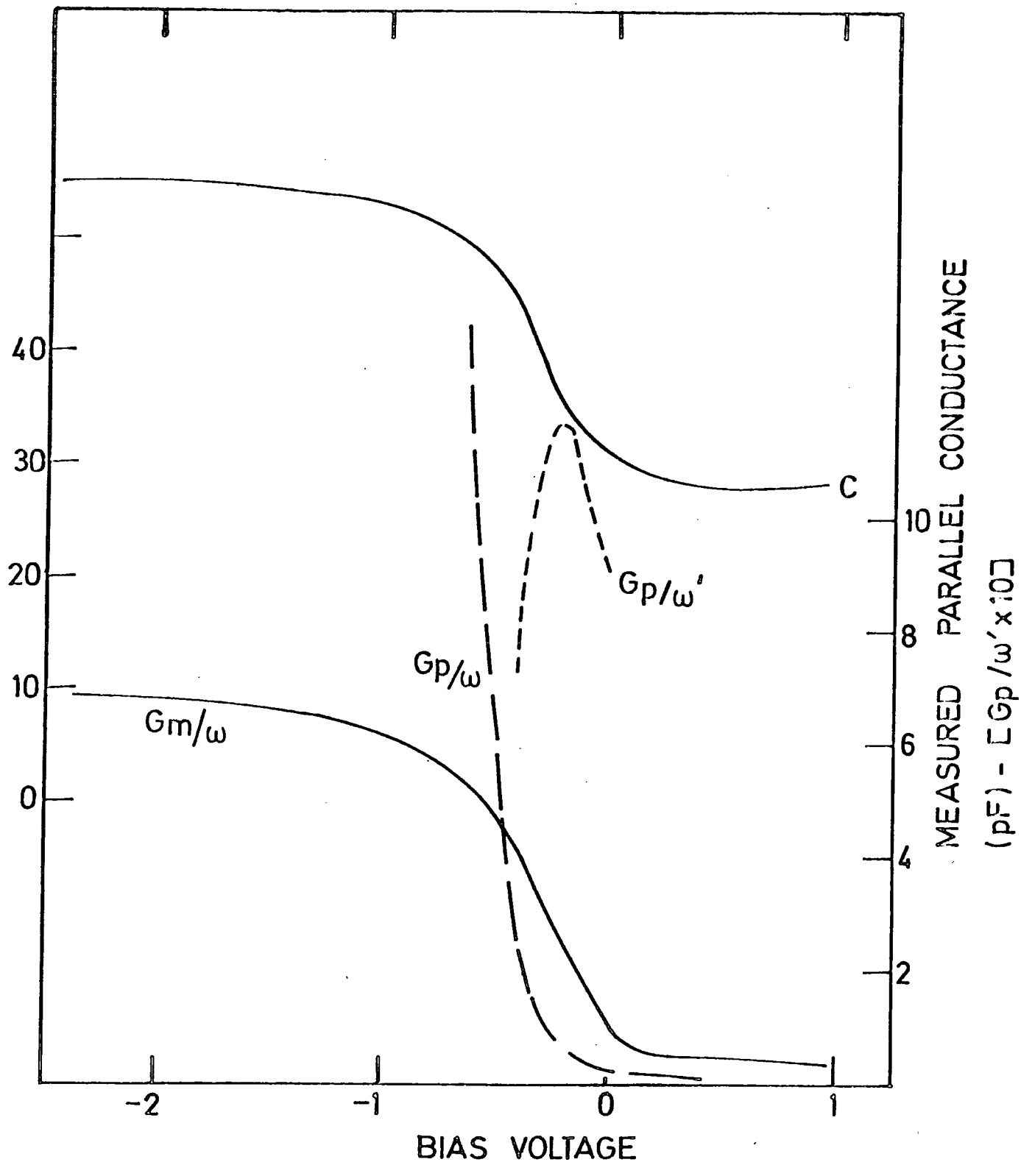


Figure 4.11 Admittance characteristics for bulk p-type sample.

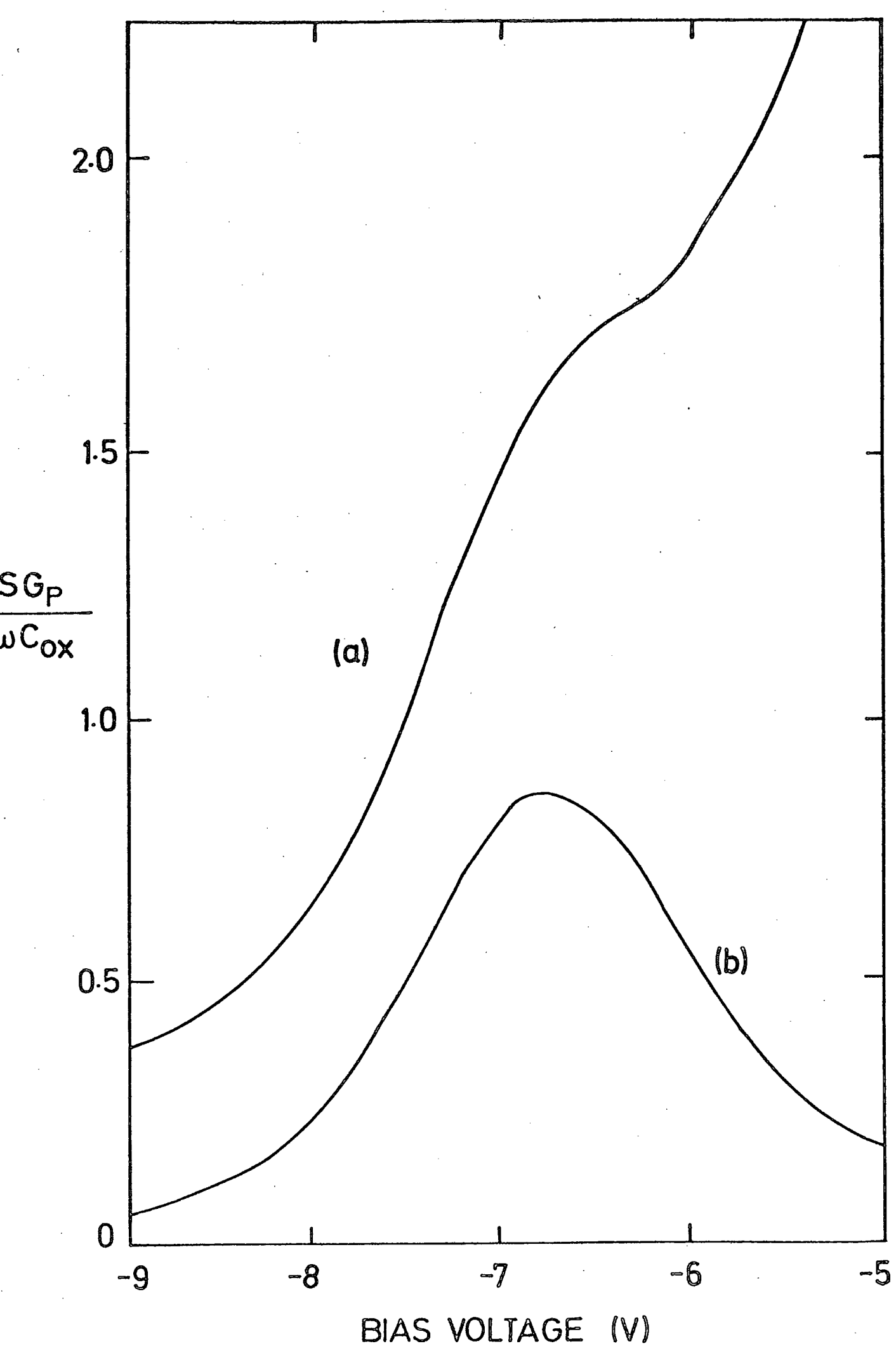


Figure 4.12 Parallel conductance curves for n-type bulk silicon (b) with and (a) without series resistance compensation.

structure are given in the next chapter where they are used to obtain a parallel conductance versus frequency curve.

Chapter 5

Surface State Density Measurement - A Novel Approach Using a Microcomputer

5.1 Introduction

In this chapter, a semi-automatic interface characterization system based on a microcomputer is introduced. The ability of the microcomputer to work in real time has enabled a development of the conductance technique to be made which significantly reduces the effort required to obtain surface state density information for an MIS device. Furthermore, by regarding the parallel capacitance of the semiconductor surface in a different way, ψ_s, the surface potential, can also be easily found.

5.2 Practical Drawbacks of the Conductance Technique

The conductance technique may be theoretically the best method for obtaining the surface state density of an MIS device, but practically it has several problems. For example, it is difficult to predict from the measured values of capacitance and conductance the likely location in the frequency domain of the resultant parallel conductance peak. Thus, the procedure of admittance measurement at various frequencies, outlined in section 3.4, is obviously wasteful, since there will be only a small voltage range which will yield parallel conductance peaks within the frequency range of the equipment. Computed curves of parallel conductance versus frequency for different surface potentials shown in figure 5.1 help to demonstrate this point. In addition, the expedient analysis techniques require accurate location of the parallel conductance peak so extra scans are normally required.

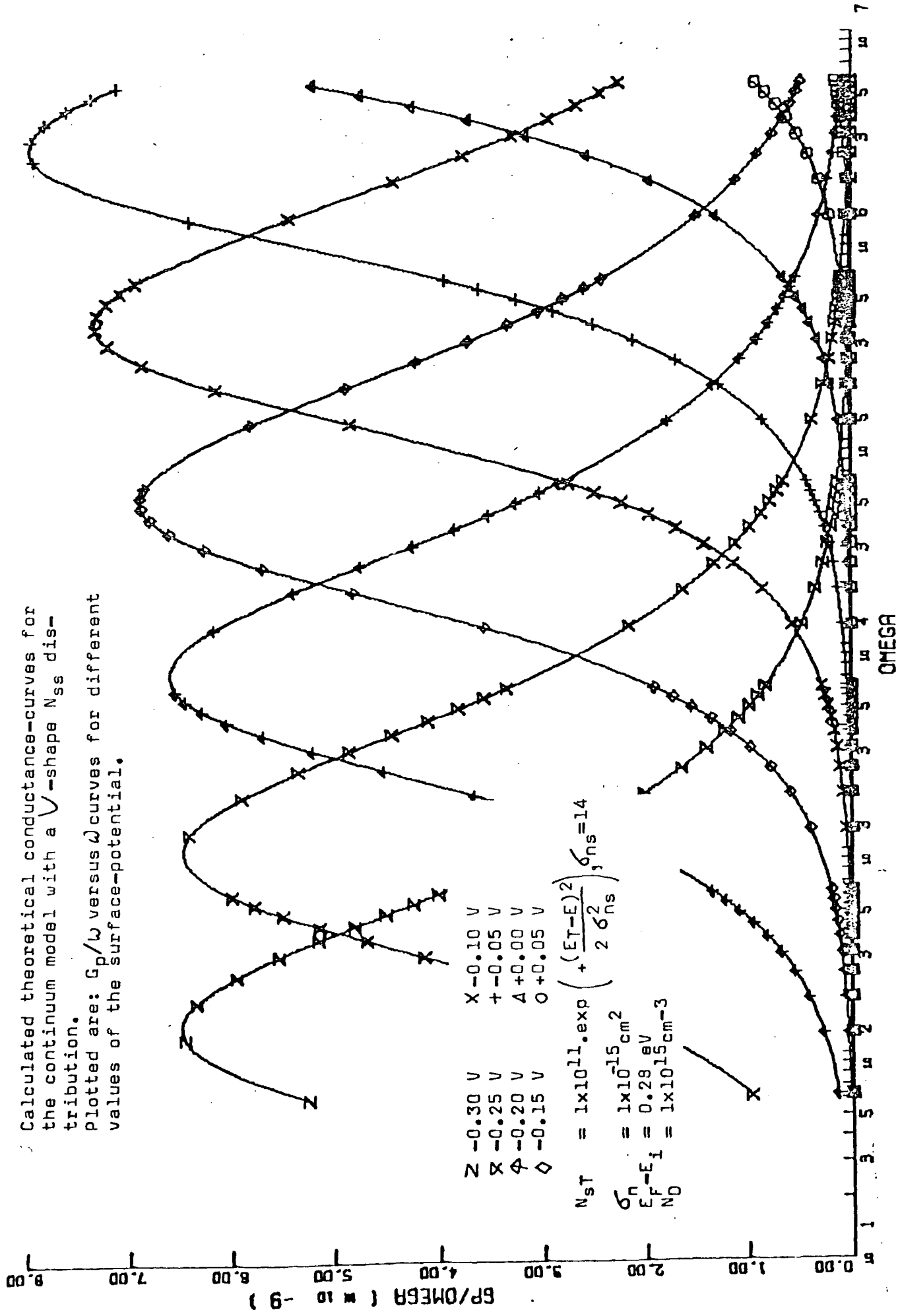


Figure 5.1 Computed curves of parallel conductance versus frequency.

A second problem is that identical voltage values at different frequencies might not correspond to the same value of surface potential: this may be due to ion motion, or trapping of charge in the oxide or, possibly, polarization. Consequently, distortion of the derived curve can result. The presence of the latter effects can be detected by examining the hysteresis characteristics when the device is cycled between negative and positive bias (see section 2.43). Since the start of this work, equipment has been described (1) which circumvents the above problems by operating in a swept frequency mode where the gate bias is held constant; however, it is complicated and great care is required in its construction. We wanted to maintain the simplicity of our apparatus but reduce the effort necessary to obtain results.

5.3 Real Time Processing

Computer-aided measurement is becoming more widespread as microcomputers become cheaper and more usable. Initially microcomputers were used simply as data logging systems; in fact, ours began in this way acting as an intelligent interface to a mainframe computer. However, small microcomputers have now become powerful enough to be used for control and/or signal processing on their own. Hence we have developed our own microcomputer as a real time processor, in particular to convert the measured data to values of parallel conductance as the bias scan proceeds.

5.4 Parallel Conductance Peaks

A set of real time parallel conductance versus bias curves for different frequencies are shown in figure 5.2. The fact that the curves exhibit maxima can be seen from a consideration of the simple single time constant expression for the parallel conductance given in section 2.51. The latter, though not strictly valid for real data analysis, is adequate for illustrative purposes as any consideration of the actual equations is obscured by mathematical complexity; and, in any case, the variation is qualitatively the same. Since equation 2.19 is symmetrical in both τ as well as ω and, as τ is directly proportional to bias, curves of parallel conductance will peak in the voltage domain in a fashion similar to that in figure 2.12. The actual curve width, however, is now determined by two factors: surface state density and the time constant dispersion. This is not the case for peaks in the frequency domain where only the latter influences their width, thus explaining their preferred use.

If we sit at the bias on the experimental curves in figure 5.2 that corresponds to a parallel conductance maximum we can see that parallel conductance values at higher or lower frequencies are smaller. Similarly, in figure 5.1, if we follow a vertical line corresponding to a single frequency, by interpolation between the curves, it can be seen that the parallel conductance curve peaks voltage-wise at the same point. That is to say that the peaks in the voltage and frequency domains are equivalent. We have shown this experimentally by sitting at the parallel conductance maximum position of a parallel conductance versus bias scan. It was found that the parallel conductance diminishes as the frequency is altered, either up

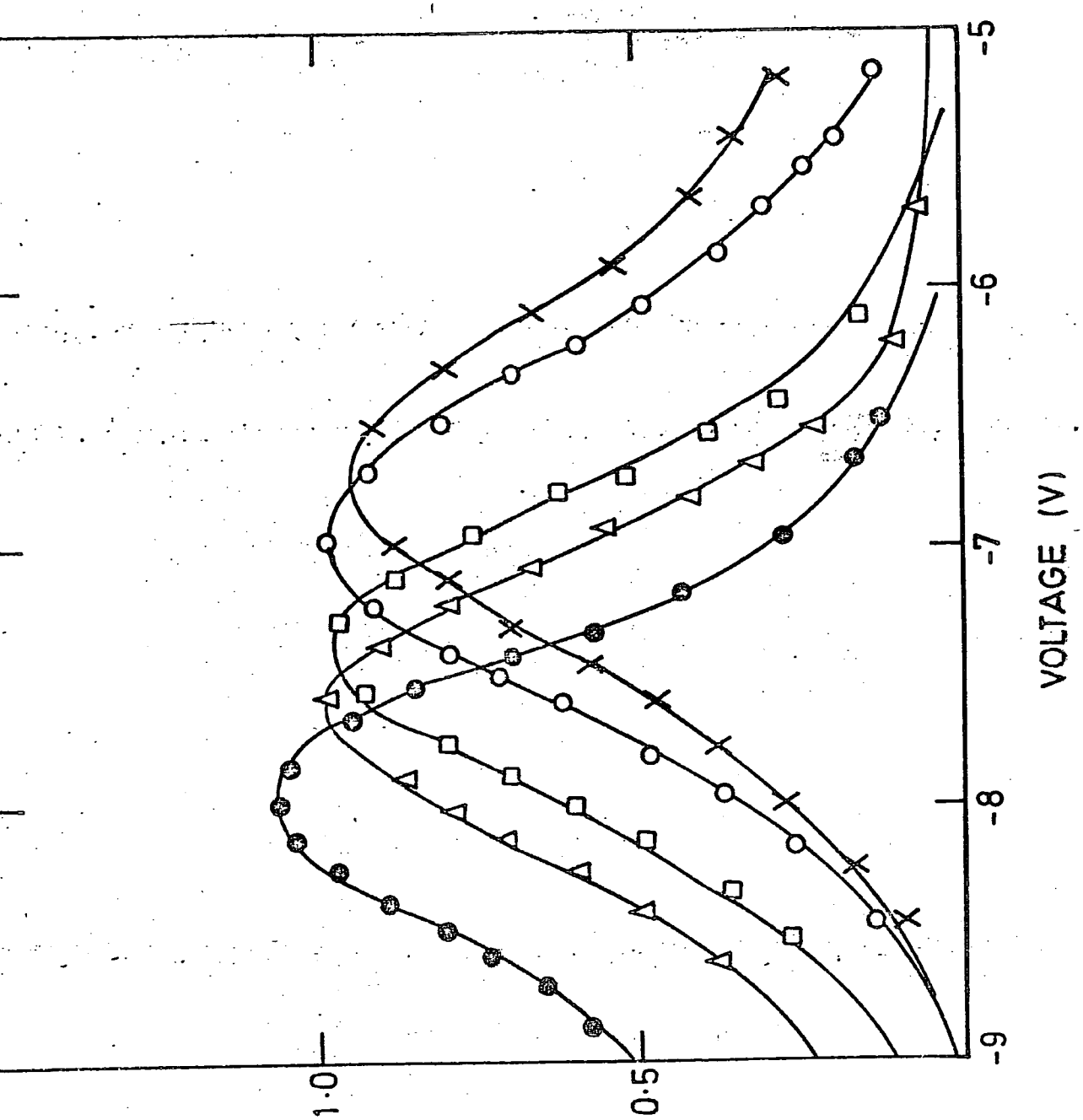


Figure 5.2 Parallel conductance versus bias for different frequencies.

or down.

A greater appreciation of the above can be obtained by considering the single level distribution again, but at biases away from the trap level. The above principle of sitting at any parallel conductance peak maximum in figure 5.3, changing the bias and seeing the parallel conductance diminish no longer holds. Thus, it can be seen that only slowly-varying distributions, such as the U-shaped one that figure 5.1 corresponds to, produce the above parallel conductance peak equivalence. This will not present problems since these are the only ones entertained by the mathematical theories that match the experimental curves.

5.5 Novel Surface State Density Measurement Procedure

The purpose of demonstrating that the parallel conductance maximum is equivalent in both domains is the basis of the proposed surface state density measurement technique. It was shown in Chapter 3 that the determination of the parallel conductance maximum in the frequency domain is of prime importance in calculating surface state density information. Since it has been demonstrated that the parallel conductance maximum is identical in the voltage domain, the proposal is to discover it there, which is far more easily done in real time with our microcomputer system. If the bias corresponding to the maximum is held constant while the frequency is varied by a factor of five and the parallel conductance is then measured, it can be seen that the Simonne ratio, and thus the surface state density, will be obtained. This procedure is obviously quicker than the conventional method where all the data has to be collected before any analysis can

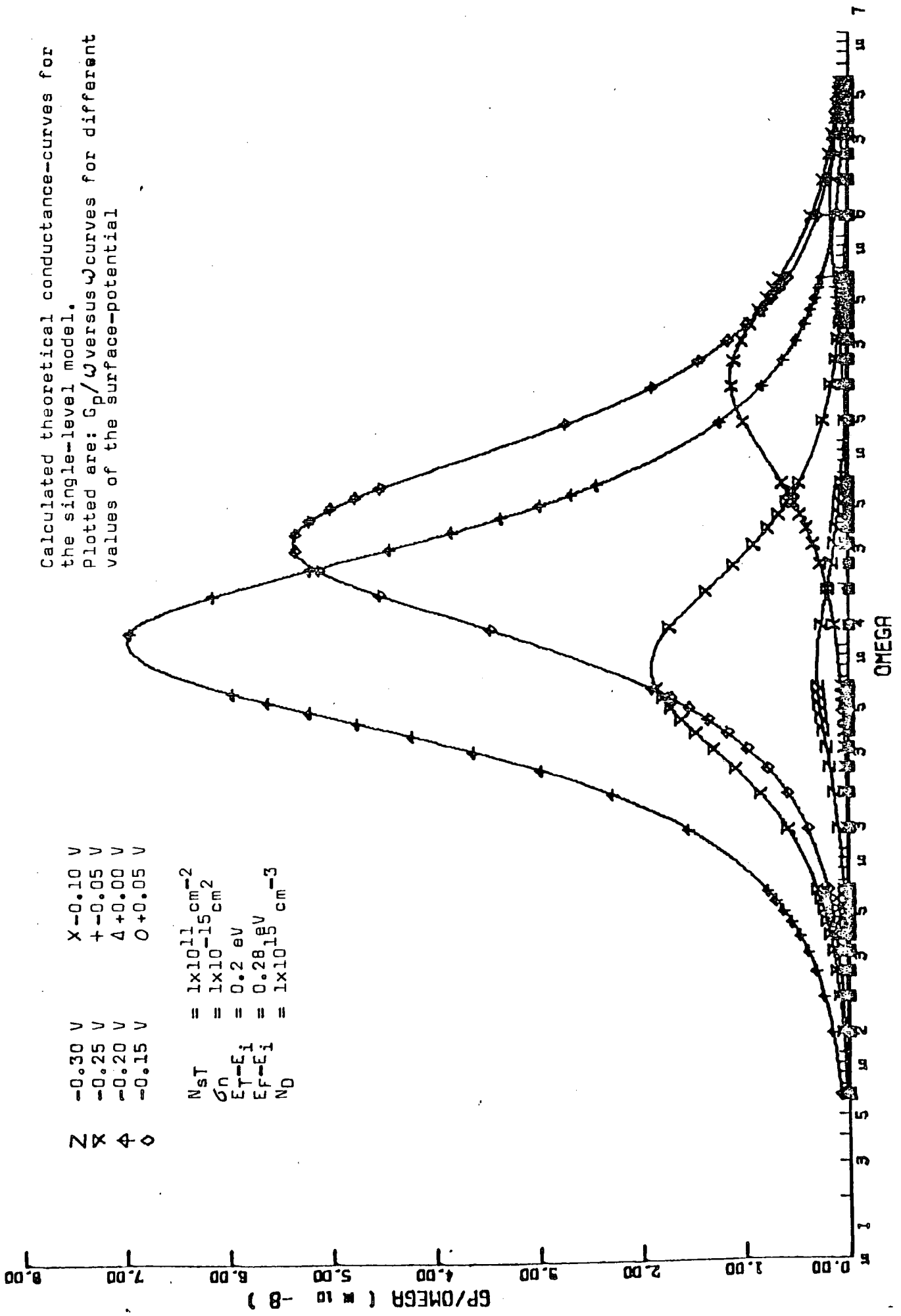


Figure 5.3 Parallel conductance versus frequency for different biases for a single state distribution

take place. Repetition of this procedure at different frequencies will build up a series of values of surface state density across the bandgap. Each point takes about half an hour to obtain, including time for calibration and calculation of bandgap position using the following. This is an estimation for the production of an accurate value; it is possible to obtain quicker less accurate answers in minutes. This compares very favourably with the period of days necessary in the standard conductance technique.

5.6 Semiconductor Capacitance

The semiconductor surface capacitance, C_p, calculated using equation 3.13, is the sum of the surface state and depletion layer capacitances (see section 2.41). It has been shown (2) that, at the parallel conductance maximum, the parallel conductance value is equal to half the surface state capacitance. Therefore, by simple subtraction, a value for the depletion layer capacitance can be found. This is a single-valued function of the surface potential and in the depletion region is given by the simple expression:

$$C_{sc}^{-2} = 2 (\Psi s - kT/q)/q \varepsilon_s N_d \qquad (5.1)$$

Consequently, if the doping density is known, the above equation can be used to relate a particular surface state density to a bandgap position. The advantage of this method is that the surface potential is obtained from the same data which gives surface state density; no further separate measurement is necessary.

5.7 Assisted Peak Location

Precise determination of the parallel conductance peak position is obviously very important, but it is not easy to do this by eye from a graph, especially in the presence of experimental noise. A more reliable semi-automatic peak locator has been developed which removes the uncertainty in the location of the peak. It is run on the microcomputer in the form of a low noise differentiator which measures the gradient of the experimental curve accurately in the presence of noise.

The process is based on the method of least squares, which is an elegant technique for handling corrupted experimental data. Here a representation of the data in the form

$$y = a_o + a_1 x + a_2 x^2 + a_3 x^3 + \ldots\ldots a_p x^p \qquad (5.2)$$

is calculated by minimising the sum of the squares of the residuals i.e. the difference between y above, assuming various values of the coefficient 'a', and y-measured, all squared. The second coefficient represents the gradient of the function at x=0 and can be calculated in terms of local values of y which have an appropriate weighting. We assume that the data can be represented by a second order parabola by truncating the series after the third term; the gradient is then given by the following expression:

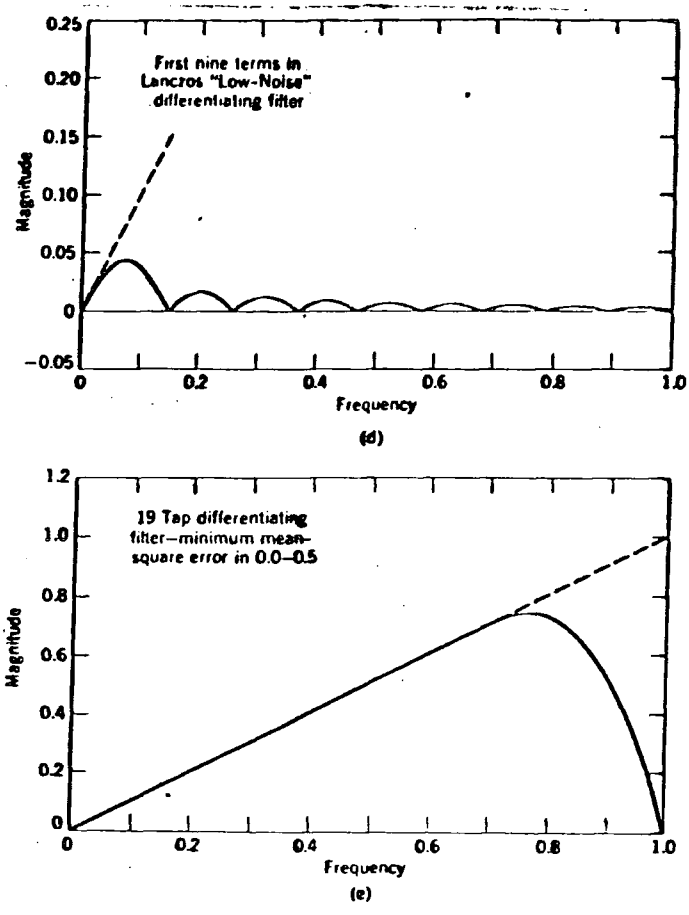


Figure 5.4 Frequency response of low noise differentiator filter. (4)

$$f'(x) = \frac{\sum_{c=-k}^{c=+k} cf(x + ch)}{2\sum_{-k}^{+k} c^2} \qquad (5.3)$$

that is, the sum of the points on either side of the point of interest, multiplied by c, the unit distance on either side, divided by some weighting factor. The actual derivation of the above is given by Lanczoz (3) and comes from a solution of a whole set of simultaneous equations. The expression above is known as a central difference formula type solution which requires knowledge of future experimental results. It is implemented by sitting at a position on the curve and multiplying neighbouring points by a factor as determined by equation 5.3 and listed in (4). The greater the number of points used, the higher the accuracy - but the lengthier the computation.

If the basic equations are resolved with a view to obtaining a backward difference formula solution, then knowledge of future values is no longer necessary and the gradient of the curve can be produced for the last measured point. In practice, the latter filter, with its predictive nature, is found to be less accurate and, indeed, a little wayward in the presence of large amounts of noise. However, when used in conjunction with the first filter, a good appreciation of the situation is obtained. The name "low noise differentiator" is derived from a consideration of the frequency response of the above shown in figure 5.4. It can be seen to be a differentiator with its high

frequency response supressed. Differentiation is an inherently noisy process since it emphasises high frequency signals; the Lanczoz filter effectively introduces zeroes into the upper end of the frequency spectrum which minimizes its response there.

5.8 Practical Procedure

In order to provide some idea of how the microcomputer is used in conjunction with the lock-in-amplifier, a typical run is now outlined. This description will include reference to the SIXTH commands that are used to get the system to perform the various tasks. It is not necessary for the operator to understand the intricate nature of SIXTH since it has been designed to be simple to use. The commands (see Appendix I for a complete listing) are user-oriented with mnemonic-type names to make them easy to remember.

The first step is to manually adjust the lock-in-amplifier to compensate for the effects of stray capacitance. This procedure was outlined in section 4.4, and included calibration of the chart recorder. The microcomputer has to be calibrated as well if the internal representation of the measured values is to be in a meaningful form, rather than the digital one inputted by some analogue to digital converter. This is done with the instruction CALIB which defines a factor that is used to compensate all the measured data. The voltage corresponding to a standard capacitance whose value has been previously entered into the computer is taken. The quotient of these two is, then, the factor by which all other input data must be multiplied. A further reason for having the internal data values in terms of capacitance and conductance is that it makes compensation

for the effect of strays so much easier. We have only compensated for the stray capacitance of the sample mount, for it was found that the conductance losses in the leads were negligible in our measurements.

Before the microcomputer is used to produce values of parallel conductance, the MIS device is checked to ensure that it gives good reproducible characteristics. This means that the forward and reverse sweeps overlay one another, but does not preclude the presence of an amount of hysteresis. The examination will also reveal gross defects such as whether the measured conductance maximum is double peaked (see section 5.8.), which we are unable to analyse, or the presence of a leaky insulator. The latter of these defects is best discovered by a quick quasi-static measurement of the system. The location of the measured conductance maximum is noted since it is in this vicinity, on the accumulation side in fact, that the parallel conductance peak will occur; in order to save time, it is best to start the computer scanning close to this point.

The next stage is to acquire the oxide capacitance and series resistance values into the system. The device is biased into strong accumulation with a voltage greater than 20 volts if possible, and the command OX typed at the terminal. The computer measures the capacitance and conductance and utilizes equation 3.12 to obtain the values of oxide capacitance and Rs/ω. The awkward frequency division is an outcome of the mathematics, and is tolerated since it makes programming easier, obviating the need to enter the operating frequency of the lock-in-amplifier. The system is now ready to give parallel conductance values.

The analogue ramp generator that has been used so far to bias the device is replaced by a voltage supply based on a D/A converter controlled by the microcomputer. The initial position is set from an examination of the exploratory curves and is usually on the zero volts side of the anticipated peak position, so that the sweep direction is away from zero. By typing SCANNER, the output of the D/A converter, and hence the bias applied to the device, is incremented. The parallel conductance is calculated at each step and output to the terminal screen and also a chart recorder. In addition, ongoing gradient values are produced by digital filters which help locate the parallel conductance peak position. If the central difference formula is used for peak location, then the voltage at which the maximum occurs has to be slightly exceeded.

Once the operator has decided that the peak position has been found, he stops the ramp by pressing any key on the terminal. This acts as an interrupt to the program and returns control to the user. If necessary, the bias is reset to the peak location using the on screen information. The corresponding value of semiconductor capacitance is found by typing in SEMICAP. The frequency is now altered by a factor of five, usually upwards because, practically, this has been found to give the best results. The reason for this is that the parallel conductance will then be on the inversion side of the peak and, hence, more accurate, since it has been shown by (5) that the error in the parallel conductance increases towards accumulation. The lock-in-amplifier has to be readjusted before this measurement can take place which involves temporary replacement of the sample with a standard capacitor. A second CALIB command is then

entered to recalibrate the microcomputer. When the device is reconnected, it should be in its former bias state, but, if charge has leaked away, then the tested-for reproducibility should ensure that the sample is in the same state. An attempt was made to construct circuitry that maintained the bias on the sample as the frequency was altered, but this was found to be unsatisfactory.

Before the value of parallel conductance at the new frequency can be obtained, the values of compensating oxide capacitance and series resistance have to be measured. This is done by biasing the device into strong accumulation again, and typing OX. The commands CALCUL OUT are then used to produce the value of parallel conductance which, when compared with G_p/ω (max), gives the Simonne ratio from which the surface state density is found.

5.9 Experimental Results

In order to check the procedure developed to measure surface state densities, a previously characterized standard MOS sample was obtained and examined. This was the Philips n-type epitaxial sample described in section 4.7. Its surface state density was calculated in both the novel way that we had developed, and also conventionally by collecting many different admittance-voltage curves. The resulting parallel conductance curves versus frequency for the latter case are shown in figure 5.5. The corresponding surface state density values are shown inset where they are compared with the results obtained from our technique. The parallel conductance versus bias data for this are displayed in figure 5.2. As can be seen, the surface state density is approximately 3×10^{11} cm^{-2} eV^{-1}. This compared favourably with

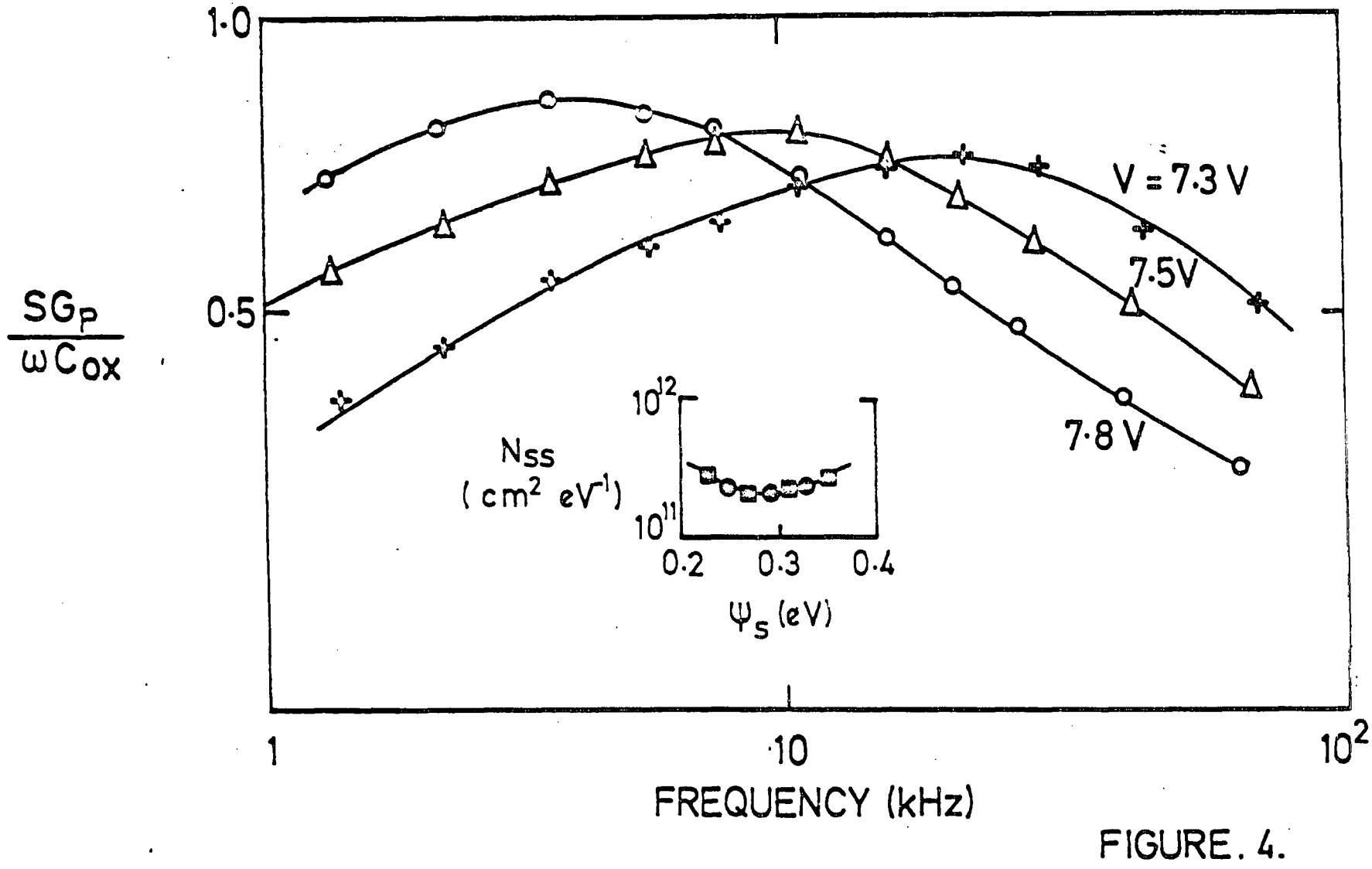


FIGURE. 4.

Figure 5.5 Measured parallel conductance curves versus frequency and corresponding surface state density for the two different methods employed. Our novel technique ( ), the standard one ( ).

the midgap value of 5×10^{11}, supplied by Philips, and also a similar value obtained using the quasi-static method.

The location of the surface state density values within the bandgap was determined using the procedure outlined in section 5.6. As previously mentioned, the advantage of this technique is that there is no need for any separate measurement or theoretical calculation to be performed. However, in order to verify our values, we did perform a Berglund (6) integration of our data and compared the results. Good agreement was found.

An epitaxial sample was used since it was found that, as with the oxide capacitance (2) it was best if these impedances were as low as possible so that only a small amount of the applied voltage was wasted by being dropped across these components. Thus, with bulk samples, the measured parallel conductance was less easy to obtain as it was obscured by the effect of the large series resistance. The values obtained were generally $3 \times 10^{11} cm^{-2} eV^{-1}$ for the wet grown samples and of the order of $10^{12} cm^{-2} eV^{-1}$ for the dry grown ones.

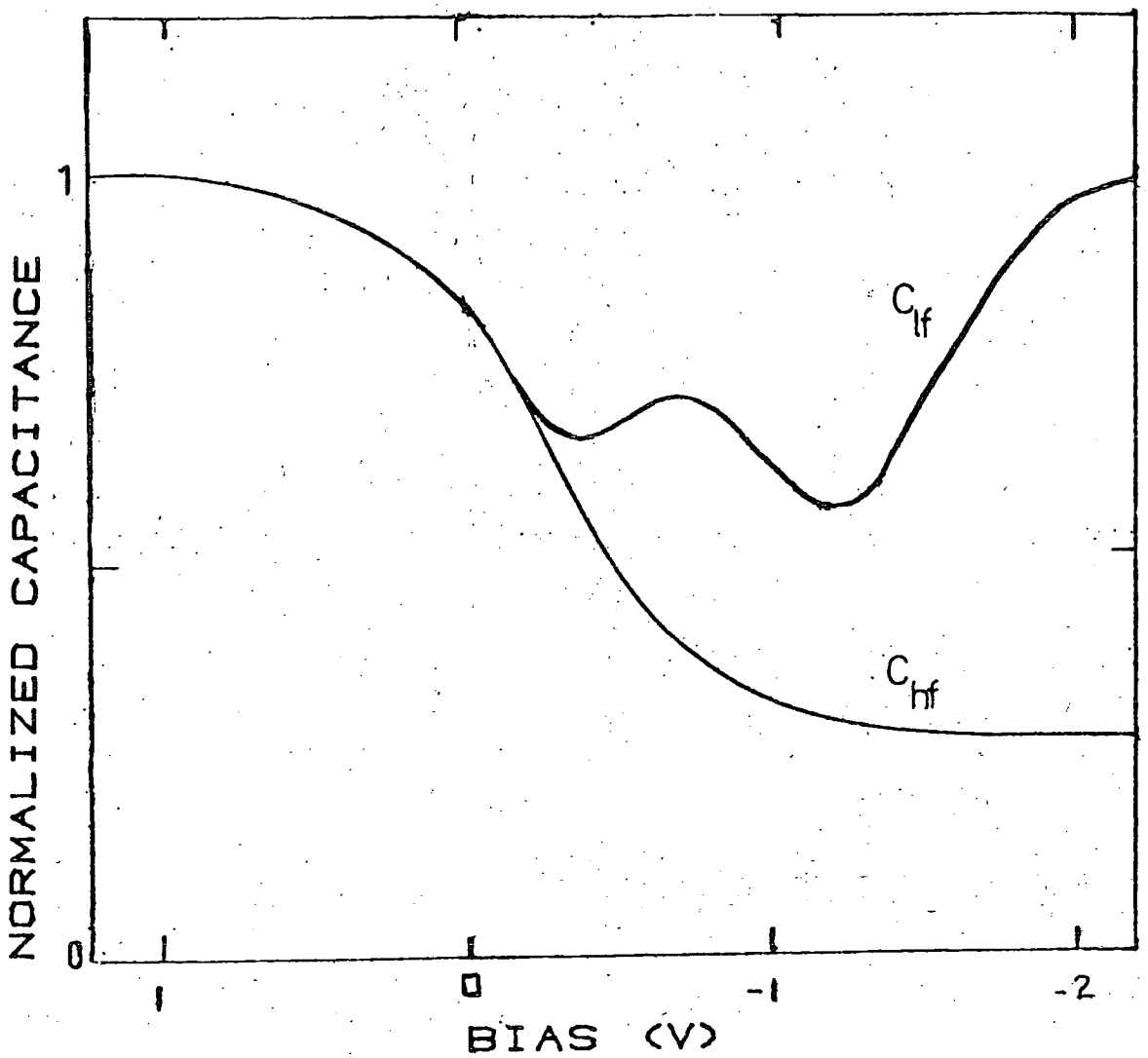
Two measurements were undertaken to see whether our system could detect surface state density change. The first was the conventional "alneal" process which consisted of a post-metallization anneal of a dry grown sample at 770K for forty minutes. The resulting surface state density was almost beyond the measurement range of the equipment and required fine adjustment of the phase control. On calculation, it was seen to be approximately $10^{10} cm^{-2} eV^{-1}$.

In the second experiment, a gold-doped sample and an identical undoped control one were compared with this technique and also with the quasi-static method. The results for the latter are shown in figure 5.6. Similar values were obtained with our technique, but owing to the poor Ohmicity of the back contact, a complete analysis was prohibited.

There were other problems when utilising our new technique, mainly produced by the presence of sodium ions. For example, double-valued measured conductance peaks seemed to give spurious results with anomalous Simonne ratios and negative values for the semiconductor capacitance. Mobile ions were proved to be responsible through the measurement of an intentionally sodium-contaminated sample which gave such twin peaks. The reason for this is that the sodium congregates in regions where it changes the surface potential on a large enough scale to produce another peak.

5.10 Summary

In this chapter, a novel surface state density measurement method that utilizes the real time processing ability of a microcomputer has been demonstrated. This has been done by outlining the practical procedure involved in the determination of a single value of N_{ss}. The advanced software makes the equipment easy and convenient to use, and is definitely more flexible than any other experimental control language such as BASIC. In addition, the results obtained using this method have been shown to be consistent with the values obtained by other techniques.



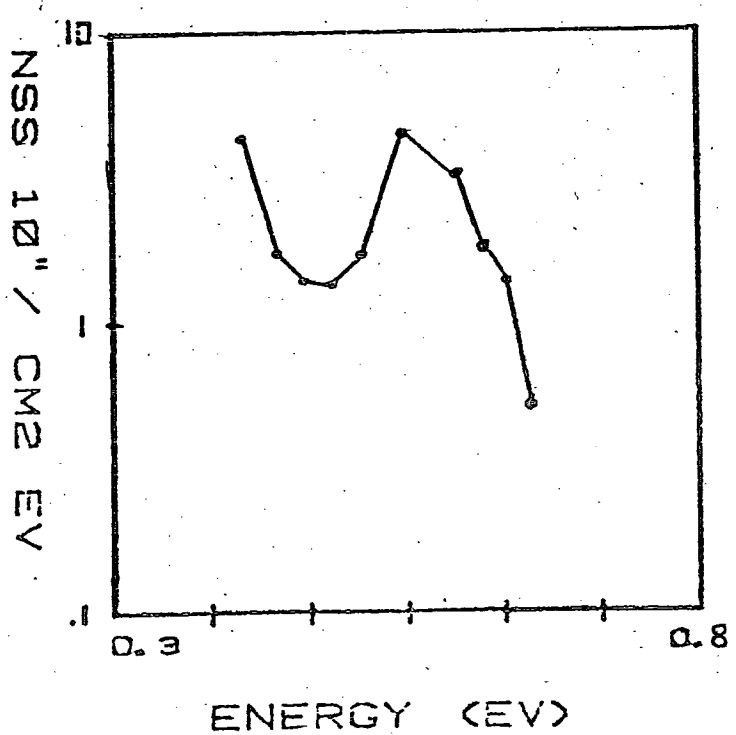


Figure 5.6 Quasi-static curves for gold-doped silicon sample.

It was decided to apply this technique to the analysis of gas effects on MIS devices, since it was felt that its speed would be useful in such an area of work. However, it was discovered that the calculated value of surface state density might be inaccurate if other elements in the equivalent circuit had been changed by the gas and incorrectly compensated for. A brief consideration of such effects is given at the start of the next chapter.

Chapter 6

Gas Effects on MOS Devices

6.1 Introduction

The physical properties of several areas of a metal-insulator-semiconductor structure device could be affected by the presence of a gas. This would normally result in a change in the measured electrical characteristics of the device. The possible influence of a gas is best analysed by dividing the MIS structure into its component parts. For example, in figure 6.1, the structure is split into three and the corresponding change in the capacitance-voltage curve is illustrated. If the gas influences the metal insulator region, then it is liable to change the work function of the device and introduce a lateral shift in the C-V curve. If it affects the insulator, possibly by changing the permittivity, the magnitude of the curve will be altered. This is due to the fact that the maximum height is directly related to the insulator capacitance which is dependent on its permittivity.

However, a varied number of interesting possibilities exist if the gas permeates through the insulator and influences the insulator-semiconductor interface. If surface states are introduced or removed, the resultant change is in such a form that the analysis techniques of Chapter 3 may be applied; but if the effect is to simply alter the occupancy of already present surface states, by changing the surface potential, then a lateral shift similar to that for the work function change case would be observed.

Any change in surface state density is best monitored through measurement of the parallel conductance of the device; but care must be taken in deriving this from the measured characteristics because a

Figure 6.1 Possible changes in the C-V characteristic of an MIS structure brought about by the effect of gas on different parts of that structure.

combination of gas effects might have occurred ie both the surface state density and the oxide capacitance could have been altered. If the oxide capacitance was then incorrectly compensated for, an imaginary surface state density change would be introduced.

The gas most extensively investigated was hydrogen as it has been shown to be a very important element in the silicon-silicon dioxide system (1,2). Most of our measurements were made on a hydrogen-sensitive structure that has been developed as a hydrogen sensor (3), but whose operation is not completely understood. We have also carried out measurements using other gases on MIS structures where the insulator is silicon dioxide; results with an alternative insulator are described in the next chapter.

6.2 Hydrogen Interactions on Palladium MOS Structures

6.21 Introduction

The palladium/hydrogen system has been the most extensively investigated metal/gas regime. Interest was originally centred on its physical properties, especially its ability to absorb and pass hydrogen; more recently, the catalytic decomposition of hydrogen by palladium has been examined. Lundstrom (3,4) and others (5,6) have utilised these properties in an MIS-type hydrogen sensor which has the following structure: palladium-silicon dioxide-silicon. There is a controversy as to the actual operational mechanism: are surface states at the insulator- semiconductor interface involved or is the influence of the hydrogen restricted to the palladium surface? Before discussing results using Pd MOS devices and a Pd Schottky barrier

7.51 The action of Moisture

Figure 7.12 shows the change in the capacitance-voltage characteristics that occurs on exposure to ammonia (similar results were obtained with hydrogen chloride): both the accumulation capacitance and the amount of hysteresis have been increased. The change in the former is due to an increase in the dielectric thickness, whilst that in the latter is due to an increased ion concentration in the film. Since the gases were derived by bubbling nitrogen through aqueous solution then these effects could possibly be accounted for by the presence of moisture in them. Indeed this was the case, for drying removed the effect and bubbling nitrogen through plain water produced similar results.

Further evidence that moisture was an important contaminant in Langmuir film devices was provided when graphite water-based top contacts were used, and not left to dry out for long enough. An anomalous step in the C-V characteristic in the accumulation region was obtained. This step in the C-V characteristic and the rate of accumulation conductance increase could be reduced by evacuation of the cryostat, which presumably extracted the moisture trapped underneath the top contact. The decrease in the magnitude of the accumulation conductance also reduced the magnitude of the surface state peak. Hence the increase in the conductance peak height that was found on some gaseous exposures (see figure 7.13) does not correspond to an alteration in the surface state density, but rather is due to a change in the acccumulation conductance. This was confirmed by the fact that the forward bias dc conductivity changed at the same time. Since this is related to the ac conductance, then it

device, a brief review of the general properties of palladium is given. This will demonstrate the extent of the effect of hydrogen and the important role played by the surface of the palladium.

6.22 General Physical Properties

Thomas Graham, as early as 1866, noticed not only the permeability of palladium to hydrogen, but also that large volumes of it were absorbed by, or as Graham termed it "occluded" by, the specimen when it was allowed to cool to room temperature in an atmosphere of the gas. The diffusion rate obviously increases with temperature, but at low temperatures (below approximately 500K), it was found that the rate limiting step was not the hydrogen transport, but rather reactions at the palladium surface, thus showing the latter's importance. Such temperature variation also facilitated analysis of the thermodynamic nature of palladium, particularly its change of phase under different conditions. In addition, the adsorption of the hydrogen was discovered to affect the physical properties (eg lattice constant, tensile strength) and electrical characteristics (eg resistance) of palladium. The most striking change is the alteration of the shape of a piece of palladium when continuously temperature-cycled: a flat rectangular specimen is seen to constrict and deform an enormous amount, probably due to phase changes within the metal.

Recently, the chemical interaction of hydrogen with palladium has been examined, using electron spectroscopy in particular (7). Demuth (8), for example, came to the conclusion that the bonding

process of hydrogen on palladium mainly involved 3d binding electrons, whereas when hydrogen reacted with nickel, 4s electrons played a part. This difference manifests itself in the sticking coefficients: 0.9 for hydrogen on palladium as compared with 0.25 for nickel (9).

6.23 Palladium MOS Device Properties

The flat band capacitance of a Pd MOS device is altered in the presence of hydrogen; a graph of concentration versus change is given in figure 6.2 to demonstrate this. The change corresponds to a lateral shift of the whole capacitance-voltage curve. Lundstrom (10) maintains that this is due to a simple work function change of the top contact (see figure 6.1). However, Keramati & Zemel (11) have stated that surface state change at the silicon-silicon dioxide interface is involved. Our equipment, which measures the parallel conductance of the device, should be able to resolve whether any surface state density change has occurred on the interaction of hydrogen with a Pd MOS device.

6.231 Work Function Change

In Lundstrom's model, hydrogen molecules dissociate into atoms on the palladium surface and some dissolve in the metal. A fraction of these are then adsorbed at the Pd-SiO_2 interface where they sit with their electrons slightly displaced towards the palladium, thus acting as dipoles. The resultant charge layer produces a voltage drop that must be added to the external applied voltage, which then gives rise

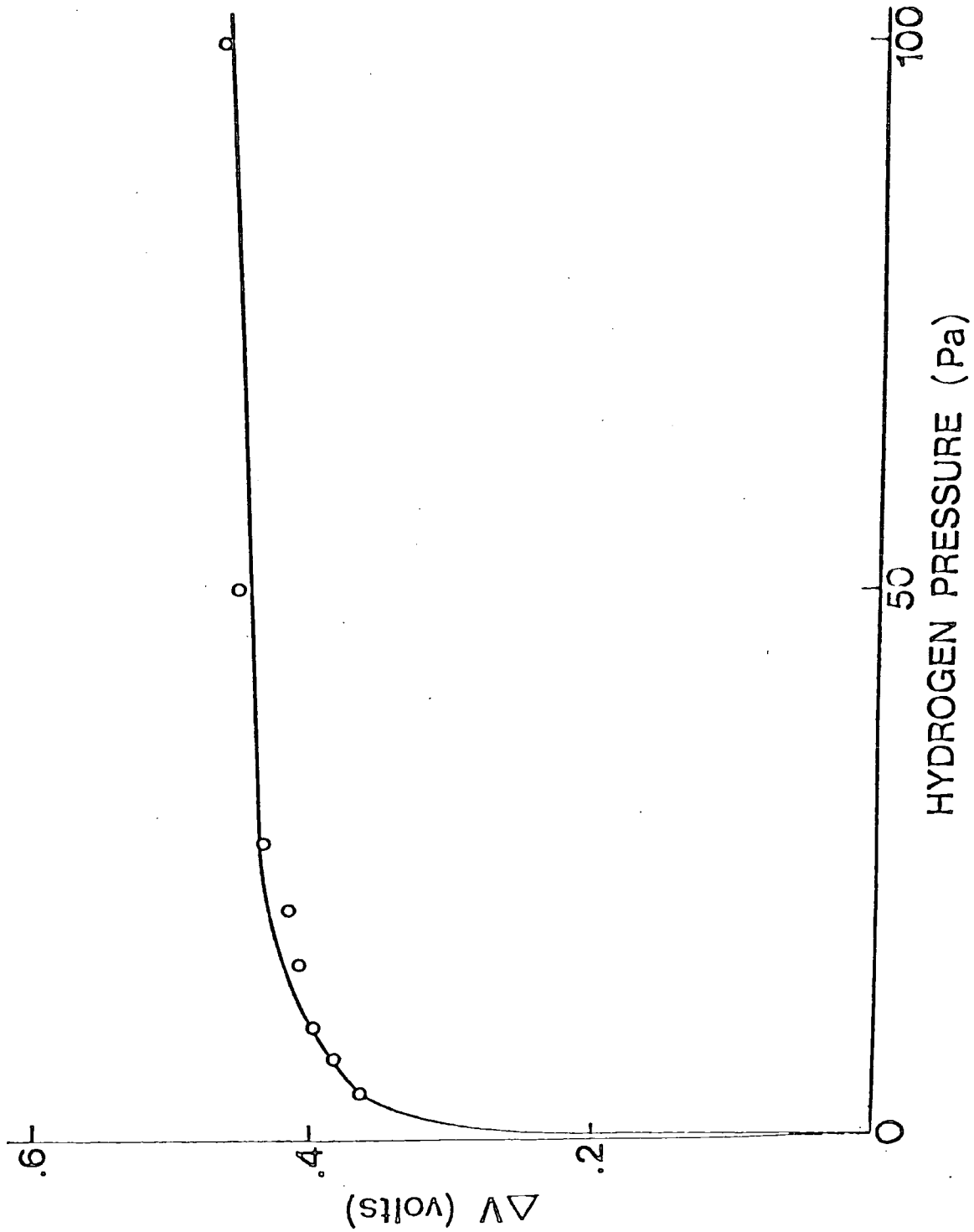


Figure 6.2 Flat band voltage shift with respect to hydrogen pressure.

to a leftward lateral shift of the C-V characteristics for both p and n-type silicon (see figure 6.3). This action can be more fully understood by the following microscopic consideration. Zero bias ideally corresponds to the flat band situation for both semiconductor types; when such dipoles are introduced into a p-type device, they will repel holes from the surface, thus driving the device into depletion. The capacitance at zero volts must then decrease, and everywhere else on the C-V curve must change accordingly, thus effectively introducing a shift of the curve to the left. Conversely, for n-type, the dipole attracts negative charge to the surface, giving rise to accumulation at zero volts ie a capacitance rise which, when extended over the whole curve, again corresponds to a leftward shift.

Steele and McIver (5) suggested that absorption rather than adsorption took place - for it had been shown (12) in vacuum that the latter gave a voltage shift in the wrong direction. They suggested an alternative explanation based on the formation of bulk palladium hydride which would give the correct flat band voltage shift. However, Lundstrom subsequently (13) explained the anomaly by pointing out that the presence of air and the fact that the dipole layer was at the internal interface produced an entirely different situation. He further proved that the reactions involved were predominantly surface ones using Langmuir adsorption isotherm plots.

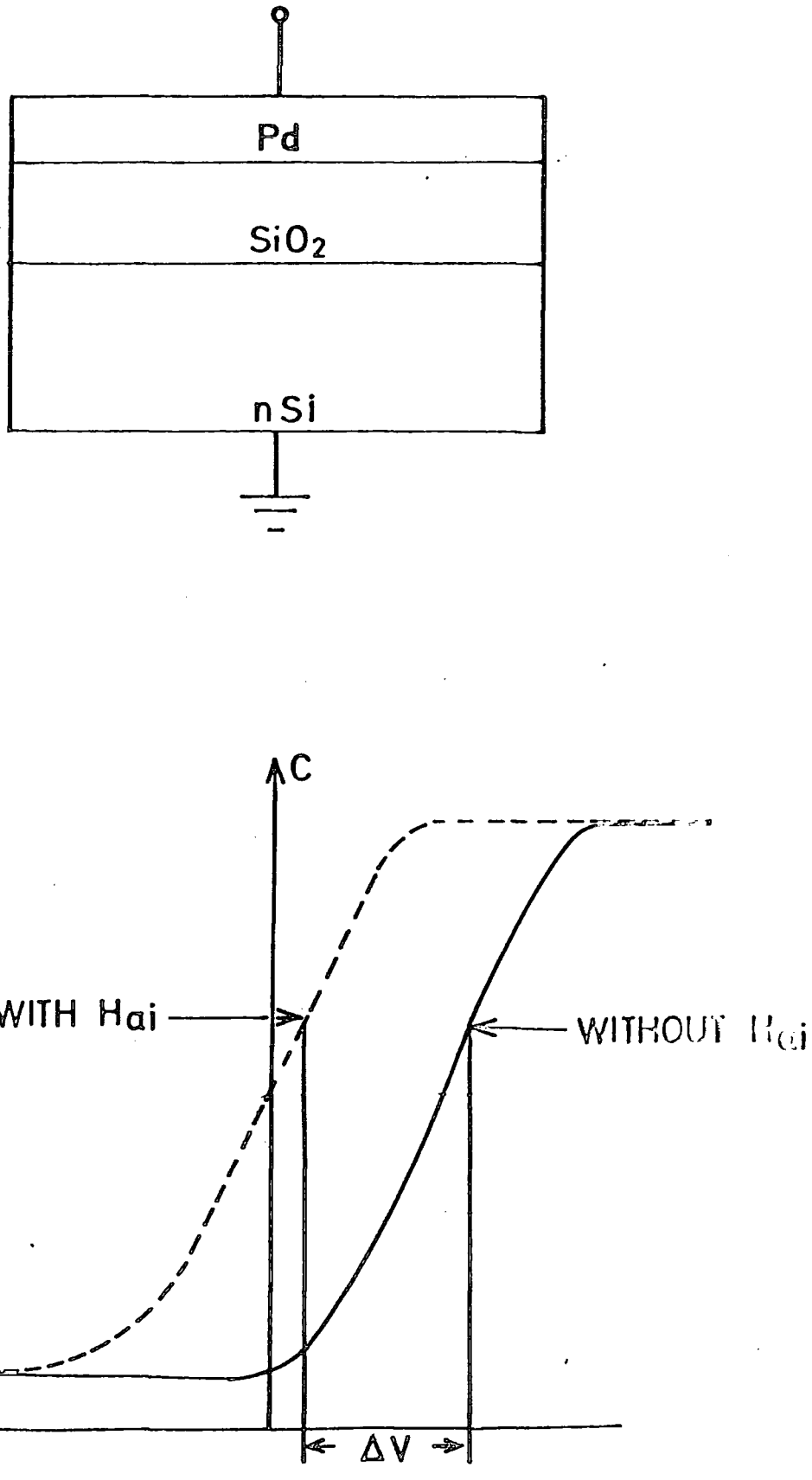


Figure 6.3 A Pd MOS device and its change of C-V characteristic under the influence of hydrogen.

6.232 Surface State Change

Contrary to Lundstrom, Keramati and Zemel maintain that surface states are involved. They have made measurements using thin tunnelling oxides and, by comparing their results with a theoretical model (14), they propose that two donor levels at 0.4 and 0.6 eV below the conduction band are introduced by the action of hydrogen. This approach is unsatisfactory in two respects. First of all, it is incompatible with the surface state reduction of silicon-silicon dioxide structures brought about by low temperature annealing in the presence of hydrogen (see section 2.2). Secondly, it cannot be used to explain the results of Lundstrom et al on thicker oxides, as will be demonstrated below.

There are several different ways that the surface state distribution could change and induce the experimentally-observed lateral shift in the high frequency C-V curve. The introduction of donor states, as shown in figure 3.1e, or the removal of acceptor states which would give the opposite effect (see figure 3.1h) are both possible examples. However, closer inspection of these curves reveals that if the states are scanned by the Fermi level as the bias is altered, their occupancy would change and the lateral shift of the C-V curve would acquire some form. This is, after all, the basis of the Terman technique. Hence the suggested levels of 0.4 and 0.6 eV, should have some effect, if not noticeably on the high frequency C-V curve, then surely on the parallel conductance curves which are more sensitive to surface state change.

6.3 Experimental Difficulties

Before the presentation of the results of the interaction of hydrogen with our devices, the problems that were encountered merit a brief discussion. Hydrogen is, by nature, a dangerous gas and measurements were carried out with due regard of its "lighter than air" nature. In order to prevent it accumulating in the laboratory, the cryostat was pumped out at the end of each experiment, or it was used in an enclosed environment such as a fume cupboard or glove box from where the hydrogen could be vented outside.

6.31 Top Contact area change

The adhesion of noble metals, like gold and palladium, on silicon dioxide is very poor. Gold can be easily scratched by probing and so it is often used in conjunction with another more adhesive metal in a double top contact configuration. Palladium also suffers in this respect, but our greatest difficulty was that the top contact of the palladium actually lifted off in the presence of hydrogen. This resulted in a decrease in the measured value of C_{ox} on some MOS devices and an increase in slope of the $1/C^2$ versus voltage curve for a Schottky barrier device that was investigated. Initially, a phase change similar to that mentioned in section 6.2 which caused constriction of a laminar sample, was thought to be responsible. However, lift off of the metal could be actually seen if a sample was viewed under a microscope as it was being exposed to hydrogen. Visually the electrode appeared to have a matt, sometimes granular, appearance. Not all palladium top contacts suffered from this problem,

not even all electrodes on the same sample. It seemed to be a particular problem on the dry oxides, but some of the wet oxides made in the University also seemed to be slightly prone. With the former, an initial hydrogen exposure of a sample could be used to discern which electrodes were worst affected - they would be the ones which possessed the matt appearance previously mentioned. Even so, those top contacts that were considered good from this test often degraded with time. Sometimes the oxide capacitance change could be compensated for by the microcomputer and a new parallel conductance value calculated, but in other cases when the accumulation conductance value altered drastically, this was not possible. Svensson (15) has suggested a technique to improve adhesion that involves heating the sample for thirty minutes in air at 473K. We tried this but found it to be unsuccessful. We discovered that evaporating onto a liquid nitrogen cooled substrate sometimes gave improved adhesion. Results using this method are given in section 6.41 for a specially prepared Schottky barrier structure.

6.32 Variation in Series Resistance

The value of the accumulation conductance which determines the series resistance of the sample was also found to change in conjunction with the oxide capacitance on hydrogen exposure. Small differences could be compensated for, but drastic changes would not result in sensible values of parallel conductance. Smaller changes in the measured conductance such as the appearance of an anomalous step on the normally flat accumulation region of the response also occurred. This effect, though, is difficult to explain; possibly the

change in resistance of the palladium mentioned in section 6.22 is to blame.

6.33 Bias Stress Effects

If a sample is biased at an elevated temperature for a period of time then a lateral shift in the characteristics will be observed on returning the sample to room temperature. This is known as bias temperature stressing and has already been discussed in section 2.43. Such stressing can occur at room temperature where it might be confused with a gas effect, if the gas is admitted with a bias applied to the sample. The ionic contamination of a sample indicated by the presence of clockwise hysteresis on p-type structures is not to be unexpected considering the method of palladium deposition. A tungsten filament which is a well-known source of sodium ions was used. Even pre-heating of the filament and masking off of the initial evaporated material did not stop sodium contamination. An electron beam evaporator would have been a far better method of deposition, but this was not available to us. The simple solution to the above problem is to admit gas at zero bias.

6.4 Experimental Results

6.41 Palladium-Silicon Schottky Barrier Results

Palladium was evaporated onto both n and p-type 3-10 ohm cm bulk silicon after the latter had been etched with buffered hydrofluoric acid (1 part HF, 4 parts ammonium fluoride). Since palladium has a

large work function (5.12 eV), it is expected to give contacts of a different nature to the two silicon types (see section 2.3): for p-type an Ohmic contact, for n-type a Schottky barrier. This was indeed found to be the case.

Two sets of measurements were made on a single n-type sample. In the first set, area change of the top electrodes was found to be a problem; this was not the case in the second set of measurements when the palladium was deposited at liquid nitrogen temperature. An area change problem for the first sample was seen to be present through the matt appearance of the electrode and the change of gradient of the inverse capacitance squared plot that occurred on recovery of the device. Figure 6.4 illustrates the change from the initial standard Schottky barrier type characteristic (curve 1) to a steep vertical rise (curve 2) curve on exposure to hydrogen, followed by recovery through curves with various $1/C^2$ versus voltage gradients (eg curve 3). This reaction and subsequent recovery was rapid and reproducible. There seems to have been a work function change combined with an area change; the fact that the latter causes a change in the gradient of the inverse capacitance squared versus voltage plot is demonstrated in figure 6.5 where a $1/C^2$ plot is shown for two different capacitor areas. One of these has effectively twice the area of the other, and is obtained practically by connecting two identical capacitors in parallel.

In the second set of measurements, no such area change occurred on exposure to hydrogen. The curve simply shifted to the left and the $1/C^2$ intercept value decreased. The results are shown in figure 6.6. In this case, the sample took much longer to return to its

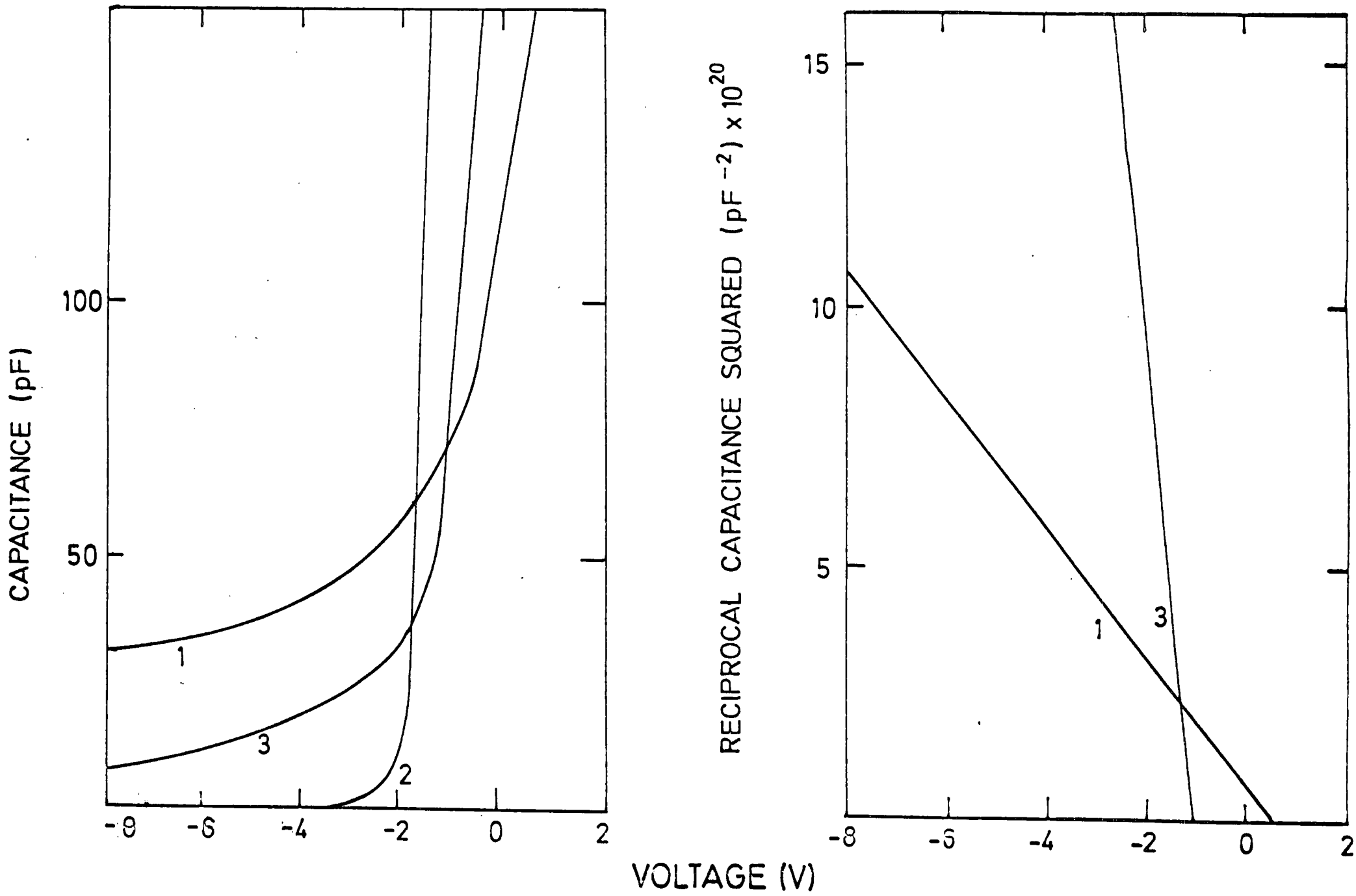


Figure 6.4 Capacitance characteristics for Schottky barrier device (1)before (2) during and (3) after exposure to hydrogen.

Figure 6.5 Capacitance curves for Schottky barrier device with two different areas.

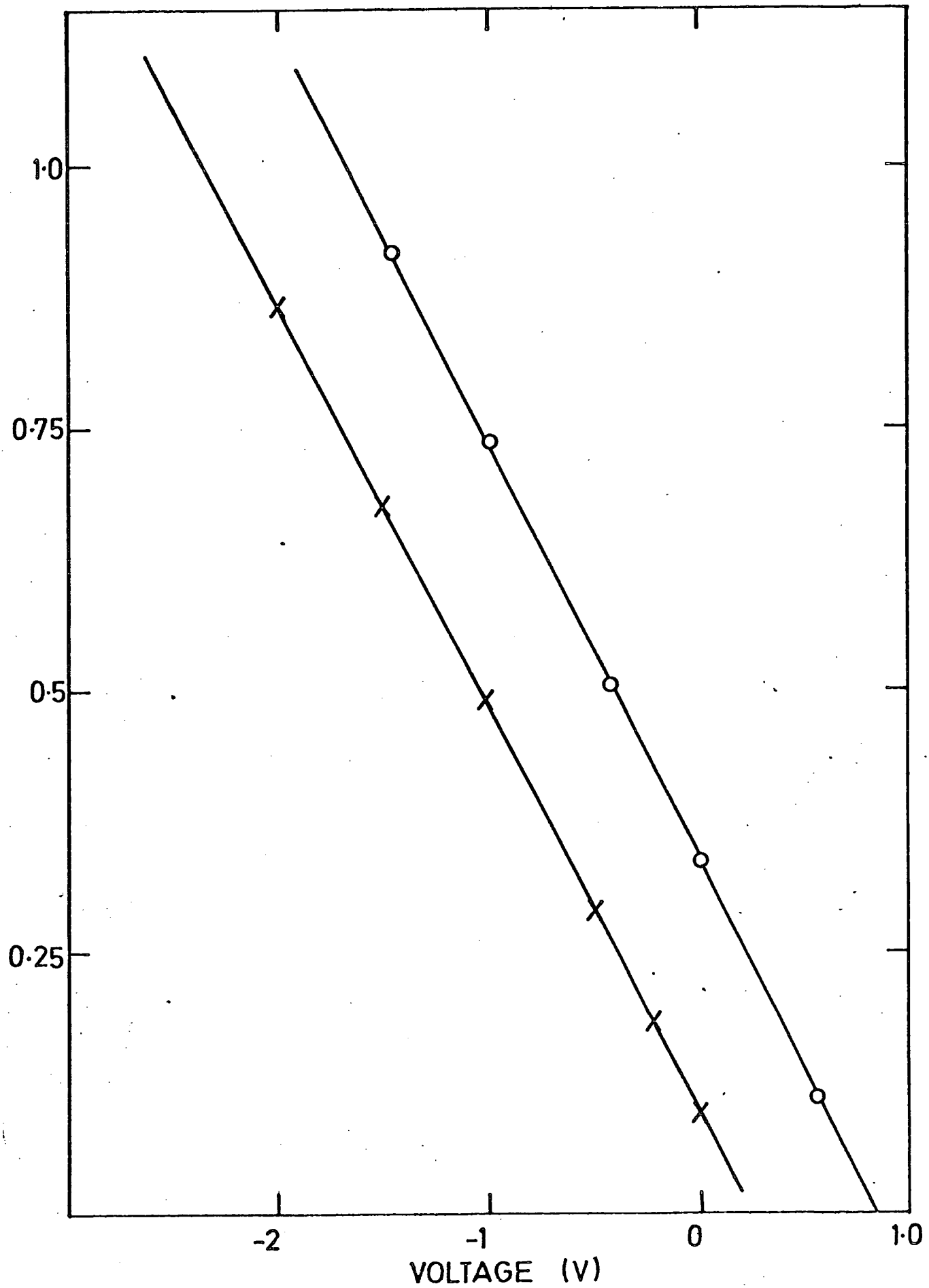


Figure 6.6 Lateral shift in capacitance characteristics for Schottky barrier diode corresponding to before (o) and after (x) exposure to hydrogen.

initial state.

6.42 MOS Device Results

(I) Wet oxide samples.

The oxides grown in the department (on epitaxial and bulk p-type silicon) and that on the Philips sample (on epitaxial n-type silicon) were classified as wet oxides, since water vapour was present in the ambient during their formation. The presence of water leads to further oxidation mechanisms in addition to the simple reaction of oxygen with silicon, which is the basis of dry oxidation. These are:

$$H_2O + Si\text{-}Si - Si\text{-}O\text{-}Si + H_2 \qquad (6.41)$$

$$H_2O + Si\text{-}O\text{-}Si - 2\ (Si\text{-}OH) \qquad (6.42)$$

and

$$2\ (Si\text{-}OH) + Si\text{-}Si - 2\ (Si\text{-}O\text{-}Si) + H_2 \qquad (6.43)$$

The hydrogen formed may diffuse away or form defects by the following reaction:

$$H_2 + Si\text{-}O\text{-}Si - Si\text{-}OH + H\text{-}Si \qquad (6.44)$$

Further, the silanol group (OH) and hydrogen will saturate dangling bonds at the surface leading to the observed lower surface state density of wet oxides as compared to dry ones (16). Thus, the surface state density value for a device cannot be regarded as a measure of the perfection at the interface since it depends only upon the number of active defects present. Defects can be activated by various

treatments such as bias stress and irradiation which can lead to degradation of device performance. For example, illumination with UV light of energy 3 eV increases the surface state density, probably through the breaking of the silicon-hydrogen bond whose energy is of the same order (17).

When hydrogen was exposed to palladium-covered wet grown oxide samples, there was a simple lateral shift both in the capacitance-voltage and the parallel conductance-voltage characteristics for all frequencies, implying that no detectable surface state change was taking place. A typical shift in the parallel conductance characteristic is given in figure 6.7. The response time was fairly quick, a matter of seconds, but recovery depended on the oxide thickness and for the thickest oxide (100 nm) was several hours, sometimes as long as eight. The value of the voltage shift was sample-dependent but was generally less than one volt. The adhesion of the top contact was also sample-dependent. The samples with oxides grown in the department were very susceptible to such top contact area change whereas the Philips structure gave no such difficulties.

(2) Dry Oxide Structures

The absence of the above silanol-based oxidation mechanisms in the preparation of "dry" oxides produces both a predictable easily-controlled growth rate and a large surface state density - the latter being presumably due to the presence of a greater number of

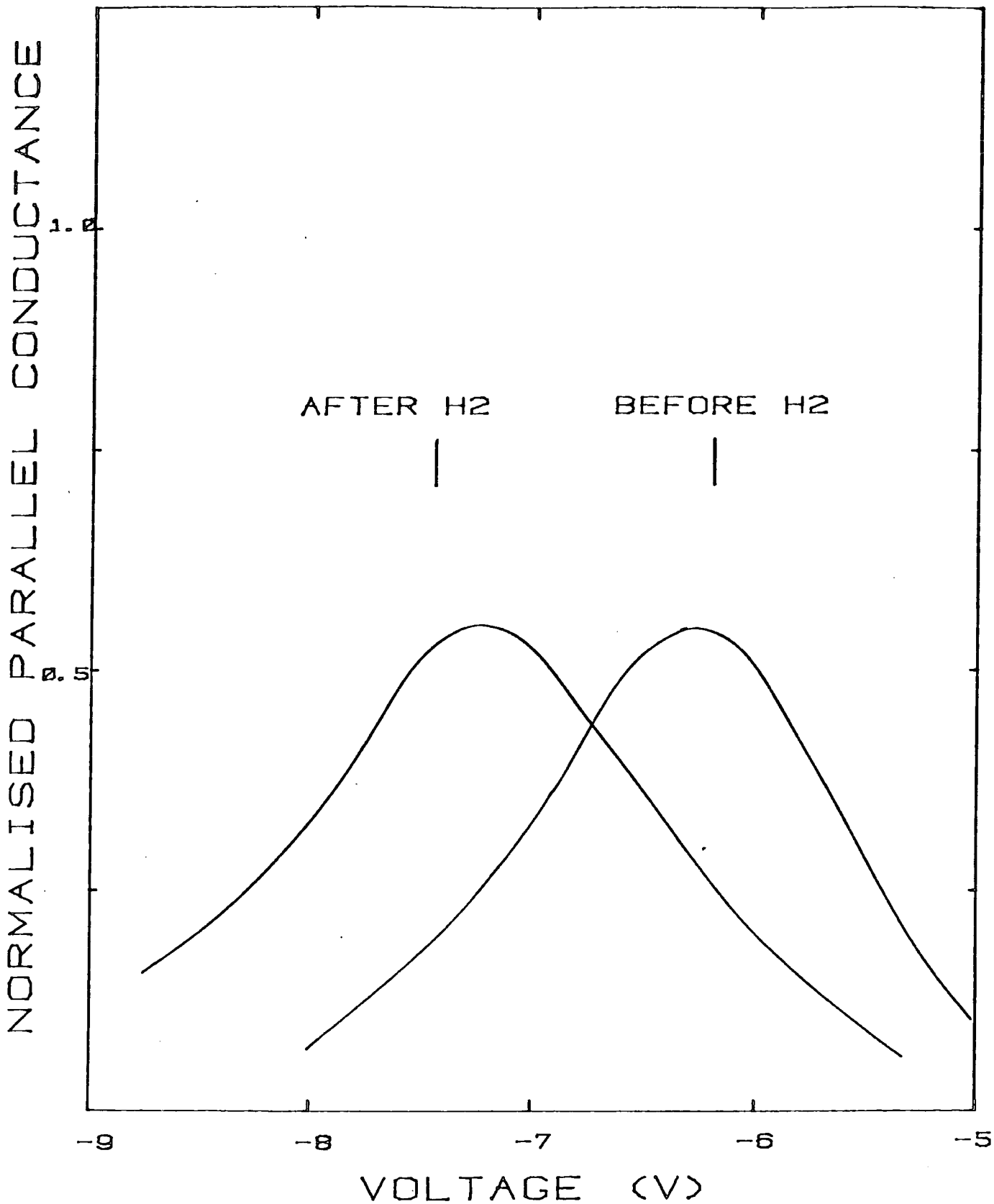


Figure 6.7 Parallel conductance plots for Pd MOS device, before and after exposure to hydrogen.

dangling bonds. Hence, the effect of atomic hydrogen might be expected to be more pronounced on such oxides. This was not found to be the case, for a simple leftward shift was measured not only on thick oxides, but also on thinner tunnelling ones (5nm) that approached the dimensions used by Keramati & Zemel. It was not possible to calculate the parallel conductance of the tunnelling oxide structures because of the associated steep rise in the accumulation conductance that prevented calculation of the series resistance value. The above authors (14) circumvented this particular problem by fitting a theoretical model to their experimental results which in fact showed a definite characteristic change on exposure to hydrogen. Since the high frequency curves in our results simply shifted to the left, it may be assumed that no detectable surface state density change has occurred.

6.5 Summary of Hydrogen Work

6.51 Discussion of Results

The results of the interaction of hydrogen with palladium are summarised in Table 6.1. It can be seen that no measurable surface state density change has been observed. This was confirmed by quasi-static measurements where there was also simply a lateral shift in the characteristic. A typical curve is shown in figure 6.8. This effect was sometimes obscured by the appearance of a peak in the quasi-static characteristic such as the one shown in figure 6.9. The origin of this peak may be surface state-related (this will be discussed in the next section).

TABLE 6.1

Oxide Thickness (nm)	Dopant Type	Lateral Shift (V)	$G_p/$ (max) Change
100	p	0.6	0
100	n	1.0	0
60	p	0.5	0
15	p	0.7	0
5	n	0.3	*
5	p	0.6	*

Table 6.1 Summary of the change in parallel conductance characteristics on exposure of an MIS device to hydrogen. * refers to the fact that it was not possible to calculate the parallel conductance of tunnelling structures. However, in this case as with the rest of the structures, a simple lateral shift of the measured characteristics was observed.

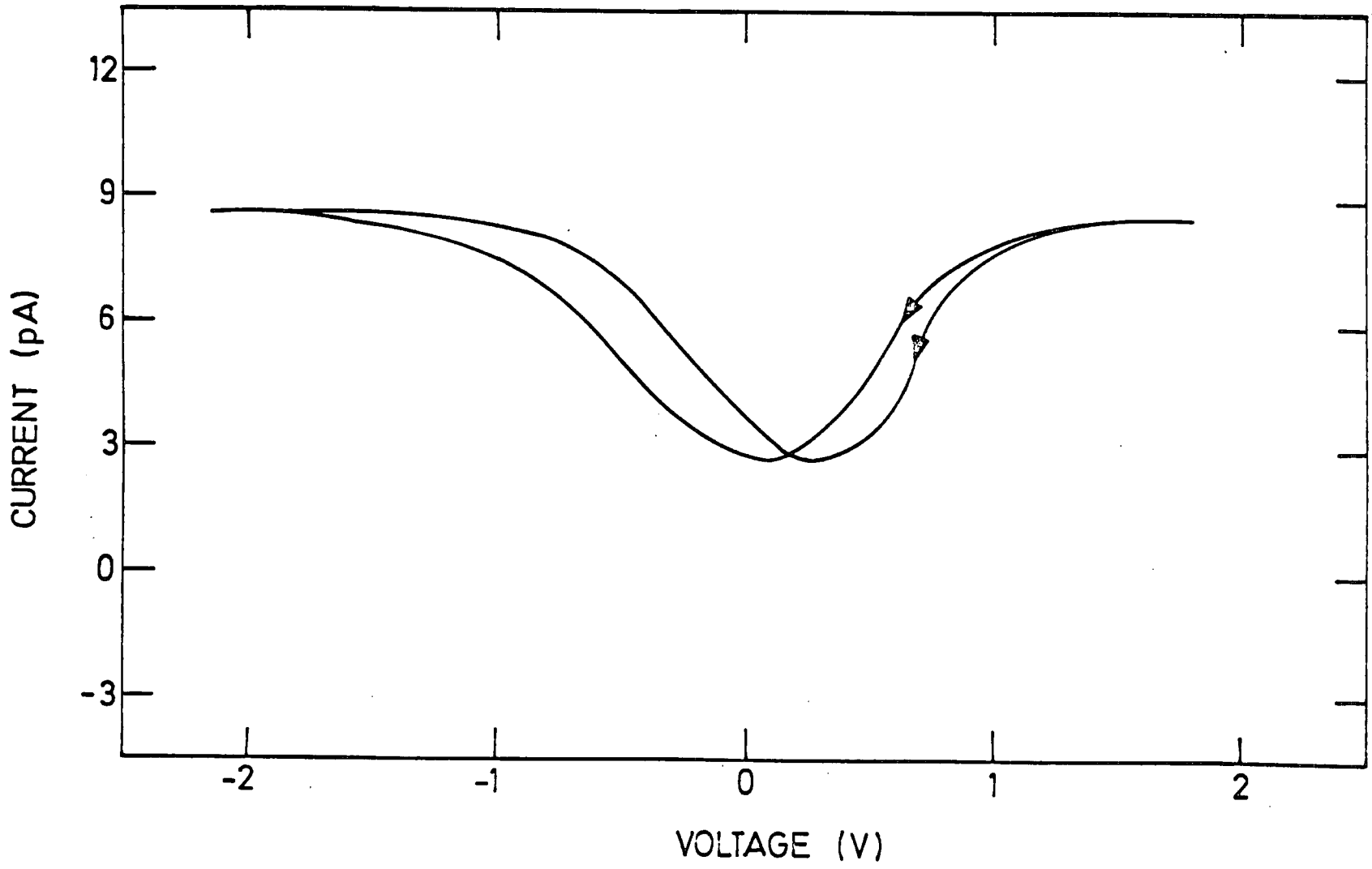


Figure 6.8 Effect of hydrogen on quasi-static curves of Pd MOS device.
(a) Before (b) after hydrogen.

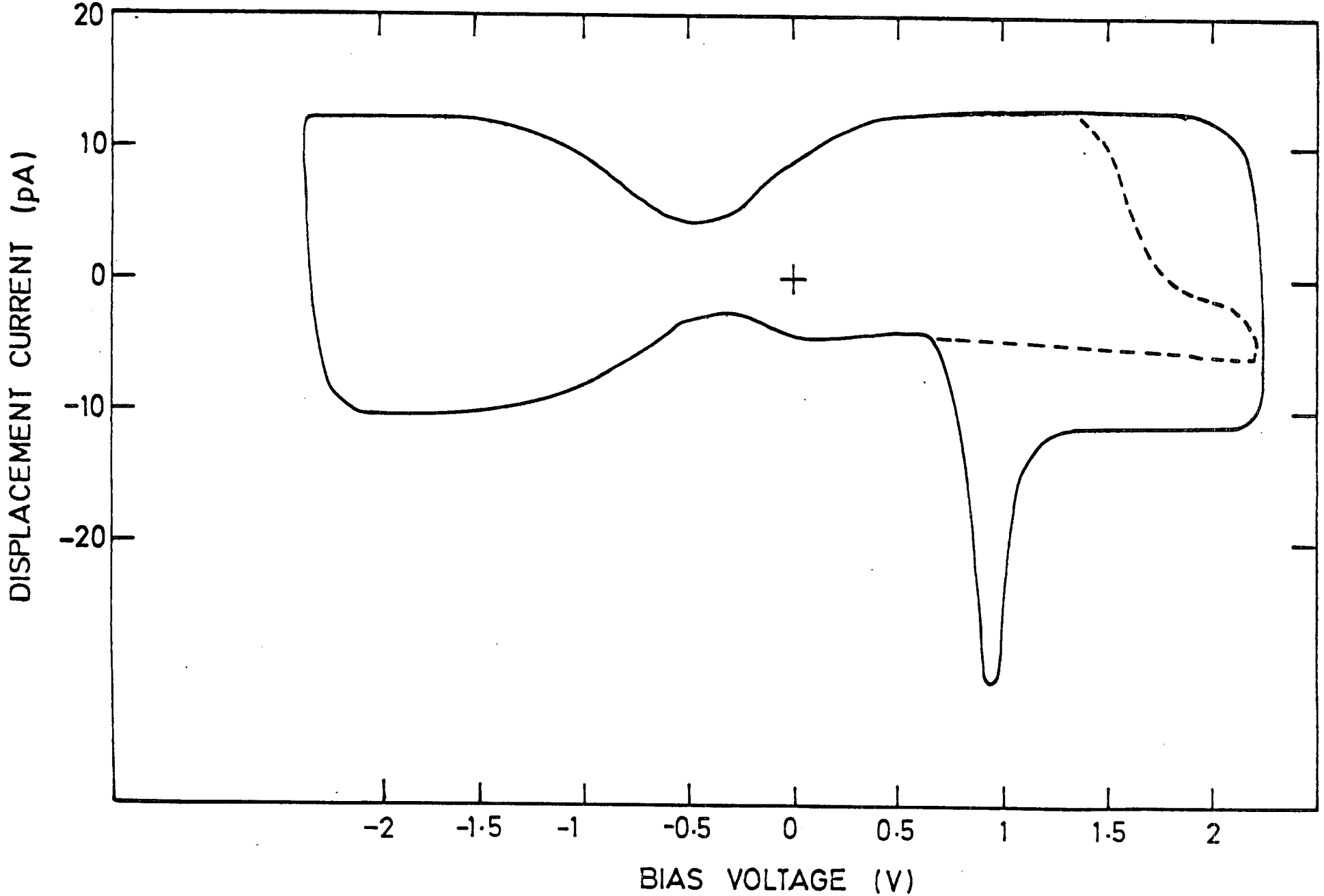


Figure 6.9 Quasi-static curve for Pd MOS device after exposure to hydrogen. Dashed curve for after removal of hydrogen.

6.52 A Hydrogen-Induced Surface State ?

The above conclusion that no surface states are introduced by gases on MOS structures may well satisfy all the quantitative measurements made, but some results imply that hydrogen, which does permeate the oxide as shown by the long recovery times of some of the devices, might introduce surface states. This would hardly be surprising considering its concentration at the interface (1). It is proposed that a donor-type surface state is introduced, which is so close to the band edge that it is above the Fermi level and therefore always positively ionized. Such a positive charge would account for some of the measured lateral shift, for the external inversion layer effects described by Zaininger & Warfield (18) who noticed the onset of inversion at lower frequencies in the presence of hydrogen. They proposed that the hydrogen induced positively-charged surface states around the top contact that gave rise to external inversion layer effects similar to those described in section 2.6.

The lack of direct evidence for surface states beneath the top contact is due to the limited surface potential range of the admittance measurement technique as pointed out by Lopez (19). Even if the surface state level was within the range, its effect could be obscured owing to the position on the characteristics where it would occur. On n-type silicon, it would be close to accumulation where the capacitance of the semiconductor is large and overwhelms any surface state capacitance change as well as dominating the measured conductance response. The latter can be appreciated from inspection of equation 6.5 which is a rewritten equivalent circuit expression of equation 3.13 with the series resistance assumed to be zero. It can

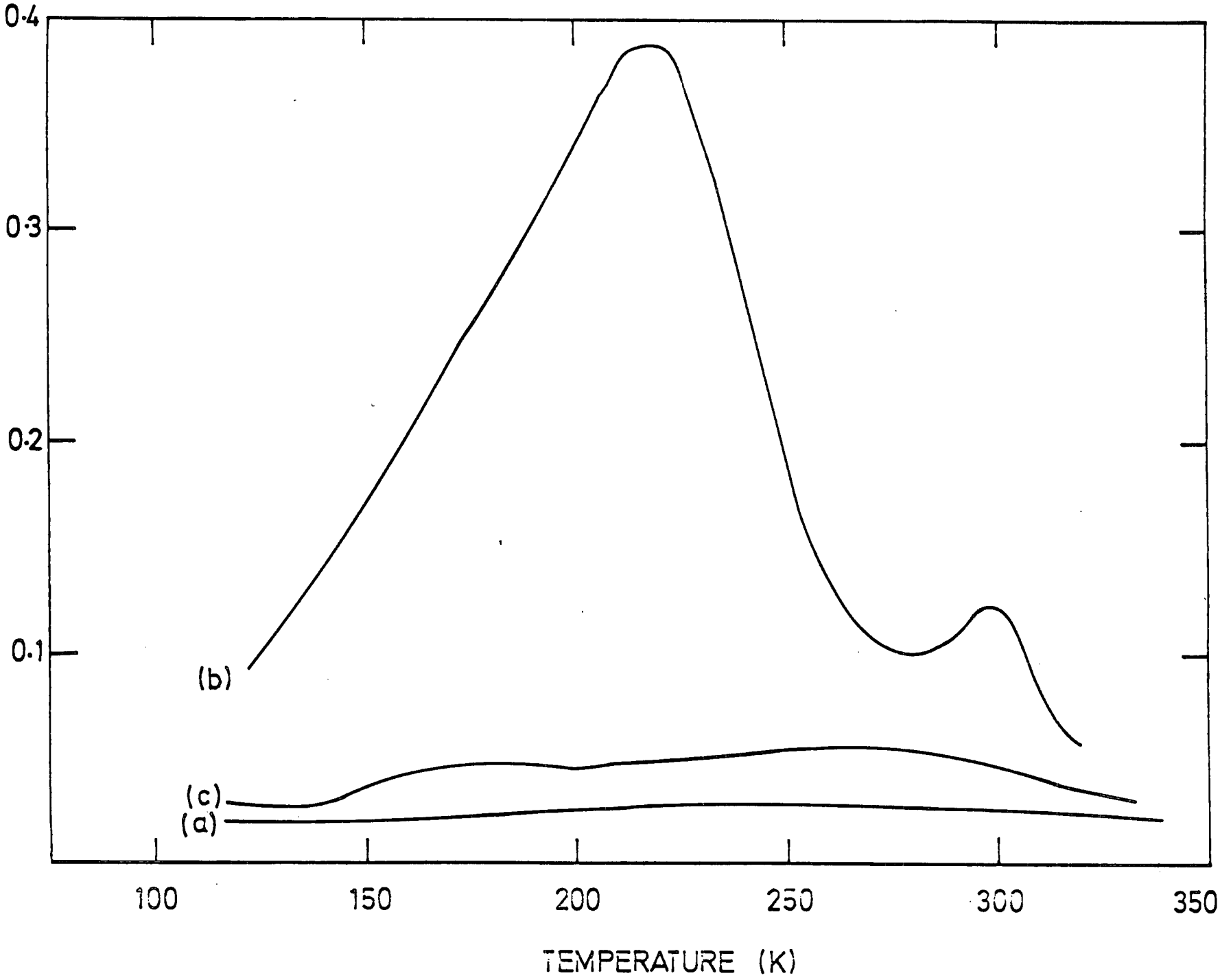


Figure 6.11 DLTS curves for Pd Schottky barrier device for (a) Before, (b) during and (c) after exposure to hydrogen.

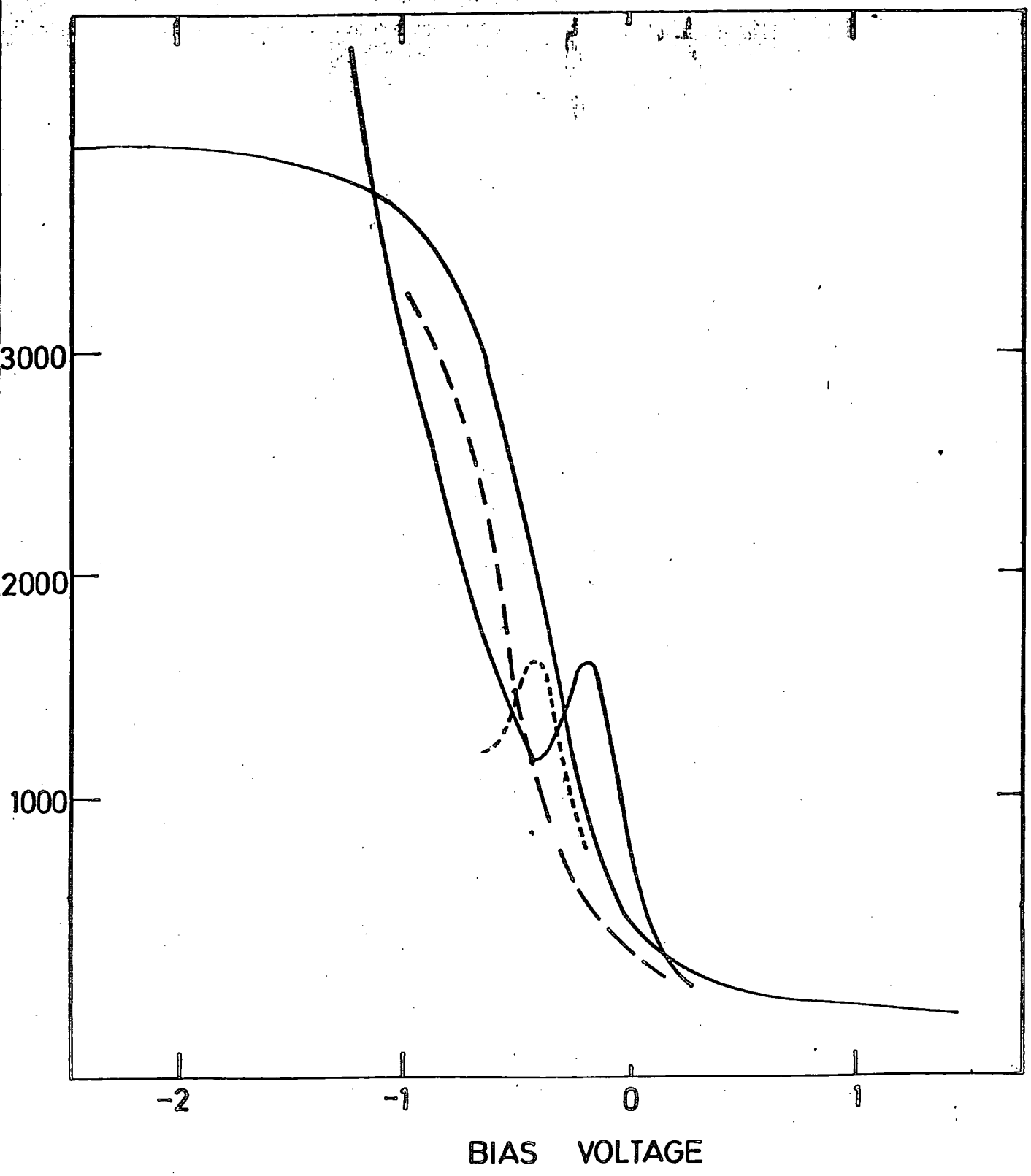


Figure 6.10 Effect of hydrazine on Pd tunnelling MOS device admittance characteristics.

be seen that if the semiconductor surface capacitance C_p is large, then the measured conductance G_m is necessarily small.

$$\frac{G_m/\omega}{C_m} = \frac{G_p/\omega}{(G_p/\omega)^2 + (C_p + C_{ox})^2} \cdot C_{ox} \qquad (6.5)$$

With p-type samples the influence of such a state would occur in inversion, where usually it would be swamped by the conductance contribution of the external inversion layer. Secondary conductance peaks that did occur just in inversion were checked to ensure that they were due to an external inversion layer. This was carried out by monitoring their bias position as the frequency was increased; as predicted by Kar & Dahlke (20) for such a condition, it was found to move into the inversion region.

Further evidence for the presence of a hydrogen-induced surface state was obtained at a late stage in the work from some DLTS measurements that were performed on the Schottky barrier structure characterized in section 6.41. The DLTS plot in figure 6.11 shows the development of structure under hydrogen exposure. The large peak that is introduced corresponds to the presence of a surface state level of density $3 \times 10^{12} eV^{-1} cm^{-2}$ at 0.1 eV below the conduction band. This is possibly hydrogen-induced, although several other explanations are feasible, in the light of the calculated capture cross section value of $10^{19} cm^{-2}$. According to DiMaria (21) a sodium ion could be responsible - or even a dipole, which would confirm Lundstrom's model.

The discrepancy with Keramati & Zemel as to the location of the peak can be rectified by pointing to a possible flaw in the assumed values of their constants. Perhaps the electron affinity value of 4.05 eV is incorrect for the situation where atomic hydrogen is present: a lower value of 3.7 eV, as suggested by Kasprak & Gaind (22), might be more likely. This would possibly alter the predicted location of their surface state to nearer the conduction band. Also, when using theoretical modelling techniques, several surface state distributions can usually be made to fit the data. Possibly a trap more in line with the ideas suggested above might fit the data better.

Unfortunately, it is practically impossible to differentiate between the action of the hydrogen states proposed above and the effect of sodium ions. It is quite possible to explain the above effects equally plausibly by the presence of sodium that is ionized or inactive and then activated. For example, the peak that occurs in the quasi-static measurements may be attributed to the action of sodium ions. Again, the drift in the steady state characteristics of Lundstrom's devices (10) may well be due to the drift on activated sodium and not, as Keramati suggests, due to the influence of surface states.

6.6 Other Gas Effects

Several gases such as carbon monoxide, hydrazine and ammonia were exposed not only to palladium covered MOS devices but also to other MOS structures. Apart from parasitic effects, no surface state related change was observed. In the case of carbon monoxide on palladium MOS, similar effects to those obtained with hydrogen have been reported but we found none. The reason for this is probably the inability of the carbon monoxide to diffuse through the top contact. According to a recent paper (24), the latter has to be made porous by some special procedure which needs further investigation. When hydrazine was exposed to the same structure, an effect was observed. The same lateral shift that was found with hydrogen occurred. In figure 6.10, the effects on the measured characteristics of a 5 nm Plessey bulk silicon sample are shown. The rising conductance in the accumulation region is due to the presence of a tunnelling current. This makes surface state calculation very difficult. It can be seen that no surface state change has occurred; this implies that the hydrazine has not penetrated the oxide, since one might expect a known silicon etchant to cause some measurable change at the interface.

The lack of effect on the interface of the ambient can probably be attributed to the high density of silicon dioxide which prevents the permeation of gases. It was decided to use an alternative insulator with a more open structure: the results of this investigation are described in the next chapter.

Chapter 7

Gas Effects on Langmuir Film Devices

7.1 Introduction

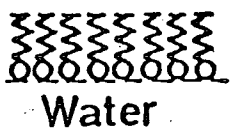
Until recently, there has been little interest in the development of an alternative insulator to silicon's natural oxide for MOS devices, owing to its almost ideal properties. The newest semiconductor materials (InP,GaAs), which promise higher logic speeds, have no equivalent insulator and, at present, much effort is being expended in the search for a suitable one (1). Langmuir "built-up" organic multilayers, whose properties are attracting an increasing degree of interest (2), form one such possibility. These thin films consist of a series of monolayers of a suitable organic material, with each monolayer being deposited on the previous one until the required thickness is reached. Provided certain conditions are carefully controlled, a film of great perfection can be obtained whose electrical properties may be extremely useful. The process is carried out at room temperature and hence leads to little disruption of the semiconductor surface, which might be an important consideration in the case of binary semiconductors where one of the components is volatile. After a description of the manufacture of Langmuir films, results will be discussed of their utilization as insulators within an MIS device and the effect of gases therein.

7.2 Preparation of Langmuir Films

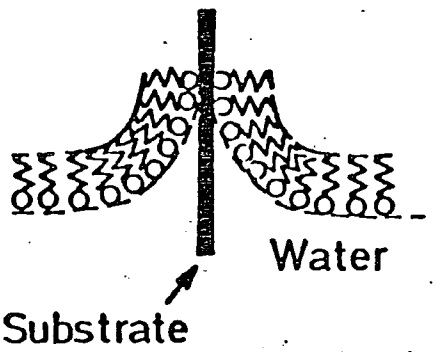
Langmuir films are formed by depositing a small quantity of a solution of a suitable material on the surface of previously purified water, waiting for the solvent to evaporate and then compressing the mono-molecular layer so produced until it forms a quasi-solid one molecule thick. In order to remove the film from the water, a suitable substrate is dipped through the quasi-solid and then removed. One monolayer is transferred to the substrate during this process, provided certain stringent requirements have been met. If the substrate is repeatedly dipped through the water, a multilayer of organic substance is built up, with a high degree of structural perfection. The process by which the multilayers are produced is illustrated in figure 7.1. Using this method, Langmuir films may be built up from an initial thickness of approximately 1.2 nm to depths in excess of one millimetre. The method is attractively simple in principle, but meticulous attention to experimental detail is essential in order to obtain deposited layers that are well-ordered and structurally stable. Furthermore, only a limited range of organic materials can be formed into Langmuir film multilayers. Both these points are discussed in the following sections.

7.21 Suitable Materials for Langmuir Films

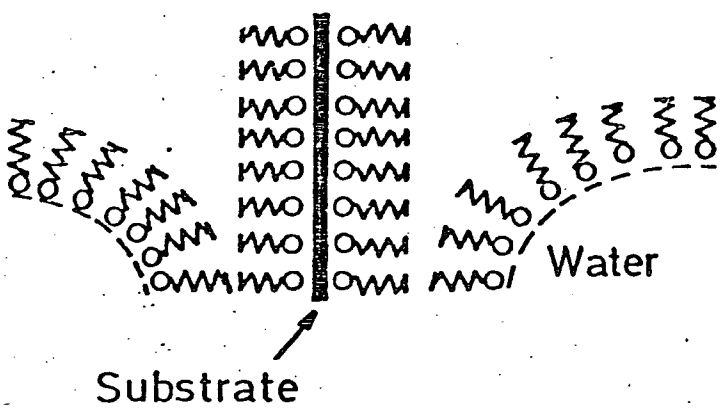
In general, molecules to be deposited using the Langmuir technique must possess both a hydrophobic and a hydrophilic component (3). Furthermore, to obtain multilayers as opposed to monolayers, the hydrophilic group must normally be quite strong. An aliphatic side-chain is normally used as the hydrophobic part of the molecule.



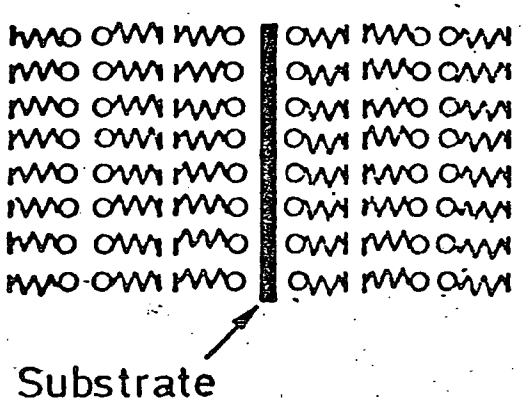
(a) Monolayer on the surface of the water.



(b) First layer on withdrawal.



(c) Second layer (2nd Insertion)



(d) Slide with three layers (after 2nd Removal)

Figure 7.1 Schematic diagram of the deposition of monolayers onto a solid surface.

In order to avoid excessive water-solubility, the aliphatic component must also be quite large. Accordingly, suitable molecules generally contain one or more long (approximately 18 carbon) aliphatic hydrocarbon chains. Materials which immediately suggest themselves are the long-chain fatty acids (3), whose structure is illustrated in figure 7.2.

Recently, a number of authors (4,5,6) have investigated the electrical properties of such fatty acid monomolecular layers. The most common materials examined were the Cd salts, cadmium arachidate, cadmium stearate and cadmium palmitate. These films were studied in two ways: sandwiched between evaporated metal (MIM), or deposited on a semiconducting surface (MIS). The general conclusion was that fatty acid Langmuir films are good insulators with dielectric strengths greater than 10^6 V/cm. Aromatic hydrocarbons, polymeric materials and biological molecules such as chlorophyll have also been deposited using the Langmuir film technique (2), but their characterization is less complete.

7.23 Preparation of Langmuir Films

The Langmuir trough used for the deposition of the organic monolayers is shown schematically in figure 7.3. The cadmium stearate dissolved in chloroform was spread on the surface of the water using a micrometer syringe, at a temperature of approximately 290 K. The solvent usually evaporated in a few minutes, after which the surface area of the monolayer was varied by means of motor driven PTFE-coated glass fibre barriers. In order to investigate the structure of the

FATTY ACID SALTS

$$[CH_3 (CH_2)_{n-2} COO^-]_2 Cd^{2+}$$

n = 18 CADMIUM STEARATE

n = 20 CADMIUM ARACHIDATE

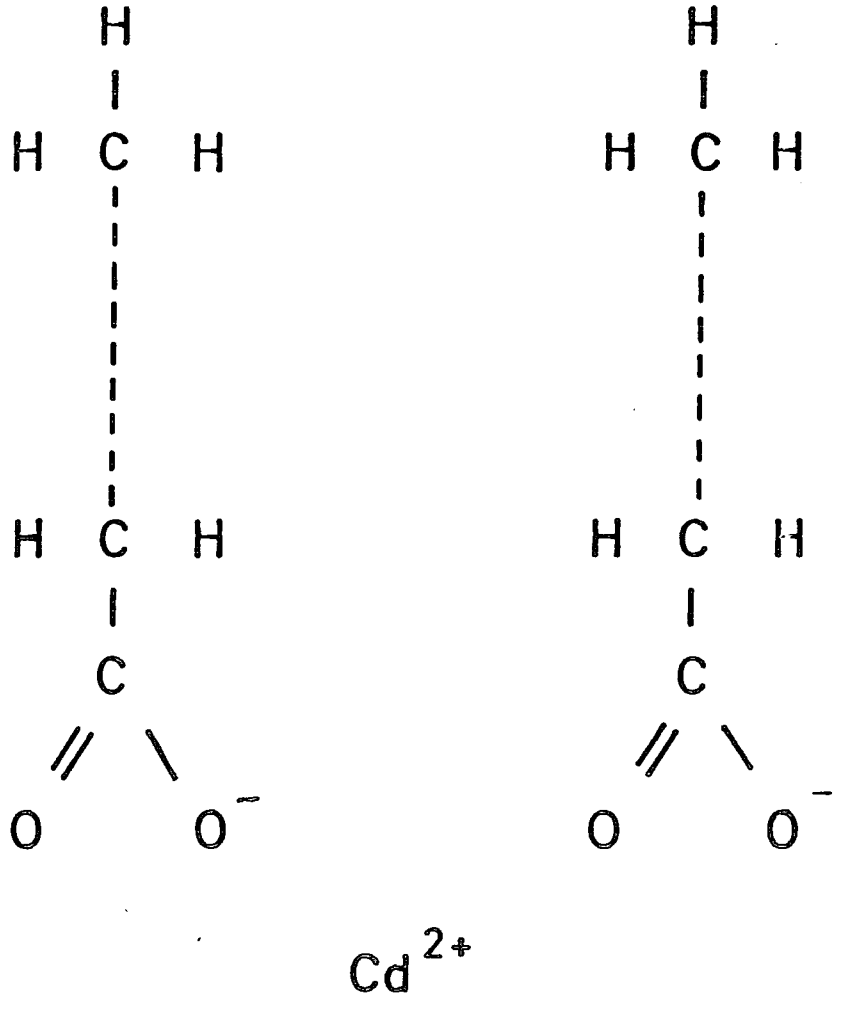


Figure 7.2 Suitable materials for Langmuir film deposition.

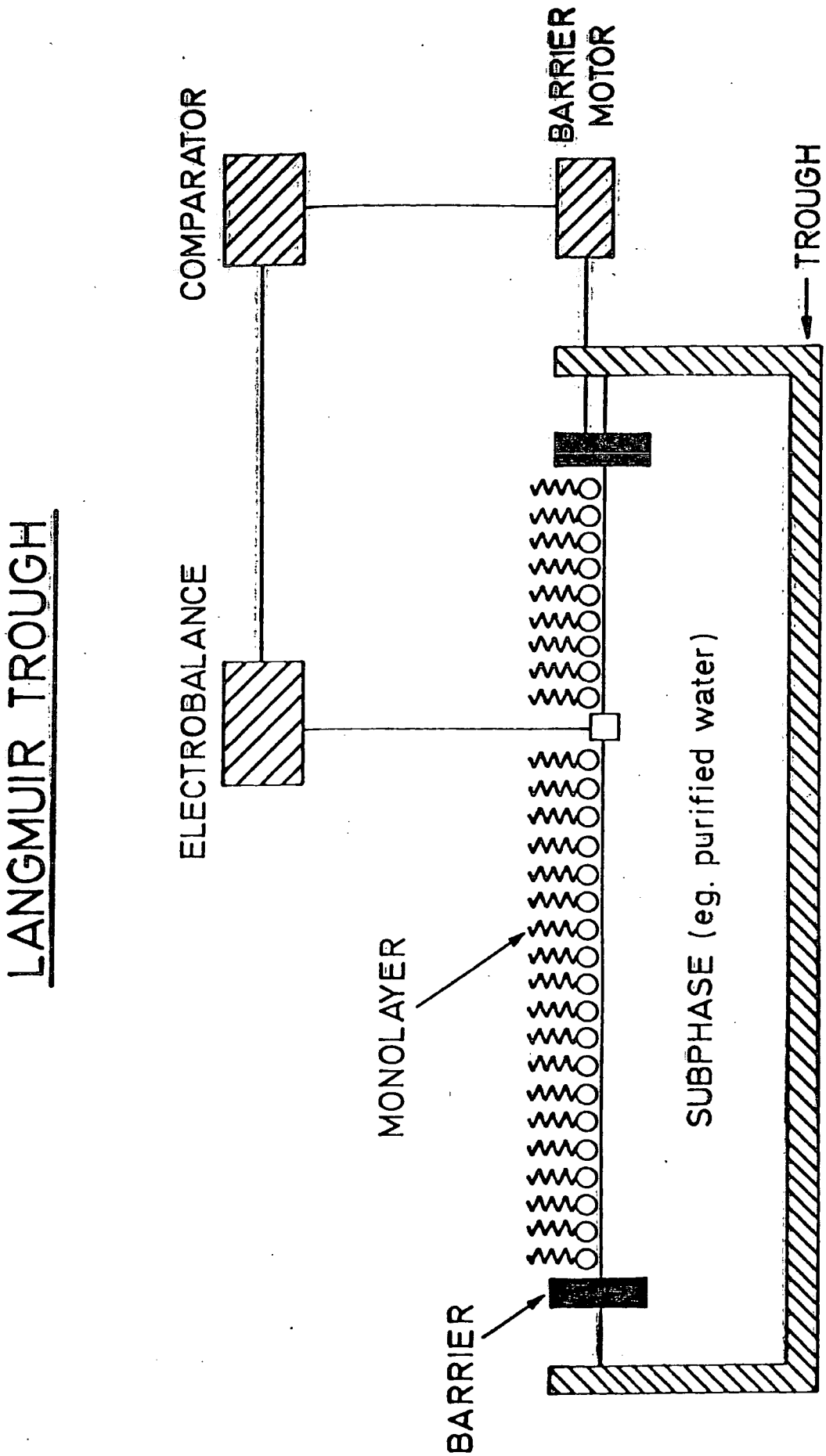


Figure 7.3 Simplified diagram of the Langmuir Trough.

monolayer, and to establish optimum dipping conditions, surface pressure-area isotherms were recorded. These were achieved by compressing the monolayer at a constant rate, typically 0.3 nm per molecule per minute, and recording the surface pressure and area on an X-Y chart recorder. Such a plot is shown in figure 7.4. The surface pressure is monitored using a piece of paper of known dimensions inserted in the monolayer that is attached to a sensitive microbalance. There are three distinct regions to the curve, corresponding to the different phases that the film can be in. At the right side of the plot, the molecules are spread out corresponding to a gas phase; here, some of the upright stearate molecules tend to bend over due to the relatively large amount of space available for them. Compression of the film decreases the surface area per molecule until eventually a quasi-solid is formed where all the molecules are upright; this is the region on the left side of the plot and corresponds to the steeply rising part of the curve. In between these two regions, delineated by the two breakpoints, the film is in a liquid phase. Further increase in the surface pressure simply makes the film more compact, until finally at the top of the graph the monolayer buckles and collapses. It is best to dip a film at a pressure corresponding to this quasi-solid region; in the main, we used a pressure of 25×10^{-3} Nm^{-1}.

In order to obtain good films, the chemicals used have to be of the best available commercial grade and the environment has to be kept dust free, as far as possible in clean room conditions. High purity water for the trough is also necessary; a "Milli-Q" purification unit was employed with the Langmuir trough used in this work. The sophistication of the components of the trough is also crucial, as the

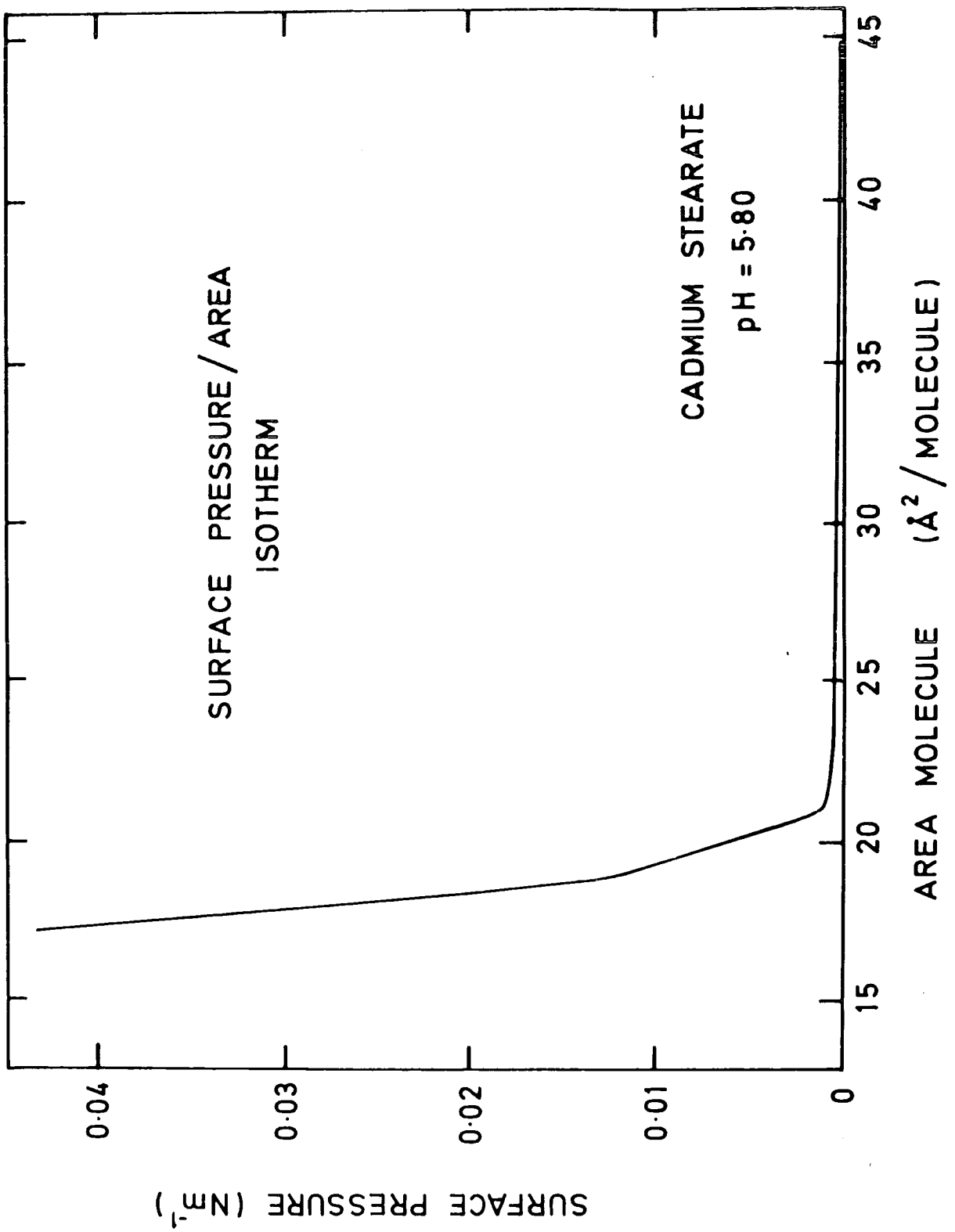


Figure 7.4 Surface Pressure/Area Isotherm for Cadmium Stearate.

feedback system maintains identical dipping conditions for each monolayer.

The substrates were dipped at a rate of 3 mm/min using a variable speed motor attached to a micrometer. The films were dry when they emerged from the subphase and the process of deposition was monitored through the recorded values of the area and pressure. Before top contacts were made to the films, they were stored under dry nitrogen in a desiccator for three days. Several methods of making top contact were attempted: sputtering or thermal evaporation performed at room temperature was found to result in shorted films. This could be overcome by evaporation onto the film whilst it was cooled using liquid nitrogen. Mercury drops were tried, but found to get dirty a little too easily. Graphite water based paste was also explored: the water base was necessary since the organic solvent bases of other conducting pastes were found to be solvents for Langmuir films. However, these contacts were found to be not very adhesive and, in addition, it was suspected from our measurements that the water might have possibly had a deleterious effect on the films.

7.3 Experimental Results

7.31 Langmuir Film Metal-Insulator-Metal (MIM) Structures

The nature of the electrical characteristics of a Langmuir film MIM structure is determined by not only the material type, but also its thickness. In order to avoid the complications of tunnelling, we used structures built up of many monolayers with dimensions similar to those of the MOS devices previously described. A typical dc response

for a 15 monolayer thick cadmium stearate ($CdSt_2$) Langmuir film is given in figure 7.5; the log J versus $V^{1/2}$ dependence is indicative of a barrier limited conduction mechanism. (In contrast, anthracene films can give Ohmic type characteristics and, at higher fields above about 10^6 V/cm, charge injection may occur resulting in a quadratic response (7).) Such measurements were made under a low pressure in an atmosphere of dry nitrogen as it was found that currents, orders of magnitude larger, were sometimes obtained in the presence of moisture. The difference in magnitude between the forward and reverse characteristics may be attributed to the presence of an internal voltage with no external applied bias. This voltage probably arises from chemical reactions within the layer or at the interface (8).

The capacitance characteristics of an MIM structure with a different number of monolayers can be used to demonstrate the degree of order within the films. The linear dependence of a plot of reciprocal capacitance against the number of layers, N, suggests an almost ideal build-up (see figure 7.6). The non zero intercept on the capacitance axis indicates the existence of an extra capacitance in the structure. Since the films were deposited on an aluminium-coated substrate, it is reasonable to assume that this extra capacitance is due to aluminium oxide. When this capacitance is included the total capacitance per unit area may be expressed as:

$$C^{-1} = \varepsilon_o^{-1} \cdot \frac{d_{ox}}{\varepsilon_{ox}} + \frac{N.d}{\varepsilon_i} \qquad (7.1)$$

where ε_i is the dielectric constant of each layer, approximately 2.5 for cadmium stearate Langmuir films. This compares with the value of

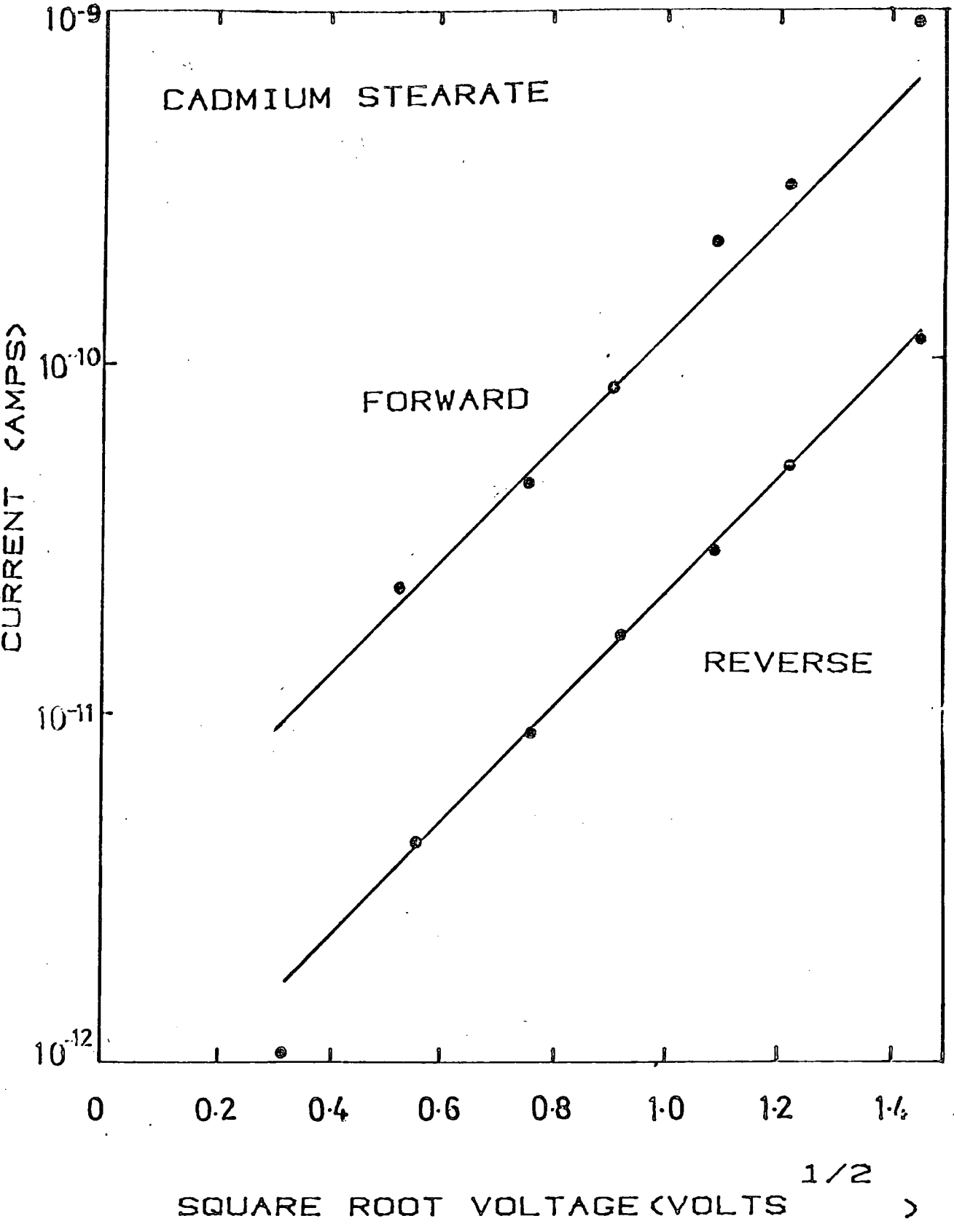


Figure 7.5 Dc response for Cadmium Stearate MIM Langmuir film structure.

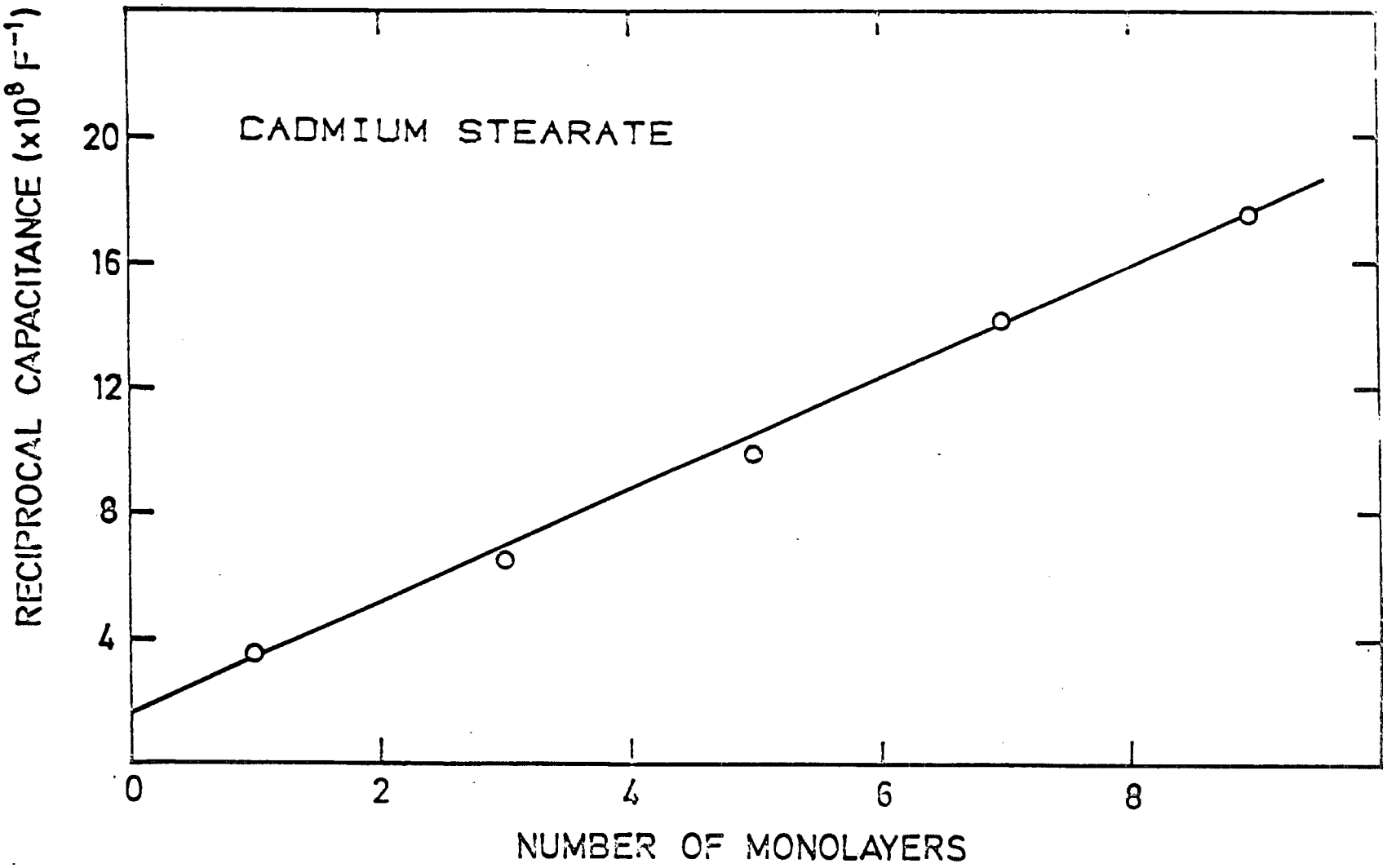


Figure 7.6 Reciprocal capacitance for different monolayer thicknesses.

2.9 calculated from the slope of the dc current plot of figure 7.5, assuming a neutral trap Poole Frenkel conduction-type mechanism.

Measurements were also performed to check the variation of capacitance with frequency. It was found to be constant over the measurement range of 10 Hz to 100 kHz, indicating the presence of a good insulator. Typical ac conductivity data for Langmuir films are shown in figure 7.7. The film exhibits a frequency independent conductivity with $G \propto \omega^n$. Below 10 kHz, n is equal to 1, whereas above that frequency it takes a value in the region of 2.0. Street et al (9) have attributed the latter to a series resistance associated with the electrodes. Indeed, it was found in practice that the long thin aluminium strips used to make contacts possessed a non-zero resistance. According to Street (9), the conductance depends on various parameters such that:

$$G \propto \omega^2 \quad C_x^2 \quad R_o \tag{7.2}$$

where C_x represents the sample capacitance and R_o its series resistance. Thus, provided that the latter are frequency independent, the conductance is proportional to ^{2}.

7.4 Langmuir Film Metal Insulator Semiconductor (MIS) Structures

Several MIS device configurations (10,11,12) have been fabricated using different combinations of organic and semiconductor materials. We decided to use the fatty acid salt cadmium stearate and single crystal silicon because of their individually well-characterized nature. Various film thicknesses were deposited on bulk and epitaxial silicon which yielded qualitatively the same results.

Langmuir film deposition on silicon was found not to be as easy as on aluminium oxide. That is, pick-up of the films from the subphase was more difficult, possibly due to the less receptive nature of the silicon surface towards Langmuir films. Various substrate preparation procedures were attempted to see if it could be improved; these are discussed in section 7.43. The result was poorer electrical characteristics. For example, the dc current response, although still log J versus $V^{1/2}$, giving the correct dielectric constant value, had a current magnitude that was considerably larger. As before, a difference in the forward and reverse characteristics was measured, but this can be explained by the presence of a depletion layer in the measurement of the latter.

7.41 Admittance-Voltage Characteristics

A typical set of admittance-voltage characteristics for a cadmium stearate Langmuir film on p-type silicon is given in figure 7.8. True capacitance accumulation can be seen on the left, its value agreeing with that expected for such an insulator thickness and top contact area; and inversion on the righthand side of the curve. The converse of these curves is obtained on n-type silicon. In figure 7.9, the capacitance curves for two different thicknesses of Langmuir film are shown, indicating the effect on accumulation and inversion capacitance values; it can be seen that a change in the dielectric thickness of the Langmuir film can be distinguished from an area change of the top contact when the magnitude of the whole of the curve decreases.

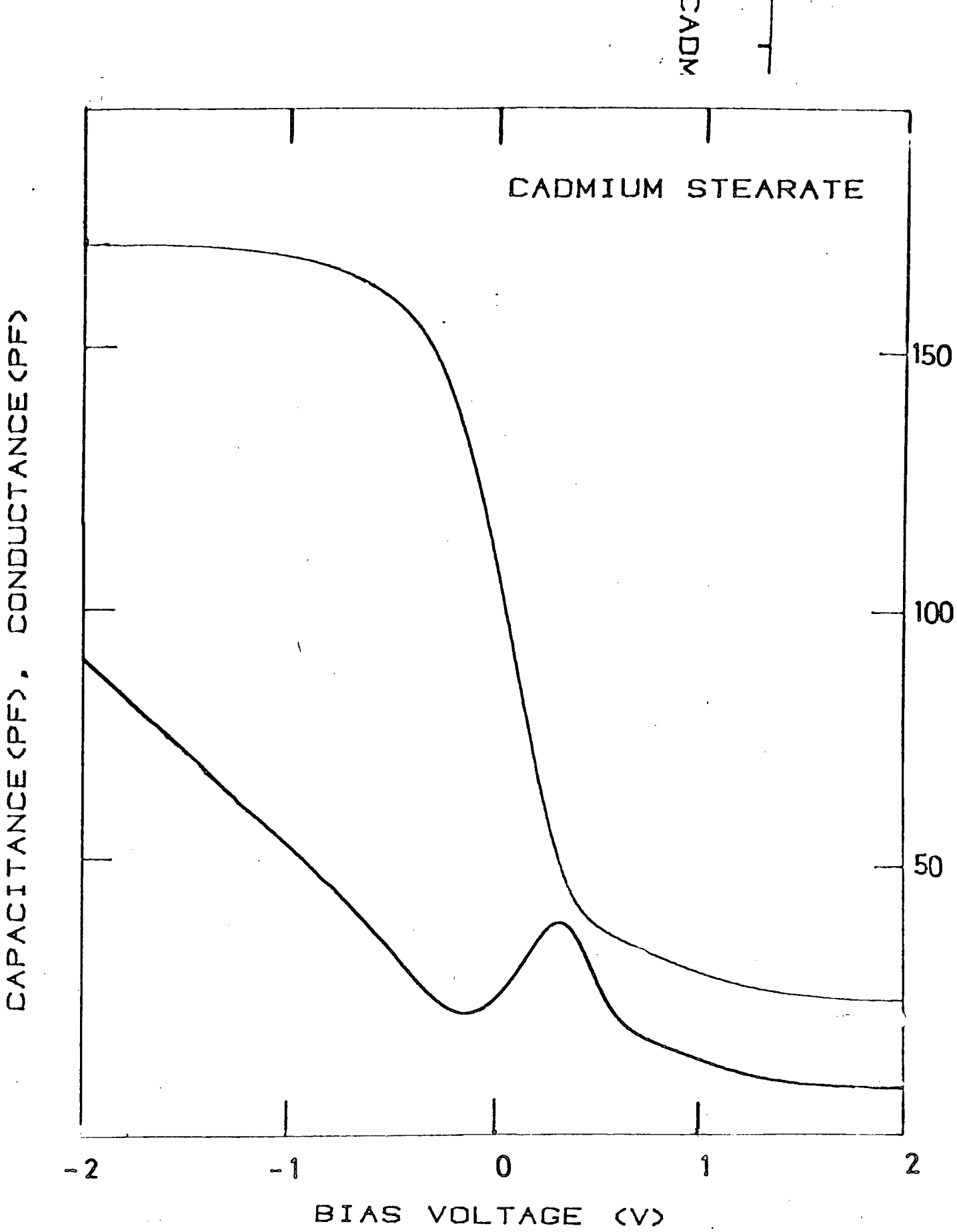


Figure 7.8 Langmuir film admittance-voltage characteristics.

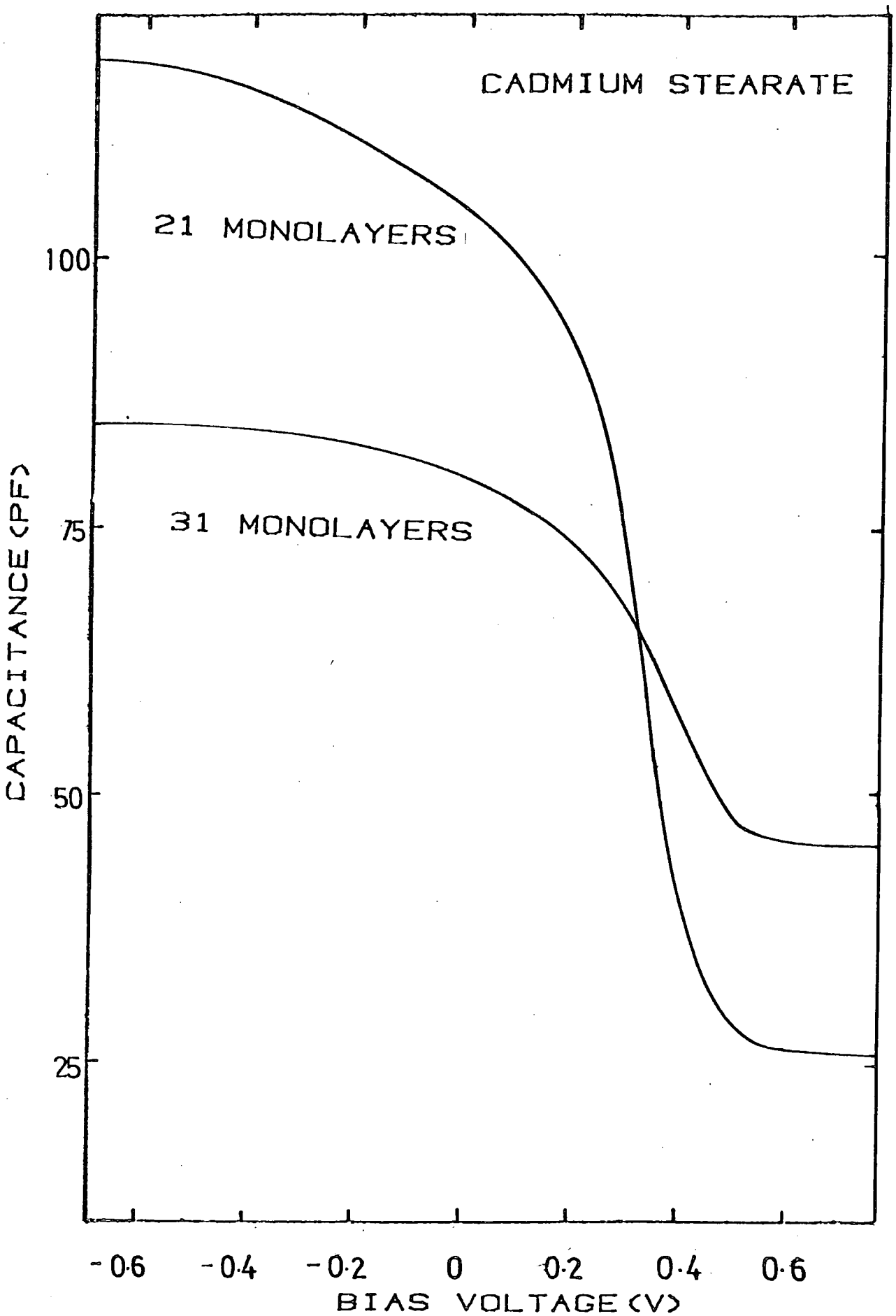


Figure 7.9 Capacitance voltage characteristics for two different thicknesses of Langmuir film.

Recently, Hickmott (13) has reported that a flat band voltage versus insulator thickness curve gives information concerning the presence of charge within the insulator or dipoles at its surface. The flat band voltage is graphically obtained from the position of the flat band capacitance. The latter may be found by various techniques, the easiest of which is the use of Goetzberger's ideal curves (14). He has provided normalised plots of flat band capacitance against insulator thickness with doping density as a parameter. The curves are actually for silicon dioxide and compensation has to be made, which is performed by multiplying the thickness by the ratio of the two dielectric constants. This has been carried out for three Langmuir film thicknesses deposited on the same substrate and the value of normalised flat band capacitance obtained. The corresponding value of flat band voltage has been found from the measured characteristics of the devices and is plotted against insulator thickness in figure 7.10. The line is straight as predicted by Hickmott, but possesses the opposite slope to that normally found for MOS devices, also shown in figure 7.10. The latter is indicative of a positive charge within the oxide, hence the positive slope we have found is indicative of negative charge. This result is reinforced by examination of the admittance characteristics themselves, which seem to be generally to the right of the zero volts axis; this, too, indicates the presence of negative charge.

The conductance-voltage characteristic shown in figure 7.8 is obviously non-ideal, possessing an anomalous increase in accumulation. In order to show that it was independent of surface preparation

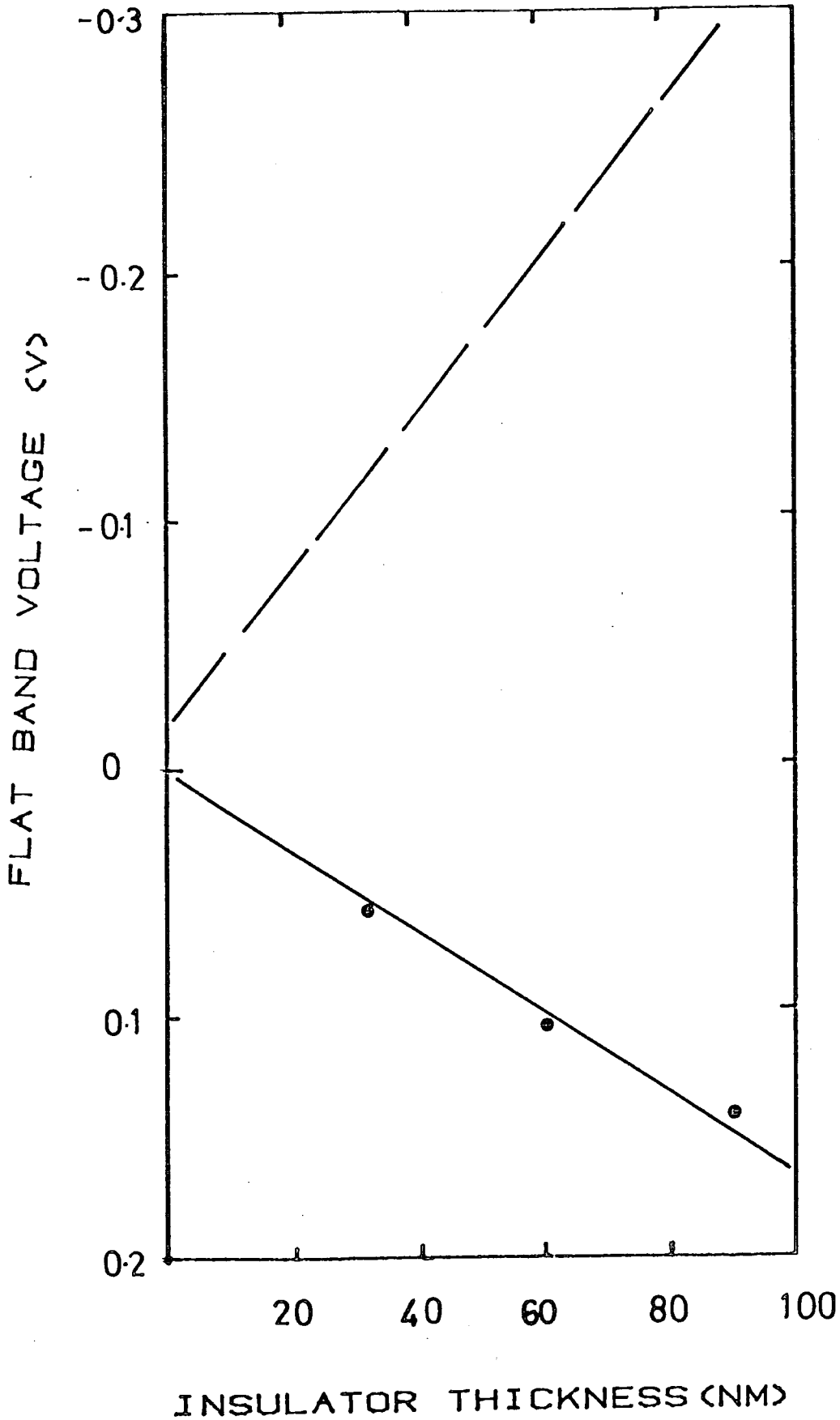
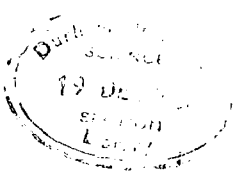


Figure 7.10 Flat band voltage versus insulator thickness for Langmuir film (●) and silicon dioxide.

technique, three different preparation procedures were undertaken. These were: (1) etching in buffered hydrofluoric acid, followed by immediate dipping; (2) etching then leaving the sample around for a while to collect a thin layer of atmospheric oxide; and (3) etching followed by a long (greater than one hour) cleansing procedure consisting of a thorough rinsing in pure water and an iso-propyl alcohol reflux. The purpose of the latter is to remove any fluorine ions which are thought to be left behind after etching. However, it was found that these procedures all gave basically the same results. Different Langmuir films on silicon also give the same effect. For example Tanguy (16) discovered the same with orthophenanthroline and we have obtained similar characteristics with a polymer film which is discussed in section 7.54.

The rise in accumulation conductance is reminiscent of the tunnelling conductance plots given in the previous chapter, implying some current flow type mechanism. A possible explanation for the rise is the poorer insulator characteristics of Langmuir films on silicon, as indicated by the larger dc current passed. If the current was Ohmic then the associated ac conductance would be constant with bias and able to be compensated for. However, since the current mechanism possesses a power law dependence, then the corresponding conductance rises with applied bias. Alternatively, carrier injection from the silicon surface could account for the observed effect. However, this seems unlikely in view of its invariance with surface preparation. In addition, the increase in conductance in forward bias was observed with both n-type and p-type samples.



One particular bulk sample did give a good flat accumulation conductance over a limited region. The reason for this was possibly that, since this sample was a bulk one, its series resistance may have swamped the conductance contribution from the film leakage. However, a complete characterization was made difficult by the instability of measured characteristics. Reproducible measurements could only be made by cycling the sample with a triangular waveform bias. The resultant hysteresis was different from that obtained with the rest of the samples. With the majority, hysteresis that can be attributed to ion motion dominated (see figure 7.11a), but with this sample, the charge seemed to leak away in accumulation, giving rise to the hysteresis shown in figure 7.11b. If the scan was slow enough (1 mV/s) then a mixture of the two hysteresis types was obtained, where ion motion type hysteresis dominated at low biases. (see figure 7.11c)

7.42 Surface State Analysis

Unfortunately, it is not possible to use the standard techniques to analyse the surface state spectrum at the silicon-Langmuir film interface. The various reasons are outlined below:

(1) Quasi-static Method

As has been pointed out in section 5.2, this technique requires insulators with leakage currents less than picoamps. It can be seen from figure 7.5 that the dc current passed by a Langmuir film MIM

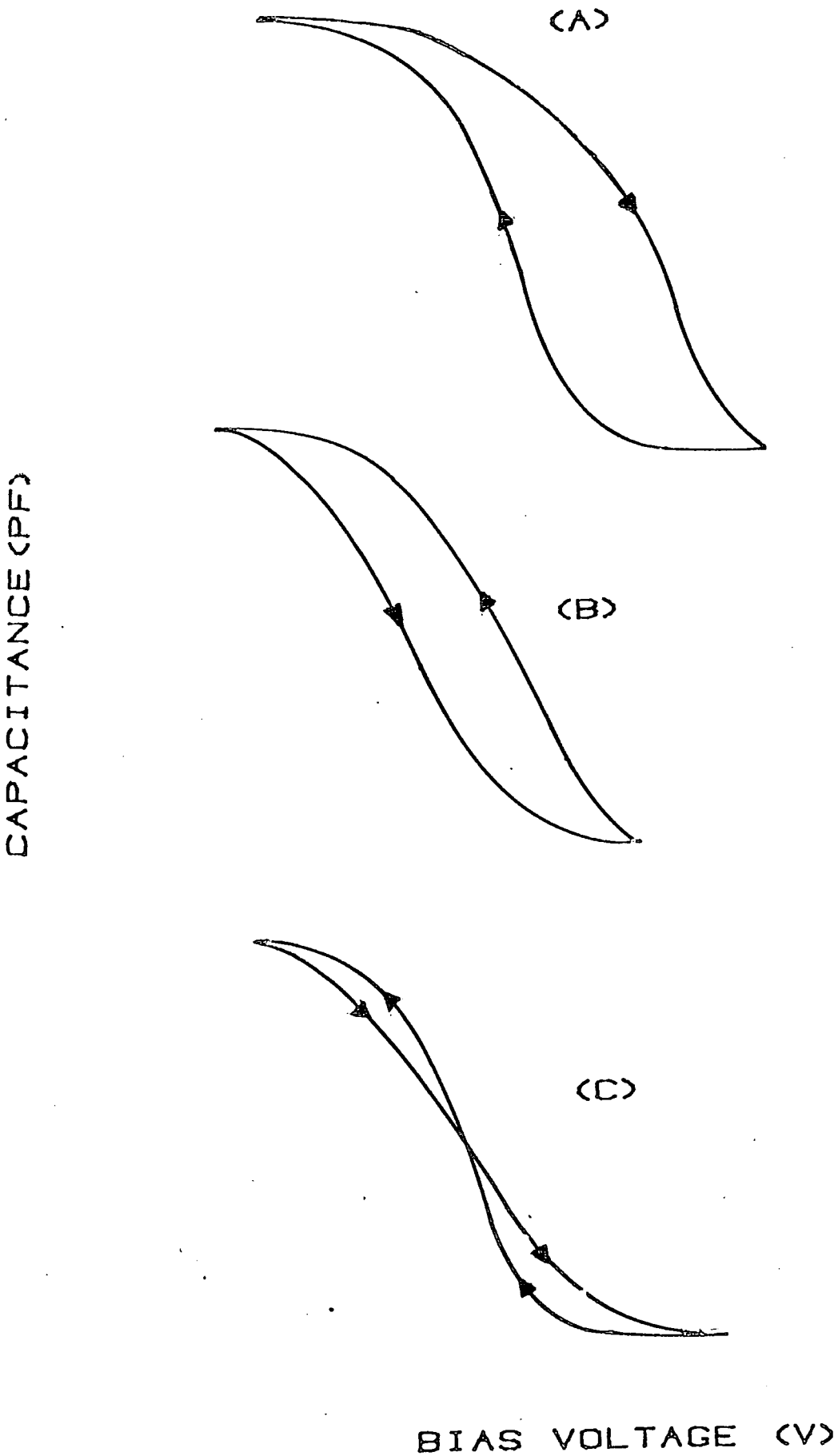


Figure 7.11 Different hysteresis forms for Langmuir films.

structure is larger by comparison, and it was mentioned in section 7.4 that the leakage current for MIS structures was larger still. Thus it can be seen that such leakage will tend to swamp the displacement current, making surface state analysis impossible.

(2) Conductance Technique

The problem with a rising value of accumulation conductance is that it makes parallel conductance calculation impossible owing to the fact that the series resistance value cannot be determined. In addition, the extra conductance will obscure the value of the conductance peak in a similar way to the series resistance effect mentioned in section 4.6. Thus the use of the conductance technique is ruled out. On the single sample that did have a limited flat accumulation conductance region, the application of the novel technique that we have developed was prevented owing to the drift of the characteristics at constant bias. In fact, the presence of the leakage current probably invalidates the approximations implicit in the modified Nicollian & Goetzberger analysis technique.

(3) Terman's Technique

It was shown in Chapter 3 that the theoretical curve calculated for the estimation of the surface state density could easily be in error and hence lead to spurious results. However, if we are interested in the change introduced by a gas, then it is not absolutely necessary to calculate the theoretical curve: we need only

be concerned with the difference between initial and final values of the measured capacitance. The Terman technique is good for the case where only the surface states are liable to be affected (or not, as was the case with MOS devices), but if the insulator capacitance changes as well, then the technique cannot be used. The reason for this is that if C_i changes, then the voltage distribution in the device does too. If the voltage drop in the semiconductor alters, then the occupancy of the surface states will be different and shape will be introduced into the high frequency C-V curve that might be misinterpreted as surface state change. With our results, to be discussed in the next section, insulator capacitance change was found to occur, thus invalidating this technique.

7.43 Comparison with Langmuir Films on Alternative Semiconductors

Langmuir films have been sucessfully deposited on several semiconductors; and good reproducible admittance characteristics reported (11,12). In all cases, however, considerable emphasis was placed on the surface preparation prior to the film deposition. Both the measured hysteresis and the surface state peak conductance magnitude were found to be sensitive to the etching technique.

The Langmuir films deposited on silicon are generally more conducting than those prepared on other semiconductors. The reason for this is unclear, but is probably related to the difficulties experienced in picking up the film from the subphase. We have examined electron diffraction patterns of the films prepared on silicon and other substrates, but have found no detectable

differences. It is possible nevertheless that poor stacking of the film could result in a higher defect-induced conductivity. Clearly, more research work is required to discover an alternative suitable surface preparation technique which will make the silicon substrate more receptive to the Langmuir film. One possibility is the silanization (15) of the surface prior to deposition, with an organic surfactant e.g. trimethylcholrosilane. This produces a monolayer coverage of methyl groups upon the surface.

7.5 Gas Effects on Langmuir Films

In spite of the above difficulties in the determination of surface state density information, several gaseous exposures were performed to see if any change occurred in the measured admittance characteristics which might be attributed to a surface state effect. The gases exposed to different Langmuir film structures were carbon monoxide, methane, ammonia and hydrogen chloride; the last two are of opposite chemical type. Since Langmuir films have a more open structure, it might be expected that gases would penetrate to the interface more easily and be more likely to have an effect. However, this was not found to be the case: most of our results could be explained by the action of moisture. It will be shown that the presence of moisture is significant.

is further proof that the effect is water-related.

Carbon monoxide and methane did not give such dramatic variations in the measured characteristics: only small changes in the accumulation admittance values were observed which were seen to simply alter the total magnitude of the curve. Such effects can be explained by changes in the water content of the film, either its extraction or displacement.

7.52 Palladium/Langmuir Film/Silicon

The effect of hydrogen on MOS structures has been described in the previous chapter. It is only when the top electrode is palladium that there is any noticeable change. When a Langmuir film was used as the insulator, a simple lateral shift in the measured curves of about 0.5V was observed. The rate of reaction was similar to that obtained with the MOS structures.

7.53 Effect of Gases on other Langmuir film MIS structures

Cadmium stearate Langmuir films have also been deposited on indium phosphide in order to investigate the effect of various gases (15). This work has shown some encouraging results regarding possible surface state change. Unlike the simple lateral shift effect of hydrogen on palladium MOS structures, hydrogen on aluminium top contacted Langmuir film structures seems to introduce a reversible change in the magnitude of the measured surface state conductance peak. At the same time, there is no corresponding significant change

in the capacitance characteristic. This might well imply a surface state effect.

Further evidence that surface state changes are induced by gases is provided by different gases, chloroform and ammonia, respectively, producing opposite lateral shifts in the measured conductance bias curves. There are at least three possible explanations for why we should observe apparent change in the surface state spectrum in indium phosphide, but not in silicon. The first relates to the oxide layer on silicon. Maybe the residual oxide layer on the silicon surface that grows almost instantaneously after etching is impermeable to gas, even at such small thicknesses. Possibly this oxide could also account for the poor quality of the deposited Langmuir films. Secondly, the suspect insulating properties of Langmuir film may cause any change in surface state density to be obscured. Finally, as has been mentioned previously (section 6.5), the accessible range within the bandgap for the admittance technique is limited; possibly, owing to the different semiconductor, the effected region in the bandgap now falls within this accessible range.

7.54 Summary and Suggestions for Further Work

Results for an alternative insulator to silicon dioxide on silicon, namely cadmium stearate Langmuir film, have been presented in this chapter. The good capacitance-voltage characteristics were undermined by the relatively high leakage current passed by these films when they were deposited on silicon. This has prevented the use of the standard surface state analysis techniques and also complicated

the interpretation of the effect of gases. The change of characteristics induced by the action of gas has been accounted for without recourse to surface state density change. It has been proposed that the presence of moisture has been responsible for the effects observed. However, as has been outlined in the previous section, encouraging results have been obtained with another semiconductor which means that there might be a chance to develop a solid state gas detector.

The drawback with cadmium stearate Langmuir film, though, is its instability, manifest by its low melting point which is less than 370K. At present there is considerable effort being expended on finding a suitable alternative: di-acetylene polymer (16) may be a possible contender.

An alternative path of research for MIS-based gas detectors is to utilize the pyroelectric effect rather than surface state change. Certain organic materials are known to be pyroelectric ie develop a voltage on exposure to heat. It may be possible to deposit them in the form of Langmuir films in an MIS structure. The top metal could conceivably be some form of material such as a catalyst specifically sensitive to certain gases. The heat of the resultant reaction could be monitored indirectly through the flat band voltage of the MIS device, and the interacting substance identified.

It should also be possible to synthesize monomolecular layers that display piezoelectric properties; the required change of polarization thus occurs from a mechanical stress change produced by a gas collecting on the top contact. Selective detection would again be

achieved by making the metal of a material that selectively absorbs or reacts with the pollutant to be monitored.

Finally the Langmuir film structure might possibly provide the vehicle for the fabrication of solid state biological sensors. Such structures where the insulator reacts with active biological molecules or enzymes have already been proposed (17).

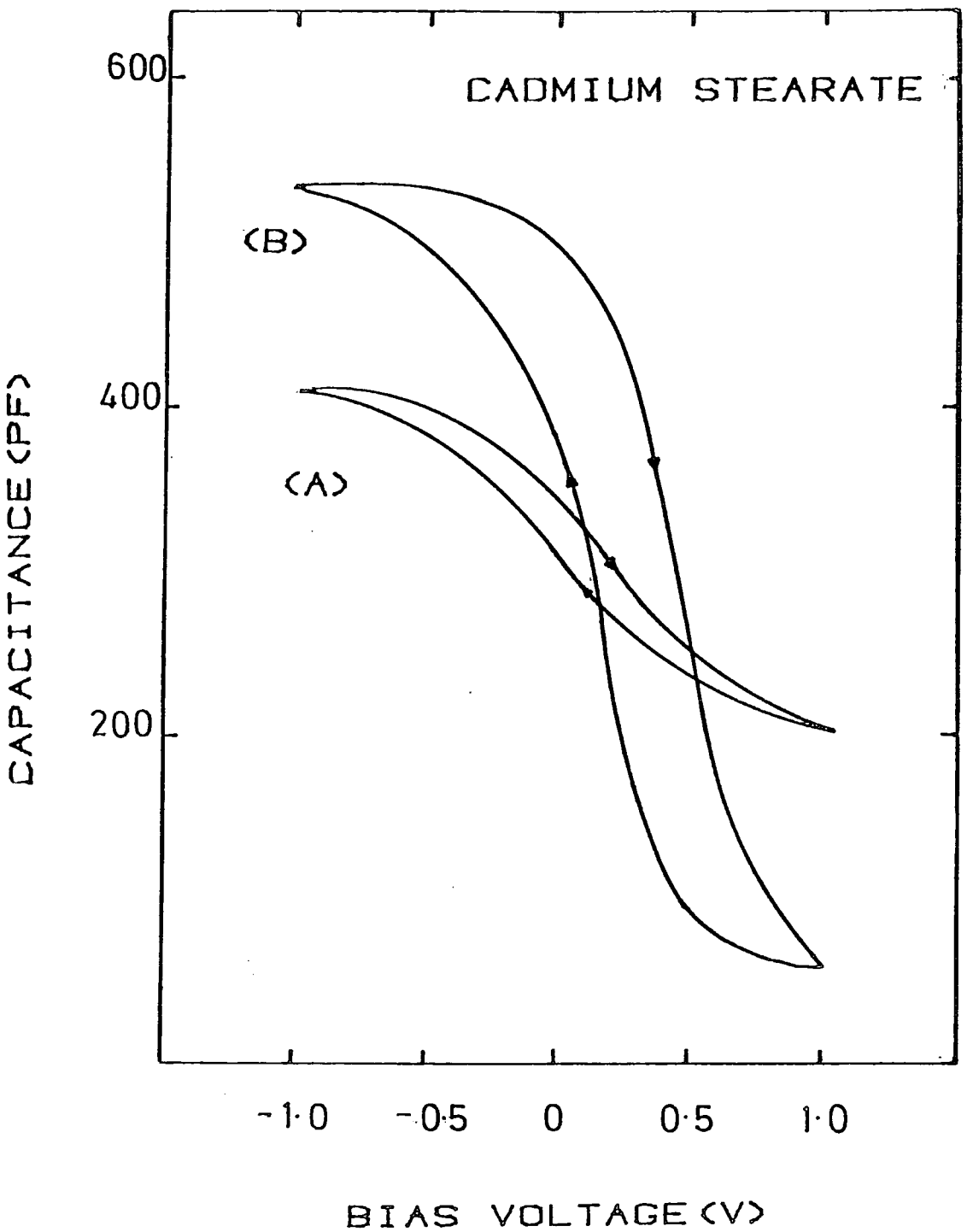


Figure 7.12 The effect of wet ammonia upon a Langmuir film MIS structure. (a) Before (b) after gas.

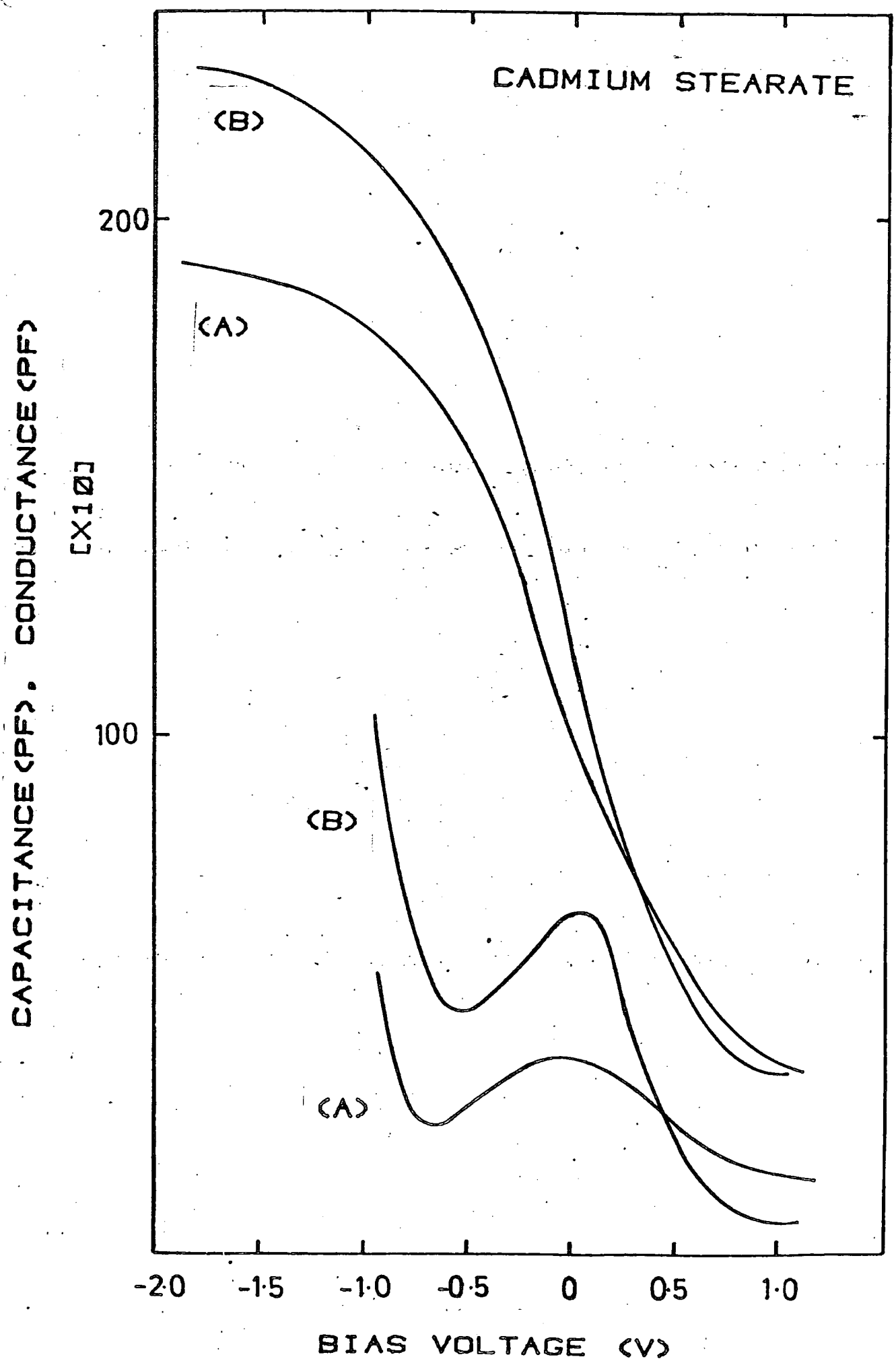


Figure 7.13 Effect of wet ammonia on admittance-voltage characteristics. (a) Before (b) after gas.

Chapter 8

Summary

In this work, a semiautomatic measurement system has been developed for evaluating the electronic structure of the interface between an insulator and a semiconductor. The associated microcomputer possesses advanced software which leads to simple operation, particularly when used in a real-time mode. By utilizing the latter facility, we have been able to reduce the effort involved in the conventional ac conductance technique. Previously, all the admittance data had to be collected before analysis was possible. This was inefficient as it produced a lot of redundant data. Such a quick analysis technique might find use in the semiconductor industry in areas where fast surface state evaluation is necessary.

The fast operation of this system has been capitalized upon in the analysis of the effect of the ambient on MIS devices. With MOS structures, we placed the emphasis on the effect of hydrogen, whose role in hydrogen sensitive Pd MOS sensors is still a subject of controversy. We have shown that hydrogen introduces no measurable surface state density, although we do suggest that possibly there are surface states introduced beyond the range of our equipment. Unfortunately, Langmuir films were not found to be ideal insulators on silicon: this prevented complete surface state analysis of the MIS devices that we produced. In addition, gaseous reactions with the structures were dominated by moisture which introduced parasitic effects that complicated the results. Nevertheless, gas effects were found with Langmuir films deposited on indium phosphide, which suggests that a selective sensitive solid state gas detector might be developed.

Even though Langmuir films in this work have not produced perfect results, it is felt that they are a very interesting field of research. We have attempted to use their insulator qualities upon semiconductors, neglecting their optical ones which show greater promise. Langmuir film monolayers have been proposed for use in MIS solar cells, integrated optic devices, and as lithographic agents. Certainly, then, there is scope for considerable further research in the area of Langmuir Films and their application.

REFERENCES TO CHAPTER 1

1. Nicollian E./Goetzberger A. BSTJ 46, p1055 (1967)
2. de Rooij N./Bergveld P. Proc.Int.Top.Conf. (N.Y.), p433 (1978)
3. Keramati B./Zemel J. Proc.Int.Top.Conf. (N.Y.), p459 (1978)
4. Lundstrom I., et al. J.App.Phys. 46, p3876 (1975)

REFERENCES TO CHAPTER 2

1. Nishi Y. Jpn.J.Appl.Phys. 5, p333 (1965)
2. Ligenza J.R. J.Phys.Chem. 65, p2011 (1961)
3. Cheng Y.C. Progress in Surface Science-8 No 5, p181 (1977)
4. Svensson C.M. Proc.Int.Top.Conf.(N.Y.), p328 (1978)
5. Lucovsky G. Philos.Mag.B. 39, p513 (1979)
6. Street G./Mott N. Phys.Rev.Lett. 35, 1293 (1975)
7. Nishi Y. Jpn.J.Appl.Phys 10, p52 (1971)
8. Poindexter E., et al. IEEE ED-24, p1217 (1977)
9. Pepper M. Proc.R.Soc.Lond. A353, p225 (1977)
10. Silversmith D. J.Electrochem.Soc. 119, p1509 (1972)
11. Fahrner W./Goetzberger A. App.Phys.Lett. 21, p329 (1972)
12. Schulz M./Klausmann E. App.Phys.Lett. 18, p169 (1979)
13. Sah C.T. IEEE Trans.Nucl.Sci. 23, p1563 (1976)
14. Balk P. J.Electrochem.Soc. 118, p494 (1971)
15. Snel J. INFOS-Durham IOP Conf. No. 50 p119 (1979)
16. Flietner H./Sinh N. Phys.Stat.Sol.(a) 37, p533 (1976)
17. Rhoderick E. "Metal-Semiconductor Contacts" O.U.P. (1978)
18. Sze S."Physics of Semiconductor Devices" Wiley N.Y. (1969)
19. Goetzberger A.,Klausmann E.,Schultz M. CRC Review (Jan 1976)
20. Goetzberger A. BSTJ 45, p1097 (1966)
21. Hu S.M.,Kerr D.,Grigor L. App.Phys.Lett. 10, p97 (1967)
22. Schwartz R.J., et al. S.S.Elect. 14, p115 71

23. Nicollian E./Goetzberger A. BSTJ 46, p1055 (1967)

24. Muls P.,Declerck G.,Overstraeten R. S.S.Elect.20, p911 (1977)

25. Preier H. App.Phys.Lett. 21, p361 (1967)

26. Heiman F.,Warfield G. IEEE Elect.Dev. ED-12, p167 (1965)

27. Warashina M./Ushirokowa A. Jpn.J.App.Phys. 14, p1739 (1975)

28. Deuling H.,Klausmann E.,Goetzberger A. S.S.Elect. 15 p559 (1971)

29. Lehovec K./Slobodskoy A. S.S.Elect. 7, p59 (1964)

30. Cooper J./Schwartz R S.S.Elect. 17, p641 (1974)

31. Deneuville A. J.App.Phys. 45, p3079 (1974)

32. Kar S./Dahlke W. S.S.Elect. 15, p221 (1972)

33. Nicollian E./Goetzberger A. IEEE ED-11, p108 (1965)

34. Lightenberg H. MSc Thesis University of Groningen (1979)

REFERENCES TO CHAPTER 3

1. Brugler J.S./Jespers P.G.A. IEEE ED-16, p297 (1969)

2. Overstraeten R. et al. IEEE ED-22, p282 (1975)

3. Terman L.M. S.S.Elect. 5, p285 (1962)

4. Zaininger K./Warfield G. IEEE ED-12, p179 (1965)

5. Sah C.T. et al. S.S.Elect. 12, p690 (1969)

6. McNutt M.J./Sah C.T. App.Phys.Lett. 26, p378 (1975)

7. Declerk G. et al. S.S.Elect. 16, p1451 (1973)

8. Berglund C.N. IEEE ED-13, p701 (1966)

9. Kuhn M. S.S.Elect. 13, p873 (1970)

10. Castagne R./Vapaille A. Elect.Lett. 6, No.22 (1970)

11. Nishimatsu S./Ashikawa M. Rev.Sci.Instrum. 15, p1109 (1974)

12. Lopez A. Rev.Sci.Instrum. 44, p200 (1972)

13. Brown D.M./Gray P.V. J.Electrochem.Soc. 115, p760 (1968)

14. Boudry M.R. App.Phys.Lett. 26, p530 (1973)

15. Snel J. INFOS-Durham IOP Conf. No.50 p119 (1979)

16. Lang D.V. J.App.Phys. 45, p3023 (1974)

17. Schultz M./Klausmann E. App.Phys. 18, p169 (1979)

18. Klausmann E. INFOS-Durham IOP Conf. No.50 p97 (1979)

19. Goetzberger A.,Klausmann E.,Schultz M. CRC Review Jan. (1976)

20. Simonne J.J. S.S.Elect. 16, p121 (1974)

21. Ziegler K./Klausmann E. App.Phys.Lett. 26, p400 (1975)

22. Lam Y.W. Jpn.J.App.Phys. 12, p916 (1973)

REFERENCES TO CHAPTER 4

1. Shewchun J./Waxman A. Rev.Sci.Instrum. 37, p115 (1966)

2. Boudry M.R. J.Phys.E. 11, p237 (1978)

3. Moore C.H. Astron. & Astrophys. 15, p497 (1974)

REFERENCES TO CHAPTER 5

1. Boudry M.R. J.Phys.E. 11, p237 (1978)

2. Nicollian E./Goetzberger A. BSTJ 46, p1021 (1966)

3. Lanczoz C. "Applied Analysis" Prentice Hall Inc. (1956)

4. Kuo F./Kaiser F. "Systems analysis by digital computer" J.Wiley & Son (1967)

5. Warashina M./Ushirokowa A. Jpn.J.App.Phys. 14, p1739 (1975)

6. Berglund C.N. IEEE Trans. ED-13 p701 (1966)

7 Simmons J. et al. S.S.Elect. 22, p887 (1979)

8. Bosch J. MSc Thesis, Groningen State University (1979)

REFERENCES TO CHAPTER 6

1. Revesz A.G. J.Electrochem.Soc. 26, p122 (1979)
2. Revesz A.G. Proc.Int.Top.Conf. (N.Y.) p222 (1978)
3. Lundstrom I. et al. App.Phys.Letts. 26, p55 (1975)
4. Lundstrom I. et al. J.App.Phys. 46, p3876 (1975)
5. Steele M.C./MacIver B.A. App.Phys.Letts. 28, p687 (1976)
6. Ito K. Surface Science 86, p345 (1979)
7. Conrad H. et al. Surface Science 58, p578 (1976)
8. Demuth J.E. Surface Science 65, p369 (1977)
9. Bucur R.V. Surface Science 62, p519 (1977)
10. Lundstrom I. et al. Surface Science 64, p497 (1977)
11. Keramati B./Zemel J.N. Proc.Int.Top.Conf. (N.Y.), p459 (1978)
12. Dus R. Surface Science 42, p324 (1973)
13. Jaeckel R./Wagner B. Vacuum 13, p509 (1963)
14. Keramati B. PhD Thesis University of Pennsylvania (1979)
15. Svensson C.M. To be published.
16. Pautrat J./Pfister J. Phys.stat.sol.(a) 11,p287 (1972)
17. Saminadyar K./Pfister J. Phys.stat.sol.(a) 36,p679 (1976)
18. Taininger K./Warfield G. Proc. IEEE Aug., p972 (1964)
19. Lopez A. Rev.Sci.Instrum. 44, p200 (1972)
20. Kar S./Dalhke W. S.S. Elect. 15, p221 (1972)
21. DiMaria D.J. Proc.Int.Top.Conf. (N.Y.), p160 (1978)
22. Kasprzak L./Gaind A. Proc.Int.Top.Conf. (N.Y.), p438 (1978)

REFERENCES TO CHAPTER 7

1. See "Proceedings of INFOS" (Institute of Physics Conference Durham 1979) Series no 50 eds. G.G.Roberts & M.J.Morant.
2. Vincett P.S./Roberts G.G. Thin Solid Films 68 p135 (1980)

3. Gaines G.L. "Insoluble Monolayers at Liquid Gas Interface" Interscience New York (1966)

4. Handy R.M./Scala L.C. J.Electrochem Soc. 113, p109 (1966)

5. Nathoo M.H./Jonscher A.K. J.Phys.C. 4, pL301 (1971)

6. Mann B./Kuhn H. J. Appl. Phys. 42, p 4398 (1971)

7. McGinnity T.M. PhD Thesis Durham University (1979)

8. Honig E.P. Thin Solid Films 33, p231 (1976)

9. Street R.A., et al. J. Non-Cryst.Solids 5, p276 (1971)

10. Tanguy J. Thin Solid Films 13, p33 (1972)

11. Roberts G.G., Pande K.P., Barlow W.A. Electron Lett. 13, p581 (1977)

12. Petty M.C./Roberts G.G. Electron Lett 15, p335 (1979)

13. Hickmott T.W. IBM Internal Research Report RC p 8117 (1980)

14. Goetzberger A. BSTJ 45 p1097 (1966)

15. R.W. Sykes (to be published)

16. Pitt C.W./Walpita L.M. Electron Lett. 12, p479 (1976)

17. Dresner J. RCA Review 30 p322 (1969)

APPENDIX 1 : SIXTH WORD DEFINITIONS

1.BASIC FLOATING POINT PACKAGE (FPP) LINKAGES

FPAC	Floating point (F.pt.) accumulator No. 1
FPOP	Floating point accumulator No. 2
POP.O	Puts address of top of stack on stack
RETFPAC	Store in FPAC (4 regs) contents of N and 3 addresses up
FPOPRET	Store in FPOP (4 regs) contents of N and 3 addresses up
TSTFPAC	Store in N and 3 addresses up contents of FPAC
FPACST	Store M,N in LSB's of FPAC
x10,/10	Change FPAC by factor of 10
ADD,SUB, MUL,DIV	Use algebraic routines in FPP to manipulate FPOP and FPAC
INP	Input to FPAC from terminal
OUT	Print contents of FPAC

2. FLOATING POINT LINKAGES TO STACK

CL	Clears FPAC and FPOP
RETFPACS	Store M,N in FPAC
FPOPRETS	Store M,N in FPOP
INTER	Store M,N in FPAC and K,L in FPOP
TSTFPACS	Store FPAC at M,N
	Put entered data onto stack as floating point number
+.	Add two floating point numbers on the stack
-.	Subtract two floating point numbers on the stack
x.	Multiply two floating point numbers on the stack
/.	Divide two floating point numbers on the stack
Z,J,V,Q	Integers
EX	Gives floating point number L,M exponent N

3. DVM INTERFACE ROUTINE

INIT	Initialise PIA's to receive data from DVM
DVM	Get data from DVM and put it back on stack
CAP	Set DVM to measure capacitance voltage
COND	Set DVM to measure conductance voltage
ZA	Compensate for different parity bit and do ASCII conversion
YY	Contains decimal point indicator
SS	Put decimal point ASCII code on stack
DPT	Sets YY depending on decimal point location
MV?	MV being measured
SIG	Test for sign
FDIG	Put value of first digit on stack
SDIG	Put value of second digit on stack
TDIG	Put value of third digit on stack
LDIG	Put value of last digit on stack
DT'2	Act if YY set to 0
DTE2	Act if YY set to 1
KONV	Convert M,N from BCD format to floating point
BCD	Take data and convert

4. ALGEBRA AND GRAPHIC WORDS

OF	Offset value of capacitance used
YX,YC,YG	Scaling factor for use with XDRAW, CDRAW, GDRAW corresponding to values in A064
K1,K2	Integer location reserved for storage of floating point value of data taken for Cox

C1,C2	As above but for actual values of Cox
J1,J2	As above but for data for Rs
R1,R2	As above but for actual value of Rs
F1,F2	As above but for value of frequency
P1,P2	As above but for value of calibration capacitor
FS	Store M,N (ie floating point number on top of stack) as frequency value
FREQ	Put F.pt. value of frequency onto stack
PP	Store M,N - F.pt. as calibration capacitor value
PF	Put calibration capacitor value on top of stack
YAXIS	N units along y axis
XAXIS	N units along x axis
ST	Compensate measured capacitance for stray capacitance
$/DATA	Take C(v),G(v) and store in memory
CG	Take capacitance and conductance voltage for Cox and Rs determination
KST	Store measured values of capacitance for Cox and Rs determination
JST	Store measured values of conductance for Cox and Rs determination
RSS	Store calculated values of Rs
COXS	Store calculated values of Cox
KRET	Put on stack measured value of capacitance
JRET	Put on stack measured value of conductance
Cox	Put on stack calculated value of Cox
Rs	Put on stack calculated value of Rs
OX	Get data and perform Cox, Rs compensation
DR	Plotting routine, shifts MSB of FPAC into N

HH	Plotting routine compensation for value of A064
CALC	Calculate GP
CALCUL	Calculate GP but compensate for Rs
CALIB	Calibrates computer so measurement made in Pf
ORIGIN	Sets pens to origin
STORE	Stores array of C(v),G(v) in block buffer
PLANT	Stores Cox and Rs at start of block buffer
RETR	Retrieves C(v) and G(v) arrays from buffer
DIGU	Retrieves Cox and Rs values
C(v)	Puts F.pt. value of capacitance for array value of V on stack
G(v)	Puts F.pt. value of conductance for array value of V on stack
SCAN	Scans x axis, accepts data and stores it
XDRAW CDRAW GDRAW	Draws appropriate curve out

APPENDIX2: PROGRAM LISTING

```
CODE POP.O .O LDX $ PUSHX JMP
CODE RETFPAC $ POPX JSR
        0 X A LDA A061 A STA 1 X A LDA A062 A STA
        2 X A LDA A063 A STA 3 X A LDA A064 A STA RTS
CODE FPOPRET $ POPX JSR
        0 X A LDA A069 A STA 1 X A LDA A06A A STA
        2 X A LDA A06B A STA 3 X A LDA A06C A STA RTS
CODE TSTFPAC $ POPX JSR
        A061 A LDA 0 X A STA A062 A LDA 1 X A STA
        A063 A LDA 2 X A STA A064 A LDA 3 X A STA RTS
CODE FPACST  $ POP JSR A061 B STA A062 A STA 17  A LDA
A064 A STA A CLR A063 A STA A060 A STA 32CB JSR RTS
CODE X10 317D JSR RTS CODE /10 319A JSR RTS
CODE ADD 3314 JSR RTS CODE SUB 339C JSR RTS
CODE DIV 345A JSR RTS CODE MUL 33A7 JSR RTS
CODE INP 3078 JSR RTS CODE OUT 31C9 JSR RTS :S
CODE INIT A CLR 800D A STA 800C A STA 800F A STA 800E A STA 35  CODE
CL A CLR A060 A STA A068 A STA RTS
: RETFPACS POP.O RETFPAC CL 2DROP ; : .. RETFPACS OUT ;
: FPOPRETS POP.O FPOPRET CL 2DROP ; : INTER RETFPACS FPOPRETS ;
: TSTFPACS 0 0 POP.O TSTFPAC ;       :   FPACST TSTFPACS ;
: +.  INTER ADD TSTFPACS ; : -.  INTER SUB TSTFPACS ; 0 INTEGER J
:X. INTER MUL TSTFPACS ; : /.  INTER DIV TSTFPACS ; 0 INTEGER Q : EX
2ROT RETFPACS DUP 4  IF 4 - -1 * 1 DO /10 LOOP ELSE
4 - 1 DO X10 LOOP THEN TSTFPACS ;      0 INTEGER OF 0 INTEGER YC
0 INTEGER K1 0 INTEGER K2 0 INTEGER C1 0 INTEGER C2 0 INTEGER Z
```

```
0 INTEGER J1 0 INTEGER J2 0 INTEGER R1 0 INTEGER R2 0 INTEGER V
0 INTEGER F1 0 INTEGER F2 : FS F1 !  F2 !  ; : FREQ F2 @ F1 @ ;
0 INTEGER P1 0 INTEGER P2 : PS P1 !  P2 !  ; : PF  P2 @ P1 @ ;
CODE YAXIS $ POP JSR 8014 B STA RTS  0 INTEGER YG 0 INTEGER YX



: C(V) 3600 V @ 2 * + @ KONV TSTFPACS OF @B  +.  PF X.  ST ;
: G(V) 3800 V @ 2 * + @ KONV /10 /10 TSTFPACS PF X.  -08 EX ; :S
: $DATA COND 5FF MSEC DVM CAP 5FF MSEC DVM 3600 J @B 2 * + !
3800 J @B  2 * + !  ; : SQ RETFPACS TSTFPACS TSTFPACS X.  ;
: CG COND 5FF MSEC BCD /10 /10 TSTFPACS CAP 5FF MSEC BCD TSTFPAC
S ; : KST K1 !  K2 !  ; : COXS C1 !  C2 !  ; : JST J1 !  J2 !  ;
: RSS R1 !  R2 !  ; : JRET J2 @ J1 @ PF X.  -08 EX ;
: KRET K2 @ K1 @ OF @B  +.  PF X.  ST ;
: OX CG KST JST JRET JRET X.  KRET /.  KRET +.  COXS JRET JRET JRET
 X.  KRET KRET X.  +.  /.  RSS ; : RS R2 @ R1 @ ; : COX C2 @ C1 @ ;
: DR A063 @B 7F LAND 1 LEFT A062 @B 80 LAND 7 RIGHT + ;
: CALL COX G(V) X.  G(V) SQ COX C(V) -.  SQ +.  /.  RETFPACS ;
: CALCUL G(V) C(V) C(V) X.  RS X.  -.  G(V) G(V) X.  RS X.  -.  COX X.
COX RS X.  C(V) X.  G(V) -.  SQ COX C(V) -.  COX RS X.  G(V) X.  -.
SQ +.  /.  RETFPACS ; : CALIB 03FD  3 EX CAP 5FF MSEC BCD TSTFPAC
S OF @B  +.  /.  PS ; : HH DUP A064 @B ¼ IF A064 @B
100 - ELSE A064 @B THEN - DUP 0= IF DROP ELSE RIGHT THEN ;
: ORIGIN 0 YAXIS 400 MSEC 0 XAXIS 400 MSEC ; :S :  FPACST TSTFPACS ;
20 ARRAY COE :  DR 3 HH ; DECIMAL
: C' 1754 3509 5263 7018 8772 10526 12281 14035 15789 1 9 DO COE
 I 2 * + !  -1 +LOOP ; HEX : /100 6 1 DO /10 LOOP ; 0 INTEGER J
```

```
: $DATA COND 5FF MSEC DVM CAP 5FF MSEC DVM 3600 J @B 2 * + !
3800 J @B 2 * + !  ; : O/P 3A00 V @ 4 * + RETFPAC TSTFPACS ;
: DIFF 0     9 I DO J @B 9 + I + V !  O/P J @B 9 +
I - V !  O/P -.  COE I 2 * + @ FPACST  /100 TSTFPACS X.  +.  LOOP ;
: SCANNER FF J !B INIT C' FF  I DO J @B 2DUP XAXIS V !  I - J !B
400 MSEC VDU?  IF ABORT   THEN $DATA CALCUL DR 0 HH OUT YAXIS
 2 SPACES     I 14    IF DIFF    OUT SPACE J @B I + .  THEN LOOP ;
: GDRAW A0 FF DO I XAXIS I V !  G(V) DR YG @B  HH YAXIS OUT .IS
-I +LOOP ; : GPDRAW F0 J !B F0 A0 DO J @B 2DUP XAXIS V !  I - J !
B O/P 2DROP DR YX @B  HH YAXIS  OUT .IS      LOOP ;
: CSRS COX C(V) -.  C(V) X.  COX X.  COX G(V) SQ X.  -.
 COX RS X.  C(V) X.  G(V) -.  SQ
 COX  C(V)  -.    COX  RS  X.    G(V)  X.    -.    SQ  +.    /.       ;
: SCS COX C(V) -.  C(V) X.  G(V) SQ -.  G(V) /.  CALCUL TSTFPACS X. ;
: SEMICAP CSRS CALCUL TSTFPACS COX X.  2    X.  -.  ;
```