## *Trapping effects in Cds devices*

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# TRAPPING EFFECTS IN CdS DEVICES

by

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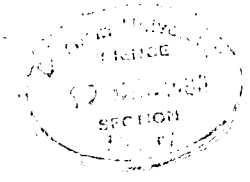
Presented in candidature for the Degree of

Doctor of Philosophy in the University of Durham



OCTOBER 1980

ACKNOWLEDGEMENTS

I would like to thank Professor G.G.Roberts and the S.R.C. for allowing me to use the facilities of the Applied Physics Department and providing finance for my work over three years.

I am especially grateful to my supervisor, Dr. J. Woods, for his valuable suggestions and helpful encouragement throughout my stay in Durham. I also wish to extend thanks to Dr. G.J.Russell for help with electron microscopy and enthusiasm in the many useful discussions on all aspects of this thesis ; to Mr. N. Thompson for the growth of crystals and a great amount of technical assistance, and to Mr. F. Spence and the staff of the workshop for their willingness to provide their skills and advice as and when required.

Finally, my thanks to my wife, Anita, for being understanding and patient throughout the time I have been writing this thesis, and for checking the typescript ; and to my parents for their constant encouragement throughout this work.

## ABSTRACT

In order to study the possible effect of interface states on the efficiency of the $CdS/Cu_2S$ heterojunction solar cell, the simpler structure of metal-on-insulator-on-CdS has been investigated. It has proved impossible to apply the theories appropriate to MIS devices on silicon, mainly because of the difficulties of producing a uniform oxide layer. However, a hypothesis has been put forward which is consistent with the experimental observations and which may be applicable to other results reported in the literature. The use of a scanning electron microscope (S.E.M.) particularly in the induced current mode, has allowed complementary investigations of surface properties to be carried out. The chemical preparation of a copper sulphide layer on CdS under different conditions is described and the various phases of $Cu_xS$ produced are identified. The optical and electronic properties of these devices have been investigated under two-beam illumination to excite trapping effects.

Further use of the S.E.M. with these structures has shown how useful this instrument can be in the analysis of semiconductor junctions. Finally, a number of conclusions relevant to the production of a more efficient cell are presented and a modified band structure model of the heterojunction is proposed.

CONTENTS

# CHAPTER 1

# HISTORY AND DEVELOPMENT OF PHOTVOLTAIC CELLS

## 1.1 Photoelectric Effects

The discovery that light could be converted directly into electricity dates back to 1839, when Henri Becquerel observed that when two electrodes were immersed in an ionic solution and one was illuminated, a potential difference was developed across them. This is known as the photoelectric effect. The first reference to a similar effect occurring in a solid was the observation in 1876 by Adams and Day in selenium.

In addition to this photovoltaic effect, there are two other photoelectric processes, namely the photoconductive effect and the photoemissive effect. The former requires that the electrical conductivity of the material increases when it is illuminated by light of a suitable wavelength. This effect was first discovered in selenium in 1873 by W. Smith. The effect also occurs in CdS where the absorption of light with sufficient photon energy causes the excitation of electrons from the valence band to the conduction band. As a result the free electron concentration is increased and aids conduction; the holes are quickly captured at defect or impurity centres leaving the electrons to make the major contribution to the conductivity. This will be seen later to have important consequences in the operation of the CdS/$Cu_2S$ heterojunction photocell which forms the major topic of this thesis.

A less important effect associated with photoconductive materials is the Dember effect. This is the production of a potential difference across a sample by non-uniform illumination. If light is incident normally on the surface of the photoconductor, it will produce electron-hole pairs, which will diffuse into the non-illuminated bulk. Since in

a material such as CdS, the electron mobility is much greater than the hole mobility, the electrons will proceed further until sufficient field is set up to oppose continued motion. Thus with a suitable contact geometry, a Dember voltage may be measured. The effect may usually be neglected; in Ge for example, it may be ~ 0.01 V.

The photoemissive effect was discovered by Hertz in the course of his work on L-C circuits in 1887. He found that a spark jumped a gap more readily when the negative electrode was illuminated by a spark from another coil. Further work established that it was the ultra-violet radiation in the spark that affected the cathode. Hallwachs demonstrated that negative charge was emitted from the cathode under U-V illumination and Lenard later showed that the charge consisted of electrons. The first photoemissive cell was produced by Elster and Geitel in 1895. Subsequent work has led to the development of the more sensitive photoemissive materials which are used in the photomultipliers and television camera tubes of today.

### 1.1.1 Photovoltaic Effect

The search for an explanation of the photovoltaic effect continued in the 20th century with the discovery by Grondahl (1927) and Lange (1936) of an e.m.f. generated across the contact between copper and copper oxide. Schottky (1930, 1931) was able to clarify this phenomenon. In spite of such an early discovery it is only in the last 25 years that serious attempts have been made to exploit the photovoltaic effect, namely in the conversion of solar radiation into electricity. Before this, probably the most important application of the effect was in selenium p.v. cells for exposure meters in photography. This is because the materials technology has not hitherto been available for the production of the large slices of high purity semiconductor required for efficient

photovoltaic conversion. To produce a photovoltage, the electrons and holes generated by light in the semiconductor must be physically separated by an inhomogeneity such as the internal electric field that occurs at a metal-semiconductor junction or a p-n junction. Thus a current can be made to flow simply by connecting a load externally between the p- and n-type regions while the junction region is illuminated.

Photocells whether photoconducting or photovoltaic have been used for many years in applications such as intruder alarms, industrial controls, and conveyor belts, where a person or object breaks a light beam irradiating the cell; in all these examples, the cells are used as light-operated switches.

## 1.2 Importance of Photovoltaic Cells

The 'space-age' is certainly one of the major factors promoting recent interest in photovoltaic cells as direct energy convertors rather than as mere energy sensors. The conception of satellites circling the earth would be totally impractical without some light-weight power source which will last almost indefinitely without maintenance. Photovoltaic solar cells were the obvious answer and much money has therefore been poured into their development, especially by the U.S.A.

At the same time, the western world has been awakening to the fact that with ever-increasing energy demands (at something like an exponential rate), our fossil fuel supplies are unlikely to last for ever. Current estimates show that supplies of oil and natural gas will run out within 30-40 years, and of coal in little more than a century. The implications of this on life, as we know it today, are colossal, and it is frightening that so little is being done in researching alternative energy sources.

The two most important alternative energy sources are nuclear power and solar power. The former has the disadvantage of its waste disposal and latent radiation, and therefore environmentally the latter must be the more favourable. Photovoltaic cells are just one of many types of solar energy converter, but they have the advantage of converting solar radiation directly into electricity - probably the most useful form of energy.

In the shorter term, interest in terrestrial solar cells has focussed on their potential to contribute to the development of the third world. A recent conference on 'Solar Energy for Development' in 1979 discussed its use in the provision of water, power production and heating and cooling, (Palz, 1979). Solar electricity is attractive for such applications, even if it is dearer per watt than conventionally generated supplies because of its flexibility ; it requires less maintenance, no fuel supplies and no transmission lines. Even a small photovoltaic generator, which in a western home would be of no importance, can provide electricity to operate a television set, bringing education and literacy to a whole village. Such provision has been successfully made in Nigeria and the Ivory Coast and other African countries. Other obvious examples are in pumping drinking water, providing telephones and lighting.

## 1.3 Costs and Efficiencies

Photovoltaic power for development is currently cost-competitive in the pure economic sense for small applications up to a few kW in remote regions, however because of limited resources in the third world, it is crucial that prices reduce rapidly in the coming years. This is also important for the west, because the lower the price per watt, the more interest will be shown in photovoltaic cells and the sooner they can take over from the dwindling fossil fuels.

A background of costs and relative efficiencies of different photovoltaic materials, and projections into the future was provided by Rappaport and Magid at the 1979 Photovoltaic Solar Energy Conference in Berlin, and will be summarised here. The present (1978 figures) annual volume of solar cell energy is in excess of 1 MW and mostly due to silicon cells. The cost of an installed system is between $20 and $40/Watt, although the cost of the cell array alone is only $7 - $15/Watt; consequently there is a need not only to reduce device costs but also systems costs. Figure 1.1 shows a graph of projected costs, the goal of $0.10 - $0.30/Watt is calculated to make solar electricity directly competitive with conventional power station generated electricity. Prospects for various types of solar cell are shown in Table 1.1.

| Array Technology | Goal (1975$) | Prospect |
|---|---|---|
| Si Flat Plate:<br>Si Czochr. single crystal<br>Si Semicrystalline Sheet<br>Si Ribbon and sheets<br>Si Amorphous Layers | $\leqslant$ \$500/kW (1986) | Excellent |
| Concentrator:<br>Si<br>GaAs<br>Total Energy | $\leqslant$ \$500/kW (1986) | Very Good |
| $CdS/Cu_2S$ thin film | $\leqslant$ \$500/kW (1986) | Very Good |
| Other thin films:<br>GaAs, $InSnO_2/Si$, CdTe etc. | \$100-300 kW | Very Promising |

Table 1.1

Figure 11 Solar energy price goals and history (after Koppelman and Magid, 1979)

Present efficiencies of different types of thin film solar cells are:-

| | | |
|---|---|---|
| (1) | $CdS/Cu_2S$ | 9% conversion efficiency. By the addition of Zn to CdS, cells have the potential for exceeding 10% by 1980. |
| (2) | GaAs | High single crystal efficiencies $\sim$ 20% have been obtained |
| (3) | Polycrystalline Si | 9% |
| (4) | $InSnO_2/Si$ | 12% on single crystal Si |
| (5) | Amorphous Si | 6% has been attained |
| (6) | $CdS/CuInSe_2$ | 6.7% evaporated cell, improved lattice match compared to $Cu_2S/CdS$ |
| (7) | CdS/InP | 14% on single crystal. |

The reason why these particular materials have been chosen for solar cells will become clear in what follows.

## 1.4 Choice of Semiconducting Material

One important point in the material selection which might appear obvious is that the cost, in terms of energy, of producing a cell, must be considerably less than the energy that cell will produce during its lifetime. This is crucial for silicon single crystal cells, because growing silicon by the Czochralski technique is very 'energy-intensive'. The elements of the material for solar cells clearly must be in great abundance upon the earth's crust. In addition to these considerations the factors affecting the choice of a photovoltaic material are:-

1. The band gap of the material must be chosen properly. The larger the band gap, the less light is usefully absorbed as most light with $h\nu < Eg$ is transmitted. However the smaller the band gap, the lower the conversion efficiency of short wavelength light, since the absorption of any photon of energy, $h\nu > Eg$ only creates useful electrical energy of Eg, the remainder being wasted as heat from intra-band transitions. In other words, the maximum internal barrier is lower, resulting in a reduction in achievable open circuit voltage. Clearly the band gap of the material has to be matched in some way to the radiant energy distribution of the sun shown in Figure 1.2. This diagram also shows the proportion of the energy usefully absorbed by several semiconducting materials. Calculations of theoretical efficiency for solar energy conversion as a function of band gap (Loferski 1956, Wysocki and Rappaport 1960 and Wolf 1960) have shown that materials with band gaps between 1.25 eV and 1.5 eV are optimal with theoretical conversion efficiencies of 24%. This would suggest that silicon with a band gap of 1.1 eV would not be ideal for a solar cell. However, silicon technology is far more advanced than that of any other semiconductor so that what the material lacks in optimum theoretical match, at present can be more than satisfied by technology. Indium phosphide with a band gap of 1.27 eV and GaAs (1.34 eV) would appear to be promising materials as they have a high mobility, about four times that of silicon. Unfortunately, preparation of III-V materials is difficult and so far only 'concentrator' systems have proved viable. (A concentrator system is essentially one where sunlight is focussed by lenses on to a small area device). The considerations described above would suggest that CdS with a band gap of 2.4 eV would be unsuitable as the basis for a solar cell. This is true, but it must be remembered that the useful light absorption occurs in the p-$Cu_2S$ side of the heterojunction and the band gap of $Cu_2S$ is $\sim$1.2 eV.

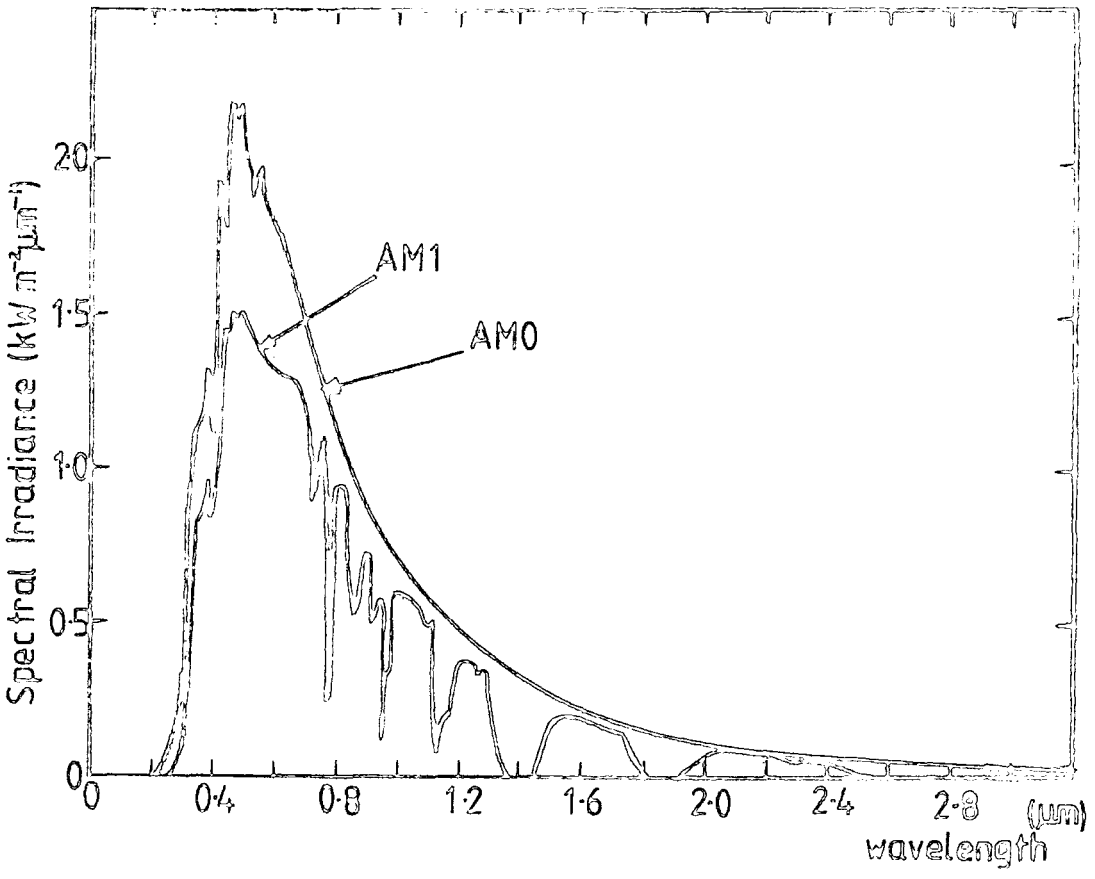



Figure 1.2(a) Energy distribution of sun

AM0-Distribution outside atmosphere
AM1-Distribution at sea level

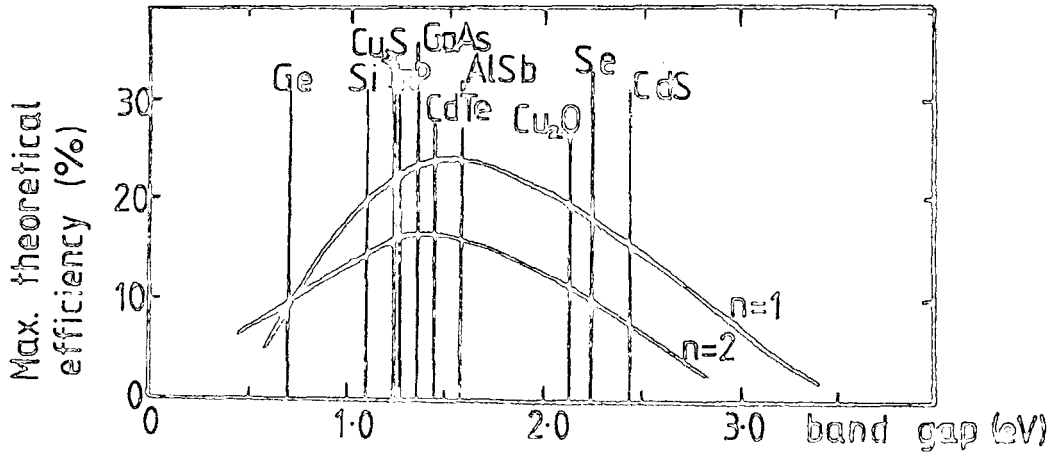



Figure 1.2(b) Proportion of sun usefully absorbed by semiconductors

(n=diode ideality factor)

2. The semiconductor must have a high optical absorption coefficient in order to absorb the maximum amount of solar radiation.

3. Ideally the whole spectrum of sunlight should be used to create electron-hole pairs.

4. All electron-hole pairs produced should be collected at the junction, i.e. all electron-hole pairs should be created within one diffusion length from the junction.

Also the following more general points should be satisfied by a cell:

(a) Reflection losses at the top surface should be a minimum.

(b) The internal series resistance should be minimal.

(c) The fill factor (sometimes known as the curve factor, see Figure 1.3) defined as the ratio of power at the maximum power point to the product of open circuit voltage and short circuit current, should be a maximum.

(d) For space use especially, the cell should be resistant to radiation damage.

## 1.5 Type of Cells

There are three basic types of photovoltaic device, having both advantages and disadvantages, which with different materials can satisfy some of the above conditions. These are p-n homojunctions, heterojunctions or metal-semiconductor cells.

### 1.5.1 Homojunctions and Heterojunctions

Cells based on homojunctions are limited to materials which can be made both n- and p-type. However it can be an advantage to use a heterojunction which has materials with different properties on either side of the junction. Thus light should be absorbed by a material with band gap of 1.25 - 1.5 eV then if the other material is chosen to have a wide band

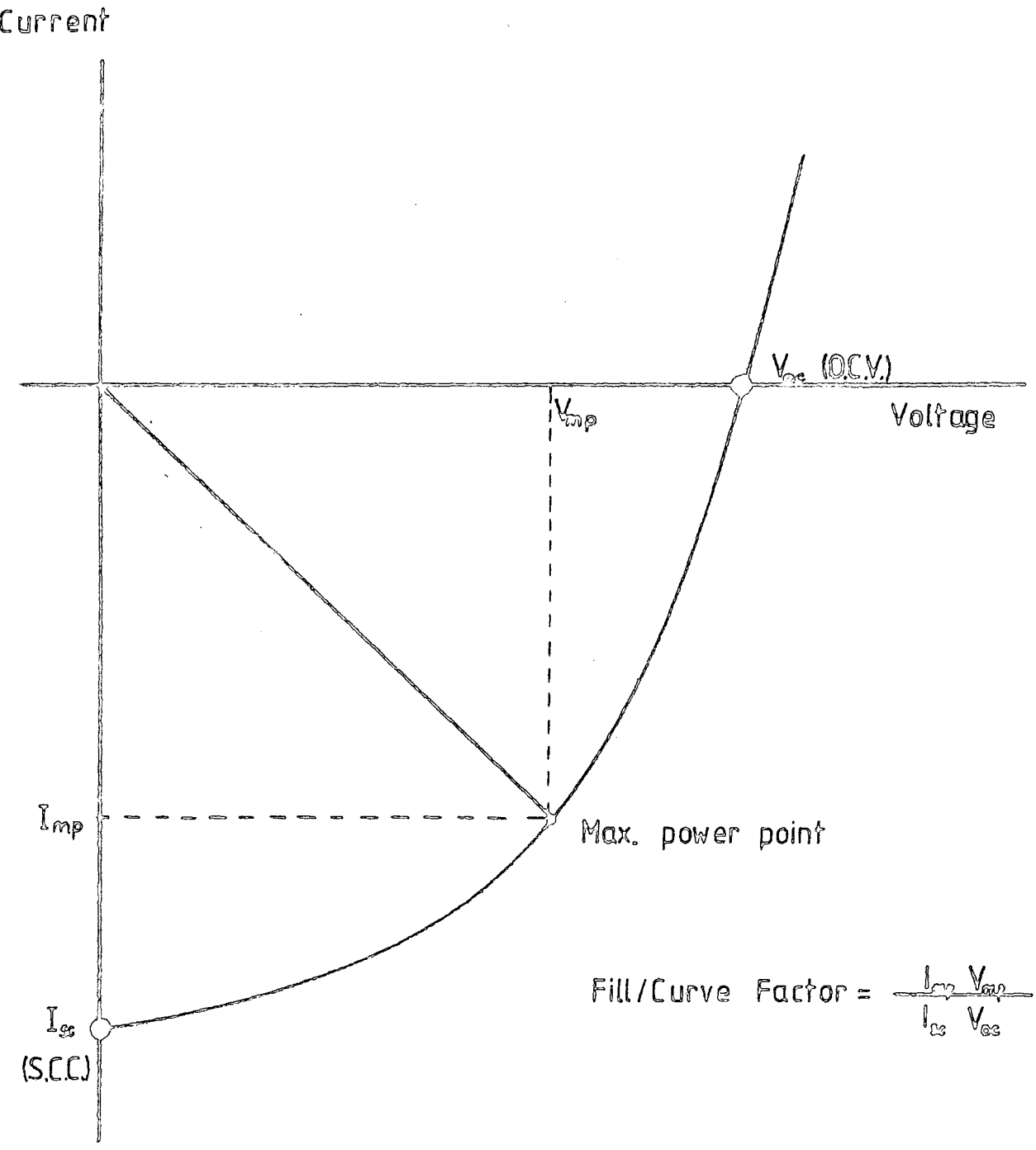



Figure 1.3 Definition of Fill/Curve Factor

gap, the device may be operated in the 'back-wall' configuration, i.e. illuminated through the high band gap material and the light will be absorbed close to the junction. Additionally in a homojunction the top layer is usually made by diffusing dopants into a region already doped in the opposite manner, and this leads to a region with low minority carrier lifetime and hence poor collection efficiency.

A disadvantage of the heterojunction is that because it consists of two different materials there will be, inevitably, stress due to mismatch of the two crystal lattices. This will create recombination centres at the junction with consequent lowering of efficiency.

### 1.5.2 Schottky Cells

The metal-semiconductor or Schottky barrier cell (and more recently the M.I.S. cell (Fonash 1976) has the advantage of ease of preparation, since it does not require diffusion processes to be carried out at elevated temperatures as the other two do.

From these considerations, the most promising cell to emerge to date is the polycrystalline silicon p-n junction device for which efficiencies of 9% have been achieved, and the CdS/$Cu_2S$ heterojunction cell, consisting of a polycrystalline layer of CdS, $\sim$ 30 μm thick deposited on plastic or glass. The surface of the CdS is converted to a layer of $Cu_2S$ $\sim$ 1 μm thick by a chemical exchange reaction. Such a cell may have an efficiency of 9% and is cheap to prepare. Amorphous silicon is the most recent material to show promise for the construction of inexpensive cells in large quantities. Assuming the present figure of 6% efficiency can be improved by further research, these may well provide the cells of the future.

## 1.6 The CdS/$Cu_2S$ Solar Cell

The original observation of a photovoltaic effect on CdS was made

when a copper contact was illuminated (Reynolds et al 1954) and since then a great deal of effort has been put into improving the efficiency of the cell and increasing the understanding of the physical processes involved. Williams and Bube (1960) observed a voltage in cells where the copper was deposited electrolytically on to CdS, and suggested it was due to electron emission from metal into semiconductor. Alternatively, Woods and Champion suggested that a high concentration of copper diffused into the CdS and produced a p-type region in the CdS, thus creating a p-n junction photovoltaic effect. Hall measurements showed that the hole conduction was via an impurity band. This idea was supported by Grimmeis and Memming (1962). Since copper has a limited solubility in CdS, however, the hole conductivity must have been associated with a separate phase of copper sulphide (Te Velde 1967). This was later demonstrated by electron diffraction measurements (Cook et al 1970). Hall measurements showed that copper sulphide was p-type with a mobility at room temperature of 2 $cm^2/V$ sec, and a hole concentration of $10^{20}/cm^3$.

In 1966, N. Duc Cuong and J. Blair produced a photovoltaic cell by evaporating copper on to low resistivity single crystal CdS. They found that the spectral response of the cell in the infra-red was enhanced by two orders of magnitude under simultaneous illumination with green light (band gap). They suggested that this was due to the creation of extra minority carriers by excitation of electrons from the valence band to impurity states in the CdS.

Thin film cells were prepared by Chamberlain and Skarman in 1966 by a spray technique. They used an aqueous solution of cadmium chloride and thiourea, which was sprayed on to a heated glass substrate coated with tin oxide. A solution of copper sulphide was then sprayed on at room temperature. The CdS in this device was only 2 μm thick, and the cell gave efficiencies of ~4%. This is a very promising technique for the mass

production of cheap cells. The photovoltaic effect in these cells owes its origin to the field at the heterojunction of the copper sulphide and the cadmium sulphide.

## 1.7 Theory of the $CdS/Cu_2S$ Device

Mytton in 1968 made cells by chemically plating $Cu_xS$ on to CdS. He measured their spectral responses as a function of the plating concentration and time. His results indicated that the intrinsic response of the cell depended on both the concentration and the dipping time in the plating solution. On the other hand, the extrinsic CdS response was largely unaffected by the dip time and dependent only on concentration. Mytton, therefore, suggested a band structure for the cell in which the junction was not abrupt, but consisted of a transition from p-$Cu_2S$ through photoconducting (high resistance) Cu-doped CdS to n-type CdS. This model is similar to those suggested by Keating in 1965 and Bockemuehl et al in 1961.

A more detailed version of this model, the Clevite Model, was proposed by Shiozawa et al in 1967, following detailed considerations of the measured electrical, optical and structural properties of a large number of cells. Other models suggested for the $CdS/Cu_2S$ cell include the Harshaw Model by Hill and Keramidas, 1966 ; the Lewis Model by Potter and Schalla, 1967; and the E.S.R.O. model by Van Aershodt et al, 1968; all contain common features but differ in the details of the shape of the potential energy barrier at the $CdS/Cu_2S$ junction.

Gill and Bube, 1970, suggested a model in which the central feature was hole trapping at deep imperfection centres in CdS near the junction to account for experimental evidence of quenching and enhancement of the photoresponse under secondary illumination. In their model a spike exists

in the conduction band at the interface. Electrons diffusing across the junction have to tunnel through this spike and the tunnelling probability is controlled by the occupancy of the deep lying acceptor states (see Figure 1.4). In 1972 Lindquist and Bube carried out photocapacitance measurements on the CdS/$Cu_2S$ junction, which they interpreted as supporting their original hypothesis. The acceptor levels were attributed to copper diffused into the CdS during junction manufacture.

### 1.7.1 Te Velde Model

An important feature of the CdS/$Cu_2S$ cell is that it is usually considered necessary to bake a cell in air at 200$^{o}$C for 2 minutes or so before optimum efficiency is achieved. Te Velde (1973) made a mathematical analysis of the CdS/$Cu_2S$ heterojunction and concluded that while copper does diffuse into the CdS, the main effect of the sensitising heat treatment is to allow the diffusion of oxygen to the junction interface, where it forms electron traps. As this takes place, the barrier between the $Cu_2S$ and CdS increases so that it is possible that a conduction band spike forms at the junction. If the barrier is low, i.e. there is a 'notch' in the conduction bands at the interface, then the open circuit voltage (O.C.V.) of the cell will be low, although the short circuit current (S.C.C.) may be good. If, on the other hand, there is a sizeable spike at the junction, then the O.C.V. will have reached a maximum, but the short circuit current will be small as a result of the poor collection efficiency of electrons flowing from the $Cu_2S$ into the CdS. The optimum heat treatment according to Te Velde is therefore one which leads to practically no discontinuity of the conduction bands. This theory fits well qualitatively with what is observed experimentally for the variation of O.C.V. and S.C.C. as the length of heat treatment in air is increased.

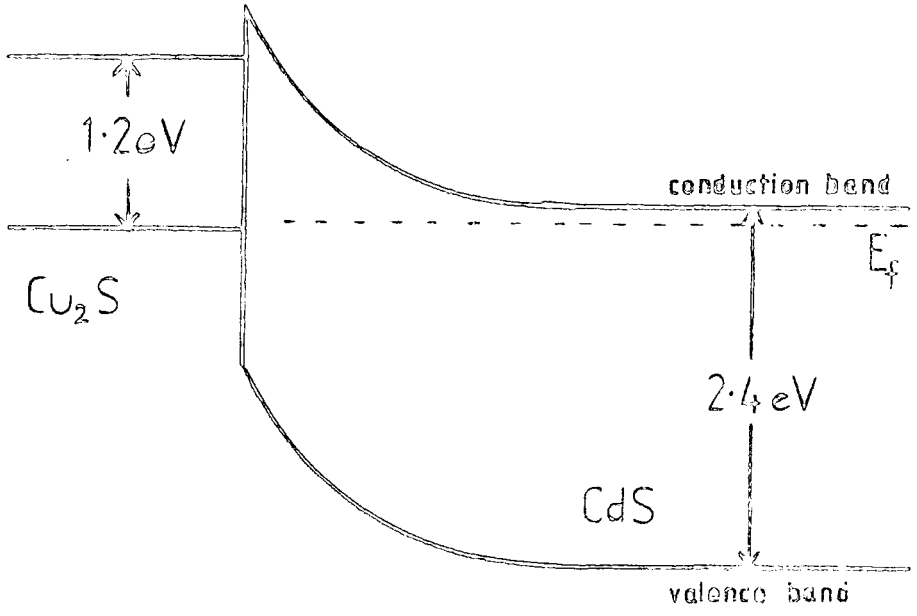



Fig.1.4 Model of $CdS/Cu_2S$ Heterojunction Band Structure (after Gill & Bube, 1970)

1.7.2 Clevite Model

The Clevite model is probably the most comprehensive yet proposed, and hence it will be described in some detail (see Figure 1.5), since it forms the basis for much of the later discussion. The basic assumptions on which the model is based are:

(1) Gold makes an ohmic contact to p-$Cu_2S$, and ZnAg is used as a substrate and makes an ohmic contact to n-CdS.

(2) Almost all the useful light absorption takes place in the thin layer of p-$Cu_2S$. Thus, the spectral response of the cell corresponds to the intrinsic absorption spectrum of $Cu_2S$, modified by the photoconductive response of the insulating CdS, (i-CdS).

(3) The i-CdS layer results from Cu diffusion during cell fabrication. This layer which is insulating in the dark is photoconductive and its resistance is therefore reduced when the cell is illuminated with sunlight. The quasi-Fermi level for electrons moves upwards during illumination and the layer becomes weakly n-type. It has the photoconductive properties of Cu-compensated CdS.

(4) When illuminated, the main junction in the cell occurs between $Cu_2S$ and i-CdS. The barrier height is then about 0.85 eV.

(5) In the dark, the principal junction occurs between the i-CdS and n-CdS. The barrier height is about 1.2 eV. A small junction of reversed polarity with barrier height of 0.35 eV occurs between the $Cu_2S$ and i-CdS.

(6) The interface states at the p-$Cu_2S$:i-CdS junction are mainly responsible for the recombination which occurs under forward bias conditions.

When the cell is illuminated by light of energy less than 1.2 eV, the photons pass through the $Cu_2S$, through the CdS and are absorbed or reflected by the ZnAg layer. With photons of energy between 1.2 eV and 2.4 eV, absorption takes place, but this is not complete as $Cu_2S$ has an indirect band gap at 1.2 eV, i.e. absorption must be phonon assisted. Because of

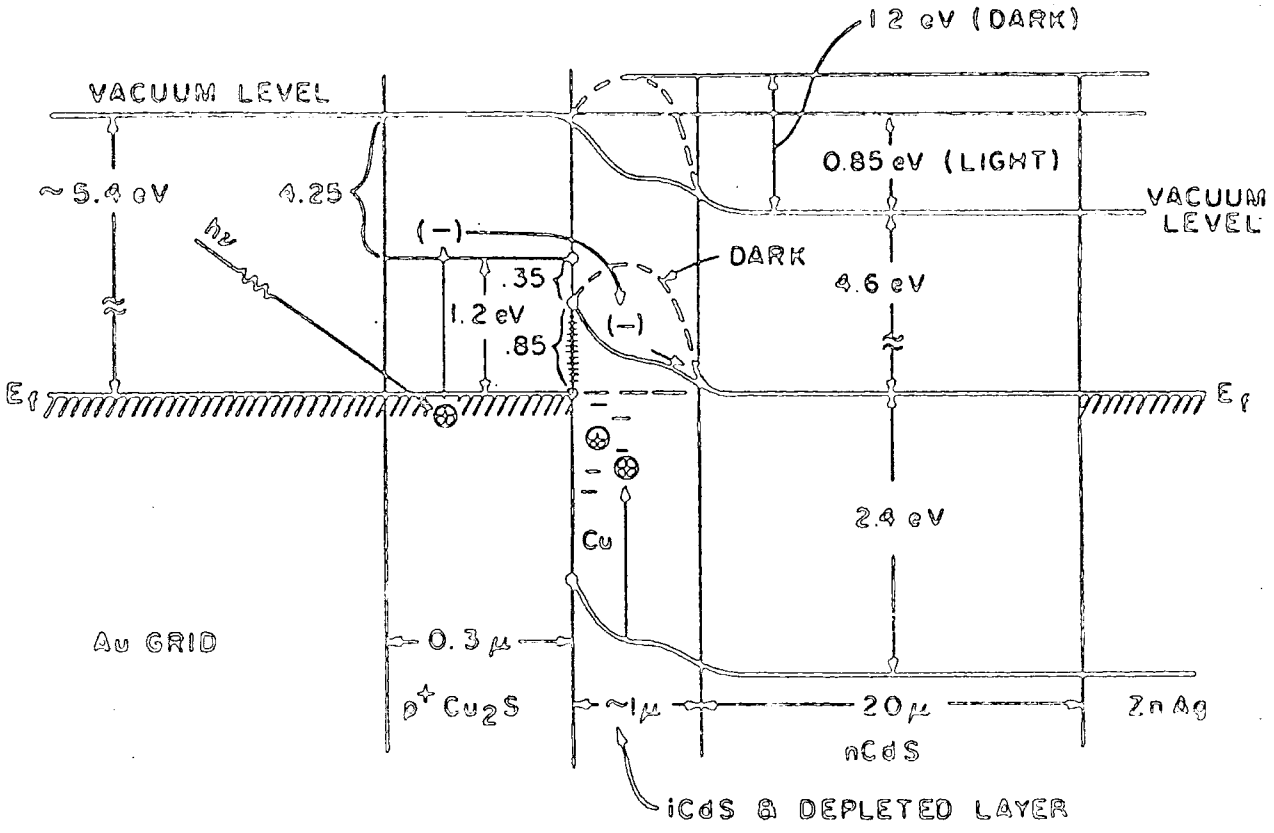



FIG. 1·5 ENERGY BAND DIAGRAM FOR $Cu_2S$-CdS SOLAR CELL UNDER ILLUMINATED SHORT CIRCUIT CONDITIONS (CLEVITE MODEL)

the combination of this and the small thickness of $Cu_2S$, $\sim 0.3$ μm, some photons with energy between 1.2 eV and 2.4 eV, reach the i-CdS layer where they make it photoconducting, i.e. weakly n-type. Photons with energies greater than 2.4 eV are absorbed in the $Cu_2S$ layer. The greater the photon energy, the closer the absorption takes place to the surface illuminated.

The photons absorbed in the $Cu_2S$ layer create electron-hole pairs. The electrons, in spite of being minority carriers have a relatively long lifetime because of the indirect band gap. Consequently, they can diffuse to the $Cu_2S$/CdS junction where they are collected by the junction field and transported into the n-CdS, whence they reach the ZnAg contact. The corresponding photoexcited holes meanwhile drift towards the gold contact where they are annihilated by incoming electrons. Recombination occurs in the bulk of the $Cu_2S$, but chiefly at the interfaces, due to recombination centres. Thus photons of energy greater than 2.4 eV which are absorbed near the front surface are unlikely to contribute to the photocurrent. Hence the diminished response of the cell to high energy radiation.

### 1.7.3 Experimental Evidence

Some of the experimental evidence which supports the existence of the Cu-compensated i-layer is as follows:

(1) The enhancement of the red part of the spectral response by simultaneous illumination with green (band gap of CdS) light.

(2) The diminution of the green portion of the spectral response by an infra-red biasing light (quenching of photoconductivity).

(3) The appearance of the above two effects only after the sensitising heat treatment of cells which indicates that the i-layer is formed by copper diffusion.

(4) The decrease in cell capacitance by the heat treatment .

(5) Enhancement of the spectral response at longer wavelengths by doping the n-CdS layer with indium. The photoconductive response of In-doped, Cu-compensated CdS extends to much longer wavelengths.

(6) The cross-over of the dark and light I-V characteristics associated with the photoconductive effect in the i-CdS layer. No cross-over occurs in silicon cells.

(7) The growth of the i-CdS with heat treatment results in a loss of tunnelling and shunting paths at the junction and consequently improves the 'squareness' of the I-V curves.

(8) The series resistance of cells heated in vacuum or inert gas increases irreversibly. This effect is due to the growth of the copper i-layer by diffusion, and can be reduced by donor doping.

## 1.8 Stability and Degradation

In the assessment of the practical use of a cell, the stability and degradation are major factors. Therefore, in recent years, a large amount of money has been spent on life-testing cells in hostile environments, such as desert conditions with extremes of temperature. These experiments are not only designed to test the performance of the cell itself, but also of the packaging, anti-reflection coatings etc.

The $Cu_2S$/CdS heterojunction is subject to a number of degradation mechanisms (W. Palz et al, 1970, 1973; Mytton et al, 1972; Shiozawa et al, 1969).

(1) The polycrystalline surface is reactive with oxygen in the atmosphere.

(2) The existence of other phases of copper sulphide besides $Cu_2S$ (chalcocite) presents possibilities for degradation.

(3) The mobility of $Cu^+$ as an ion in $Cu_2S$ is a mechanism for ionic segregation when a potential difference is developed across the $Cu_2S$.

(4) Cu diffusion into CdS provides another mechanism for degradation,

migration occurring via $Cu^+$ vacancies. The diffusing copper leads to the growth of the i-CdS layer which results in increased series resistance of the cell. This effect can be reduced by the introduction of donors into the CdS.

The composition of the copper sulphide layer affects the spectral response of the short circuit current and open circuit voltage and their magnitudes vary considerably (Palz et al 1972). This will be discussed in greater detail later. The quantum efficiency of cells with orthohombic chalcocite ($Cu_2S$) layers is the highest, but is reduced as the composition of the copper sulphide is changed by chemical reaction with the atmosphere.

Copper sulphide can also exist as $Cu_{1.96}S$ (Djurleite), and $Cu_{1.8}S$ (Digenite). In addition, there is at least one hexagonal phase of $Cu_xS$ where x is nearly 2 (Cook et al 1970). X-ray studies by Shiozawa et al (1969) have revealed that typical degradation accompanies a change from Cu-rich to Cu-deficient copper sulphide due to oxidation. This causes a reduction in the short circuit current. Studies of the output from cells prepared with different $Cu_xS$ compositions show that there is a gradual decrease in S.C.C. as x decreases, exactly the same as with ageing. The best results are obtained when $x = 2.0$, i.e. when the copper sulphide layer is composed of chalcocite.

Degradation is enhanced at higher temperatures and different effects occur in vacuum and in air. In vacuum, the series resistance of the cell increases, as expected, since the resistivity of semiconducting n-CdS increases after heating in vacuum. Heating in air, conversely, oxidises the copper sulphide and lowers the S.C.C. while leaving the series resistance substantially unaltered.

Various means of reducing the effects of the various degradation mechanisms have been reported, e.g. by doping the CdS (Palz et al, 1973), or using a special etch solution (Mytton et al, 1972) or depositing excess copper (Bogus and Mattes, 1972) to act as a 'reservoir' when

degradation mechanisms attempt to reduce the copper concentration of the $Cu_xS$.

In this thesis, the conditions under which the various phases of copper sulphide can be prepared on cadmium sulphide will be discussed, as will their effect on the spectral response of the cell. Post-deposition phase changes will also be discussed. The possible role of interface states at the junction of the heterojunction will also be described following work on Metal-Insulator-Semiconductor devices on CdS. A modified model of the band structure of the heterojunction following the sensitising heat treatment has been developed to explain the spectral response of the O.C.V., S.C.C. and photocapacitance of devices with and without bias illumination. In addition, studies on electron barrier effects in II-VI semiconductors made with a scanning electron microscope will be discussed.

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# CHAPTER 2

# BASIC THEORY OF SCHOTTKY AND MIS DEVICES

## 2.1 Introduction

As previously mentioned, interface states at the $CdS/Cu_2S$ boundary are thought to lower the efficiency of the solar cell by acting as recombination paths for free holes and electrons. They are also likely to control or affect the magnitude of the barrier height and hence the value of open circuit voltage (O.C.V.). Part of the work reported in this thesis has therefore been carried out in an attempt to investigate their properties with the ultimate aim of reducing their density, or at least decreasing their effects on efficiency.

Because the $CdS/Cu_2S$ heterojunction is a very complex device, it was anticipated that effects other than those directly concerned with interface states might obscure the experimental observations. Therefore, in an initial preliminary study, Metal-Insulator-Semiconductor (MIS) structures were fabricated on CdS, and measurements of their properties were made in the hope that these structures would prove simple to interpret. The theoretical basis of that work is outlined in what follows.

## 2.2 Metal-Semiconductor Contact

When a metal is brought into intimate contact with a semiconductor and thermal equilibrium is established, the Fermi levels of the two materials must be coincident. In general, for this to happen, there must be a transfer of charge between metal and semiconductor. If the work function of the metal is $\phi_m$ and that of the n-type semiconductor is $\phi_s$, and $\phi_m > \phi_s$ then a flow of electrons from the semiconductor to the metal will occur. This results in a bending of the semiconductor bands at the interface, as shown in Figure 2.1. In the absence of surface states, the amount of band bending simply accommodates the difference between the two

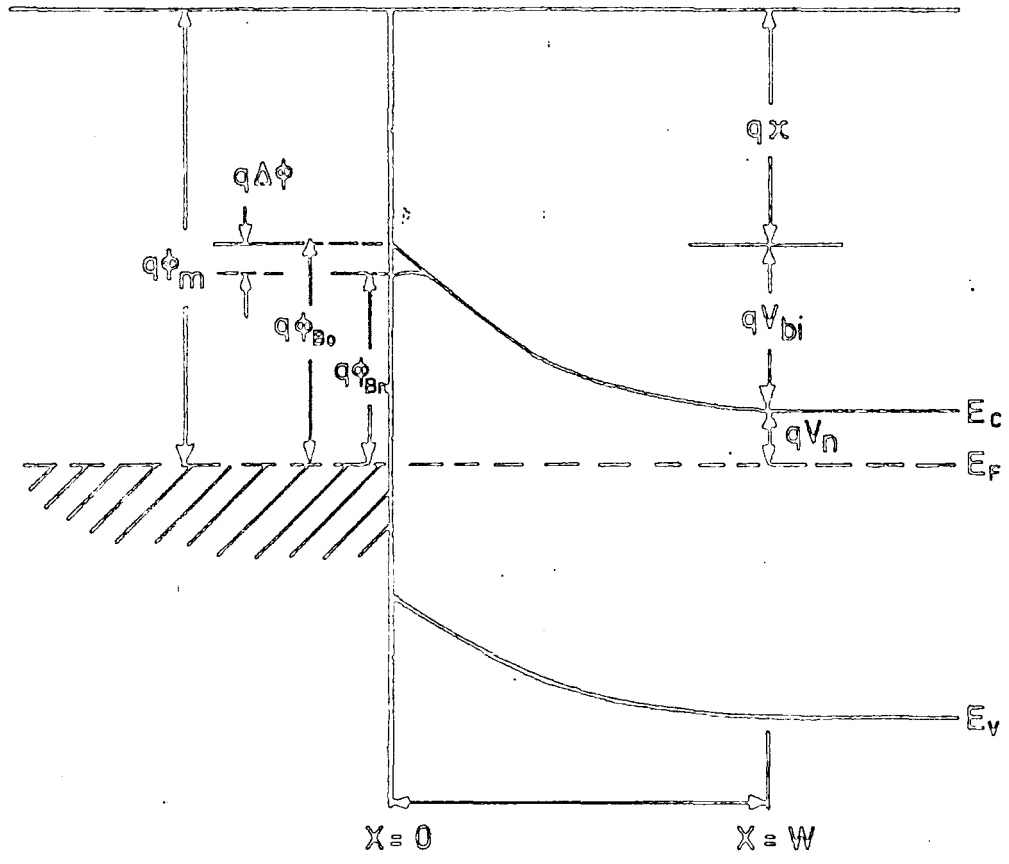



FIG. 2.1 ENERGY BAND DIAGRAM OF A METAL-n-TYPE SEMICONDUCTOR CONTACT

work functions. This potential difference, $q\phi_m - q(\chi + V_n)$ is known as the contact potential, where $q\chi$ is the electron affinity of the semiconductor measured from the bottom of the conduction band to vacuum level, and $qV_n$ is the energy difference between the Fermi level and the conduction band in the bulk. If Schottky barrier lowering and the possible presence of an interfacial layer are neglected, the barrier height is given by:

$$q\phi_{Bn} = q(\phi_m - \chi) \qquad (2.1)$$

In the presence of a large number of surface states, when the interfacial layer is thin, a small change in band bending would be accompanied by a large alteration in charge, because the surface states will be in equilibrium with the metal. Thus they would tend to pin the barrier relative to the Fermi level in the metal, the barrier height being determined by the surface states independently of the metal work function. With an interfacial layer thicker than $\sim 30$ Å the surface states are in equilibrium with the semiconductor (Card and Rhoderick 1971). As the thickness of interfacial layer increases, the device behaves less like an ideal Schottky diode; the case of an MIS diode will be discussed later. In what follows an ideal contact is considered between a metal and a uniform n-type semiconductor. For simplification, it is assumed that the charge density, $\rho$, in the semiconductor is given by $\rho = qN_D$ ($N_D$ = donor doping density) for $x < W$ and $\rho = 0$ for $x > W$ ($W$ = depletion width). Integration of Poisson's equation with these boundary conditions yields

$$V(x) = \frac{qN_D}{\varepsilon_s}\left(Wx - \tfrac{1}{2}x^2\right) - \phi_{Bn} \qquad (2.2)$$

Electric field

$$|E(x)| = \frac{qN_D}{\varepsilon_s}(W - x) \qquad (2.3)$$

Depletion width

$$W = \left[ \frac{2\varepsilon_s}{qN_D} \left(V_{bi} - V - \frac{kT}{q}\right) \right]^{\frac{1}{2}} \tag{2.4}$$

Here $\varepsilon_s$ is the permittivity of the semiconductor, $V_{bi}$ is the diffusion potential at zero bias, and $\frac{kT}{q}$ arises from the kinetic energy of the mobile charge carriers. The space charge $Q_{SC}$ per unit area, assuming total ionisation of the donors and the depletion capacitance per unit area are given by

$$Q_{SC} = qN_D W = \left[ 2q\varepsilon_s N_D \left(V_{bi} - V - \frac{kT}{q}\right) \right]^{\frac{1}{2}} \tag{2.5}$$

and

$$C = \frac{\partial Q_{SC}}{\partial V} = \left[ \frac{q\varepsilon_s N_D}{2\left(V_{bi} - V - \frac{kT}{q}\right)} \right]^{\frac{1}{2}} = \frac{\varepsilon_s}{W} \tag{2.6}$$

Thus the depletion layer capacitance is voltage dependent, and inversely proportional to the depletion width, similar to an ordinary parallel plate capacitor. Equation (2.6) may be written more usefully as:

$$\frac{1}{C^2} = \frac{2\left(V_{bi} - V - \frac{kT}{q}\right)}{q\,\varepsilon_s\,N_D} \tag{2.7}$$

Providing that $N_D$ remains constant throughout the depletion width, a plot of $\frac{1}{C^2}$ against V should produce a straight line, the voltage intercept of which gives the diffusion potential $V_{bi}$ while the gradient yields the donor density, $N_D$. If there are electron traps present in the depletion layer, then when a large reverse bias is applied to the diode, and the Fermi level drops relative to the semiconductor bands, some traps will empty. Depending on whether or not the trap concentration is large compared with the donor density, a plot of $\frac{1}{C^2}$ against bias will be either a straight line or have a downward concave curvature (Goodman 1963).

## 2.3 Conduction in Schottky Diodes

The normal means of forward conduction in an n-type Schottky diode is by transport of electrons from the semiconductor over the barrier into the metal. There are other processes which can occur, and these cause the deviations from ideality which are found in real diodes. Henisch (1957) gives a summary of the early work in this field. Some examples of the mechanisms are (i) injection of holes into the neutral region of the semiconductor (Green and Shewchun 1974), (ii) recombination of holes and electrons in the depletion region of the semiconductor via recombination centres (Yu and Snow 1968), and (iii) quantum mechanical tunnelling of electrons through the barrier (Padovani and Stratton 1966).

Several theories have been proposed to explain conduction over the barrier. The first of these, known as the diffusion theory, was put forward by Wagner (1931) and by Schottky and Mott (1939). In 1942 the thermionic emission theory was proposed by Bethe. This suggests that conduction occurs by the thermal emission of electrons over the barrier into the metal. It assumes that the quasi-Fermi level in the semiconductor is constant and hence that the mean free path $\lambda$ is long compared with the depletion width. Both theories result in the same form of equation

$$J = J_S \left( \exp\left(\frac{eV}{kT}\right) - 1 \right) \qquad (2.8)$$

but in the diffusion theory $J_s$ is field dependent while in the thermionic model $J_s$ is more temperature dependent. Bethe's theory accurately describes the current when $E_{max}\,\lambda > \frac{kT}{q}$ where $E_{max}$ is the maximum field in the barrier and $\lambda$ is the mean free path of electrons. When this condition is not satisfied, the diffusion theory is more accurate. Crowell and Sze (1966) developed a theory which combines these two to form one of universal applicability. This is done by the introduction of

a recombination velocity, $V_R$, for electrons at the metal semiconductor interface. Then, depending on whether the effective electron diffusion velocity within the depletion region $V_D$ is less than or greater than $V_R$, the diffusion or thermionic emission theories apply respectively. In his book, "Metal-Semiconductor Contacts", Rhoderick shows that in terms of an energy band diagram, the basic difference between the diffusion and thermionic emission theories lies in the location of the quasi-Fermi level for electrons at the barrier. The quasi-Fermi level is the hypothetical energy level which gives the correct concentration of electrons, if inserted into the Fermi-Dirac distribution function even though the system is not in true thermal equilibrium. Far from the junction, the quasi-Fermi level must coincide with the Fermi levels in the metal and the semiconductor respectively. In the diffusion theory, the quasi-Fermi level is coincident with the metal Fermi level at the junction, rising (in forward bias) to join the semiconductor level within the depletion region. The thermionic emission theory, on the other hand, requires the quasi-Fermi level through the semiconductor to remain constant, dropping (in forward bias) within the metal. Rhoderick (1972) has found that the thermionic emission theory describes the current-voltage characteristics of Au/CdS diodes very adequately.

## 2.4 Measurement of Barrier Height

The most common techniques for measuring barrier heights in metal-semiconductor diodes utilise C-V, I-V and photoelectric threshold measurements. In the first two of these, the diode has to be biased and thus is perturbed by an external field, whereas with the photoelectric method, the measurement is direct and therefore can be most accurate.

### 2.4.1 Capacitance-Voltage Characteristics

It has already been shown that it is possible to measure barrier height

and donor concentration by this method. In a real device it may be necessary to consider an equivalent circuit, which in the absence of an interfacial layer may consist of a conductance, G, and capacitor, C, in parallel, both voltage dependent, together with a resistor, r, in series, corresponding to the semiconductor bulk resistance. Since it is possible only to measure the admittance and hence G' and C' for the combination of components, there will be restrictions on the use of the simple theory to predict results of experiments. It can be shown quite simply that if $rG \ll 1$ and $\omega^2 r^2 C^2 \ll 1$, G and C correspond to the measured values, where $\omega$ is the a.c. frequency of the bias voltage. C and G are both frequency dependent because of the effects of trapped charge; however, this dependence may be reduced by using a frequency high enough so that the traps are not excited by the a.c. signal.

### 2.4.2 Effect of Interfacial Layer

It has been shown by Crowell et al (1965), that an interfacial layer of non-zero thickness must exist between metal and semiconductor even when both are in intimate atomic contact. This affects the measured barrier height which is in fact a function of the thickness of the layer. Cowley, (1966) proved that for a device with an interfacial layer but without surface states, the voltage intercept, $V_o$, of a plot of $\frac{1}{C^2}$ versus V is :

$$V_o = V_{bi} - \frac{kT}{q} + \frac{V_1}{4} + (V_1 V_{bi})^{\frac{1}{2}} \qquad (2.9)$$

where

$$V_1 = \frac{2 q \varepsilon_s N_D d_i^2}{\varepsilon_i^2} \qquad (2.10)$$

$V_{bi}$ = diffusion potential at zero bias

$d_i$ = thickness of the interfacial layer

$\varepsilon_s$ = permittivity of semiconductor

$\varepsilon_i$ = permittivity of interfacial layer

He extended the theory to cover a contact with a uniform density of surface states in equilibrium with the metal surface. This corresponds to an interfacial layer less than $\sim 30$ Å thick with the Fermi level at the semiconductor surface remaining 'pinned' to the metal Fermi level (Card and Rhoderick, 1971). The equations from the previous section are altered by the inclusion of a voltage dependent surface state charge to modify the equation of Gauss' Law across the interface region. This yields a value of voltage intercept which can be shown to be equivalent to:

$$V_o = V_{bi} + \left[ V_1^{\frac{1}{2}} \left( V_{bi} - \frac{kT}{q} \right)^{\frac{1}{2}} \right] \Big/ (1+\alpha) + \frac{V_1}{4(1+\alpha)^2} - \frac{kT}{q} \qquad (2.11)$$

where $\alpha = qN_{ss} \, d_i / \varepsilon_i$ )

with $N_{ss}$ = surface state density / eV / $cm^2$

Thus if the diffusion potential is known accurately (by photothreshold measurements for example) an estimate of the surface state density may be made from the value of the voltage intercept.

Another, more general approach is that of Crowell and Roberts (1969); their method does not require the limiting assumption of a constant surface state density. An n-type semiconductor with donor density $N_D$ and surface state density $N_{ss}/eV/cm^2$ is placed in contact with a metal with an interfacial layer of thickness $\delta_i$ and permittivity $\varepsilon_i$. A field E will exist at the surface of the semiconductor due to the ionised donors in the depletion region. If the applied bias is altered, or if there is a change in the doping concentration of the semiconductor, this field will change by an amount $\Delta E$, corresponding to a change in charge $\varepsilon \Delta E$ in the semiconductor. This will be accompanied by a similar variation in the charge in the surface states and metal to maintain overall neutrality. It gives rise to a change in the interface field and the density of filled

surface states, resulting in a barrier height alteration of $\Delta\phi_{Bn}$, thus:

$$\varepsilon_s \Delta E = -qN_{ss}\Delta\phi_{Bn} - \left(\frac{\varepsilon_i}{\delta_i}\right) \Delta\phi_{bn} \tag{2.12}$$

or

$$\frac{d\phi_{bn}(E)}{dE} = -\varepsilon_s \left[qN_{ss} + \left(\frac{\varepsilon_i}{\delta_i}\right)\right]^{-1} \tag{2.13}$$

Once again the assumption has been made that the occupation of surface states is determined by the Fermi level in the metal.

The quantity $\frac{d\phi_{bn}(E)}{dE}$ will affect the capacitance voltage characteristic. From Poisson's equation in the depletion region the expression

$$E^2 = \frac{2qN_D}{\varepsilon_s}\left(\phi_{bn} - \phi_n - V - \frac{kT}{q}\right) \tag{2.14}$$

can be derived. Here $q\phi_n$ is the energy difference between the conduction band and the Fermi level in the bulk of the semiconductor. The depletion capacitance can be written as

$$C = \varepsilon_s \left(\frac{dE}{dV}\right) \tag{2.15}$$

Differentiation of (2.14) with respect to E gives:

$$\frac{dV}{dE} = -\left(\frac{\varepsilon_s E}{qN_D}\right) + \frac{d\phi_{bn}}{dE} \tag{2.16}$$

and hence

$$\frac{1}{C^2} = \frac{2}{\varepsilon_s q N_D}\left[\phi_{bn} - V - \phi_n - \frac{kT}{q} - E\left(\frac{d\phi_{bn}}{dE}\right) + \frac{qN_D}{2\varepsilon_s}\left(\frac{d\phi_{bn}}{dE}\right)^2\right] \tag{2.17}$$

This equation shows that if

$$\left[\left(\frac{qN_D}{\varepsilon_s}\right)\left(\frac{d\phi_{bn}}{dE}\right) - E\right]\left(\frac{d^2\phi_{bn}}{dE^2}\right)\left(\frac{dE}{dV}\right) << 1 \qquad (2.18)$$

then the slope of the plot of $1/C^2$ versus V gives the donor density. The voltage intercept, $V_i$, leads to an apparent barrier height $\phi_a$ defined by

$$\phi_a = V_i + \phi_n + \frac{kT}{q} = \phi_{bn} - E\left(\frac{d\phi_{bn}}{dE}\right) + \left(\frac{qN_D}{2\varepsilon_s}\right)\left(\frac{d\phi_{Bn}}{dE}\right)^2 \qquad (2.19)$$

As the term $\left(\frac{d\phi_{bn}}{dE}\right)$ is always negative as defined, the true barrier height must always be less than that measured. This equation is directly equivalent to (2.11) above.

### 2.4.3 Photoelectric Threshold

It has already been stated that the photoelectric method of measuring barrier height is most direct. The theory will now be outlined. Under illumination with monochromatic light of energy $h\nu$, the metal surface of a metal-semiconductor junction can emit an electron over the barrier into the semiconductor if $h\nu > q\phi_{bn}$. If the light is incident on a thin metal layer, and the photon energy $h\nu$ is greater than the band gap $E_g$ of the semiconductor, electron-hole pairs will be produced in the depletion region and then separated by the internal field. In the open-circuit configuration this will cause a photovoltage to appear across the device. If the illumination is from the back, (i.e. via the semiconductor) the same photoelectric emission process from metal to semiconductor is observed, however if $h\nu > Eg$ then the light will be very strongly absorbed at the back contact and the electron-hole pairs will simply recombine in the absence of a field to separate them.

According to the theory developed by Fowler (1931), the photoemissive current produced by each incident photon is given by :

$$R \simeq \frac{T^2}{\sqrt{E_s - h\nu}} \left[ \frac{x^2}{2} + \frac{\pi^2}{6} - \left( e^{-x} - \frac{e^{-2x}}{4} + \frac{e^{-3x}}{9} \ldots\ldots \right) \right] \text{ for } x > 0$$

(2.20)

where $E_s$ is the sum of $h\nu_o$ ($\equiv q\phi_{bn}$) and the Fermi energy measured from the bottom of the metal conduction band. $x \equiv \frac{h\nu - h\nu_o}{kT}$. Subject to the conditions that $E_s >> h\nu$ and $x > 3$, the above equation simplifies to

$$R \simeq (h\nu - h\nu_o)^2 \qquad (2.21)$$

or the form in which it will be used later,

$$\sqrt{R} \simeq h\nu - h\nu_o \qquad (2.22)$$

2.4.4 Current-Voltage Characteristics

The current flowing in an ideal Schottky diode under the conditions of thermionic emission is given by

$$J = A^* T^2 \exp\left(-\frac{q\phi_{bn}}{kT}\right)\left(\exp\frac{qV}{kT} - 1\right) \qquad (2.23)$$

where A* is the modified Richardson constant. $\phi_{bn}$ is the true barrier height and is a function of voltage because of the barrier lowering of the image force.

$$\phi_{bn} = \phi_{bo} - \Delta\phi \qquad (2.24)$$

where $\Delta\phi = \sqrt{\frac{qE}{4\pi\varepsilon_o}}$ and E is the field at the semiconductor surface,

$$E = \left[\frac{2q N_D}{\varepsilon_s}\left(V_{bi} - V - \frac{kT}{q}\right)\right]^{\frac{1}{2}} \qquad (2.25)$$

With forward bias $V > \frac{3kT}{q}$, the current density may be simplified to

$$J = A^* T^2 \exp\left(-\frac{q\phi_{bo}}{kT}\right) \exp\frac{q(\Delta\phi + V)}{kT} \qquad (2.26)$$

However, because A* and $\Delta\phi$ are both voltage dependent, this equation can be rewritten

$$J = J_s \left(\exp \frac{qV}{nkT}\right) \tag{2.27}$$

where

$$n = \frac{q}{kT} \left[\frac{d(\log_e J)}{dV}\right]^{-1} \tag{2.28}$$

Note that n, the so-called ideality factor, is a function of V, as defined here. More generally n is a function of barrier height and temperature as well as voltage. This is to embrace the non-ideality introduced by the mechanisms of current flow previously mentioned such as recombination in the depletion region and tunnelling through the barrier. As V tends to zero, $\log_e J$ extrapolates back to $\log_e J_S$ and therefore the barrier height is given by

$$\phi_{bn} = \frac{kT}{q} \log_e \left\{\frac{A^*T^2}{J_S}\right\} \tag{2.29}$$

## 2.5 Metal-Insulator-Semiconductor (MIS) Diodes

The principle of the metal on insulator on semiconductor diode has very wide applications in the field of modern electronics, especially for memory devices which utilise the insulator properties to store a charge almost indefinitely. Another use is in high density logic circuits, relying on the fact that the controlling mechanism is an electric field, not the movement of carriers as in a bipolar device. The power dissipation is consequently much lower. In the field of device physics a study of MIS devices offers one of the most useful techniques for investigating semiconductor surfaces. Since the surface properties of a semiconductor material can determine the stability of a device, such a study is of great importance. It is worth noting that most theories of MIS diodes assume that the insulator is perfect, i.e. that it has a very large band gap, zero conductance, and

perfect uniformity of thickness. Space does not permit a detailed account of MIS theory. For this, "Semiconductor Surfaces" by Many et al, and "Physics of Semiconductor Devices" by Sze give a good comprehensive treatment. A brief outline of the operation of an MIS diode follows.

The energy band diagram of an MIS diode on an n-type semiconductor is shown in Figure 2.2. This depicts the semiconductor surface in the so-called depletion mode, i.e. there is a depletion region similar to that found in a Schottky diode. Hence the capacitance of the device can be considered as the series combination of an insulator and a depletion capacitance. If the applied voltage (reverse bias) is increased, the band diagram in Figure 2.3 results. Here $E_i$, the intrinsic Fermi level has crossed $E_f$ at the surface. This implies that the number of minority carriers (holes) exceeds the number of majority carriers (electrons); the surface is thus inverted and the inversion mode has been formed. The capacitance of the device can be explained in the following way: a small change in voltage occurring slowly causes a change in the charge in the inversion layer and the charge at the metal-insulator interface. Thus the capacitance is simply that of the insulator alone. At high frequency, the charge in the inversion layer cannot follow the applied voltage and the capacitance is therefore that of insulator and depletion region capacitances in series.

When the applied voltage is reversed the band diagram is as shown in Figure 2.4. In this mode there is an accumulation of electrons at the insulator-semiconductor interface and therefore the capacitance becomes that of the insulator alone. The capacitance voltage curve therefore looks like that shown in Figure 2.5.

It can be demonstrated (Goetzberger and Sze, 1969) that $C_D$ for an n-type semiconductor is given by:

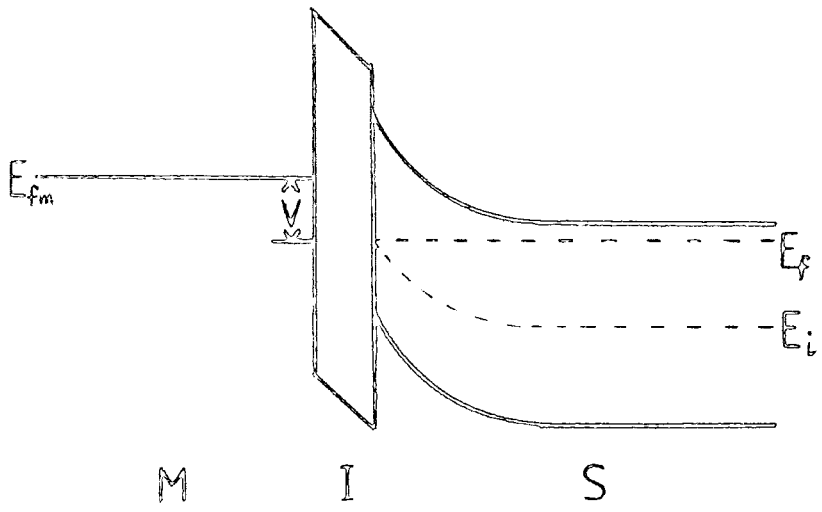



Fig.2.2 In Depletion Mode

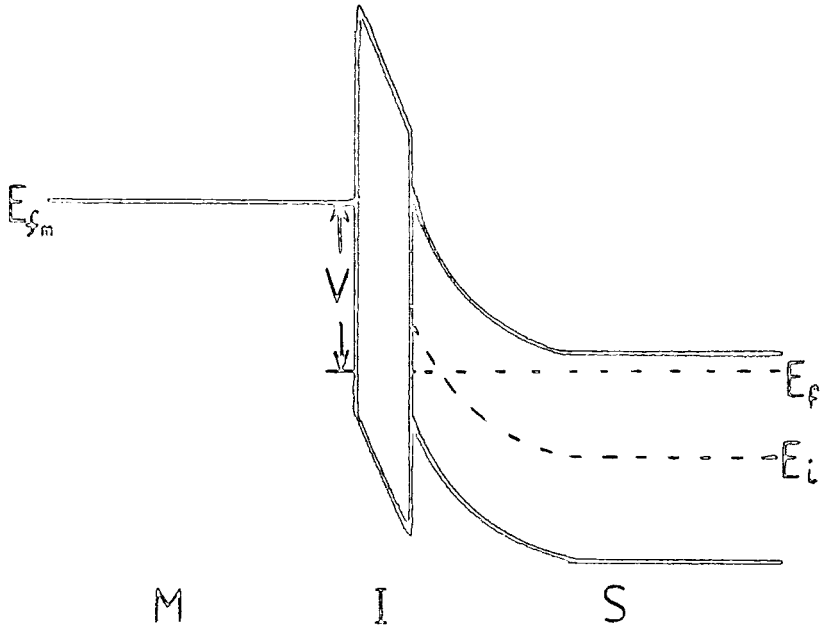



Fig.2.3 In Inversion Mode

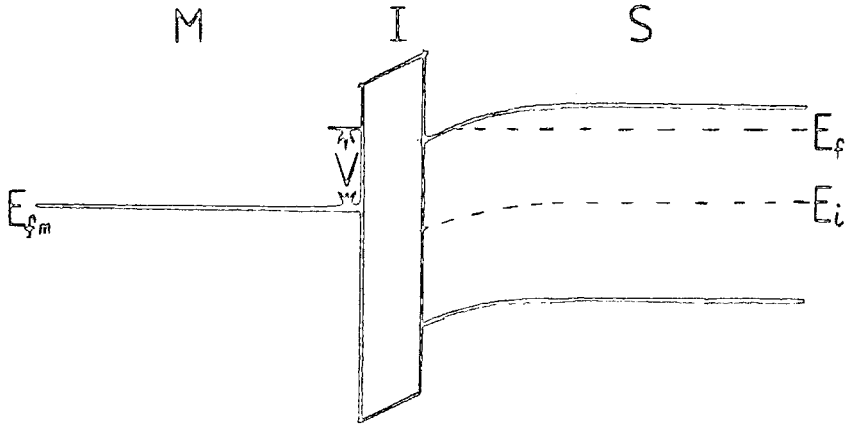



Fig.2.4 In Accumulation Mode

Band Structure of MIS Diode (n-type semiconductor)

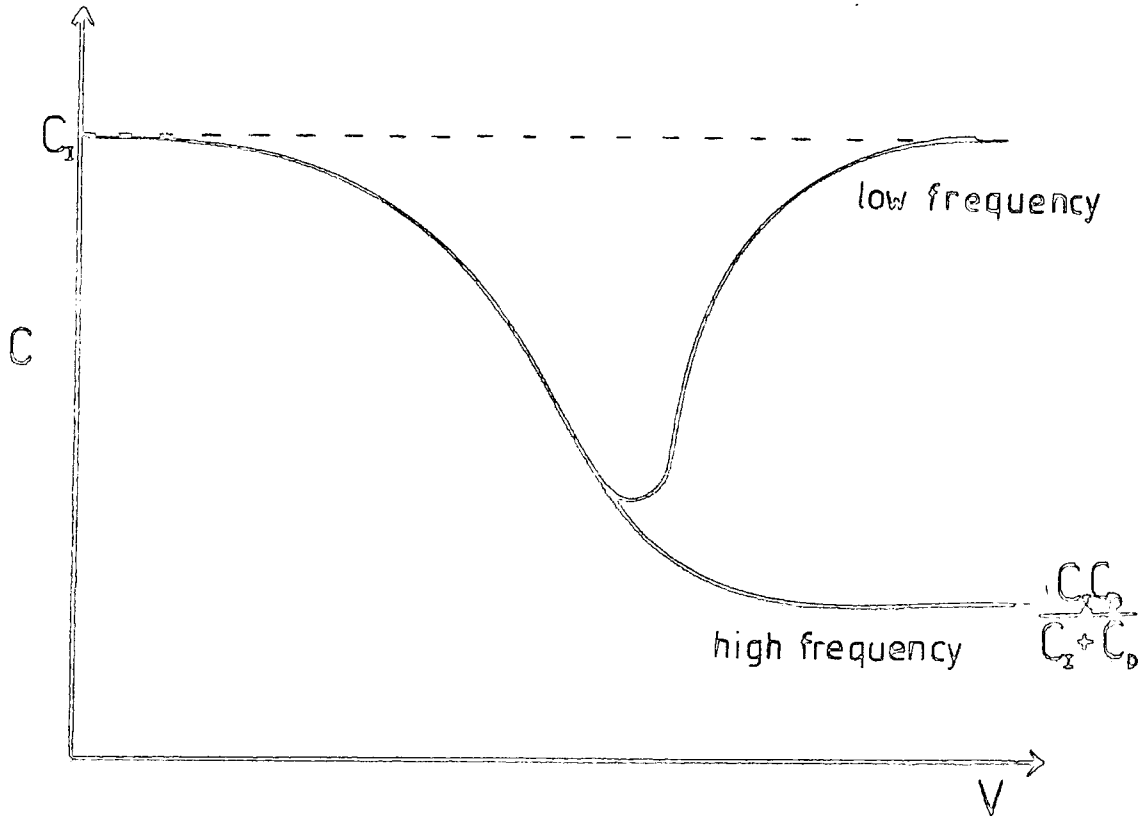



Fig. 2.5 Capacitance against Voltage for an MIS diode

$$C_D = \frac{\varepsilon_s}{\lambda_n} \frac{\left[1 - e^{-q\psi_s/kT} + \frac{p_o}{n_o}\left(e^{q\psi_s/kT} - 1\right)\right]}{G\left(\psi_s, \frac{p_o}{n_o}\right)} \qquad (2.30)$$

where $\lambda_n$ is the extrinsic Debye length for electrons, $\psi_s$ is the surface potential (the band bending) of the semiconductor, $n_o$ and $p_o$ are the bulk densities of electrons and holes, and $G(\psi_s, \frac{p_o}{n_o})$ is given by

$$G\left(\psi_s, \frac{p_o}{n_o}\right) = \left\{e^{q\psi_s/kT} - \frac{q\psi_s}{kT} - 1 + \frac{p_o}{n_o}\left[e^{-q\psi_s/kT} + \frac{q\psi_s}{kT} - 1\right]\right\}^{\frac{1}{2}} \qquad (2.31)$$

The voltage applied across an MIS device is divided accordingly:

$$V = V_I + \psi_s + \phi_{ms}/q \qquad (V_I = \text{insulator voltage}) \qquad (2.32)$$

where

$$V_I = \frac{\varepsilon_s}{\lambda_n C_I} \times \frac{2kT}{q} \times G\left(\psi_s, \frac{p_o}{n_o}\right) \qquad (2.33)$$

and

$$\phi_{ms} = \phi_m - \phi_s$$

## 2.6 Interface States

The above theory applies to the case of a 'perfect' semiconductor surface, i.e. one without any surface states or traps. When surface or interface states are present they will affect both the capacitance and conductance of the device. A very detailed treatment has been given by Nicollian and Goetzberger (1967). The surface states are occupied according to the Fermi-Dirac distribution, and therefore each occupied state adds a capacitance of one electron charge. If as the applied voltage is altered, the Fermi level sweeps through the state and empties it, the capacitance will be reduced. The change is therefore in the form of a step. Interface

states, however, cannot capture or emit electrons infinitely quickly and thus a loss mechanism and time constant must be associated with them, this gives rise to a conductance. This situation should be compared with the ideal MIS device with zero conductance.

On application of an a.c. signal, the Fermi level varies with time, and according to Shockley and Read (1952), the capture rate of electrons, as majority carriers, by a single-level state is:

$$R_n(t) = N_s C_n \left[1 - f(t)\right] n_s(t) \qquad (2.34)$$

and emission rate

$$G_n(t) = N_s e_n f(t) \qquad (2.35)$$

where $N_s$ is the density of states/cm$^2$, $C_n$ the electron capture probability, $e_n$ the electron emission constant, $f(t)$ the Fermi function at time $t$, and $n_s(t)$ the electron density at the silicon surface at time $t$.

The net current density flowing is:

$$i_s(t) = q N_s C_n \left[1 - f(t)\right] n_s(t) - q N_s e_n f(t) \qquad (2.36)$$

To simplify this, it is necessary to split the equation into d.c. and a.c. components.

$$f(t) = f_o + \delta f \qquad (2.37)$$

$$n_s(t) = n_{so} + \delta n_s \qquad (2.38)$$

Substituting and neglecting second order terms, (small signal approximation) gives

$$i_s(t) = q N_s C_n \left[(1 - f_o)\, n_{so} + (1 - f_o)\, \delta n_s - n_{so} \delta f\right] - q e_n N_s (f_o + \delta f) \qquad (2.39)$$

It is also necessary that there should be d.c. equilibrium, i.e. $R_n = G_n$, therefore

$$q N_s C_n (1 - f_o) n_{so} = q e_n N_s f_o \tag{2.40}$$

Substituting in equation (2.39)

$$i_s(t) = q N_s C_n \left[ (1 - f_o) \delta n_s - n_{so} (\delta f_o / f_o) \right] \tag{2.41}$$

This current can also be expressed by the time derivative of the Fermi function

$$i_s(t) = q N_s \left( \frac{df}{dt} \right) \tag{2.42}$$

Equating (2.41) & (2.42) gives

$$\frac{df}{dt} = C_n (1 - f_o) \delta n_s - C_n n_{so} \delta f / f_o$$

For a sinusoidal a.c. signal $\delta f = f_m e^{i\omega t}$, so that $\frac{df}{dt} = i\omega \delta f$

thus

$$\delta f = \frac{f_o (1 - f_o) \delta n_s}{n_{so} (1 + i\omega f_o / C_n n_{so})} \tag{2.43}$$

and

$$i_s(t) = \frac{i\omega q N_s f_o (1 - f_o) \delta n_s}{n_{so} (1 + i\omega f_o / C_n n_{so})} \tag{2.44}$$

From the Boltzmann relation $n_s = n_{so} e^{(\psi_{so} - \psi_s) q / kT}$, therefore

$$\frac{\delta n_s}{n_{so}} = \frac{q}{kT} \delta \psi_s \tag{2.45}$$

and

$$i_s(t) = i\omega \frac{q^2}{kT} \frac{N_s f_o (1 - f_o) \delta \psi_s}{(1 + i\omega f_o / C_n n_{so})} \tag{2.46}$$

This may be written in terms of admittance as

$$i_s(t) = Y_s \, \delta\psi_s \tag{2.47}$$

therefore

$$Y_s = i\omega \frac{q^2}{kT} \frac{N_s f_o (1 - f_o)}{(1 + i\omega f_o / C_n n_{so})} \tag{2.48}$$

Equation (2.48) describes the admittance of an RC series network with capacitance $C_s = q^2 N_s f_o (1 - f_o)/kT$ and time constant $\tau = f_o / C_n n_{so}$. The equivalent parallel capacitance of a single-level surface state is therefore

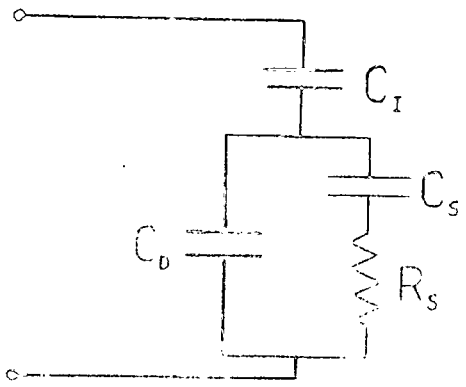
$$C = C_s / (1 + \omega^2 \tau^2) \tag{2.49}$$

and conductance

$$G = C_s \omega^2 \tau / (1 + \omega^2 \tau^2) \tag{2.50}$$

## 2.7 Equivalent Circuit of an M.I.S. Device

Since the total small signal a.c. current is obviously the sum of the contributions of the space charge and interface charge, and the potential $\psi_s$ is the same in both cases, this network must be in parallel with the depletion capacitance. The contribution from the insulator capacitance must be in series with this parallel combination, and therefore the equivalent circuit of the M.I.S. device with a single level of surface states is:




$C_I$ = Insulator capacitance

$C_D$ = Depletion capacitance

$R_s$ = Surface state resistance

$C_s$ = Surface state capacitance

where $R_s C_s$ = $\tau$ mentioned above.

Figure 2.6

This may be arranged in a more convenient way for comparison with experiment as

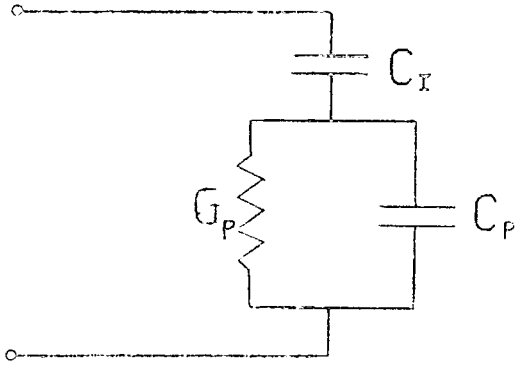



Figure 2.7

where

$$G_p = \frac{C_s \omega^2 \tau}{1 + \omega^2 \tau^2} \qquad (2.51)$$

and

$$C_p = C_D + \frac{C_s}{1 + \omega^2 \tau^2} \qquad (2.52)$$

It is easily shown that $G_p/\omega$ goes through a maximum when $\omega\tau = 1$ and $(G_p/\omega)_{max} = \frac{C_s}{2}$. Therefore, once the conductance has been corrected for the insulator capacitance, $\tau$ and $C_s$ may be found directly. The surface state density is then simply given by $N_{ss} = \frac{C_s}{qA}$ where A is the area of the contact.

## 2.8 Generalised Surface State Model

So far only the case of a single-level interface state has been considered. In general, there will be a continuum of states of varying density and capture cross-section. These complications will lower the maximum point and broaden the peak of the conductance curve by requiring integration over all the states. The peak, however, is still found to be

too sharp to fit experimental results, and Nicollian and Goetzberger (1967) therefore introduce the idea of statistical surface potential fluctuations, while Preier (1967) presents a theory of tunnelling to surface states as a cause of further dispersion in the conductance peak. Goetzberger et al (1976) provide a comprehensive review of the theory of interface states at the insulator semiconductor interface and alternative experimental techniques for their measurements.

The surface state model, and barrier height measurements described above, form the basis of much of the work of the following chapters, on metal insulator semiconductor diodes. The theory of surface states was initially developed for silicon devices, but has been shown to be applicable to other semiconductors. An attempt will be made to apply it to CdS devices, and the results discussed.

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# CHAPTER 3

## CRYSTAL GROWTH, MIS DEVICE PREPARATION AND EVALUATION

### 3.1 Growth of CdS Crystals

All II-VI compounds can be grown from the melt or from the vapour phase. The CdS used in this work was all grown by one of the three vapour phase techniques:

(1) Sublimation of the actual compound.

(2) Reaction of the constituents in the vapour phase.

(3) Chemical transport (using a carrier gas).

In all vapour phase methods the gas molecules diffuse to a region where supersaturation occurs, and under suitable conditions stoichiometric crystals form.

The most basic method of sublimation growth, developed by Reynolds and Czyzack (1950), is that of coalescence and occurs by an interchange of material between the powder charge and the vapour so that crystals grow on the charge itself. This has the drawback that impurities in the charge are also present in similar concentrations in the crystals. An improvement to this, is the method of Piper and Polich (1961) whereby a temperature gradient is established across a growth ampoule so that the material is transported from the hot to the cooler end of the tube. The growth tube is then moved relative to the furnace as the crystal grows, producing a single crystal of considerable size. In Clark and Woods' (1966) modification of this method the growth ampoule is not sealed, but allowed to communicate via a narrow opening with an argon atmosphere inside the furnace tube. This permits a non-stoichiometric excess of either element to diffuse away before much growth occurs. Stoichiometry is important because the evaporation rate of CdS varies by more than two orders of

magnitude with a slight deviation from stoichiometric proportions. A drawback with this method which employs horizontal furnaces, is that there is in general a non-uniform radial temperature gradient associated with the difficulty of positioning the growth ampoule along the central axis of the tube. To overcome this, Clark and Woods (1968) describe a vertical system, using sealed growth tubes. These tubes consist of growth ampoules with a tail $\sim$ 30 cm long containing a reservoir of cadmium or sulphur. The function of the element in the reservoir is to provide a known partial pressure, because it is held at a constant temperature throughout growth in a separate furnace. Thus optimum conditions for growth can be determined externally, independent of the charge. The presence of the partial pressure provided by the element in the tail has another effect on the growth: that is, it can limit the rate of transfer of CdS from charge to crystal, since growth in vacuo takes place in a few hours and results in a polycrystalline lump of material (Fochs et al, 1968).

All the cadmium sulphide used in the present work was grown as boules using this last method of Clark and Woods (1968). Since the purity of the starting material is very important in controlling the properties of the grown CdS boule, the charge used consisted of crystalline rods and platelets grown by sublimation in a continuous stream of argon (Clark and Woods 1966). The starting material was B.D.H. Optran grade CdS.

## 3.2 Properties of Cadmium Sulphide

Cadmium sulphide is a II-VI semiconducting compound with a direct band gap of 2.4 eV, which usually forms crystals with the hexagonal wurtzite structure. Another phase may occur under certain conditions, this has the metastable cubic sphalerite structure. For example, thin films with this structure may be grown on cubic substrates such as NaCl (Wilcox and Holt, 1969). Although cadmium melts at 321$^{o}$C and sulphur at

119°C, the minimum temperature at which cadmium sulphide melts is 1475°C and that is accompanied by an equilibrium vapour pressure of ∿4 atmospheres. However sublimation starts to occur at 700°C at atmospheric pressure.

CdS is a direct gap material which can only be made n-type or insulating. The result of attempts to incorporate acceptor impurities such as copper into the lattice is self-compensation by non-metal vacancies, so that the resistivity remains very high $\sim 10^{12}$ Ωcm. N-type cadmium sulphide is readily formed by growth under non-stoichiometric (cadmium-rich) conditions which lead to the formation of predominantly one type of vacancy (sulphur). Such crystals may be regarded as self-doped. The ability of a II-VI compound to be made n-type or p-type depends on the ratio of cation radius ($r_c$) to anion radius ($r_a$). If $\frac{r_c}{r_a} > 1$ as in most II-VI compounds, then n-type conductivity is possible, but not p-type; if $\frac{r_a}{r_c} > 1$, p-type conductivity but not n-type results, as in ZnTe. Finally if $r_a \simeq r_c$ the compound may be made either p or n-type, e.g. CdTe. A detailed account of self compensation is given in the paper by Fischer (1966).

It is because of the impossibility of making p-type CdS that copper sulphide is used as the p-type material in the $Cu_2S$-CdS solar cell. $Cu_2S$ may be grown topotaxially on CdS by a displacement reaction of copper and cadmium, which will be described later.

## 3.3 Cadmium Sulphide Sample Preparation

To prepare a good heterojunction or Schottky diode on a single crystal substrate, it is necessary that the resistivity be low in the range 1 - 100 Ωcm, otherwise measurements will be complicated by a high bulk series resistance and a wide depletion region. Some crystal boules, grown with cadmium tails were found to have resistivities of the right magnitude, $\rho \sim 1 - 5\ \Omega$cm, while others grown with sulphur tails, and some

which were orange in colour, had resistivities of $\sim 10^{8}$ Ωcm. In order to reduce these high resistivities a heat treatment in either cadmium liquid or vapour was administered.

Dice 2 x 2 x 2 mm which had been previously cut from the crystalline boule using a diamond saw, were etched in concentrated HCl to clean the surface and remove the work-damaged layer. After washing in methanol and distilled water, the dice were placed at one end of a silica tube, shaped like an hour-glass, containing some cadmium metal. The silica tubing had been cleaned in methanol and distilled water. Tubes were evacuated to a pressure of better than $10^{-5}$ torr and then sealed off. Each tube was suspended in a vertical furnace for three days at 600$^{o}$C with the CdS dice immersed in the molten cadmium. Finally the tube was removed from the furnace and inverted to allow the cadmium to flow off the CdS leaving the dice caught at the neck of the tube. They were then left to cool.

For heat treatment in Cd vapour a similar arrangement was used, except the tube was placed in the furnace the other way up, with the crystals held above the cadmium by the constriction. The vapour method was used more frequently since heating in the liquid generally lowered the resistance too far (even after a few hours it had fallen several orders of magnitude), and sometimes small balls of molten cadmium would remain stuck to the surface of the dice after inversion of the tube. Removal of these after cooling proved difficult without damage to the sample.

## 3.4 Device Preparation

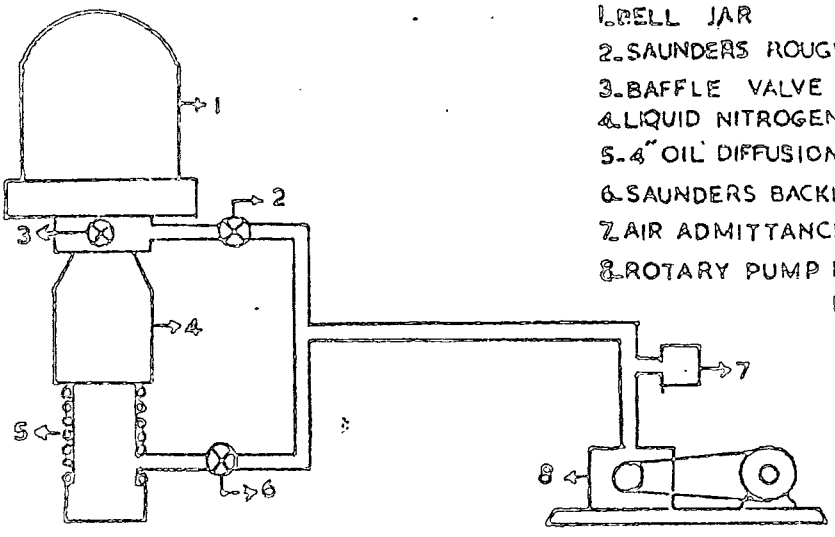
Throughout this work, the devices used were fabricated on either 2 x 2 x 2 mm cubes, or 4 x 4 x 2 mm dice cut from single crystal boules by a diamond saw. The crystals were first aligned, using the X-ray back reflection technique, and then cut into slices 2 mm thick with the c-axis perpendicular to the surface. These slices were then polished using

3 μm Aloxite powder to remove saw marks and make the c-axis faces readily recognisable later. After this, the slices were cut into cubes or dice as appropriate.

For all the experiments undertaken, at least one ohmic contact was required and this was invariably made using indium wire in the following manner. The sample was etched in concentrated HCl for 20 seconds and washed in methanol. The etch clearly revealed the difference between the two c-axis faces, the (0001) cadmium and the $(000\bar{1})$ sulphur face (Warekois et al, 1962, 1966). The cadmium face appeared generally smooth, with several large hexagonal etch pits, whereas the sulphur face was uniformly matt. With most devices the ohmic contact was made on the shiny cadmium face, but sulphur faces were also used occasionally. A pellet of indium wire $\sim \frac{1}{2}$ mm thick was cut and pressed on to the CdS surface. The sample was then placed on a strip heater in an argon atmosphere and heated to 200°C for 10 minutes, allowing the indium to melt and diffuse into the surface. After cooling, a mechanically and electrically sound contact had been produced.

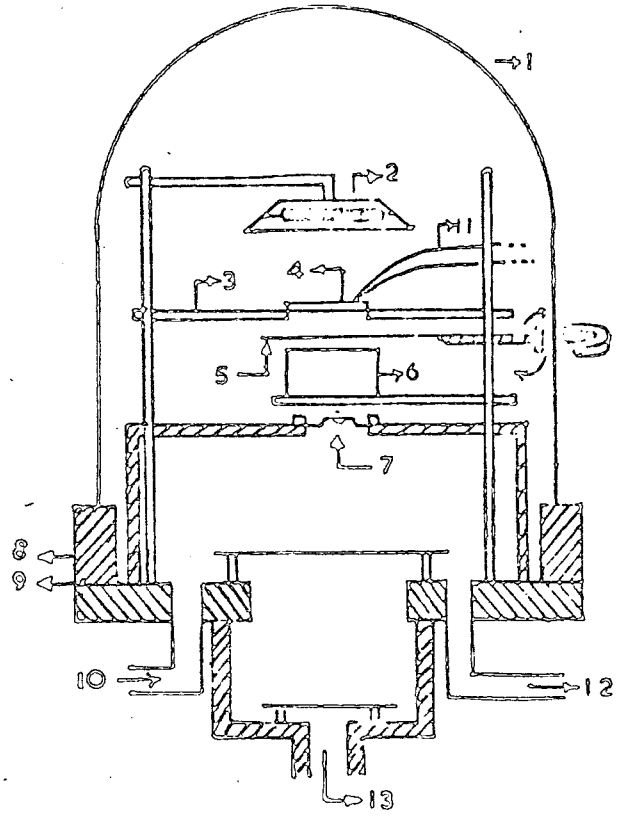
## 3.5 Preparation of Metal-Semiconductor and MIS diodes

The sample now carrying an ohmic contact was first polished using 3 μm Aloxite powder on the face opposite the contact and then etched in concentrated HCl for 20 seconds and washed in methanol. It was placed still wet into the vacuum system illustrated in Figure 3.1 for gold evaporation. A mask with a round hole of 1 $mm^2$ area was used to define the gold contact. Evaporation took place from a molybdenum boat at a pressure of better than $2 \times 10^{-5}$ torr, and lasted approximately 10 seconds. In the manufacture of an MIS diode, the method was similar to that described above, except that the sample was polished using 1 μm diamond paste before being etched for ~10 seconds. Two different types of deposition




1. BELL JAR
2. SAUNDERS ROUGHING VALVE
3. BAFFLE VALVE
4. LIQUID NITROGEN TRAP
5. 4" OIL DIFFUSION PUMP
6. SAUNDERS BACKING PUMP
7. AIR ADMITTANCE VALVE
8. ROTARY PUMP EDWARDS ES 200

SCHEMATIC DIAGRAM OF PUMPS AND VALVES OF EVAPORATOR




1-12" PYREX BELL JAR
2-W-I LAMB SUBSTRATE HEATER
3-STAINLESS STEEL SUBSTRATE
4-MASK
5-SHUTTER
6-SILICA CYLINDER
7-MOLYBDENUM BOAT
8-STAINLESS STEEL COLLAR
9-VITON 'O' RING
10-GAUGE HEADS
11-THERMOCOUPLE
12-ROTARY PUMP
13-HIGH VACUUM LINE

BELL JAR FIXTURES

FIG. 3.1 SCHEMATIC DIAGRAM OF VACUUM SYSTEM & BELL JAR FIXTURES

of the SiO insulator were tried. In the first, a tantalum boat, 1 cm x 3 cm with a centre section of 1 cm x 1 cm x ½ cm deep was filled with B.D.H. Vactran grade SiO powder. The sample to be coated was held ∿ 7 cms away in a molybdenum clip, so that the whole surface could be covered with the SiO. Evaporation took place at a pressure of ∿ 2 x $10^{-5}$ torr and lasted two minutes, the power dissipation was ∿500watts at 50 amps, giving an evaporation rate of ∿20 Å/sec. During deposition the temperature of the CdS increased from 15°C to 150°C due to radiation from the heated boat, in consequence the system was left for one hour to cool before breaking the vacuum. Afterwards the sample was moved over a mask for a gold evaporation.

The insulating layer could also be put down by electron beam deposition. The vacuum system with which this was used, was also equipped with a Speedivac film thickness monitor model 1, so that the thickness deposited could be controlled much more accurately. SiO powder was placed in a molybdenum crucible which was screwed into a water-cooled, earthed hearth. The filament cathode, of circular design with a hole in the centre was placed above this, and some 8 cms beyond, the samples were held in molybdenum clips beside the quartz crystal. After pumping the system down to a pressure < 2 x $10^{-5}$ torr, the filament current was turned on to outgas the electron gun system. When the pressure had fallen again to 2 x $10^{-5}$ torr, the filament current was reduced to zero, and the H.T. increased to 4 kV. The filament current was then increased slowly until evaporation began. Evaporation usually lasted several minutes and layers ranging between 500 Å and 2000 Å in thickness were deposited. A variety of other insulators (e.g. ZnS, $Y_2O_3$) were also deposited in a similar manner.

## 3.6 Measurement Techniques

The type of measurements required as indicated by the theory of the previous chapter, were of a.c. capacitance and conductance as functions of both frequency and bias voltage. A Brookdeal 'Ortholoc' model 9502 was used for all these measurements. This instrument (see Fig 3.2) consists of two phase sensitive detectors with a phase difference of $90^{\circ}$ between them. Details of the specification and circuitry are given in the 9502 Ortholoc Instruction manual. The reference signal was provided by the Brookdeal 5012 F oscillator which was used between frequencies of 10 Hz and 100 kHz with an output level set at 50 mV R.M.S. throughout. A continuous monitor of the frequency was provided by a Marconi Instruments digital frequency meter model 2430. The high and low frequency circuits shown in Figure 3.3 and 3.4 were built to provide the input signal from the device while at the same time allowing a d.c. bias to be applied.

The frequency range of operation of the high frequency circuit is limited by the pulse transformer since its transfer characteristics fall off sharply below 2 kHz. To satisfy the conditions that this circuit provides a signal which is related linearly to the impedance of the device being measured, it is apparent that $Y_{device} << Y_T$ where $Y_T$ is the total admittance of all the other components in the circuit, hence $R_1 \rightarrow R_7$ are provided in the range from 10Ω to 1.5 kΩ for use with a wide range of device impedances.

For low frequency operation, i.e. f < 3 kHz, the non-inductive circuit in Figure 3.4 was used. The condition for the admittance measured, to be proportional to that of the device, is again that its impedance be large compared with that of the rest of the circuit. The variable voltage in both these circuits was provided by an integrated circuit voltage ramp, with a rate adjustable from 1 sec/volt to 1000 sec/volt and

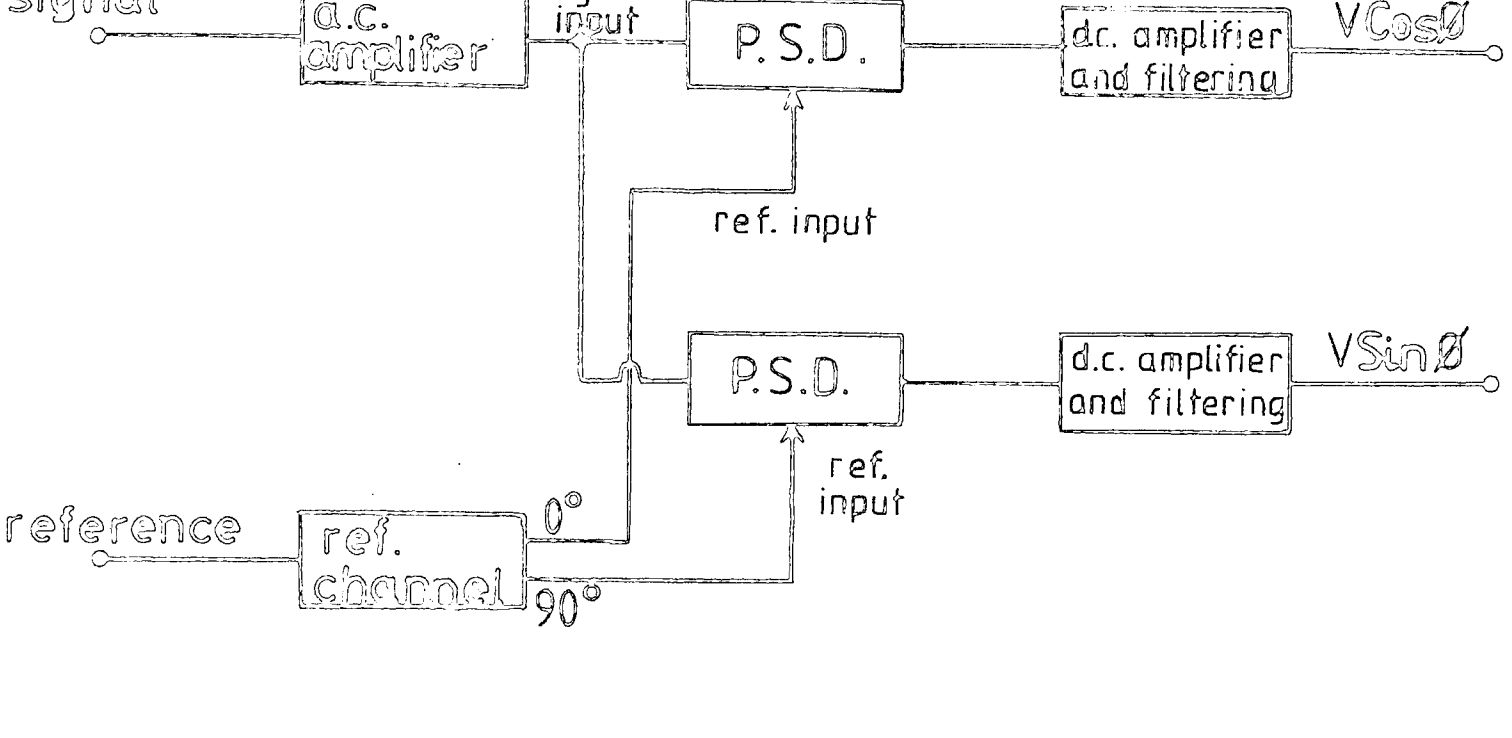
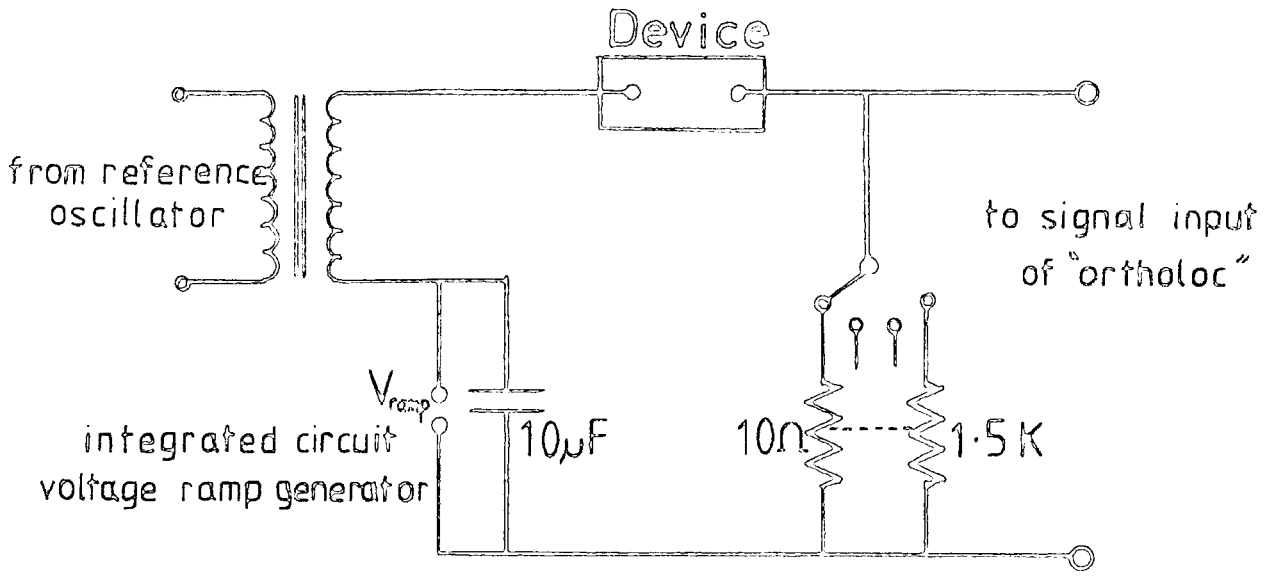
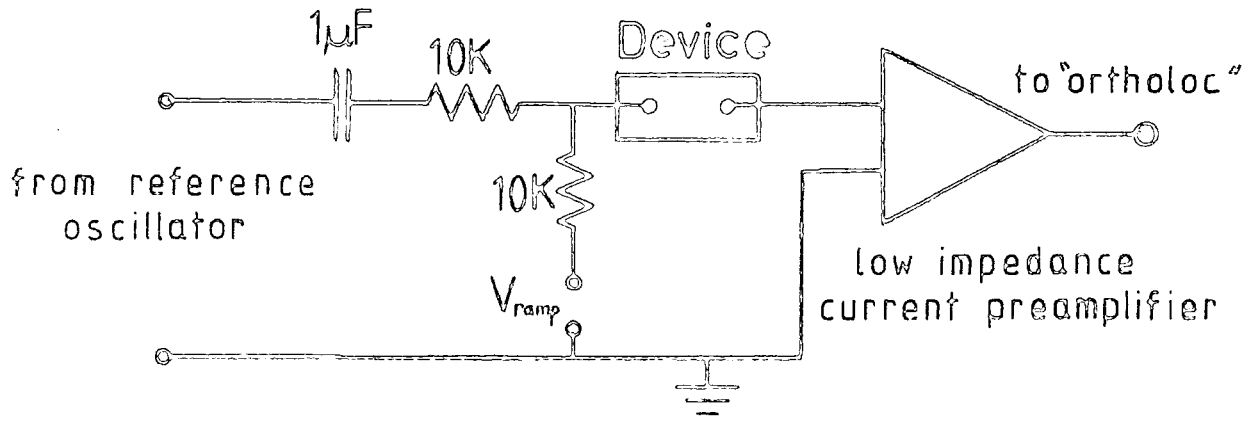



Fig. 3.2 Block Diagram of "Ortholoc"




High Frequency Measurement Circuit

Figure 3.3




Low Frequency Measurement Circuit

Figure 3.4

capable of running from positive to negative or negative to positive without being reset at zero. The ramp voltage was fed direct to the X input of a Hewlett Packard X-Y-T recorder Model 7041A, the Y input was obtained from the output of either the in-phase or quadrature outputs of the Ortholoc. Thus C-V and G-V curves could be plotted automatically.

As the Ortholoc provides an output proportional to the admittance of the diode, it is necessary to calibrate at each frequency using a standard silver-mica capacitor and known resistors. This was done in the following way; the capacitance and conductance of the device were guessed, and the nearest standard capacitor was connected. The Ortholoc phase control was adjusted until the conductance (in-phase) meter read zero, two resistors, differing in value by a factor of ten and being either side of the unknown value were sought and connected in turn across the capacitor until the conductance meter reading altered by a factor of exactly ten. If this did not happen, then the phase control might need some slight adjustment. When this was in order, the chart plotter could be calibrated, and plots of G and C versus voltage taken. The experimental limitations of accuracy of this system are readily apparent. If G is to be measured to an accuracy better than an order of magnitude, then $100\,G > \omega C$ (otherwise the phase setting error will swamp G with a fraction of C), and similarly the other way round. Fortunately for most of the measurements in this work $10\,G \simeq \omega C$ and so accurate measurements could be taken.

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# CHAPTER 4

## EXPERIMENTAL RESULTS ON MIS DEVICES ON CdS WITH SiO AS INSULATOR

### 4.1 The Insulating Layer

A brief description of the apparatus used in this investigation has already been given, therefore this chapter will start with some details about the choice of insulator. Silicon dioxide is the insulator normally associated with MIS devices, because it has very good insulating properties and can be grown easily on silicon as it is the natural oxide. However, being so stable, it has a very high melting point and a high temperature for evaporation (above 1000°C at $10^{-5}$ torr). Silicon monoxide has also been studied as an insulator, and has the advantage over $SiO_2$ that it sublimes at a temperature of $\sim$800°C at $10^{-5}$ torr, and may be evaporated thermally or by electron beam, relatively easily. It is unstable at temperatures below 1180°C, and at room temperature exists as an intimate crystalline mixture of silica and silicon, however it is thought that it can exist in a metastable state at room temperature in a thin film form, probably with the air interface somewhat oxidised. According to Rochow in 'Comprehensive Inorganic Chemistry' (1973), a good silicon monoxide layer is deposited when the evaporation takes place at low pressure, i.e. less than $10^{-4}$ torr. Otherwise oxidation to $SiO_2$ occurs.

Pliskin and Lehman (1965) show that SiO and $SiO_2$ may be distinguished quite readily by the differences in their infra-red absorption spectra. Silicon dioxide absorbs very strongly at 9.1 μm whereas silicon monoxide has a similar strong absorption at exactly 10 μm. A film of SiO deposited at higher pressure, $10^{-3}$ torr, and slow rate $< 5$ Å/sec shows a strong band at 9.5 μm implying that oxidation has occurred.

SiO was adopted as the first choice for an insulator. In order to investigate the composition of films being produced here on the CdS, a film was deposited on a piece of potassium bromide crystal under normal conditions. The optical transmission of the layer was analysed using a Perkin Elmer 457 Infra-red Grating Spectrometer. The percentage absorption is shown in Figure 4.1, where the curves for pure $SiO_2$ and SiO are included for reference.

Whilst the absorption spectrum indicates that the SiO layers grown were not perfect SiO they do imply that they were more similar to SiO than to $SiO_2$.

The layers deposited on CdS proved to be unstable under atmospheric conditions. After a period varying between two minutes and several days, a film would start to peel off the cadmium sulphide. To prevent this effect, which was thought to be due to differential thermal contraction, the sample was heated to 200$^{o}$C before evaporation commenced. Sometimes a good film was produced which adhered well and at other times films which peeled off in a few hours. A gold contact was evaporated on to the good films and electrical contact was made using a light phosphor-bronze spring contact and copper plate. Measurements of capacitance versus voltage and conductance versus voltage were made at frequencies between 10 Hz and 100 kHz at values of 1, 2, 4, 7 in each decade. With certain diodes an external oscillator capable of higher frequencies was used in conjunction with the Ortholoc to provide C/V and G/V data up to 220 kHz , the maximum frequency of operation of the Ortholoc.

## 4.2 Experimental Results

About 40 devices were measured and typical C/V and G/V curves are shown in Figures 4.2 and 4.3. What is actually plotted for conductance is G/f in order that all the values are of similar magnitude. At small

forward biases the conductance became very high rendering the capacitance unmeasurable. This may have been due to localised breakdown occurring at weak spots in the film under the high fields present in forward bias.

It is immediately apparent that the diode did not exhibit true MIS behaviour; compare for example the capacitance-voltage characteristics in Figure 4.2 with MIS C/V curves in Figure 2.5, and the conductance voltage characteristics with those of Nicollian and Goetzberger (1967). Another important feature was that the diode did not reach accumulation in forward bias, or inversion in reverse bias. In contrast, however, when the conductance and capacitance at fixed bias were plotted against frequency, as shown in Figures 4.4 and 4.5, the shape of the resulting curves was quite similar to those expected from the surface state model, which are of the form of Debye relaxation curves.

## 4.3 A Surface State Model

In an attempt to fit these results to the surface state model, the following simplifying assumptions were introduced. At high frequency, i.e. 220 KHz the surface states would be unable to respond and could therefore be ignored, while at low frequency the resistor $R_s$ could be ignored. Thus the equivalent circuits shown in Figure 4.6 would be applicable.

$C_I$ was not known accurately, but an estimate could be obtained from a knowledge of the thickness of the SiO layer from interferometric measurements. Using a value of 5.8 for the dielectric constant of SiO, $C_I$, was calculated to be between 300 and 400 pF. The model shows that at all frequencies, the measured capacitance must be less than that of the insulator alone. Since this would not be so if 300 pF < $C_I$ < 400 pF, the interferometer measurement was assumed to be invalid and $C_I$ was taken to be 1.2 nF initially. Then the measured capacitance at high frequency

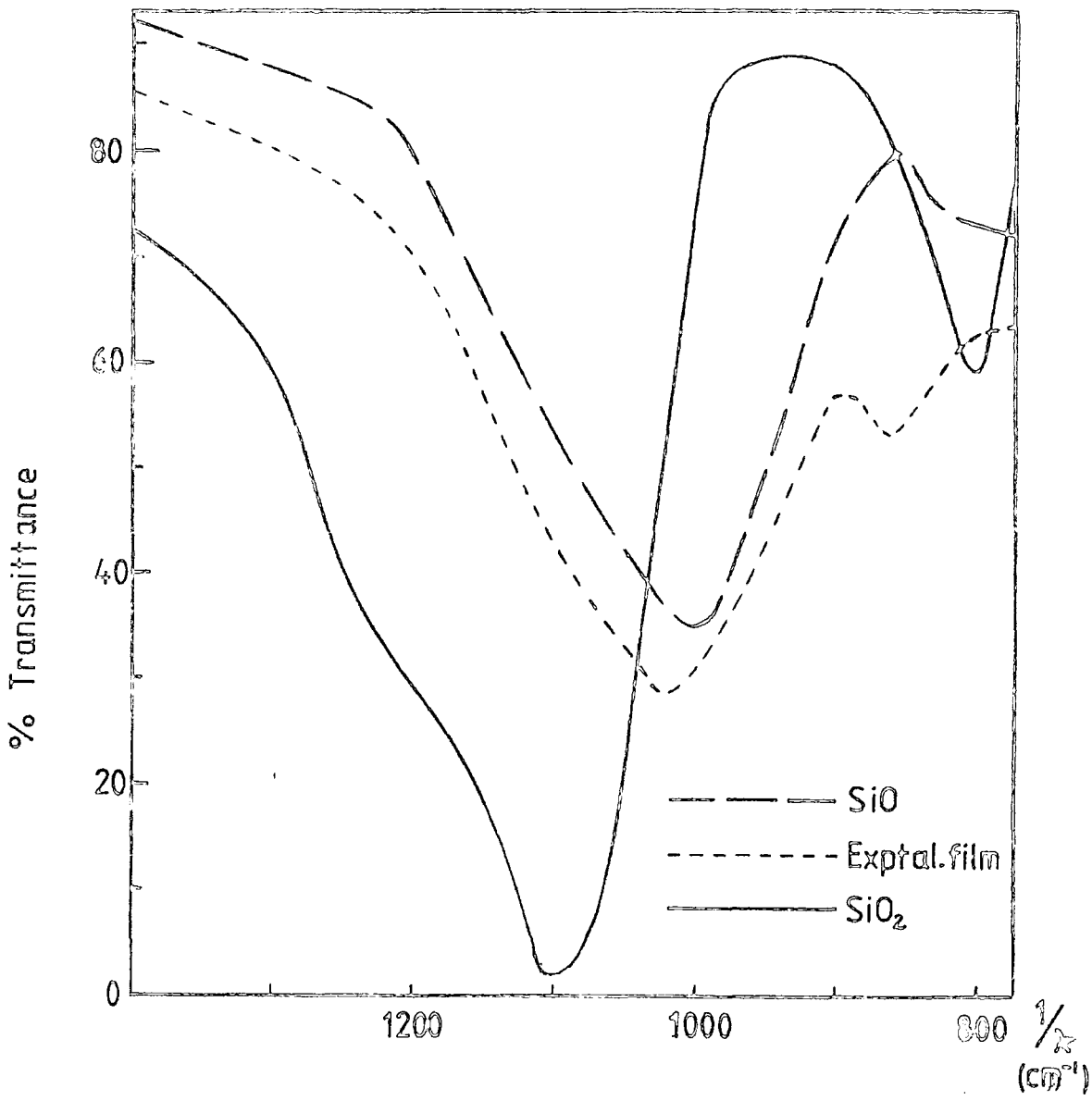
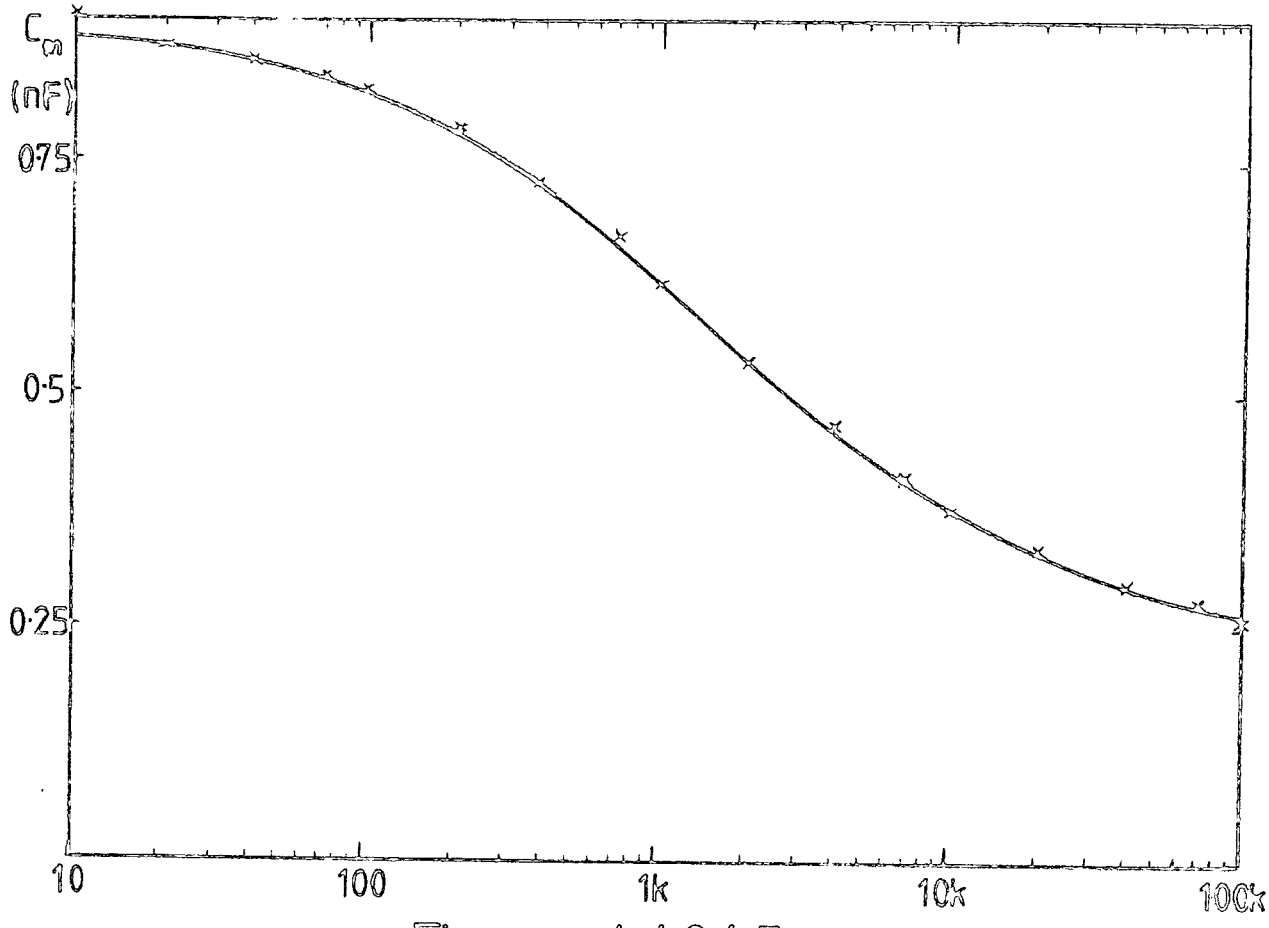



Figure 4.1 I.R. Absorption Spectra

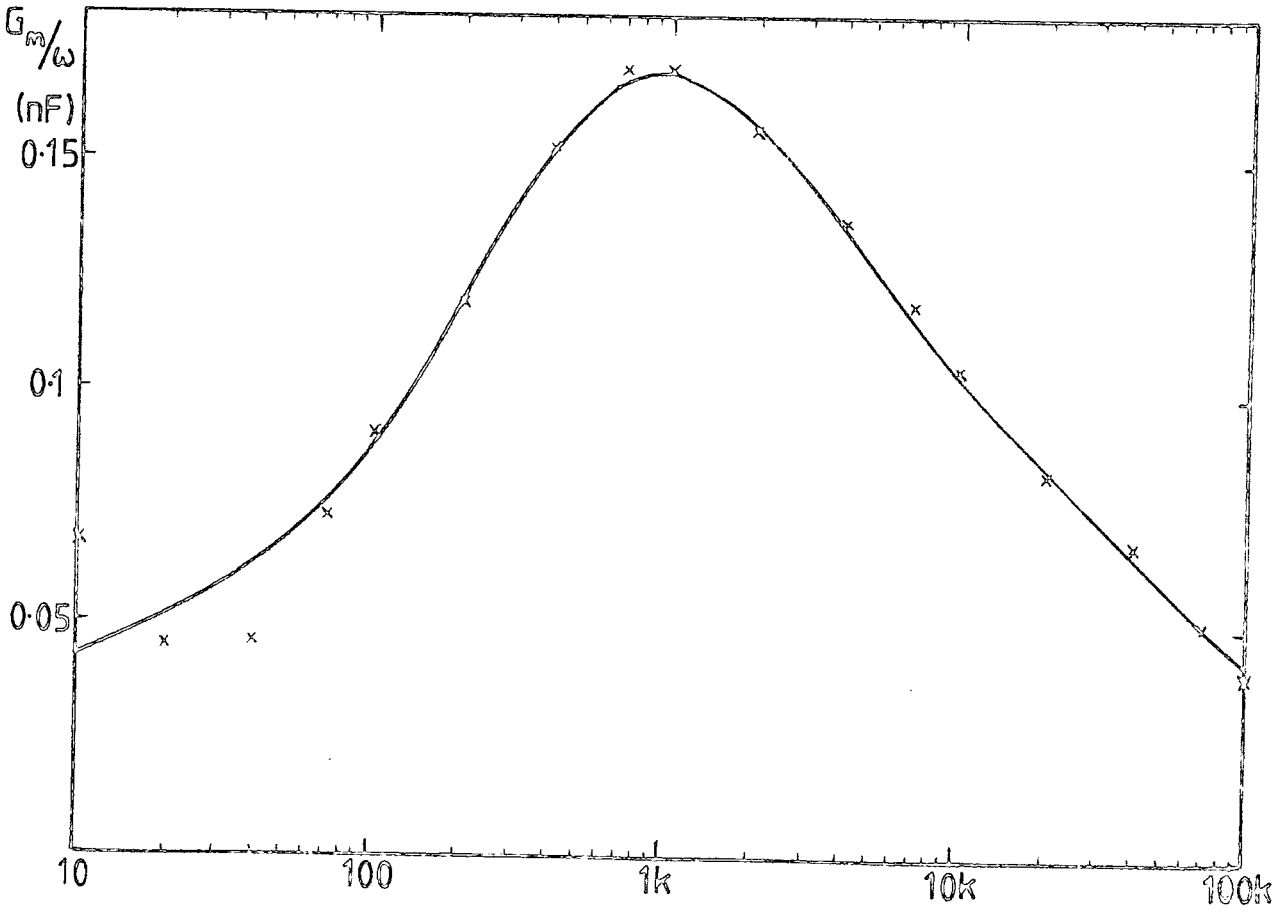
(after Pliskin & Lehman, 1965)

Figure 4.2 Typical Capacitance/Voltage characteristics

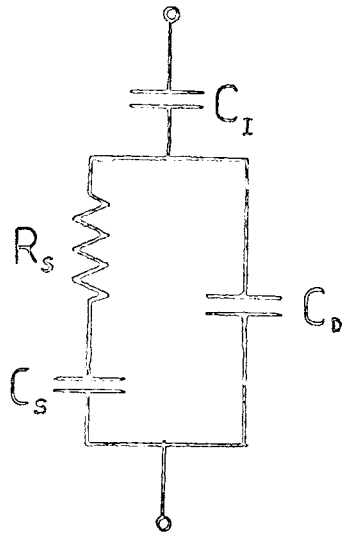
Figure 4.3 Typical Conductance/Voltage Characteristics



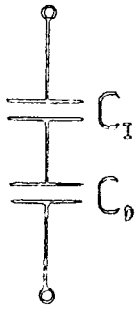

Figures 4.4 & 4.5



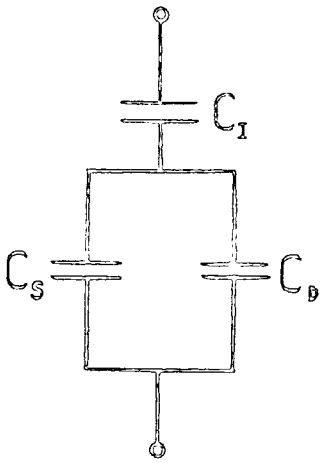

Typical Device Characteristics




(a) MIS Diode




(b) MIS Diode
simplified at high freq.




(c) MIS Diode
simplified at low freq.

Fig.4.6 Equivalent Circuits

is

$$C_{mh} = \frac{C_I C_D}{C_I + C_D} \qquad (4.1)$$

or

$$C_D = \frac{C_I C_{mh}}{C_I - C_{mh}} \qquad (4.2)$$

and at low frequency

$$C_D + C_S = \frac{C_I C_{ml}}{C_I - C_{ml}} \qquad (4.3)$$

where $C_{mh(l)}$ = measured capacitance at high (low) frequency. Using these equations on the curves of 220 kHz and 10 Hz gives the results in Table 4.1

| (V) Voltage | 0 | -0.5 | -1 | -1.5 | -2 | -2.5 | -3 | -3.5 | -4 |
|---|---|---|---|---|---|---|---|---|---|
| $C_D$ (nF) | 0.259 | 0.240 | 0.227 | 0.216 | 0.208 | 0.199 | 0.192 | 0.187 | 0.182 |
| $C_D + C_S$ (nF) | 142.8 | 37.6 | 20.0 | 14.4 | 11.4 | 9.65 | 8.43 | 7.46 | 6.82 |
| $C_S$ (nF) | 142.5 | 37.4 | 19.8 | 14.2 | 11.2 | 9.45 | 8.24 | 7.27 | 6.64 |

Table 4.1

Clearly $C_S$ may be calculated by subtraction as above, since the d.c. bias applied is independent of frequency. The voltages, however, are not those actually across the depletion region.

The surface state density $N_{SS}$ may be calculated from $C_S$ using the equation $N_{SS} = C_S/qA$, where A is the metal plate area, here 1 $mm^2$. This yields a maximum value of $N_{SS}$ of $10^{14}$ states/$cm^2$/eV which would require all surface atoms to contribute one surface state with its level lying within the band gap, a clearly impossible occurrence. One cause of the anomalously high value of $C_S$ at 0 V was the choice of $C_I$ to be 1.2 nF. The model was therefore tested with $C_I$ equal 2.0 nF. With this value

$C_D$ and $C_D + C_S$ are now as shown in Table 4.2.

| Voltage (V) | 0 | -0.5 | -1 | -1.5 | -2 | -2.5 | -3 | -3.5 | -4 |
|---|---|---|---|---|---|---|---|---|---|
| $C_D$ (nF) | 0.238 | 0.222 | 0.211 | 0.201 | 0.194 | 0.187 | 0.181 | 0.176 | 0.171 |
| $C_D + C_S$ (nF) | 2.93 | 1.67 | 1.20 | 0.974 | 0.827 | 0.730 | 0.658 | 0.597 | 0.556 |
| $C_S$ (nF) | 2.69 | 1.45 | 0.99 | 0.773 | 0.633 | 0.543 | 0.477 | 0.421 | 0.385 |

Table 4.2

Here again $C_S$ is large compared with $C_D$ representing a surface state density in excess of $10^{12}$ states/$cm^2$/eV. In addition, the value assumed for $C_I$ is an order of magnitude higher than that predicted from the interferometer measurements. If $1/C_D^2$ is plotted against the d.c. voltage expected across $C_D$, i.e.

$$V_D = \frac{V C_I}{C_I + C_D + C_S} \qquad (4.4)$$

the resulting curve is not a straight line but is convex upwards. The voltage intercept is at about 3 volts, an unrealistically high value unless an interfacial layer similar to that described by Cowley (1966) is present, and this is excluded in the assumed surface state model.

Another difficulty is that the relaxation of the capacitance between low and high frequency in Figure 4.4 is less steep than for a perfect Debye relaxation curve, however this can be explained by the surface state model. The simple Debye relation only applies for a single level interface state. Introducing a continuum of states, creates an infinite series of $R_{si} C_{si}$ combinations in parallel, which has the effect of broadening the capacitance step. The presence of statistical fluctuations in the surface potential of the semiconductor provides a further mechanism for this broadening.

## 4.4 A Modified Model

The calculations described in the previous section suggest that the network of capacitors and resistors of the interface state model is not adequate to explain the capacitance and conductance results obtained experimentally. In order to account for the large measured capacitance when the insulator capacitance is estimated to be smaller, an insulator leakage is introduced, as a conductance in parallel with the insulator capacitance; and in order to simplify the resulting model, as a first approximation, the interface state components $R_S$ and $C_S$ are neglected. This creates the network shown in Figure 4.7.

### 4.4.1 High and low frequency limits

To compare the validity of this model with the experimental results, the low and high frequency limits will again be investigated. The high frequency limit simply yields the insulator capacitance in series with the depletion capacitance, while the low frequency limit consists of the depletion capacitance in series with the insulator resistance. If $\omega C_D R_I << 1$ then the capacitance measured reduces to $C_D$.

Table 4.3 gives the depletion capacitance simply taken to be the low frequency measured capacitance. The insulator capacitance may then be calculated at different voltages from the measured high frequency capacitance, $C_{mh}$, according to the equation

$$C_I = \frac{C_D C_{mh}}{C_D - C_{mh}} \qquad (4.5)$$

| Voltage (V) | 0 | -0.5 | -1 | -1.5 | -2 | -2.5 | -3 | -3.5 | -4 |
|---|---|---|---|---|---|---|---|---|---|
| $C_D$ (nF) | 1.190 | 0.910 | 0.750 | 0.655 | 0.585 | 0.535 | 0.495 | 0.460 | 0.435 |
| $C_I$ (nF) | 0.383 | 0.364 | 0.357 | 0.354 | 0.353 | 0.346 | 0.336 | 0.338 | 0.337 |

Table 4.3

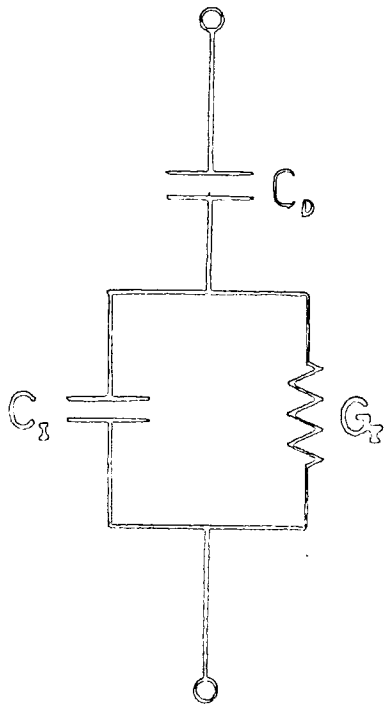
$C_I$ is seen to be constant to within an error of less than ± 10%. This represents good agreement between theory and practice in view of the use of the 10 Hz signal as the low frequency limit and 100 kHz as the high frequency limit. It was used rather than the 220 kHz result since this was measured using a different oscillator. Implicit in this model is the assumption that all the applied d.c. bias is dropped across the depletion region of the semiconductor because of the insulator leakage $R_I$. It is therefore reasonable to predict that a plot of $1/C^2$ versus V in the low frequency limit should yield a straight line with a voltage intercept of the diffusion potential of the semiconductor to insulator interface.

Figure 4.8 shows graphs of $1/C_m^2$ versus V ($C_m$ = measured capacitance) at various frequencies between 10 Hz and 220 kHz, the presence of $R_I$ and $C_I$ increases the intercept voltage as the frequency increases. In contrast, Figure 4.9 shows $1/C_D^2$ versus V for frequencies of 10 Hz and 100 kHz where $C_D$ is as given in equation (4.2) and $C_I$ is taken to be 0.350 nF.

The close similarity of both slope and voltage intercept for these results at frequencies differing by a factor of $10^4$ is yet further evidence for the validity of the proposed model. The values of intercept voltage of between 0.2 V and 0.6 V imply that there is little change in diffusion potential from the basic metal-semiconductor Schottky diode where a band bending of roughly 0.66 V is generally accepted to occur, for a gold contact on cadmium sulphide, (Sze, 1969).

### 4.4.2 Extension to all frequencies

Up to this point only the lowest and highest frequency capacitance data has been considered. The conductance and the rest of the capacitance measurements will now be considered in more detail. From elementary circuit theory, the admittance, $Y_m$, of the arrangement in Figure 4.7 is




Modified MIS Model (proposed)

Figure 4.7

Figure 4.8 $1/C_c^2$ (measured) against Voltage at various frequencies

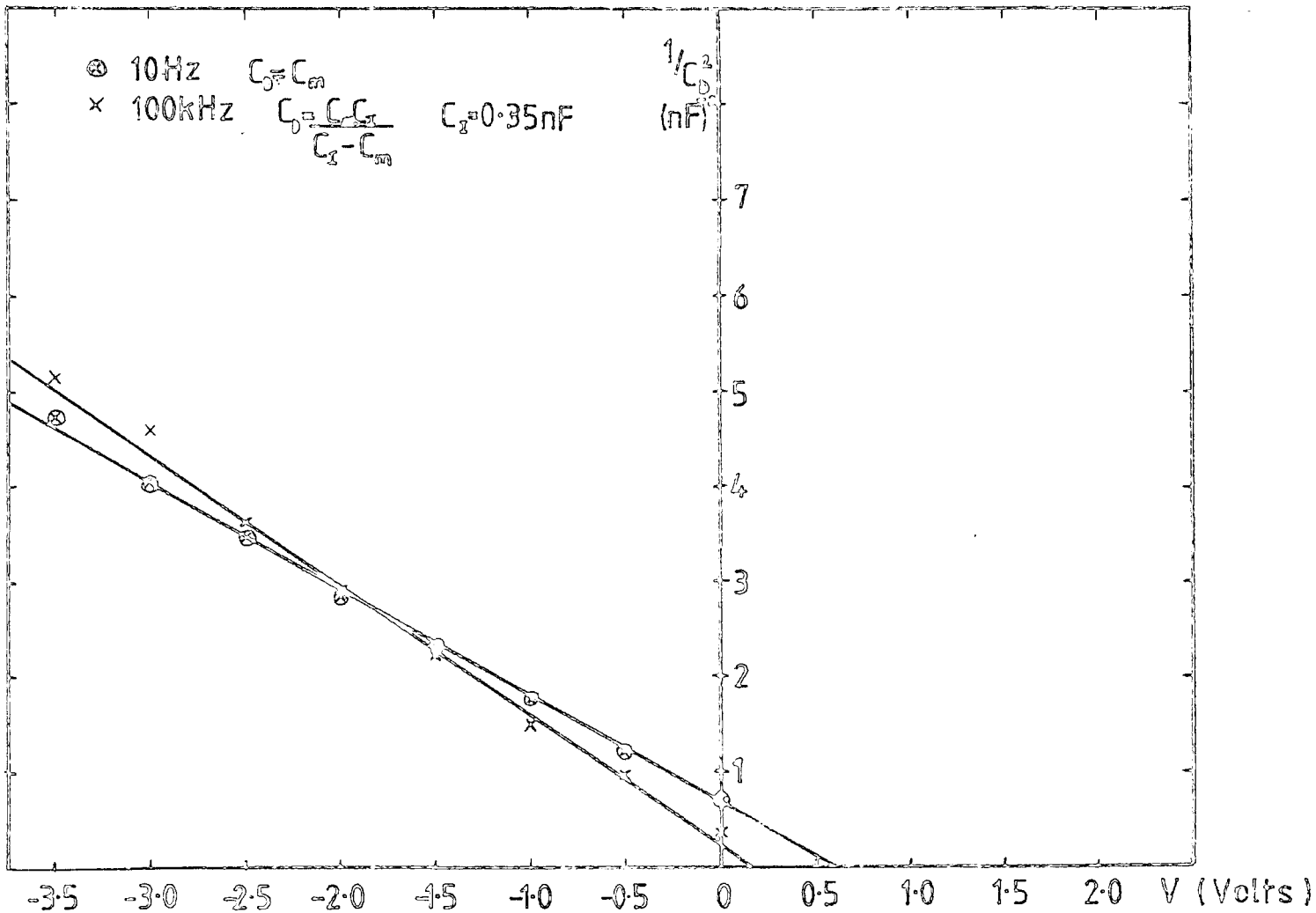



Figure 4.9 $1/C_D^2$(calculated) against Voltage showing similarity at different frequencies

given by:

$$Y_m = \omega \left[ \frac{\frac{G_I}{\omega} C_D^2 + i\left(\frac{G_I^2}{\omega^2} C_D + C_D C_I \left(C_I + C_D\right)\right)}{\frac{G_I^2}{\omega^2} + (C_I + C_D)^2} \right] \qquad (4.6)$$

Splitting $Y_m$ into real and imaginary parts, as measured by the 'Ortholoc', gives

$$Y_m = G_m + i\omega C_m \qquad (4.7)$$

and therefore

$$\frac{G_m}{\omega} = \frac{\frac{G_I}{\omega} C_D^2}{\frac{G_I^2}{\omega^2} + \left(C_I + C_D\right)^2} \qquad (4.8)$$

and

$$C_m = C_D - \frac{C_D^2 (C_I + C_D)}{\frac{G_I^2}{\omega^2} + (C_I + C_D)^2} \qquad (4.9)$$

Differentiation of equation (4.8) with $C_D$ and $C_I$ assumed frequency independent but leaving $G_I$ an arbitrary function of frequency, shows that a maximum value will occur in $G_m/\omega$ for a frequency satisfying the condition that $G_I/\omega = C_I + C_D$ (4.10). This may be compared with the interface model where the equivalent condition is that $\omega\tau = 1$ or $\omega R_S C_S = 1$ (4.11). Estimates for $G_I$, $C_I$ and $C_D$ may be used in equations (4.8) and (4.9) in order to try to fit the experimental results. However, no combination can provide a good fit to the experimental points, because the form of the equations is such that the functional dependence with frequency is fixed regardless of the values of the components $C_I$, $G_I$ and $C_D$. This means that the width of the peak of $G_m/\omega$ according to (4.8) is constant and too narrow to fit the experimental curve. Similarly, the frequency range over

which $C_m$ changes from its upper value of $C_D$ to its lower value of $\frac{C_I C_D}{C_I+C_D}$ is fixed. The denominator in equations (4.8) and (4.9) is responsible for this; it is of the form $1 + \frac{1}{\omega^2\tau^2}$ where $G_I/(C_I + C_D) = \frac{1}{\tau}$.

In order to broaden the theoretical relaxation curve, the normal procedure is to introduce a statistical variation in the Debye-like mechanism creating the phenomenon, thus causing a dispersion of time constants $\tau_i$. In our model, however, we assume that the observed 'relaxation' curves are a consequence of the series combinations of the depletion capacitance with the insulator admittance. Therefore, a frequency dependence for the insulator conductance and capacitance is introduced next.

It can be shown by comparing calculated peak widths that an insulator conductance with a frequency dependence,

$$G_I \propto \omega^{0.6} \tag{4.12}$$

in conjunction with constant values of $C_D$ and $C_I$ gives the correct frequency dependence. Graphs of $C_m$ and $G_m/\omega$ calculated in this way are shown in Figures 4.10 and 4.11 where the experimental points are also shown for reference. The values of parameters used are $C_D$ = 0.875 nF, $C_I$ = 0.4nF, and $G_I/\omega = 23.76\ f^{-0.4}$ nF where f is the frequency measured in Hertz. It is immediately apparent, that while there is an excellent fit to the capacitance data, the conductance curve is nearly a factor of two too great throughout. Altering the assumed values to make the conductance fit, would only reduce the low frequency capacitance and increase the high frequency capacitance, thus making a poor capacitance fit.

It is therefore necessary to vary another parameter, the insulator capacitance $C_I$. This is regarded as being made up of a frequency dependent part $C_A \propto \omega^{n-1}$ and a constant part $C_B$, the reason for this will be discussed later. With these assumptions:

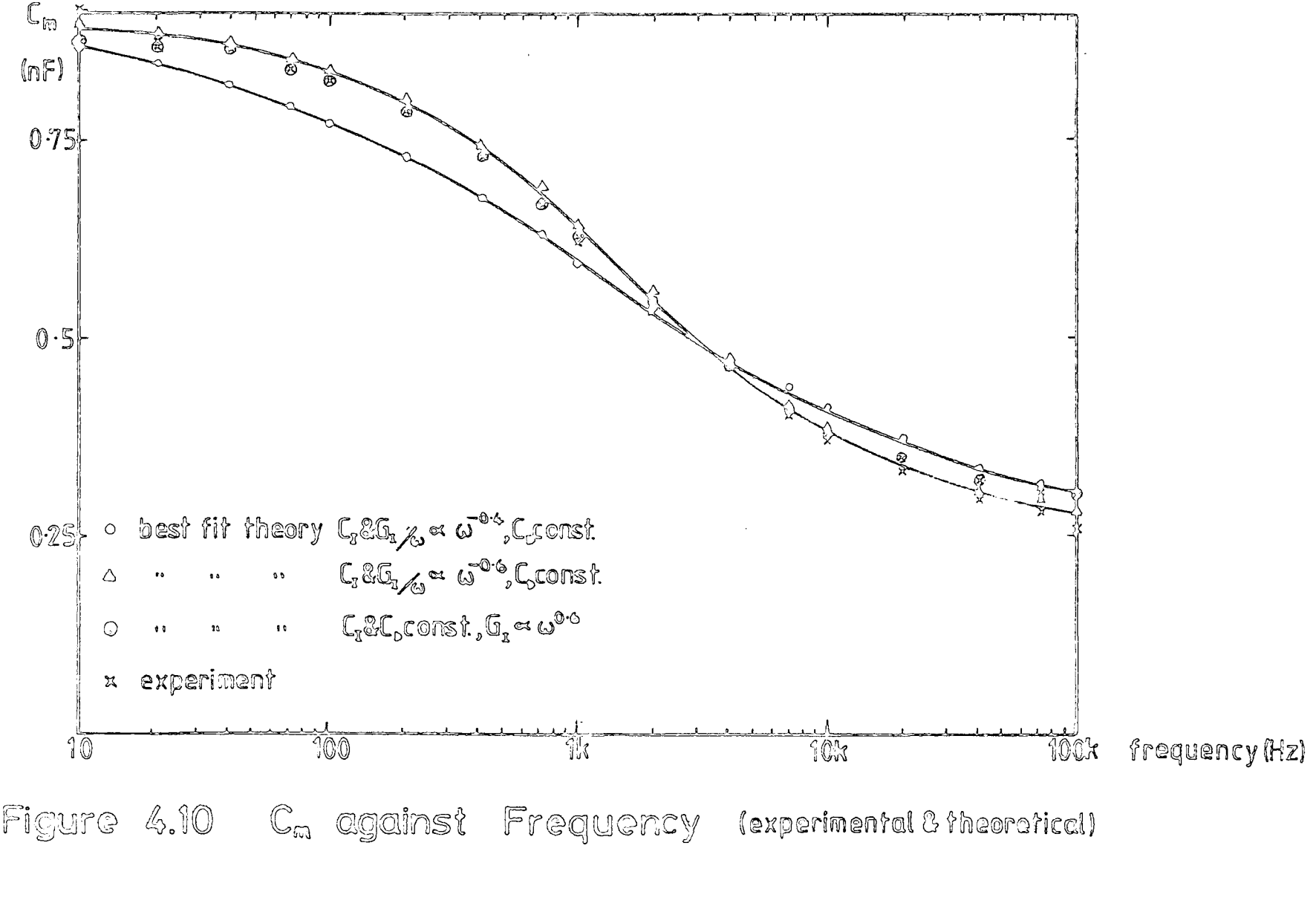



Figure 4.10 $C_m$ against Frequency (experimental & theoretical)

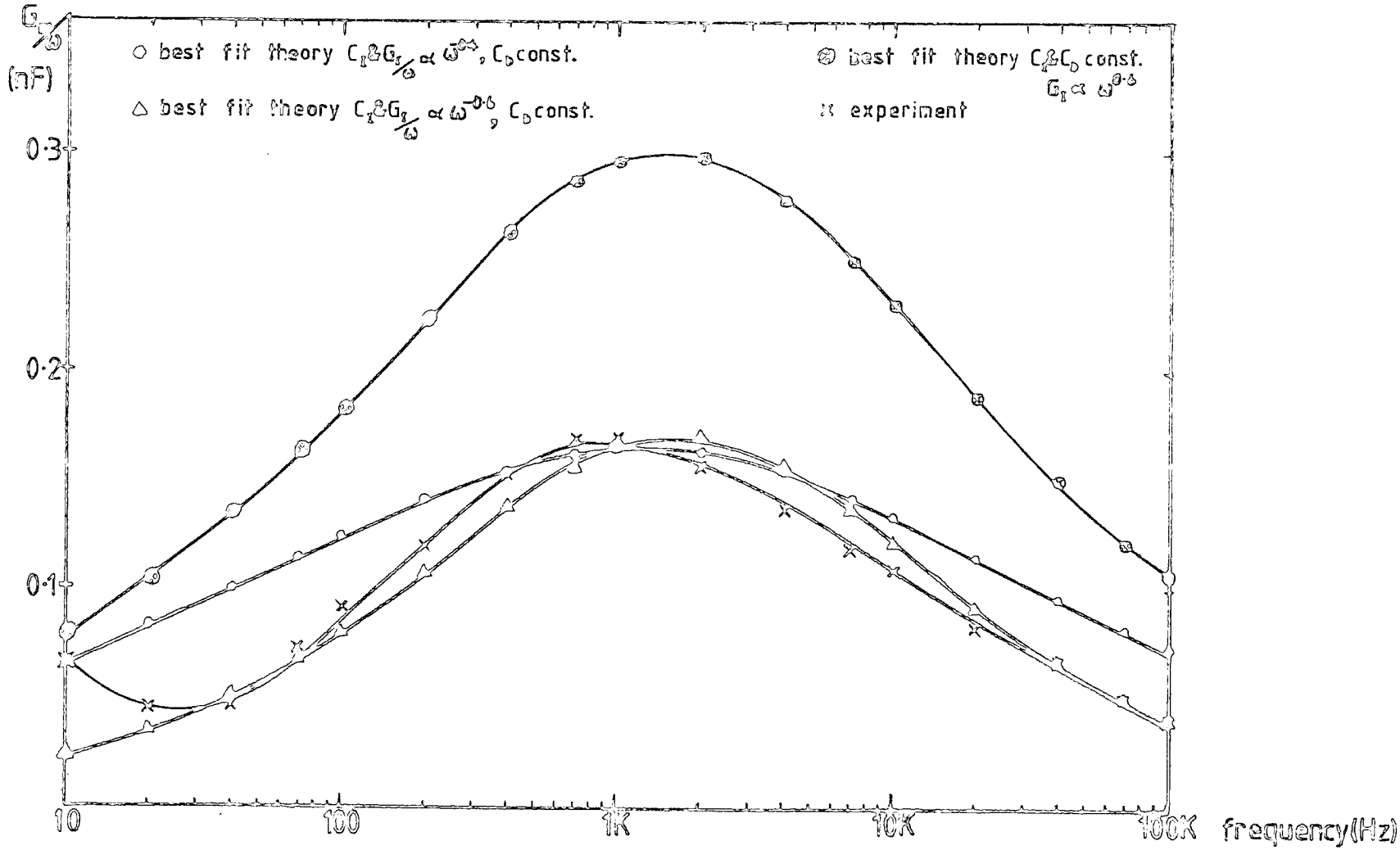



Figure 4.11 $G/\omega$ against Frequency (experimental & theoretical)

$$C_I = C_A + C_B \tag{4.13}$$

$$\doteq A\omega^{n-1} + B \tag{4.14}$$

where

$$G_I = D\omega^n \tag{4.15}$$

This gives an insulator admittance of

$$Y_I = D\omega^n + iA\omega^n + i\omega B$$

$$= (D + iA)\omega^n + i\omega B \tag{4.16}$$

Under these conditions, equation (4.9) still yields a value of $C_m = C_D$ at low frequencies and at high frequencies instead of $C_m = \frac{C_I C_D}{C_I + C_D}$, $C_m = \frac{C_B C_D}{C_B + C_D}$ which is basically of the same form. With the previous cases it is easily shown that the frequency at which $G_m/\omega$ is a maximum, is equal to that at which $C_m$ is the average of $C_{max} = C_D$ and $C_{min} = \frac{C_I C_D}{C_I + C_D}$, i.e.

$$C_m = C_D - \frac{C_D^2}{2(C_I + C_D)} \tag{4.17}$$

It is important to know whether this is true for this case also. Equations (4.8) and (4.9) now become

$$G_m/\omega = \frac{D\omega^{n-1} C_D^2}{D^2\omega^{2n-2} + (B + C_D + A\omega^{n-1})^2} \tag{4.18}$$

and

$$C_m = C_D - \frac{C_D^2 (B + C_D + A\omega^{n-1})}{D^2\omega^{2n-2} + (B + C_D + A\omega^{n-1})^2} \tag{4.19}$$

At the maximum

$$\frac{d(G_m/\omega)}{d\omega} = 0$$

$$G_m/\omega = \frac{D\,C_D^2}{D^2\omega^{n-1} + \left((B+C_D)\omega^{-(\frac{n-1}{2})} + A\omega^{\frac{n-1}{2}}\right)^2}$$

therefore

$$\frac{d(G_m/\omega)}{d\omega} = \frac{D\,C_D^2\left[(n-1)(D^2+A^2)\omega^{n-2} - (n-1)(B+C_D)^2\omega^{-n}\right]}{\left[D^2\omega^{n-1} + \left((B+C_D)\omega^{-(\frac{n-1}{2})} + A\omega^{\frac{n-1}{2}}\right)^2\right]^2}$$

$$= 0$$

therefore

$$(n-1)(D^2+A^2)\omega^{n-2} = (n-1)(B+C_D)^2\,\omega^{-n}$$

$$\omega^{2n-2} = \frac{(B+C_D)^2}{D^2+A^2} \qquad (4.20)$$

Putting this value of $\omega$ into equation (4.19) and simplifying it leads to

$$C_m = C_D - \frac{C_D^2}{2(B+C_D)} \qquad (4.21)$$

which has exactly the same form as (4.17).

In order to test the frequency dependence of $C_I$ and $G_I$ in this model, the same dependence as that shown for $G_I$ previously, i.e. $n = 0.6$, was arbitrarily adopted for $C_I$ also. The values of the parameters were $C_D = 0.92$ nF, $C_I = 0.3 + 13.17\ f^{-0.4}$ nF and $G_I/\omega = 16.17\ f^{-0.4}$ nF. The values of $C_m$ and $G_m/\omega$ resulting from the use of these components are also shown in Figures 4.10 and 4.11. It is clear that while the magnitudes

of both curves are now approximately correct, the frequency dependence is too weak. Study of the shape of the $G_m/\omega$ curve reveals that the correction required to fit the frequency dependence of $G_I$ and $C_I$ is to reduce n from 0.6 to 0.4. The parameters used next were $C_D = 0.9$ nF., $C_I = (0.35 + 60.36\, f^{-0.6})$nF and $G_I/\omega = 88.52\, f^{-0.6}$ nF. The curves obtained by using these values are also shown in Figures 4.10 and 4.11. At last it is apparent that a good fit to the experimental points has been obtained for both the magnitude and frequency dependence of the capacitance and conductance.

### 4.4.3 Alternative method of analysis

A different way of finding $G_I$ and $C_I$ is, of course, to invert equations (4.8) and (4.9) to give $G_I$ and $C_I$ directly i.e.

$$G_I/\omega = \frac{G_m/\omega \; C_D^2}{(G_m/\omega)^2 + (C_D - C_m)^2} \qquad (4.22)$$

and

$$C_I = -C_D + \frac{C_D^2 (C_D - C_m)}{(G_m/\omega)^2 + (C_D - C_m)^2} \qquad (4.23)$$

$G_I/\omega$ and $C_I$ calculated for diode 637/5 are shown in the next figure (Figure 4.12).

The errors in $C_I$ and $G_I/\omega$ at low frequencies can be very large indeed. For example, an error of 10% in $C_D$ and $C_m$ could produce an error of several hundred per cent in $C_I$ because at low frequencies $C_D \approx C_m$. Also shown in Figure 4.12 is the frequency dependent part of $C_I$ alone, where the constant part has been estimated as 0.35 nF, $G_I/\omega$ and $C_A$ are evidently the same function of frequency, to within experimental error.

Values of $C_I$ and $G_I/\omega$ obtained from a similar diode 637/8 immediately after fabrication are shown in Figure 4.13. Here there

appeared to be two regions of different frequency dependence ; this will be discussed later.

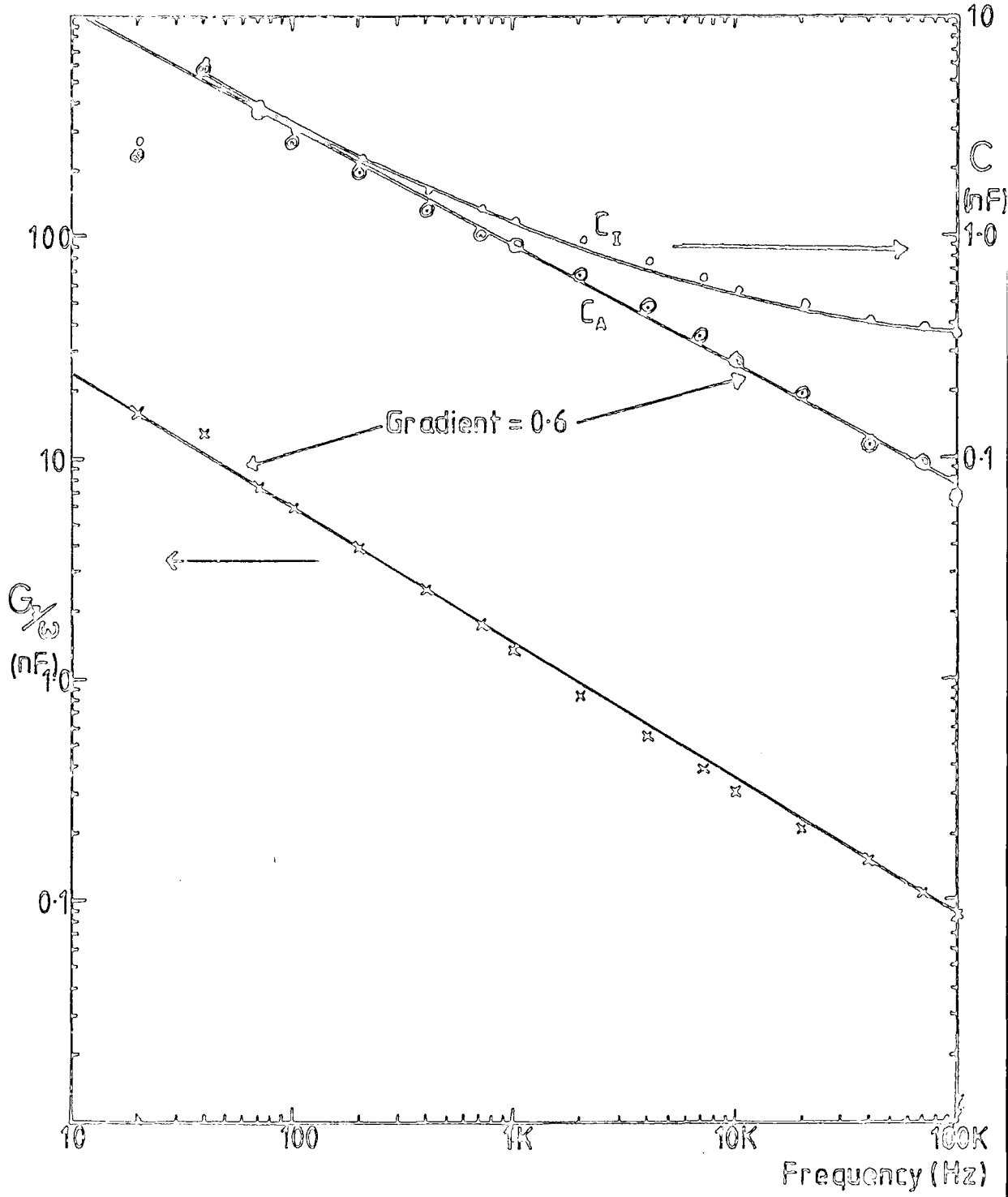
To ascertain whether the insulating film could be rendered mechanically more stable, it was subjected to two periods of a heat treatment in argon at 150° C ; 30 minutes followed by one hour. After each heating the device was remeasured. Both sets of values of $G_m$ and $C_m$ were the same to within experimental error, so that the results of the last measurements only are shown in Figure 4.14.

The values of components used in these calculations were $C_B$ = 0.7 nF and $C_D$ = 1.75 nF for the device as made and $C_B$ = 0.28 nF and $C_D$ = 1.35 nF after the heat treatments. Originally the slopes of $G_I/\omega$ and $C_I$ correspond to a frequency dependence of $\sim$ -0.33 at low frequency and -0.61 at high frequency. After heating the slopes are uniform throughout the frequency range with a gradient of -0.5. The peak of the corresponding measured conductance curves, $G_m/\omega$ versus $\omega$ shifted from 1 kHz initially to 20 Hz. It is important to notice that the heat treatment reduced the frequency dependent part of $C_I$ and $G_I/\omega$ by a factor of about 10.

## 4.5 Discussion

The considerations outlined above show firstly that it is quite impossible to explain the experimental measurements in terms of the interface state model of Nicollian and Goetzberger (1967) or its subsequent modifications. The simplest suitable model is a three component one of insulator capacitance and conductance, and depletion capacitance. It proved necessary to introduce a frequency dependent conductance in order to obtain a reasonable fit to the experimental curves. Closer inspection revealed that it was impossible to fit both the conductance and capacitance curves with the one set of parameters. A composite insulator capacitance was then introduced consisting of a constant part together with a variable part with the same frequency dependence as $G_I/\omega$.

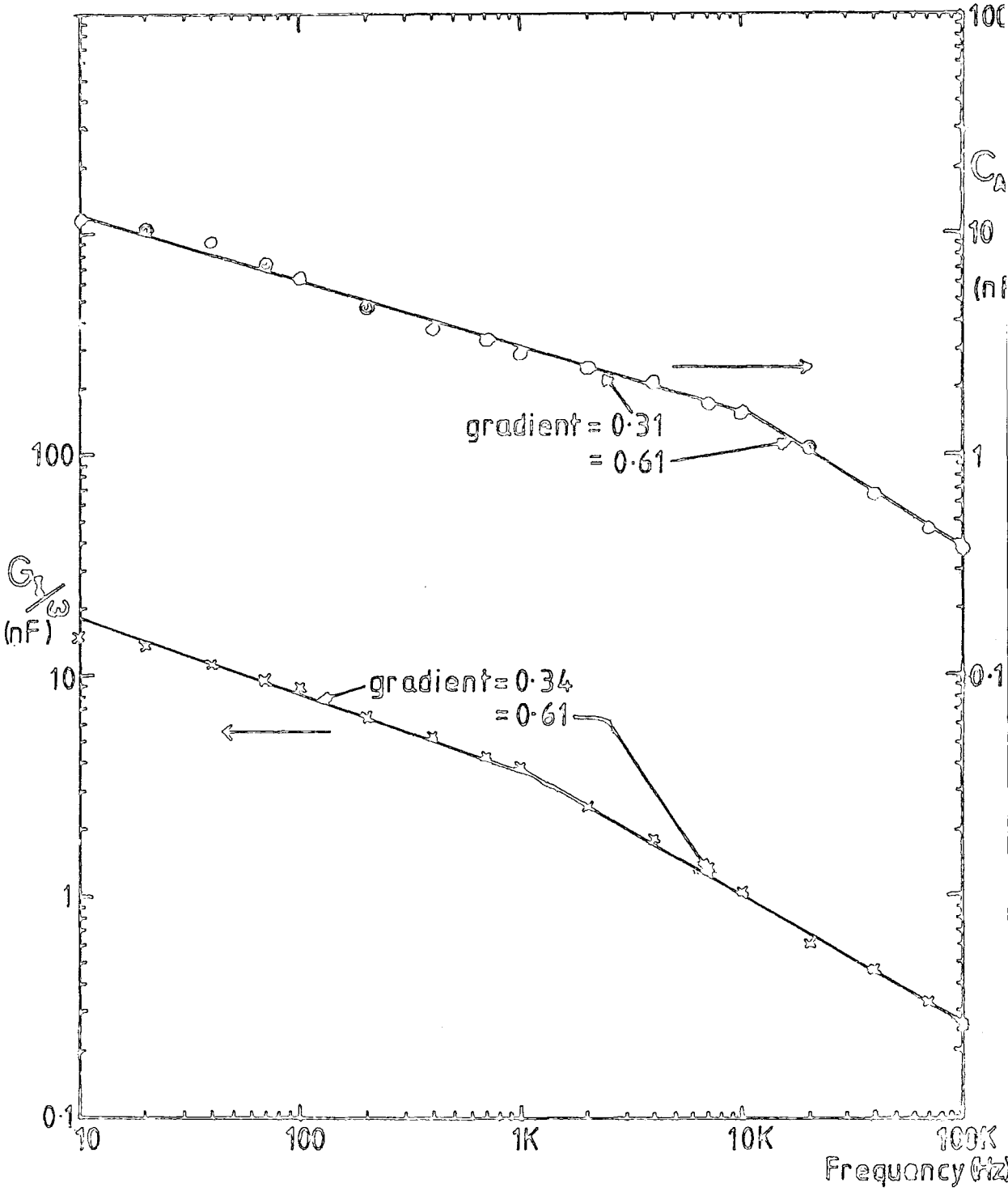
Device 637/5




Calculated Insulator Capacitance and Conductance against Frequency ($C_I = C_A + 0{\cdot}35nF$, $C_0 = 0{\cdot}9nF$)

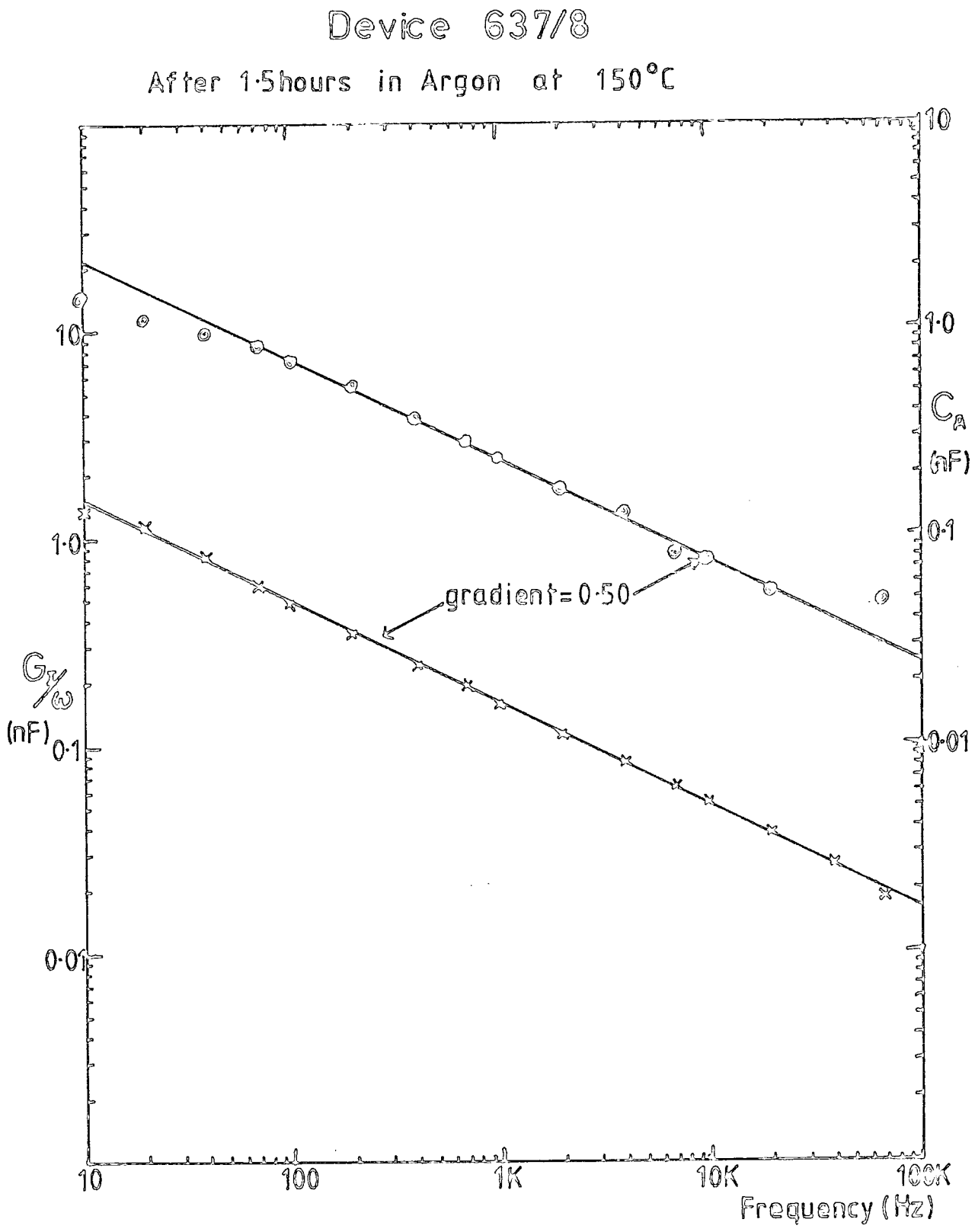
Figure 4.12

Device 637/8




Calculated Insulator Capacitance and Conductance against Frequency ($C_s = C_A + 0{\cdot}7nF$, $C_D = 1{\cdot}75nF$)

Figure 4.13




Calculated Insulator Capacitance and Conductance against Frequency ($C_I = C_A + 0{\cdot}28$nF, $C_I = 1{\cdot}35$nF)

Figure 4.14

This assumption allowed an extremely good fit to be obtained after the value of n had been suitably adjusted to 0.4.

A literature search revealed that a large number of papers have been published describing various aspects of the mechanisms of current flow in dielectric films of silicon monoxide, all concerned with MIM or Metal Insulator Metal Structures which are obviously easier to analyse than the MIS diode. The main conclusion from these papers is that the sample preparation conditions are of paramount importance in determining the current flow in the material. It appears that there may be up to four different mechanisms of d.c. conduction occurring under different conditions of temperature and electric field. It is generally accepted that at low fields and relatively high temperatures, conduction is due to mobile positive ions, (Argall and Jonscher, 1968; De Wilde and De Mey, 1976) possibly sodium ions which are highly mobile. This region is characterised by a linear (ohmic) current-voltage characteristic and time dependent effects. Another low field mechanism which is electronic in nature resembles space charge limited current flow in crystalline materials with its $I \alpha V^2$ characteristic (Servini and Jonscher, 1969). At high fields and low temperature ( $\sim$ 77 K) a mechanism associated with tunnelling between closely spaced centres occurs with a very steep $I \alpha V^n$ power law dependence.

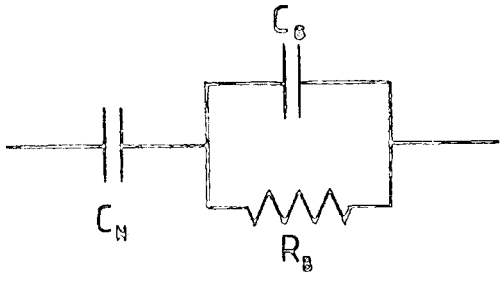
The most important method of current flow is that occurring at high fields and moderate temperatures characterised by a relationship of the form $\log I \alpha V^{\frac{1}{2}}$. This is consistent with either a Poole-Frenkel bulk mechanism or with Schottky lowering of the barrier limited injection at the cathode. The Poole-Frenkel process is favoured by De Mey and De Wilde (1974) because symmetrical characteristics were observed for films between two different electrodes. In addition it is extremely unlikely that all carriers injected at the electrodes would be able to propagate freely across the amorphous insulating film.

According to Zdanowicz and Zielinska (1977), both Poole-Frenkel bulk conduction and Schottky barrier conduction can occur in SiO Metal-Insulator-Metal structures; they find that two types of conduction occur, one stable and the other unstable. The unstable one is assumed to be Poole-Frenkel in nature with a constant field through the sample, while the other is a Schottky mechanism with a space charge region (stable equilibrium). The latter mechanism becomes more important at relatively higher temperatures and lower voltages.

The observations above apply to thermally evaporated films. However, a further complication is introduced in electron-beam evaporated samples where Roger et al (1975) have shown that while the I-V data is consistent with Poole-Frenkel conduction, the capacitance is a function of bias, resulting from the formation of a space charge region at the positive electrode. This explains simply the a.c. dispersion of capacitance with frequency they observe, as due to a capacitance resistance equivalent circuit (Figure 4.15), similar to the model proposed earlier to explain our results. This appears to agree substantially with the 'Simmons Model' (Simmons 1968) for a.c. conduction in insulating films, which consists of a Schottky barrier region next to each contact, and an interior conductive region as shown in Figure 4.16.

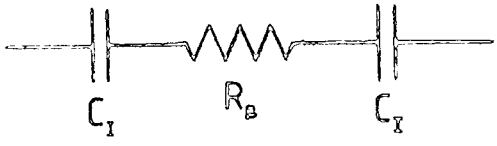
Bigorgne et al (1974) report a.c. measurements of capacitance and conductance on thermally evaporated thin films of SiO which they explain in terms of the Simmons model. It seems perhaps more realistic to interpret both these sets of results in terms of ion movement rather than electronic conduction, i.e. in terms of interfacial polarisation, as the relaxation frequencies are very low $\sim$10 Hz; this transport mechanism was suggested by Argall and Jonscher (1968) for low fields.

Another a.c. conduction mechanism has been suggested by Argall and Jonscher (1968) and extended by Adachi and Shibata (1975) which utilises the two-site hopping model. In this model a distribution of pairs of




$C_N$= -ve space charge capacitance at +ve contact
$C_D$= bulk capacitance
$R_D$= " resistance

Figure 4.15 Equivalent circuit of metal/SiO/metal structure
(after Roger et al., 1975)




$C_I$=interface capacitance
$R_D$=bulk resistance

Figure 4.16 Equivalent circuit of Au/SiO/Al structure
(after Simmons et al., 1968)

potential wells is separated by a distance 2a and a potential barrier of height $W_o$. One electron is normally assumed to occupy each pair of levels and may be accommodated in either position in thermal equilibrium. Application of a field lowers the barrier and makes occupation of one state more likely than the other. Using this model Adachi et al(1978b) explain the observed lowering of capacitance with increasing d.c. bias at low frequencies to be due to preferential polarisation of pairs with longer time constants by relatively lower d.c. biasing voltages. Since a longer time constant implies a higher activation energy, such pairs will be 'frozen out' with increasing frequency causing the relaxation frequency to increase and the activation energy to decrease. This fitted the experimental observations but the reason for the preferential polarization was not explained.

In another paper, Adachi et al(1978a) show that the measured a.c. conductance $\sigma_T(\omega)$ can be expressed as $\sigma_T(\omega) = \sigma_o + \sigma_1(\omega)$ where $\sigma_o$ is a constant and $\sigma_1(\omega)$ varies approximately as $\omega^{0.66}$ above the relaxation frequency over a range of four decades of frequency. Frost and Jonscher (1975) agree about the form and frequency dependence of the conductance, but their work suggests that $\sigma_1(\omega) \alpha \omega^{0.6}$ over eight decades without the existence of a relaxation frequency. This conductance is related to $\chi''(\omega)$ the imaginary part of the dielectric susceptibility

$$\chi = \varepsilon/\varepsilon_o - 1 = \chi'(\omega) - i\chi''(\omega)$$

since

$$\sigma_1(\omega) = \varepsilon_o \omega \chi''(\omega) \qquad (4.24)$$

$$\chi''(\omega) = A\omega^{n-1} \text{ where } n = 0.6 \qquad (4.25)$$

as a consequence of the Kramers-Kronig relations, the real part of the susceptibility

$$\chi'(\omega) = A \tan(n\pi/2)\, \omega^{n-1} \qquad (4.26)$$

Since the measured values of capacitance are proportional to $\varepsilon_r'$ $\chi'(\omega)$ may be calculated using the relation $\chi'(\omega) = \varepsilon_r'(\omega) - \varepsilon_\infty$, where $\varepsilon_\infty$ is the contribution to $\varepsilon_r'$ of all loss mechanisms above the frequency range of the present loss mechanism.

In terms of the experiments reported earlier in this chapter following the theories of Frost and Jonscher, $\chi'(\omega) \propto C_A$, $\varepsilon_r'(\omega) \propto C_I$ and $\varepsilon_\infty \propto C_B$. However, the values of n found in the present work, for various samples are not 0.6 as reported by the last-mentioned authors, but varied between 0.4 and 0.7. No obvious reason for this is apparent, and it must therefore be ascribed to impurities in the $SiO_x$ layer, non-stoichiometry of the $SiO_x$ or the influence of a native oxide beneath the $SiO_x$ layer. With the sample which received the heat-treatment the two loss mechanisms (characterised by the two different slopes) present in the sample immediately after fabrication, appear to have been replaced by one only, after 1½ hours annealing in Argon at 150°C. While this resulted in a decrease of ∿25% in the depletion capacitance, probably due to the contact area becoming smaller during heating, the decrease in the value of the constant part of the insulator capacitance $C_B$ was ∿60%. This may have been due in part to a decrease in the loss mechanisms following the annealing.

Finally some discussion of the d.c. breakdown of the SiO films is required. From the original measured curves Figures 4.2 and 4.3, it is apparent that at voltages above 0.2 V in forward bias or 6 V in reverse bias the a.c. conductance began to increase very rapidly. This corresponds to avalanching of the d.c. current and some type of localised breakdown obviously occurs. The mechanism for this is not known but some studies of its properties, in particular its dependence on the nature of the semiconductor surface, will be presented in the following chapter. A certain hysteresis was observed in the current-voltage characteristics of the devices which suggests that ion movement may be an influence in the

breakdown. The net charge accumulated at the rough cathode surface may lower the barrier for electron injection locally causing the observed reversible breakdown. For a detailed treatment of dielectric breakdown see, for example, J.J. O'Dwyer,'The Theory of Dielectric Breakdown in Solids.' In the preceding analysis, the effect of shunting paths through the insulator has been assumed to be negligible at the low reverse biases used. $G_I \propto \omega^n$ fits well over four orders of frequency magnitude and this would appear unlikely to be so if shunting paths were important.

## 4.6 Final Considerations

The errors in the measurements using the 'Ortholoc' are estimated to be $\sim 2\%$ where the capacitance and conductance are within the ratio 10 : 1, the error in the smaller quantity increases to about 6% as the real and imaginary parts are increased to 100 : 1. A reasonable estimate of the error in the assumed value of depletion capacitances $C_D$ is 5%, thus the error in $C_I$ at low frequencies can be greater than 100% whereas at high frequency it reduces to at worst about 12%. The error in $G_I/\omega$ at low frequency is similar to that in $C_I$ as it is caused by the same subtraction, $(C_D - C_m)$, of quantities of similar magnitudes. At high frequency the error reduces to about 15%. It is obvious that a method such as this is unsuitable for a serious study of the conduction processes within insulators as the analysis is complicated by the presence of the space charge region of the semiconductor. For example, it is impossible to support or discount the presence of a space charge layer in the SiO layer, suggested by several authors, because the value of $C_D$ used could in reality be composed of a true depletion capacitance for the semiconductor in series with the space charge capacitance of the SiO.

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# CHAPTER 5

# SCANNING ELECTRON MICROSCOPY OF MIS DEVICES

## 5.1 Introduction

In order to discover more about the topography and electrical properties of the cadmium sulphide surface both with an insulating film deposited, and with other surface treatments, a study was undertaken using a scanning electron microscope, Cambridge Instruments S600. Three modes of operation were employed,

(a) Secondary Emission (or S.E.)

(c) Cathodoluminescence (or C.L.)

(c) Electron Beam Induced Current (or EBIC)

A brief description of the scanning electron microscope and these modes follows.

## 5.2 Operation of the Scanning Electron Microscope

A schematic drawing of a scanning electron microscope (S.E.M.) is shown in Figure 5.1. The basic principle of operation is that an electron beam scans the sample, and the secondary electrons emitted are collected. They then provide the z (or contrast) modulation signal directly or indirectly to a cathode ray tube, the beam of which is being scanned using the same deflection signal as the sample beam.

### 5.2.1 The Secondary Emission Mode

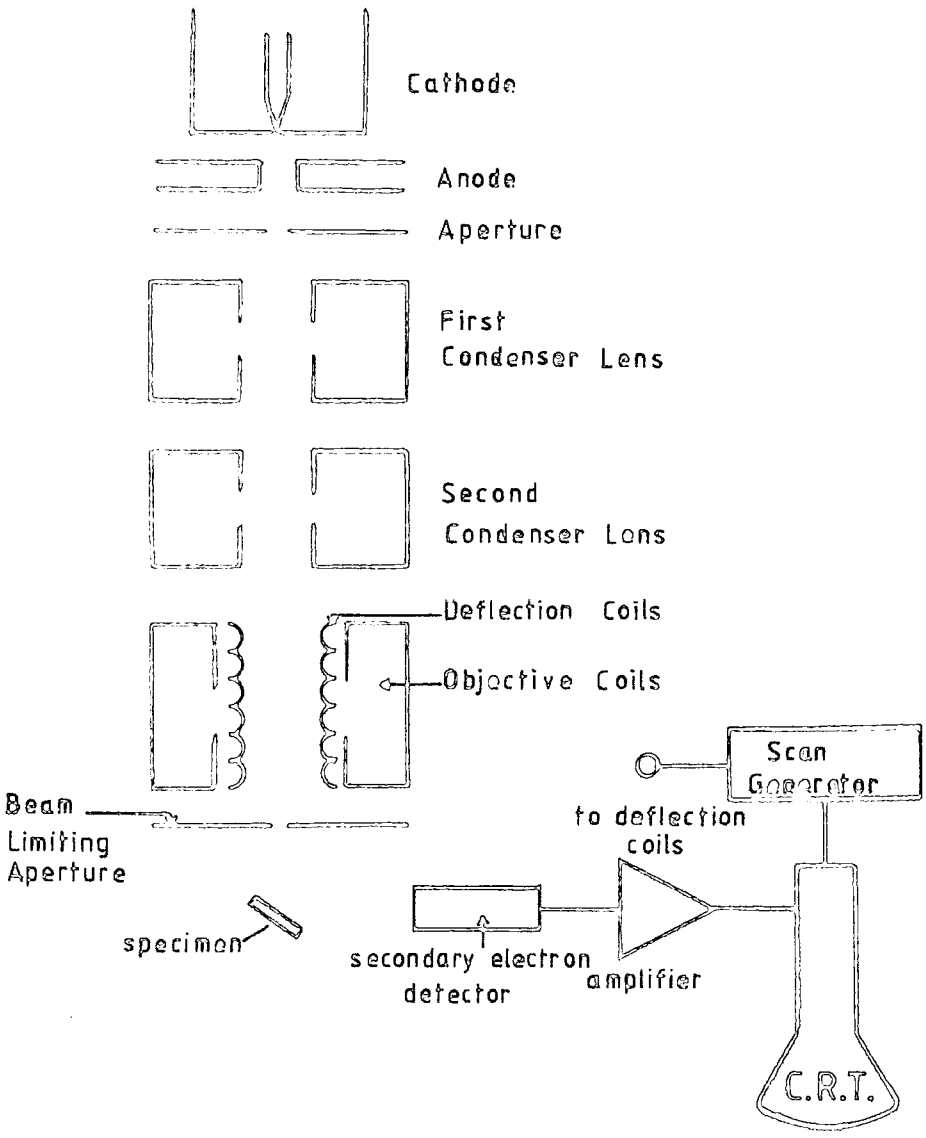
The secondary electrons emitted by the sample are collected by an Everhart-Thornley detector. This is essentially a scintillator and photomultiplier arrangement, consisting of a collector which is a Faraday cage with a metal mesh front; this is biased at +250 V. After passing through the mesh, the electrons are accelerated to strike a scintillator attached to a light-pipe. This is achieved by applying 10 kV between a thin layer

of aluminium deposited on the scintillator and the mesh. The light-pipe transfers the resulting light signal to a photomultiplier tube. This system is adopted as its output is linear with electron signal over a wide range, has a large band-width and creates very little noise. The contrast in this mode is a result of the angle at which the electron beam strikes the surface, i.e. more secondary electrons are emitted for grazing incidence, where the beam is absorbed nearer the surface than for normal incidence (Murata et al 1971). The angular distribution of the secondary electrons is also important.

Contrast may also be produced when parts of the surface are at different potentials; this is referred to as voltage contrast and was first observed by Oatley and Everhart in 1957. The electron signal collected depends on the voltage between the specimen and the collector mesh, so that areas at lower voltages give larger signals.

### 5.2.2 Cathodoluminescence

In the cathodoluminescent or C.L. mode the light produced by electrons striking the sample is collected by a light-pipe and fed directly to the photomultiplier tube. A problem in studying C.L. is that of the low intensity of light produced compared with electrons emitted. Thus more amplification is required and the signal is more noisy. Additionally, the spatial resolution of C.L. is much poorer, since compared with S.E. where secondary electrons are emitted from within 500 Å of the surface, light is produced by recombination mechanisms extending further (x 10) into the bulk. Figure 5.2 shows a summary of the range and spatial resolutions of the processes resulting from the interaction of the incident electron beam with the specimen. The C.L. mode is chiefly used for the observation of crystalline defects near the surface. These act as recombination centres to excited electrons causing non-radiative transitions, and consequently a lack of signal from that area. Examples of what may




Schematic Diagram of the
Scanning Electron Microscope (S.E.M.)
Figure 5.1

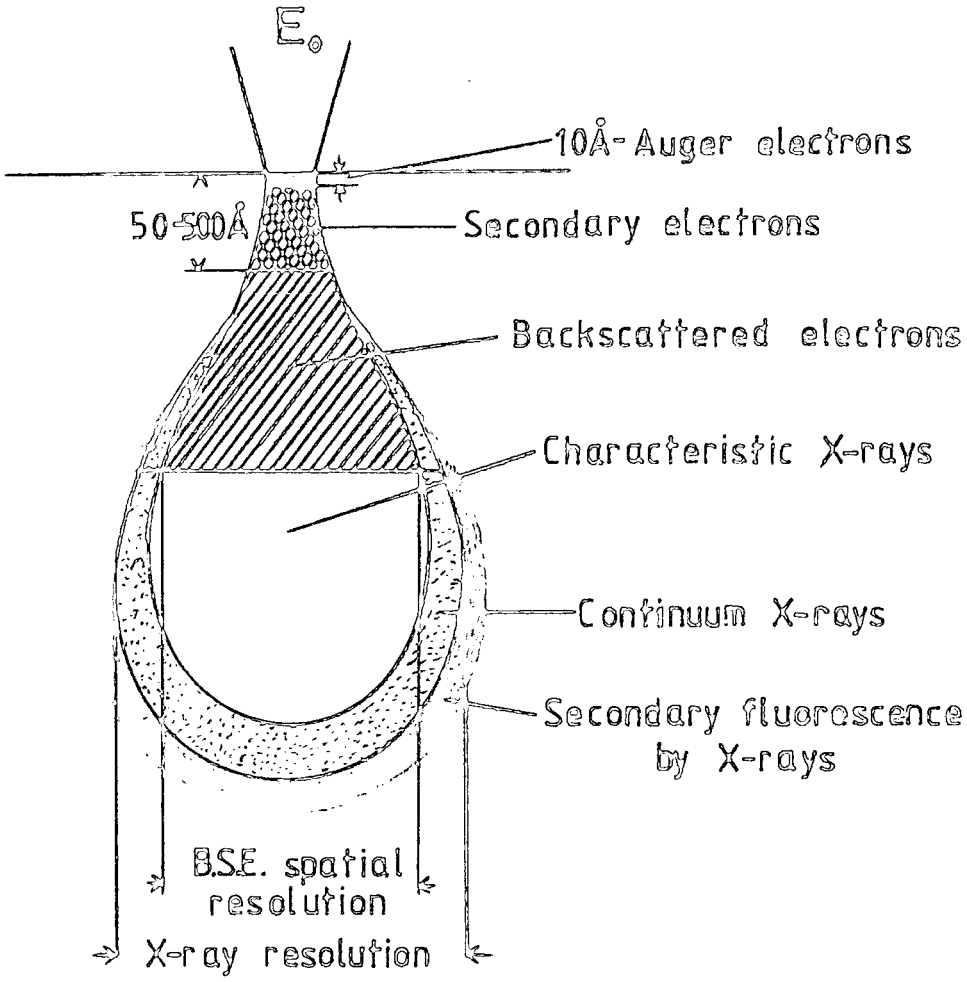



Figure 5.2 Summary of range of electrons and X-rays produced in a scanning electron microscope (from Goldstein)

be seen are dislocations, grain boundaries, defect clusters and precipitates.

### 5.2.3 The Electron Beam Induced Current Mode

The term Electron Beam Induced Current or E.B.I.C. is used to cover a variety of modes of operation, all similar in that the signal is derived directly from the interaction of the electron beam with current flowing in the sample. Holt (1974) describes these modes well, but a brief description will be presented here.

(1) Specimen Current. That part of the beam current which is absorbed by the specimen is collected by an ohmic contact at the base of the sample and passed to earth through a current amplifier. This current creates the image on the C.R.T. As might be expected this technique permits further investigation into the bulk than the secondary emission technique allows, and is less affected by surface topography. The image produced is a consequence of the continuity of beam current, i.e.

$$\Delta i_{SC} = -\Delta i_e \qquad (5.1)$$

where $\Delta i_{SC}$ is a change in the absorbed current and $\Delta i_e$ in the emitted current. Thus the image should be the negative of the S.E. image; however the S.E. current collection is angle dependent whereas absorbed current is not and this results in less shadowing in the latter.

(2) Barrier Electron Voltaic Effect. The definition of the barrier electron voltaic effect (e.v.e.) is the generation of voltages by electron bombardment of regions containing electrical barriers in semiconducting or insulating materials. There is a close analogy between this effect and the barrier photovoltaic effect; in both, a current is caused to flow in a semiconductor p-n junction or Schottky diode, following the absorption

of energetic particles or waves. This phenomenon was first observed by Ehrenberg (1951) and Rappaport (1954). An electrical barrier contains a built-in electric field and this creates the barrier e.v.e. by the separation of holes and electrons which are generated in or near the depletion region by the absorption of the electron beam. These separated pairs can create a potential difference across the junction if the external circuitry is of high impedance. Alternatively if the diode is short circuited, the separated carriers will form a current generator. The number of electron-hole pairs created per electron in the beam, is the generation factor G, given by $G = \frac{E_{eff}}{e_i}$, where $E_{eff}$, the effective energy of the beam is less than the actual beam energy to allow for back-scattered and secondary emission from the surface, and $e_i$ is the average formation energy of electron-hole pairs. Since $E_{eff}$ is of the order of $10^4$ eV while $e_i$ is a few times the semiconductor band gap, G is of the order of $10^3$. G is the theoretical maximum for a collection efficiency of unity. As reverse bias is increased, the depletion region broadens resulting in a larger collection efficiency and a higher current is delivered to an external circuit.

The electron voltaic effect, apart from being a very useful analytical tool, has aroused interest in the device applications field. One such application is the beta voltaic battery, in which beta particles from suitable radioactive sources bombard the junction to produce electrical power (Rappaport, 1954; Pfann and van Roosbroeck, 1954). Another is where an avalanche photodiode is bombarded with an electron beam to provide a useful amplification of over $10^5$ times (Gibbons et al, 1975).

(3) The Bulk Electron Voltaic Effect. The bulk electron voltaic effect is the generation of a voltage across a semiconducting specimen by electron bombardment of a region of non-uniform resistivity. The physical cause for the effect, is the same as for the bulk photovoltaic effect (Tauc 1962). Local variations in resistivity cause the energy

bands to bend, so that local fields must exist. When such a region is subjected to electron bombardment, the bulk e.v.e. is generated by two mechanisms. One is similar to the barrier e.v.e. called the 'chemical' contribution which arises from the separation of electrons and holes by the local field, the other is due to the Dember effect, previously described. At the boundaries of the electron beam, there is a concentration gradient of injected carriers and both holes and electrons will therefore diffuse away. Generally the mobility of the holes will be much lower than that of the electrons, so electrons will diffuse further away. This will not occur symmetrically at opposite edges of the beam if the doping is non-uniform, and this asymmetric separation sets up the Dember voltage.

Munakata (1966,1967) modified the bulk photovoltaic effect to be applicable to bombardment by an electron beam. He neglected the chemical voltage as the field is normally low enough not to alter the diffusive flow of the carriers. The results of his theoretical derivation, show that the sensitivity of the signal increases strongly with the minority carrier diffusion length ($L_p$). In materials with short $L_p$, such as CdS and GaAs, however, the technique does not give sufficient resolution to allow it to be used.

(4) β-Conductivity. This effect resembles that of photoconductivity. The electron beam creates free carriers which lower the resistance of the specimen (Munakata, 1968) and this increased conductivity can be measured simply using a circuit such as that shown in Figure 5.3. The change in conductivity $\Delta\sigma$ will be constant throughout the specimen, but its effect will be position dependent for the following reason.

When the region on which the electron beam is incident has a high conductivity, the total current through the sample remains substantially unaltered; however if the region is of low conductivity a large change in

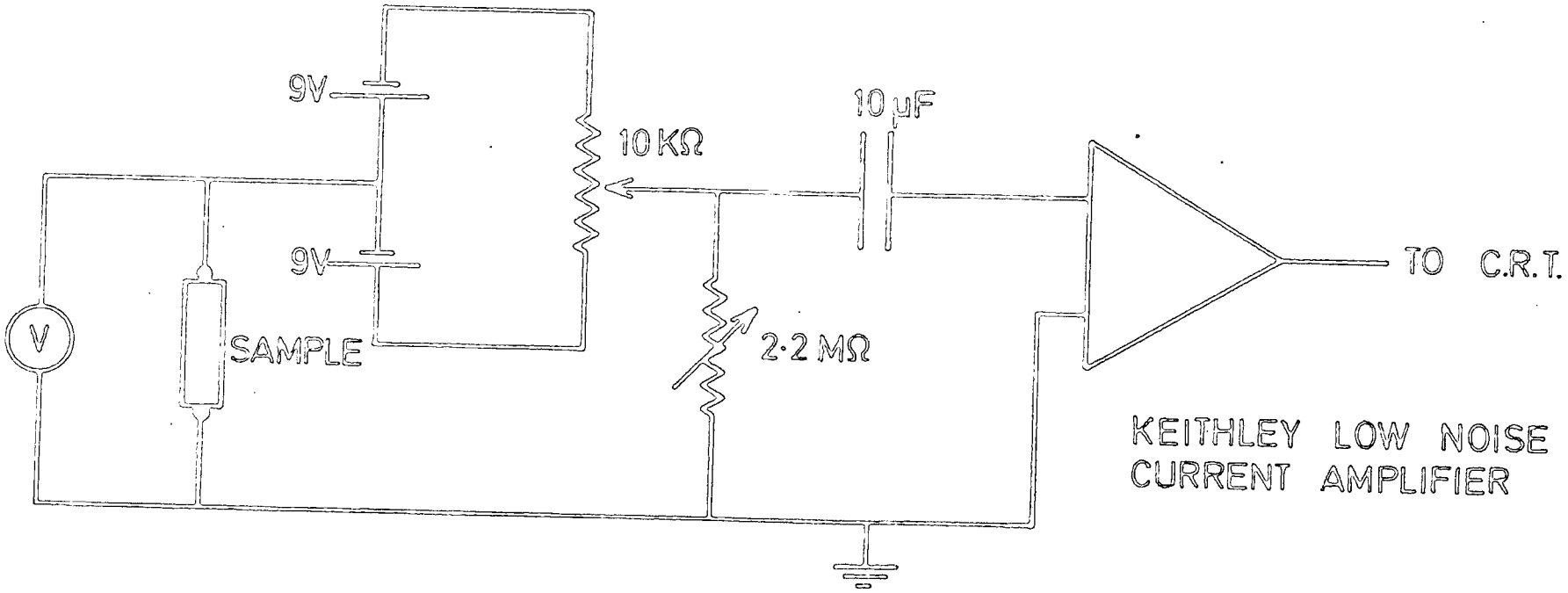



Figure 5.3 Measurement Circuit for β-conductivity

total current will result which will be amplified by the current amplifier. Displaying this output on the C.R.T. allows conductivity variations across the sample to be observed directly.

The circuit shown in Figure 5.3 may also be used to study the effect of applied bias on the barrier electron voltaic effect. If the sample is a Schottky diode most of the applied bias will appear across the depletion region (except in high forward bias), with very little across the bulk, thus the β-conductivity effect will not be important, but the depletion layer may be examined as a function of bias. If, however, there is a resistive surface layer present on the sample, the β-conductivity effect may be the dominant mechanism.

In what follows, the analysis of metal-semiconductor diodes made by depositing gold on CdS subjected to various surface treatments will be described, and later the use of these techniques applied to CdS/$Cu_2S$ p-n heterojunctions. In Appendix A, a study of grain boundaries in ZnSe using the techniques developed here will be reported.

## 5.3 The Analysis Circuit

It is important to check that the image displayed on the S.E.M. used in the EBIC mode, really does represent the conductance or current variations induced in the specimen; in other words, it is necessary to know the characteristics of the detector circuit, as it contains both capacitative and conductive elements.

The circuit may be simplified, initially, by noticing that the 10 kΩ biasing potentiometer is of negligible value compared with the resistance of both the sample and $R_g$ (see Figure 5.4), and that the resistance of the current amplifier is negligible.

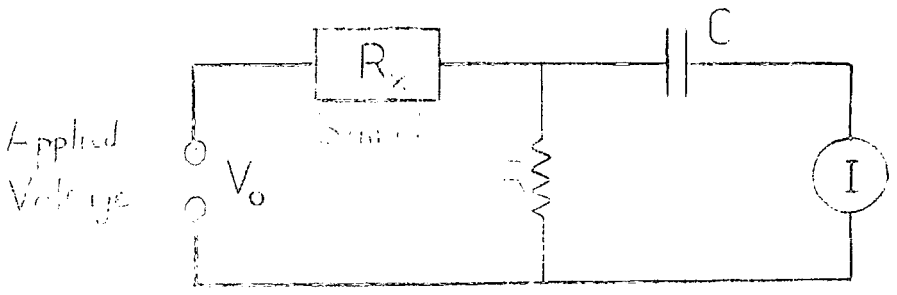



FIG. 5.4

It is assumed initially that the sample may be considered purely resistive, with resistance $R_x$. The circuit can be further reduced using Norton's theorem, to the following form:

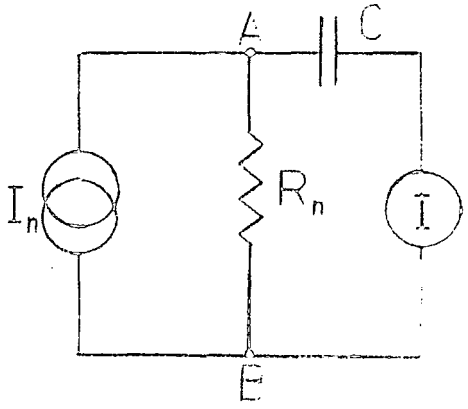



FIG. 5.5

where

$$R_n = \frac{RR_x}{R + R_x} \tag{5.2}$$

and

$$I_n = \frac{V_o}{R_x} \tag{5.3}$$

Assume then, that when the electron beam scans a certain point on the device, the resistance changes from $R_x$ to $R_x + \Delta R_x$, the small signal approximation. The current $I_n$ will consequently change from $I_n$ to $I_n + \Delta I_n$, thus

$$\Delta I_n = \frac{V_o}{R_x + \Delta R_x} - \frac{V_o}{R_x} \tag{5.4}$$

$$\Delta I_n \approx -\frac{V_o \Delta R_x}{R_x^2} \tag{5.5}$$

and the change in $R_n$ ,

$$\Delta R_n = \frac{R^2 \Delta R_x}{(R + R_x)^2} \tag{5.6}$$

If the conductance of the sample is considered instead of the resistance, equation (5.5) becomes

$$\Delta I_n = V_o \Delta G_x \tag{5.7}$$

The instantaneous current, $I_m$, measured by the amplifier in response to the change of resistance $\Delta R_x$ is calculated in the following manner. Since the charge on the capacitor C cannot change infinitely quickly, the voltage across AB in Fig 5.5 must remain unaltered immediately after the impulse, $\Delta I_n$. Now, the current $I_m$ must consist of two parts, one due to the change $\Delta I_n$ and the other due to $\Delta R_n$.

In steady state,

$$V_{AB} = I_n R_n \tag{5.8}$$

following the impulse

$$V_{AB}(\text{unaltered}) = I_{AB} R'_n \tag{5.9}$$

where

$$R'_n = R_n + \Delta R_n \tag{5.10}$$

and $I_{AB}$ is the current through $R'_n$.

Also

$$I'_n = I_{AB} + I_m \tag{5.11}$$

where

$$I'_n = I_n + \Delta I_n \tag{5.12}$$

Rearranging equations (5.11), (5.8) and (5.9) gives

$$I_m = I'_n - \frac{I_n R_n}{R'_n} \tag{5.13}$$

This may be rewritten using (5.10) and (5.12) as

$$I_m = \Delta I_n + \frac{I_n}{R'_n} \Delta R_n \qquad (5.14)$$

From equations (5.2), (5.3), (5.5) and (5.6) this becomes

$$I_m \approx - \frac{\Delta R_x V_o}{R_x (R + R_x)} \qquad (5.15)$$

In terms of conductance variations, equation (5.15) becomes

$$I_m \approx \frac{V_o G \Delta G_x}{(G + G_x)} \qquad (5.16)$$

Therefore, providing that the change in resistance $\Delta R_x$ is small compared with $R_x$, the instantaneous current measured will be proportional to $\Delta R_x$.

It is readily seen that an induced current in a device will produce a similar signal. The current created in either way is in an RC network and will as a result decay exponentially with a time constant given by $R_n C$. It is therefore necessary that $R_n C$ be very much greater than the time taken to scan a region of varying conductivity. An upper limit is imposed on the value of $R_n C$, by the need to be able to alter the bias readily, as this causes a current to flow which also decays with time constant $R_n C$. The values of components chosen were such that with a sample of resistance 1 MΩ, a time constant of ∿1 sec. resulted. The scan speed of the S.E.M. generally used both for an EBIC picture and for a single line graphical display was 18.2 ms. per line, satisfying the aforementioned condition.

The capacitance of a sample will tend to reduce any sudden variations in current induced by the electron beam, rounding sharp edges on current steps. The minority carrier lifetime will also limit the rise time of the observed signal, (Miyazaki et al, 1966; Abraham et al, 1966). Tests for these effects were made in the work which follows, by varying the scan speed until it was sufficiently slow for no change in image to appear with scan speed.

## 5.4 Sample Preparation

Metal-semiconductor diodes were fabricated on several differently prepared surfaces of CdS, namely cleaved, etched, polished and surfaces coated with an insulator. Firstly ohmic indium contacts were applied to the face opposite where the barrier was to be made using gold as the barrier metal. For the cleaved samples a prismatic plane of the hexagonal structure was exposed by carefully cleaving the crystal with a fine blade. Gold evaporation took place at a pressure of less than $10^{-5}$ torr for all the samples considered. CdS of moderate resistivity, $\rho \sim 10^{4}$ Ωcm, was used in this case, as the EBIC signal from low resistivity samples was difficult to measure because noise caused the current amplifier to oscillate.

The etched surface was prepared on the polished sulphur face of the basal plane of a CdS die, by immersion in concentrated hydrochloric acid for 20 seconds followed by washing in methanol. To produce the polished surface, the sulphur face of a sample was first smoothed using 3 μm Aloxite powder and finally polished using 1 μm diamond paste. These devices had a depletion capacitance of ∿ 250 pF. In preparing an MIS device for this study a CdS die was first polished and lightly etched, then a layer of SiO between 1,000 Å and 2,000 Å in thickness was evaporated as previously described using the electron beam deposition system, following which a gold dot of 1 $mm^2$ area was thermally evaporated.

Inside the microscope, contact was made to the devices by means of an aluminium stub, on which the sample sat and to which the indium made contact, and a phosphor bronze probe touching the gold dot. Electrical connections were made through opposite sides of the vacuum chamber, and externally screened coaxial cables were used with a single common earth point to reduce noise.

## 5.5 Experimental Results

All measurements were carried out with a beam energy of 15 keV unless otherwise stated. The pictures were taken using a 1000 line, 20 sec. scan frame and the line traces had a scan speed of 18.2 msecs.

### 5.5.1 Cleaved Diodes

The main feature of the diodes made on freshly cleaved samples was the dependence of the EBIC signal contrast on the energy of the incident electron beam and on the bias applied to the sample. The gold contact appeared virtually transparent for incident electron energies of 15 keV and above. This caused electron-hole pair generation and separation to occur over the whole area of the gold dot, with the consequent white contrast in the EBIC mode shown in Figure 5.6. At lower values of accelerating voltage, e.g. 7.5 kV, however, current flow caused by the electron beam only occurred around the perimeter of the gold film where the gold was thinner and this gave the contrast observed in Figure 5.7. As an increasing reverse bias was applied to a sample, while a beam of 15 kV was maintained, the EBIC signal across the gold dot which was relatively flat at 0 V bias, became more and more steeply curved as shown in Figure 5.8, which shows two line scans across the contact at zero and 3 volts reverse bias. The signal at the edge increased to several times its initial value while that at the centre remained substantially unaltered. This resembles the shape of signal from an unbiased device at 7.5 kV (shown in Figure 5.7). The effect of forward bias on these devices with beam voltages of 15 kV was to reduce the amplitude of the EBIC signal, corresponding to a reduction in current flow, but the overall flat response seen at zero bias in Figure 5.8 remained unaltered. These observations will be discussed later.

### 5.5.2 Etched Diodes

The Schottky diodes made on surfaces which had been etched in hydrochloric acid, behaved in all respects similarly to those described above. The only minor difference was that the EBIC contrast was viewed against a background of etch hillocks instead of the smooth cleaved surface containing a few cleavage steps.

### 5.5.3 Polished Surface Diodes

In addition to showing the type of contrast described above, Schottky diodes made on polished surfaces exhibited small dots ( 1-10 μm diameter) of different contrast when viewed in the EBIC mode. With a forward bias of a few hundred millivolts applied to the sample, these appeared as dark spots (see Figure 5.9), while a reverse bias of similar magnitude produced a signal with white spots (Figure 5.10). These features will hereinafter be referred to as 'pinholes'; inverted commas are used because physically there is no difference at all in the surface of a pinhole. The secondary emission micrograph of the surface, Figure 5.11, shows this very clearly. At zero bias, in EBIC, the 'pinholes' virtually disappear, and with a higher current amplifier gain, dark lines may be seen (Figure 5.12) which are due to the presence of scratches on the mechanically polished surface. The additional small contrast feature present at A can be attributed to a small dust particle on the surface of the diode. The cathodoluminescent mode image of this surface, Figure 5.13, also demonstrated the presence of scratches on the sample surface, which act as non-radiative recombination centres, but showed no evidence whatsoever for the existence of the so-called 'pinholes'.

The other feature of the EBIC contrast observed at these 'pinholes' was its dependence on the electron beam energy. 'Pinholes' were observed with beam energies of 7.5 keV, 15 keV and 25 keV, although the magnitude

of the current signal at a given bias varied greatly between 7.5 keV (the smallest and 25 keV the largest) as might be supposed. Figure 5.14 records line scans taken of the same 'pinhole' at the three accelerating potentials, with the signal gain adjusted in each case to give comparable levels. In spite of this, the 25 kV trace is seen to be broader than the 15 kV which is broader than that at 7.5 kV.

### 5.5.4 MIS Structures

The region of light contrast visible around the edge of the gold dot in the Schottky diodes already described was very much reduced when MIS devices were examined in the EBIC mode. This is almost certainly attributed to the presence of the thick layer of insulator on these samples. However, within the region defined by the gold dot, these devices often exhibited features like that shown in Figure 5.15. It is presumed that these had formed as a result of the substrate being masked by a surface particle during the evaporation of the SiO but not during the gold evaporation, and in this way a real pinhole was formed in the insulator. Figure 5.16 and 5.17 show the pinhole in Figure 5.15, imaged in the EBIC mode with forward and reverse biases of 3 volts respectively. The dependence of contrast on bias clearly resembles that observed from the features described as 'pinholes' in the previous section.

Another type of feature where this kind of contrast could be observed was at etch pits. Often the surface would contain several etch pits much deeper than the others, (probably as a result of insufficient polishing) and at one edge of these, EBIC contrast could normally be observed. Presumably because of the angle of incidence of the insulator vapour on these holes, the faces did not become coated evenly, hence effectively forming a pinhole region.

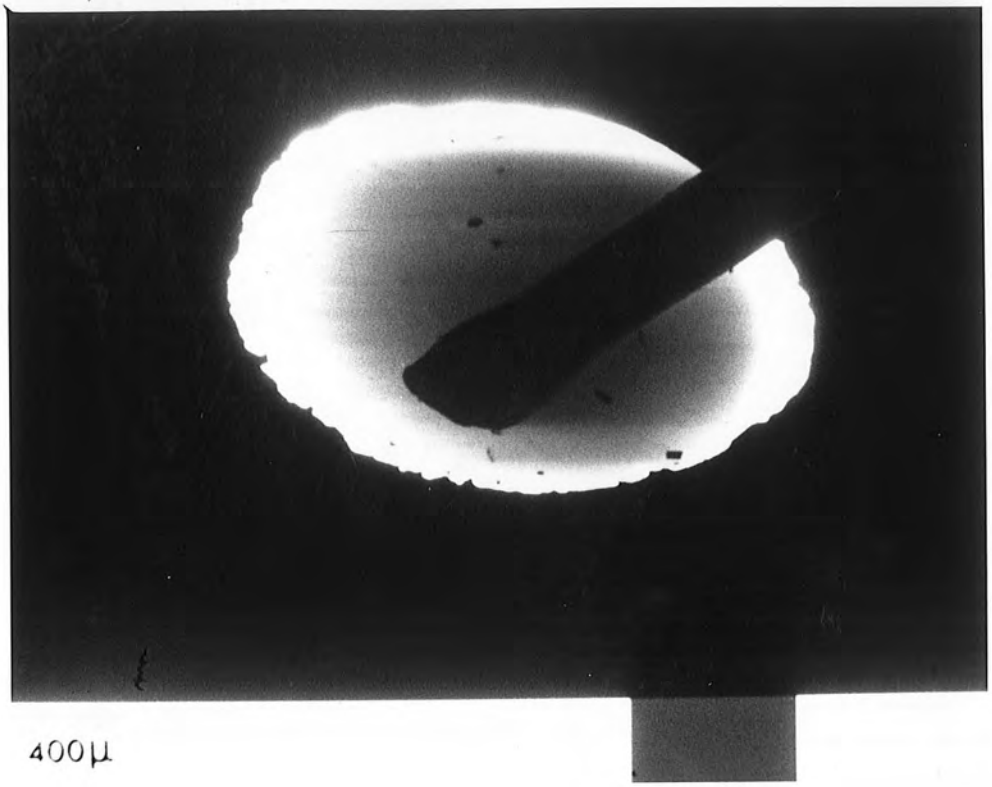
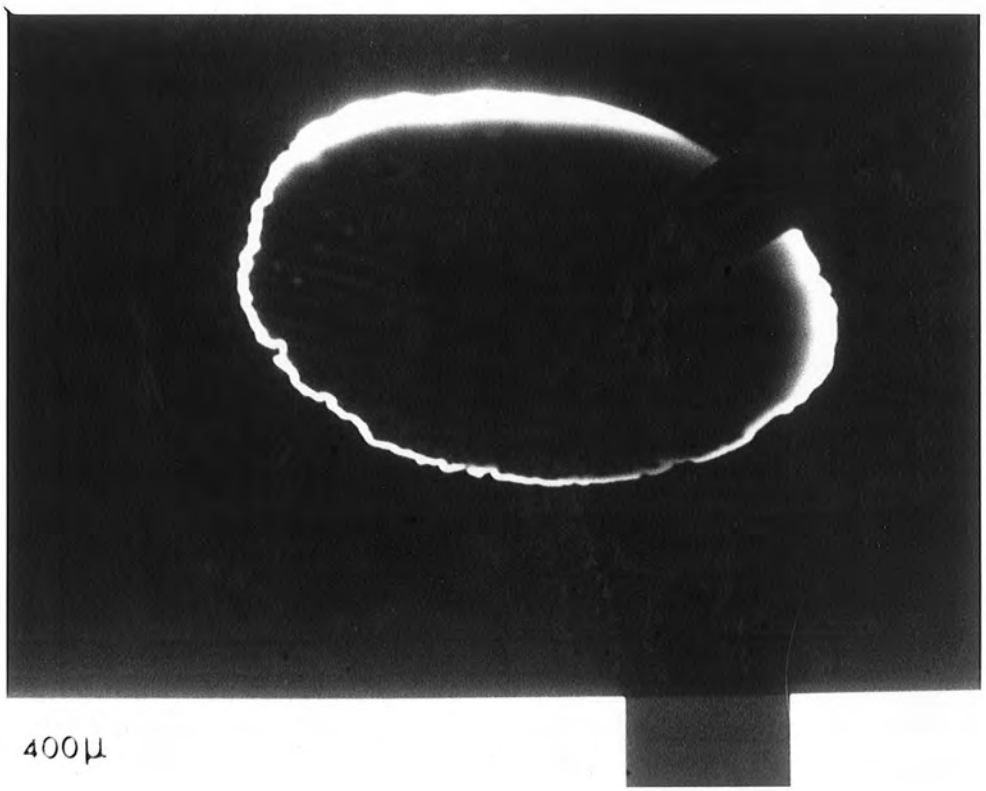



Figure 5.6 : E.B.I.C. signal through the gold Schottky contact on a cleaved CdS surface : 15 kV accelerating potential.



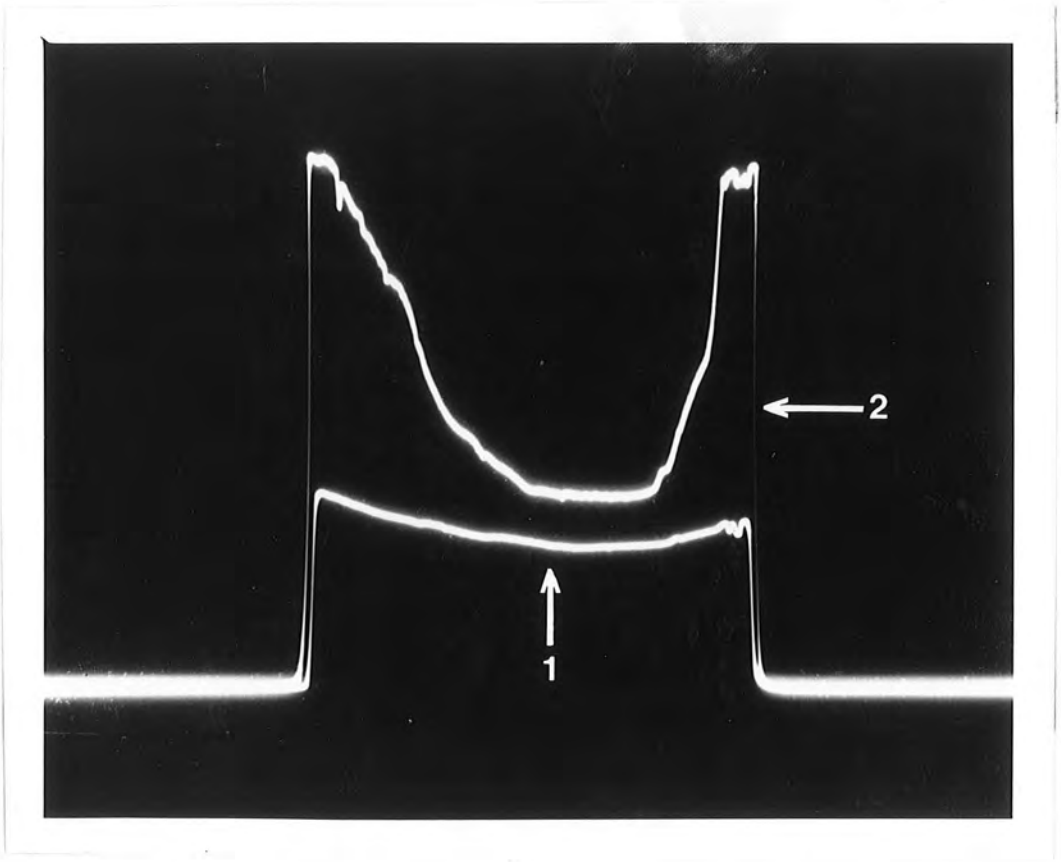



Figure 5.8 : Two E.B.I.C. line scans (15 kV) across the gold dot

(1) zero bias applied to device

(2) 3 volts reverse bias.

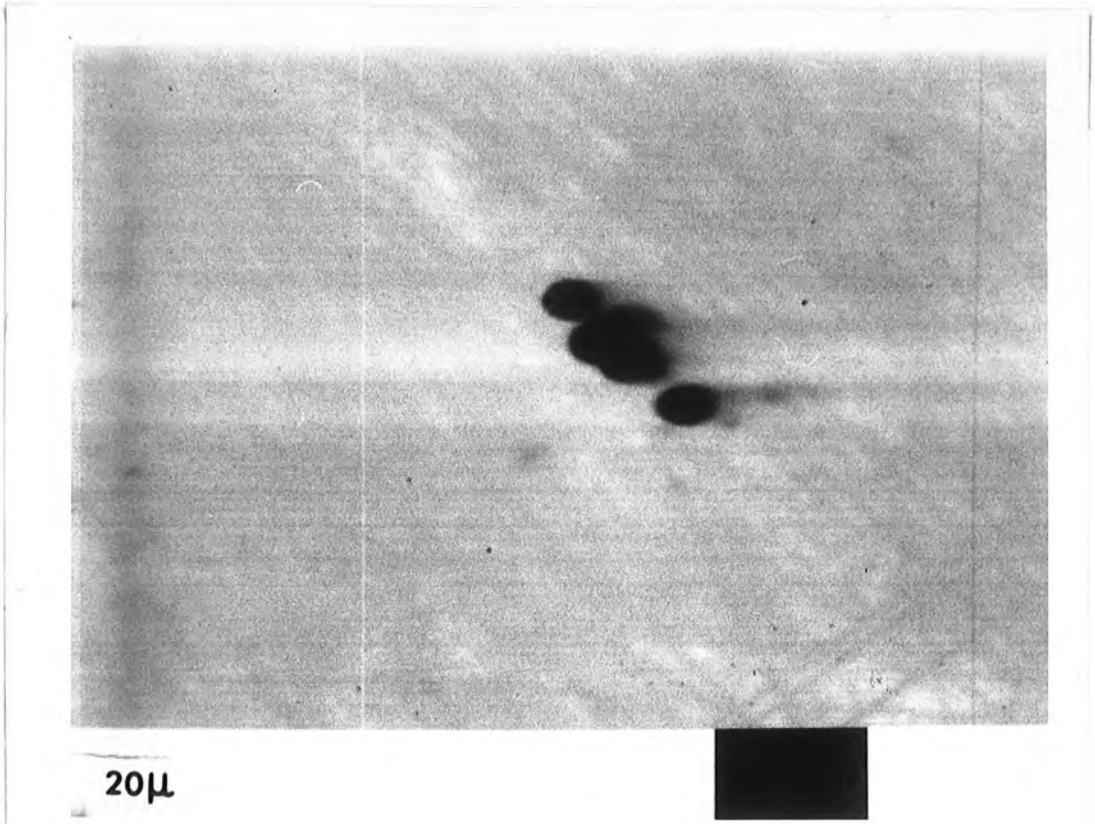
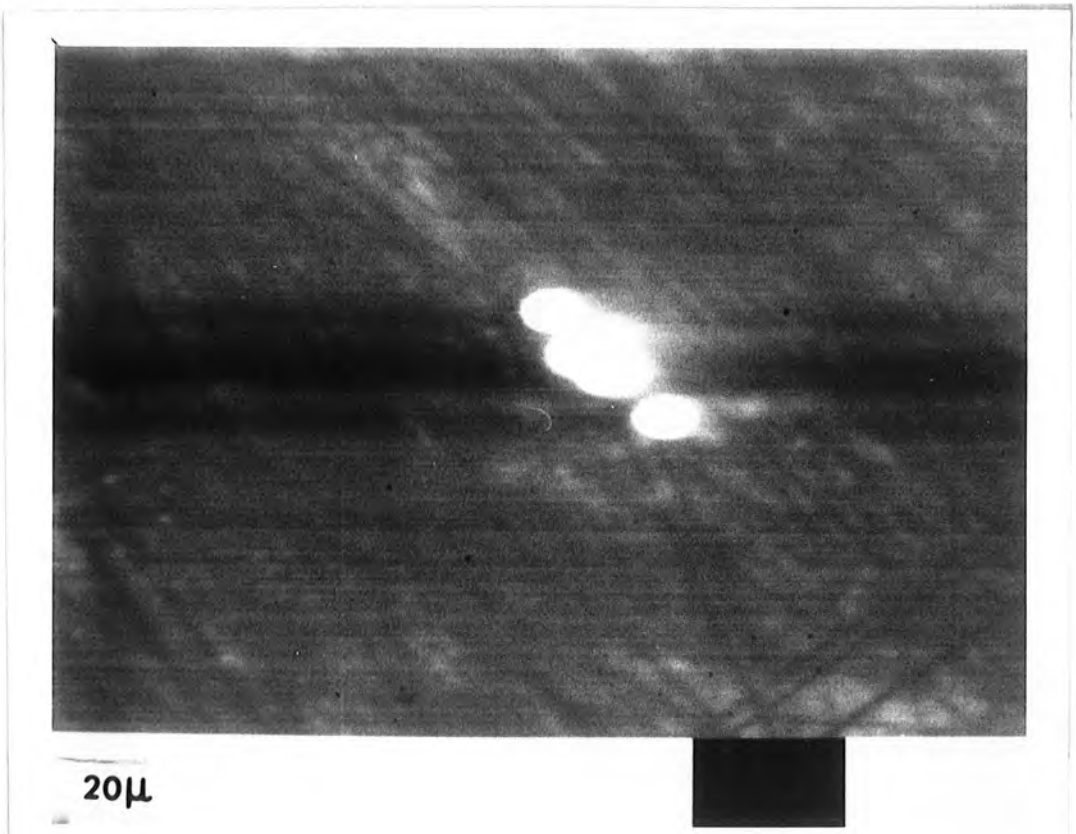



Figure 5.9 : Polished surface diode E.B.I.C. signal (forward bias)



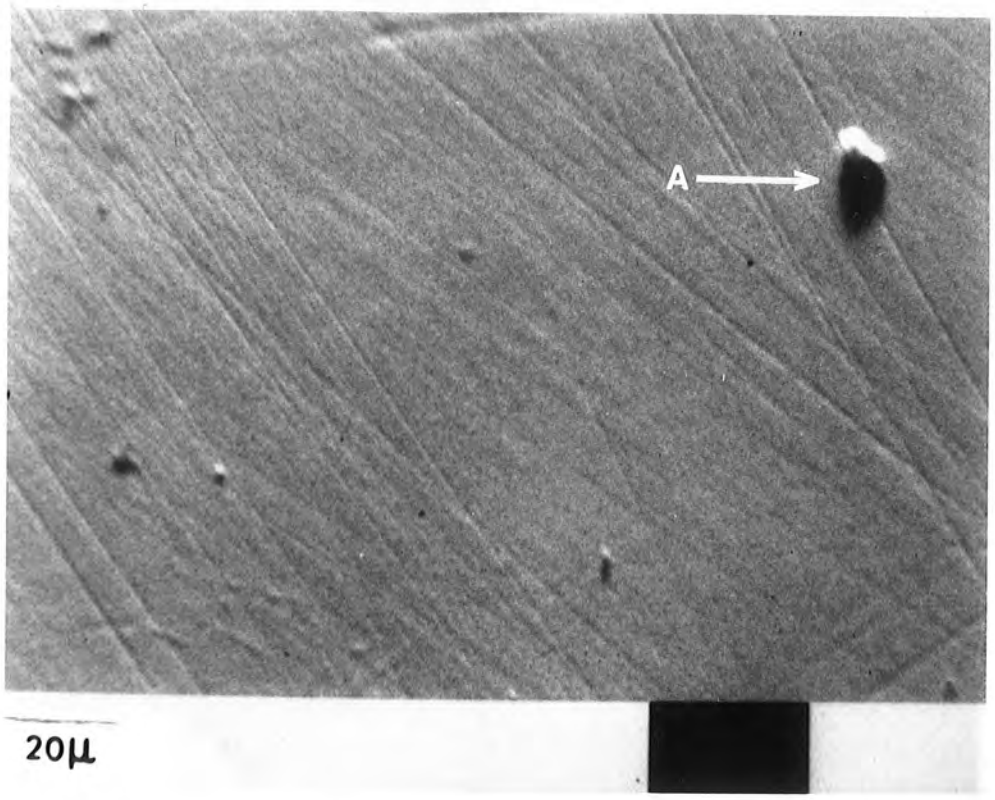



Figure 5.11 : S.E. image corresponding to Figs. 5.9 and 5.10

(Dust particle marked by A)

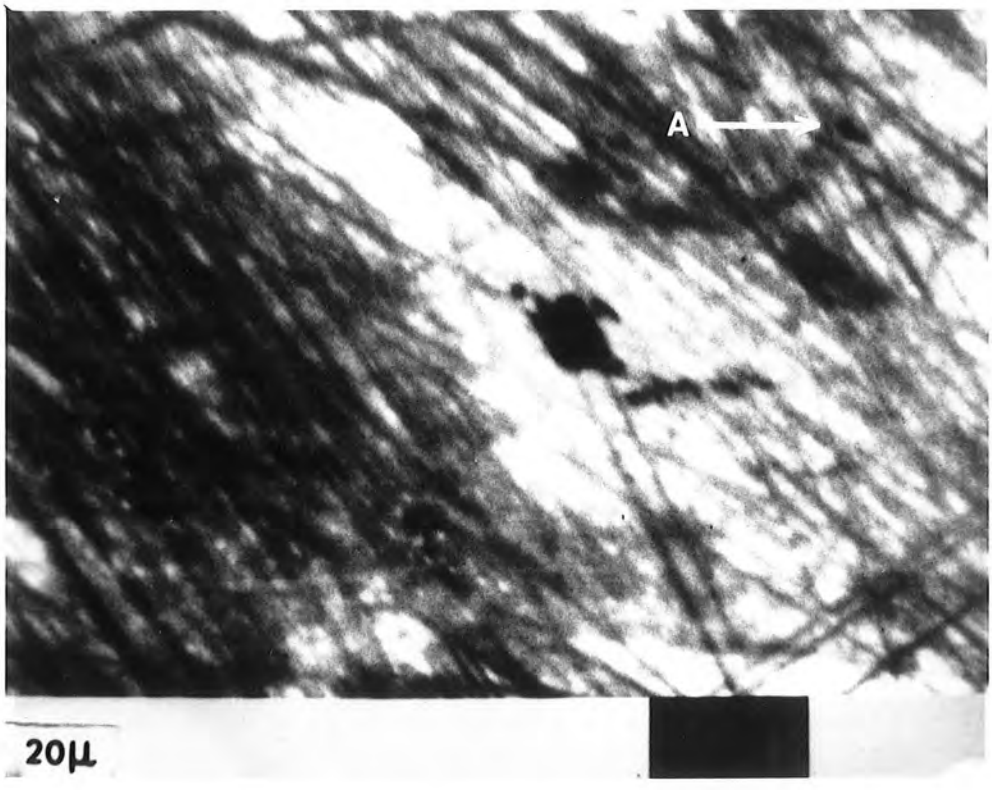



Figure 5.12 : E.B.I.C. image (of above) at zero bias

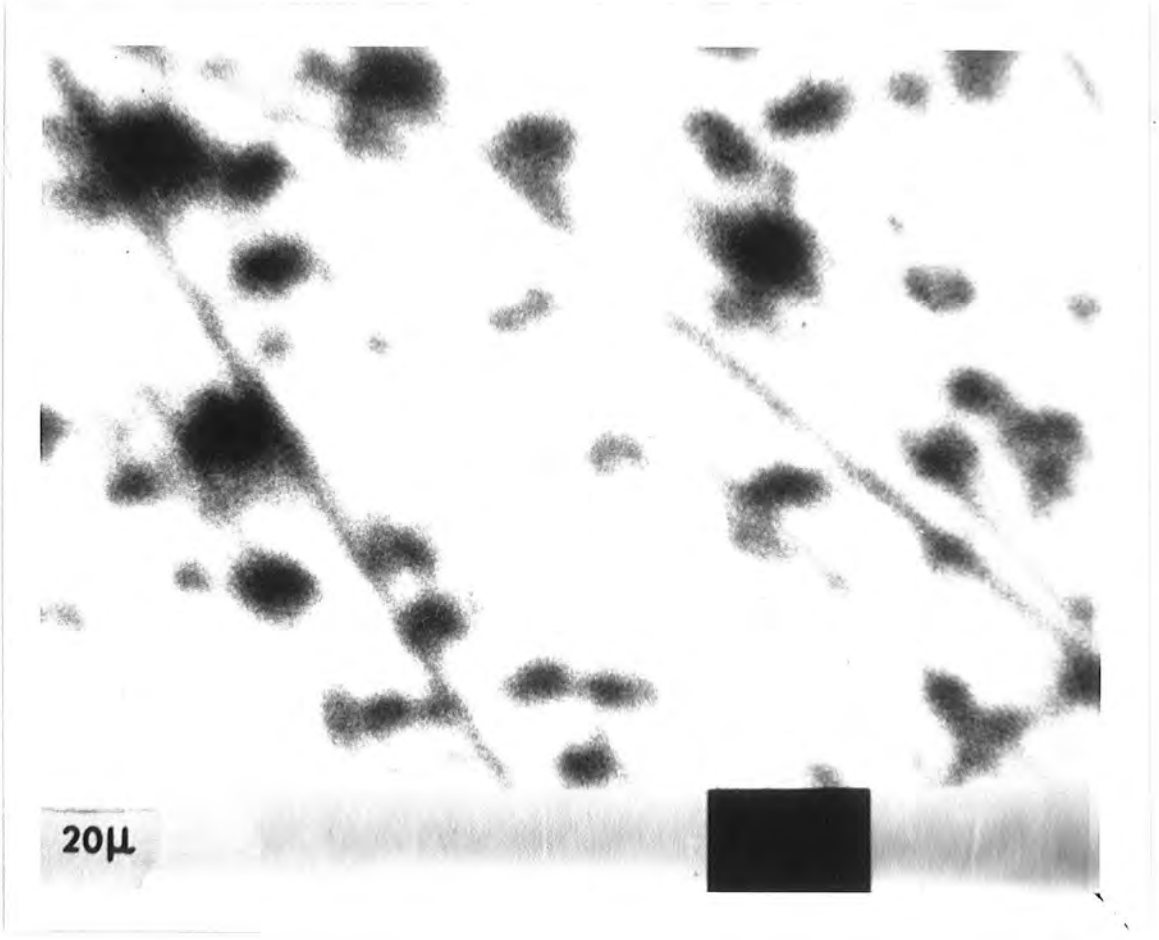



Figure 5.13 : Cathodoluminescence of Fig. 5.11 showing the effect of scratches.

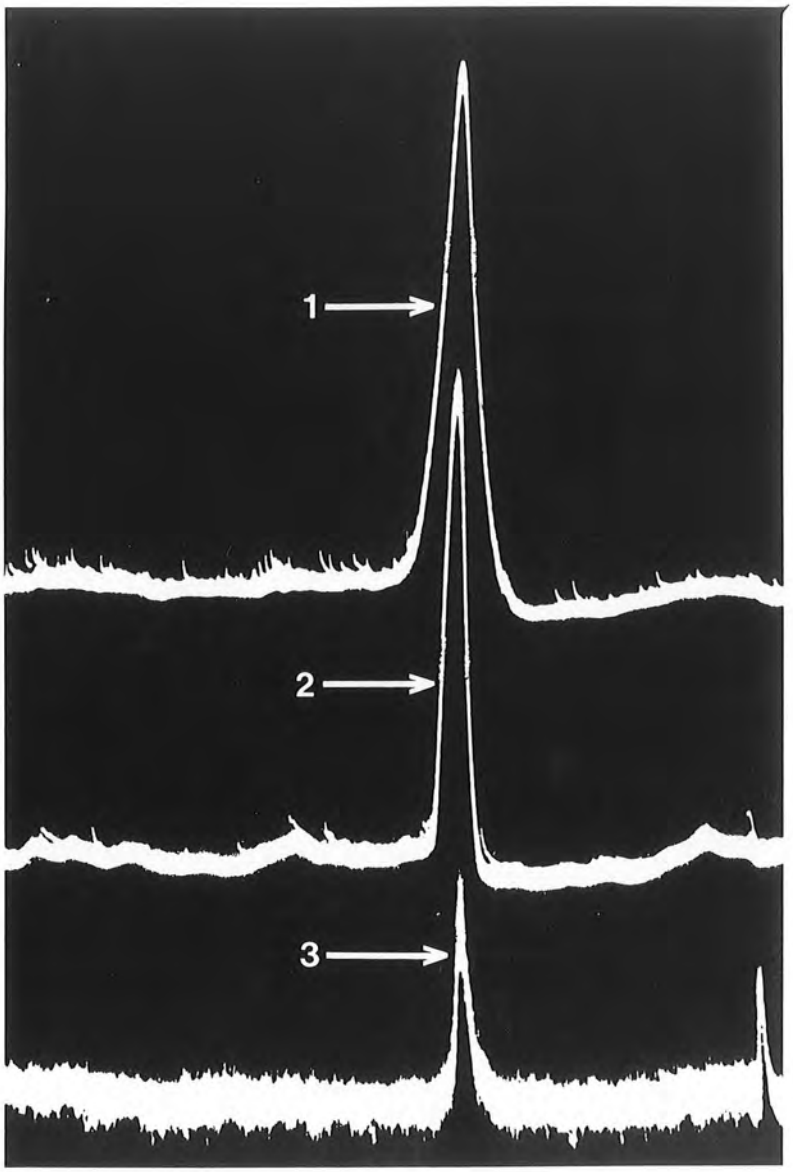



Figure 5.14 : Line scans of E.B.I.C. signal at a pinhole using three accelerating potentials (1) 25 kV, (2) 15 kV, (3) 7.5 kV

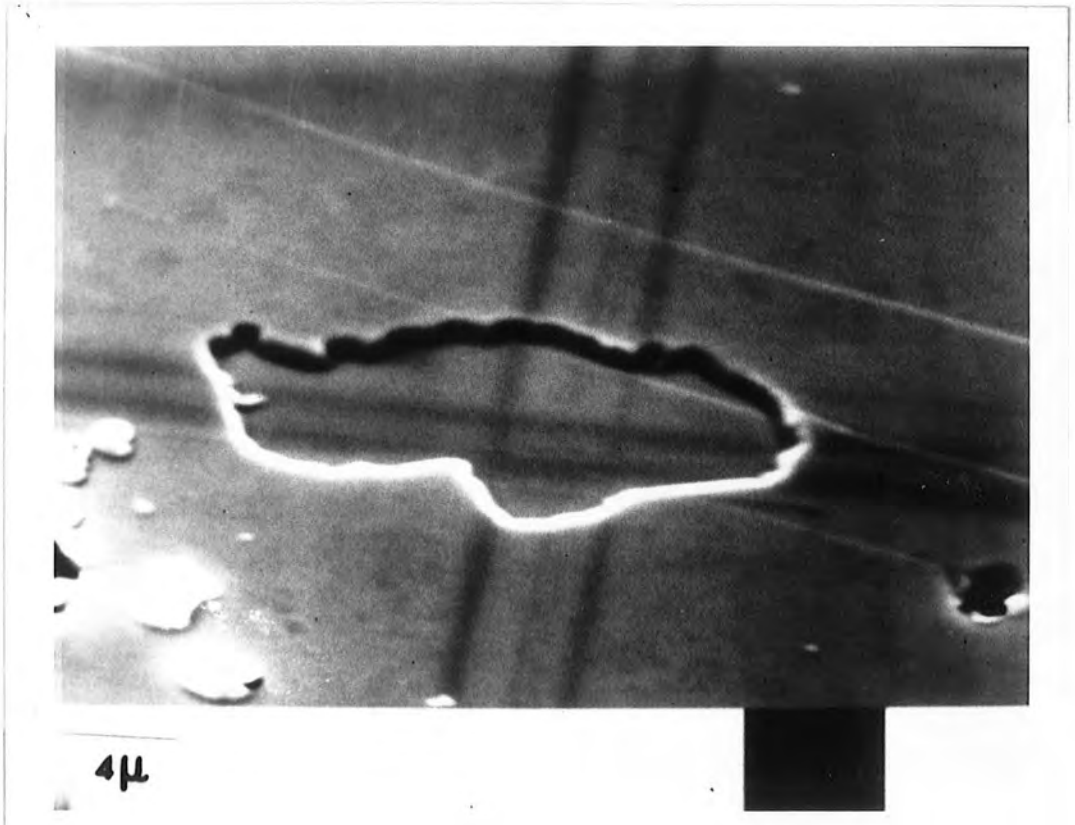



Figure 5.15 : Secondary emission micrograph of pinhole in SiO layer.

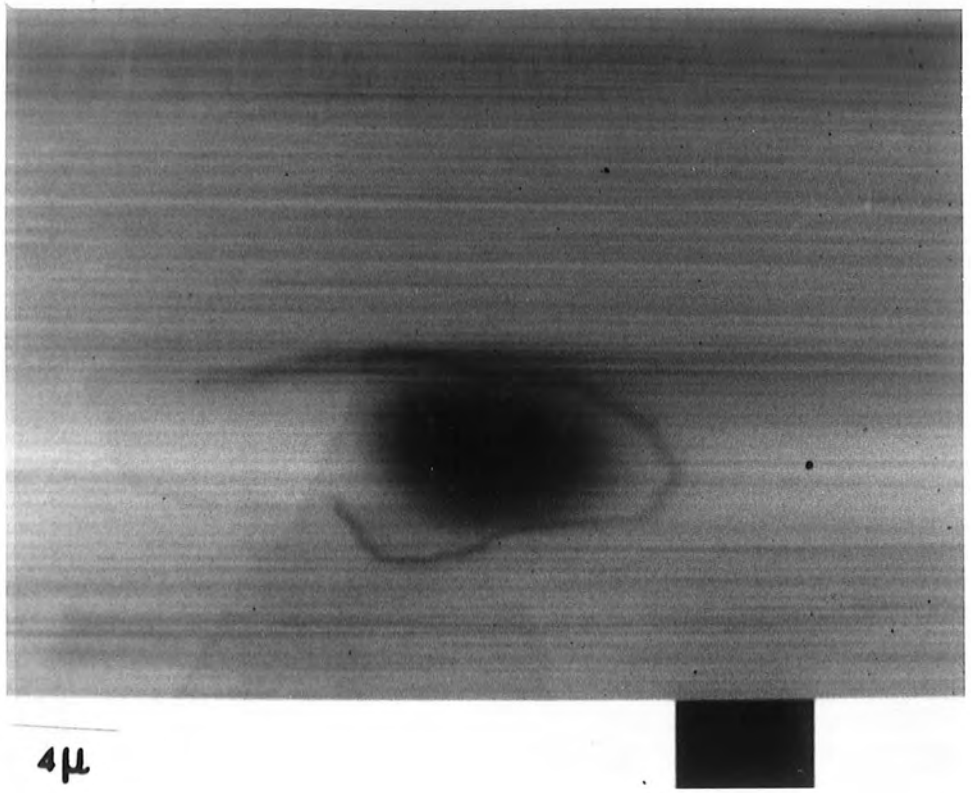
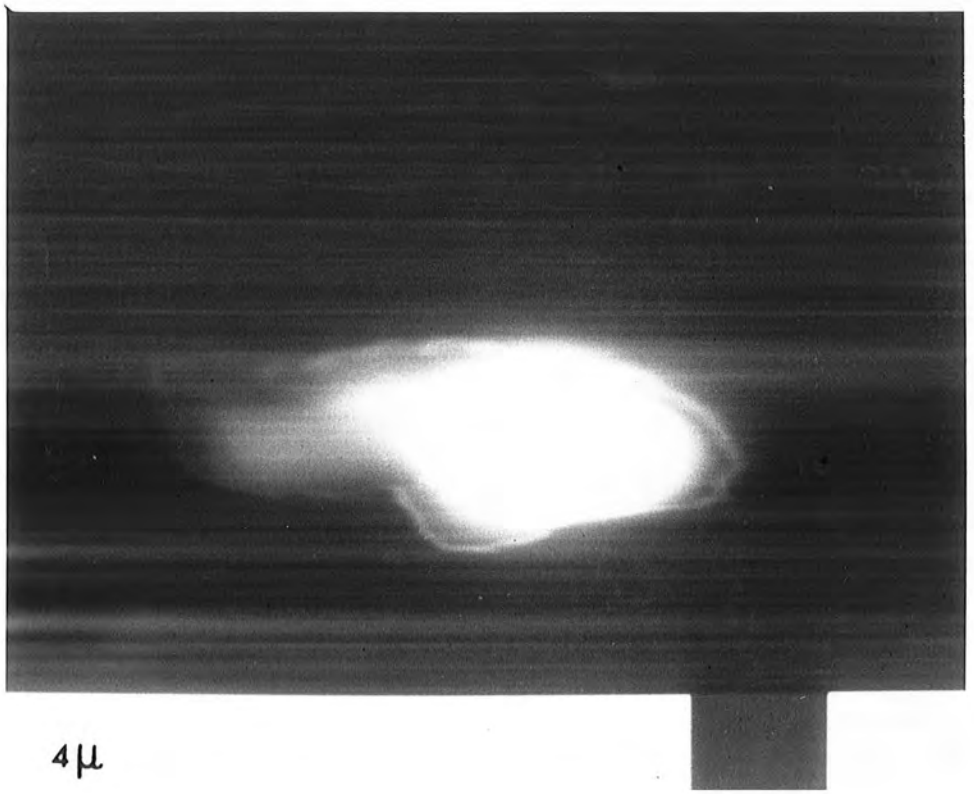



Figure 5.16 : E.B.I.C. micrograph of Fig. 5.15 in forward bias.



## 5.6 Discussion

Although the observations of cleaved and etched diodes described were made on moderately high resistivity $10^3 - 10^5$ Ωcm cadmium sulphide in order to obtain noise-free signals, it has been possible to confirm that the results were fundamentally of the same form as those for lower resistivity ( $\rho \sim 1$ Ωcm) CdS which was used for the polished and MIS diodes. This was necessary in order to discount the possibility of the observations being wholly or in part due to photoconductive effects induced in the bulk of the CdS by the electron beam. The current through the Schottky diode in forward bias was, indeed, found to be strongly dependent on the presence of the electron beam, reducing by a factor greater than 10 when the beam was extinguished. However, as the lifetime associated with this enhancement effect was measured to be $\sim 1$ second, the contrast observed in Figure 5.8, 5.9 and 5.10, which were imaged using line scan times of 20 m secs. cannot be attributed to photoconductivity. The photoconductive effect should therefore be regarded as merely reducing the bulk resistance of the devices by a certain factor, independent of scan position.

The alteration of contrast with different beam energy shown in Figures 5.6 and 5.7, may be explained by the penetration of the electron beam as a function of accelerating potential. Bresse (1972) has shown that when an electron beam enters a solid, its energy is dissipated by a random series of collisions within a volume which is roughly spherical with the circumference tangential to the surface. The radius of this volume depends on the electron beam energy, atomic weight of the material, density etc. Gold for example absorbs the energy of a 15 kV beam within a depth of 0.53 μm (Kanaya and Okayama 1972). When the beam scans across the gold dot on the sample, a larger proportion of its energy will be dissipated in the CdS at the edges of the dot (where the gold is thinner)

than at the centre. This energy is absorbed producing electron-hole pairs in the depletion region of the CdS. Before they can recombine many of these pairs will be separated by the internal electric field (the barrier electron voltaic effect) causing a current to flow. This is the case in Figure 5.6. At a lower accelerating potential (7.5 kV), very little of the beam penetrates the centre of the gold dot, consequently only the edge displays an EBIC signal (Figure 5.7). A similar effect occurring in planar p-n junctions has been described by Chi and Gatos (1977). To explain the effect of bias shown in Figure 5.8, the model illustrated in Figure 5.18 is proposed.

Electron hole pairs produced within the depletion region contribute to the external current. Because of the short minority carrier diffusion length in CdS, at zero bias, a current will be produced at the edge, where much of the beam is absorbed further into the CdS beyond the depletion region, which is comparable to that produced at the centre where a large proportion of beam energy is lost in the gold.

The current signal from the centre of the gold will therefore be largely unaffected by an increase in reverse bias, whereas at the edge more absorption will take place within the broadened depletion region to produce a larger current flow as the reverse bias is increased. The reduced response under forward bias with uniform contrast across the dot as for zero bias, follows immediately from the model. A narrower depletion region and lower field imply less induced current. A good demonstration of this is given by de Kock et al (1977) who show that striations in EBIC contrast across a silicon Schottky diode are due to resistivity fluctuations causing variation in depletion width.

As previously stated, the etched Schottky diodes showed very similar results, and it seems reasonable to use the same interpretation to describe them. It must be emphasised that both types of device showed

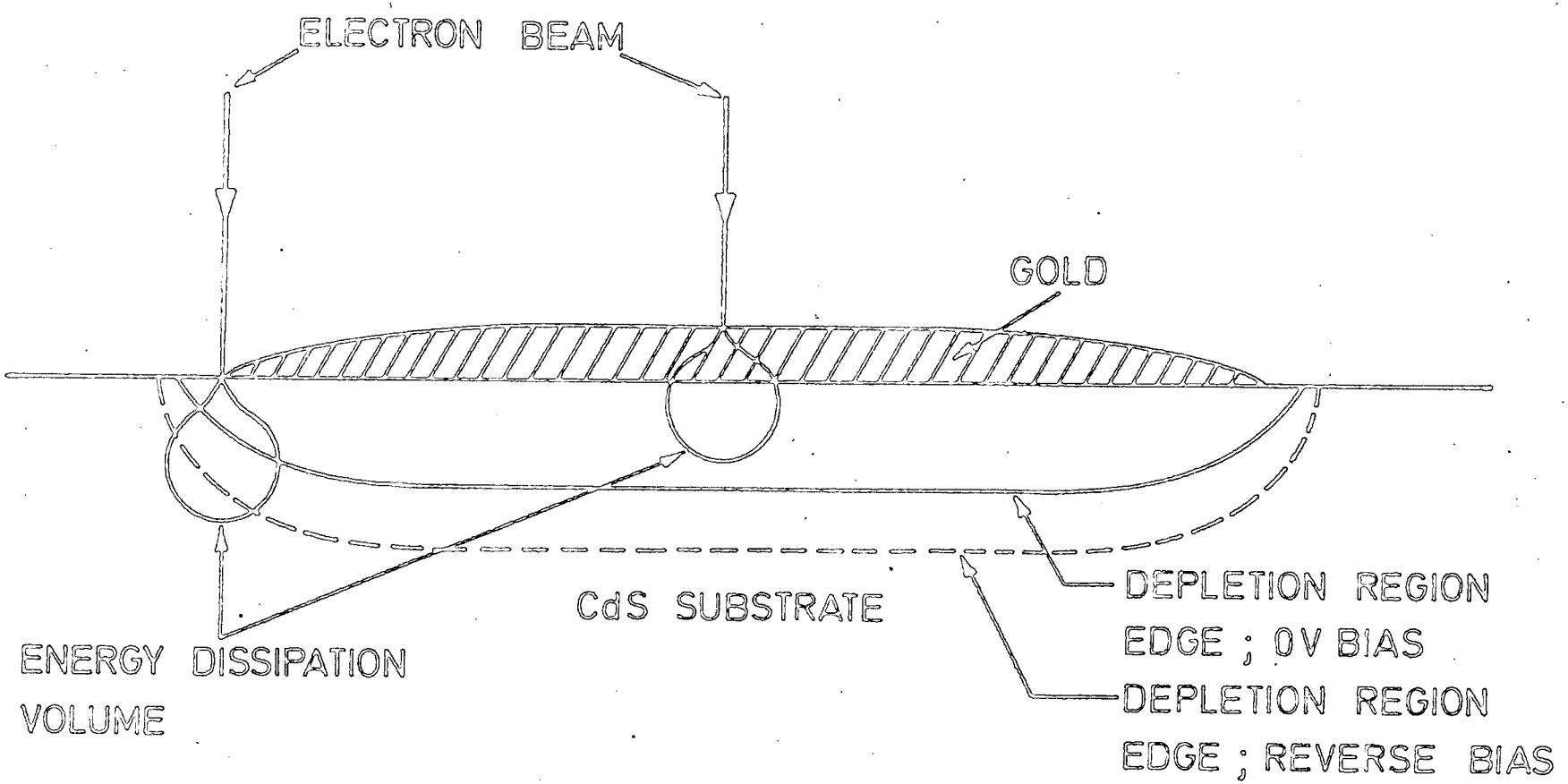



Figure 5.18 Model to explain penetration effect

only white contrast on the region defined by the gold dot when the bias was varied. As the forward bias was increased, the level of contrast reduced but did not change sign.

The characteristics of Schottky diodes prepared on polished unetched CdS cannot be explained by the above model, although the penetration effect with differing beam energies was observed. The small dots or 'pinholes' which changed contrast with reversal of bias were obviously associated with a quite different effect. Similar observations have been reported by Peach et al (1979) and Galstyan et al (1972).

It is proposed that the work damaged surface forms a resistive layer containing recombination centres between the gold and CdS bulk. Therefore the current which is induced to flow by the electron barrier voltaic effect will be reduced by increased recombination within this surface region. In contrast, the current flowing through a biased device when the beam illuminated one of these 'pinholes' was observed to be several times greater than when the beam was elsewhere. Quantitative measurements of current versus voltage were therefore undertaken and are shown in Figure 5.19. In order to carry these out, the electron beam was used in the spot mode, i.e. the scan was switched off, and the beam positioned manually. Three sets of measurements were taken:

(1) Electron beam off (dark condition)

(2) Electron beam away from 'pinhole'

(3) Electron beam at centre of 'pinhole'.

The measurements were made using a high impedance $\sim 10^9$ Ω D.V.M. Bradley Voltmeter 173B, to measure the potential across the sample, and the low impedance Keithley current amplifier previously described to measure the current. The voltage was provided by two 9 volt dry cells in a potential divider network. To begin with the current and voltage were set to zero with the electron beam off, then the electron gun e.h.t.

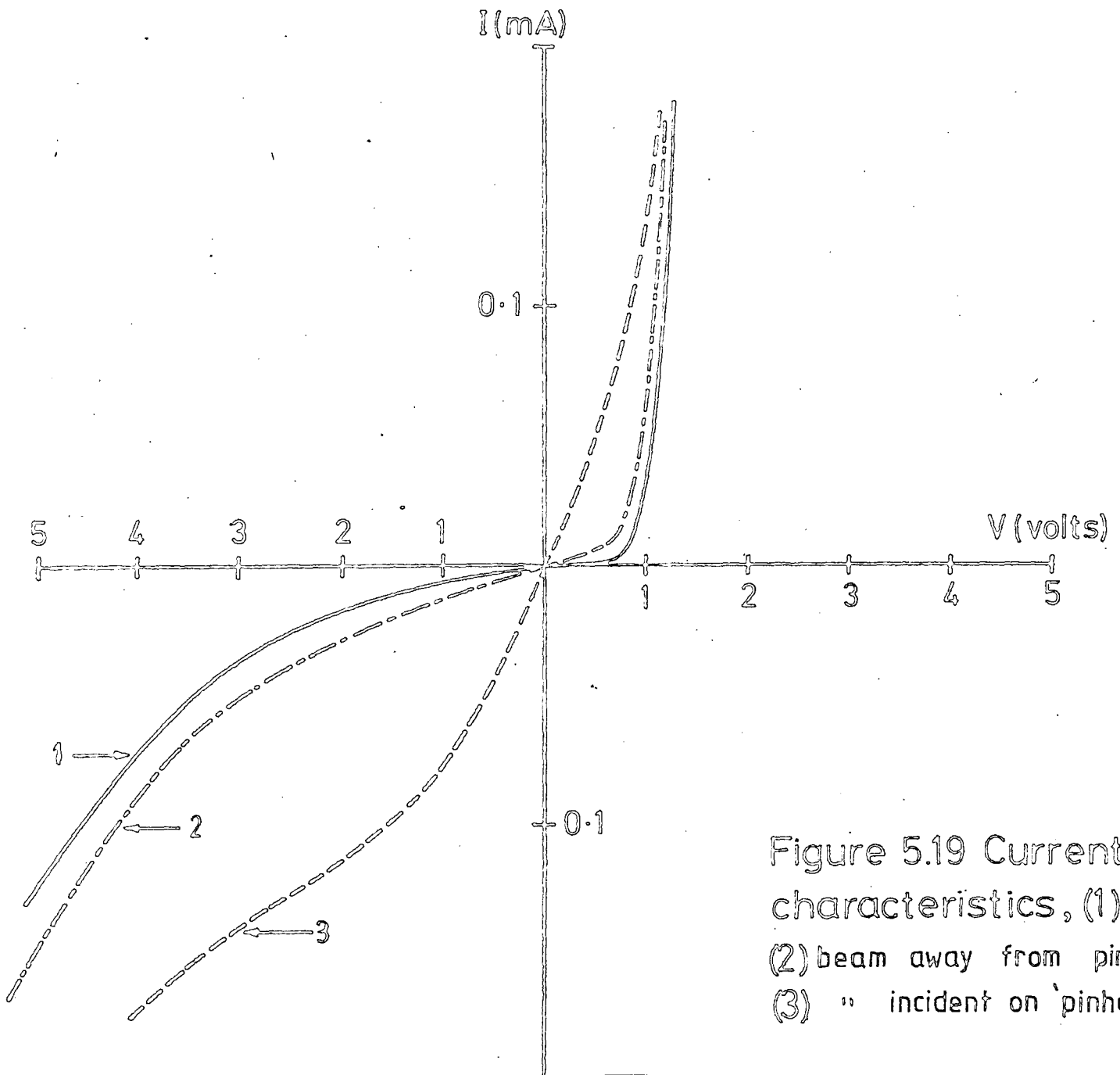



Figure 5.19 Current-Voltage characteristics, (1) Electron beam off
(2) beam away from pinhole
(3) " incident on 'pinhole'

was switched on. This caused a small voltage ∿ 3 mV to appear on the voltmeter at zero current. This voltage was found to be larger for experiment (3), but still less than 10 mV, and it was therefore concluded that no significant open circuit voltage or short circuit current was produced by the electron beam. This is in contrast to the work of Rappaport (1954) on silicon p-n junctions where O.C.V's. of 200 mV were found. This is not surprising in view of the surface treatment.

The reverse bias was then increased and the voltage and current recorded. When the current approached 1 mA or the voltage 5 V, the voltage was reduced slowly and readings again taken to check for hysteresis. The current in forward bias was then measured similarly. A significant hysteresis was observed with all devices; however, in relation to the difference between curves (1) and (3), Figure 5.19, this was negligible. A dark characteristic was measured first, then the light ones, and finally as a control experiment, another dark one. While the current in this case was higher in both forward and reverse biases than originally, as it was still considerably below the 'pinhole' current, the results in Figure 5.19 are still valid.

It is apparent that there is a minimal effect on the current-voltage characteristics when regions other than 'pinholes' are bombarded. This must be due to a high recombination probability for electron-hole pairs in the work-damaged layer, so that few carriers reach the depletion region. In contrast, the current in both forward and reverse bias is considerably higher when the electron beam impinges on a 'pinhole' and from the shape of the I-V characteristics it appears that the effect of the electron beam is to lower the electron barrier height, or equivalently increase the semiconductor temperature in the vicinity of the barrier region. The former process would occur if the polished (work damaged) layer affects the potential energy band structure in such a way as to increase the barrier

height for devices kept in the dark, compared with that of a pure Schottky diode. To explain the experimental observations the barrier height would be required to decrease when the 'pinhole' is bombarded. This might occur as a result of a change in occupancy of traps in the interfacial region under irradiation by the electron beam; or if the barrier height is controlled by the resistivity of the surface layer, then by analogy with the photoconductive effect, the impinging electrons would reduce the barrier.

Bottoms et al (1975) have used the EBIC technique to demonstrate the barrier lowering produced by mobile positive ions which had been caused to drift to the semiconductor insulator interface by the application of a bias and heat treatment. The result was a light contrast due to the increased beam induced current. When the same treatment was used but with the opposite bias, the spots disappeared, showing that the ions had drifted away from the interface. The presence of positive ions at the semiconductor work damaged layer, therefore, might produce one type of contrast in forward bias, but it is unlikely that they would cause the opposite contrast with reversal of bias.

The suggestion of a change in temperature would require local heating of the crystal and in view of the fact that the irradiation is with 15 keV electrons, this is not impossible. It is perhaps more likely that the beam will cause work damage or 'burning' on the surface regions especially when used in the spot mode. This would explain the hysteresis (reversible 'heating') and the drift of characteristic after measurements had been taken.

A third possibility is that the diode ideality factor (n-factor) is altered by the electron beam. Yu and Snow (1968) have suggested that n may be a function of recombination current within the depletion region. This will clearly be altered by the impinging electron beam.

That there should be no obvious physical surface features to distinguish these 'pinholes' is rather surprising since their electrical characteristics have been shown to be very different from the surrounding area. It must be emphasised that these 'pinhole' defects were not like the stacking faults or impurity centres observed by Czaja (1965) and Kawado (1975) amongst others. These latter defects behaved as recombination centres showing only dark contrast.

The other contrast features, in Figures 5.9, 5.10 and 5.12, are due to surface scratches and are similar to those described by Holt and Chase (1968). They were also observed to change contrast with reversal of bias, but with a non-zero threshold. Their contrast was the negative of that of the 'pinholes', and they are consequently regarded as centres of enhanced recombination. The cause of the different threshold may be the different contact geometry at the scratch.

In Figure 5.14, the change in peak width with beam energy may be attributed to the different cross-section of penetration of the electron beam at different energies, it might also, however, be associated with the physical dimensions of the pinhole through the surface layer, but this is only speculation.

The current-voltage characteristics of the MIS diodes were measured in the same way as for the previous type of device, and are shown in Figure 5.20. The features of these characteristics closely resemble those in Figure 5.19, with the thick oxide region exhibiting little change in current with or without the impinging electron beam, while the pinhole current is significantly higher both under forward and reverse bias. The simplest explanation of the behaviour in the thick insulator, is that most of the beam is absorbed in the gold and the SiO and little,in fact, reaches the CdS. Actually at the pinhole, there is likely to be a much thinner surface layer beneath the gold contact and when the electron beam strikes

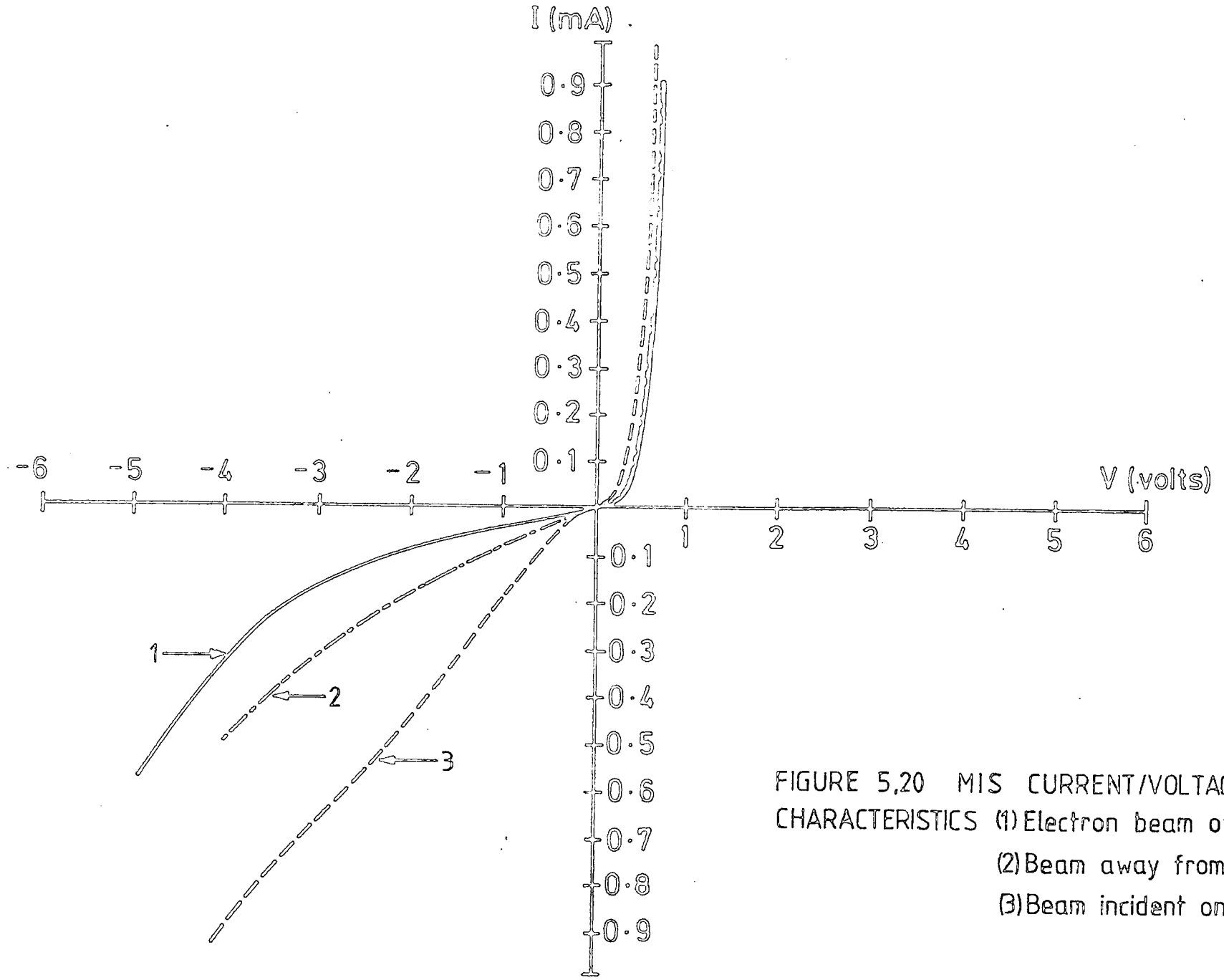



FIGURE 5.20 MIS CURRENT/VOLTAGE CHARACTERISTICS (1) Electron beam off
(2) Beam away from pinhole
(3) Beam incident on pinhole

this, it is suggested that the barrier height is lowered, as it was for the polished Schottky diode, causing a higher current to flow in both forward and reverse directions.

While electrical measurements on both the polished and MIS diodes revealed similar mechanisms, physically the two cases are very different. The former contained no physical pinhole whereas the latter certainly possessed a real pinhole, as the secondary emission micrograph in Figure 5.15 shows. The suggested explanation satisfies both cases without much modification, but in order to test it further, another device was fabricated.

The sulphur face of a die of CdS, already possessing an indium contact opposite, was polished with 3 μm Aloxite powder, followed by 1 μm diamond paste. After a short etch, 10 seconds in conc. HCl, it was placed over a mask in the evaporation system and evacuation took place. The mask prevented half the surface from receiving the evaporated layer, which was SiO, and of $\sim$ 1000 Å thickness. After this, a gold dot was evaporated, partly over the insulator and partly direct on to the CdS. When this was examined in the EBIC mode, the section free of insulator was seen to resemble that of the cleaved or etched devices described earlier with no negation of contrast with reversal of bias. Adjacent to this was a region, still outside the apparent edge of the insulator (as seen in secondary emission) which did change contrast with bias. Attempts to measure I-V characteristics with the beam stationary here were unsuccessful, the drift in current between starting the measurements and finishing altered the characteristics by a factor greater than 4. The beam spot seemed to 'burn' the region, leaving a mark, which could be seen when the region was scanned afterwards. This effect of radiation damage has been observed by several authors, for example Peckerar (1973). This region is thought to be coated with a thin surface layer, consequently producing

similar results to the pinholes. Within the edge of the insulator, the current-voltage characteristics were very similar to those with the beam switched off, consistent with the previous results on MIS diodes.

## 5.7 Conclusions

The observations discussed above, on the four types of surface, can all be attributed to two basic effects, the barrier electron voltaic effect, and the β-conductivity effect described earlier. Both the cleaved and etched devices showed behaviour consistent with the barrier electron voltaic effect, while the samples possessing a resistive surface layer appeared to show that the presence of β- conductivity dominated.

The device described finally, with an insulator under part of the gold only, shows both these effects at different parts of its surface. From an empirical point of view, specimens where β-conductivity is important show reversal of contrast with bias, whereas those where the barrier e.v.e. dominates show merely a change in magnitude of contrast with reversal of bias.

Returning to the work of the previous chapter, the high conductance found in MIS devices in forward bias, with voltages in excess of 500 mV may be explained by conduction through the pinholes. There were only a few pinholes on the devices examined, so it is supposed that at low forward bias and reverse biases up to, say, 6 V, the resistance of a pinhole, since the device is a Schottky diode, is high. Under these conditions the 'pinholes' do not affect the total resistance of the device. Similarly, as they are of small area, their contribution to the capacitance will be small. However, as the bias is increased in the forward direction, the differential conductance of the pinholes will increase dramatically. Current flow through 'pinholes' will dominate the total

conductance which will increase exponentially. With reverse biases exceeding 6 V, breakdown will start to occur at the pinholes, again their differential resistance will fall dramatically, resulting in the sudden dramatic increase in conduction found experimentally.

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# CHAPTER 6

# $Cu_2S$ ON CdS

## 6.1 Introduction

One of the most important areas of study of the copper sulphide-cadmium sulphide heterojunction has been into the way that copper sulphide forms on single crystal cadmium sulphide. This is because, as mentioned in Chapter 1, several phases of copper sulphide exist, but only one, chalcocite, $Cu_2S$, produces a heterojunction with a comparable efficiency to that of the Silicon cell, (Te Velde and Dieleman (1973) and Palz et al (1973)). Extensive investigations of the phases of copper sulphide have been carried out by Djurle (1958), using X-ray diffraction. In this chapter, a description of the methods of formation of various types of copper sulphide layer, and the results of investigation of their properties will be given.

## 6.2 Growth of Copper Sulphide Layer

Copper sulphide can be produced on cadmium sulphide by a chemical displacement reaction between cuprous and cadmium ions according to the equation

$$2\,Cu^{+} + CdS \rightarrow Cu_2S + Cd^{++}$$

As with any displacement reaction, once the first monolayer has been formed on the CdS, the rate of formation of further $Cu_2S$ is determined by the diffusion of $Cu^{+}$ ions through the $Cu_2S$ and the out-diffusion of $Cd^{++}$ ions into solution. Buckley and Woods (1974) have shown that the rate of formation of $Cu_2S$ on CdS obeys a parabolic law.

If the reaction is taken to a conclusion, a cracked, but single, crystal of orthorhombic $Cu_2S$ (chalcocite) is obtained (Cook et al 1970). During the reaction, the sample undergoes a weight increase of 10.1% since $Cu_2S$ has a higher atomic weight than CdS. The cracks are caused by the

lattice constant mismatch between CdS and $Cu_2S$ which sets up strain within the crystal.

The p-type $Cu_2S$ layers were formed on the single crystal CdS by immersion in a copper ion plating bath which was prepared in the following way, following the description of Caswell, Russell and Woods (1975).

(1) 75 ml deionised water was placed in a beaker and oxygen free nitrogen gas bubbled through it.

(2) After several minutes, 12 ml of concentrated hydrochloric acid was added to the water, and heating commenced; the nitrogen gas flow was maintained throughout the experiment.

(3) Approximately 7 ml of hydrazine hydrate solution was added to the solution to produce a pH of 2.5 measured by narrow range pH paper.

(4) 1 g of CuCl was added and the pH checked.

(5) While heating proceeded to 94°C, the pH was measured several times and if necessary corrected to 2.5 by using a few drops of HCl or hydrazine hydrate.

(6) Plating then took place (at 94°C). The crystals were lowered into the bath, for a time dependent on the thickness of layer required, but normally for 10 seconds.

The purpose of the continuous flow of oxygen-free nitrogen, and the use of a strong reducing agent such as hydrazine hydrate in the plating solution was to stop the oxidation of the colourless cuprous, $Cu^{+}$, ions to the blue coloured $Cu^{++}$. Cupric ions would displace the cadmium to form copper deficient phases of copper sulphide. If the solution was left without the nitrogen flowing, a deep blue precipitate would form on the surface after a short time. This was due to cuprammonium type complexions, which redissolved on heating. If, however, the solution was left for several weeks like this, its colour changed from clear to blue-green. When the solution was cooled to room temperature with the nitrogen

flow maintained, white needle-like crystals of cuprous chloride formed from the saturated solution. In order to reduce any possible effects of oxidation which might occur between usage, a fresh solution was made up each time devices were to be prepared.

## 6.3 Sample Preparation

In the preparation of samples for plating, the same procedures were followed as for the MIS devices, except that the size of the crystals was generally 4 x 4 x 2 mm. After the indium contact had been made on the cadmium face, the sulphur face was repolished with 3 μm Aloxite powder and the group of samples to be plated stuck down to a glass slide using 'lacomit', an impervious varnish. All the faces except the sulphur one were coated with this. A short etch in concentrated HCl lasting for 15-20 seconds and a wash in deionised water were administered immediately prior to dipping in the copper solution.

After the copper sulphide layer had been formed, a gold contact 1 $mm^2$ was evaporated, as described previously. This was positioned in one corner of the sample, so that the gold would not interfere in reflection electron diffraction measurements, which were carried out to check the phase of copper sulphide present.

## 6.4 Reflection Electron Diffraction

The technique of reflection electron diffraction (R.E.D.) has been used extensively in the study of copper sulphide layers on single crystal CdS, see, for example, Cook et al (1970), Hadley et al (1977) and Russell and Woods (1978). Its usefulness lies in the ease with which the different phases of copper sulphide may be distinguished by their R.E.D. patterns. Compared with X-ray examination, RED has a number of other advantages: (1) X-rays are absorbed to a depth of hundreds of microns,

whereas the surface layer of $Cu_2S$ on a typical solar cell is only 1 μm thick. An electron beam used, as here, with glancing incidence, will only penetrate some 100 Å into a very smooth surface. (2) The diffraction pattern could be studied as the sample orientation was altered. For a good introduction to the theory and techniques, see 'Electron Diffraction' by T B Rymer.

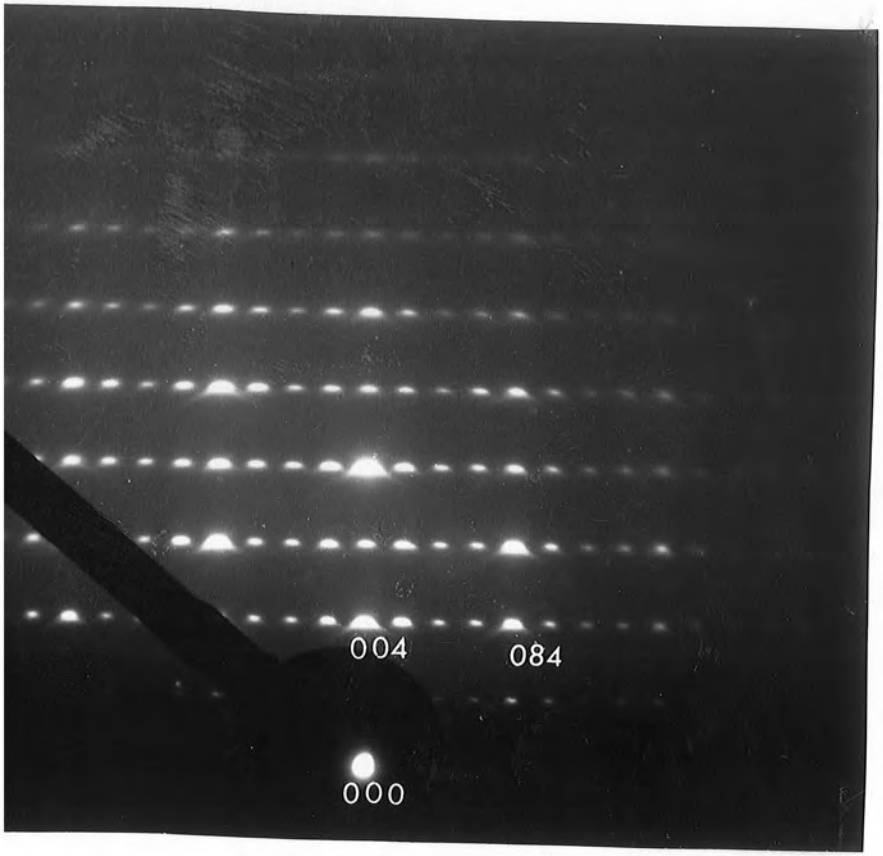
A diffraction pattern corresponds to a crystal lattice in reciprocal space. A reciprocal lattice point with coordinates $(h,k,\ell)$ is produced by a plane lying normal to the vector $\begin{pmatrix} h \\ k \\ \ell \end{pmatrix}$. The length of this vector is inversely proportional to the interplanar spacing. In three dimensions, the Bragg reflection condition can be determined using a geometrical model known as the Ewald sphere construction. This is shown in Figure 6.1. The crystal under investigation has its axis of rotation on the surface of a sphere of radius $1/\lambda$, at point B. The electron beam (wave) is incident normally to the surface at A. When the crystal is rotated so that a reciprocal lattice point lies on the surface of the sphere the diffraction occurs. The direction of the diffracted beam is given by the radius vector of the sphere through this point. The Bragg angle is simply $\theta$ in the diagram.

R.E.D. patterns were taken of a large number of copper sulphide layers grown on single crystal CdS by dipping in the $Cu^+$ ion solution for 10 seconds. The phases of copper sulphide were identified following the paper by Russell & Woods (1978). For reference, good R.E.D. micrographs of chalcocite and djurleite are shown in Figures 6.2 and 6.3. These patterns are formed by the unit cell geometries for chalcocite and djurleite shown in Figure 6.4 (Cook et al 1970). The so-called 'normal' orientation pattern is formed by diffraction of the electron beam by planes parallel to the a-axis. Since the energy of the beam is such that diffraction occurs at an angle of incidence of nearly $90^\circ$, the beam is incident parallel

to the a-axis. As an example, since a narrow spacing of planes will create a broadly-spaced diffraction pattern and vice versa, it is apparent that the narrowly spaced spots in the chalcocite pattern correspond to the broad spacing of planes, length b. The corresponding spots in the djurleite patterns are at double the distance apart, as a result of its b-axis being half the length. A full analysis of the patterns is more rigorously and easily carried out using reciprocal lattice vectors. The diagram in Figure 6.4 also demonstrates that chalcocite grains can form on CdS in three distinct orientations lebelled P,Q,R. Thus a $30^{o}$ rotation of the sample from the 'normal' orientation allows the beam to impinge and be diffracted by planes parallel to the b-axis of one of the other grains. This orientation is referred to simply as the $30^{o}$ position. Another $30^{o}$ rotation provides yet another 'normal' orientation for a diffraction pattern, and so on.

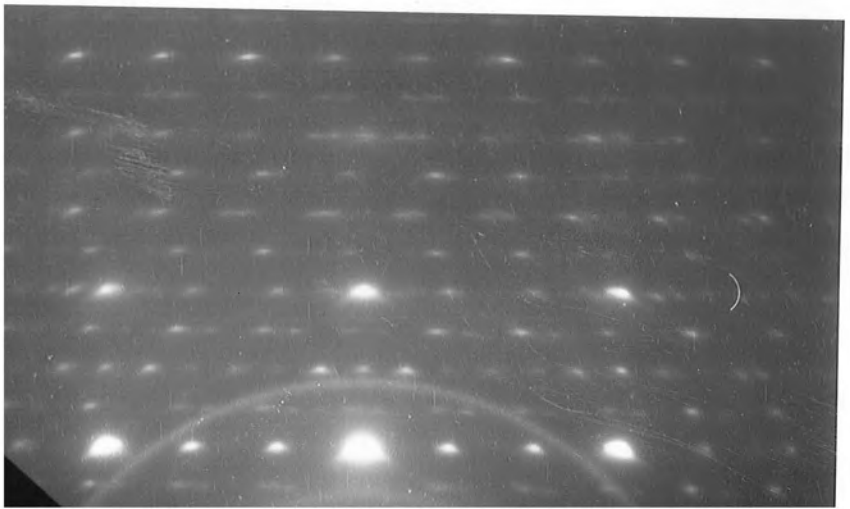
## 6.5 Electron Diffraction Results and Analysis

The R.E.D. patterns of several of the chalcocite layers in the 'normal' orientation displayed some extra and some missing spots, see Figure 6.5. In the $30^{o}$ orientation the expected chalcocite pattern was observed. Additionally, a regular hexagonal pattern was observed over a large area when the sample was rotated some $8^{o}$ clockwise or anticlockwise from the position for the usual pattern, Figure 6.6. It was thought, at first, that another phase might be responsible for this. However, the cell parameters calculated on this assumption did not fit any known phase of copper sulphide. A simpler explanation is forthcoming if one considers the leading diagonal XY (grain P) in the (001) plane of chalcocite, (Figure 6.4). This direction defined as $[1\bar{1}0]$ is $7.5^{o}$ from the a-axis of another grain (grain R) as observations required. By using the camera equation




a):R.E.D. micrograph of chalcocite "normal" orientation

(showing indexing of spots)



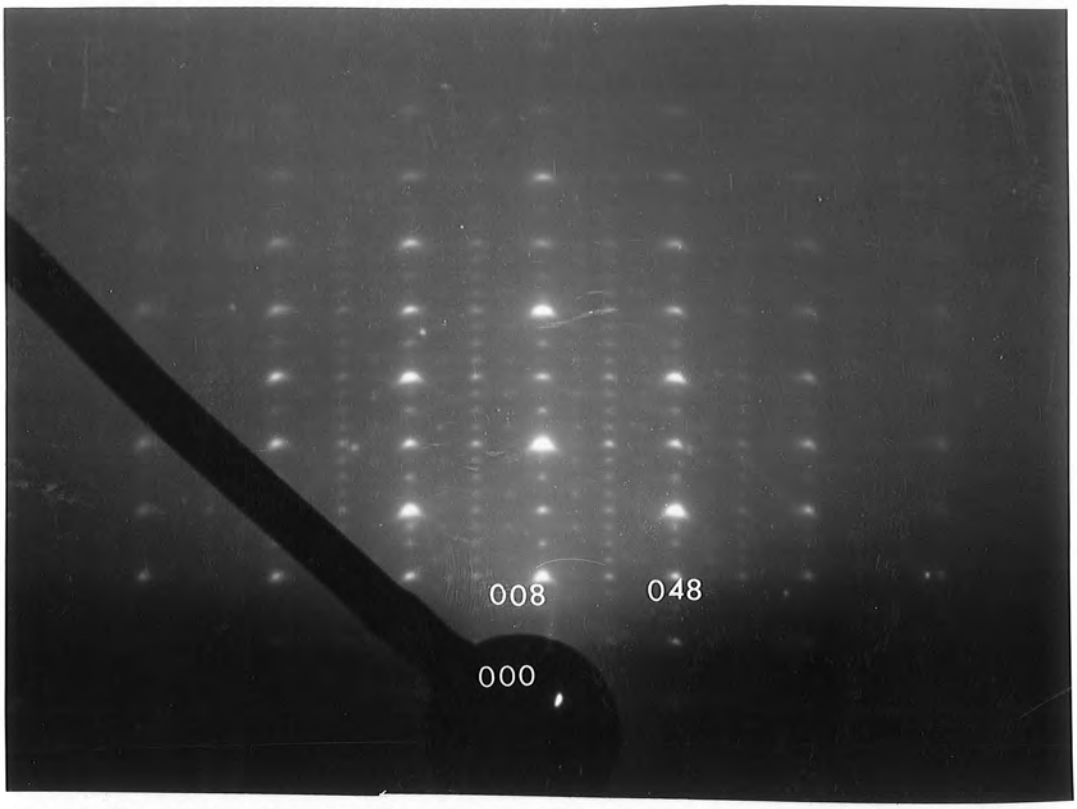
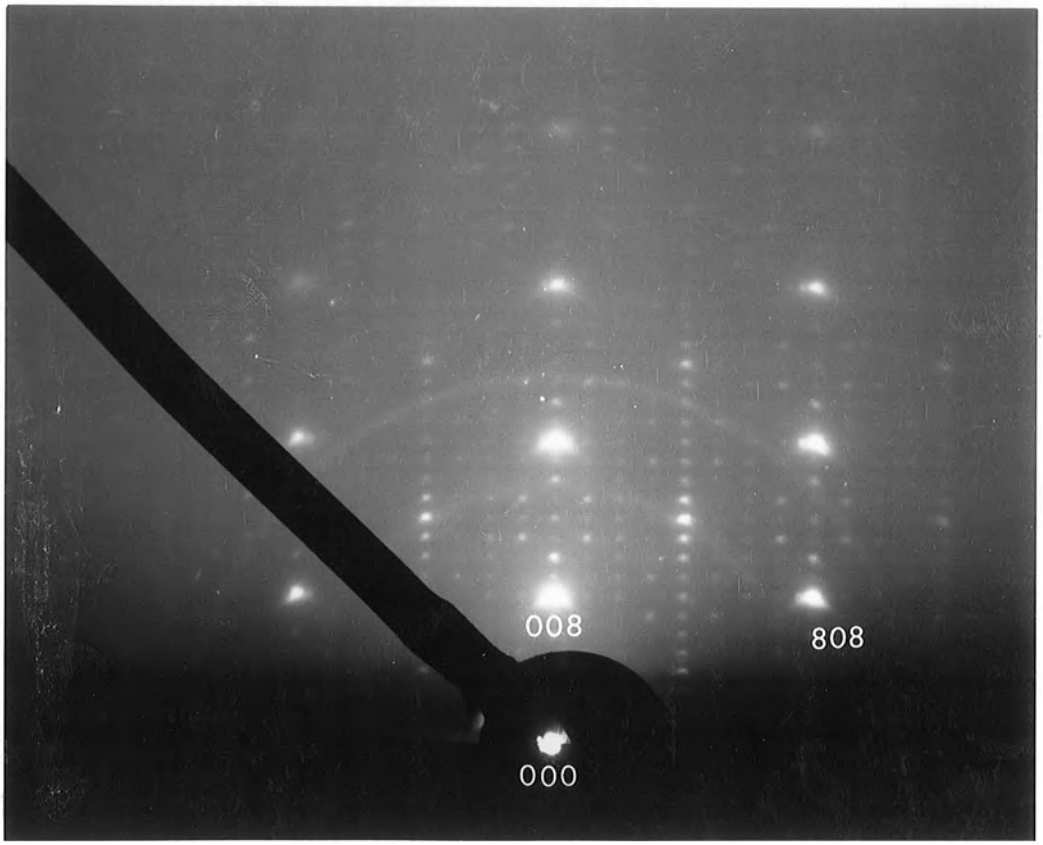



Figure 6.3 (a): R.E.D. micrograph of djurleite "normal" orientation

(showing indexing of spots)



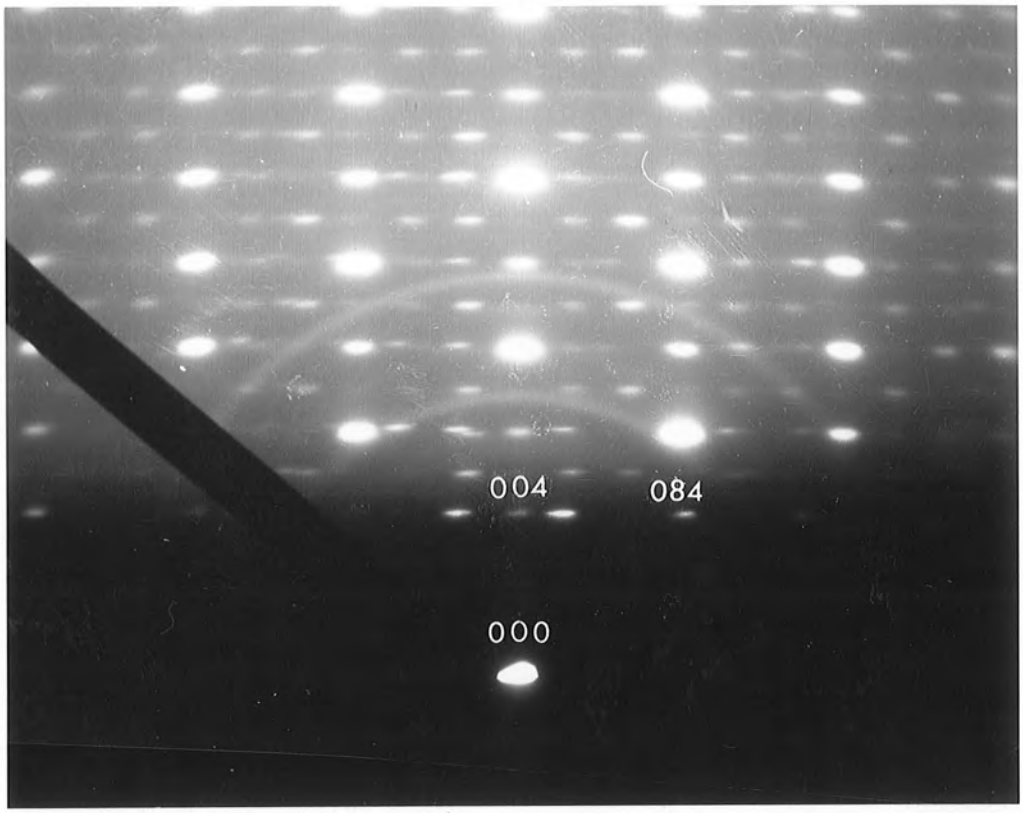
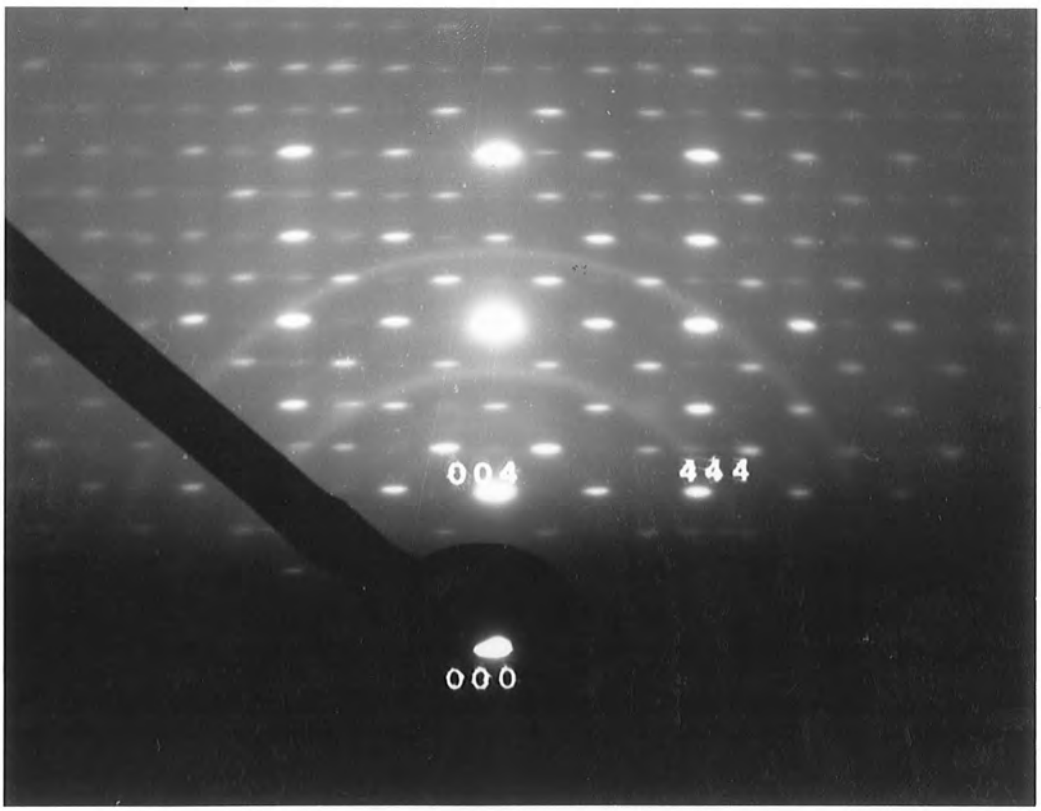



Figure 6.5 : R.E.D. micrograph of "modified" chalcocite pattern (showing indexing of spots)



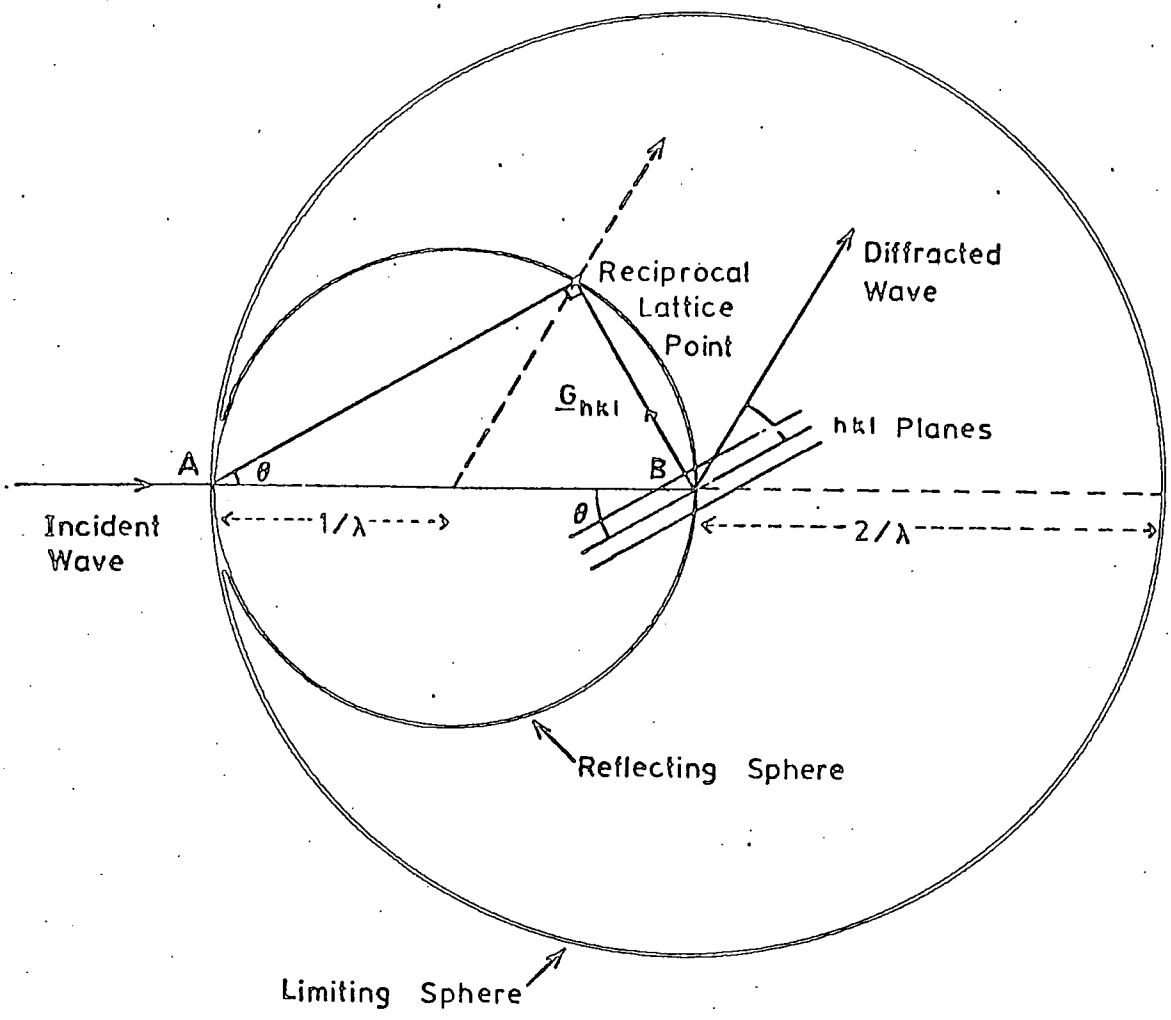



FIG. 6.1 SPHERE OF REFLECTION IN A RECIPROCAL LATTICE

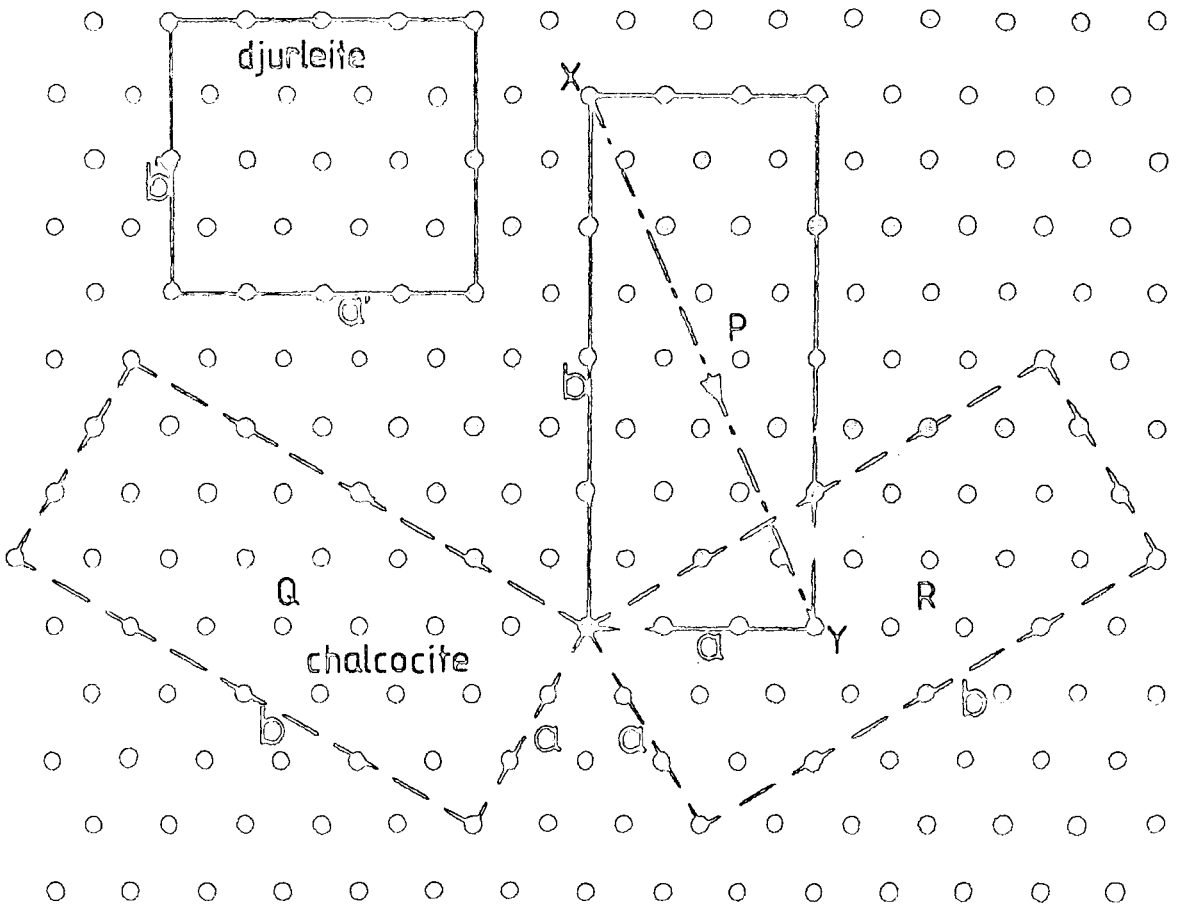



Figure 6.4 Unit cell geometries of Chalcocite and Djurleite

$$\lambda\ell = r_{hk\ell} d_{hk\ell} \qquad (6.1)$$

(where $\lambda\ell$ is the camera constant and $r_{hk\ell}$ is the diffraction spot spacing), and the A.S.T.M. index, the pattern was indexed as shown, agreement between calculated and measured d-values being better than 3% in all cases. Taking the cross-product of two of these reciprocal lattice vectors, namely (002) and (111) gives the direction of the electron beam as $[2\bar{2}0]$. This is seen to coincide with XY in Figure 6.4 confirming the indexing of the diffraction pattern.

As previously mentioned, the 'normal' orientation pattern $\sim 7.5^{o}$ from this one (see Figure 6.5), has some spots missing and some additional to those associated with the chalcocite. Around each bright spot appears a regular array of four weaker ones. The spacing of these is exactly the same (to within measurement error) as that of the spots surrounding the bright dots in Figure 6.6. It is suggested that double diffraction, i.e. diffraction of a diffracted beam, is responsible for this.

The explanation of the appearance of such phenomena on only a few samples is thought to be due to surface topography. The crystal cell parameters of chalcocite fit those of CdS to within a few per cent, but are smaller (see Cook et al, 1970, and Hadley et al, 1977). This means that as the copper sulphide grows on the CdS, microcracks occur, these will only grow in certain crystallographic directions (see Figure 6.7, which is of a layer of copper sulphide on the Cd basal plane of CdS). According to Reynolds and Cyzack (1960) the vertices of the hexagonal etch pit lie on the $\{10\bar{1}0\}$ planes of CdS, which correspond to $\{010\}$ planes in $Cu_2S$. Figure 6.7 shows that the cracks generally form along the direction of these vertices, i.e. the $[100]$ direction and must therefore be due to stress in the $[010]$ direction (b, in Figure 6.4). This is reasonable as the greatest lattice mismatch with CdS, 4.8% is in this

direction. If there is some slight misorientation of the crystal, i.e. cut a few degrees off the basal plane, then the cracks may grow preferentially in one direction, reducing the long range order perpendicular to this. This means that the R.E.D. patterns from the three grain orientations P,Q,R will be of different strengths. Similar reasoning is proposed to account for the infrequent appearance of the $8^{\circ}$ diffraction pattern.

It was not possible to obtain a good R.E.D. pattern from the copper sulphide on the smooth shiny cadmium face of the CdS. However the matt black copper sulphide grown on the sulphur face of the CdS dice produced good diffraction patterns. Observation showed that the temperature of the plating bath was extremely important. Dice plated at $90^{\circ}C$ had mixtures of the djurleite ($Cu_{1.96}S$) and chalcocite ($Cu_2S$) phases while those plated at $85^{\circ}C$ had djurleite with a small amount of chalcocite. Those dipped at $94^{\circ}C$, however, had layers of good chalcocite, all over the surface. The results were different for the dice subjected to longer dipping times. A die dipped at $90^{\circ}C$ for 45 minutes showed no trace of djurleite whatsoever, the whole surface being coated with a layer of chalcocite.

This sets a more stringent condition for the manufacture of chalcocite in actual devices than that suggested by Caswell, Russell and Woods (1977), who only looked at dice after long (45 minute) immersion in the plating bath. There are two possible explanations for this:

(1) the copper sulphide initially forms on the CdS substrate as djurleite and is then converted to the copper-rich phase of chalcocite by the further incorporation of copper ions. This would imply that in a normal heterojunction cell a thin layer of djurleite exists at the interface between the chalcocite and the cadmium sulphide; this is suggested by Massicot (1972) to be so after heat treatment; alternatively

(2) the thermal mass of the CdS substrate may be responsible, i.e. during a 10 second dip in the plating solution at $90^{\circ}C$ the sample (initially at

room temperature) does not achieve thermal equilibrium with the solution, because of its heat capacity. Thus, effectively the plating takes place at a temperature less than 90°C, and djurleite forms. With a longer dip, equilibrium is reached and any djurleite initially produced is converted to chalcocite. This is supported by the small existence region of $Cu_2S$ in the copper sulphide phase diagram of Dumon et al (1974).

### 6.5.1 The Effect of Thermal Mass

Two experiments were performed to test this latter hypothesis, (1) samples were heated prior to plating, and (2) samples with half the normal thickness, i.e. 1 mm thick, were used. In the first experiment, the pre-heating was accomplished, either by dipping the sample in deionised water heated to 90°C for 30 seconds after the normal etch in concentrated hydrochloric acid, or by using as the etchant a 15% solution of this acid heated to 90°C. In the latter event an etch of 20 seconds was administered and no wash took place before dipping.

In the second experiment the normal plating treatment was used, but samples only 1 mm thick were stuck to a glass slide with 'lacomit'.

The devices produced by these experiments were analysed using the R.E.D. technique. Those which had received a pre-dip heat treatment, generally produced a good chalcocite layer, even when devices made under control conditions, i.e. without pre-heating yielded a layer composed predominantly of djurleite. However, results were not totally consistent; on several occasions, a composite R.E.D. pattern was produced demonstrating that a mixture of djurleite and chalcocite had been formed. Twice pure djurleite with no trace of chalcocite was present, nevertheless the best chalcocite layers were produced by this technique, and there seemed to be little difference between samples pre-heated in deionised water or subjected to the hot etch. R.E.D. patterns of the copper sulphide on the

thin CdS substrates, exhibited a layer of djurleite, contrary to what had been expected. It is thought that there was little reduction in total thermal mass however, because the samples were stuck on to glass microscope slides.

6.5.2 Etching

While it is concluded that thermal mass is a contributory factor in determining the phase of copper sulphide which forms on CdS, the fact that the chalcocite was not always consistently produced implies that there is another important variable which has been neglected in the work described above. A study of the surfaces of ten diodes made previously, using the scanning electron microscope in the secondary emission mode, revealed that there was some correlation between the surface roughness of the plated layer and the efficiency of a cell with the rougher surfaces producing the more efficient devices. This might be expected, as a lightly etched surface could still possess a work damaged layer of CdS from the mechanical polishing and this, at the heterojunction interface, would form a shunt path. However, a R.E.D. investigation of the phase of copper sulphide on CdS substrates after different etching times in HCl, was undertaken. This showed that in general, samples given a longer etch in acid were more likely to produce chalcocite layers. For example, a sample etched in HCl for 1 minute and then heated to 90$^{o}$C in deionised water before plating for 10 secs, produced a very good R.E.D. pattern of chalcocite with no trace of djurleite, whereas a similar sample given a 10 second etch followed by the same pre-heat and plating treatment, produced a pattern which resembled predominantly that of djurleite with traces of chalcocite as the beam was moved across the surface. S.E.M. micrographs of the surfaces of heavily and lightly etched heterojunction cells are shown in Figure 6.8. The corresponding R.E.D. patterns are

are shown in Figure 6.9. It is not known why the severity of the etch which produces increasingly pronounced hexagonal cones on the sulphur face of the CdS substrate should control the phase of copper sulphide, but the effect is possibly a result of different proportions of the crystallographic faces being exposed during prolonged etching, and it may be that different planes have different probabilities for the formation of the various copper sulphide phases. The work of Borders (1976) using ion backscattering suggests a dependence of copper sulphide growth on crystallography and surface treatment, however, there has been no time to investigate this latter point further.

### 6.5.3 Consequences of Heat Treatment

A brief heat treatment at 200°C is normally administered to a freshly plated CdS/$Cu_2S$ heterojunction cell in order to achieve optimum photovoltaic efficiency. This is generally thought to cause the diffusion of copper ions from the copper sulphide into the CdS creating a high resistance copper compensated region in the vicinity of the junction (see, for example, Shiozawa et al 1969). It has been suggested from the evidence of changes in the spectral response, that this leads to the conversion of the chalcocite to the less copper-rich phase of djurleite (Massicot, 1972; Caswell and Woods, 1977). Devices which showed good R.E.D. patterns of chalcocite immediately after fabrication, were subjected to a two minutes 'bake' at 200°C. When these samples were examined again in the electron microscope, they showed R.E.D. patterns which typically corresponded to a mixture of chalcocite and djurleite, that is, a partial transformation from chalcocite to djurleite had occurred. The R.E.D. pattern of a sample after this heat treatment is shown in Figure 6.10. The pattern after heat treatment is clearly that of djurleite with some extra spots around the bright

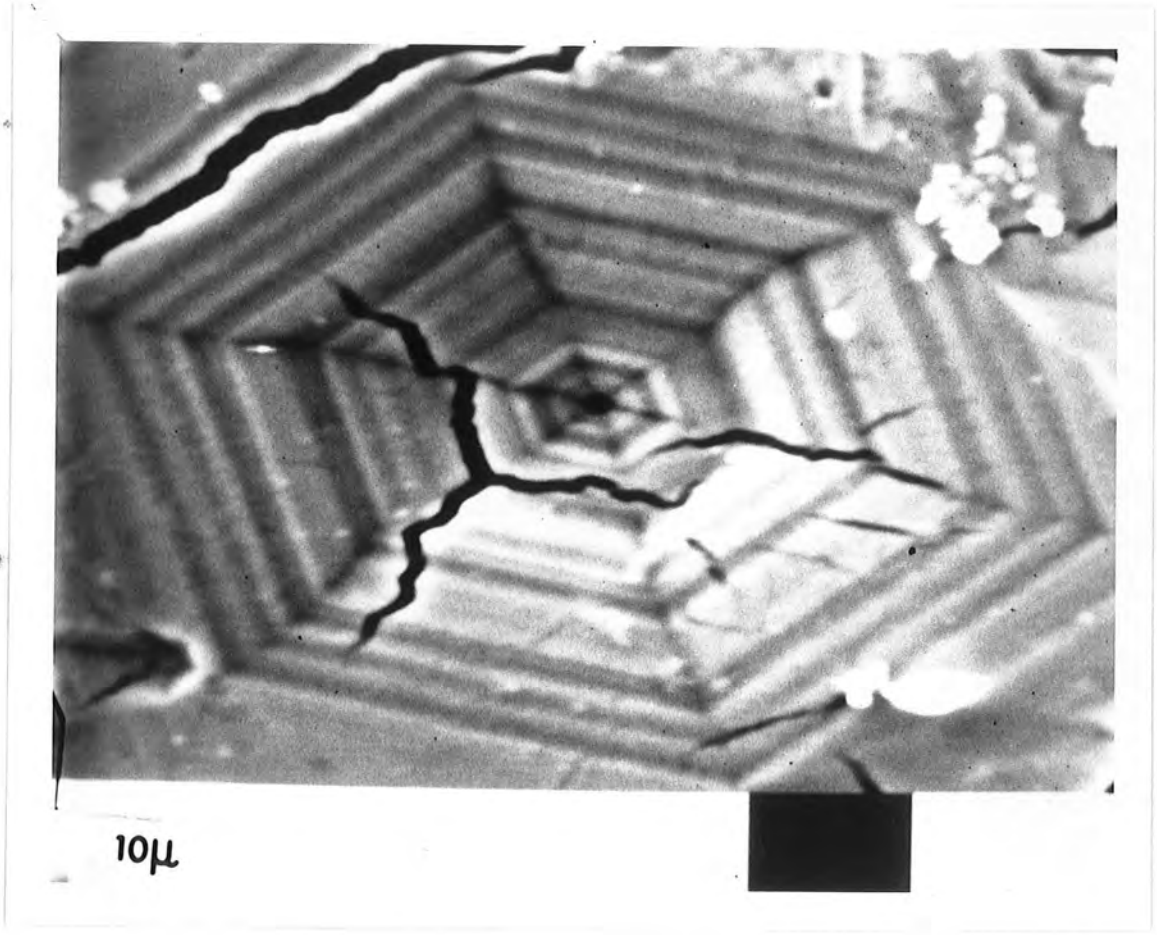



Figure 6.7 : Cracks in $Cu_2S$ grown on Cd basal plane of CdS.

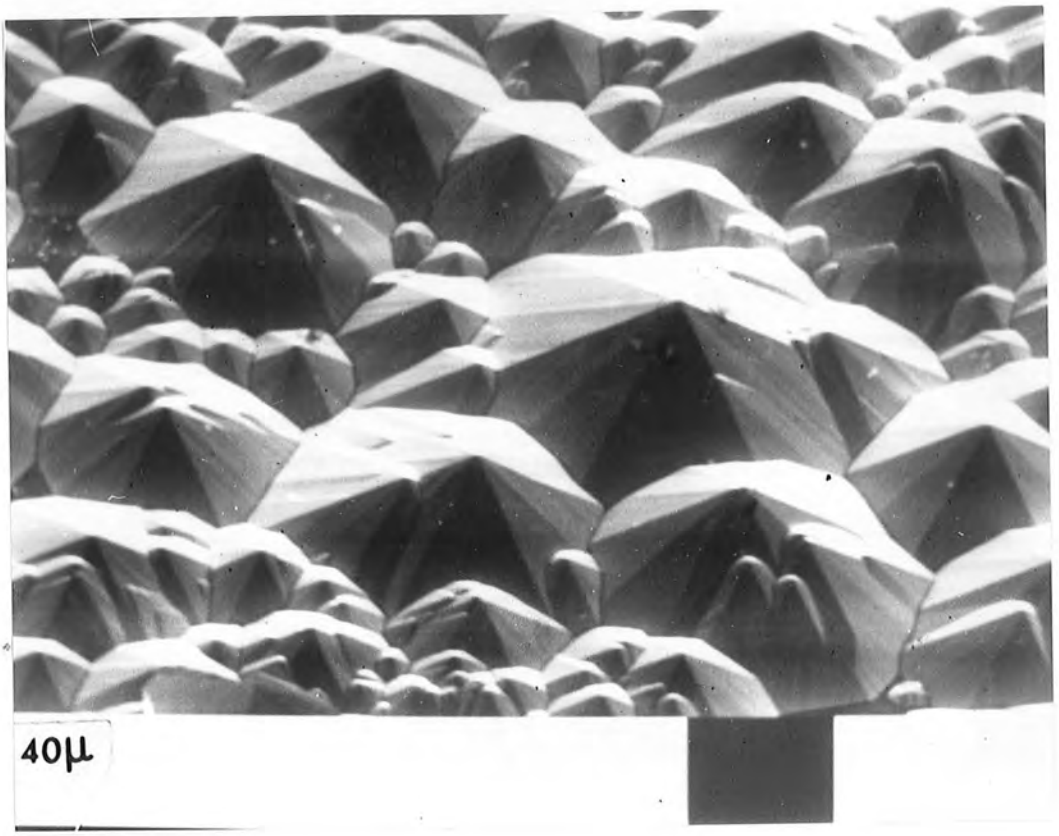
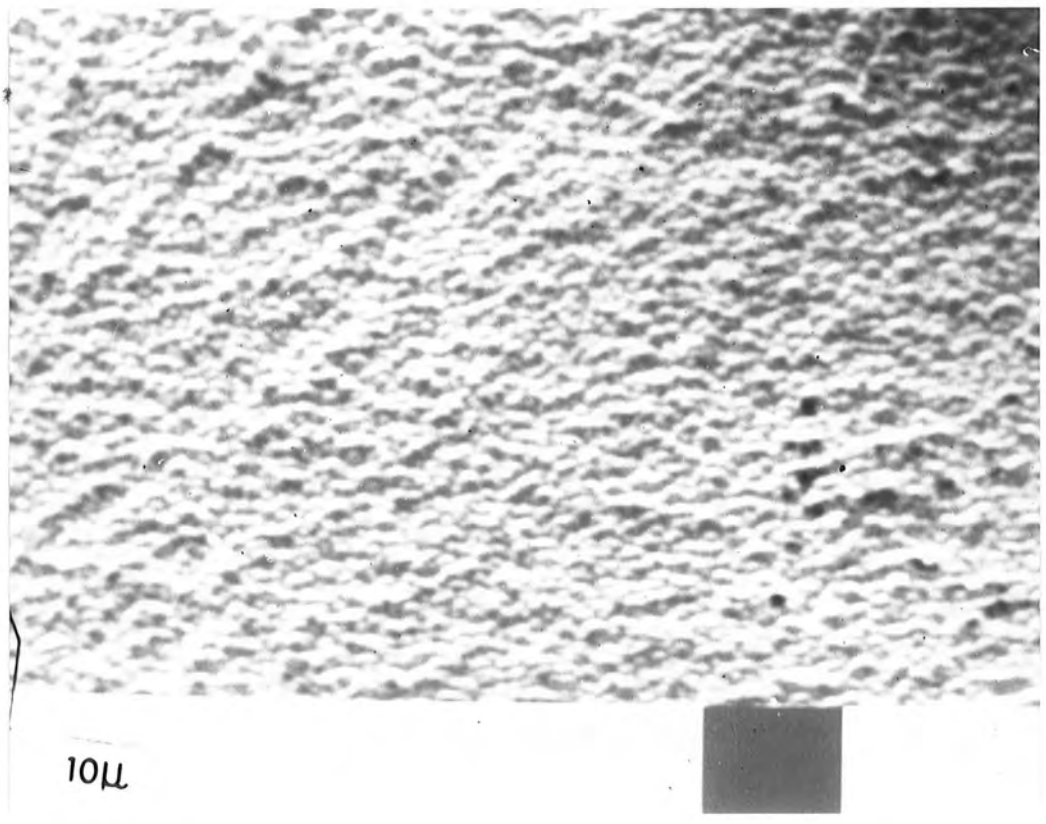



Figure 6.8 (a) : $Cu_2S$ grown on deeply etched CdS (S-plane)



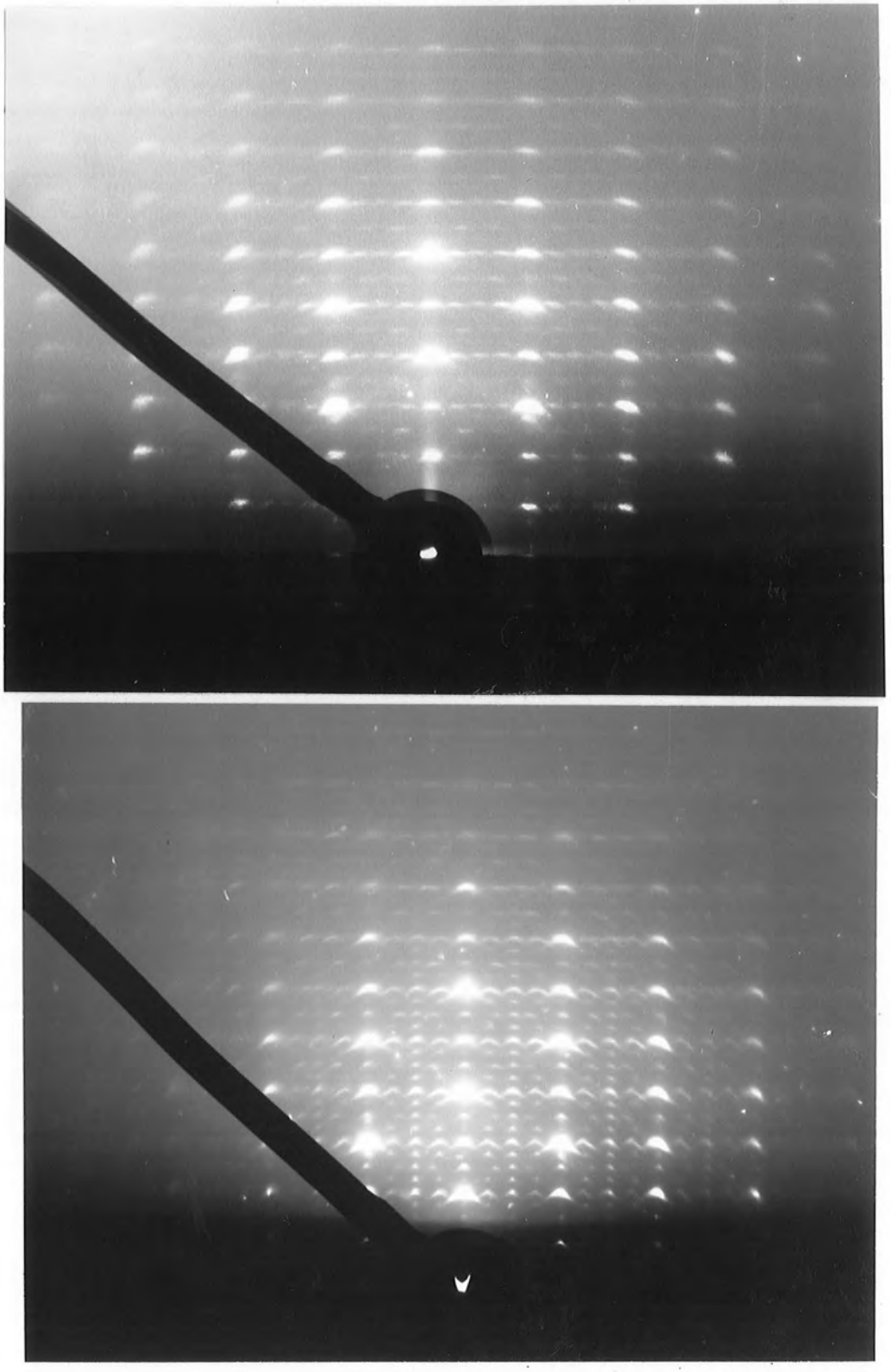


Figure 6.9: R.E.D. patterns from the surfaces in Fig. 6.8

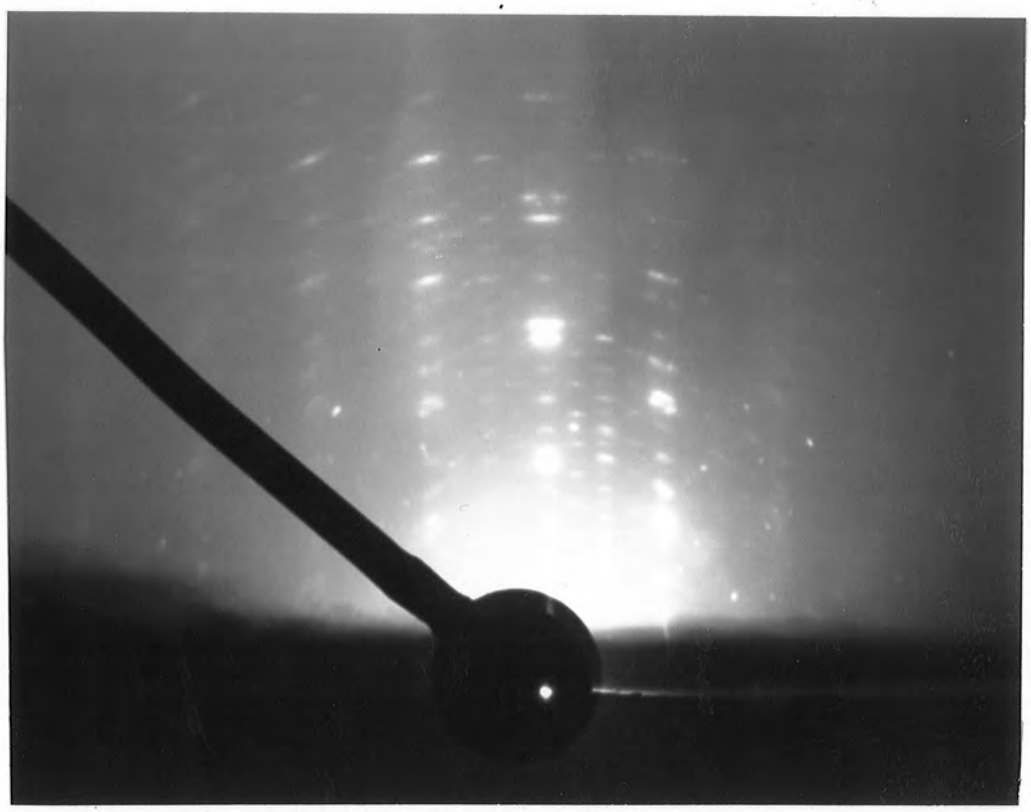


Figure 6.10: R.E.D. micrograph of djurleite after heat treatment

ones, in addition, suggesting oxidation of the surface. Diodes which had R.E.D. patterns of djurleite prior to baking showed no significant change after 2 minutes heating in air at 200°C.

It must be emphasised that the R.E.D. technique can only reveal the phase of copper sulphide present within a few hundred angstroms of the surface, whereas the heterojunction in a typical cell lies roughly 0.3 μm (i.e. some 3,000 Å) below the surface. However on a sample roughened by the customary HCl etch, the effective penetration of the beam will be greater, because of the range of different angles the surface presents to the beam. Thus the actual depth of the copper sulphide layer which is observed is a function of surface treatment and cannot be closely determined. Therefore in the experiment just described, it may only be the surface of the copper sulphide which is oxidised to form djurleite during the heat treatment, while the material at the junction remains chalcocite. This would at least be consistent with the observations.

Caswell and Woods (1977) also suggest, again from spectral response measurements, that djurleite may be transformed back to chalcocite by chemical reduction. In order to extend this evidence, experiments were conducted on samples possessing a layer of djurleite either as a consequence of the heat treatment, or because of the conditions of growth. These showed that djurleite formed in both ways reduced to chalcocite when immersed in a solution of hydrazine hydrate for periods of between 2 and 24 hours. This is quite consistent with the predictions of Caswell and Woods (1977), who suggested that oxidation is a two-stage process; firstly surface oxidation occurs, with little effect on cell characteristics, secondly oxygen ions reach the heterojunction interface where they form traps (Te Velde, 1973).

### 6.5.4 Variation in pH. of Plating Solution

In another series of experiments the effects that changes in the pH of the plating had on the phase of copper sulphide were investigated. The plating solution was made up using the normal procedure, the pH being brought to 2.5 as determined with narrow range pH paper. A sample was then dipped for 10 seconds after the customary acid etch but without any pre-heat treatment. A few drops of HCl were then added to bring the pH close to 1.5, and another sample dipped for 10 seconds. Several drops of hydrazine hydrate were then added to bring the pH of the solution to about 3.5 and a CdS die dipped once more. However after 10 seconds, it was apparent that little copper sulphide had formed, and the sample was therefore subjected to a further 10 seconds plating. A R.E.D. analysis revealed that both the control and the layer produced under increased acidity consisted of a mixture of the chalcocite and djurleite phases. On the other hand the alkaline preparation conditions led to the formation of hexagonal copper sulphide. The particular hexagonal phase was that referred to by Cook et al (1970) as $Cu_xS$.

The experiment was repeated incorporating a pre-heat treatment for the CdS substrates. This time the plating lasted for 10 seconds in all three trials, and resulted in the production of good chalcocite in both the control and acidic cases, while the alkaline conditions produced a good djurleite layer. Russell and Woods (1978) have shown that when unencapsulated $CdS/Cu_2S$ heterojunction cells are left in the atmosphere for two years, a chalcocite layer transforms to a djurleite one with traces of chalcocite, whereas an initial djurleite layer undergoes a phase change to the Cook hexagonal form. Re-examination of devices after eight months revealed R.E.D. patterns which support these observations totally, both for samples initially prepared as djurleite and those transformed into djurleite as a result of heat treatment. This suggests that the Cook

hexagonal $Cu_xS$ is a less copper-rich phase than djurleite, which the experiments using plating solutions with difference pH's support. It appears that with values of pH between about 2.5 and 4, the copper sulphide layer becomes richer in copper as the pH decreases. If the pH is made less than about 1.5 the solution turns blue-green, indicating the presence of $Cu^{++}$ ions and a less copper-rich phase of copper sulphide would form. Thus a pH of about 2 seems to create the best conditions for chalcocite growth. A likely explanation is the following. Cuprous chloride is only slightly soluble in water, however if mixed with HCl it forms a $Cu_2Cl_4^{--} + 2H^+$ complex, soluble at temperatures near $90^oC$. This complex is relatively stable, but in order to prevent oxidation to $Cu^{++}$, the reducing agent hydrazine hydrate is added.

This stabilises the $Cu_2Cl_4^{--}$ ion further by forming cuproammonium type complex with the copper. There will of course be a complicated dynamic equilibrium set up between alkali and acid and copper chloride, otherwise a salt would be produced and the HCl and hydrazine hydrate would serve no useful purpose. If excess acid is added, it will upset this equilibrium, causing the production of more hydrazine chloride salt. This means effectively a reduction in the quantity of alkali available to stabilise the $Cu_2Cl_4^{--}$ ion, and oxidation to $Cu^{++}$ occurs, which is observed as the solution turns blue-green. In the experiment, the solution was still colourless when plating occurred, hence chalcocite was produced. If the pH is altered in the other direction by adding excess hydrazine hydrate, then two possibilities occur. The reducing agent may reduce the copper ions to metallic copper, thus decreasing the number of $Cu^+$ ions available for reaction, or the excess alkali may react with acid to produce more salt, this will reduce the amount of HCl available to form the stable $Cu_2Cl_4^{--}$ ion, allowing the oxidation of $Cu^+$ to $Cu^{++}$.

In fact, the formation of metallic copper was observed, suggesting the former mechanism, and djurleite was produced on the CdS substrate.

The effect of changes in the pH of the plating solution are compounded by the effects of changes in temperature, and of variations in thermal mass, length of plating and etch treatment. Changes in all these variables affect the phase of the copper sulphide layer produced. In addition the level of doping of the CdS is known to influence the phase of $Cu_xS$ produced (Hill et al., 1977, Kantariya, 1978), however all these experiments were carried out on material from one crystal boule, so this, at least, was eliminated.

## 6.6 Conclusions

With so many variables, it is very awkward to optimise conditions to provide higher efficiency cells, indeed it is very difficult even to attain reproducibility. However, the work reported here has provided some insight into the problems associated with the chemistry of formation of the copper sulphide layer. As a result, subject to strict conditions of pH (near 2), temperature ($95^{o}C$), etch (30 seconds in conc. HCl), and a pre-plating heat treatment, good reproducibility and uniformity of chalcocite layers on the CdS substrate has been achieved.

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## CHAPTER 6


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# CHAPTER 7

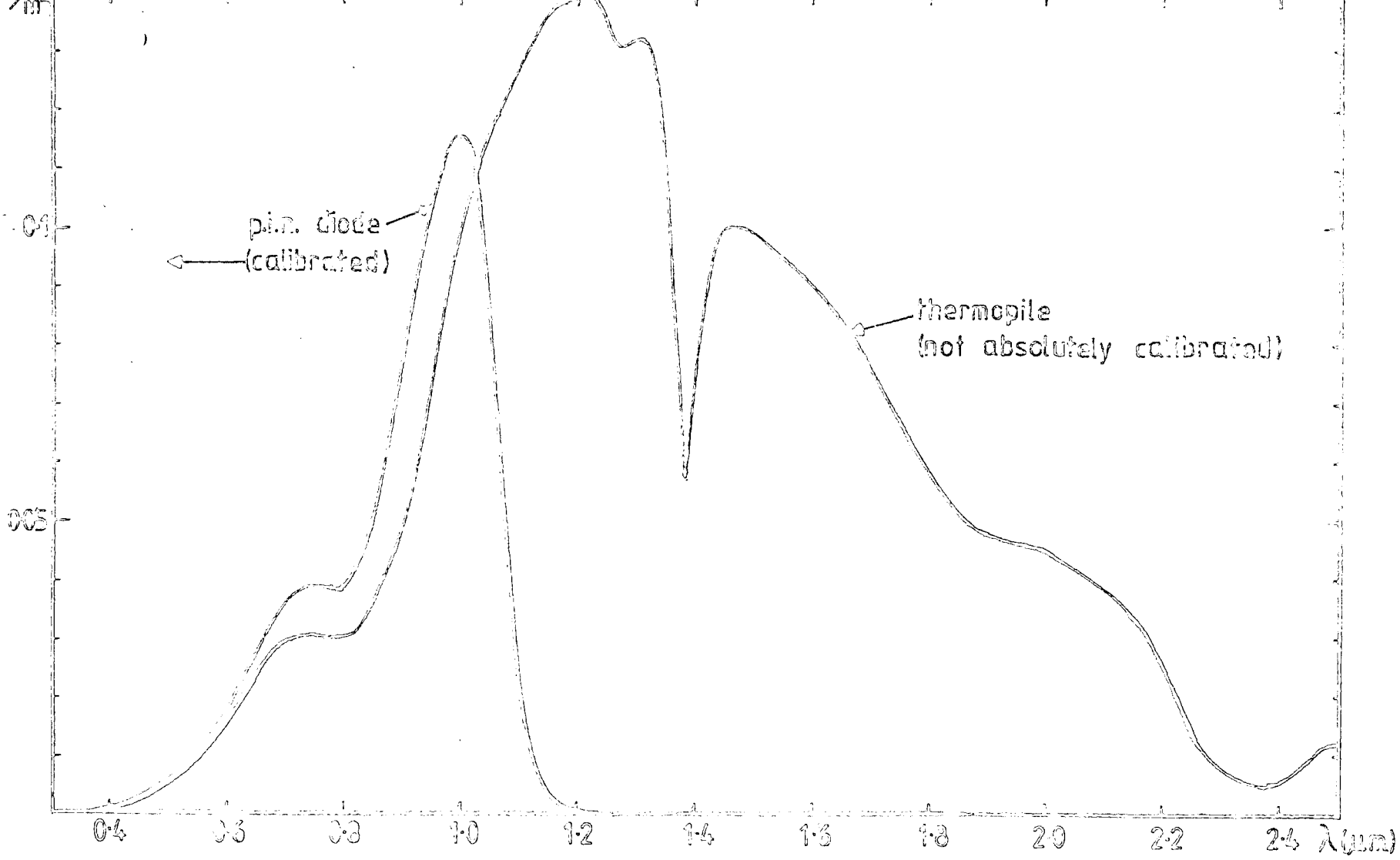
## PHOTORESPONSE MEASUREMENTS

### 7.1 Introduction

The models of the $CdS/Cu_2S$ solar cell considered in detail earlier, the Clevite Model and that of Te Velde, both demonstrate the importance of the copper compensated layer in the optimised cell. Thus, it is expected that the spectral response of the photoconductivity of CdS:Cu will have a significant effect on the response of the solar cell, if either of these models is correct. The experiments described in this chapter were all designed to give a better insight into the operation of the $Cu_2S/CdS$ solar cell. The measurements included spectral distribution of photoconductivity in copper doped CdS, photocapacitance of Schottky diodes and heterojunctions, photoresponse of the open circuit voltage and short circuit current of photovoltaic devices. In addition current-voltage characteristics were measured under illumination and in the dark. All these parameters were studied as a function of heat treatment.

### 7.2 Measurement of Spectral Response

All of the spectral response measurements were made over the wavelength range from 0.35 μm to 2 μm, using a Barr and Stroud monochromator, Type VL2, fitted with Spectrosil 'A' silica prisms. The light source used was a 250 watt 24 volt quartz halogen tungsten lamp. Generally this was supplied from a 20 V D.C. stabilised power unit. The energy distribution of this source with the VL2 monochromator is shown in Figure 7.1. This measurement was made using a thermopile to measure the energy at the exit slit of the monochromator. To enhance the signal the incident beam was chopped at 8 Hz and the thermopile output fed into a lock-in amplifier (Brookdeal Ortholoc 9502). The slits of the monochromator were




Figures 7.1 & 7.2 Energy distribution of light source + monochromator

adjusted to a width of 0.5 mm and were not altered from this value for any of the subsequent experiments.

In order to provide a check on this measurement and to provide an absolute value of radiant power, at the exit slit, the output of the monochromator was measured using a silicon P.I.N. diode type 10 DF, made by United Detector Technology Inc. This has essentially a flat band response between 450 nm and 950 nm and is calibrated at one wavelength. The output from this device was large enough to drive a chart plotter (Honeywell 196) directly. The response recorded using this diode is shown in Figure 7.2. It is readily observed that the agreement between these two measurements is very close. The bandwidth of the monochromator varied with wavelength from 70 Å at 0.5 μm to 350 Å at 1.15 μm.

### 7.2.1 Setting up Procedure

Before the monochromator was used, and frequently during use, its wavelength was calibrated in the following manner. The tungsten lamp was replaced by a sodium line source which was placed at $L_1$ (Figure 7.3). Mirrors $M_1$ and $M_2$ were adjusted until a sharp image of the sodium source was focussed on the entrance slit $S_1$. The wavelength drum was rotated until the maximum yellow light intensity was observed at the exit slit. This ought to correspond to a wavelength of 5893 Å or a drum reading of $23^{\circ}\ 35'$, if it did not, the coupling spindle was loosened, adjusted and tightened. The drum was then taken to longer wavelength and rotated slowly back to the maximum until satisfactory adjustment had been achieved. In this way the monochromator was calibrated for measurements from low to high photon energy, however it was not adjusted for measurements in the other direction owing to the backlash in the worm gearing.

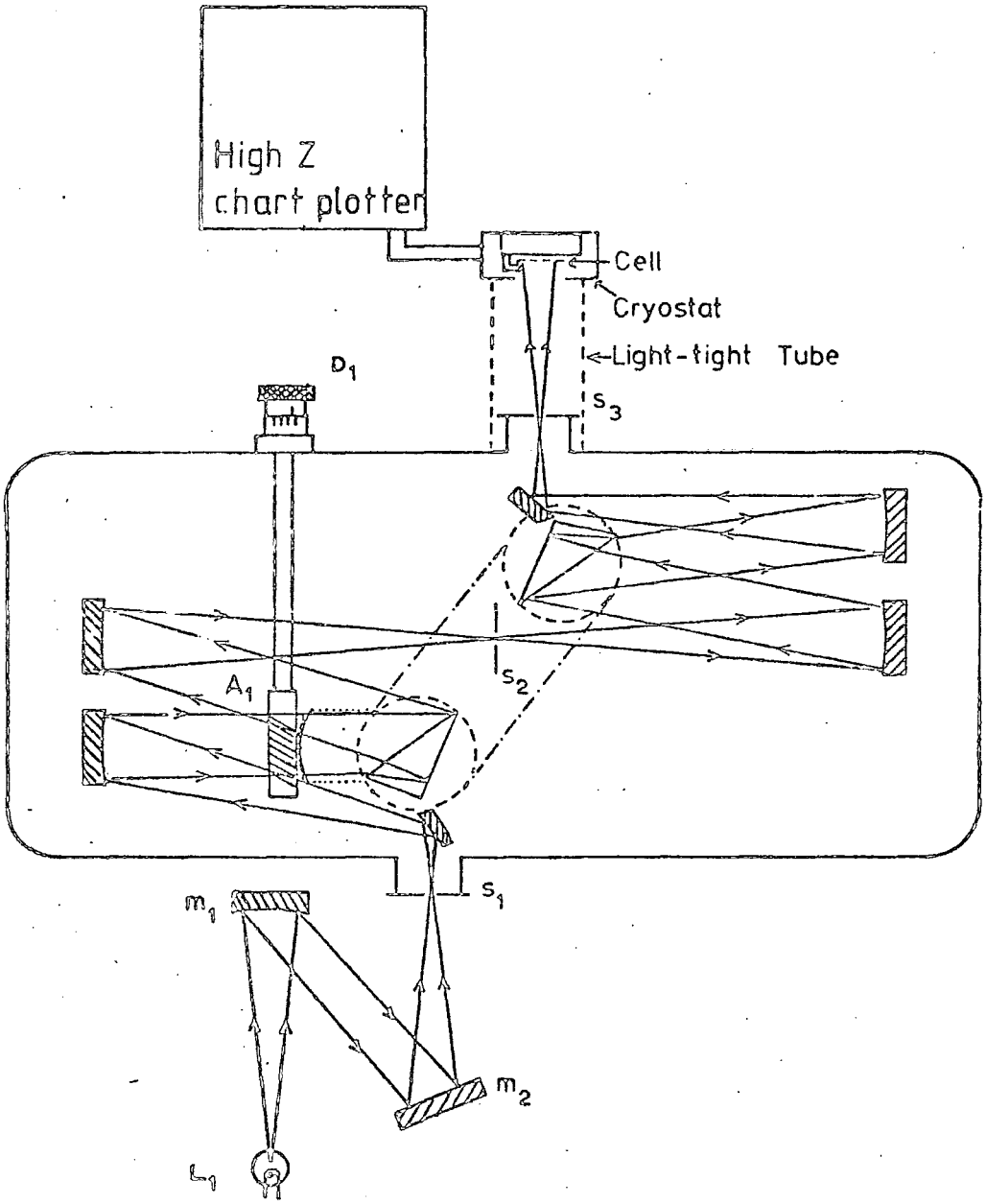



FIG. 7.3 MONOCHROMATOR AND O.C.V MEASUREMENT APPARATUS

## 7.3 Photoconductivity

This phenomenon has already been described but further details will now be given. The photoconductive gain of a bulk sample may be defined as the number of charge carriers passing between the electrodes per photon absorbed. Thus a gain of less than one means an electron recombines with a hole before it has reached the anode. A gain of greater than one implies that the generated electron passes through the sample to the anode, but to preserve charge neutrality, another electron must be injected at the cathode. The number of such electrons traversing the sample before recombination occurs determines the gain. The hole also generated by the photon is trapped quickly as hole lifetimes in CdS are very much shorter than those of electrons, and can usually be neglected. It is therefore apparent that the gain is inversely proportional to the response time. It is impossible to produce a fast sensitive photoconductor.

### 7.3.1 Sensitisation

The long electron lifetime required for high sensitivity may be obtained by incorporating certain recombination centres known as sensitising centres. Experimentally, a relatively pure crystal of CdS is found to have electron and hole lifetimes in the range of $10^{-6}$ - $10^{-8}$ secs, and is therefore regarded as an insensitive photoconductor. The incorporation of cadmium vacancies will convert it into a sensitive photoconductor, with an electron lifetime of $10^{-2}$ - $10^{-3}$ secs and a hole lifetime less than $10^{-8}$ secs (see, for example, Bube 1960). The electron lifetime is improved only at the expense of the hole lifetime. Increasing the number of recombination centres of the type originally present, would of course only decrease both electron and hole lifetimes, however, sensitisation occurs when recombination centres of a different kind are introduced. This is illustrated by a simple quantitative model, following Rose (1963).

Consider a photoconductor containing one class of recombination centres whose capture cross section for both electrons and holes is $10^{-15}$ $cm^2$. The densities of electron and hole occupied centres are taken to be the same, $10^{15}$ $cm^{-3}$. Then the electron and hole lifetimes are given by ,

$$\tau_n = \tau_p = (V S_{n1} P_{r1})^{-1} = 10^{-7} \text{ secs} \qquad (7.1)$$

$V$ = thermal velocity of electrons and holes

$S_{n1}$ = capture cross-section of class 1 centres

$P_{r1}$ = density of occupied centres.

Suppose now $10^{16}$ $cm^{-3}$ impurity states are added just below the Fermi level, so that they are all filled with electrons in the dark. These have a small capture cross section for electrons of $10^{-20}$ $cm^2$ and a larger cross section of $10^{-15}$ $cm^2$ for holes. Under illumination, a redistribution of electrons and holes within the recombination centres takes place subject to the following condition that free holes and electrons must enter the centres at the same rate, i.e.:

$$n\, p_{r1}\, V\, S_{n1} = p\, n_{r1}\, V\, S_{p1} \qquad (7.2)$$

and

$$n\, p_{r2}\, V\, S_{n2} = p\, n_{r2}\, V\, S_{p2} \qquad (7.3)$$

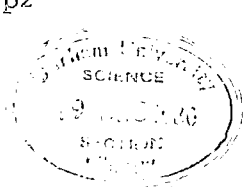
where $p$, $n$ are densities of free holes and electrons,

$r_1$ and $r_2$ refer to recombination states class 1 and class 2

$S$ refers to capture cross sections.

Rearranging gives

$$\frac{p_{r1}}{n_{r1}}\frac{S_{n1}}{S_{p1}} = \frac{p_{r2}}{n_{r2}}\frac{S_{n2}}{S_{p2}} = \frac{p}{n} \qquad (7.4)$$



Because the number of recombination centres must remain constant

$$n_{r1} + p_{r1} = \text{const.} = N_{r1} \tag{7.5}$$

$$n_{r2} + p_{r2} = \text{const.} = N_{r2} \tag{7.6}$$

Equation (7.4) becomes, with $S_{n1} = S_{p1}$

$$p_{r1} = \frac{p_{r2}\, n_{r1}}{n_{r2}} \frac{S_{n2}}{S_{p2}} \tag{7.7}$$

Since the class II centres have a low capture cross section for electrons, there will be a tendency for electrons to shift from class II to class I centres; thus for low light levels

$$n_{r1} \rightarrow N_{r1}$$

$$p_{r2} \rightarrow N_{r1}$$

$$\text{and} \quad n_{r2} \approx N_{r2}$$

With these approximations, equation (7.7) becomes

$$p_{r1} \doteq N_{r1} \frac{N_{r1}}{N_{r2}} \frac{S_{n2}}{S_{p2}} \tag{7.8}$$

putting in values, $p_{r1} \doteq 10^{-6} N_{r1}$ .

The rate at which electrons are trapped is :

$$n/\tau_n = n\, p_{r1}\, V S_{n1} + n p_{r2}\, V S_{n2} \tag{7.9}$$

and

$$\tau_n = \frac{1}{P_{r1}\, V S_{n1} + P_{r2}\, V S_{n2}} \tag{7.10}$$

$$= \frac{1}{10^{-6}\, N_{r1}\, V S_{n1} + N_{r1}\, V S_{n2}}$$

$$= \frac{1}{N_{r1}\, V S_{n2}} = 10^{-2} \text{ sec.}$$

Thus the sensitivity of the photoconductor has been increased by a factor of $10^5$ by adding the sensitising centres. The hole lifetime has been decreased from $10^{-7}$ to $10^{-8}$ secs. Phenomenologically the electron recombination traffic through the Class I states has been greatly reduced by filling them with electrons from Class II states.

### 7.3.2 Infra-red Quenching

A phenomenon normally associated with photoconductive CdS is infra-red quenching. This occurs when a given photocurrent excited by visible light is considerably reduced by simultaneous illumination with infra-red light. This may be explained by considering a photoconductor, containing both Class I and II centres, sensitised as described above. If the sample is illuminated with infra-red light that is selectively absorbed by the Class II centres, electrons will be excited from the valence band into these centres, see Figure 7.4. The free holes thus produced may then be captured by the insensitive, Class I states. Since this process has shifted holes from Class II to Class I centres, the situation is now exactly the reverse of sensitisation, and so the electron lifetime is reduced, as is the photocurrent. Thermal quenching, a related phenomenon is an increase in temperature while the illumination remains fixed causing the sensitised photoconductor to revert to the insensitive state, because the steady state Fermi levels are shifted further from the band edges with the result that the sensitising states become traps instead of recombination centres.

## 7.4 Experimental Techniques

Measurement of the spectral response of photoconductivity is a useful tool for providing information about the energy levels of trapping and recombination levels in semiconductors. This technique has been used extensively in the study of impurity levels in CdS, for example by

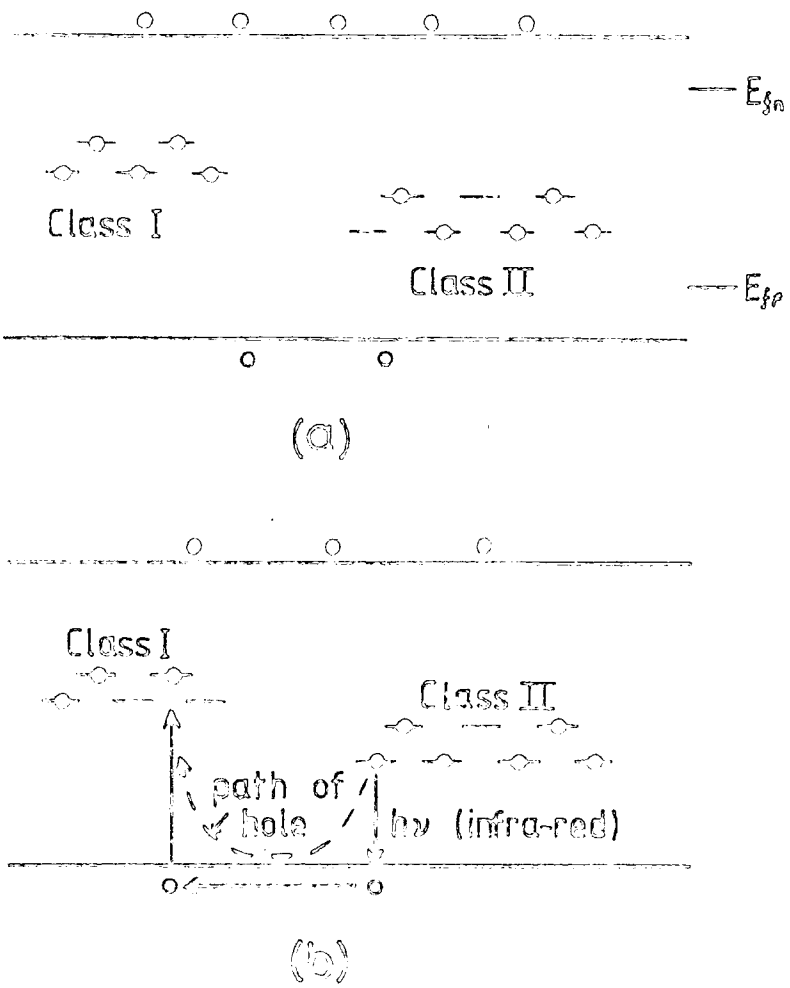



Figure 7.4 Model for Infra-red Quenching

(a) supralinear photoconductor strongly illuminated
(b) addition of infra-red light to (a)

Rose (1951), Bube and Thomsen (1955) and Nicholas and Woods (1964). By using a secondary light source to provide a 'bias illumination' it is possible to sensitise suitably photoconductive samples of CdS, so that the energy levels responsible for infra-red quenching may also be observed (Liebson, 1955). The Class II centres found in copper doped CdS are generally accepted to be 1.1 eV above the valence band (Bube, 1957).

### 7.4.1 Photocapacitance

Another technique similar to that of photoconductivity is photocapacitance. Sah et al (1970) provide a description of this and a comprehensive survey of complementary experiments. To have a significant photoconductive response, the dark conductivity of a sample must be low, which implies only material with a resistivity greater than $10^3$ Ωcm is useful. Lower resistivity material is unsuitable simply because of the small ratio of the number of photoexcited to free carriers. In the photocapacitance experiment, a Schottky barrier contact replaces one of the ohmic contacts, creating a depletion region, thus a change in occupancy of any traps produced by the absorption of light in this region alters its width and changes it capacitance. The different electronic processes responsible for photocapacitance effects can be described in terms of the energy band diagrams in Figure 7.5.

The processes illustrated are:

(a) Excitation of photocapacitance by intrinsic radiation. When an electron-hole pair is created in the vicinity of the junction, the electron drifts in the built-in field further into the CdS, while the hole is captured by one of the deep levels in the CdS depletion region. The increase in positive space charge this creates gives rise to the measured photocapacitance by narrowing the depletion region in the CdS.

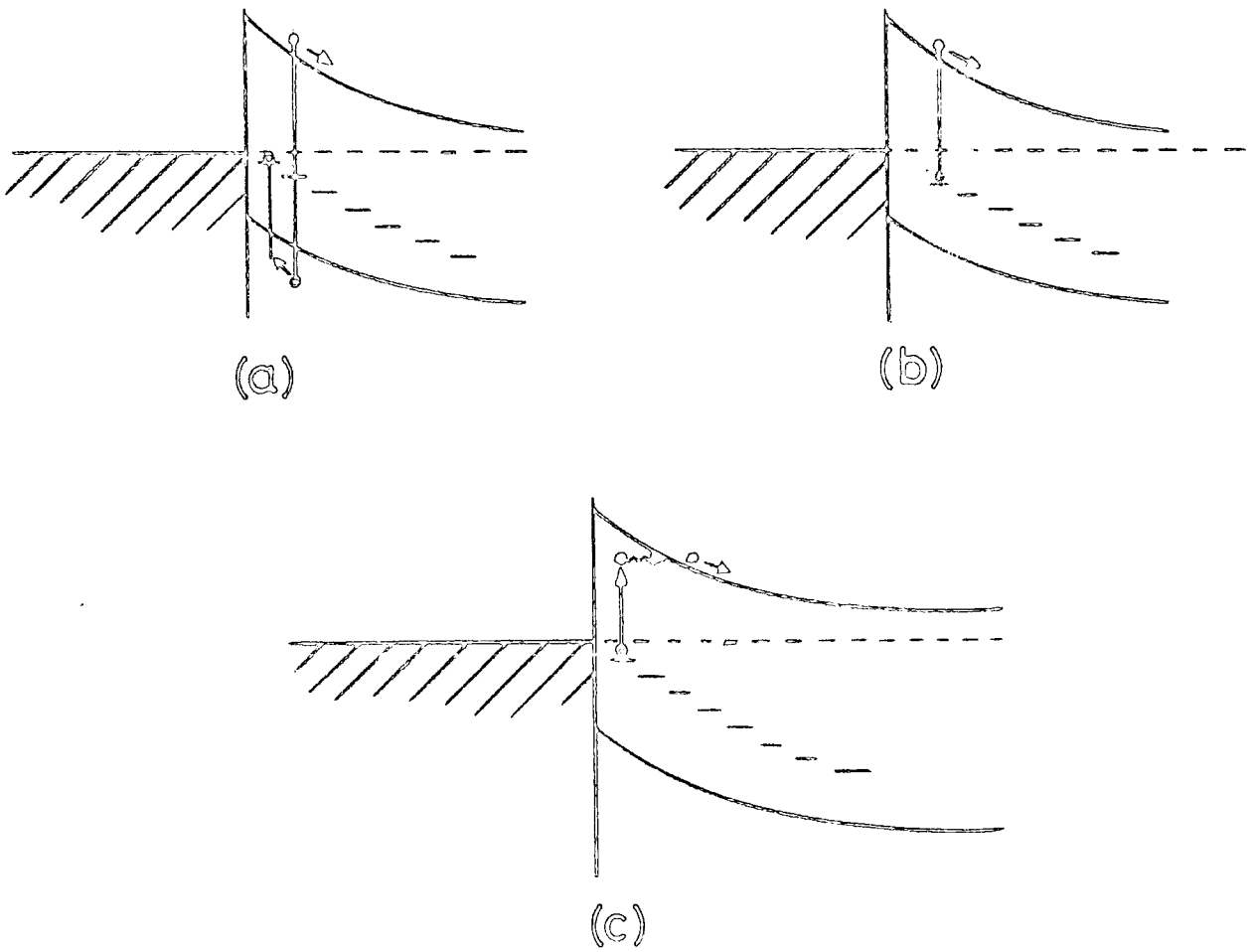



Figure 7.5 Electronic processes responsible for photocapacitance

(b) Excitation of photocapacitance by extrinsic radiation, $\lambda \sim 0.5 - 1.0$ μm. Light with these wavelengths can cause direct excitation out of a deep level leaving behind a trapped hole with the same result as (a).

(c) Excitation of photocapacitance by extrinsic radiation with $\lambda > 1$ μm. Light of this wavelength has insufficient energy to excite an electron from a filled deep level to the conduction band near the junction because of the barrier height at the surface. Excitation is however possible by the emission of an electron to a higher lying interface state followed by tunnelling into the conduction band.

(d) Quenching of photocapacitance by extrinsic radiation $\lambda \sim 0.8 - 1.5$ μm. Quenching occurs here in a similar way to that described for photoconduction. The sample is excited by a 'bias illumination' as in (a), and there must be both Class I and Class II centres in the CdS. With the intrinsic radiation alone, the Class II centres in the depletion region will be predominantly filled with holes, (sensitised condition). When infra-red radiation is absorbed by those centres, the holes will be excited to the valence band where they may be recaptured by the Class I centres. Since this lowers the electron lifetime, it has the effect of reducing the number of positively charged levels in the depletion region, thus reducing the photocapacitance.

Clearly the spectral response of photocapacitance should yield the same information from low resistivity samples as the photoconductance measurements do for high ρ materials. Such measurements will be described in Chapter 8.

### 7.4.2 I-V Measurements

In addition, the current-voltage characteristics of diodes were measured in the dark and under simulated A.M.1. conditions, see Figure 7.6.

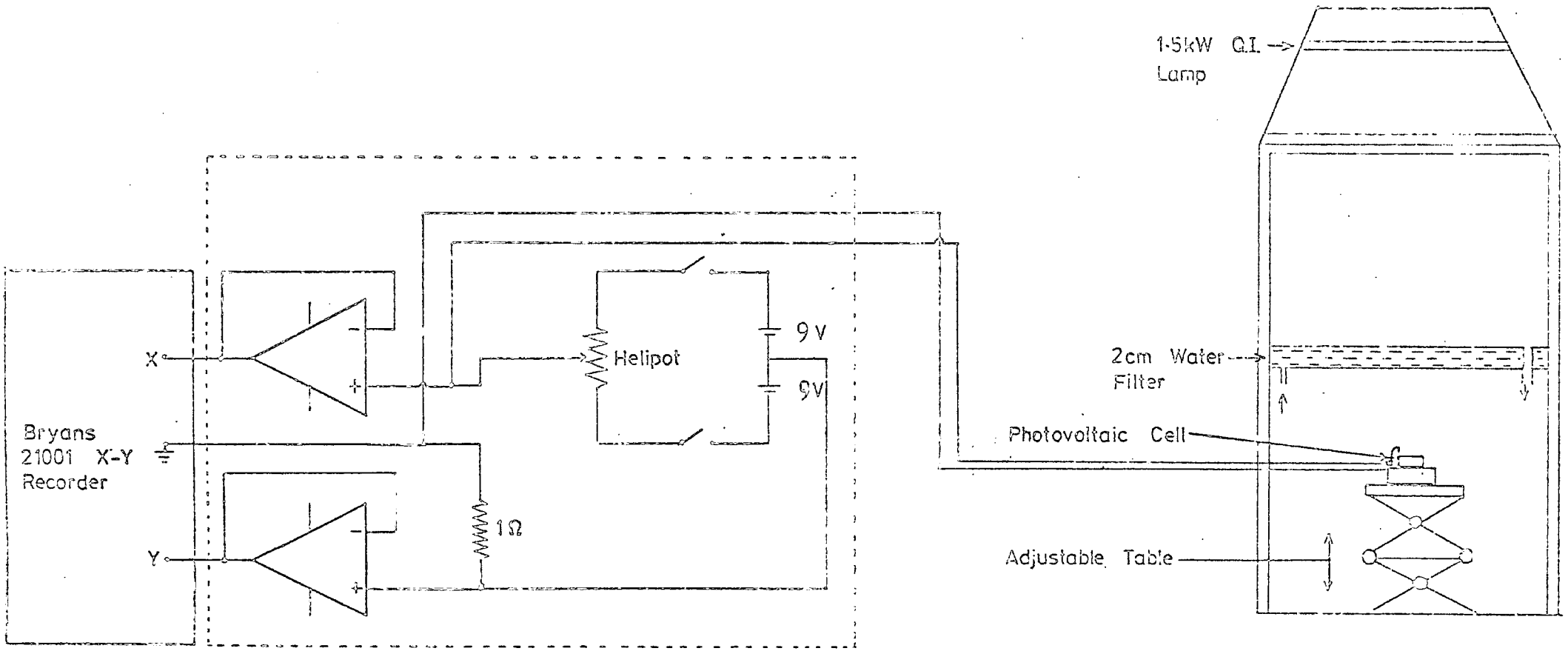



FIG. 7.6 CIRCUIT FOR SEMI-AUTOMATIC PLOTTING OF PHOTOVOLTAIC CELL I-V CHARACTERISTICS

The 'sunlight' was produced by filtering the light from a 1.5 kW quartz halogen lamp by passing it through 1 cm of water to reduce its infra-red content. The light was calibrated using the silicon P.I.N. diode mentioned earlier with two 1% neutral density filters mounted on the stage; the level being adjusted until A.M.1. illumination, 140 $mW/cm^2$ was obtained.

### 7.4.3 Photovoltage and Photocurrent

Other experiments undertaken involved the measurement of open circuit voltage (O.C.V.) and short circuit current (S.C.C.) as a function of wavelength, with $CdS/Cu_2S$ heterojunctions made under different conditions and subjected to different heat treatments. These measurements were made both with and without bias illumination corresponding to the CdS band gap, (i.e. $h\nu$ = 2.4 eV) in order to counteract the effect, if any, of infra-red quenching in this complex structure. The secondary illumination was incident parallel to the plane of the junction, that is, at right angles to the direction of the monochromatic light, which was also incident normal to the surface. The secondary source was a 60 W 240 V tungsten lamp filtered by an Oriel 5,200 Å band pass filter used in conjunction with an Oriel infra-red absorbing filter. The intensity of this illumination was adjusted so that the response of a cell was the same when it was illuminated with monochromatic light alone ( $\lambda$ = 5,200 Å) as with bias light alone.

The measurements of O.C.V. and S.C.C. were taken using a Honeywell 196 chart plotter with an input impedance of 10 MΩ on all ranges between 1 mV and 100 mV F.S.D. For O.C.V. the output of the cells was fed directly into the plotter. For S.C.C. the 1 mV voltage range was always used with a small parallel resistor inserted, the value of which was chosen so that a reasonable response was produced on the chart paper. A value of the order of 1 kΩ was normally used. While this means that the S.C.C. measured was not generally the true short circuit current, it does mean that if the

response differed from the O.C.V. response, it would be because the true S.C.C. and O.C.V. responses were dissimilar.

## 7.5 Model of the Photovoltaic Cell

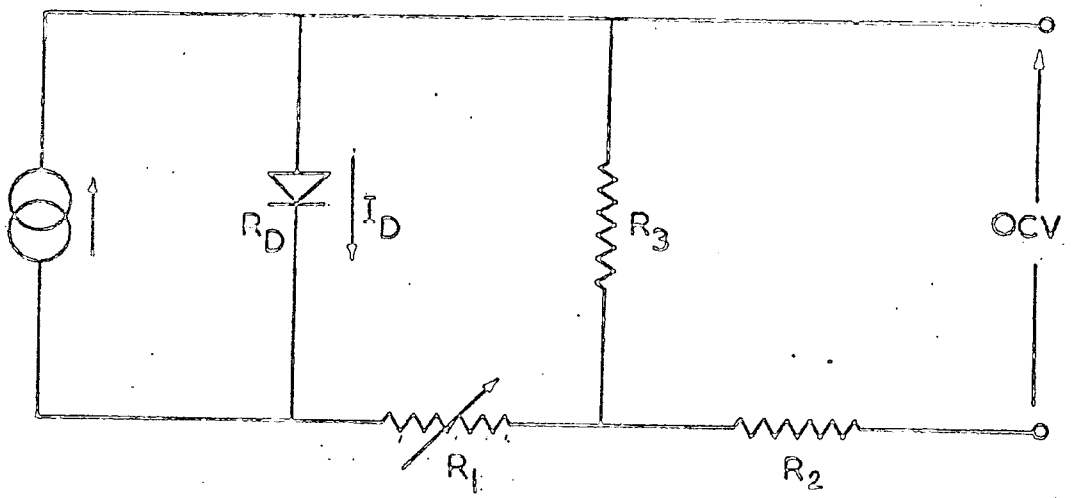
In the simplest analysis of a photovoltaic cell, the effect of illumination is simply the production of electron-hole pairs in the depletion region of the semiconductor. The carriers are separated by the built-in field of the diffusion potential, and if the cell is short-circuited, a current $I_L$ will flow. If, however, the device is open-circuit then a movement of charge will occur which will cause a movement in Fermi levels across the junction, apparently forward biasing the device so that the forward current cancels out the light induced reverse current. Put mathematically, the diode equation:

$$I = I_S (e^{qV/kT} - 1) \qquad (7.11)$$

becomes

$$I = I_S(e^{qV/kT} - 1) - I_L \qquad (7.12)$$

under illumination. This may be simply regarded as a shift of the I-V characteristic downwards by $I_L$. In a real device, however, there will be shunt paths across the junction, e.g. as a result of conduction along grain boundaries, and a bulk series resistance, due to the substrate. This gives an equivalent circuit for the cell, as shown in Figure 7.7. It is apparent that a shunt resistance will affect the measurement of O.C.V. to a larger extent than that of the S.C.C. and vice versa for the series resistance. Shiozawa et al (1969) demonstrate this with quantitative examples. Hence a comparison of the spectral response of O.C.V. and S.C.C. may provide some insight into the nature and properties of the shunt and series resistances in $Cu_2S$/CdS cells.




$I_D$ = Recombination Current.

$R_D$ = Diode effective resistance (voltage dependent).

$R_1$ = i-CdS resistance.

$R_2$ = Lumped series resistance.

$R_3$ = Shunt resistance.

FIG. 7.7 CdS SOLAR CELL EQUIVALENT CIRCUIT.

The results of the experiments described here and their significance in relation to the band structure model of the CdS/$Cu_2S$ heterojunction are described in the following chapter.

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## CHAPTER 7


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# CHAPTER 8

## EXPERIMENTAL RESULTS OF THE CdS/$Cu_2S$ HETEROJUNCTION

### 8.1 Introduction

In the previous two chapters, both the fabrication of $Cu_2S$/CdS heterojunction devices, and the measurement techniques have been fully described. In this chapter the experimental observations are reported and their implications are discussed in terms of the various proposed models of the heterojunction.

### 8.2 The Effect of Copper as a Dopant in CdS

Some of the crystal boules grown with a cadmium tail as previously described, were orange in colour, and of high resistivity, $\rho \sim 10^6$ Ω cm. Such crystals were highly photosensitive and were therefore thought to contain an impurity forming a compensating acceptor. The photoconductive spectrum of a 2 mm cube cut from one such boule is shown in Fig 8.1. Curves A and B illustrate the photoresponse with and without a "bias illumination" of CdS band gap light. Two infra-red quenching bands were observed with maxima at 0.92 μm and 1.39 μm. A comparison of these values with generally accepted values (0.9 and 1.4 μm) suggests that the impurity responsible for the photoconductive sensitisation was copper. This was confirmed analytically by atomic absorption spectroscopy (Russell and Woods, 1979). Cubes of this material were of too high a resistivity for the fabrication of either CdS/$Cu_2S$ heterojunctions or Schottky diodes, and therefore were heated in cadmium vapour at 600°C for three days. This reduced the resistivity by several orders of magnitude to $\rho \sim 10$ Ωcm. Two series of Schottky diodes were then prepared on this material in the normal manner, one set with gold as the barrier metal and the other with copper.

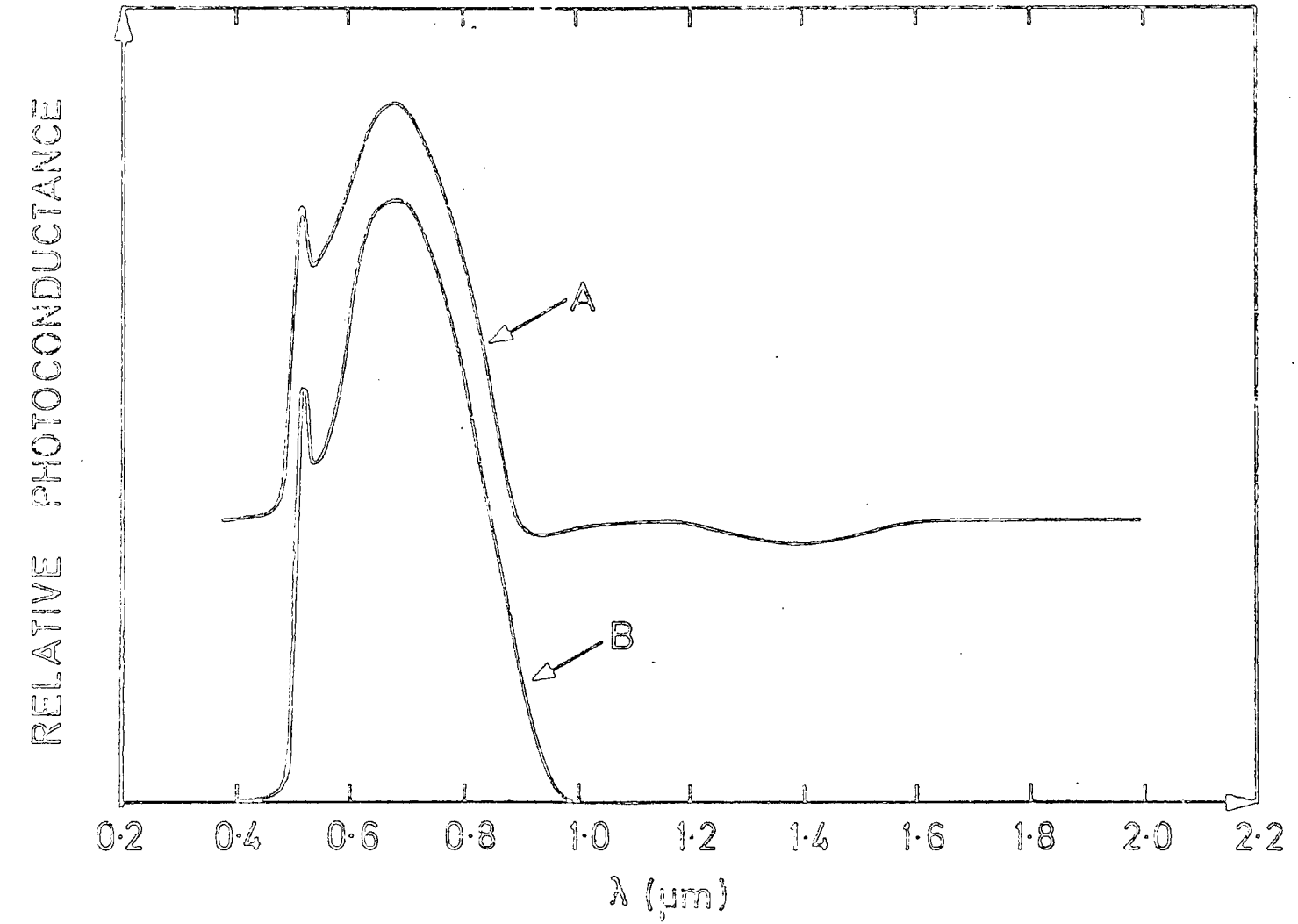


FIG. 8.1 PHOTOCONDUCTIVITY OF CdS : Cu
(A) with 0·52um bias light showing quenching peaks &
(B) alone

## 8.3 Photocapacitance Measurements

The photocapacitance of these samples, at zero bias, was measured and typical results are shown in Fig 8.2. The other spectra in this figure were obtained when a constant bias illumination was used. The close similarity of the two responses clearly shows that diffusion from the copper contact cannot be responsible for the infra-red quenching, and since the quenching maxima occur at the same energies as before, this demonstrates that the heat treatment in cadmium has not removed the copper acceptors. Schottky diodes, made with gold contacts, on the clear yellow, low resistivity (as grown) CdS showed negligible photocapacitance in comparison. Only in the region of the CdS absorption edge was there a slight response, due most probably to excitation of free carriers across the band gap, followed by trapping of holes in the depletion region.

Carter and Woods (1973) have demonstrated by comparing the infra-red quenching spectrum at 77° K with that at room temperature, and by using the technique of thermally stimulated currents, that the two maxima are associated with levels lying 0.2 eV and 1.1 eV above the valence band. The photocapacitance change at 0.9 eV and 1.1 eV is negative and consequently is attributed to a widening of the depletion region. This results from the decrease in the concentration of free carriers which quenching causes, by exciting holes out of Class II centres into Class I centres via the valence band. Irradiation with light with photon energy 1.3 eV should excite an electron from this 1.1 eV level to the conduction band, assuming that the level does not move significantly on being filled. This process is the opposite of quenching and will result in an increase in capacitance. A transition from a negative to a positive photocapacitance is indeed what was observed. The depth of the level below the conduction band can be calculated by applying Fowler's Theorem to the low energy threshold shown in Fig 8.2.

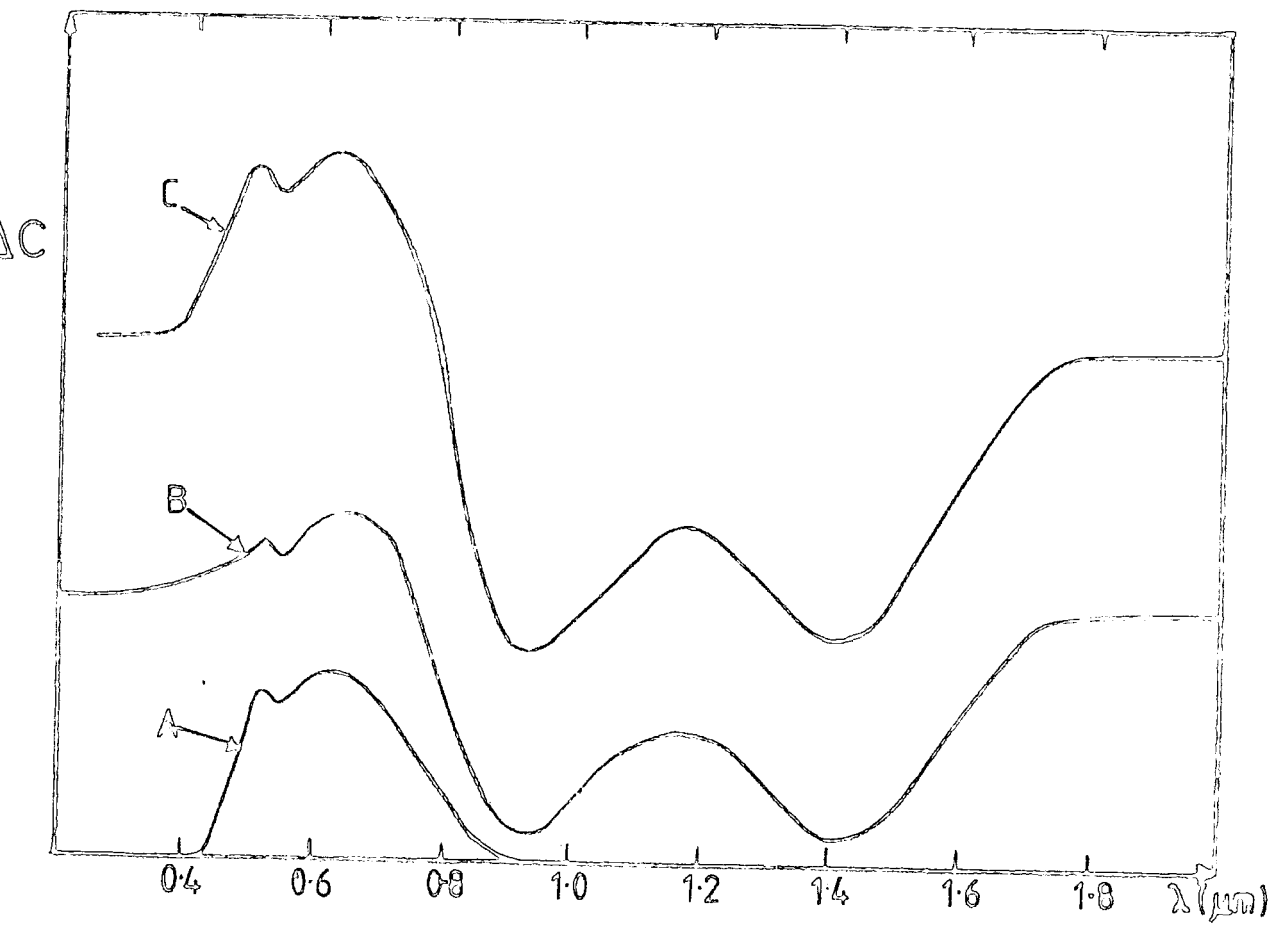


Figure 8.2 Photocapacitance of:
(A) Au/CdS:Cu & Cu/CdS:Cu
(B) Cu/CdS:Cu with bias light
(C) Au/CdS:Cu " " "

A graph of $(\Delta C)^{\frac{1}{2}}$ versus photon energy is shown in Fig 8.3 which yields a value of 1.25 eV for the displacement of the level from the conduction band, in good agreement with the quenching data.

8.4 O.C.V. Measurements

All the devices used in the following experiments, unless otherwise stated, were made from the low resistivity CdS which showed a negligible photocapacitance in Schottky diodes. First a good djurleite ($Cu_{1.96}S$) layer was plated on to a CdS die at 85°C and after checking its R.E.D. pattern, the spectral responses of its S.C.C. and O.C.V. were measured. These were found to be of identical shape and therefore the O.C.V. only is shown in Fig 8.4. The addition of a bias light produced a constant shift in the value of the O.C.V. but left the shape unaltered. For comparison, the O.C.V. of a good chalcocite, $Cu_{2.0}S$/CdS heterojunction is also shown in this figure. The curves have been normalised so that the maxima are of the same height ; however, in reality the djurleite response was less than that of the chalcocite at all wavelengths. Similarly to the spectral responses of the djurleite device, those for the chalcocite junction showed no difference between the O.C.V. and S.C.C., with or without bias illumination. Both curves in Fig 8.4 show the presence of three peaks, one at 0.92 μm, one at 0.68 μm, and the third at 0.5 μm. These curves closely resemble those of Caswell, Russell and Woods (1977), and it is generally accepted that they arise in the following manner. For the chalcocite sample the largest peak (at 0.92 μm) corresponds to absorption of light across the indirect band gap of $Cu_2S$, which has been established to be 1.2 eV (Marshall and Mitra (1965) ). The small peak at 0.68 μm corresponds to the stronger absorption of light in the chalcocite at the direct band gap of 1.8 eV, while that at 0.5 μm is caused by absorption of light within the CdS substrate . The djurleite device exhibits its

maximum response at 0.68 μm which corresponds to excitation across the band gap of djurleite at 1.8 eV. This is in agreement with Palz et al (1972) who demonstrated the shift in maximum response with the composition of $Cu_xS$ (i.e. they varied the x in $Cu_xS$, see Fig 8.5).

As stated in Chapter 7, none of the curves presented here has been corrected for variation of monochromator bandwidth or variation of light energy with wavelength. If this correction is made using the transmitted energy spectrum of lamp + monochromator, shown in Fig 7.1, Fig 8.6(a) transforms to Fig 8.6(b). These curves still show the features which have been described, however, the individual peaks are not so prominent. Consequently, since comparison of different spectral responses is of interest and not absolute values, all such graphs will be presented in the uncorrected form.

## 8.5 Photoconductive Effects

According to Caswell, Russell and Woods (1975) a photoresponse similar to that of an as-prepared $Cu_{1.96}S$/CdS device may be obtained by a different route, that is from a $Cu_2S$/CdS heterojunction after it has been subjected to a heat treatment in air. In Fig 8.7 curve (A) represents the O.C.V. of a chalcocite device as made, while (B) shows the effect of a two minute bake at 200°C in air. The close similarity between (B) and the djurleite response is immediately apparent, and it has been suggested by Massicot (1972) that this is because heating in air causes the diffusion of copper from the chalcocite at the interface to form a layer of djurleite. Others have suggested that copper diffuses to the free surface to form copper oxide or into the CdS, while the loss of copper produces djurleite. An alternative explanation is that the diffusion of copper into CdS during the heat treatment forms a photoconductive resistive layer (Clevite Model) and that the resultant photoresponse of the O.C.V. is the convolution of the two

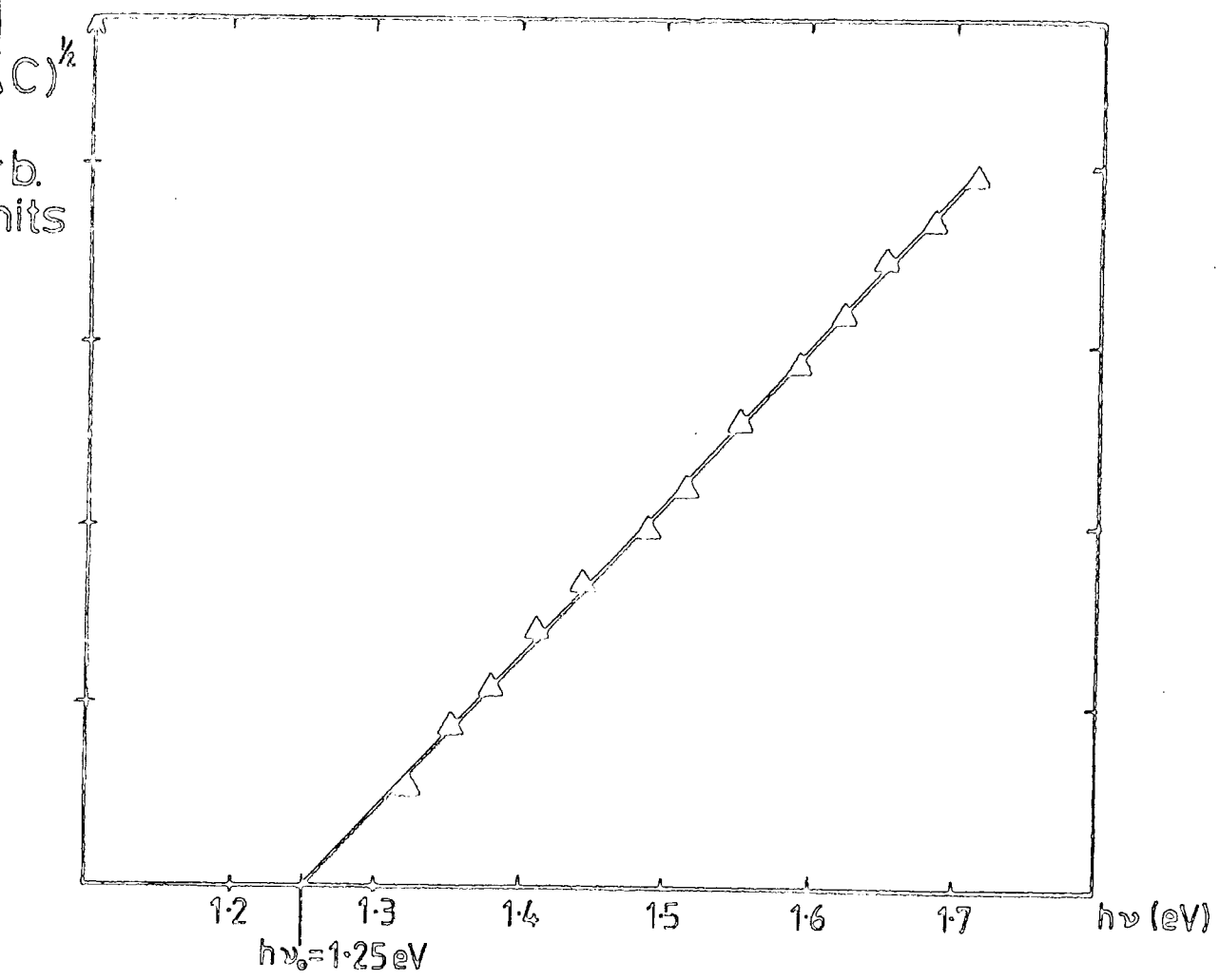


Figure 8.3 Fowler plot of $(\Delta C)^{1/2}$ versus Energy

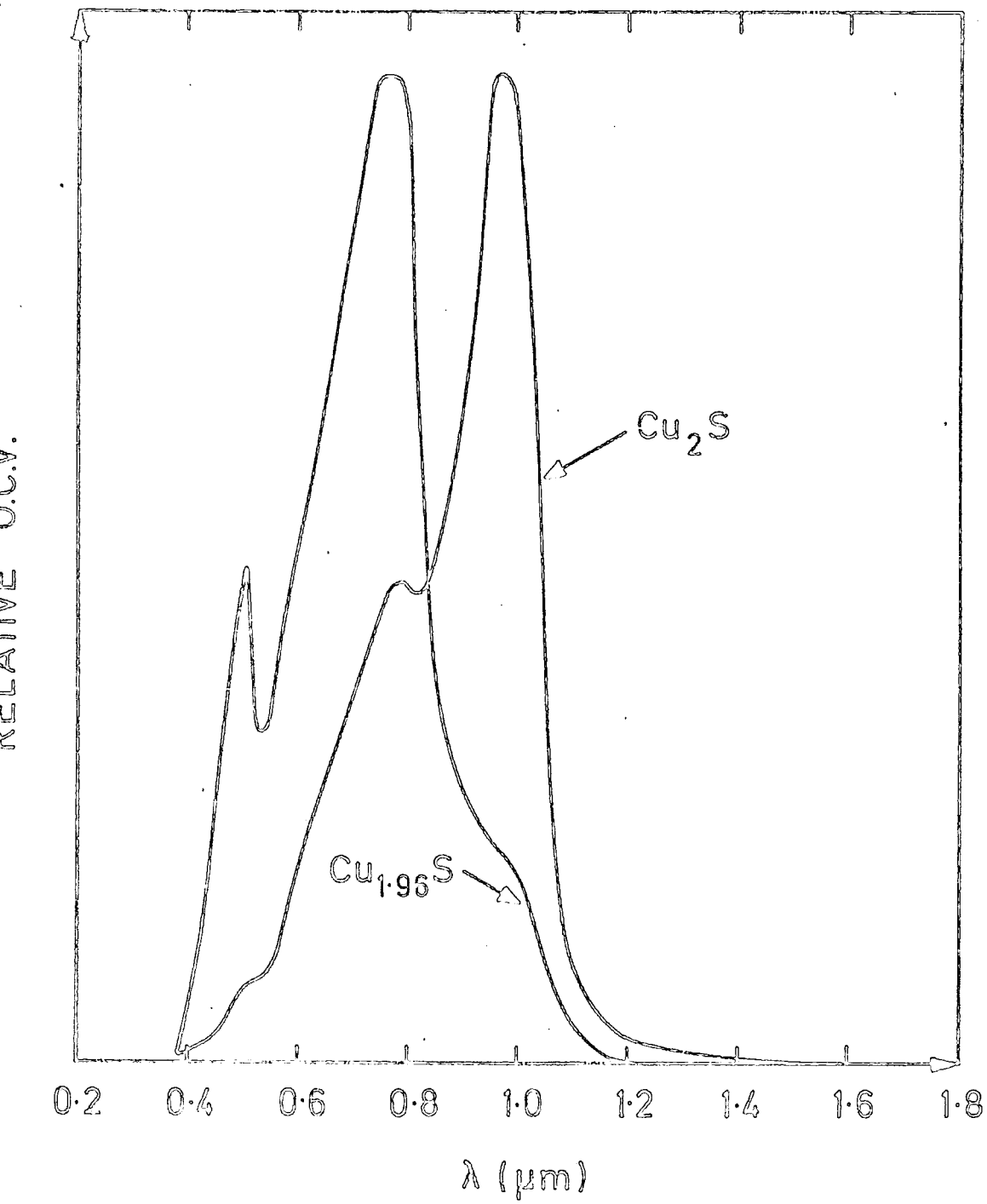


FIG. 8.4 RELATIVE PHOTORESPONSE OF CHALCOCITE AND DJURLEITE.

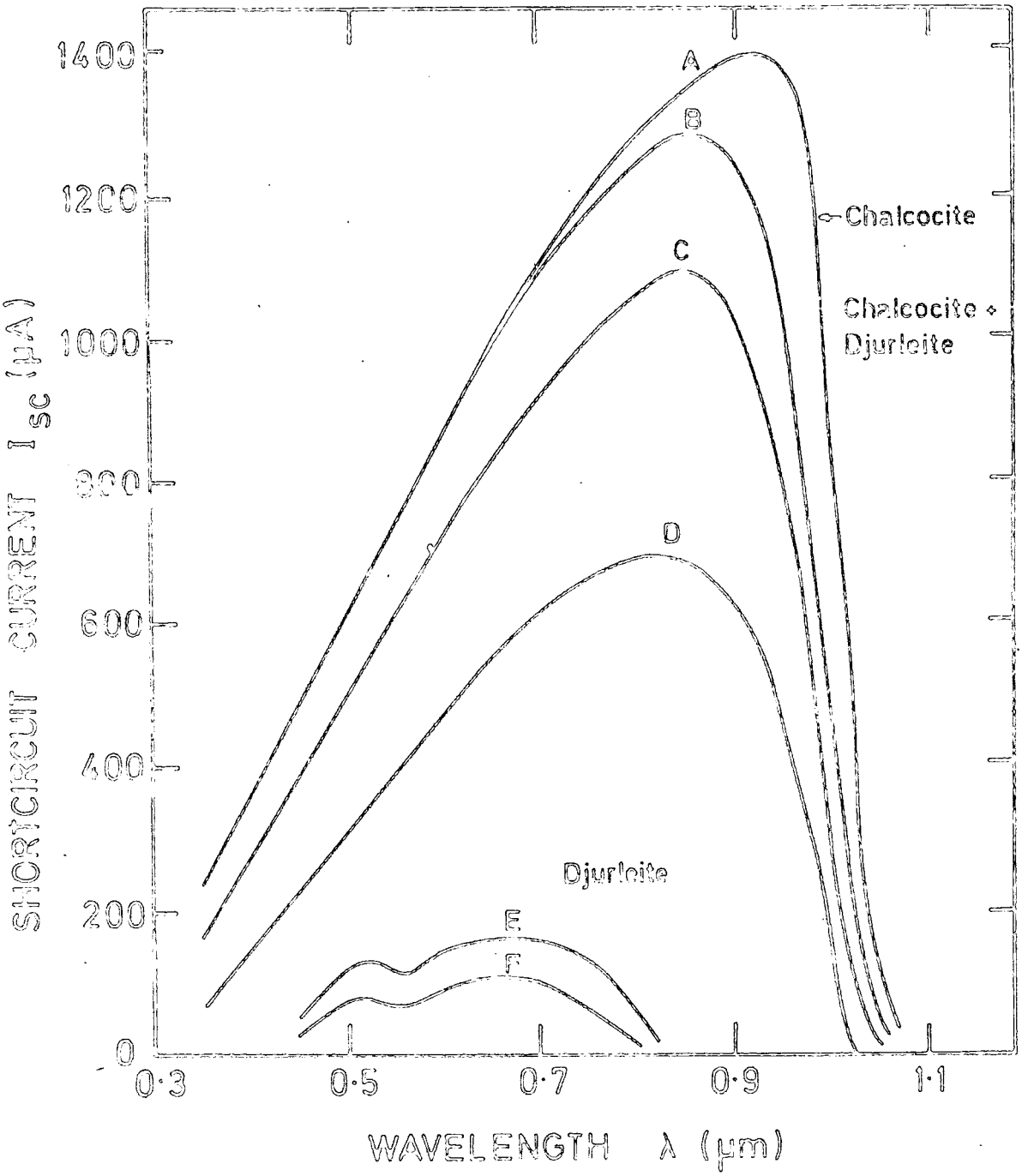


FIG. 8.5 SPECTRAL RESPONSES OF $CdS-Cu_xS$ AS A FUNCTION OF x

A x = 1·995 B x = 1·994 C x = 1·988

D x = 1·972 E x = 1·955 F x = 1·923

W. PALZ etal (1973)

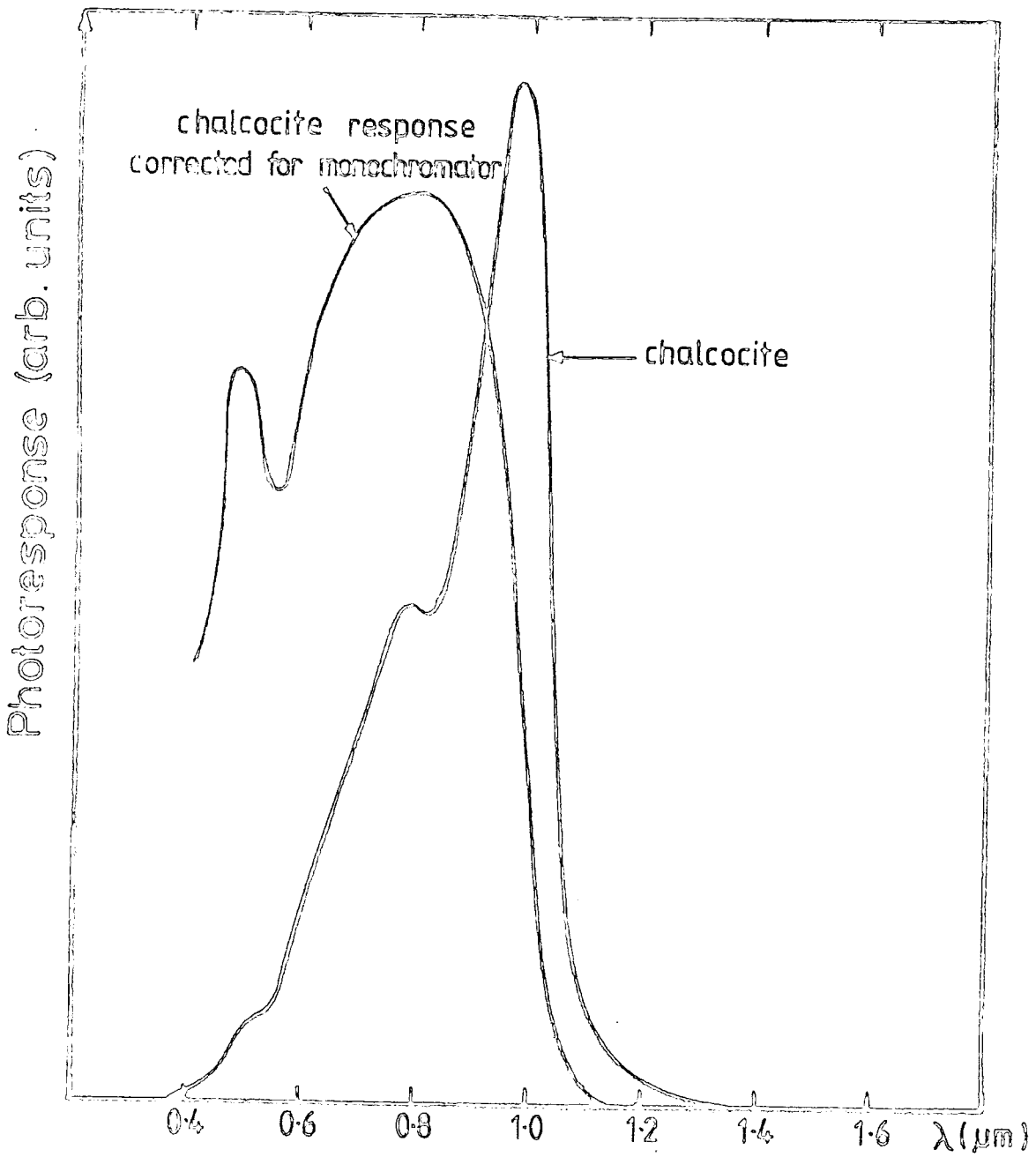


Figure 8.6 Uncorrected & corrected chalcocite responses

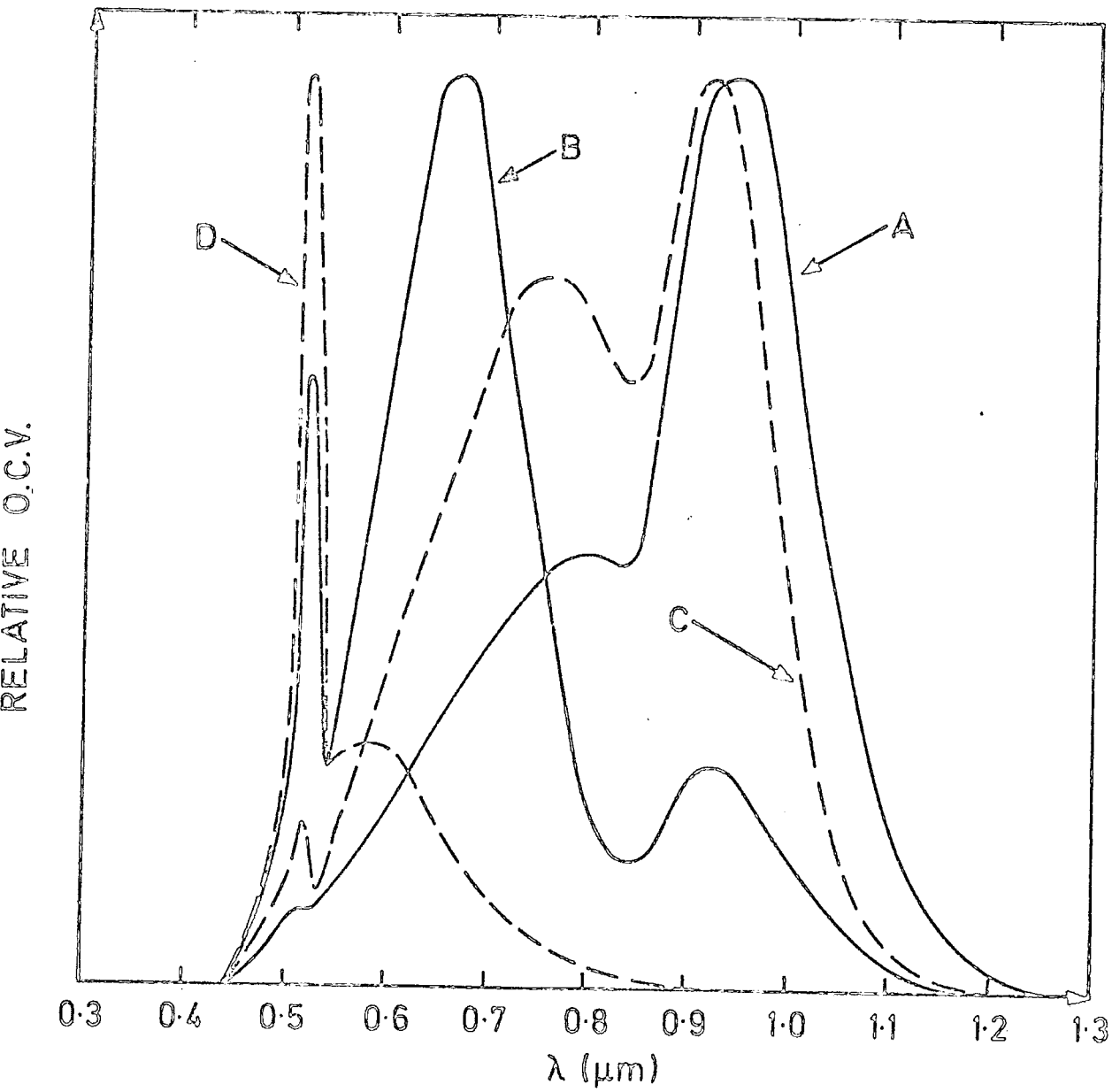


FIG. 8.7 OPEN CIRCUIT VOLTAGE FOR
(A) pure CdS heterojunction as made
(B) pure CdS heterojunction after bake
(C) Cu-doped CdS heterojunction as made
(D) Cu-doped CdS heterojunction after bake

spectra. Support for this belief is provided by the fact that the response time to radiation with wavelengths of about 0.70 μm was ∿10 secs., orders of magnitude larger than that to light with λ ∿0.50 μm. Photocapacitance measurements revealed that while the djurleite device showed negligible change in capacitance, the 'baked' heterojunction had a photoresponse similar to those for the Schottky diodes prepared on copper doped CdS, which are shown for comparison in Fig 8.2. While these observations do not exclude the possibility of the formation of djurleite at the interface, they do prove that copper diffuses into the CdS during the heat treatment in air.

In Fig 8.7 curves (C) and (D) show the O.C.V. of a heterojunction on copper doped CdS before and after baking in air. Comparison of these with (A) and (B) shows that the presence of the copper impurity depresses the long wavelength response.

## 8.6 I-V Measurements

Measurements of the current-voltage characteristics of all the samples made were carried out under illumination (A.M.1.) and in the dark. Not infrequently, a heterojunction measured immediately after fabrication would show "soft" characteristics (see Fig 8.8). This was ascribed to the presence of a low shunt resistance, i.e. a poor junction. For comparison, the I-V characteristics of a more normal heterojunction are also shown in Fig 8.8. After the administration of the standard 2 minute bake treatment, both sets of characteristics improved, i.e. the fill factor and O.C.V. increased (see Fig 8.8). However, the change in the poor device was the more dramatic, a very large increase in shunt resistance accompanied a four-fold enlargement of O.C.V. and similar increase in fill factor. In spite of this, it was generally found, in both I-V and spectral measurements that devices which had initially a good I-V characteristic remained superior to the

Figure 8.8 Typical $Cu_xS/CdS$ I/V Characteristics Before and After Heat Treatment

others even after heat treatment. Prolonged heating of samples gradually reduced the short circuit current while increasing the cross-over effect, that is the displacement of light and dark characteristics in forward bias. This is the result of a combination of a change in barrier height with an increase in bulk resistance.

## 8.7 Comparison of O.C.V. and S.C.C. Responses

Spectral response measurements of O.C.V. and S.C.C. of a normal chalcocite heterojunction cell with the addition of a bias light show no difference immediately after fabrication, however, after the usual two minute heat treatment, a significant distinction was observed between the O.C.V. and S.C.C. responses. This difference in response disappeared when the bias light was removed and it was therefore concluded that the bias played an active role. A typical pair of spectra areshown in Fig 8.9. These were obtained from a diode which produced a large photoresponse after fabrication and possessed a good chalcocite layer according to the R.E.D.pattern. The open circuit voltage shows the following features ; first two quenching bands, one at 1.35 μm, the other at 1.0 μm. There is also a small peak at 0.9 μm and a much larger one at 0.7 μm. At the band gap of CdS there is a small sharp spike immediately followed at shorter wavelength by a shallow minimum. The response of the short circuit current reveals the same two quenching bands at long wavelengths ; however at 0.9 μm there is merely a shoulder on the large broad peak which is centred on 0.67 μm. At 0.5 μm there is a single sharp maximum, which exceeds the height of the broad peak, and there is no sign of a minimum at slightly shorter wavelengths. If the bias illumination had been directed on to the front ($Cu_2S$ plated face) of the cell together with the light from the monochromator, then the response of O.C.V. and S.C.C. might have been expected to be similar, since most of the bias light would have been absorbed in the $Cu_2S$

causing little difference in the value of either shunt or series resistance. However, since the bias illumination fell on to the side of the junction, it would probably have been absorbed in the bulk of the CdS, and would particularly have changed the value of the series resistance in the equivalent circuit, on absorption by the photo-conducting CdS:Cu layer.

For completeness, a set of spectral responses of the O.C.V. and S.C.C. with bias illumination were measured, with the directions of the incident irradiation interchanged, i.e. with the green 0.52 μm illumination from the front and the monochromatic irradiation from the side. The resultant responses are shown in Fig 8.10. In the O.C.V. there was an enhancement at 1.35 μm instead of a quenching. The highest peak in the response was found at 0.9 μm, with a shoulder at about 0.65 μm. The response as the wavelength approached the band gap of CdS fell steeply to the background level. Quenching occurred in the S.C.C. at 1.35 μm and to a lesser extent at 1.0 μm. At shorter wavelengths a small peak was found at 0.85 μm, but the maximum response lay at about 0.70 μm. As before, the response decreased steeply to zero at 0.5 μm.

## 8.8 A Proposed Model

In order to explain these characteristics, a band structure model is required with (1) a barrier height and (2) a series resistance both of which vary as a function of the wavelength of illumination. The enhancement of S.C.C. with the corresponding quenching of O.C.V. near 0.5 μm in Fig 8.9, for instance, cannot be explained in terms of either of these mechanisms alone, but the results can be understood if both processes occur. The model to be proposed, combines many features of the models of Te Velde (1973), Deb & Saha (1977), Gill and Bube (1970) and the Clevite model (Shiozawa et al (1969)), details of which follow below.

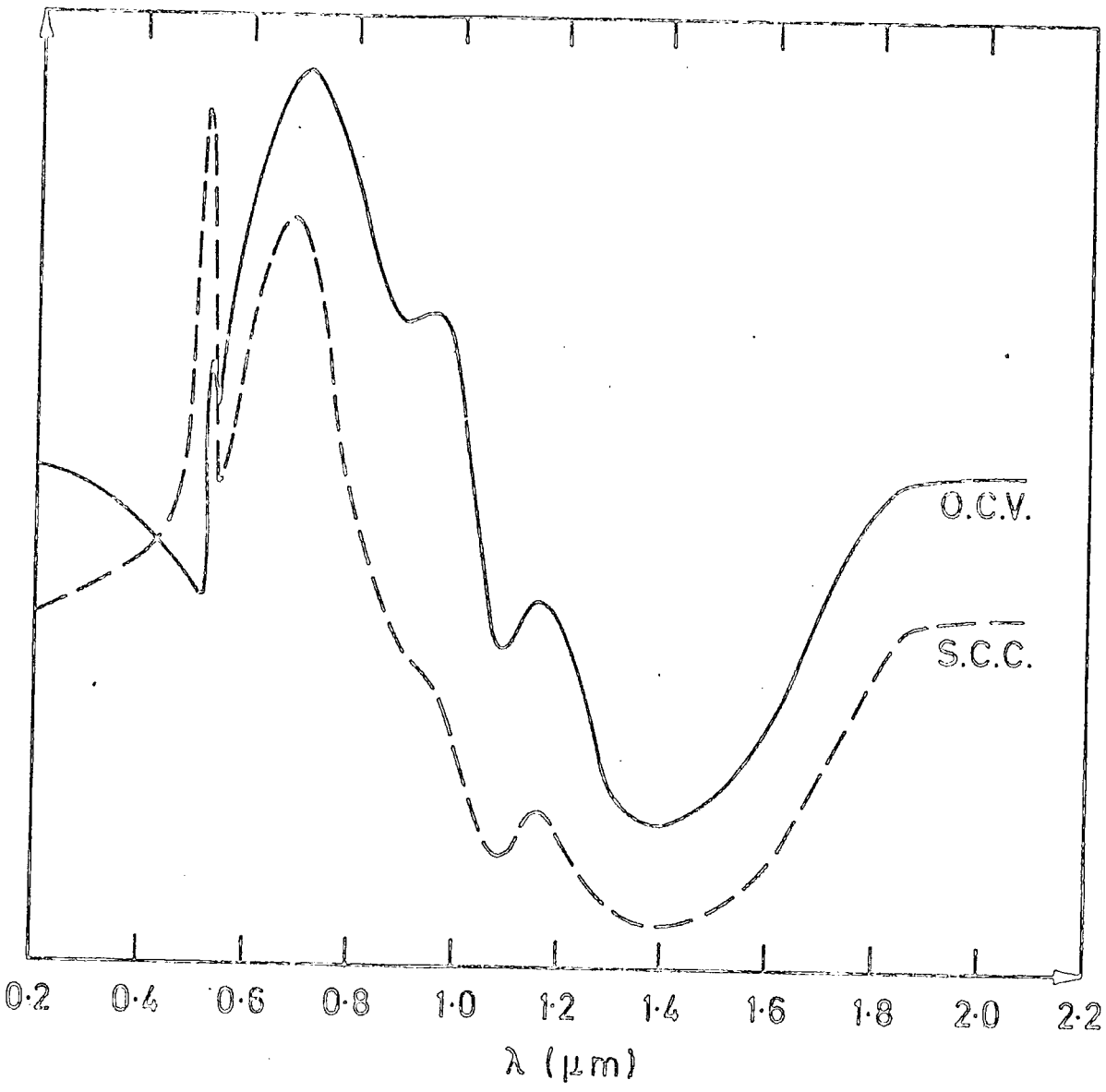


FIG. 8.9 COMPARISON OF O.C.V. AND S.C.C. FOR A HETEROJUNCTION ON PURE CdS AFTER HEAT TREATMENT WITH 0·52 μm BIAS LIGHT ILLUMINATING THE SIDE.

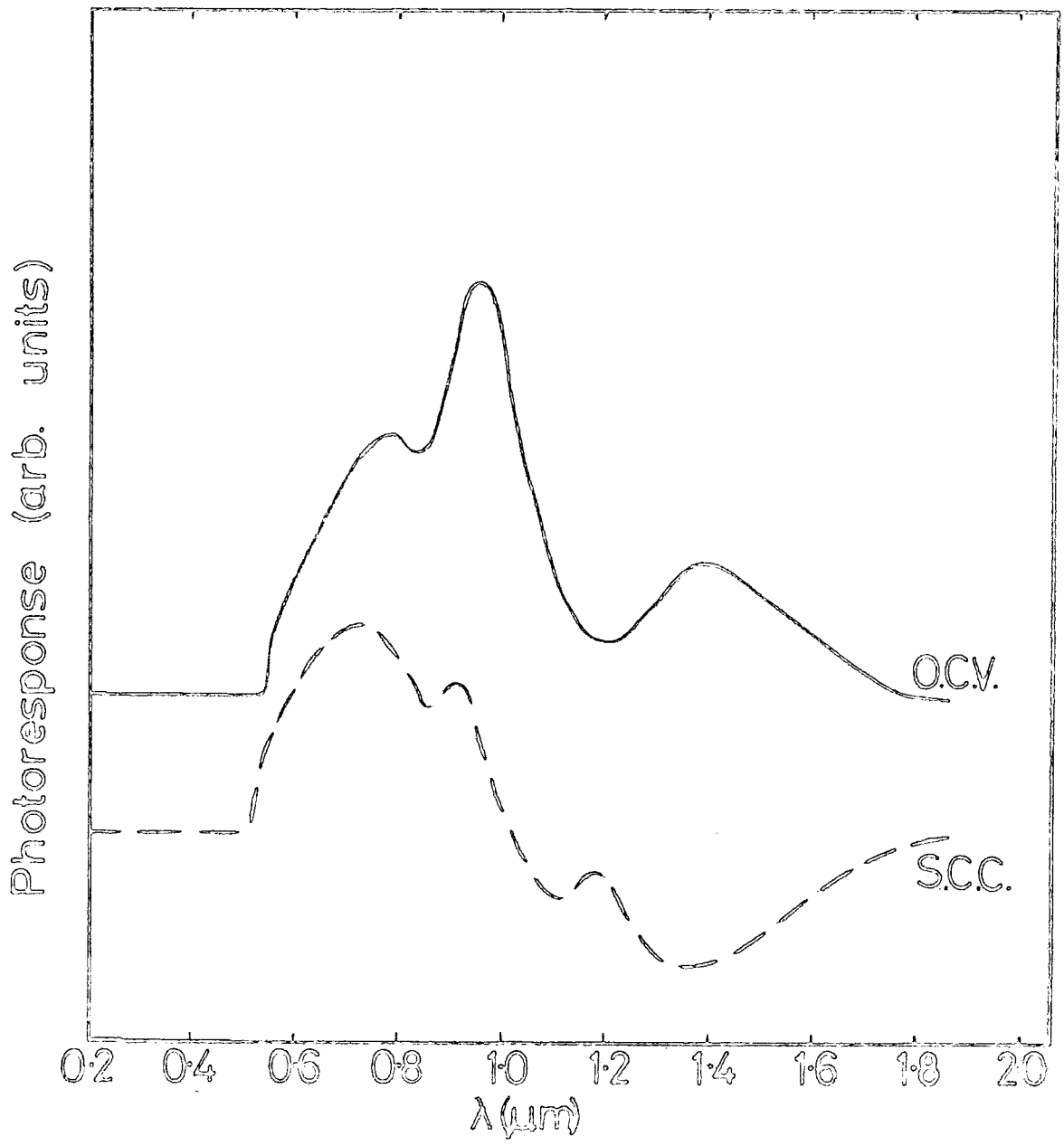


Figure 8.10 Comparison of O.C.V. and S.C.C. For a CdS Heterojunction After Heat Treatment with 0·52μm Bias Light Illuminating from the front

The actual form the potential energy diagram of the junction takes in each of these models is different, but each incorporates one if not both of the basic features (1) and (2) above. In the model of Gill and Rube, the spike in the conduction band is narrowed by illumination of the Cu-compensated CdS depletion region. This, effectively, lowers the barrier height while the photoconductive CdS:Cu forms a variable series resistance. The Clevite model has already been discussed in some detail, including the way in which a variation in both barrier height and series resistance is supposed to take place. Te Velde relies on oxygen traps at the $Cu_2S$/CdS interface to alter the CdS barrier height after heat treatment, and does not consider photoconductive effects at all. One objection to this model is that the vacuum level cannot always be continuous because the barrier height alters. To overcome this difficulty Deb and Saha (1977), postulate the existence of a thin insulating layer ($\sim$ 10 Å) between the $Cu_2S$ and CdS with a variable potential across it. Their analysis is similar to those given by Fonash (1976) and Viktorovitch and Kamarinos (1977) describing the influence of an interfacial layer on the efficiency of MIS solar cells, although with $Cu_2S$/CdS devices most light is absorbed in the semiconducting $Cu_2S$ layer. In the models of Te Velde and Deb and Saha, it was suggested that oxygen traps were responsible for the increase in barrier height after heat treatment. This is consistent with measurements of surface photovoltage on CdS by McCarthy and Yee (1973) and Kramer et al (1975). McCarthy and Yee demonstrate that chemisorbed oxygen states with a density of $\sim 3 \times 10^{11}/cm^2$ are responsible for the variation in barrier height on Au/CdS and Cu/CdS Schottky diodes with illumination. They propose the presence of a thin interfacial layer between the metal and semiconductor with the oxygen states at the semiconductor surface, in general agreement with Lepley et al (1976).

Rucher (1973) explains essentially similar observations in Cu-diffused Au/CdS junctions by a "humped" depletion region similar to that in the Clevite model. Such a band profile requires a sharp cross-over from a region with negative space charge to one with positive space charge. This implies that copper diffuses uniformly to a certain depth and then stops abruptly, which seems a rather remote possibility. If an exponential distribution, which would appear more likely, is used the maximum possible negative space charge density at the surface could not give rise to a "hump" in the depletion layer since Gauss' Law would then be violated. These remarks of course apply equally to the Clevite model, and agree with those of Pfisterer et al (1979).

Vasilevski et al (1976) suggest that a band model of the CdS/$Cu_2S$ junction which includes a hump is unnecessary to explain the observed cross-over of light and dark I-V characteristics following heat treatment. They propose a model where the electric field on the CdS side of the junction is controlled by the intensity and wavelength of the illumination. This in turn alters the ratio of the recombination and photocurrents which result from the absorption of electron hole pairs within the CdS. They point out, however, that their analysis is applicable only when the cross-over in the dark and light characteristics occurs in the exponential part of the characteristics which is generally not the case.

Moreover, their analysis would not be consistent with some of the quenching effects demonstrated in Figs 8.9 and 8.10, for example the quenching of O.C.V. together with enhancement of S.C.C. with band gap illumination from the front and bias from the side.

After due consideration of the various aspects of all these models, it is concluded that the experimental results reported in this thesis can best be explained in terms of a model(Fig 8.11) incorporating the following two features :

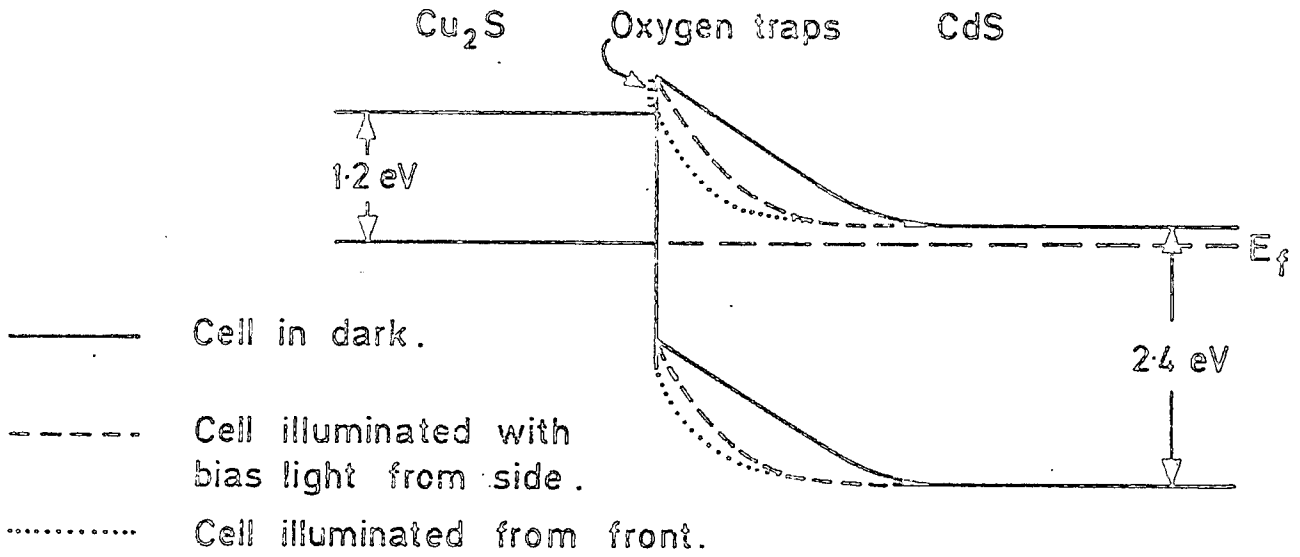


FIG. 8.11 THE ENERGY BAND STRUCTURE PROPOSED FOR THE BAKED $Cu_2S$ / CdS HETEROJUNCTION ON PURE SINGLE CRYSTAL MATERIAL.

(a) The formation of oxygen traps at the $Cu_2S$-CdS interface after baking in air at 200°C for 2 minutes.

(b) The existence of a Cu-compensated photo-conductive layer of CdS following the heat treatment within the depletion layer of the CdS.

8.9 Explanation of Results

Without illumination the band structure is as shown, Fig 8.11, (full line) ; the high resistance CdS:Cu layer makes the depletion layer rathe wide. With light of 0.52 μm wavelength incident from the front, (1) the number of carriers in the conduction band of the CdS:Cu is increased by intrinsic excitation and (2) oxygen traps are emptied lowering the barrier height causing the bands to bend to the position shown by the dotted line (Fig 8.11). With band gap illumination from the side similar band bending takes place except that relatively less absorption takes place at the junction so that the barrier height is essentially unchanged as shown by the dashed line. Because of the junction field, electron-hole pairs will be separated creating a photocurrent or photo-voltage. With the addition to this situation of infra-red radiation with $\lambda$ = 1.35 μm (see Fig 8.9) incident on the front of the cell, the photoconductivity is quenched and the energy bands return towards the "dark condition". The flow of photo-induced carriers from the depletion region is reduced, this lowers the photocurrent, or if the measurement is made under O.C.V. conditions, the movement of a reduced quantity of charge will create a lower potential. The next quenching peak at shorter wavelengths can be explained similarly except that it occurs at almost the same wavelength as the absorption in $Cu_2S$ at 0.92 μm, the two mechanisms therefore compete. The light absorbed in the $Cu_2S$ produces electrons which diffuse to the junction where some will tunnel through the conduction band spike producing a photocurrent. The width

of this spike is modulated by the radiation which is absorbed by the CdS:Cu, and reduces the photocurrent (and also the photovoltage as the diffusion potential is unchanged). Which of the two is reduced more is determined by the size of the recombination current, the series resistance of the CdS:Cu and the shunt resistance of the junction. In our device it is the S.C.C.

The broad response with its maximum at about 0.7 μm occurs in both S.C.C. and O.C.V. and can be explained in the following way : most of the monochromatic light is absorbed in the $Cu_2S$ to produce free electrons in the conduction band. The remainder is absorbed in the CdS:Cu increasing its photoconductivity, and emptying some of the oxygen traps at the interface, which lowers the spike slightly. A large photocurrent then flows and this can therefore produce a large O.C.V. At the band gap of CdS, the light which is not absorbed in the $Cu_2S$ layer, is strongly absorbed by the CdS, and consequently is absorbed near the junction. This reduces the spike and may even produce a notch at the junction. This will certainly increase the short circuit current, but, as the diffusion potential has been reduced, will not increase the O.C.V. by such an extent, and indeed may even reduce it as is the case here.

The model can also explain the responses observed when the sources of illumination were interchanged. With reference to Fig 8.11, as previously mentioned, irradiation with constant bias light on the front of the cell will reduce the conduction band spike shown by the dotted line. Illumination from the side with 1.35 μm light, decreases the conductivity in the photoconductive region lowering the short circuit current, but increasing the diffusion potential, that between the CdS:Cu and the CdS now dominating. This means that the O.C.V. may actually increase as observed in Fig 8.10. The same occurs for the next infra-red quenching peak at 0.9 μm, except that superimposed on it is the

production of a sizeable photocurrent by absorption of the light in the $Cu_2S$. This increases both responses. The responses at 0.7 μm are self-explanatory, while when the wavelength is reduced still further, the photoresponse decreases sharply to zero at the band gap of CdS. This is because of the very strong absorption of the light with the result that little will reach the junction.

8.10 Discussion

Because of the large number of unknown parameters and variables, it is difficult to propose a model which fits the experimental observations to the exclusion of all others. Indeed the graphs presented in Figs 8.9 and 8.10 are the responses of only one device. Other devices measured showed similar spectra although quenching and enhancement occurred to different extents. The Clevite model will fit the observations qualitatively with assumptions about the extent of band bending etc., but the space charge distribution required seems rather improbable. The model shown in Fig 8.11, like that of Te Velde (1973) does not contain an interfacial layer between the CdS and the $Cu_2S$, although the presence of such a layer in a heterojunction with a lattice mismatch of some 4% in one direction, is thought to be quite possible. Boer (1978) allows for a layer of this type in his band model. Accepting this variant to the proposed model, leads to a band structure which resembles the Clevite model, if the region from the junction to the top of the hump is equated to the interfacial layer. In thickness, however, these two regions are by no means equivalent, the thickness in the Clevite scheme being $\sim$ 0.5 μm, while in the other only $\sim$ 10 Å. This might possibly be resolved by recalling that the Clevite model was developed for polycrystalline films whereas the structure proposed here applies to single crystals. A general broadening would be expected in the polycrystalline situation owing to grain boundaries and defects at

the junction.

## 8.11 Final Considerations

The discussion underlines the difficulty in distinguishing between models when the experimental data is essentially of a qualitative nature because of the large number of unknown parameters in the system, which is a consequence of the breadth of composition of the $CdS/Cu_2S$ heterojunction. Thus, while certain of the many models proposed for the $CdS/Cu_2S$ heterojunction may be quickly discounted because they cannot even qualitatively fit all the experimental data, there remain, however, certain different hypotheses about the band structure which cannot be discarded on this basis alone. In this chapter, the results of experiments have been presented which support a modified model of the $CdS/Cu_2S$ heterojunction; however, it has not been possible to prove the Clevite model inapplicable.

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# CHAPTER 9

# SCANNING ELECTRON MICROSCOPE STUDIES OF HETEROJUNCTIONS

## 9.1 Introduction

To supplement what might be described as the macroscopic studies of the CdS/$Cu_2S$ heterojunction discussed in the preceding chapter, microscopic observations were also undertaken. This involved an examination of some 20 devices using the scanning electron microscope. The modes of operation employed were cathodoluminescence (C.L), secondary emission, absorbed current, and electron beam induced current (EBIC) ; all of which have already been discussed in Chapter 5. With the assumption that the effect of an electron beam on a CdS/$Cu_2S$ heterojunction is of similar nature to that of a light beam, the surface features of a cell were examined and correlated with the electrovoltaic properties revealed by the EBIC mode. Degraded cells were also examined for comparison and suggestions for mechanisms of degradation discussed.

## 9.2 Experimental Observations

To reveal how the various regions of the junction appear in different modes, Fig 9.1(a),(b) and (c) shows the absorbed current image, the EBIC signal and the cathodoluminescence respectively, of a cleaved diode looking parallel to the junction plane. It should be noted that this device was fabricated by dipping in the copper plating solution for a long period in order to produce a very much thicker copper sulphide layer than that normally produced (< 1 μm) in order to aid identification. The diode had also received the customary heat treatment as its low resistance prior to this had made EBIC measurements impossible. All diodes studied in the S.E.M. received this bake. The absorbed current

image resembles the secondary emission signal as described in Chapter 5, except that there is less shadowing. The whole area of the device in Fig 9.1(a), looks similar, with the $Cu_2S$ (top layer) appearing slightly cracked. The EBIC signal, taken with zero bias shows the actual electrical junction very clearly ; it is the region of high internal field where electrons and holes are separated to produce a current in the external circuit. Comparison of Fig 9.1 (a) and (b) reveals that the junction is, in fact, between the cracks and uncracked areas in Fig 9.1(a). Fig 9.1(c) lends support to this ; the CdS appears white while the $Cu_2S$ is black.

Fig 9.2 shows part of the $Cu_2S$ layer of a cell fabricated in the normal manner, viewed perpendicular to the junction plane. This secondary electron micrograph was taken with an accelerating potential of 15 kV, and shows the etch features characteristic of the sulphur face of CdS. The same area viewed in the EBIC mode is shown in Fig 9.3 with a reverse bias of a few hundred millivolts. It is apparent that the areas etched deepest, the "valleys", appear dark, together with the highest etch features, the "summits", while the sides of the conical hillocks appear lighter. This implies that the number of separated electron-hole pairs produced by the incident electron beam is greatest on the sides of the hillocks. Figure 9.4 is of the EBIC signal with a small forward bias, which shows an almost complete reversal of contrast over the whole surface area. This reversal of contrast does not occur at zero bias, but with a forward bias of $\sim$ 50 mV. In an attempt to gain further information about these different regions of the surface, the scanning electron beam was switched off, and the electron beam positioned manually. Current-voltage characteristics were then measured with the beam incident on the three different regions, i.e. summit, valley and sides of hillocks and for comparison, with the electron beam off.

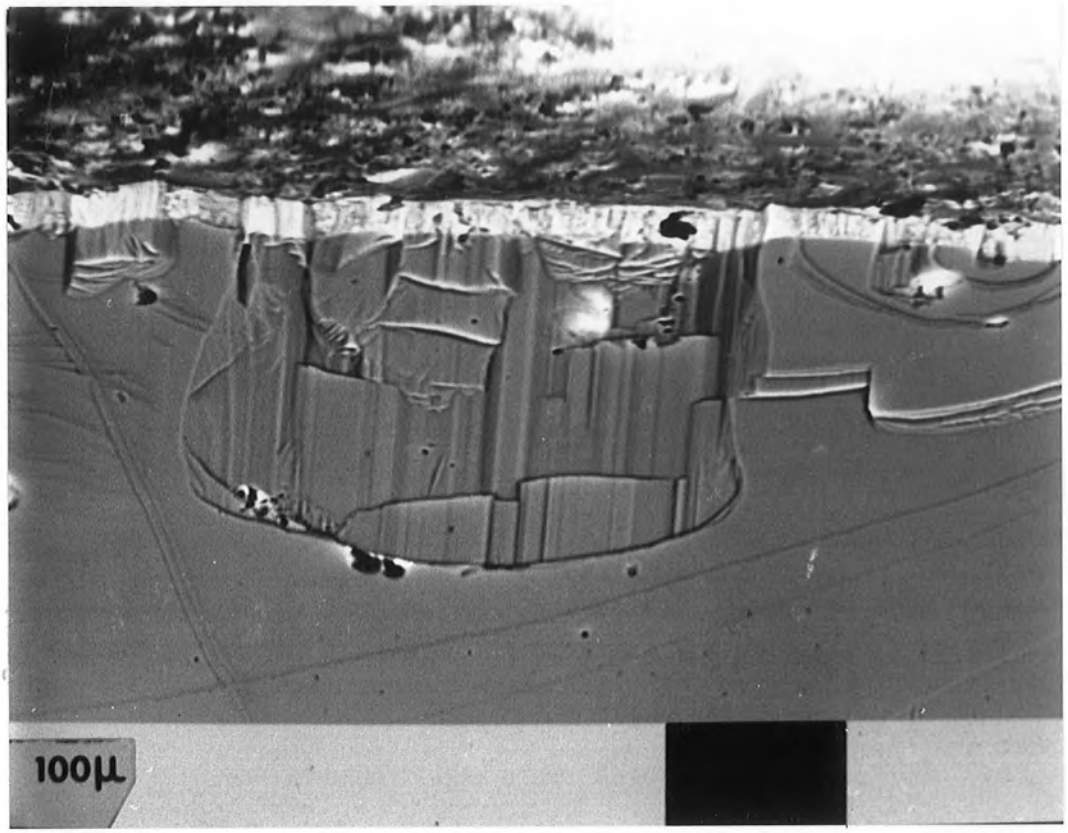
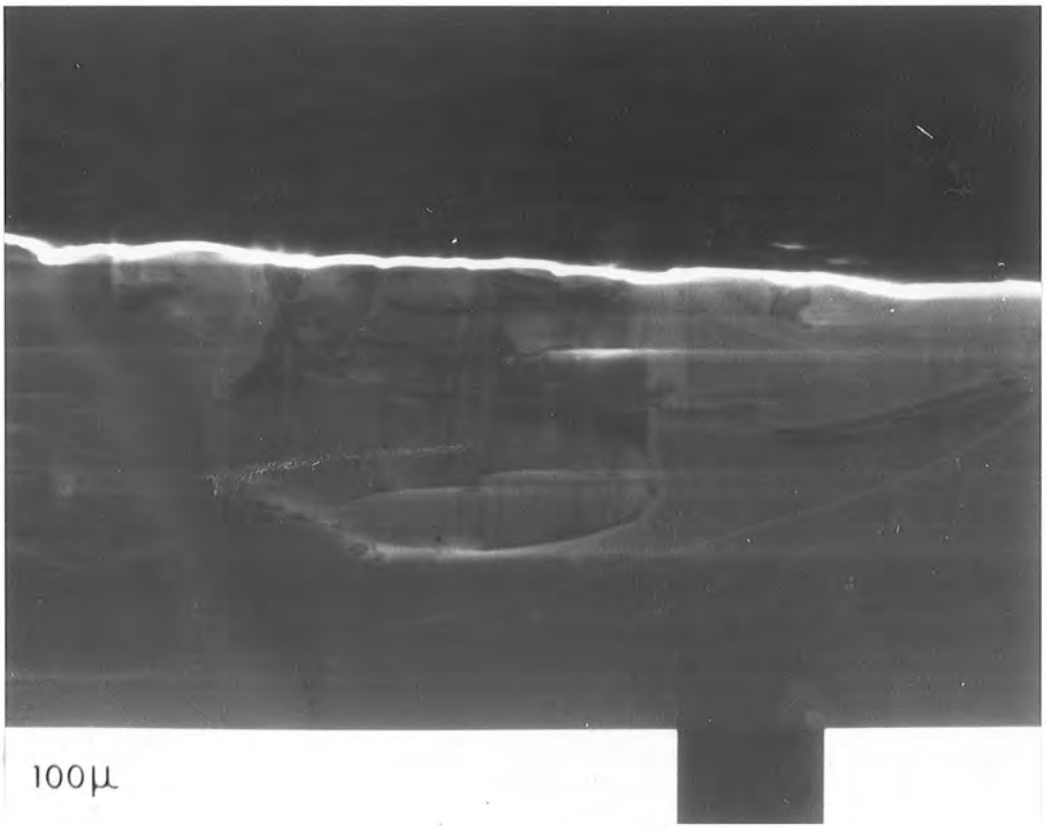



Figure 9.1 (a): Absorbed current image of a cleaved heterojunction diode.



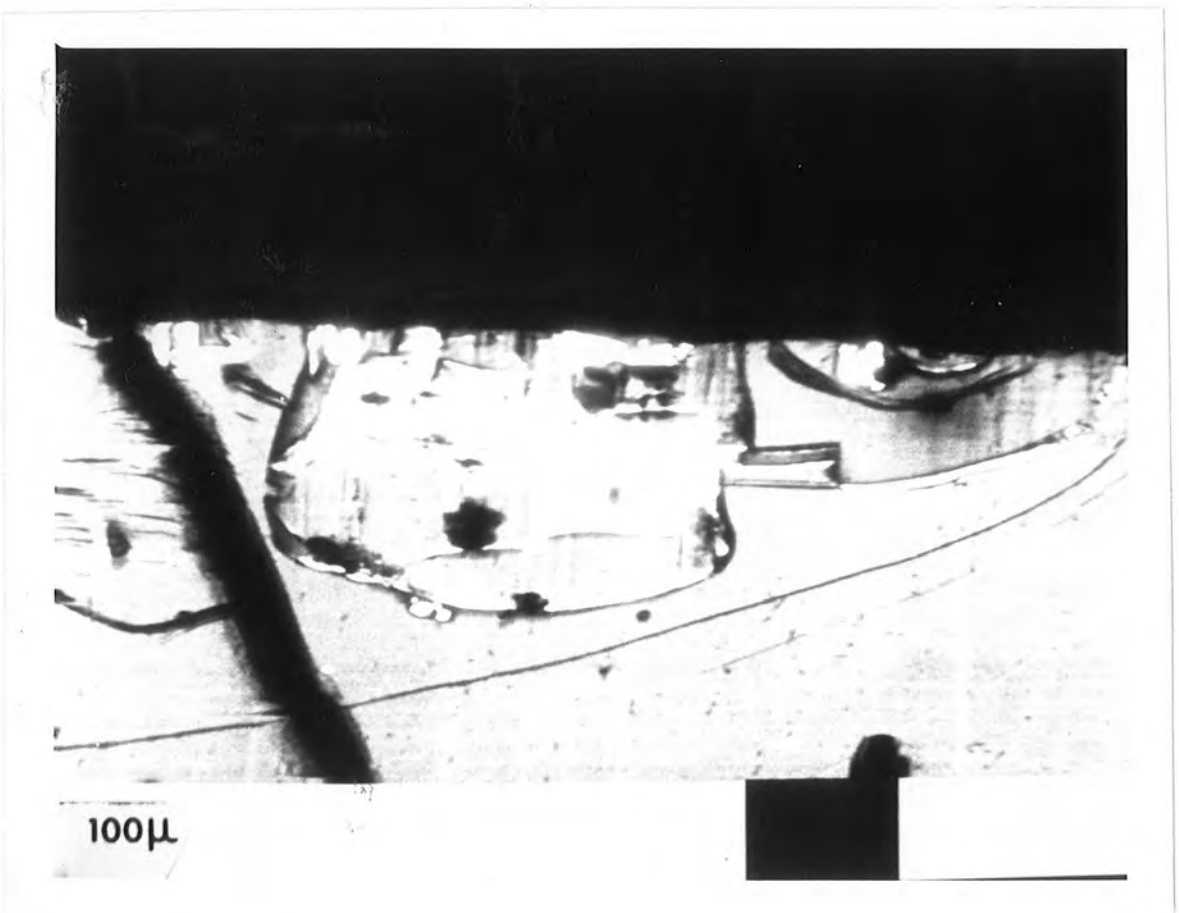



Figure 9.1 (c): Cathodoluminescence of the device in Fig. 9.1(a).

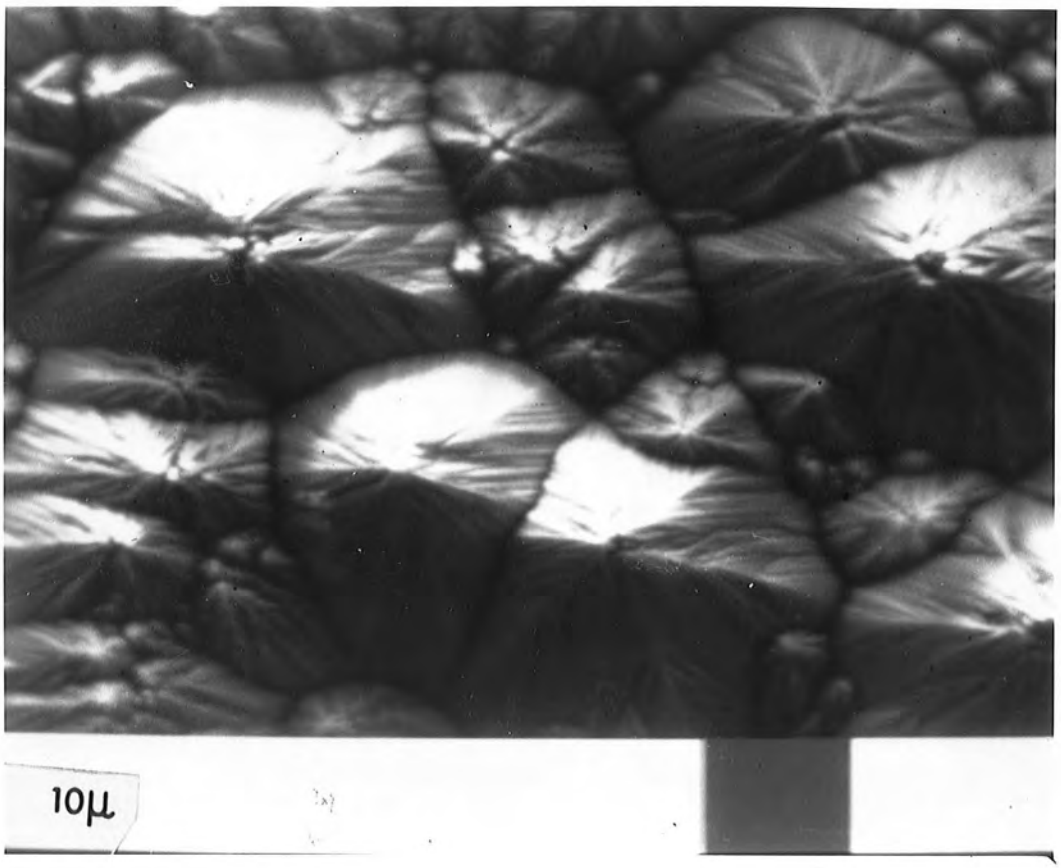



Figure 9.2: Secondary emission micrograph of $Cu_2S$/CdS heterojunction.

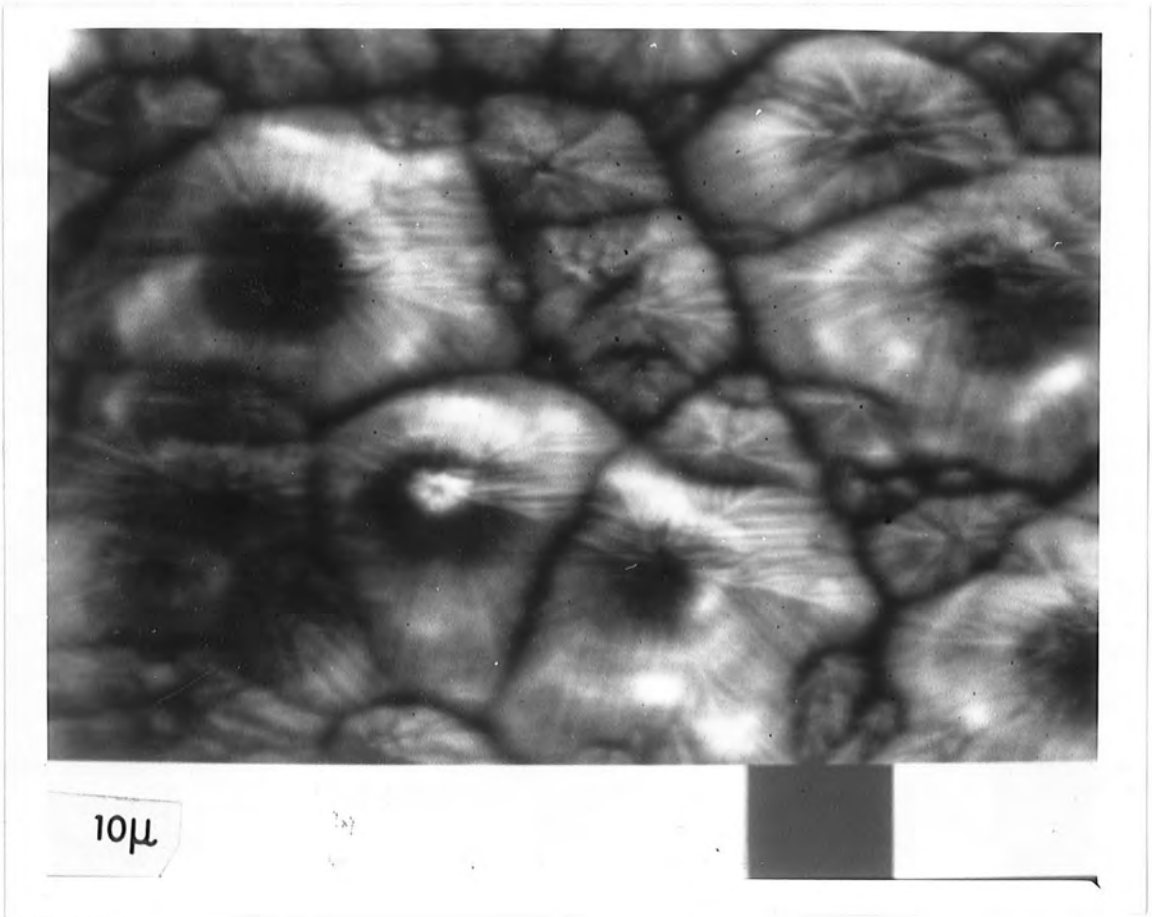



Figure 9.3 : E.B.I.C. of Fig. 9.2 ( ∿ 300 mV reverse bias)

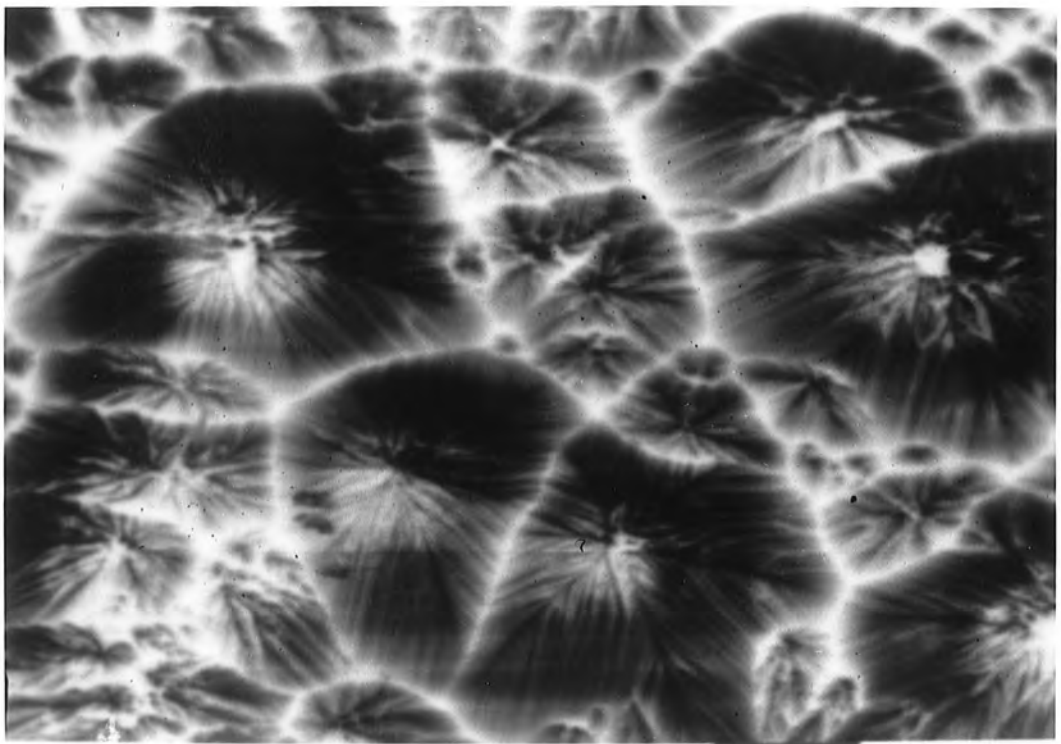



Figure 9.4 : E.B.I.C. of Fig. 9.2 ( ∿ 200 mV forward bias)

These are plotted in Fig 9.5 ; the characteristics in the valley and summit were so similar that just one of these is plotted. The simplest explanation of these characteristics is that the sides of the hillocks produce an electrovoltaic effect while the contribution of the tops and bases is smaller. In addition since these three curves cross over in forward bias, the implication is that the electron beam lowers the barrier height of the junction (see Chapter 5), to a small extent on the sides, and to a lesser extent on the tops and valleys. Fig 9.6 shows another sample in the EBIC mode where another type of feature is present, namely a number of flat-topped hillocks (e.g. the large black area). These were noticed occasionally on the surfaces of devices, but never formed more than about 1% of the surface. Why there should be regions which have not etched to form the usual type of surface is not known but the electrical properties of these flat regions appear to resemble those of ordinary hilltops. Studies of the cathodoluminescence from these surfaces revealed bright areas corresponding to the flat tops ; the signal elsewhere producing a generally uniform dark image. From the earlier observations, it appears that there is either a very thin layer of $Cu_2S$ or none at all present on these flat areas.

## 9.3 Discussion

### 9.3.1 Surface Topography

The EBIC and cathodoluminescence measurements show how different surface features react electrically to an incident electron beam, and from this evidence allow explanations of the behaviour to be suggested. Four different areas of a surface will be considered, (a) sides, (b) tops, (c) valleys of hillocks and (d) flat-topped hillocks.

It is envisaged that the thickness of copper sulphide varies over these areas as follows : on the flat-topped hillocks, there appears to be little or no copper sulphide ; on the summits where diffusion of copper can occur most easily, the layer will be thickest. By this

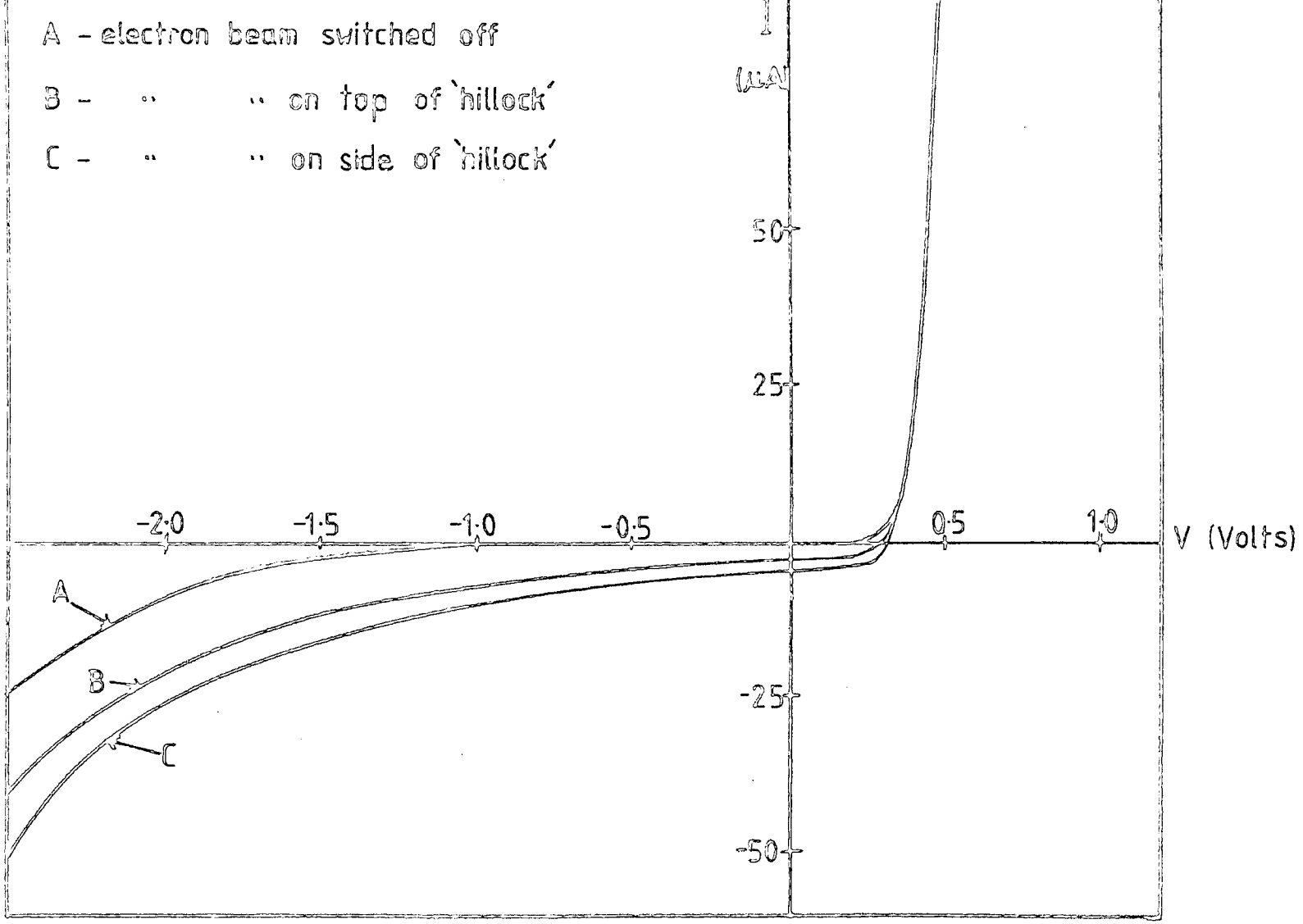



Figure 9.5 Current-Voltage characteristics for a diode in the S.E.M.

reasoning, the copper sulphide on the sides will be thinner and that in the valleys will be thinnest since diffusion is least probable here.

(a) Sides. Here the electrovoltaic effect is greatest and it is reasonable to suggest that the incident electron beam is being absorbed most efficiently, the $Cu_2S$ layer being of the optimum thickness and uniformity, and the number of recombination centres low.

(b) Tops. The extent of the regions giving rise to this EBIC contrast, was found to be a function of beam energy. The area increased as bias decreased, and it is therefore proposed that there is a thickness variation of $Cu_2S$ over the top of the hillock. Because the formation of copper sulphide is by a displacement reaction with CdS, it is likely that the copper sulphide layer will be thicker at the summits. The electron-hole pairs produced by the beam are expected to recombine before they reach the junction, resulting in current-voltage characteristics resembling those at low illumination.

(c) Valleys. By analogy with the previous case, it is suggested that a thinner layer of copper sulphide forms at the bases of the hillocks than elsewhere. Two possibilities then are that the production of a beam induced current in this region is hindered by the series resistance of the $Cu_2S$ in the valleys or by surface recombination. Another speculative hypothesis is that the series resistance of the heterojunction in the valleys is higher than at other places because copper is driven in more easily there by the heat treatment. Any (or all) of these suggestions would result in the observed contrast.

(d) Flat-topped Hillocks. The distribution of cathodoluminescence confirms that a very thin or non-existent layer of copper sulphide exists on the flat tops of the hillocks. If there is no layer at all, the I-V characteristics will always remain flat, i.e. open circuit. For a very thin layer the former suggestion in the previous section would be applicable.

It has been demonstrated that the conical sides of CdS etch hillocks form the most efficient collectors of energy from an electron beam, some speculative suggestions to account for this have been put forward. A further point is that crystallography may play a part in determining the efficiency of a particular surface by controlling the way that the copper sulphide layer forms (Cook et al, 1970).

At this stage, it perhaps goes too far to suggest that the observations described here of the interaction of an electron beam with a $CdS/Cu_2S$ solar cell can be explained in general in the same way as the interactions of a light beam with a cell. The relative energies of photons and electrons and their absorption by $Cu_2S$ and CdS are very different, and further experimental evidence is required such as a comparison of scanned light and electron beam induced currents before positive statements can be made.

9.3.2 Degradation

The device from which the micrograph shown in Fig.9.2 was taken shortly after manufacture, was re-examined 9 months later. A secondary emission micrograph and the corresponding EBIC display are shown in Fig 9.7(a) and (b). While the secondary emission signal is of precisely the same form as that originally found, EBIC contrast shows some different features, most significantly the presence of small dots on the conical hillocks. This means that the degradation process cannot be associated with a physical change in the surface, but must nevertheless result in a change in electrical properties. The contrast of the dots corresponds to a lower conversion efficiency than the rest of the face, and this is shown in the measured current-voltage characteristics of the degraded device which show a lower short circuit current and open circuit voltage than originally found. The mechanism which produces these dots has not yet been investigated but it is important to notice that the dots

appear to lie at the vertices of the conical faces. Oxidation is the most likely cause of the degradation as these devices were left exposed to the atmosphere in the laboratory during the 9 months. Further study of this ageing effect under different conditions of temperature, illumination and atmosphere will obviously prove interesting.

9.3.3 Etching Procedure

Another type of feature observed on a plated CdS surface is shown in Fig 9.8, (a) shows the S.E. micrograph and (b) the E.B.I.C. signal. This sample was prepared by administering an extended etch in concentrated HCl prior to the dip in the copper plating solution. The etch lasted for 5 minutes and the 10 second plating produced a layer that appeared brown rather than the customary black of the normal copper sulphide layer. The nodules on the surface of the device appear to shield the junction from the electron beam as the EBIC signal shows. The dark contrast corresponds to a low induced current. A reflection electron diffraction study of this sample revealed a pattern of rings. The large number of rings present ($\tilde{\sim}$ 30) and their nature suggest that several compounds are present, one of which from comparison of the A.S.T.M. index with the ring spacings, is certainly chalcocite or djurleite as expected. Without other evidence, with so complicated a pattern, it has proved impossible to work out the other compounds present. The formation of nodules on copper sulphide has also been reported by Lampkin (1979), but he concluded that they were due to cadmium chloride, the undissolved product of the exchange reaction. Reference to the A.S.T.M. index for $CdCl_2$ has shown that the ring pattern does not contain any component from $CdCl_2$, which is not really surprising as $CdCl_2$ is soluble in water, and the sample was well washed after fabrication. In spite of the shadowing effect of these nodules, this device showed good spectral response and I-V characteristics.

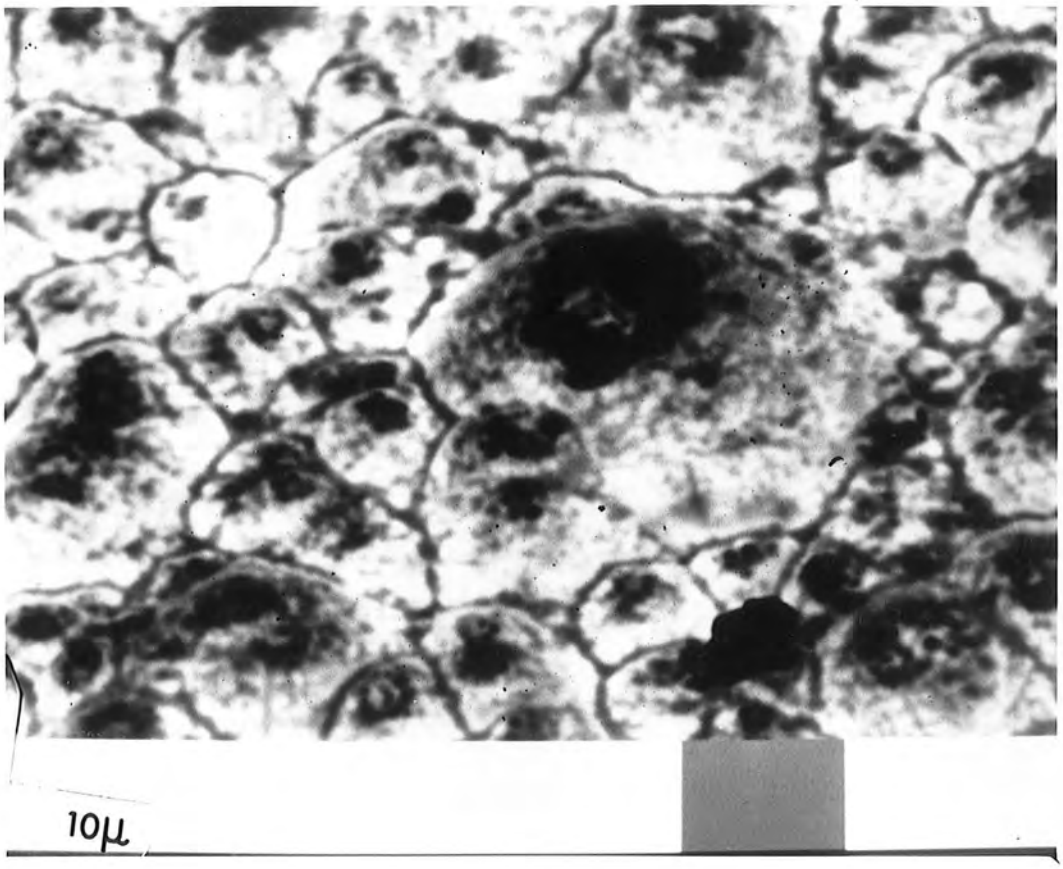



Figure 9.6 : E.B.I.C. micrograph of sample with flat-topped hillocks.

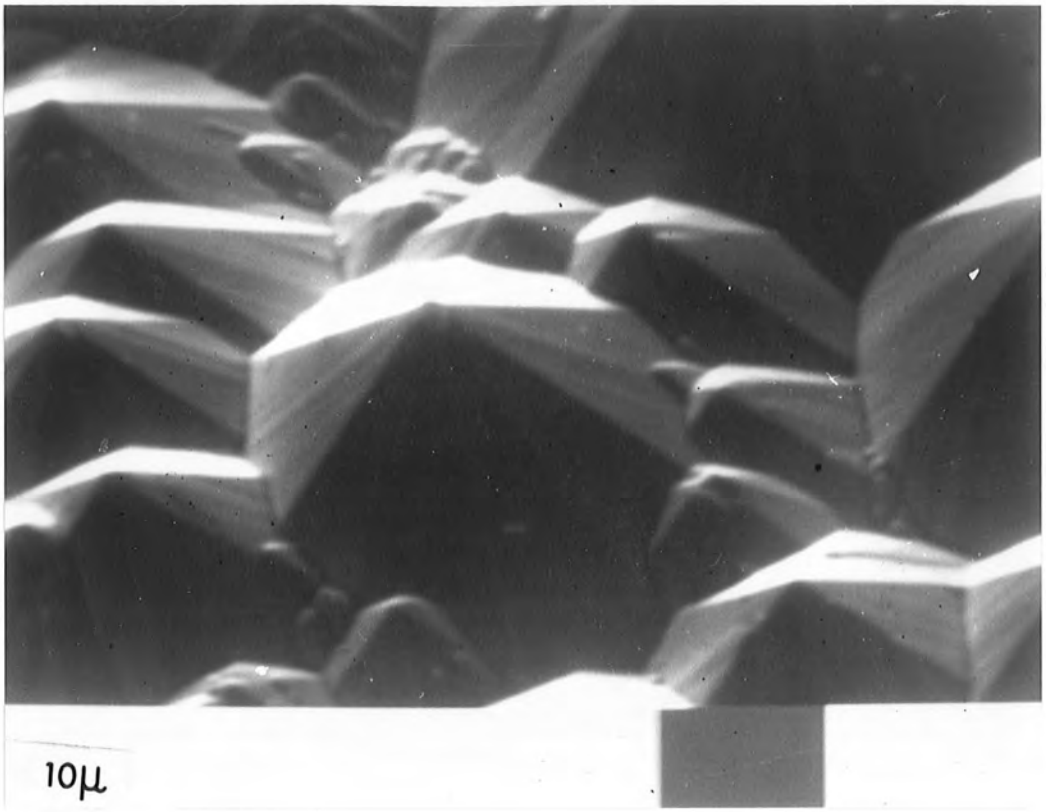
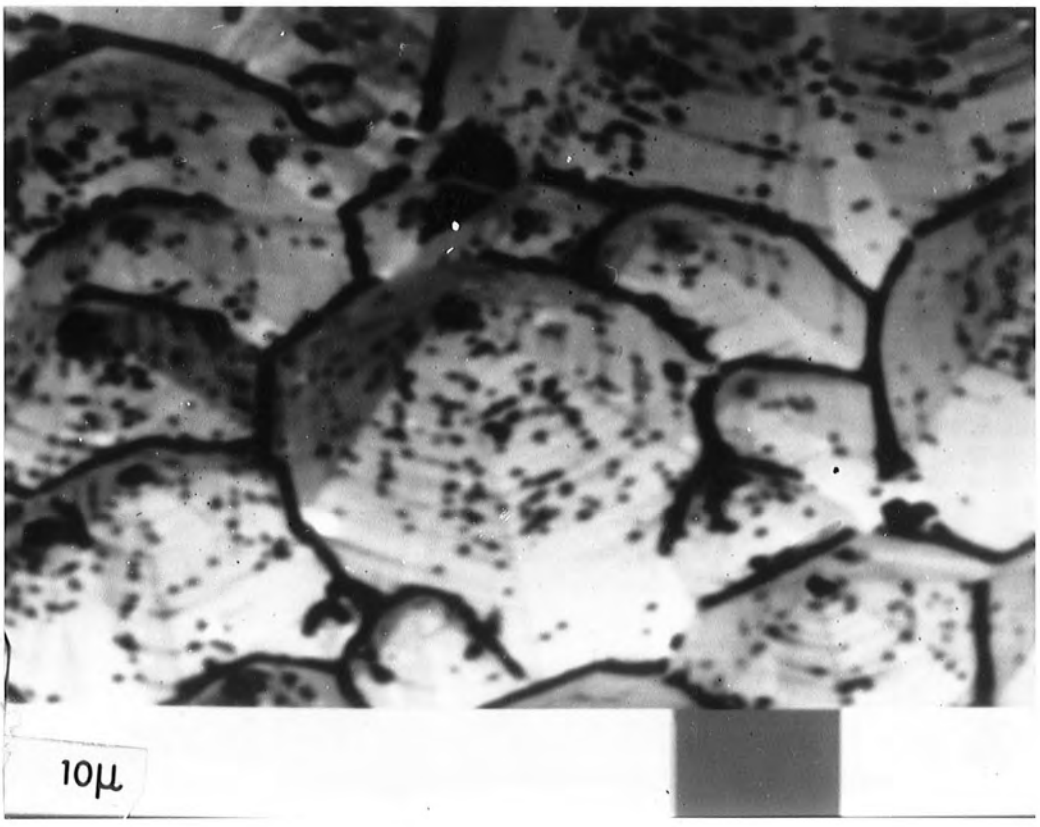



Figure 9.7 (a): Secondary emission micrograph of sample.



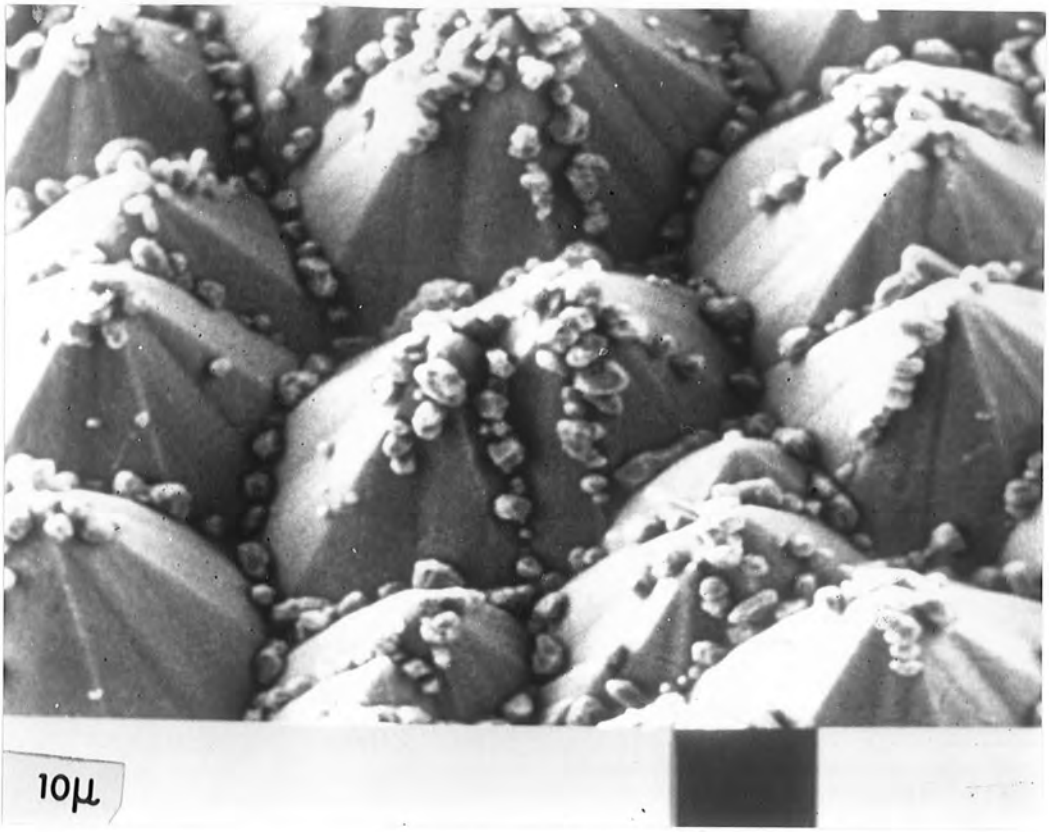
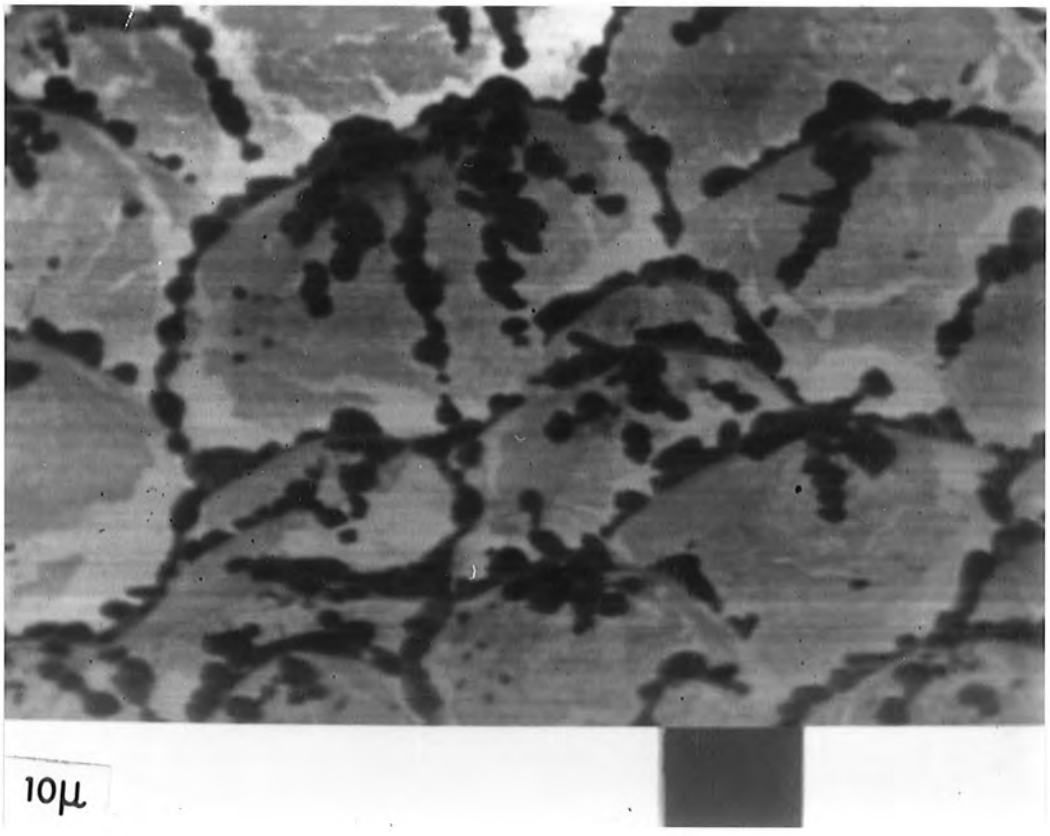



Figure 9.8 (a): Secondary emission micrograph of deeply etched sample.



Further work on the microscopic effects of variations in fabrication techniques should prove interesting. To this end, the scanning electron microscope is obviously a powerful tool not only for looking at surfaces, but also for studying the microscopic electronic properties of devices, as Appendix A also demonstrates.

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# CHAPTER 10

# CONCLUSIONS

## 10.1 In Conclusion

The ultimate aim of the work described in this thesis was to gain a greater understanding of the electronic and optical processes occurring within the CdS/$Cu_2S$ heterojunction photocell, and thence to propose means by which its efficiency might be improved. As many authors, e.g. Shiozawa et al (1969), Potter et al (1968), Fahrenbruch and Bube (1974) have suggested that interface states at the junction control the current flow and thus the optical and electronic properties, it was decided that a study of interface states might prove interesting.

In the CdS/$Cu_2S$ heterojunction the problem of studying states at the junction is complicated by the presence of a photoconductive layer, and by a layer of copper sulphide of variable thickness and composition. Consequently as a simplification, initially an MIS structure with CdS as the semiconductor was investigated. Analysis of the conductance and capacitance characteristics of these devices using the theory of Nicollian and Goetzberger (1967) showed that their model was inapplicable to the experimental data. An alternative explanation (one of insulator leakage) was developed therefore and shown to be consistent not only with the experimental observations but also with the proposals of several other authors. It is further suggested that this explanation may also be applicable to experimental results for other materials described in the literature and interpreted differently. Further work on this would prove interesting.

In Chapter 5, an analysis of different surface layers on CdS single crystal material using and comparing the various modes of

operation possible with a scanning electron microscope was given. This study complemented the preceding conductance and capacitance measurements, and demonstrated the ease with which the uniformity of a surface layer may be determined beneath a Schottky contact. Apparently contradictory results of measurements of the electron beam induced current as a function of bias voltage were resolved by involving two mechanisms, one of which was analogous to the photovoltaic effect, while the other resembled the photoconductance effect. Investigations of ZnSe single crystal material using the techiques developed in this study are presented in Appendix A.

Chapter 6 was concerned with an analysis of the standard preparative conditions for CdS/$Cu_2S$ heterojunctions. Temperature, etch time, and pH of the plating solution were some of the parameters varied, in an attempt to understand more fully the conditions of formation of the different phases of copper sulphide. These were identified by reflection electron diffraction using a transmission electron microscope. In general, it was found that (a) the longer the CdS was etched in HCl before plating the better was the layer of chalcocite produced ; (b) the temperature of the plating bath should be at least 93$^{o}$C, and if the sample was heated before plating the resulting $Cu_2S$ layer was more uniform ; (c) a pH between 2.0 and 2.5 appears to be optimum.

Following this analysis of the preparative conditions, an investigation of the electronic and optical properties of the single crystal devices was reported, with mention being made of measurements of photocapacitance, current versus voltage, and of photocurrent and photovoltage as a function of wavelength. It was first demonstrated by comparing photocapacitance and photoconductance measurements that copper does diffuse from the copper sulphide into the CdS during a 2 minute heat treatment at 200$^{o}$C in air. The spectral response of the

short-circuit current, of a djurleite device was shown to resemble that of a heat treated chalcocite device. It was however concluded that this did not imply that heating in air altered the phase of the copper sulphide, from chalcocite to djurleite, but rather that a photoconductance in series with the photo-emf was responsible. In the djurleite example the response occurred by excitation across the djurleite bandgap. It was also observed that the photoconductance could be excited by the use of a steady bias illumination. In this way the photocell spectrum could be studied without the complication of this photoconductive response.

Using this dual beam technique, with the radiation from the monochromator illuminating the front of the cell while band gap bias light was incident from the side, spectral response measurements were made of both the O.C.V. and S.C.C., since these were found to be dissimilar. Although the responses varied in detail from diode to diode, the principal difference was that at 0.52 μm (CdS band gap), where the photocurrent peaked, the photovoltage displayed a minimum. To make the experiment complete, the light sources were interchanged.

A discussion of some of the many band structure models followed, with particular reference to the experimental results, and the requirement that there be both a variable barrier height and a photoconductance. The Clevite model was found to fit the details of the experiment qualitatively, however the band bending required, which involves a hump in the conduction band of CdS, was thought unlikely from considerations of space charge distribution. A modified band structure model was proposed which combined some features of the Clevite model and others of the Te Velde model (Te Velde 1973). It was found possible to fit all the experimental observations qualitatively. Additional work of a quantitiative nature should prove valuable in establishing

the validity of the model.

Further use of the scanning electron microscope to study the individual surface features of the device, revealed the crystallographic planes which give the greatest electron voltaic effect. If the assumption, that the electron voltaic effect is equivalent to the photovoltaic effect, is valid, then the efficiency of the $CdS/Cu_2S$ heterojunction may be optimised crystallographically. This is, again, an area requiring further work.

10.2 Suggestions for Further Work

In addition to the topics outlined above, future experiments should include measurements of characteristics, particularly the O.C.V. and S.C.C. (under double source illumination), of devices prepared under a wide range of conditions including different phases of copper sulphide. A useful future study involving the S.E.M. would be the development of a more sophisticated circuit for biasing devices and analysing the electron beam induced current created. As was mentioned previously, the EBIC circuit employed did not allow measurements of low resistance devices to be made, owing to the high level of noise.

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# APPENDIX A

## AN ELECTRON BEAM INDUCED CURRENT STUDY OF GRAIN BOUNDARIES IN ZINC SELENIDE

JOURNAL OF MATERIALS SCIENCE 15 (1980) 939–944

# An electron beam induced current study of grain boundaries in zinc selenide



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An electron beam induced current investigation of crystalline samples of zinc selenide in the scanning electron microscope has proved particularly useful in revealing the existence of grain boundaries. Changes in the EBIC contrast which are observed when the bias is altered, or at places where twin bands intersect the grain boundaries, are explained in terms of a model which associates a potential energy barrier, similar to two Schottky barriers back to back, with a grain boundary.

## 1. Introduction

Although the electron beam induced current (EBIC) mode of operation of the scanning electron microscope (SEM) has been used for several years to study such crystalline defects as dislocations [1] and stacking faults [2], there is little recorded evidence so far of its use in the examination of grain boundaries [3]. However, we have found the method to be of great assistance in studying grain boundaries in single crystals of ZnSe doped with indium or gallium. Such material is particularly well suited to EBIC investigation since its resistivity can be varied over a wide range from 10 to $10^7\ \Omega$ cm, or larger, by altering the doping concentration. The purpose of this paper is to describe the nature of the EBIC contrast produced at grain boundaries, and to offer an explanation of the various features observed.

The electrical properties of ZnSe doped with indium or gallium are interesting because unusual donor compensation effects occur at increasing concentrations of the added impurity [4, 5]. Indeed, there are reports [6], that heavily doped epitaxial layers of ZnSe: In have been made *p*-type. We, in this laboratory, have been studying the electrical properties of ZnSe: In and ZnSe: Ga for some time past, and for this purpose have usually prepared samples in the form of small bars (8 mm x 2 mm x 1 mm), with indium contacts at either end, and at intervals along the length. It is quite evident that an applied voltage is not always dropped uniformly along the length of a sample, and such non-uniformity is usually found to have been caused by the potential barrier provided by a grain boundary. Such samples are unsuitable for the evaluation of electrical properties, but are eminently suitable for the investigation of grain boundaries in the EBIC mode in the SEM.

## 2. Experimental procedure

The crystals for this work were grown using the vapour phase technique described by Cutter *et al.* [7], with the modification that appropriate quantities or indium or indium doped ZnSe were added to the charge to produce boules containing concentrations of indium in the range 5 to 1000 p.p.m. Actual indium concentrations were determined by atomic absorption spectroscopy. Undoped crystals of ZnSe were also used in control experiments, but it was necessary first to heat them in molten zinc at 850° C for 48 h to reduce their resistivities from about $10^{12}\ \Omega$ cm to about $10\ \Omega$ cm.

The bars with dimensions of 8 mm x 2 mm x 1 mm were cut from the boules using a diamond wheel. The faces of the bars were mechanically polished with 1 $\mu$m diamond paste and were then chemically etched in a 1% solution of bromine in methanol. After the samples had been rinsed successively in methanol, carbon disulphide and absolute alcohol, contacts were applied by pressing pellets of indium on to them. Finally the bars were heated in argon for 10 min at 300° C.

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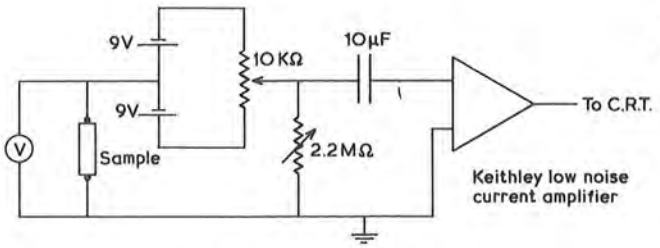


*Figure 1* Biassing and EBIC signal detection circuit for high impedance samples.

The specimens were examined in a Cambridge S600 SEM employing a Keithley specimen current amplifier type 427 to produce the EBIC images. A biassing arrangement was incorporated in the amplifier circuit, see Fig. 1, to enable the behaviour of electrically active defects to be studied as a function of bias voltage.

## 3. Experimental observations

When the indium-doped specimens which exhibited a non-uniform distribution of potential were examined using the EBIC technique, contrast was immediately apparent at some of the grain boundaries, see Fig. 2. This contrast is similar to that produced by the barrier electron voltaic effect at $p$–$n$ junctions in semiconductors [8]. However it differed from the latter effect in that it changed from white (Fig. 2) to black (Fig. 3), when the potential applied to one of the end contacts was changed from + 3 V to − 3 V relative to the other. Fig. 4 is the secondary emission micrograph of the same region of the sample. The grain boundary which gave rise to the EBIC contrast is clearly visible. The lines of light contrast which do not deviate as they cross the grain boundary are associated with saw marks from the diamond wheel which were not removed by the mechanical and chemical polishing from this particular sample. The abrupt termination of twin bands at B draws attention to another grain

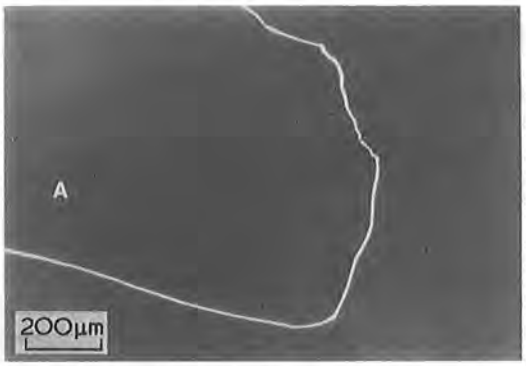


*Figure 2* EBIC micrograph of a grain boundary in ZnSe where + 3 V is applied to grain A.

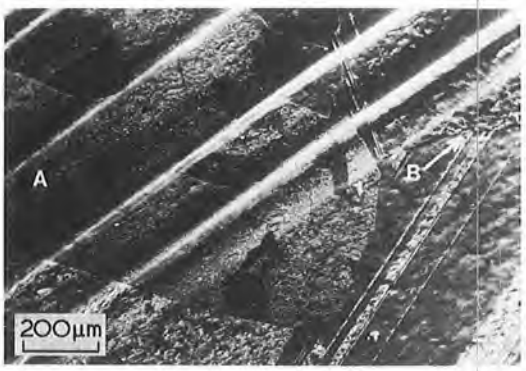


*Figure 4* Secondary emission micrograph of the region shown in Fig. 2 with no bias.

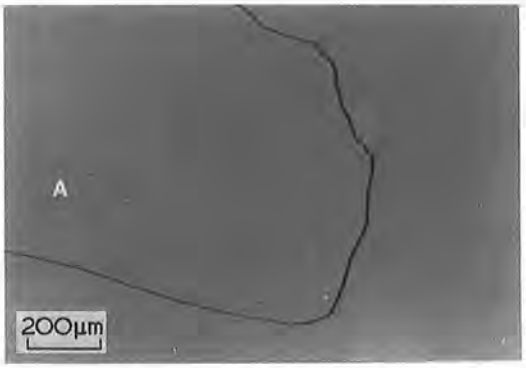


*Figure 3* EBIC micrograph of the region shown in Fig. 2 where − 3 V is applied to grain A.

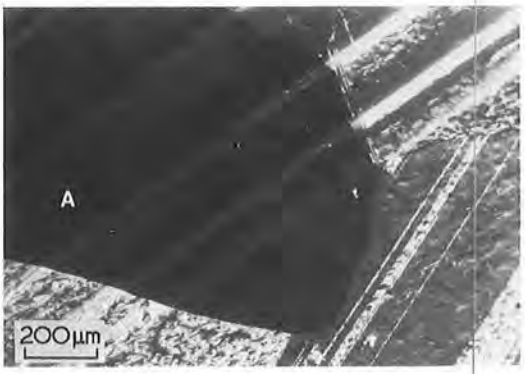


*Figure 5* Secondary emission micrograph of the region shown in Fig. 2 where + 3 V is applied to grain A.


*Figure 6* Secondary emission micrograph of the region shown in Fig. 2 where − 3 V is applied to grain A.

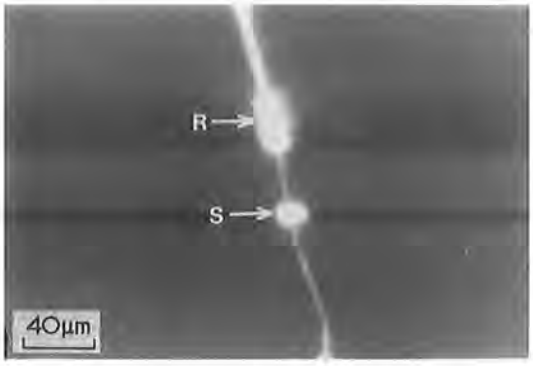


*Figure 7* Micrograph showing the modification to the EBIC signal where twin bands meet a grain boundary in ZnSe.

boundary, which, with the electrode configuration employed, was not active in the EBIC mode. However, contrast at this grain boundary was readily obtainable when the bias was applied to a different set of electrodes. In general the boundaries active in the EBIC mode formed a single continuous barrier between the two electrodes across which the potential was applied. Boundaries connecting the two electrodes were invariably inactive in the EBIC mode.

Confirmation that the EBIC contrast shown in Figs. 2 and 3 was associated with an electrical barrier along a grain boundary was provided by the voltage contrast effects observed in secondary emission. Figs. 5 and 6 show secondary emission micrographs of the same area seen in Fig. 4. Fig. 4 was obtained with zero voltage applied to the sample, but Figs. 5 and 6 resulted when the grain A was biassed to + 3 V and − 3 V relative to the remainder of the sample. In both the latter two micrographs the contrast is uniform in two separate regions, inside or outside of grain A. In each micrograph the region of light contrast corresponds to a surface carrying a negative potential, while the area of dark contrast corresponds to regions with a positive one. Thus an abrupt potential difference occurs only at the boundary which surrounds grain A. It is interesting to record that when the bias was increased to about 30 V, so that a current density of some 5 A $cm^{-2}$ was flowing, spots of yellow light were emitted from the same grain boundary surrounding grain A. This light emission is no doubt associated with regions of high localized electric field.

An important feature of the EBIC signal emanating from grain boundaries was its dependence of the local crystallography. This was most obvious at places where twin bands terminated at

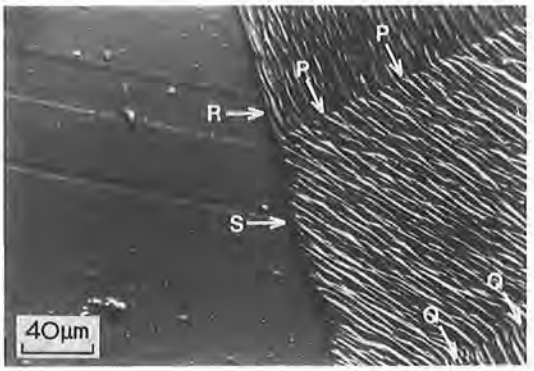


*Figure 8* Secondary emission micrographs of the region shown in Fig. 7.

an electrically active boundary thus introducing local modifications in the crystal structure at the intersection of the two grains. An example illustrating this effect is shown in Fig. 7, while the corresponding secondary emission micrograph forms Fig. 8. Comparison of the two micrographs reveals that the two twin bands in the grain on the left-hand side in Fig. 8, give rise to a broadening of the EBIC signal at points R and S on the boundary, as is clearly evident in Fig. 7. From a closer inspection of Fig. 8 the presence of twin boundaries can also be inferred along PP and QQ where the striations produced by the etching change direction. The presence of this wide twin band on the right-hand side of Fig. 8 gives rise to an EBIC signal which is broader at the top of Fig. 7 than that at the bottom.

The effect of reversing the polarity of the voltage applied to the region shown in Fig. 7 is recorded in Fig. 9. Comparison of the two EBIC images leads to the conclusion that EBIC signals that are wide for one sign of applied voltage are

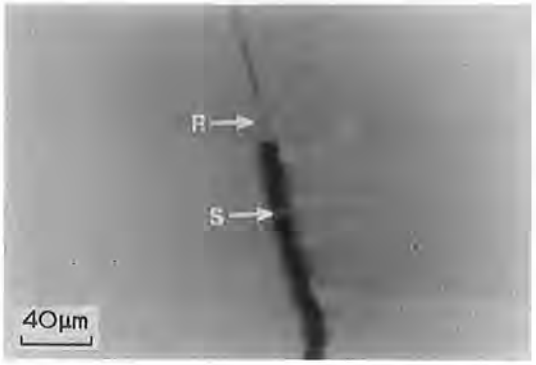


*Figure 9* EBIC micrograph of the region shown in Fig. 7 with the polarity of the applied voltage reversed.

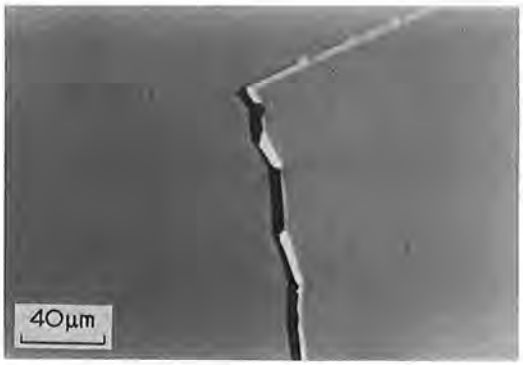


*Figure 10* EBIC micrograph from another grain boundary in ZnSe with zero applied bias.

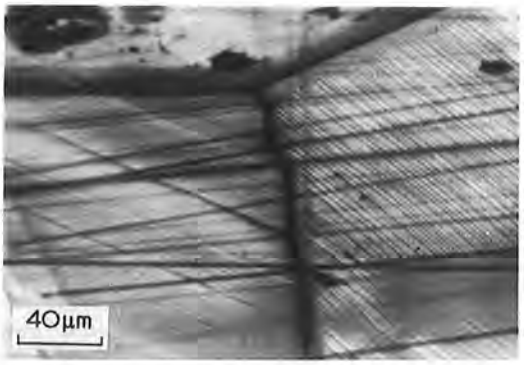


*Figure 11* Cathodoluminescent image of the region shown in Fig. 10.

narrow for the other, and vice versa. An interesting consequence of this effect is the form of the EBIC signal obtained with zero bias. Such an image is shown in Fig. 10, which is from a different area from that used to obtain Figs. 7 and 9. It does however correspond to a grain boundary with twin bands terminating along its length. The zero bias contrast takes a form which is intermediate between those exhibited by a similar boundary in the two different bias conditions shown in Figs. 7 and 9. The grain boundary then gives rise to a black/white contrast to varying degrees along its length. By rotating the sample through 180° in the SEM it was demonstrated that this particular contrast was independent of the direction of the beam scan. The origin of the contrast effect is discussed below.

Finally, it is worth mentioning that examination of the samples in the SEM in the cathodoluminescence mode shows that the luminescence was always suppressed at the grain boundaries. This is illustrated in Fig. 11 which is a cathodoluminescent image of the same area which provided the EBIC image shown in Fig. 10. Clearly radiationless recombination occurs preferentially at these grain boundaries.

## 4. Discussion

The qualitative model proposed to explain the EBIC observations can be understood by reference to the potential energy diagrams shown in Fig. 12. At some grain boundaries the conduction and valence bands of the *n*-type ZnSe will be bent upwards as illustrated in Fig. 12a. The band bending may well be a consequence of the segregation of impurities to the grain boundaries where they can act as acceptor states. Electrons from donors in the immediate vicinity would be captured by the acceptors, producing a layer of negative charge at the grain boundary, and leaving a region of positive space charge in the ZnSe close to the boundary. The width of the resultant depletion region would depend on the conductivity of the grain and the concentration of surface acceptor states at the grain boundary. The suggestion is therefore that each grain boundary would be accompanied by a potential barrier similar to that in Fig. 12a, and consequently each grain boundary would have a built-in electric field associated with it. When such grain boundaries with their associated depletion regions form a continuous barrier between contacts, they will limit the total current flow. Electron bombardment within a depletion region will then lead to a beam induced current so that contrast will be observed in the EBIC mode. When a grain boundary forms a connecting path between the contacts, the accompanying depletion regions will have a very small effect on the total current flow, with the result that

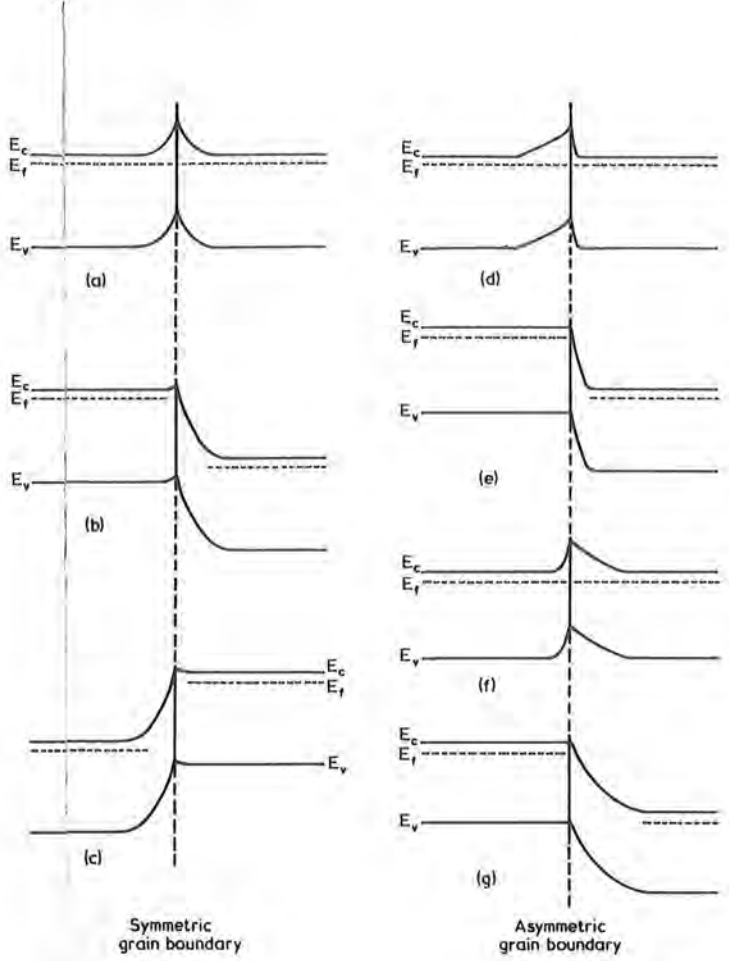


*Figure 12* Energy band diagrams for: (a) a symmetric grain boundary without bias. (b) The boundary in (a) with negative bias on the left-hand side. (c) The boundary in (a) with negative bias on the right-hand side. (d) An asymmetric grain boundary without bias. (e) The boundary in (d) with negative bias on the left-hand side. (f) The other configuration for an asymmetric grain boundary without bias. (g) The boundary in (f) with negative bias on the left-hand side.

bombardment within the depletion region will have virtually no effect on the total current flow. No EBIC contrast therefore will be observed.

Consider next what happens when the electron beam is scanned from left to right across a grain boundary with an associated potential barrier such as that depicted in Fig. 12a. Assume first that zero bias is applied. When the beam reaches the left-hand depletion region, the beam-induced electron–hole pairs are separated by the internal field, and the majority carriers (electrons) are swept towards the left-hand contact while the minority carriers (holes) recombine via the recombination centres at the grain boundary with electrons captured from either side of the boundary. That such recombination centres exist is demonstrated by the cathodoluminescent image in Fig. 11 which shows that luminescence is suppressed at grain boundaries. If the sample is connected so that the electron current flow to the left from the grain boundary produces a dark image on the screen, then a black line will be formed just to the left of the grain boundary. When the beam reaches the right-hand side of the grain-boundary, the current flowing in the external circuit will reverse and electrons will flow from left to right. A white line will then be produced in the EBIC image. This is exactly what is observed in Fig. 10.

When a bias is applied to the sample, the potential energy barriers become asymmetric as shown in Figs. 12b and c, which are for the two possible polarities of the applied voltage. As the beam scans a biassed barrier, Fig. 12b, little separation of the induced electron–hole pairs to the left of the barrier occurs, so that the total current is only slightly affected. On the right-hand side of the barrier, however, a high field exists so that the electron–hole pairs are readily swept apart. As a result an intense white line appears in the EBIC image as in Fig. 2. With reversed polarity the potential energy diagram in Fig. 12c is appropriate and clearly the beam induced electron current now flows from right to left, producing a dark line in the EBIC mode, Fig. 3. In effect, if the barriers in Figs. 12b and c are regarded as two Schottky barriers back-to-back, one of the Schottky barriers is biassed in the forward direction and the other in the reverse. A beam induced current would only be expected at a reverse-biassed Schottky barrier. In this discussion of the

contrast when an external voltage is applied, it has been assumed that virtually all the voltage is dropped across the grain boundary. This is indeed a reasonable assumption as the micrographs obtained in secondary emission with voltage contrast (Figs. 5 and 6) show.

The more complicated EBIC effects illustrated in Figs. 7 and 9 can be explained if the extent of the band bending is different on either side of the grain boundary, as in Figs. 12d and f, and varies when the crystallographic orientation of the grains changes (for example when twin bands intersect the grain boundary). The different widths of the black and white portions of the unbiassed EBIC images in Fig. 10 can also be explained with the same model, namely that a barrier such as that in Fig. 12d will have a broader stripe of contrast on the left corresponding to the wider depletion region.

With the appropriate bias applied, the barrier in Fig. 12d goes over to that in Fig. 12e, while 12f goes to 12g. In Fig. 12e the internal field is large and the depletion region is relatively narrow; as a result the white line in the EBIC image, is narrow as can be seen in the bottom half of Fig. 7. With the situation shown in Fig. 12g however, the electric field extends over a wider region, leading to the broader white region at the top of Fig. 7. When the bias is reversed, Fig. 12e, for example, will be replaced with a diagram in which the space charge region now on the left of the barrier is wider than that on the right in Fig. 12e. This means that reversal of polarity will lead to the replacement of a narrow white stripe with a broad black one; a narrow black line will also replace a broad white one. This is clearly shown in Fig. 9.

In conclusion, it might be remarked that the EBIC technique has proved to be invaluable in demonstrating which samples of ZnSe are most useful for the evaluation of the electrical properties of the material, i.e. to demonstrate which samples contain no potential barriers and which can therefore be used to provide meaningful Hall coefficient measurements, etc. The proposed qualitative theory of grain boundary barriers can explain all the observed phenomena and could, if necessary, be put on a quantitative basis. Preliminary attempts to determine whether segregation of indium to the grain boundaries is primarily responsible for the band bending have proved inconclusive, but it should be reported that we have also observed similar EBIC contrast effects at grain boundaries in nominally undoped samples of ZnSe that have been heat treated in molten Zn at 850° C.

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Received 3 August and accepted 20 September 1979.