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INFLUENCE OF GASES ON THE ELECTRICAL PROPERTIES OF MIS DEVICES

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Abstract

This thesis studies the effects of gas ambients on the electrical properties of the insulator-semiconductor interface of a MIS capacitor. A microcomputer-controlled instrumentation system has been developed to extract this information from measurement of the a.c. admittance of MOS or MIS devices. The system incorporates several novel developments in circuitry and software which enable these admittance data to be automatically collected and processed in the frequency domain by remote recalibration of the instrumentation. This advancement permits interface state density information to be calculated more quickly and accurately than has been previously possible using manually-operated equipment.

The system has been used to investigate the influence of gases on the density of interface states in a MIS capacitor, in particular the palladium/silicon dioxide/silicon structure which is sensitive to hydrogen gas. A distinct change in the distribution of surface state density across the silicon bandgap has been observed upon exposure to a hydrogen ambient. An alternative insulating layer, an organic Langmuir-Blodgett film multilayer of ω-tricosenoic acid, has been characterised and examined, and increased sensitivity of this structure to hydrogen gas has been indicated.

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15. FEB. 1987

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CHAPTER 1 : INTRODUCTION

There is currently a great deal of interest in the development of a wide range of transducers for accurate measurement of physical properties in order to effectively interface electronic equipment to the real world. One structure which is well-suited for this purpose is the metal-insulator-semiconductor (MIS) capacitor, as its electrical properties may be altered by external influences on the device. Impurities or defects either inherent in the semiconductor material or introduced during device processing may create trapping levels at the insulator-semiconductor boundary which interact with mobile carriers in the semiconductor, thus changing the admittance characteristics of the device. We have been particularly interested in the effects of different gases on these interface (or surface) states with a view to developing a sensitive gas detection system.

The electrical nature of these MIS devices is described in chapter 2 by first considering the properties of an ideal device and by expanding this theory to allow for additional charges in the structure introduced by impurities in the insulator and at the semiconductor surface. In chapter 3, the methods used to determine the electrical characteristics of the MIS capacitor are considered, and the measurements necessary for evaluating the surface state density (N_{ss}) distribution are discussed. The most accurate is the conductance technique of Nicollian and Goetzberger, in which the a.c. admittance properties of the device are recorded. However, the standard approach is time-consuming in practice because of the large amount of data which must be collected and the need to calibrate the instrumentation at each measurement frequency. In this work, an instrumentation system has been developed to reduce the time and effort involved in surface state evaluation. These savings have been accomplished by using a microcomputer to automatically recalibrate the equipment, take admittance readings and interpret these data for N_{ss} calculation. In addition, a number of improvements in the electronic signal-processing circuitry have been incorporated into

the design. Details of the instrumentation and hardware developments are given in chapter 4 whilst the operational procedure and software are discussed in chapter 5 along with an assessment of the system performance.

The degree to which the electrical characteristics of MIS devices are influenced by the ambient surrounding the device is a subject of great controversy. One area which has received particular attention is the well-recognised hydrogen response of palladium-gate silicon dioxide/silicon structures. Some workers have indicated that surface states are affected by the presence of hydrogen gas, but others believe that this is not so. The instrumentation system developed in this work has been used to measure the electrical properties of $Pd/SiO_2/Si$ capacitors in order to resolve this argument, and a distinct change in surface state density has been observed upon exposure to a hydrogen atmosphere; these experiments are reported in chapter 6. In an attempt to increase the magnitude of this response, MIS structures incorporating a Langmuir-Blodgett (LB) film insulator have been investigated. The electrical characteristics of the LB film material, ω-tricosenoic acid, have been measured, and the effect of external influences (such as moisture, film preparation and storage conditions) on the device properties have been examined. Increased sensitivity to hydrogen gas has been indicated, and the results obtained with these organic multilayer structures are detailed in chapters 7 and 8.

CHAPTER 2: PHYSICS OF METAL-INSULATOR-SEMICONDUCTOR STRUCTURES

2.0 Introduction

The metal-insulator-semiconductor (MIS) capacitor is perhaps the most important structure used for studying the electrical properties of semiconductor devices. By far the most investigated and best understood system is the silicon - silicon dioxide combination, and this chapter will consider in the main the properties of this MOS (metal-oxide-semiconductor) structure, although the concepts presented here are equally applicable to devices of other insulator and semiconductor materials.

Most oxidised silicon surfaces and many other similar systems contain a number of trapping levels close to the oxide-semiconductor interface (surface states) which will influence the electrical behaviour of MIS devices. Although the density of surface states for thermally-oxidised silicon can be as low as 10^9 $cm^{-2}eV^{-1}$ with careful preparation (1), some four or five orders of magnitude lower than that of "bare" silicon surfaces, these may still have a significant effect upon the electrical properties of a practical device.

In order to understand the characteristics of practical MIS devices, we shall first consider the "ideal" MOS capacitor and then examine the nature and behaviour of "real" structures.

2.1 The ideal MOS Capacitor

For the purpose of conciseness, the theoretical discussions presented below will be limited to consideration of n-type semiconductors only; all samples examined in the experiments reported in this thesis were based on n-type silicon. However, the theory is very similar for p-type semiconductors, and the reader is referred to some of the many texts on semiconductor physics for further information (1, 2). Throughout this chapter, unit area is assumed when discussing charge, capacitance and density of states.

2.1.1 Basic Principles

The cross-section of a MIS capacitor is shown in figure 2.1 and consists of a semiconductor substrate on top of which lies an insulating layer. A metal electrode is deposited onto the insulator, and the metal-insulator-semiconductor structure is completed by making an ohmic back contact to the semiconductor. In the case of a silicon MOS device, the insulator is a layer of thermally oxidised silicon grown on a silicon single crystal. This structure was first used to investigate silicon surfaces by Terman (3), and other researchers (4, 5).

To be termed "ideal", a MOS capacitor must possess the following properties:

1) The semiconductor substrate is uniformly doped and has no defect levels
2) The oxide is free of space charges
3) The oxide is an insulator of infinite electrical resistance
4) There is no energy difference between the metal and the semiconductor work functions at zero applied bias.

This last condition may be described mathematically for n-type semiconductors by

$$\phi_{ms} = \phi_m - (\chi + (E_c - E_v)/2q - \psi_B) = 0 \qquad (2.1)$$

and the corresponding energy-band diagram is depicted in figure 2.2; q is the electronic charge, ϕ_m the metal work function, χ the semiconductor electron affinity and ψ_B the potential difference between Fermi level E_F and intrinsic Fermi level E_i. E_c and E_v represent the edges of the conduction and valence bands respectively. With no applied voltage, the energy bands are flat and the metal and semiconductor Fermi levels are aligned - this is called the flat-band condition.

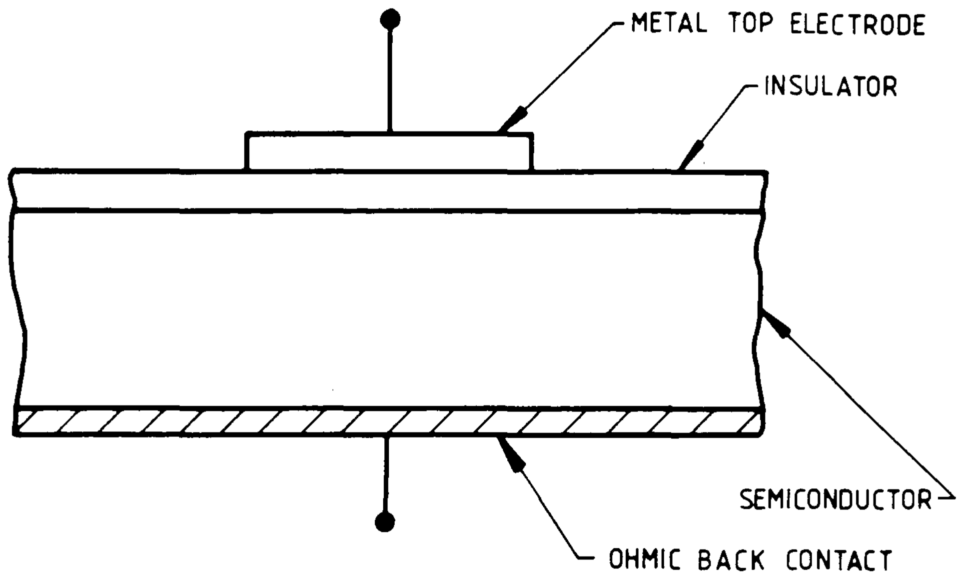


Figure 2.1 : Cross-section of metal-insulator-semiconductor structure

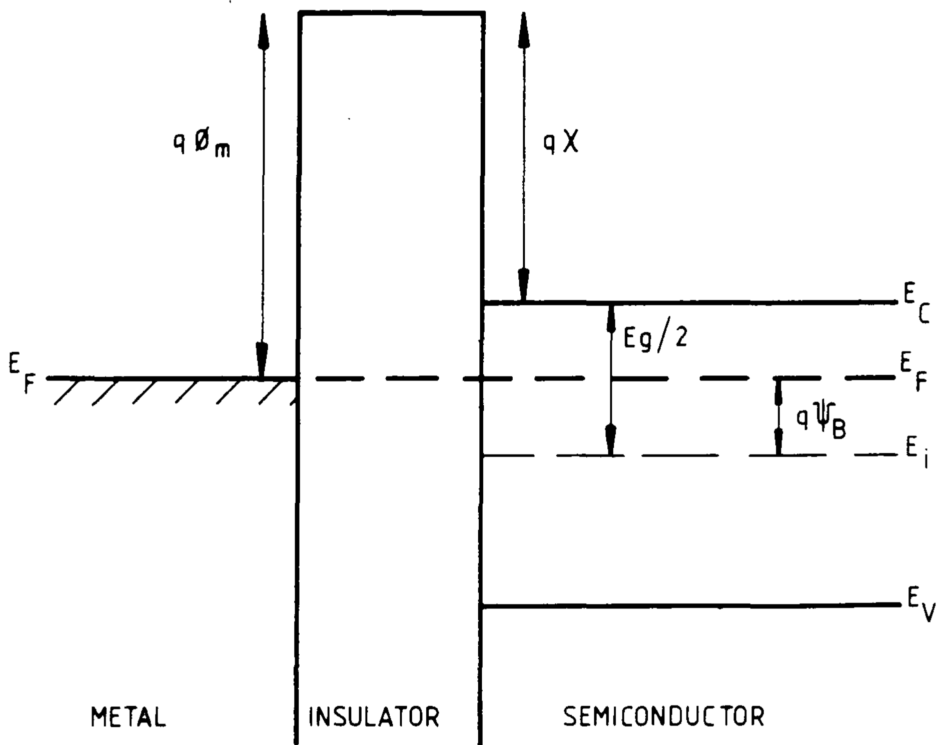


Figure 2.2 : Energy band diagram for n-type ideal MIS device with zero applied bias

When a d.c. bias voltage is applied to the device, electrons in the metal will flow towards or away from (depending on the polarity) the metal-insulator junction, causing a net charge Q_m at this interface. Consequently, there will be a build-up of oppositely-charged carriers near the semiconductor-insulator interface which will result in the bending of energy bands in the semiconductor. The total semiconductor space charge Q_{sc} will equal the charge Q_m on the metal electrode. The amount of band bending is measured with respect to the energy of the intrinsic Fermi level E_i in the bulk of the semiconductor, and is represented by the electrostatic potential at the semiconductor surface, ψ_s.

Electron and hole concentrations at this point are given by:

$$n = n_o \exp(q\psi_s/kT) \qquad (2.2a)$$

and

$$p = p_o \exp(-q\psi_s/kT) \qquad (2.2b)$$

where n_o and p_o are the densities of electrons and holes in the semiconductor bulk, k is the Boltzmann constant, and T the absolute temperature.

Varying degrees of band bending may be achieved by changing the voltage V applied to the MOS structure. Conventionally V is defined as the potential between the metal top electrode and the semiconductor back contact (i.e. V is positive if the metal field plate is more positive than the semiconductor). The possible ranges of surface potential for n-type semiconductors are illustrated in figure 2.3. These are:

<u>Accumulation</u> (Fig. 2.3a)

$\psi_s > 0$: enhanced electron concentration at the interface

<u>Flat-band</u> (shown in Fig. 2.2)

$\psi_s = 0$: electron and hole concentrations equal to intrinsic values

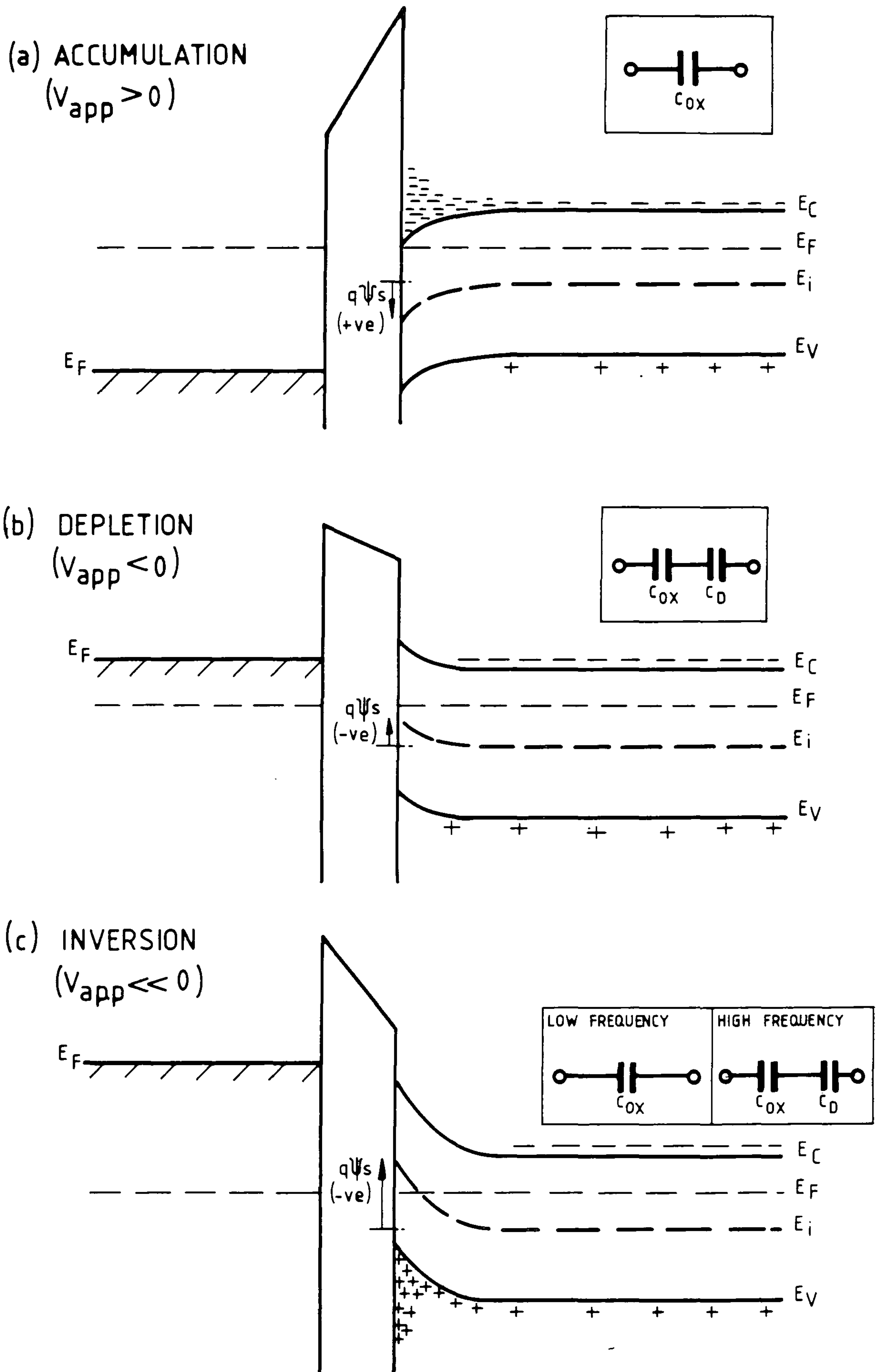


Figure 2.3 : Energy band diagrams for n-type ideal MIS device with applied bias (Insets show equivalent electrical circuits)

Depletion (Fig. 2.3b)

$0 > \psi_s > 2\psi_B$: depleted electron concentration at the interface

Inversion (Fig. 2.3c)

$\psi_s < 2\psi_B$: enhanced hole (minority-carrier) concentration at the interface

It is clear from the above that the carrier concentration in the semiconductor space-charge region will change as the energy bands are influenced by applied bias. The total charge per unit surface area may be determined by integration of the one-dimensional Poisson equation or invoking Gauss' law. For electrons, this procedure yields the relationship (2, 6)

$$Q_{sc} = \pm \frac{\varepsilon_s}{\lambda_D} \frac{2kT}{q} G\left(\psi_s, \frac{p_o}{n_o}\right) \tag{2.3}$$

(positive for $\psi_s < 0$, negative for $\psi_s > 0$). ε_s is the semiconductor dielectric permittivity, and the abbreviations λ_D (the extrinsic Debye length) and $G(\psi_s, p_o/n_o)$ are given by

$$\lambda_D = \left(\frac{2kT\varepsilon_s}{N_d q^2}\right)^{\frac{1}{2}} \tag{2.4a}$$

and

$$G\left(\psi_s, \frac{p_o}{n_o}\right) = \pm\left\{\exp\left(\frac{q\psi_s}{kT}\right) - \frac{q\psi_s}{kT} - 1 + \frac{p_o}{n_o}\left[\exp\left(\frac{-q\psi_s}{kT}\right) + \frac{q\psi_s}{kT} - 1\right]\right\}^{\frac{1}{2}} \tag{2.4b}$$

N_d is the semiconductor doping concentration.

The differential capacitance of the space-charge region is defined as [2, 7]

$$C_D \equiv \frac{\partial Q_{sc}}{\partial \psi_s} = \frac{\varepsilon_s}{\lambda_D} \frac{1-\exp(q\psi_s/kT) + \frac{p_o}{n_o}\left[\exp(-q\psi_s/kT)-1\right]}{G\left(\psi_s, \frac{p_o}{n_o}\right)} \quad (2.5)$$

This relationship satisfactorily describes the depletion and weak inversion conditions, under which all experiments reported below were performed. (A more general treatment of the space charge capacitance, which is also valid for accumulation and strong inversion, has been presented in an article by Brown and Gray [8], to which the reader is referred; however, this work will not be reproduced here).

2.1.2 Electrical Properties

The simple MOS device discussed in the previous section may be considered as a series connection of the oxide capacitance, C_{ox}, and the space charge capacitance, C_D. The total capacitance of the structure is thus:

$$C = \frac{C_{ox} C_D}{C_{ox}+C_D} \quad (2.6) \qquad \text{or} \quad \frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_D} \quad (2.6a)$$

and any applied voltage will appear partly across each region, according to the relation

$$V_{app} = V_{ox} + \psi_s \quad (2.7)$$

V_{ox} is the voltage across the oxide layer, and is given by

$$V_{ox} = \frac{Q_{sc}}{C_{ox}} \quad (2.8)$$

where Q_{sc} is the semiconductor space charge as defined in equation 2.3.

The relationship between MOS capacitance and bias voltage is best illustrated by considering the insets of figure 2.3 and the typical capacitance-voltage (C-V) curve [7] shown in figure 2.4. This is obtained by applying a d.c. bias perturbed by a small a.c. signal to the sample and measuring the device capacitance [7, 1, 2]. The four bias regions described above (section 2.1.1) may be distinguished. In accumulation, the total capacitance is close to the oxide capacitance since the space charge capacitance of the semiconductor is large (i.e. charge is concentrated close to the oxide/semiconductor interface). At the flat-band condition, $V_{app} = 0$, the space charge is more spread out into the semiconductor and adds a series capacitance, obtained by expanding the exponential terms in equation 2.5, of

$$C_{D(fb)} = \frac{\sqrt{2}\varepsilon_s}{\lambda_D} \tag{2.9}$$

which reduces the total capacitance of the structure. This space charge region grows wider as the majority carriers are depleted, and there is a further decrease in MOS capacitance. In the depletion regime, equation 2.5 becomes

$$C_{D(dep)} = \left[\frac{qN_d\varepsilon_s}{2(\Psi_s - kT/q)} \right]^{\frac{1}{2}} \tag{2.10}$$

In the inversion region, the enhanced minority carrier concentration at the interface influences the total device capacitance, but its effect is dependent upon the frequency of the applied signal. At low frequencies (typically below 1Hz) the minority carriers are able to respond to the applied a.c. ripple and consequently the total capacitance rises to close to the oxide capacitance. (Again, charge is concentrated close to the interface, effectively "short-circuiting" the space charge region). However, at high frequencies (typically >10 kHz) these carriers cannot follow the a.c. excitation; they are in equilibrium with the d.c. bias. The differential space charge capacitance $C_{D(inv)}$ saturates in the inversion region at the value given by equation (2.10) and the total capacitance remains low.

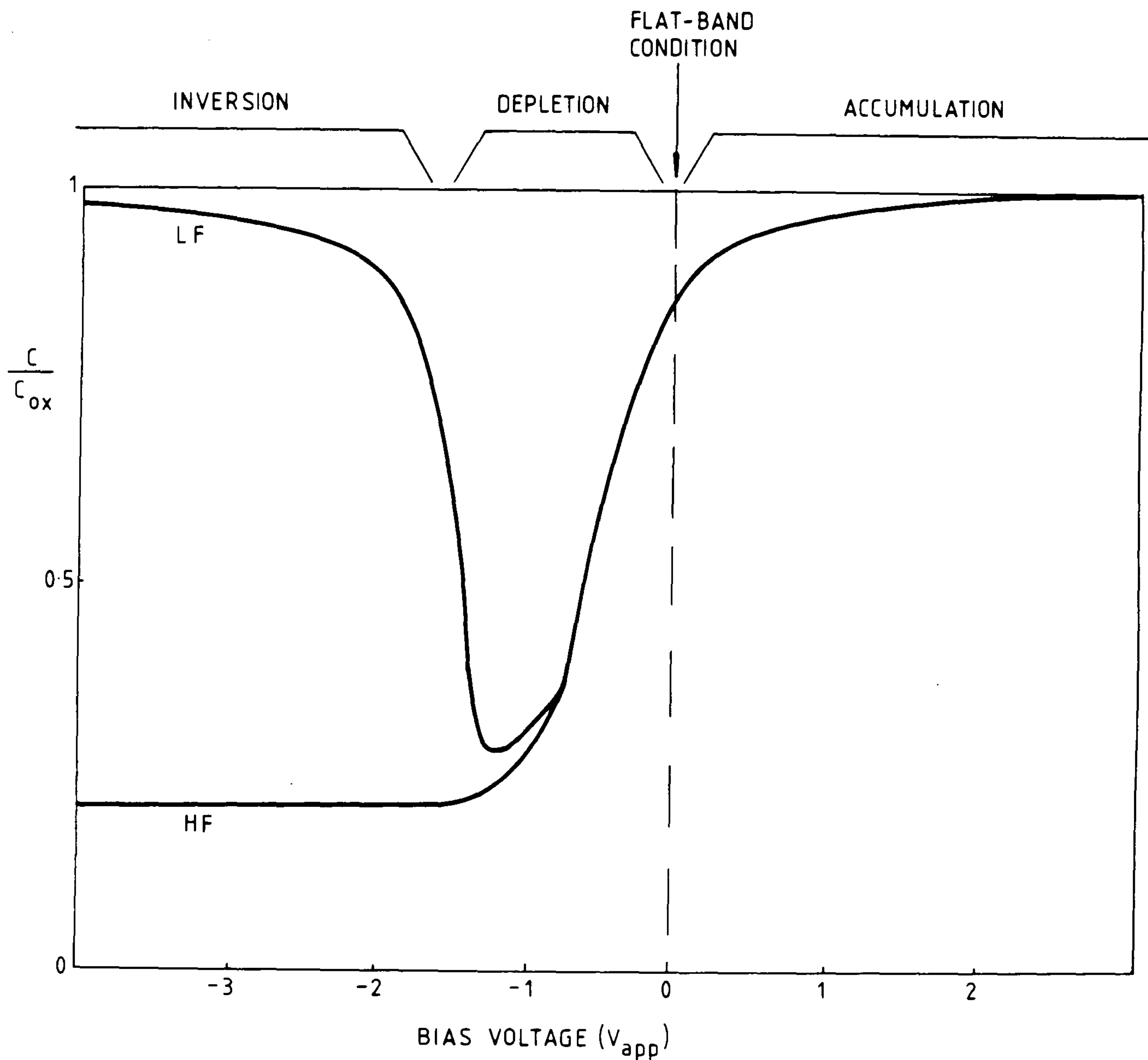


Figure 2.4 : Low frequency (LF) and high frequency (HF) capacitance-voltage curves for an ideal MOS capacitor

The shape of the C-V characteristics varies for different semiconductor doping densities and insulator thicknesses. Goetzberger[9] has published sets of C-V plots, surface potential versus applied voltage data and flat band capacitance values, all calculated with respect to these two parameters, for the ideal metal-SiO_2-Si system. These curves may be applied to other insulators by simply rescaling to allow for the different dielectric permittivity [2].

2.1.3 Characteristics of non-ideal devices

In a real MIS capacitor, the C-V curves will be altered from the idealized case considered above due to work function differences between the metal and semiconductor, dipole layers in the device structure, charges in the insulator and trapping states at the insulator/semiconductor interface.

Where there is a non-zero work function difference between metal and silicon (i.e. in equation 2.1, $\phi_{ms} \neq 0$) the Fermi levels in figure 2.2 will not be aligned and the energy bands will be bent even without any applied bias [5]. This "built-in" voltage changes the surface potential relationship to applied bias; equation 2.7 becomes

$$V_{app} = V_{ox} + \psi_s + \phi_{ms} \tag{2.11}$$

The flat-band condition will be restored when the applied bias equals the barrier potential

$$V_{FB} = \phi_{ms} \tag{2.12}$$

which will offset this additional voltage. The shape of the C-V characteristic will be unaltered from the ideal response (figure 2.4) but there will be a parallel shift of the curve along the voltage axis by an amount equal to V_{FB} (which is called the flat-band voltage).

If any dipole layers exist [10] at the metal-insulator interface, or within the insulator, then equations 2.11 and 2.12 become

$$V_{app} = V_{ox} + \psi_s + \phi_{ms} - \frac{\sigma t}{\varepsilon_{ox}} \tag{2.11a}$$

and

$$V_{FB} = \phi_{ms} - \frac{\sigma t}{\varepsilon_{ox}} \tag{2.12a}$$

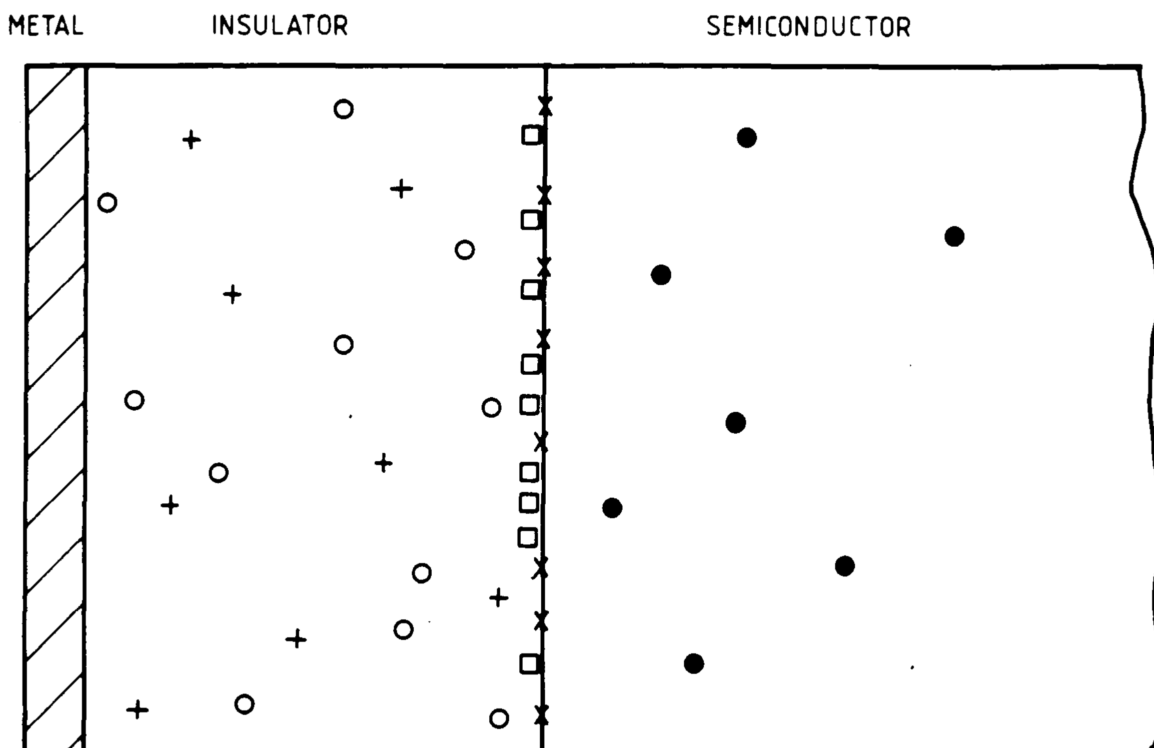
where σ is the charge density, ε_{ox} the absolute permittivity of the oxide, and t the distance of separation of the two sheets of charge.

Charges in the insulator will invoke a similar shift in the C-V curves, and possibly a hysteresis[7] in the measured characteristics due to mobile ions. Interfacial trapping sites distort the curve shape as well as stretching out the response with respect to the voltage axis. These effects are explained more fully in the following sections.

2.2 Insulator Charge and Semiconductor Surface States

Because of its importance as a test structure to assess the performance and behaviour of semiconductor devices, the MIS capacitor has been extensively modelled and investigated by a great number of researchers; a book by Nicollian and Brews[1] deals solely with this subject, and is recommended as a comprehensive reference.

The discussion of the ideal MIS capacitor presented above does not consider any charges in the structure apart from the majority and minority carriers in the semiconductor. In a real device, however, a number of additional charges may be present [2] due to imperfections and impurities either inherent in the semiconductor crystal and/or insulating layer or introduced into these materials during device processing (Figure 2.5).



□ FIXED SURFACE CHARGES
+ IONISED TRAPS
○ MOBILE IONS
X SURFACE STATES (INTERFACE STATES)
● BULK SEMICONDUCTOR TRAPS

Figure 2.5 : Possible states and charges in a non-ideal MIS device

This section concentrates particularly on the nature of the possible states and charges in the insulator and at the semiconductor surface of a SiO_2-Si MOS capacitor, and their effect on the electrical properties of the device.

2.2.1 Nature of the silicon - silicon dioxide system

Any interruption of a perfect crystal lattice by a defect or impurity will result in the creation of extra energy levels that may be situated in the "forbidden" bandgap of the material. If these levels occur in the bulk of the material they are referred to as bulk traps; at the surface or at an interface with another material they are known as surface or interface states.

In silicon crystals, the surface states are believed to be due to a dangling bond at each atomic site at the semiconductor surface[11], as depicted schematically in figure 2.6a. The growth of silicon dioxide reduces the number of surface states by saturating some of these dangling bonds; however, some will remain unbound as a result of the mis-match between the Si and SiO_2 lattices (Figure 2.6b). Two types of defects are considered [7] to be present in this interface region : fast states which can exchange charge very quickly with free carriers in the silicon and which are located within 1nm of the Si-SiO_2 interface[12], and very slow (effectively fixed charge) states distributed over a region of the oxide some 5 to 10nm from the interface. Many different models [1, 13, 14] have been developed in attempts to explain the origins of these two types of defect states. Although there is no experimental support for any one theory alone, the model described below seems to be supported by many researchers[15, 13,16].

This model considers trivalent silicon defects in the silicon-silicon dioxide interface region which results in an unsatisfied bond[17]. Figure 2.7 shows three possible defects. The Si_s site is considered to be a surface state whilst the others are hole traps; due to its interaction with the silicon surface, the Si_{os} trap is a much slower state and is believed to be the source of the fixed oxide charge.

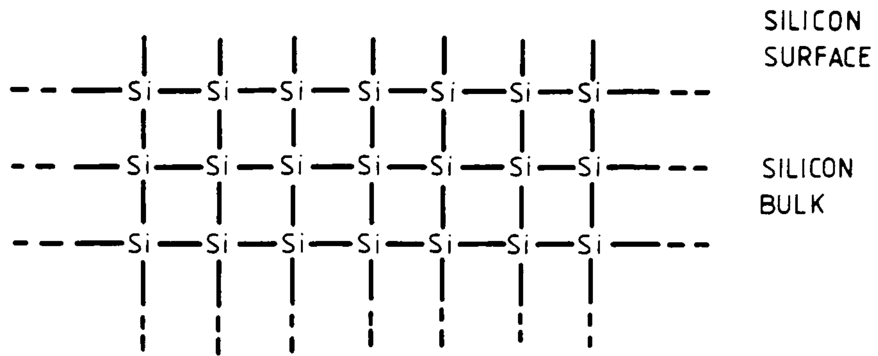


Figure 2.6a : Schematic diagram of silicon surface

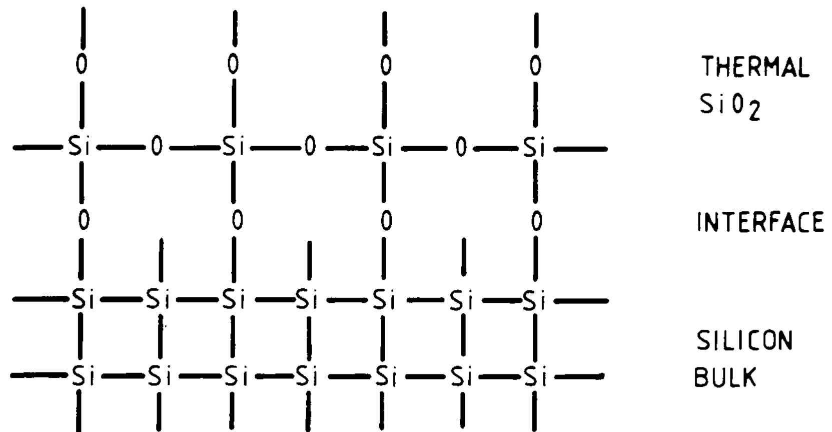


Figure 2.6b : Schematic diagram of the silicon-silicon dioxide interface

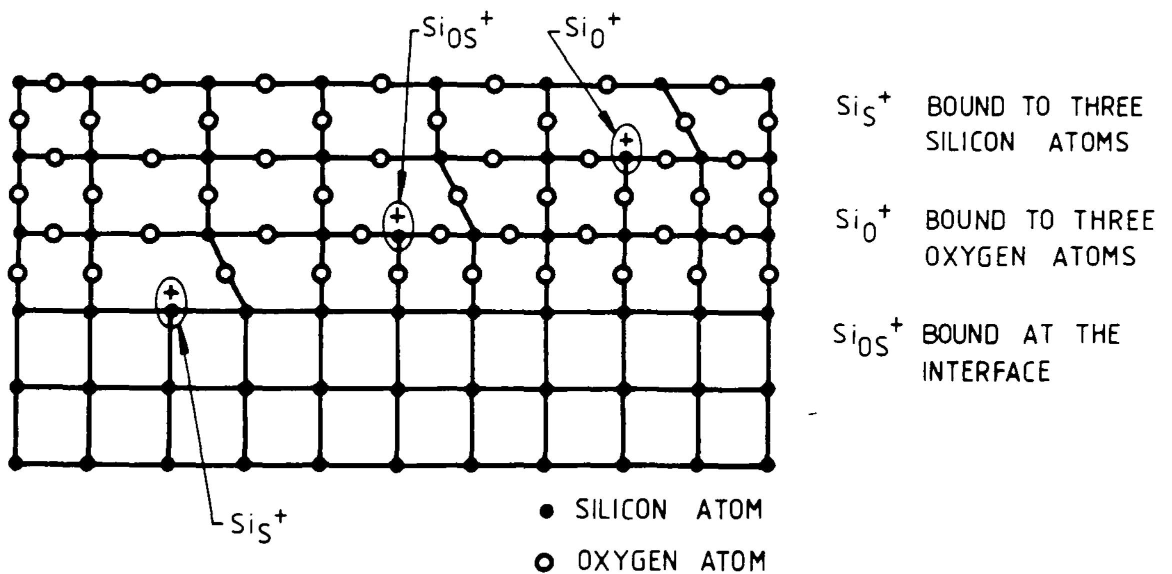


Figure 2.7 : Examples of trivalent silicon defects in the $Si - SiO_2$ interface region

The theory is favoured because of its ability to account for the changes in surface state density observed after low- and high-temperature annealing in hydrogen [7, 15] and due to the results of extensive electron paramagnetic resonance (EPR) studies[16, 18, 19] of the SiO_2-Si interface; the latter research has identified a number of possible defects which are suggested to be responsible for the energy levels observed within the bandgap of the devices.

The number of states present at a silicon - silicon dioxide interface is dependent upon the crystal orientation, since this will determine the number of unsatisfied bonds at the silicon surface prior to oxidation [1]. For example, there are almost twice as many available bonds per unit area in the <111> plane than in the <100> plane[7], and hence the interface state density and oxide charge will be a minimum in devices of <100> orientation.

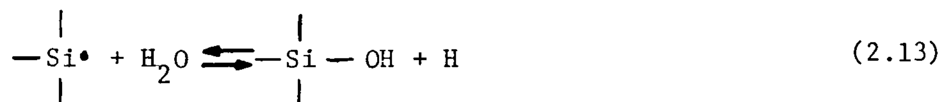
In addition to the intrinsic properties discussed above, a number of external factors will influence the density of states within the SiO_2-Si structure. Dislocations and miscrosplits in the silicon surface, either present in the crystal or introduced during processing (e.g. in diffusion, ion-implanation or wafer-sawing steps), will increase the number of defects [7] in the interface region. It is also believed that increased oxide charge is a result of damange produced by strain or radiation effects [1], or possibly by the introduction of metal impurities which diffuse into the oxide (e.g. during top electrode evaporation). The situation is further complicated by the presence of mobile ions (e.g. Na^+,K^+) in the oxide layer [20, 21]; these are mainly responsible for the instabilities observed [22] in the C-V measurements of SiO_2-Si devices and may also add to the number of surface states [23, 24] and fixed surface charges[2] in the structure if they drift to the SiO_2-Si interface.

The conditions under which the oxide is grown on the silicon surface are critical to the purity of the oxide and to the properties of the interface region. The oxidation processes in ambients of dry oxygen, wet oxygen and steam are described in detail elsewhere[1], but the essential steps in each process are the same. After oxygen has been introduced into the oxide already grown, it must diffuse

through this layer in order to react with silicon at the interface to form SiO_2 [25].

Oxidation in a dry oxygen atmosphere produces the purest oxide, but at low temperatures ($<1000^oC$) the interface state density is high since the reaction rate is slower - consequently, many unsaturated silicon bonds are produced and there is excess oxygen in the oxide. Lower interface state densities may be obtained by high-temperature oxidation ($>1000^oC$) as the faster reaction time will produce SiO_2 predominately. In both cases, a low temperature annealing process is desirable to further reduce interface and oxide charge [1].

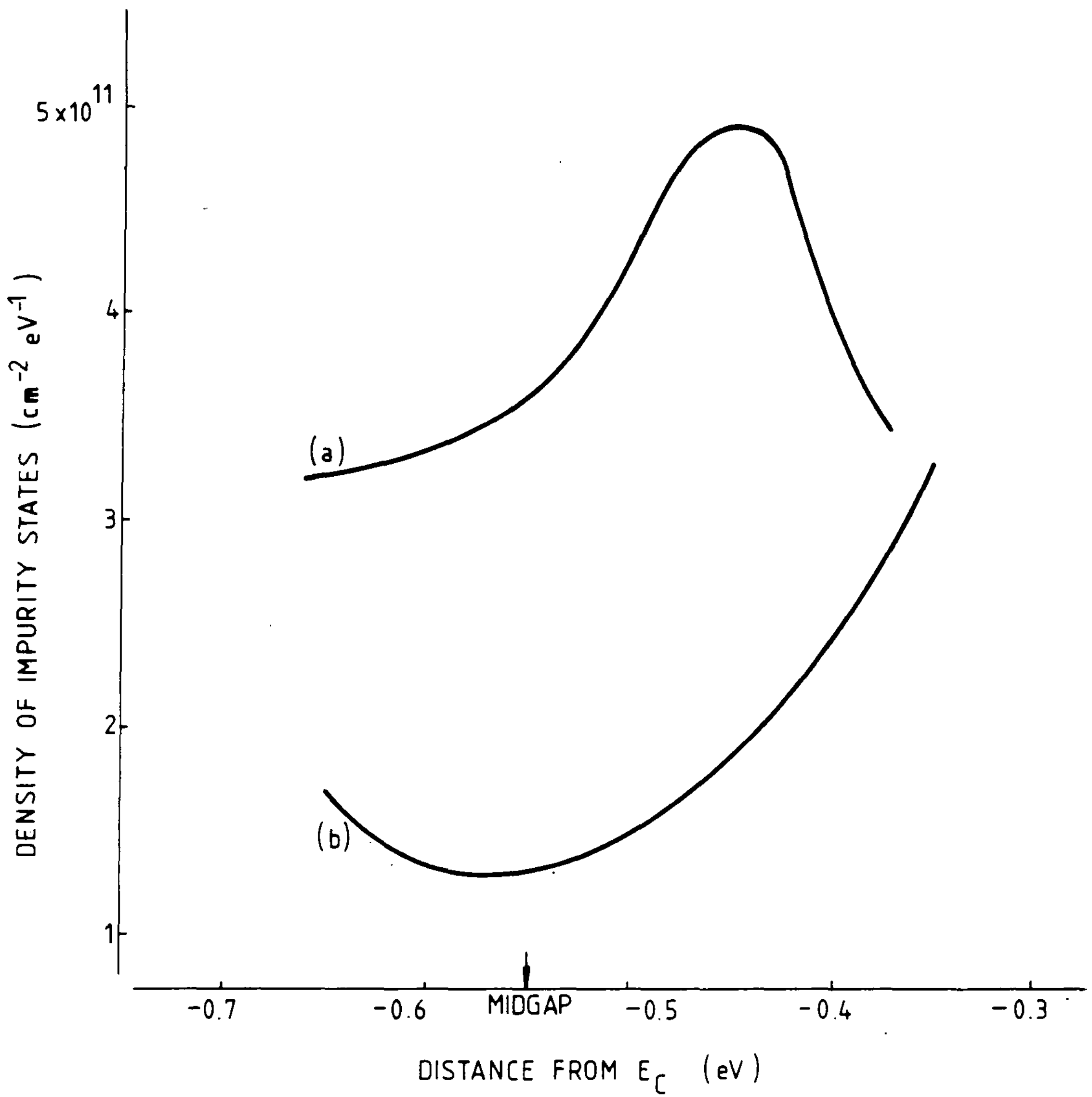
Steam oxidation is a faster process and produces oxides with a greatly reduced number of interface states [26]. As well as leaching out impurities from the oxide and silicon surface, it is believed that water vapour chemically reacts with unsaturated silicon bonds at elevated temperatures. This may be described in terms of the trivalent silicon model discussed above by considering the following reaction:



$$-\overset{|}{\underset{|}{Si}}\bullet + H_2O \rightleftharpoons -\overset{|}{\underset{|}{Si}} - OH + H \qquad (2.13)$$

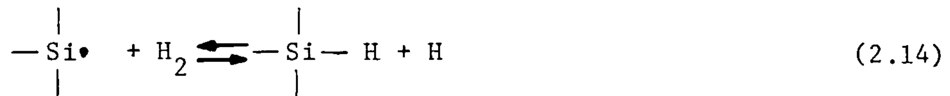
This reaction will decrease the number of dangling bonds by the formation of silanol groups. Oxides grown in this way exhibit a surface state distribution which is of reduced magnitude and U-shaped across the semiconductor bandgap [27]. Figure 2.8 illustrates the effect of annealing on surface state density distribution [28].

The density of interface states produced by either of the oxidation processes mentioned above may be further improved by annealing in the presence of hydrogen; for an oxide grown in dry oxygen this will also result in the characteristic U-shaped distribution mentioned above [1,29]. Again considering the trivalent silicon model, a similar chemical reaction to (2.13)



<u>Figure 2.8 : Surface state distribution of a typical MOS device</u>

may be envisaged when heating in a hydrogen atmosphere:



$$-\overset{|}{\underset{|}{Si}}\bullet + H_2 \rightleftharpoons -\overset{|}{\underset{|}{Si}}- H + H \qquad (2.14)$$

In this case the unsatisfied Si bond is effectively neutralised by capturing a hydrogen atom. The oxide charge always decreases during an annealing process regardless of the temperature. However, the interface state density will only be reduced if the annealing temperature is below about 500°C; above this temperature the hydrogen bond of the above reaction is split and an increase of surface state density occurs.

The shape of the interface state density curve is attributed to the different types of defect found at different energy levels in the bandgap. The density of states at the band edges is due to bond distortion and strain near the silicon surface[11] and these are not affected by a post-oxidation anneal. The mid-gap surface state density, however, is affected by this process; dangling bond defects are responsible for states in this region[30], and these may be significantly reduced in number by hydrogen annealing, hence producing the characteristic U-shaped distribution.

So far, the discussion has been limited to the possible origins and types of defects found within the metal-insulator-semiconductor system. In the next two sections, the effects of these impurities on the electrical properties of the structure will be considered. The first part (section 2.2.2) will describe the effects of insulator charge and the second (section 2.2.3) the influence of states at the insulator-semiconductor interface.

2.2.2 Electrical effects of charges in the insulator

Impurities in the insulating layer are due to insulator trapped charge, mobile ionic charge and fixed surface charge as demonstrated in figure 2.5. These parameters will change the electrical behaviour of a metal-insulator-semiconductor device; the specific case of a metal $-SiO_2-S_i$ structure is discussed below.

Charge trapped in the SiO_2 insulating oxide layer is a result of defects present in the oxide. These defects may result in energy levels in the Si bandgap which can trap electrons or holes injected into the oxide (e.g. from the gate electrode, from the semiconductor or from electron-hole excitation), as detailed elsewhere[31]. As the charge held in these trapping centres will be constant provided that no carrier injection takes place, the only effect on the electrical characteristics of the MOS capacitor will be a lateral voltage shift (Figure 2.9a). If charge injection does occur, however (e.g. as a result of illuminating the sample, or by biasing the device into strong accumulation or inversion), then a hysteresis [20] in the measured response will be observed; i.e. the C-V characteristcis recorded with a positive voltage ramp will be shifted with respect to the curve obtained with a negative voltage ramp, as the amount of trapped charge will be different (Figure 2.9b).

The presence of mobile ions [23, 32, 33] in the oxide will also cause a hysteresis in the measured C-V curves[21]. This instability is due to alkali ions (Na^+, K^+) which are usually trapped at the SiO_2-Si interface but which may drift freely at elevated temperatures or under the influence of an applied electric field. Other ions (e.g. H^+ protons[34]) may also cause drifting effects. The change in charge distribution within the oxide again produces a shift in the flat-band voltage [22].

Fixed surface charge is generally positive and is located in a region of the oxide less than 25Å from the SiO_2-Si interface. This charge is affected only by the sample processing techniques and results in a permanent contribution to the flat-band voltage.

The total voltage shift of the C-V curves due to the three types of oxide charge discussed above may be written as[6]

$$V = - \frac{1}{d_{ox} C_{ox}} \int_{o}^{d_{ox}} x \cdot \rho(x) \, dx = - \frac{\bar{x} Q_o}{d_{ox} C_{ox}} \qquad (2.15)$$

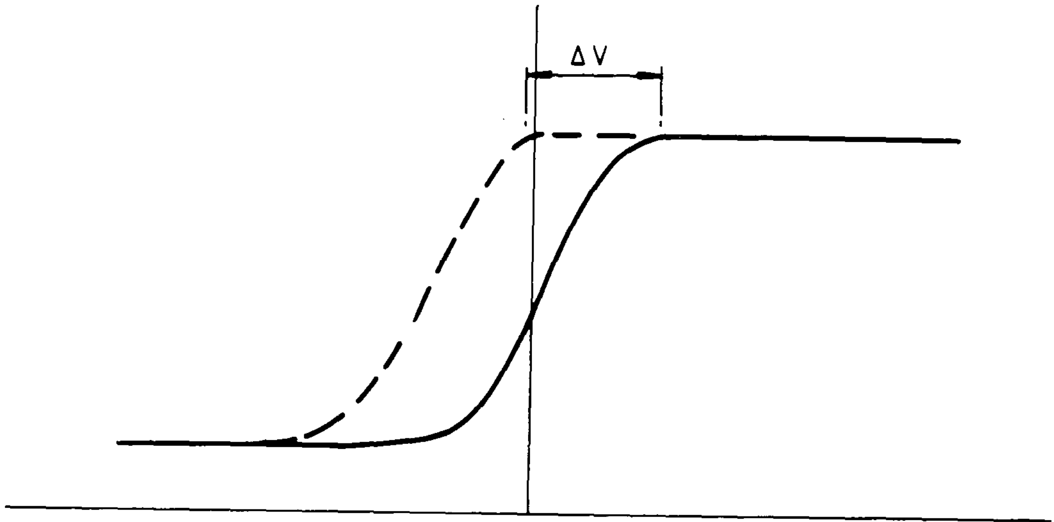


Figure 2.9a : Example of C-V curve showing lateral voltage shift due to flat-band voltage change (high frequency case)

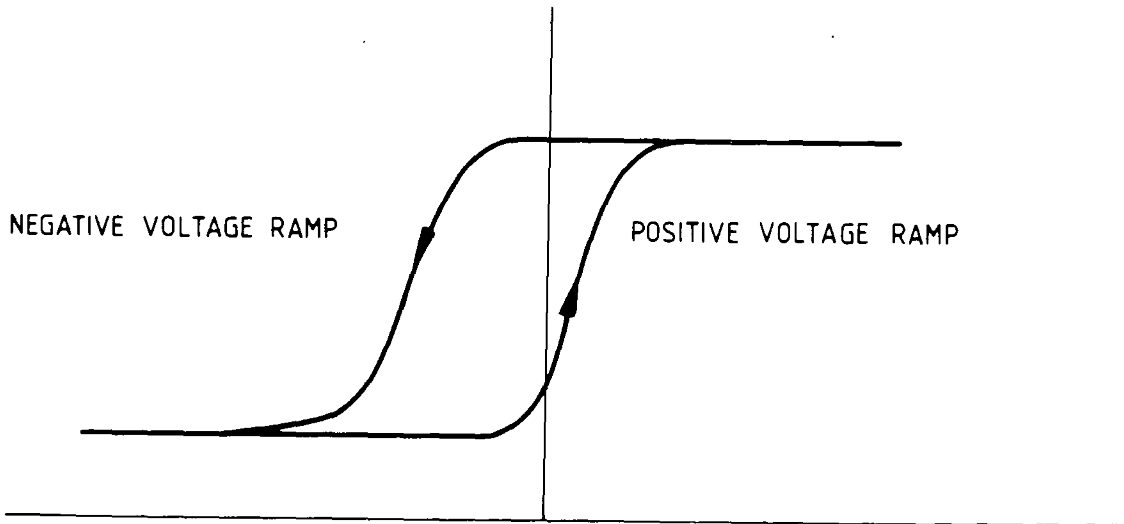


Figure 2.9b : Example of C-V curve illustrating possible hysteresis effect (high frequency case)

where d_{ox} is the oxide thickness and $\rho(x)$ represents the charge density distribution. Q_o is the total oxide charge due to trapped charge Q_t, mobile ionic charge Q_i, and fixed surface charge Q_f, such that

$$Q_o = Q_t + Q_i + Q_f = \int_0^{d_{ox}} \rho(x)\, dx \qquad (2.16)$$

and $\bar{x}$ is the position of the effective charge centroid, i.e.

$$\bar{x} = \frac{1}{Q_o} \int_0^{d_{ox}} x.\, \rho(x)\, dx \qquad (2.17)$$

These equations may also be applied to multi-layer insulators, e.g. Langmuir-Blodgett films (see chapters 7 and 8).

Equation 2.11a must now be modified thus:

$$Vapp = V_{ox} + \psi_s + \phi_{ms} - \frac{\sigma t}{\varepsilon_{ox}} - \frac{\bar{x}Q_o}{d_{ox}C_{ox}} \qquad (2.18)$$

and the flat-band voltage becomes:

$$V_{FB} = \phi_{ms} - \frac{\sigma t}{\varepsilon_{ox}} - \frac{\bar{x}Q_o}{d_{ox}C_{ox}} \qquad (2.19)$$

This additional term can in practice be greatly reduced by careful device processing to give lower fixed surface charge and fewer mobile ions in the oxide, and by controlling the conditions of device storage and measurement to reduce trapped charge (e.g. preventing charge injection by avoiding elevated temperatures, illumination and large bias voltages). However, as Q_o may change due to the factors indicated above, flat-band voltage will be a function of device history and consequently there may be slight variations in

V_{FB} over a period of time.

2.2.3 Electrical behaviour of interface traps

The presence of trapping sites at or near the insulator-semiconductor interface creates allowed energy levels with the semiconductor bandgap; these levels may exchange charge with the conduction (valence) band by capture or emission of electrons (holes). Donor-type states will exhibit positive or neutral charge when empty or filled respectively, acceptor-type states will be neutral or negatively charged under like conditions. The occupation of interface states in thermal equilibrium is determined by the Fermi-Dirac function;

$$f(E) = \left[1 + g.\exp\left((E-E_F-q\psi_s)/kT\right) \right]^{-1} \qquad (2.20)$$

where f(E) is the probability that a state at energy level E is occupied by an electron, and g is the spin correction factor (usually 2 for donor and 1/4 for acceptor-type states). Figure 2.10 depicts the energy band diagram at the insulator/semiconductor interface region.

Changes in the occupancy of interface traps can be achieved by varying the applied bias voltage and hence the surface potential, ψ_s. Consequently, a small ($\sim kT/q$) a.c. voltage applied to the device will modulate the position of the Fermi level which will cause majority carriers to be captured or emitted by interface states whose energy levels lie within a few kT/q of E_F. As this capture/emission phenomenon is not infinitely fast, there will be a time delay associated with the exchange process. This will be manifested as an energy loss at all but very low and very high signal frequencies (under which conditions all or none of the interface traps respond to the applied signal, respectively) and contributes to the ohmic losses observed in non-ideal MIS structures.

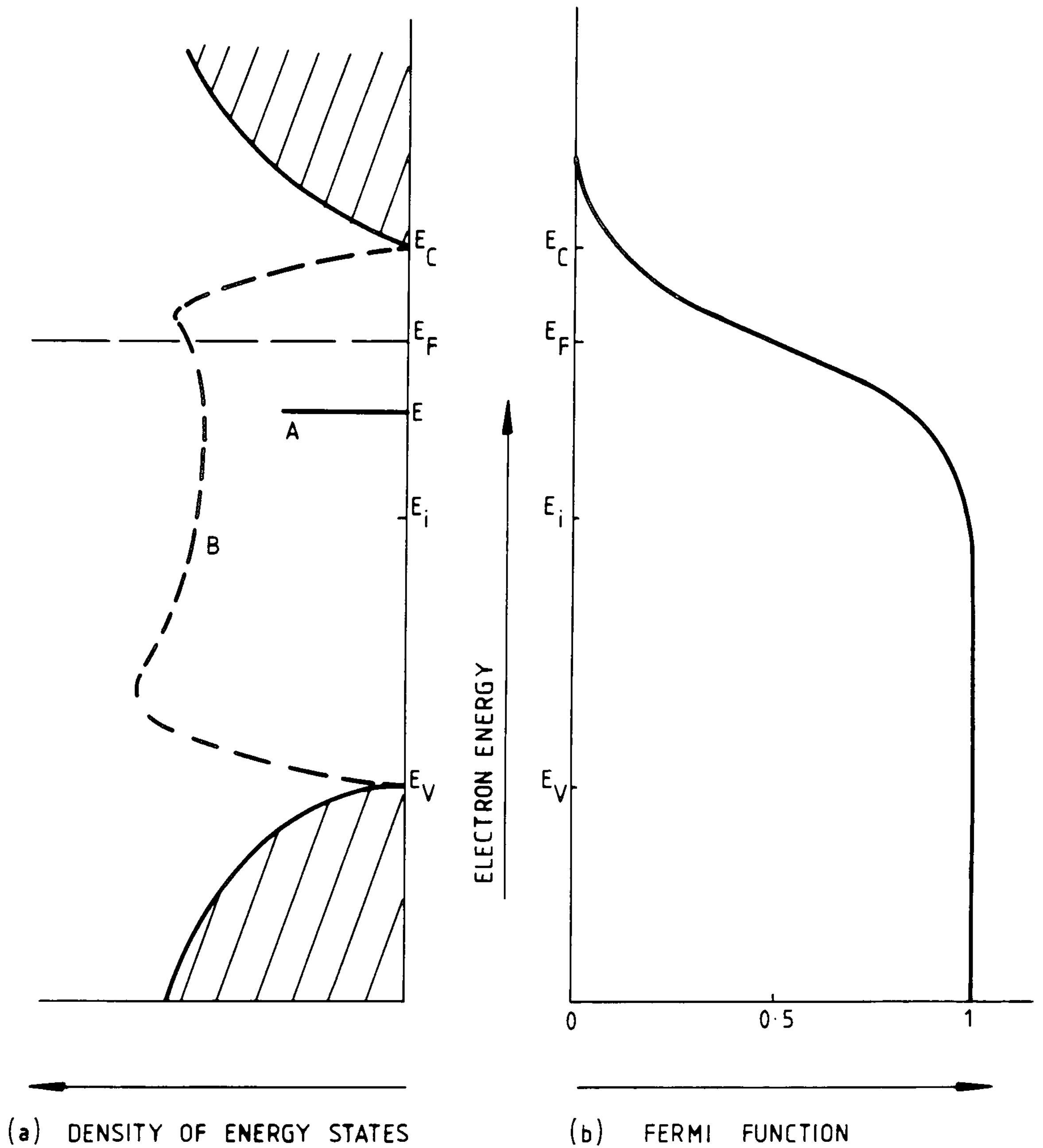


Figure 2.10 : Energy band diagram at the insulator - semiconductor interface

(a) Density of energy states across bandgap
A ≡ single level state of energy E
B ≡ continuum of states

(b) Probability of electron occupancy across bandgap

The effects of interface charges on the C-V curve discussed in the previous sections are manifold. The capacitance will be increased by one elementary charge per state and so, therefore, will the lateral voltage shift, i.e.

$$V_{app} = V_{ox} + \psi_s + \phi_{ms} - \frac{\sigma t}{\varepsilon_{ox}} - \frac{\bar{x}\, Q_o}{d_{ox} C_{ox}} - \frac{Q_{ss}}{C_{ox}} \qquad (2.21)$$

and

$$V_{FB} = \phi_{ms} - \frac{\sigma t}{\varepsilon_{ox}} - \frac{\bar{x} Q_o}{d_{ox} C_{ox}} - \frac{Q_{ss}}{C_{ox}} \qquad (2.22)$$

where Q_{ss} is the total charge introduced by interface traps. This charge (and hence the additional capacitance term) is strongly dependent upon surface potential and so also upon applied bias; when the Fermi level is at the energy of the trap its effect will be maximised. Furthermore, the electric surface field itself is changed by the interface charge and more applied voltage is required to create the same amount of band-bending as in the ideal case. These effects are observed as a shift, a distortion and a stretching-out in the measured C-V curves.

A quantitative explanation of the electrical influences of interface traps can be obtained by considering first the admittance of a single-level state and expanding the treatment to the continuous distribution of states across the bandgap observed in real devices. Finally surface potential fluctuations will be discussed.

The admittance of the single-level state for small signal conditions may be written as[27]

$$Y_{SL}(E) = \frac{j\omega q^2}{kT} \; \frac{N_{SL} f_o (1-f_o)}{(1+j\omega f_o / c_n n_{so})} \qquad (2.23)$$

where ω is the angular frequency of the applied signal, N_{SL} is the single-level state density, f_o is the value of the d.c. Fermi function, c_n is the electron capture rate, and n_{so} the electron density at the surface.

This admittance may be considered as a parallel combination of capacitance C_s and conductance G_p such that:

$$C_s = C_{SL} / (1 + \omega^2 \tau_n^2) \qquad (2.24)$$

and

$$G_p/\omega = C_{SL}\, \omega \tau_n / (1 + \omega^2 \tau_n^2) \qquad (2.25)$$

where the capacitance C_{SL} and the time constant τ_n associated with the single-level state are given by

$$C_{SL} = q^2 N_{SL} f_o (1-f_o)/kT \qquad (2.26)$$

and

$$\tau_n = f_o / c_n n_{so} \qquad (2.27)$$

The electrical equivalent of the total system in depletion is given in figure 2.11a; the interface and space-charge region terms may be reduced to a single parallel circuit as shown in figure 2.11b, where:

$$C_p = C_s + C_D \qquad (2.28)$$

It can be seen from equation 2.25 that G_p/ω will be a maximum when $\omega\tau_n = 1$, and that this maximum will be

$$(G_p/\omega)_{max} = C_{SL}/2 \qquad (2.29)$$

A typical plot of C_s and G_p/ω versus frequency for this single-level case is given in figure 2.12. Knowing the value of $(G_p/\omega)_{max}$

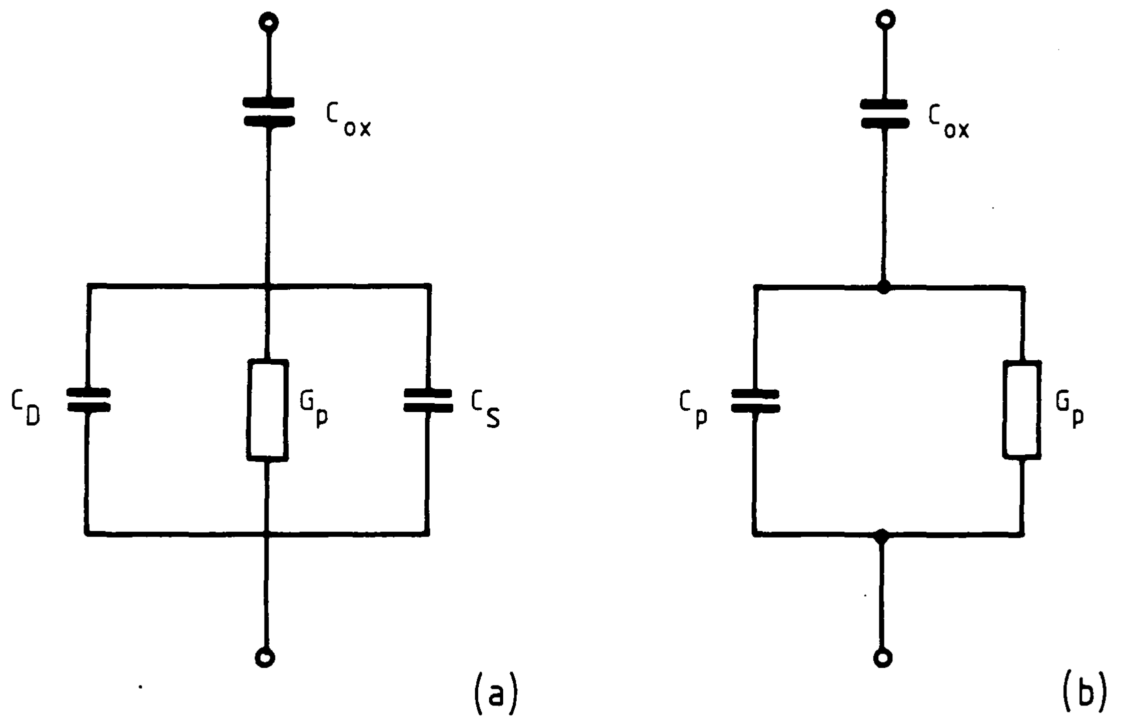


Figure 2.11 : Equivalent circuits of a MIS device in depletion

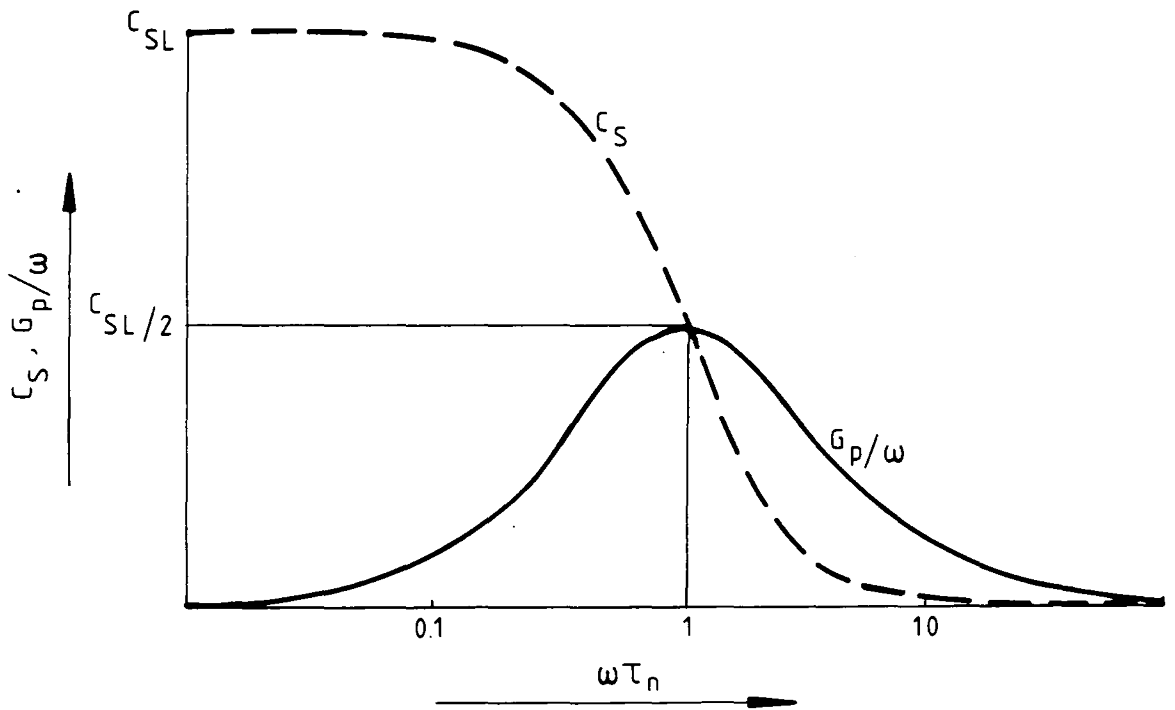


Figure 2.12 : Example of C_s, G_p/ω versus frequency for single-level model

and the corresponding surface potential, N_{SL} may be calculated (from equation 2.26) for the energy level.

It is more realistic in practice to consider the case of a continuous distribution of energy states across the bandgap[35], each of which may be individually described as above. The total admittance of this arrangement, Y_{ss}, may be derived by integrating Y_{SL} over the whole range of trap energies in the bandgap:

$$Y_{ss} = \int_{E_v}^{E_c} Y_s(E)\,dE = \frac{j\omega q^2}{kT} \int_{E_v}^{E_c} \frac{N_{ss} f_o (1-f_o)}{1+j\omega f_o / c_n n_{so}} \, dE \qquad (2.30)$$

The result [27] may be expressed, as before, as a parallel conductance and capacitance network, where:

$$C_S' = q \, N_{ss} \arctan (\omega\tau_m) \qquad (2.31)$$

and

$$(G_p/\omega)' = q \, N_{ss} \; \ln (1 + \omega^2 \tau_m^2) \; / \; 2\omega\tau_m \qquad (2.32)$$

$$\tau_m = 1 / \bar{c}_n n_{so} \qquad (2.33)$$

This procedure is only valid if N_{ss} (the density of distributed interface states per electron volt) and $\bar{c}_n$ (the average capture probability over the range of the integral) are not greatly varying functions of surface potential, i.e they may be treated as constants over a range of a few kT/q. This is generally true for most practical systems provided that the amplitude of the applied signal is small ($\sim$kT).

From equation 2.32 it can be calculated that the maximum G_p/ω will occur at $\omega\tau_m = 1.98$.

Figure 2.13 [27] compares the normalised G_p/ω versus ω curves for the single-level state model (curve (a)) and the continuous model (curve (b)). In practice, however, a response similar to that shown in curve (c) is obtained, where the G_p/ω maximum is found at $\omega\tau = 2.5$. This broadening of the response is attributed [7] to fluctuations in the surface potential caused by lateral variations in the electric field due to ionized charge or localised oxide charge near the interface region and/or oxide thickness non-uniformities. Several models account for this [27, 11, 20, 36] and derive expressions for the device admittance which may only be solved by numerical techniques.

The equivalent circuits described above are valid for the device when biased in the depletion region. A more comprehensive model has been developed by Lehovec and Slobodsky [37] which describes the inversion and accumulation regions also. However, it will be seen later (Chapter 3) that by using numerical analysis techniques, the simple model discussed above is sufficient as the devices to be investigated will be biased in the depletion region only.

2.3 Summary

This chapter has described the electrical properties of real metal-insulator-semiconductor devices by first explaining the behaviour of an ideal MIS capacitor and then considering the effects of charges introduced by defects in the structure. The nature and origin of these charges have been related to the observed electrical characteristics. The metal-SiO_2-Si system has been given specific attention because this is the strucutre of samples investigated in this work and also because it is the most common example of a MIS device. However, the principles discussed above may equally well be applied to many other combinations of insulator and semiconductor which are currently of interest. [38]

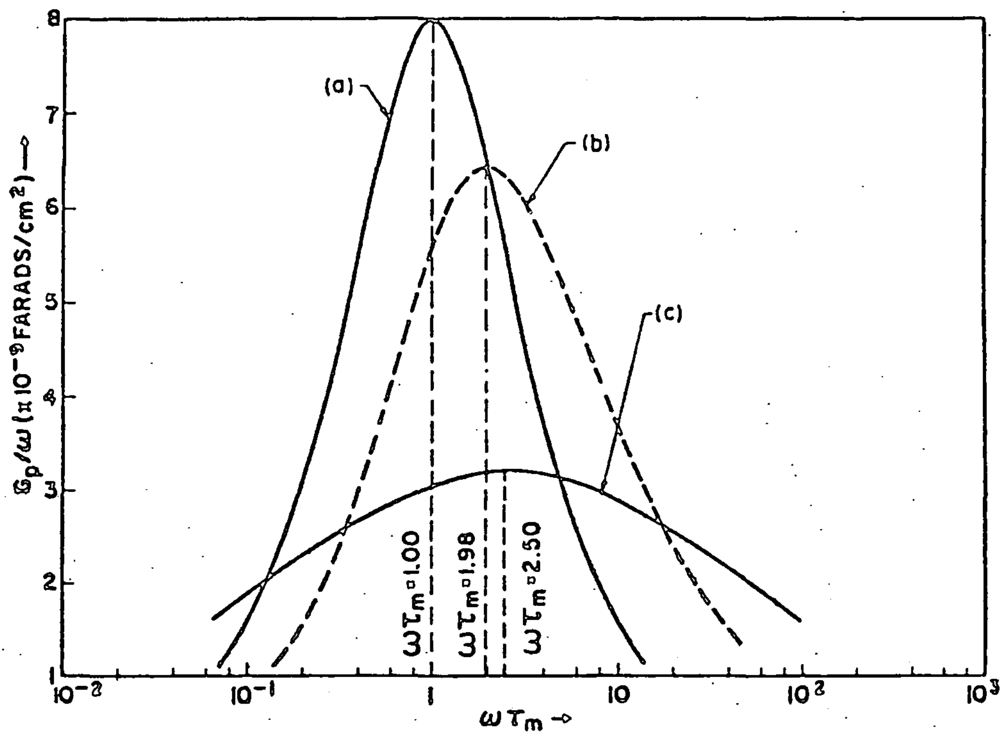


Figure 2.13 : Calculated G_p/ω curves versus log $\omega\tau_m$

(a) single-level state

(b) continuum of states

(c) response with surface potential fluctuations

In the next chapter, the evaluation of MIS device properties from measured electrical data and some of the methods used to extract this information will be described. In particular, experimental techniques which may be used to analyse the interface state density distribution across the semiconductor bandgap will be considered.

CHAPTER 3 : CHARACTERISATION OF MIS DEVICES

3.0 Introduction

The electrical behaviour of metal-insulator-semiconductor devices has been examined in chapter 2 along with the physical properties responsible for this behaviour.

In this chapter, the idea of plotting capacitance and conductance with respect to voltage and frequency will be more fully discussed, especially the use of this technique for measurement of MIS device parameters such as flat-band voltage, insulator trapped charge and doping density. Various methods to calculate interface state density distribution will be considered; in particular, the a.c. conductance technique and its application to measurement of real MIS devices are described.

3.1 Electrical Characterisation of MIS Structures

From the data gathered in a single capacitance-voltage scan performed on an MIS sample, a large amount of information may be extracted about the electrical properties of the device. This procedure may be repeated after a period of time or after a sample treatment operation, say, in order to determine the electrical effects of aging or of the treatment process.

The following three sections (3.1.1, 3.1.2, and 3.1.3) show how C-V plots may be used to calculate flatband voltage, insulator charge, and doping density; section 3.1.4 discusses the procedure for determing the dielectric permittivity of the insulator layer, and finally the experimental apparatus used for C-V measurement and insulator permittivity calculation is outlined (section 3.1.5). All of these analysis techniques are utilised for characterising the devices investigated later in this work.

3.1.1 Flat-band voltage calculation

In the flat-band condition the insulator-semiconductor surface is depleted of majority carriers, and the equivalent circuit is given by a series combination of insulator and depletion capacitances as shown for the metal-SiO_2-Si system in chapter 2 (section 2.1.2).

The oxide capacitance, C_{ox}, may be found from the C-V plot by calculating the value of capacitance measured in strong accumulation. The depletion capacitance is given by equations 2.9 and 2.4a:

$$C_{D(fb)} = \left(\frac{\varepsilon_s A^2 q^2 N_d}{kT} \right)^{\frac{1}{2}} \tag{3.1}$$

The parameters ε_s, q, N_d, k and T are as defined in chapter 2, but the additional A^2 term is introduced to relate the depletion capacitance to the device top contact area, A.

From equation 2.6, the value of measured capacitance at the flat-band point is:

$$C_{fb} = \frac{C_{ox}\, C_{D(fb)}}{C_{ox} + C_{D(fb)}} \tag{3.2}$$

By calculating the value of C_{fb} for a particular sample and determining the point on the C-V curve at which it occurs, the flat-band voltage V_{FB} may be obtained (figure 3.1). This procedure may be applied to any MIS combination by inserting the appropriate electrical constants into equation 3.1.

3.1.2 Determination of insulator charge

The total amount of charge incorporated in a MIS device can be determined from equation 2.19 if the flat-band voltage is calculated as shown in section 3.1.1. By using a technique known as

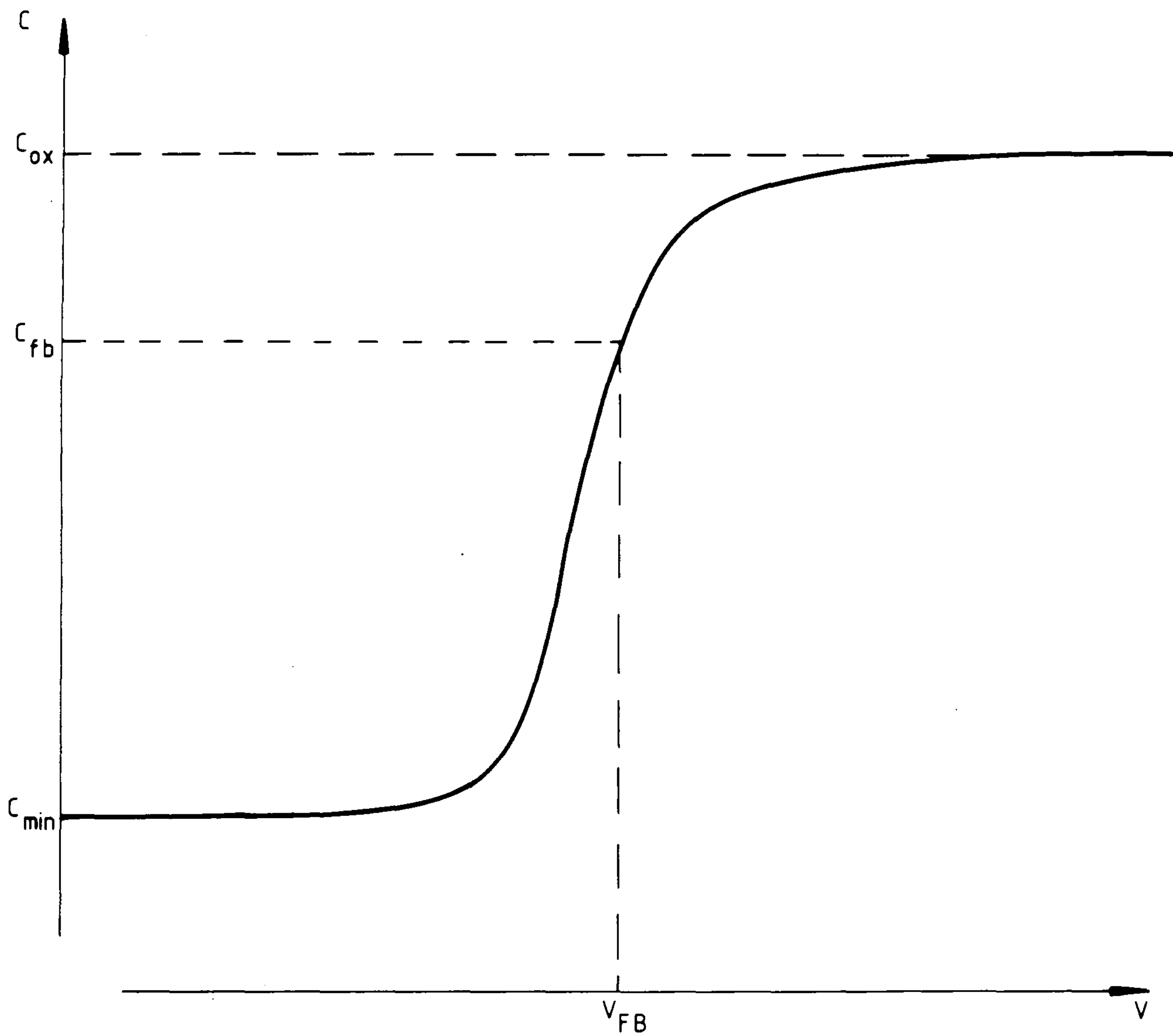


Figure 3.1 : Determination of V_{FB} from plot of measured capacitance versus bias voltage (high frequency case)

Bias-Temperature Stressing [1, 2], information about the components of the insulator charge can be obtained from the hysteresis effects on the C-V curve. The procedure is to bias the device into inversion at elevated temperature for some minutes, after which a C-V scan is performed. The sample is then held in strong accumulation (again at elevated temperature) for a similar length of time before repeating the C-V measurement. The two resulting curves are plotted as in figure 3.2 (n-type device). Curve (a) shows the C-V response after application of a negative voltage (inversion) when all mobile (positive) ionic charges have drifted to the metal-oxide interface; in this condition there is no contribution to the flat-band voltage ($x = 0$ in equation 2.15). Curve (b) denotes the C-V characteristics after biasing in accumuation (positive applied voltage) when all the mobile charges are at the insulator-semiconductor interface; the flat-band voltage shift will be a maximum (as $x = d_{ox}$ in equation 2.15):

$$\Delta V_i = \frac{-Q_i}{C_{ox}} \tag{3.3}$$

Hence the value of Q_i may be determined.

It is generally found that curves 3.2(a) and 3.2(b) differ by no more than 0.1V as the number of mobile ions is very low for modern processing techniques [3]. However, analysing C-V curves in this way can indicate sample quality and is used as a standard process monitoring technique. Other researchers have shown how this method can be used to investigate trapping effects [4] and polarisation of the insulator [5]. In addition, any changes in insulator charge introduced by subsequent device treatment can be observed by the effect upon flat-band voltage.

The main contribution to the flat-band voltage shift from the "ideal" case is the oxide fixed charge, Q_f. If the number of ionised traps is small, and assuming that there are no dipole layers of charge in the insulator, then Q_f may be calculated from equations 2.16 and 2.19:

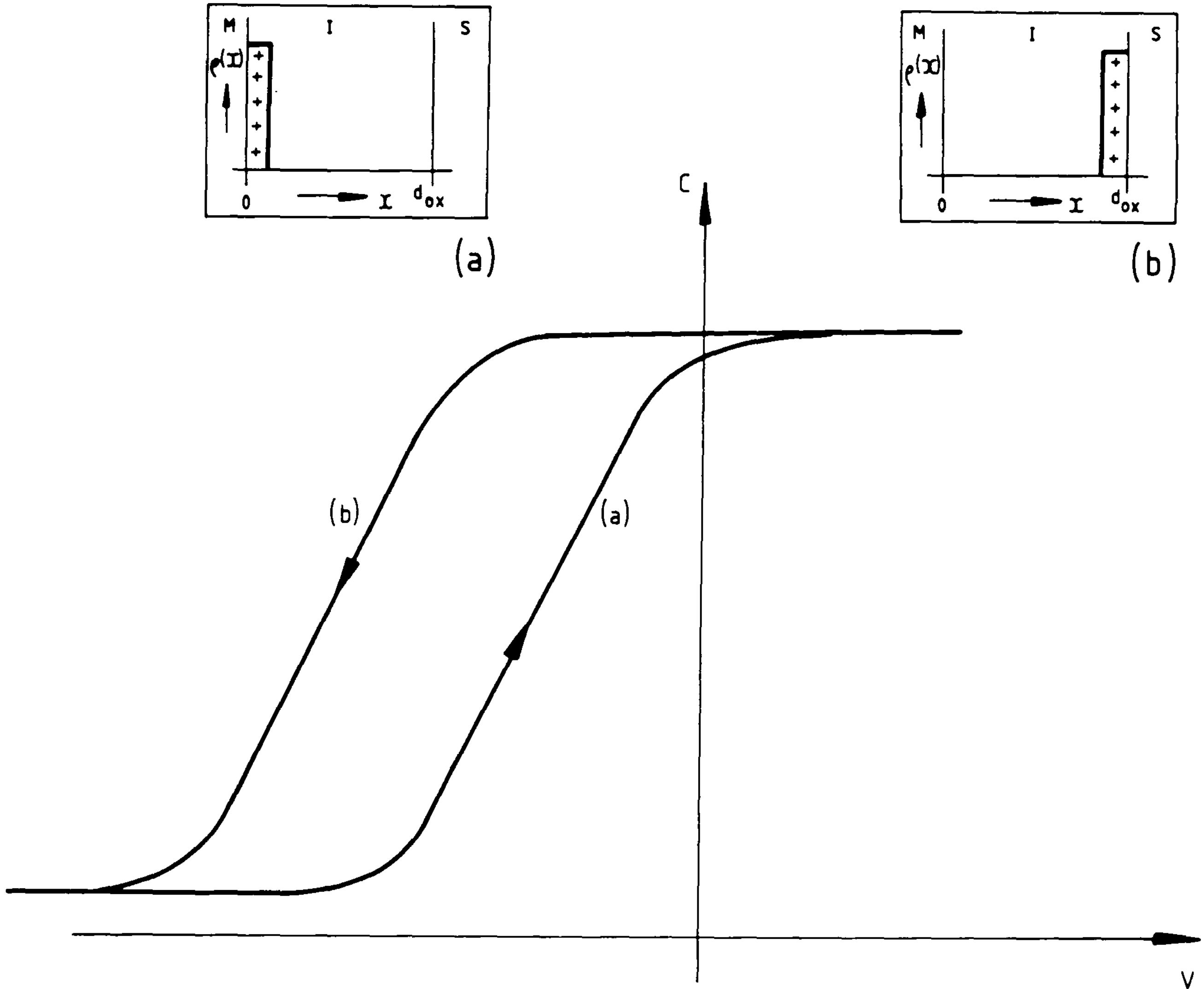


Figure 3.2 : Schematic plot of hysteresis effect on high frequency C-V curve due to mobile ionic charge (insets show position of charge in MIS structure)

$$V_{FB} = \phi_{ms} - \frac{Q_f}{C_{ox}} \quad (3.4)$$

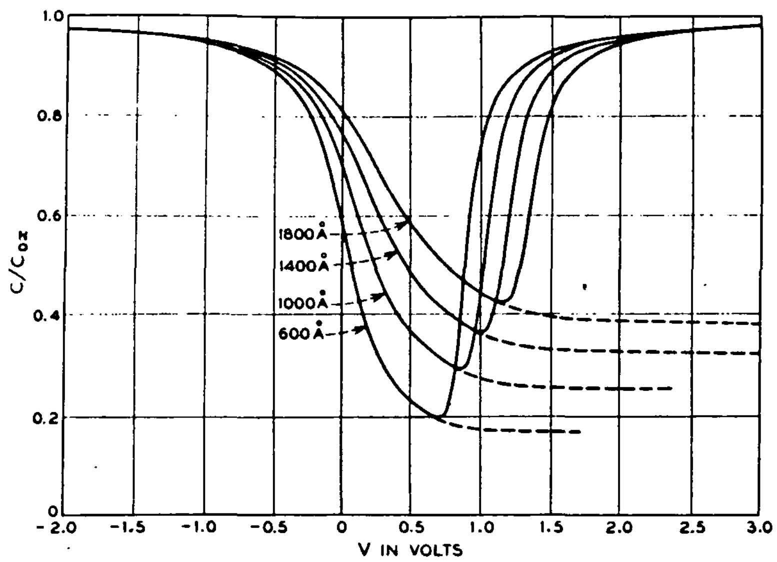
In practice, this calculation will not be exact due to the other charges present, but although these cannot be totally ignored their effect will be small and so a reasonable approximation to Q_f can be obtained.

It should also be noted that in the above calculations no allowance is made for the effects of interface states. The interface state charge can be determined by other means (see section 3.2) and the Q_{ss} term in equation 2.22 removed, enabling Q_i and Q_f to be obtained as above.

3.1.3 Calculation of doping concentration

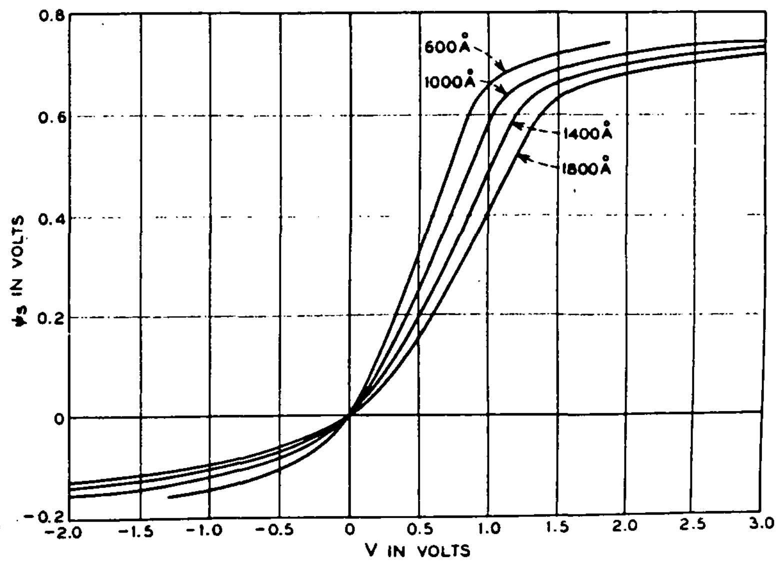
The doping impurity density within the semiconductor must be known for the region near the insulator-semiconductor interface in order to calculate the MIS device parameters. An average doping concentration can be determined from a high-frequency C-V plot [6] by measuring the minimum capacitance C_{min} which occurs in the inversion region as described in chapter 2 (section 2.1.2). Curves have been computed which relate capacitance, surface potential, applied voltage, oxide thickness and doping concentration for the metal-SiO_2-Si system [6, 7]; similar curves may be obtained for other insulator-semiconductor combinations. An example of these plots [7] is shown in figure 3.3 for p-type silicon (conversion to n-type silicon is achieved by reversing the voltage axes). If the oxide thickness is known, the doping density, N_d, can be calculated by measuring C_{min} and C_{ox}, the oxide capacitance (see figure 3.1), and reading from a set of curves such as figure 3.3c the value of N_d which corresponds to the C_{min}/C_{max} ratio thus determined.

An alternative evaluation of N_d is given by examining the high frequency C-V curve in a different way. When a bias voltage V is applied to a MIS device in depletion, equation 2.10 becomes:



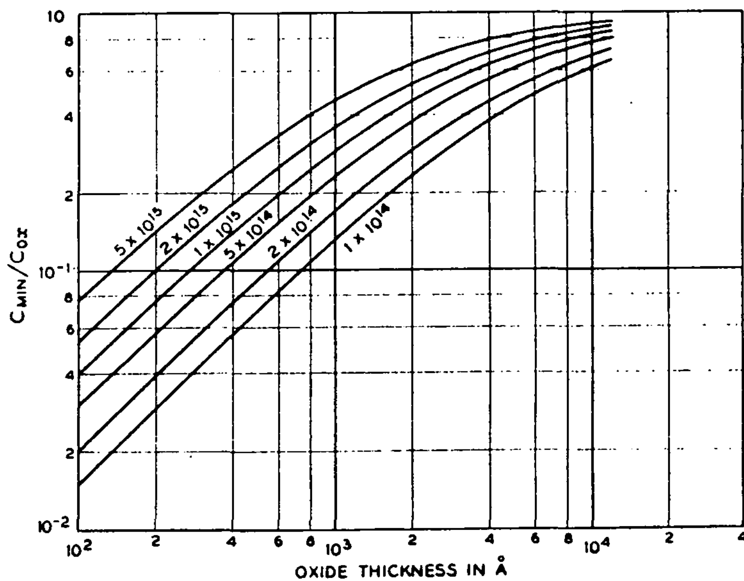
MOS capacity vs voltage. Oxide thickness 600–1800 Å. ($N_A = 1.0 \times 10^{15}$ cm^{-3})

Figure 3.3a



Surface potential vs voltage. Oxide thickness 600–1800 Å. ($N_A = 1.0 \times 10^{15}$ cm^{-3})

Figure 3.3b



Minimum capacity vs oxide thickness. Doping density as parameter 1×10^{14}–5×10^{15} cm^{-3}.

Figure 3.3c

$$C_D = \left(\frac{qN_d \varepsilon_s A^2}{2(\psi_s + V - kT/q)} \right)^{\frac{1}{2}} \tag{3.5}$$

or

$$\frac{1}{C_D^2} = \frac{2}{qN_d \varepsilon_s A^2} (V + \psi_s - kT/q) \tag{3.5a}$$

and the doping concentration may be extracted from the slope of a plot of $1/C_D^2$ versus V. (C_D is obtained from the measured capacitance C by using equation 2.6a). This treatment can be extended to obtain impurity profiles for non-uniformly doped semiconductors and to correct for the effects of interface states [(8)]; however, the average value of N_d as determined above is sufficient for most practical calculations of MIS device characteristics.

3.1.4 Insulator permittivity

Information on the electrical properties (such as dielectric constant) of SiO_2 and other commonly-used insulators is readily available in textbooks and tables of constants. However, when a novel insulating material is incorporated into a MIS device, it is necessary to calculate these values experimentally, as they are often required for determination of other device parameters. The simplest structure for effecting measurements on an insulator is a metal-insulator-metal (MIM) "sandwich" which can be fabricated by depositing a film of the insulating material onto a metal and then evaporating a metal top electrode.

The electric permittivity, ε, of the insulating layer may be obtained from measurement of the MIM device capacitance, C, as

$$C = \frac{A\varepsilon}{d} = \frac{A\varepsilon_r \varepsilon_o}{d} \tag{3.6}$$

where A is the device area and d the thickness of the insulating layer. The absolute permittivity of the insulator is generally expressed as the product $\varepsilon_r\varepsilon_o$, where ε_o represents the permittivity of free space and ε_r is a constant for the material which is known as the relative permittivity or the dielectric constant.

To determine the relative permittivity accurately a number of capacitance measurements should be carried out on MIM structures of different insulator thickness. Plotting C against 1/d should give a straight line of slope $A\varepsilon_r\varepsilon_o$ passing through the origin. In the case of Langmuir-Blodgett film insulators (which are discussed in chapters 7 and 8), where the insulating layer can be built up in multiples of a monolayer thickness, equation 3.6 may be rearranged and rewritten as:

$$\frac{1}{C} = \frac{Nd_i}{A\varepsilon_r\varepsilon_o} \qquad (3.7)$$

Here, N is the number of monolayer of thickness d_i deposited onto the metal electrode. A plot of 1/C against N will give ε_r (in this case the straight line slope is $d_i/A\varepsilon_r\varepsilon_o$).

In some plots of 1/C versus N (or d) for MIM devices a non-zero intercept may be recorded. This is often due to oxidation of the surface of the deposited metal electrodes resulting in the formation of a region of metal oxide (e.g. Al_2O_3 on Al electrodes). As a consequence, the apparent insulator thickness is increased by a constant amount which contributes an extra series capacitance; modifying equation 3.7 for this effect, we find

$$\frac{1}{C} = \frac{Nd_i}{A\varepsilon_r(i)\varepsilon_o} + \frac{d_{mo}}{A\varepsilon_r(mo)\varepsilon_o} \qquad (3.8)$$

where $\varepsilon_r(i)$ is the relative permittivity of the LB film insulator, $\varepsilon_r(mo)$ is the value of ε_r for the metal oxide and d_{mo} is the thickness of the metal oxide. It can be seen that the slope of the 1/C - N line will be unchanged, enabling $\varepsilon_r(i)$ to be calculated as before.

In addition, the thickness of the metal oxide layer may be determined from the value of the intercept with the 1/C axis if $\varepsilon_r(mo)$ is known (since at this point $d_i = 0$). A typical 1/C - N characteristic for a metal - LB film - metal structure is shown to illustrate this feature (figure 3.4).

The technique for evaluating the dielectric constant of an insulating layer has so far been applied only to a MIM structure. However, should it not be possible to fabricate such a device, experiments may be carried out on a MIS structure biased into strong accumulation (under this condition, just the insulator capacitance will be measured, as there will be no depletion region), and $\varepsilon_r(i)$ determined as above.

3.1.5 Experimental equipment

Capacitance-voltage plots are obtained by the method outlined in section 2.1.2 in which the sample is perturbed by a small a.c. signal whilst applying a d.c. voltage ramp. By using a phase-sensitive detector the a.c. admittance of the device may be measured and resolved into its capacitive and conductive components, and hence the C-V and G-V characteristics determined. An automated experimental system was especially developed to facilitate the recording of these and other parameters and is fully described, along with details of the measurement technique, in the next two chapters.

The procedure for calculating the insulator permittivity is to measure the capacitance of a number of MIM devices with different thicknesses of insulator; figure 3.5 is a schematic diagram of the equipment used for this purpose. The Boonton model 72BD Capacitance Meter displays capacitances of up to 2000pF by measuring the small signal response to a low amplitude 1MHz a.c. signal which is generated internally. When using MIM samples, no d.c. bias is required for determination of insulator capacitance. However, MIS devices may also be measured with this apparatus if a d.c. voltage is applied so as to bias them into accumulation (see section 3.1.4); the voltage source (Time Electronics 9814) and

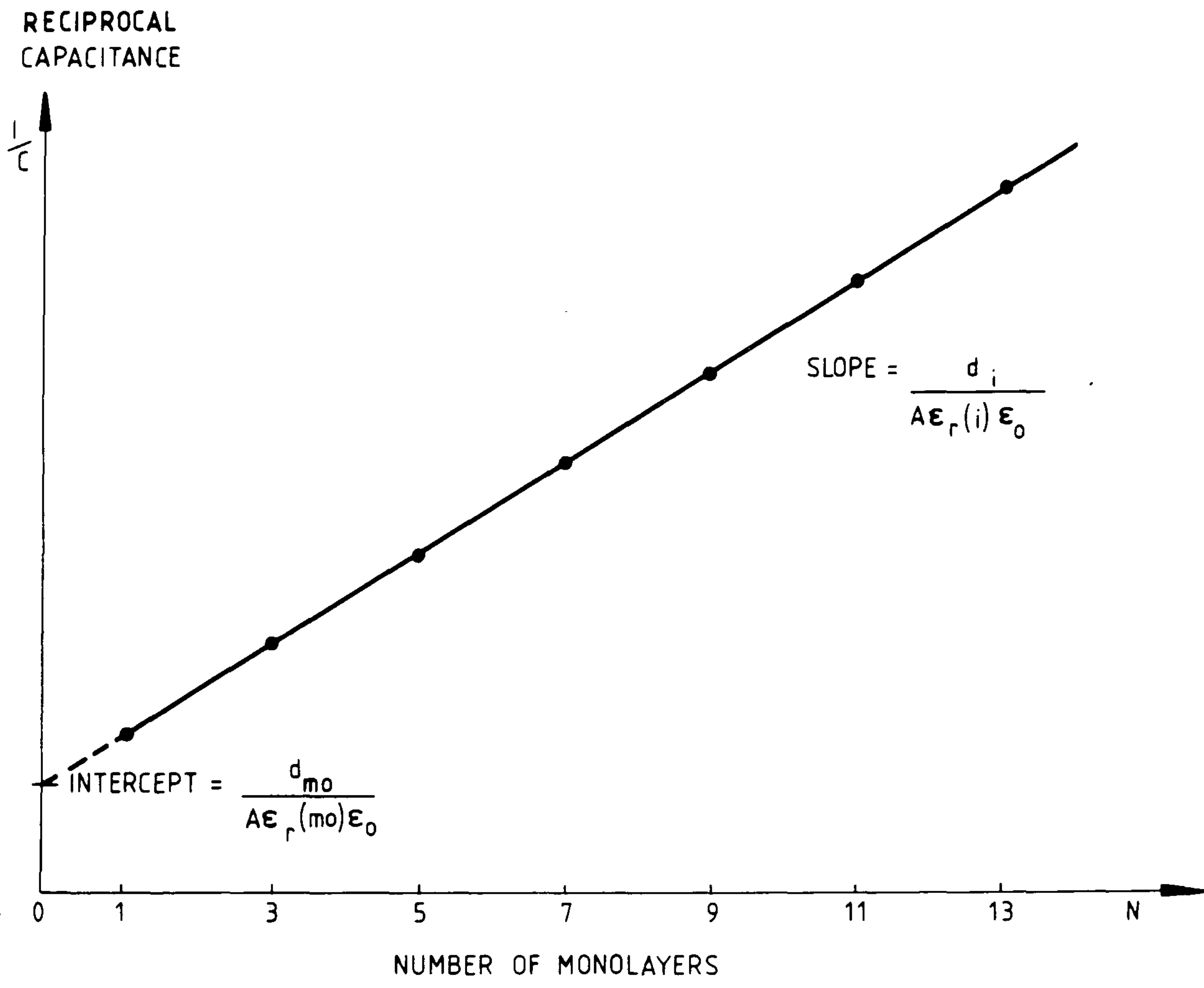


Figure 3.4 : Typical 1/C versus N plot for a metal - LB film - metal structure

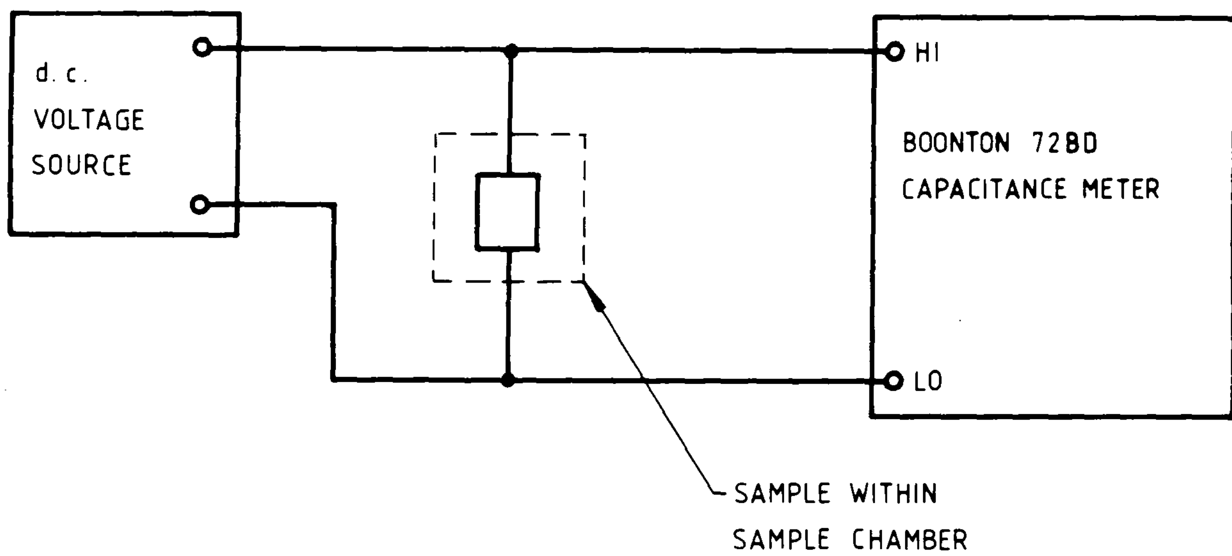


Figure 3.5 : Schematic of apparatus for permittivity calculations

sample chamber are considered in chapter 4.

3.2 Surface State Density Evaluation

A number of different methods have been employed to calculate the interface state density distribution of a MIS device. Some of these techniques require the capacitance-voltage characteristics of the sample to be recorded and are discussed in section 3.2.1. However, as will be seen, the drawbacks associated with this C-V approach may be largely overcome by utilising the conductance technique of Nicollian and Goetzberger [9] which involves measuring the relationships between a.c. conductance, signal frequency and bias voltage. Section 3.2.2. is devoted to this method and explains how the surface state density is calculated from the experimental data.

3.2.1. Capacitance-voltage methods

The earliest technique employed to determine surface state density was that of Terman [10], in which a high frequency C-V curve is measured experimentally as outlined in section 3.1. Although surface states do not respond to a high frequency signal, their trapped charge results in a lateral displacement from the ideal theoretical curve (figure 3.6). At each energy position this lateral voltage shift ΔV depends upon the surface state distribution N_{ss} at that point, and is given by:-

$$Q_s = C_{ox} \Delta V \tag{3.9}$$

where Q_s represents the total charge in the surface states. If Q_s is calculated over the range of applied bias voltage so that the Q_s versus surface potential (ψ_s) relationship can be determined, then:

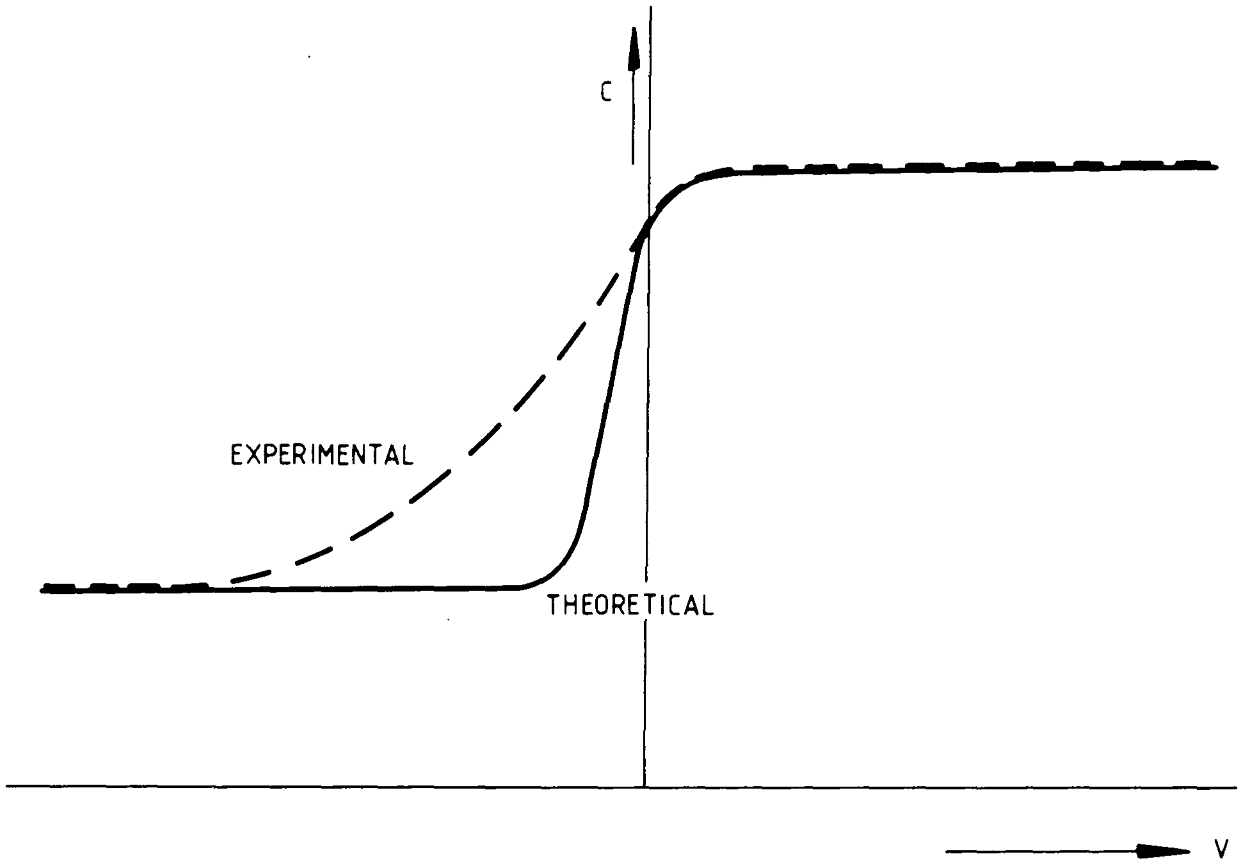


Figure 3.6 : Comparison of typical experimental and theoretical high frequency C-V plots

$$N_{ss} = \frac{1}{q} \quad \frac{\partial Q_s}{\partial \psi_s} \qquad eV^{-1}\ cm^{-2} \tag{3.10}$$

This equation expresses N_{ss} as a function of energy, and with knowledge of the flat-band position (where $\psi_s = 0$) each calculated value of surface state density can be related to a particular energy position in the bandgap. (The $\partial Q_s/\partial \psi_s$ terms must be obtained by graphical differentiation methods). One disadvantage of this method is that it is very sensitive to surface potential fluctuations, which can lead to considerable apparent surface state densities being wrongly detected. A further error can arise near the band edges, where even a frequency of 1MHz is not high enough to ensure that the surface states do not respond.

Another method of interface state density analysis involves measuring the C-V curve with a low frequency (quasistatic) applied signal [11]. If the period of this signal is longer than the time constants of the surface states, then these states will contribute to the total device capacitance, $C_{1f}(V)$. This is measured by recording the displacement current, i, resulting from the application of a slowly-rising linear voltage ramp,[12] as given by

$$i = \frac{dQ}{dt} = \frac{dQ}{dV}\ \frac{dV}{dt} = C_{1f}\ \frac{dV}{dt} \tag{3.11}$$

For the simple MIS capacitor described in figure 2.11a,

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_D + C_S} \tag{3.12}$$

Assuming that $C_S = qN_{ss}A$ and rearranging equation 3.12:

$$N_{ss} = \frac{1}{qA}\left(\frac{C_{1f}}{1 - C_{1f}/C_{ox}} - C_D\right) \tag{3.13}$$

C_D can be calculated from equation 2.10 or derived experimentally from applying equation 3.12 to a high frequency curve (in which case $C_S = 0$). Thus, equation 3.13 becomes:

$$N_{ss} = \frac{1}{qA} \left(\frac{C_{1f}\, C_{ox}}{C_{ox} - C_{1f}} - \frac{C_{hf}\, C_{ox}}{C_{ox} - C_{hf}} \right) \qquad (3.14)$$

Unfortunately, as with the high frequency technique, surface potential fluctuations may give rise to incorrect determination of surface state density [13], since the theoretically calculated value for C_D in equation 3.13 will be inaccurate. It is better to compare the high- and low-frequency curves, using equation 3.14, but this is only accurate provided that the high frequency is such that C_S is zero (i.e. that no surface states can follow the applied signal).

The surface potential, ψ_s, may be obtained directly from the low frequency C-V plot by integrating the curve over the range from strong accumulation towards inversion [11]:

$$\psi_s = \int_{Vacc}^{V} (1 - C_{1f}/C_{ox})\, dV = \psi_s^* + \Delta \qquad (3.15)$$

Numerical integration maybe performed to determine ψ_s^*, and the additive constant, Δ, may be found by comparison with ideal curves or calculated from the horizontal intercept of a high frequency $1/C^2$ versus V curve; from equation 3.5a, when $1/C_D^2 = 0$:

$$\text{intercept} = \psi_s - \frac{kT}{q} = \psi_s^* + \Delta - \frac{kT}{q} \qquad (3.16)$$

These, and other, capacitance techiques have been used for surface state density evaluation [14], but all suffer drawbacks of one kind or another. Some are very susceptible to errors due to surface potential fluctuation or are inaccurate because of uncertainty in the determination of the integration constant Δ, or of C_{ox} and N_d;

others fail when the C/C_{ox} ratio becomes close to unity (in this case even an accuracy of 10% on measurement of C can give great errors in N_{ss} and ψ_s). Becuase of these problems, it was found necessary to adopt a new approach to surface state density determination, and the a.c. conductance technique, described in the next section, was developed [9].

3.2.2 The a.c. conductance technique

By considering the loss mechanisms associated with the presence of interface states as discussed in section 2.2.3, further information about these states may be obtained. The procedure proposed by Nicollian and Goetzberger, [9] requires the determination of the complex frequency response of the small signal admittance of a MIS device from which the parallel capacitance and conductance, C_p and G_p (see figure 2.11b), are acquired and the surface state information extracted.

This is achieved by measuring the capacitance C_m and the conductance G_m of the sample over a wide frequency range at a large number of bias voltages. The device structure is shown in figure 3.7a and the electrical equivalent circuit in figure 3.7b: C_{ox} is the oxide (or insulator) capacitance, R_s the series resistance of the top and back contacts, leads and bulk semiconductor, and the parallel G_p-C_p network represents the combined effects of interface traps and depletion layer capacitance. Figure 3.7c denotes the circuit as measured experimentally.

The values of R_s and C_{ox} may be determined from measurements of C_m and G_m in strong accumulation:

$$R_s = G_m \;/\; (G_m^{\;2} + \omega^2 C_m^{\;2}) \qquad (3.17)$$

$$C_{ox} = C_m \left[1 + (G_m^{\;2} + \omega^2 C_m^{\;2}) \right] \qquad (3.18)$$

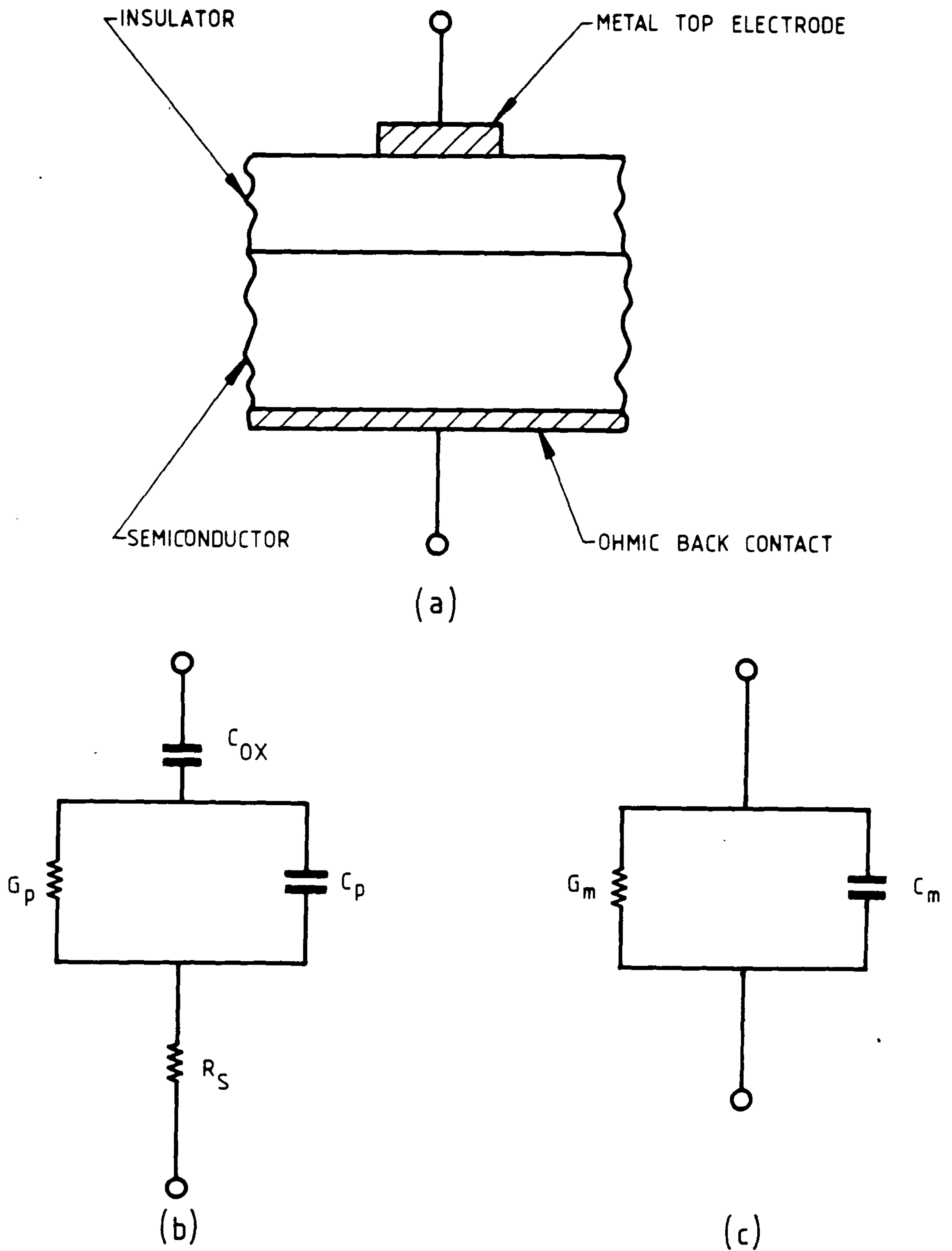


Figure 3.7: Schematic cross-section of MIS device with electrical equivalent circuits

It is important to compensate for these elements as they may otherwise obstruct correct interface state analysis [15]; for ideal devices the terms are bias and frequency independent, but in practice R_s and C_{ox} must be calculated at each measurement frequency to offset any frequency-dependent effects. The importance of this compensation is not commonly appreciated, but it shall be demonstated in experiments reported later (chapter 5.2.4).

The parallel conductance and capacitance terms, G_p and C_p respectively, may now be determined from the following equations:

$$A\,G_p = \frac{\omega^2 C_{ox}^{\,2}(G_m - \omega^2 C_m^{\,2} R_s - R_s G_m^{\,2})}{(\omega^2 C_{ox} R_s C_m - G_m)^2 + \omega^2 (C_{ox} - C_m - C_{ox} R_s G_m)^2} \qquad (3.19)$$

$$A\,C_p = \frac{\omega^2 C_{ox} C_m\,(C_{ox} - C_m) - C_{ox} G_m^{\,2}}{(\omega^2 C_{ox} R_s C_m - G_m)^2 + \omega^2 (C_{ox} - C_m - C_{ox} R_s G_m)^2} \qquad (3.20)$$

where A is the area of the top electrode, and R_s and C_{ox} are as defined in equations 3.17 and 3.18. The surface state density N_{ss} can be obtained from either C_p or G_p (see section 2.2.3). C_p is made up of two components: the surface state capacitance C_s and the depletion layer capacitance C_D (equation 2.28), and so the problem of evaluating C_D accurately is again encountered (as in the C-V techniques discussed in section 3.2.1.). However, G_p is directly related to N_{ss} (equation 2.32), and this fact enables values of surface state density to be calculated more accurately.

The standard experimental procedure for obtaining N_{ss} is to plot a number of C-V/G-V curves at different signal frequencies, and from these to build up plots of normalised G_p/ω versus ω for different values of bias voltage [9]. Figure 3.8a shows a

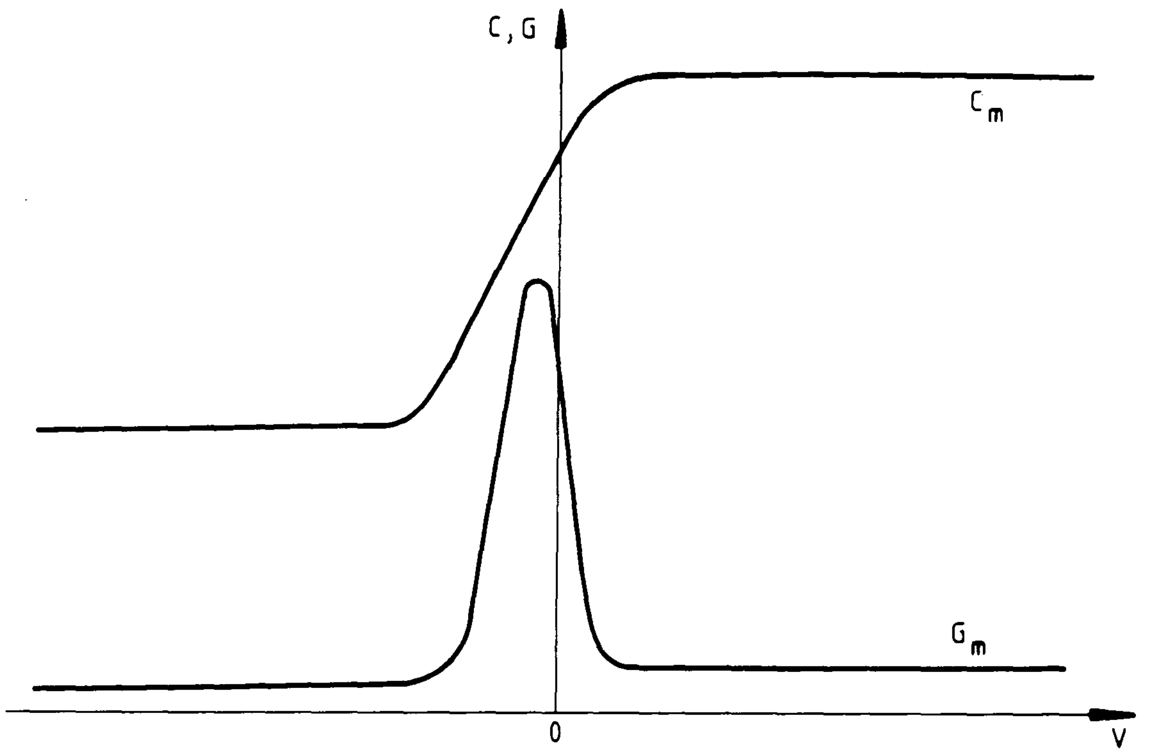


Figure 3.8a : Measured C-V, G-V characteristics for a MIS structure

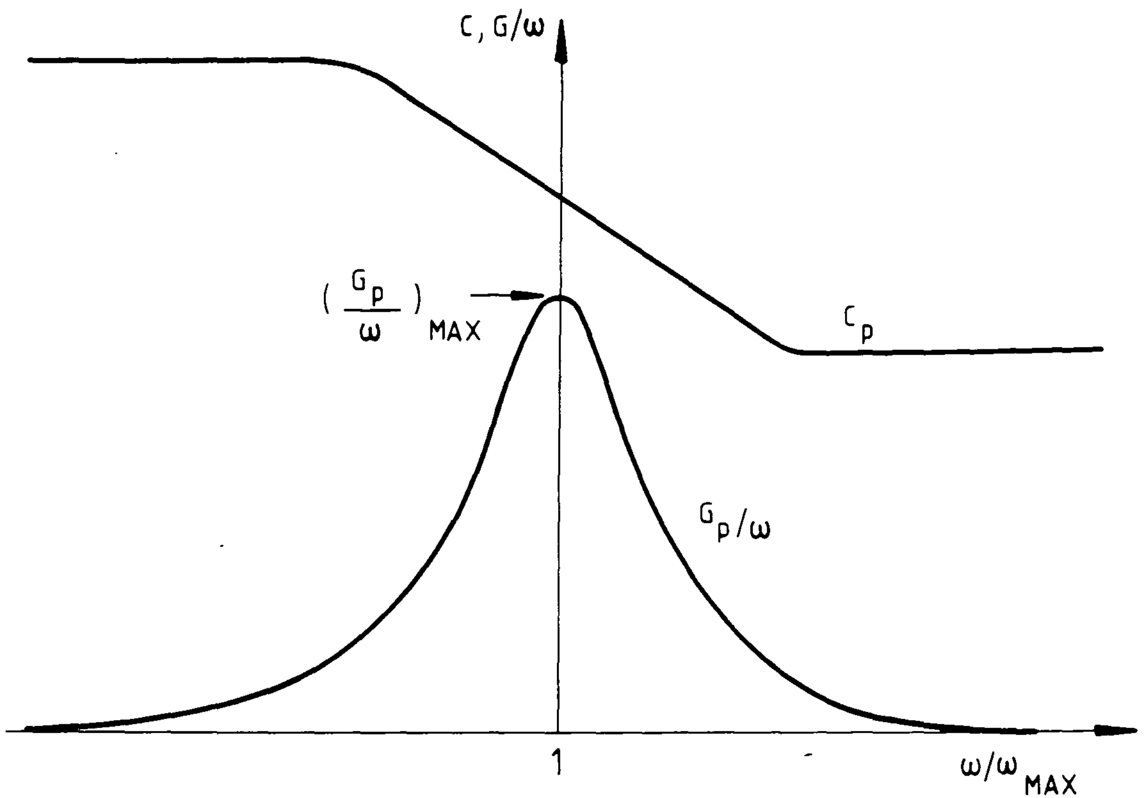


Figure 3.8b : Equivalent parallel admittance characteristics for a MIS structure

schematic curve of C_m, G_m versus V and figure 3.8b a single C_p, G_p/ω versus ω/ω_{max} plot made up of data from a number of C-V/G-V runs (both curves plotted in arbitrary units). The surface state density can be calculated from the equation:

$$N_{ss} = \frac{1}{qA}\left(\frac{G_p}{\omega}\right)_{max} / f_N(\sigma_g) \qquad (3.21)$$

The value of $(G_p/\omega)_{max}$ is obtained graphically from the parallel conductance plot. The statistical function $f_N(\sigma_g)$ depends purely upon the variance σ_g of the normalised G_p/ω versus ω response. By comparing the experimental result with standard curves plotted with σ_g as parameter (figure 3.9a), the curve variance can be found; the corresponding value of f_N is obtained from a standard plot of this function[14] (figure 3.9b).

In order to obtain the value of surface potential ψ_s (and hence the position in the bandgap relating to each particular surface state), the complicated integration procedure[11] described in section 3.2.1 can be avoided by measuring the value of C_p at the position of the G_p/ω peak. From equation 2.10, modified for surface area:

$$C_D^{-2} = \frac{2}{q\varepsilon_s N_d A^2}\left(\psi_s - \frac{kT}{q}\right) \qquad (3.22)$$

or

$$\psi_s = \frac{kT}{q} + \frac{q\varepsilon_r\varepsilon_o N_d A^2}{2\, C_D^2} \qquad (3.22a)$$

However, $C_D = C_p - C_s$ from equation 2.28, and since in general[14]:

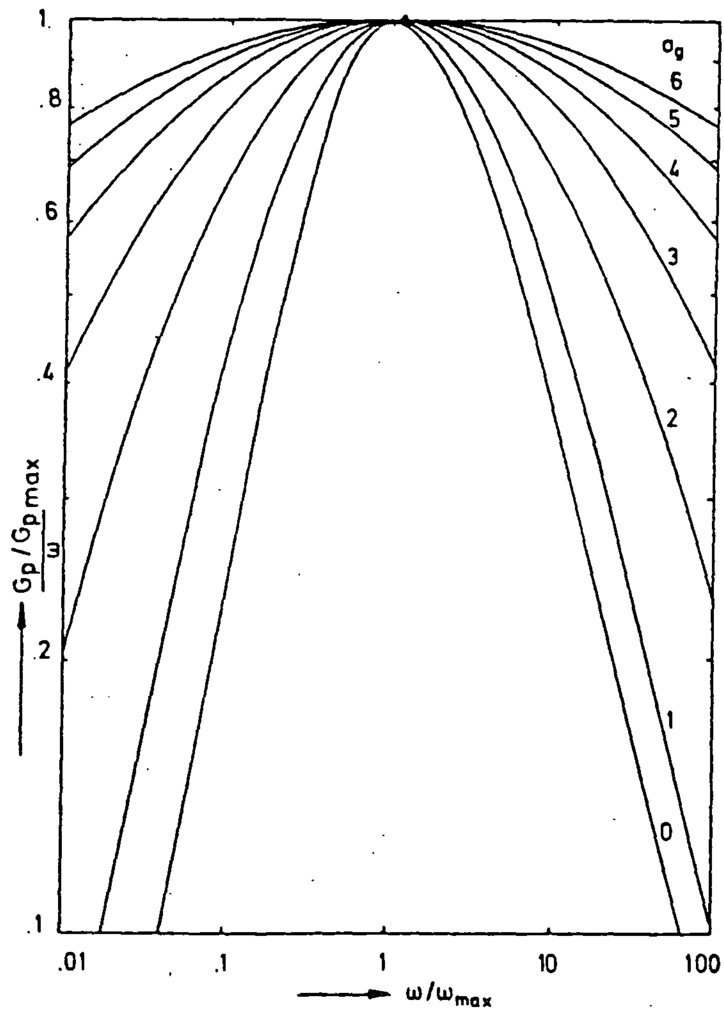


Figure 3.9a : Normalised parallel conductance curves plotted with variance σ_g as parameter

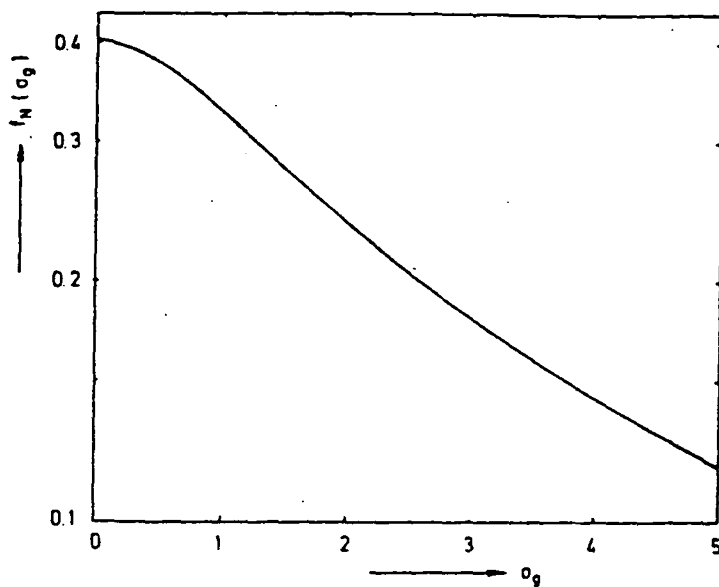


Figure 3.9b : Plot of the statistical function σ_g

$$C_s = qAN_{ss} \quad (3.23)$$

then from equation 3.22a:

$$\psi_s = \frac{kT}{q} + \frac{q\varepsilon_r\varepsilon_o N_d A^2}{2(C_p - qAN_{ss})^2} \quad (3.24)$$

Here, C_p is the parallel capacitance value corresponding to $(Gp/\omega)_{max}$ and N_{ss} is as defined in equation 3.21. This method of determining ψ_s dispenses with the need for numeral computation of the integral in equation 3.15 and graphical evaluation of the additive constant Δ; this means that no separate measurements are required as all the information is contained in the G_p/ω and C_p data already calculated.

The conductance technique is more accurate than the C-V methods discussed in the preceding section since it does not rely on an approximate evaluation of the depletion capacitance (an accuracy of 10^9 $eV^{-1}cm^{-2}$ is attainable compared with 10^{10} $eV^{-1}cm^{-2}$ for the best C-V method). However, it has the disadvantage of requiring a large amount of data to be acquired for each N_{ss} value determined (one full C-V/G-V sweep will contribute only one point to each $G_p/\omega - \omega$ plot; thus to calculate $(G_p/\omega)_{max}$ precisely it is necessary to perform a large number of voltage scans). A procedure developed by Simonne(16) enables an N_{ss} value to be extracted from just two conductance measurements: one at a frequency ω_{max} and one at a frequency a factor of five different. This is a far simpler evaluation, but it does not alleviate the basic problem of requiring a G_p/ω versus ω curve to determine the peak position.

The solution to this problem is to record the admittance characteristics whilst sweeping the signal frequency but keeping the applied bias fixed; hence the G_p/ω versus ω relationship can be calculated directly without the need for numerous C-V scans. By applying this swept-frequency approach for a large range of bias voltages, it is possible to measure the variation of surface state density across the bandgap of the device. In practice, the experimental apparatus must be recalibrated at each new

frequency within the scan[17]; this makes the associated electronic circuitry rather complex and the procedure very time-consuming. The novel system developed in this work and presented in chapters 4 and 5 performs such a frequency scan; it utilises a micro-computer to control and calibrate equipment, take readings and process data, thus enabling N_{ss} and ψ_s to be determined rapidly and with great saving in operator time and effort.

3.3 Summary

This chapter has outlined the different experiments (which are performed later in this work) to characterise the electrical properties of MIS devices and has indicated the way in which the experimental results are interpreted. The methods of determining flat-band voltage, semiconductor doping concentration, insulator permittivity and trapped charge have all been considered.

A comparison of the conductance technique with standard capacitance-voltage measurements for surface state density evaluation has been made and the practical drawbacks discussed; an introduction to the swept-frequency approach adopted in this work for fast $N_{ss} - \psi_s$ calculation has been presented. The instrumentation and measurement procedures developed in order to employ this technique for interface state analysis of MIS samples are examined in the following two chapters.

CHAPTER 4 : DEVELOPMENT OF AUTOMATED ADMITTANCE MEASUREMENT SYSTEM

4.0 Introduction

The a.c. conductance technique of Nicollian and Goetzberger [1] as described earlier (section 3.2.2) can be used to determine the density of states at the insulator-semiconductor interface over a large part of the semiconductor bandgap of a MIS device. However, considering its advantages this technique is not used as widely as might be expected because of the difficulty of making accurate small-signal admittance measurements over a wide range of frequencies.

In order to extract the surface-state density information using a manually-operated admittance bridge, admittance data must be obtained by sweeping the sample with a d.c. voltage bias at a large number of different a.c. frequencies. Automation of this task [2,3] enables some saving in time, but there are two inherent disadvantages. The C-V and G-V data recorded at each frequency must be rearranged to give the fixed-voltage G-ω and C-ω curves from which the interface state density is calculated, and therefore a large amount of information must be gathered, not all of which will be used in the N_{ss} determination. Furthermore, practical MIS devices may exhibit a slight instability in the applied bias versus surface potential relationship due to deep level trapping, polarisation of passivation levels or ionic motion in the oxide. This can lead to errors in the G-ω and C-ω curves since applying the same bias voltage at a different frequency will not guarantee that measurements are being taken at the same position in the bandgap.

Consequently, it is better to measure the capacitance and conductance with changing frequency whilst maintaining a fixed voltage on the sample. As the equipment requires calibration at each new frequency, it is highly desirable to automate the system. This chapter, together with chapter 5, describes the extensive work carried out on development of a computer-controlled instrumentation system capable of determining the a.c. admittance of a MIS sample over a wide range of signal frequencies and bias voltages in order to extract interface state density information from the measured data.

Chapter 4 details the stages in hardware development and describes the improvements and innovations in circuit design incorporated into the system. In chapter 5, the custom-designed software will be explained and the operational performance of the instrumentation will be considered; in addition, preliminary results obtained whilst commissioning and proving the system are presented.

4.1 Manual measurement of a.c. admittance

The configuration of a typical manually-operated system to collect C-V and G-V data is shown in figure 4.1. A variable frequency oscillator of ∿5V rms output provides the reference for a dual-phase, lock-in amplifier and after attenuation gives ∿8mV root-mean-square (rms) a.c. stimulation to the sample. This small a.c. voltage is mixed with the d.c. bias from the ramp generator, and the combined signal is applied to either a calibration capacitor (which is assumed to have zero conductance) or the sample under test. The resultant output is fed through a virtual earth amplifier to the signal input of the lock-in amplifier; this instrument has two phase-sensitive detectors which are set up to measure the in-phase (capacitance) and orthogonal (conductance) signal components.

A number of steps must be followed to acquire C-V and G-V data from this manual system.

Step 1: Set oscillator frequency to desired value and select appropriate time constant for phase-sensitive detectors.

Step 2: Connect calibration capacitor and adjust the sensitivity and phase of psd channels until one gives zero indication (this is defined as the conductance channel) and the other displays an on-scale deflection (this is the capacitance channel).

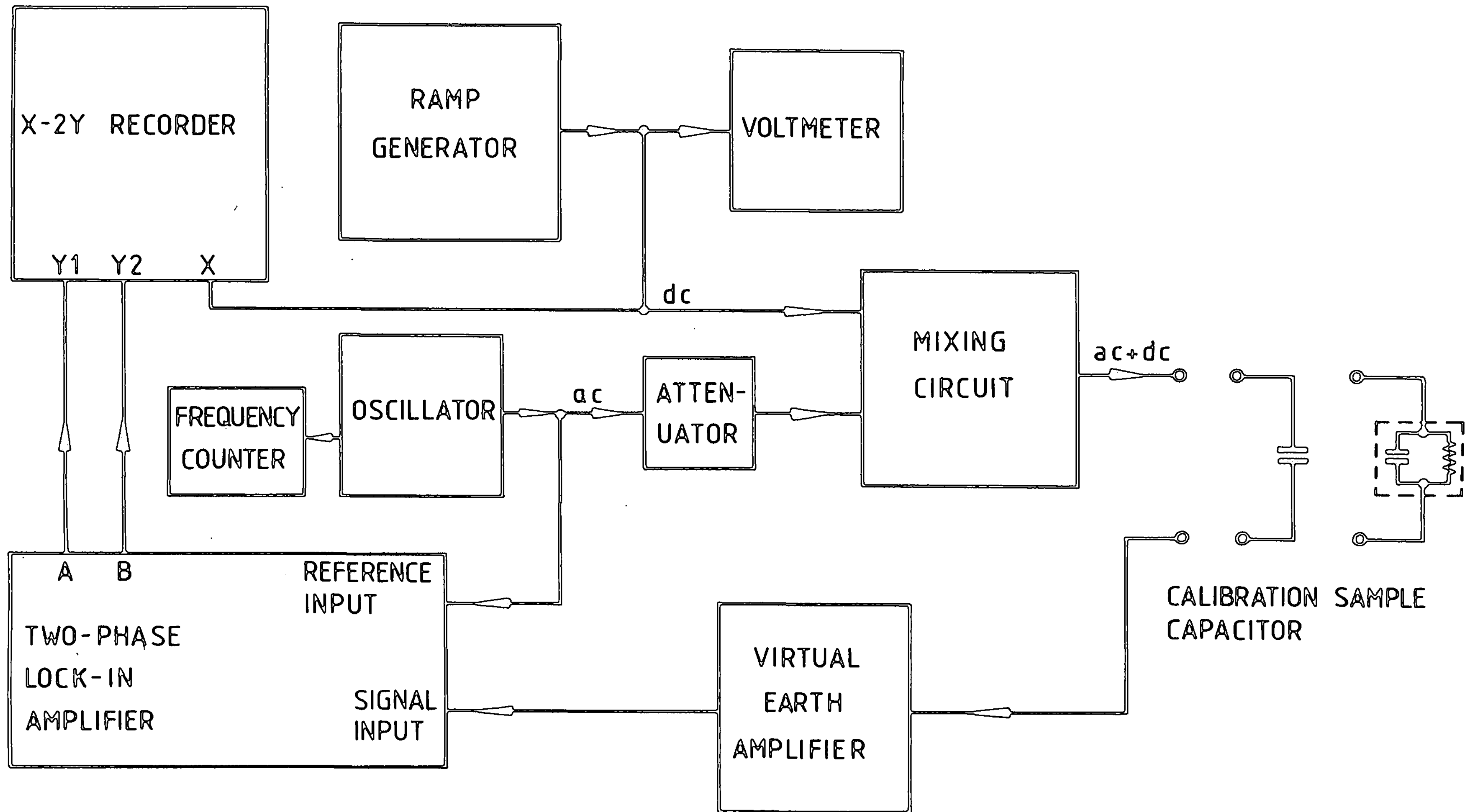


Figure 4.1 : Block diagram of a typical manual admittance measurement system

Step 3: Adjust plotter setting to calibrate capacitance channel (≡C).

Step 4: Reverse plotter input leads and adjust plotter setting to calibrate conductance channel (≡G/ω). Restore plotter input leads.

Step 5: Adjust plotter setting to calibrate voltage channel.

Step 6: Connect sample under test, start plotter and activate voltage ramp.

This sequence of operations will give a plot of capacitance and conductance against voltage at one fixed frequency, and in order to build up the C-ω and G-ω information necessary for surface state analysis, the same procedure must be followed over a wide range of frequencies. Clearly, this is extremely inefficient, and when considered with the disadvantages outlined in section 4.0 reinforces the need for an automated system which can operate in the swept-frequency mode.

4.2 Development of automated a.c. admittance instrumentation

A block diagram of the measurement system is shown in figure 4.2. An a.c. signal is derived from the Brookdeal 5206 Lock-In Amplifier, which consists of a frequency-programmable oscillator and a phase-sensitive detector (psd). The 5 Volt output is attenuated in order to give only a small ($\sim kT$, $\sim 8mV$) a.c. stimulation to the sample (see section 2.2.3). This is mixed with the bias voltage, a high resolution d.c. level generated by the programmable Time Electronics 9814 Voltage Calibrator. The combined signal is then fed via a switching network based on the HP59306A Relay Actuator to either a polystyrene calibration capacitor or the sample under test. Both these components are housed within the custom-built sample chamber. The signal which emerges from the sample chamber is amplified by a

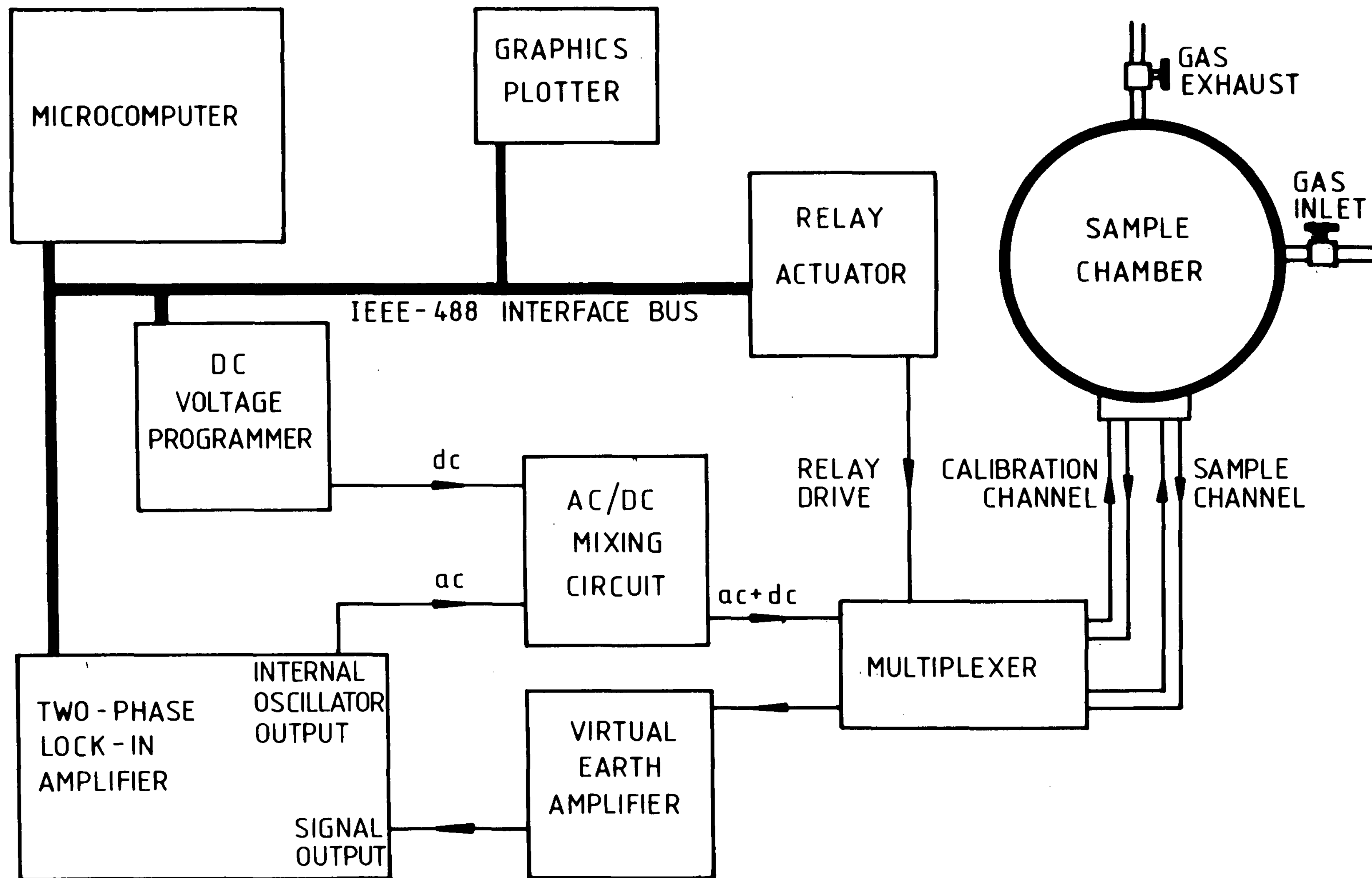


Figure 4.2 : Block diagram of automated admittance measurement instrumentation

virtual earth amplifier (vea), and is sent to the phase-sensitive detector.

The Hewlett-Packard 85 microcomputer is used to program the experimental variables, to control the operation of instrumentation and to retrieve and process data; this is achieved with an original BASIC software program in conjunction with the IEEE-488 interface bus option.

4.2.1 Lock-In Amplifier

The Brookdeal Model 5206 "Two Phase Lock-In Analyzer" offers many advantages over conventional lock-in amplifiers. In addition to a number of self-contained, automated operation routines, it may be externally controlled by a computer via a digital interface (RS232C serial or IEEE-488 parallel data link) (4).

In order to implement computer control, the IEEE-488 digital interface option has been installed. This enables the equipment to communicate with the system with complete source and acceptor hand-shaking and service-request capabilities, and permits computer control of all instrument functions.

Also installed is the internal oscillator option. With all three plug-in frequency range cards (Broadband, Audio Frequency and Low Frequency), this can generate a programmable a.c. signal of 0.1% frequency resolution over the range 0.1Hz to 100kHz, with amplitude adjustable from 0 to 5 Volts rms by means of a rear-panel potentiometer. In practice, a very small signal amplitude ($\sim$8mV rms) is needed; as this level is difficult to achieve from the internal oscillator without degradation by noise the output is set at 5 Volts rms and is attenuated in the a.c./d.c. mixing circuit (section 4.2.3) before reaching the sample.

The phase-sensitive detection circuitry of this lock-in amplifier will recover a.c. signals which are at the same frequency as the reference

channel. The two detectors have a very wide sensitivity range (1μV to 5V rms full-scale sensitivity) and good dynamic reserve (between 20dB and 60dB), and operate between frequencies of 0.2Hz to 100kHz with all three frequency range cards. The reference channel is driven at the frequency of the internal oscillator, and its phase can be altered to coincide with that of an incoming signal. As the Channel 1 and Channel 2 demodulating signals are orthogonal, the in-phase and 90° out-phase components respectively of any subsequent incoming a.c. signal will be displayed as a d.c. voltage. Output noise reduction is accomplished by means of switchable low-pass filters with time constants between 100ms and 100 seconds, and attenuation rates of -6 or -12dB/octave, also switchable.

The Channel 1 signal may be increased by a factor of 10 in order to more accurately measure small phase angles (i.e. where one channel reading is much less than the other; for example, the conductance of a thick-oxide MOS device will be very small compared with the capacitance).

As the Model 5206 has a built-in microprocessor, a number of automatic functions are available, giving the instrument great flexibility and ease of operation. The most powerful of these autofunctions is the AUTOSET facility, which matches the signal of interest by adjusting the full-scale sensitivity and phase of the detectors to give a maximum deflection of Channel 1 (which measures the in-phase signal component) and a zero indication on Channel 2 (which measures the orthogonal signal component). If this autofunction is invoked when examining the polystyrene calibration capacitor - which can be considered to have zero conductance - the psd channels will directly measure capacitance (Channel 1) and conductance (Channel 2). After calibration in this way, the complex admittance can be calculated for any device subsequently connected into the circuit.

4.2.2 Voltage Calibrator

As the d.c. bias applied to a device has to be carefully controlled in order to determine the position in the bandgap of the interface states under observation (see section 3.2.2), the voltage source used must have an accurate, stable, high-resolution output over a range of around -10 Volts to +10 Volts. The Time Electronics 9814 Programmable Voltage Standard fulfills these requirements [5], and has the added advantage of an integral IEEE-488 digital interface which enables the user to operate the equipment from the front-panel push-buttons or from a computer controller. The d.c. voltage output is variable between -13V and +13V with 0.01% accuracy, and a resolution of 50 μV or better is attainable. There are four voltage ranges (10V, 1V, 100mV, 10mV) and also an auto-ranging facility. The instrument provides a true bipolar output (i.e. the "Lo" output terminal can remain at earth for all ouput values and polarities), thus eliminating common mode errors or the need to reverse input connections when changing polarity.

When under computer control, the Voltage Calibrator may be used as a ramp generator (although it is more precise to describe the output as a high resolution "staircase" waveform, as it consists of a large number of discrete steps), and hence conductance- and capacitance-voltage scans may be carried out.

4.2.3 a.c./d.c. mixing circuit

A double R-C network developed by Boudry [6] is widely used to mix a.c. and d.c. signals (Fig. 4.3a). Analysis of this circuit reveals that its ouput resistance (R_{out}) is approximately 10MΩ, and consequently a d.c. voltage will be dropped across the network when a sample is connected, since a potential divider will be formed (Fig. 4.3b). When applied to "typical" [6] thick (~100nm oxide) MOS devices, for which Boudry's apparatus was designed, this voltage drop is small because the device impedance will be some orders of magnitude greater than R_{out}. However, the circuit is unsuitable

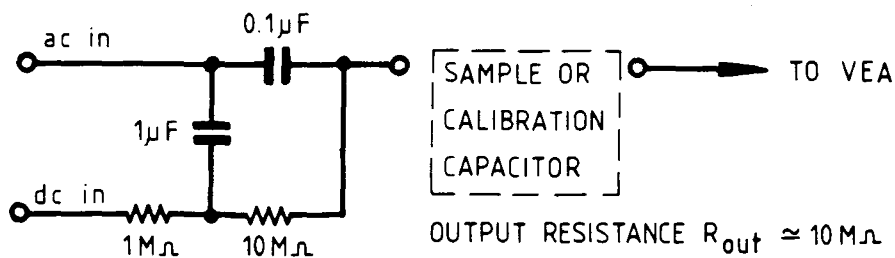


Figure 4.3a : Double RC mixing network

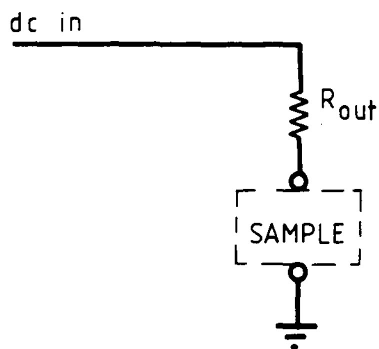


Figure 4.3b : d.c. equivalent circuit for RC mixer and sample configuration

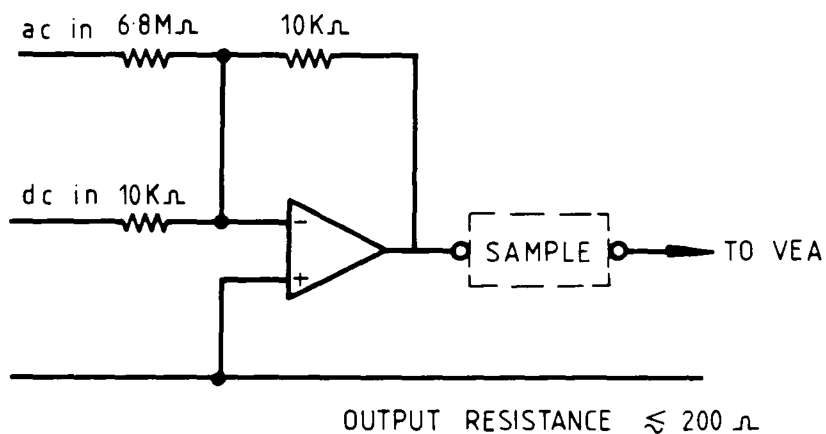


Figure 4.4 : Simple operational amplifier circuit

for use with lower impedance (e.g. thin oxide or Langmuir-Blodgett film) insulating layers for which resistance will be of similar magnitude to R_{out} and thus a significant fraction of the d.c. bias may appear across the mixing circuit and not across the sample, resulting in incorrect biasing of the device.

Simple experiments conducted with a high impedance voltmeter (Keithley Model 181: impedance $>10^9\Omega$) showed that this was the case, and indicated the need for a mixing circuit which has low output impedance. In addition to this requirement, the circuit should ideally be capable of operation over a wide range of a.c. frequency (∿0.1Hz - 100kHz) and should also if possible be able to attenuate the 5V rms a.c. signal from the lock-in amplifier down to about 8mV rms (section 4.2.1).

In order to satisfy these criteria, the circuit in figure 4.4 was designed. By using an operational amplifier in the unity gain configuration, a programmed voltage level can be added to the small a.c. excitation; as R_{out} is only 200Ω or less for this arrangement, which is many orders of magnitude lower than the impedance of any MOS device (even that of thin oxide samples), the output voltage drop is negligible. In addition, with careful choice of resistors the circuit will perform the attenuation of the a.c. signal.

The voltage gain A_V of an operational amplifier can be expressed as [7]:

$$A_V = \frac{V_o}{V_i} = \frac{-Z_f}{Z_i} \qquad (5.1)$$

where V_o = voltage output, V_i = voltage input,

Z_f = feedback impedance, Z_i = input impedance.

Examing the circuit in figure 4.4, it is clear that the d.c. voltage gain will be -1, since Z_f = 10kΩ = Z_i for the d.c. input. For the a.c. signal, however, Z_f = 10kΩ and Z_i = 6.8MΩ, so the a.c. voltage gain will be -1.47×10^{-3} (i.e. a 5V rms signal will

will be attenuated to ∿ 7.4 mV rms).

For both a.c. and d.c., the voltage gain is negative as the operational amplifier is being used in an inverting mode. This will result in a 180° phase shift of the a.c. signal, which will be compensated for by the internal phase control of the psd when the "AUTOSET" routine is run (section 4.2.1). In the d.c. case the applied voltage will be inverted (i.e. a +1V bias will appear at the output as -1V); this is not at all desirable, and so an additional inverting stage is required in the d.c. channel.

A μA741CP general-purpose operational amplifier was found to be sufficient to meet the design specifications. Although this component has a small full-power bandwidth (∿10Hz), its gain-bandwidth product is 1MHz which in this application gives a bandwidth of 1MHz since it is being used in unity gain configuration.

Fig. 4.5 shows the completed design as implemented in the system. The second operational amplifier stage is placed in the d.c. path before mixing with the a.c. signal. A number of extra components are shown in the circuit diagram. A 4.7kΩ resistor inserted between the non-inverting operational amplifier terminal and ground was included to balance the input bias currents to the operational amplifier, and the offset voltage was nulled by adjusting a 10kΩ potentiometer which was connected to the 741 offset pins and tapped with -15V (derived from the negative power rail). A 220nF d.c. blocking capacitor appears in series in the a.c. channel, and a 470nF capacitor connected from the d.c. line to ground smoothes any ripple on the d.c. level.

The final design was constructed on a custom-built printed circuit board (pcb) and after being fully tested for correct operation was housed in a shielded die-cast metal box, together with the voltage-controlled relays (section 4.2.4) and the virtual earth amplifier (section 4.2.6), as described later in section 4.2.7.

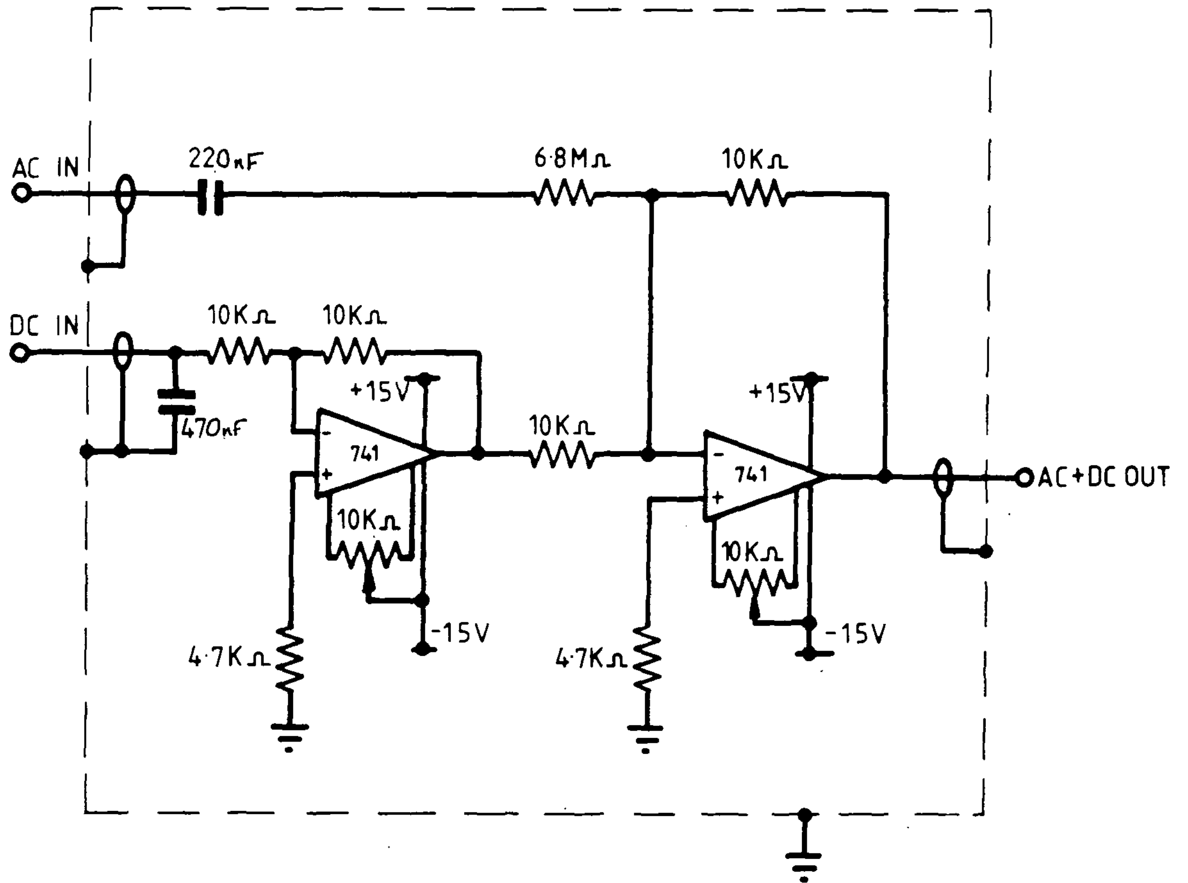


Figure 4.5 : Operational Amplifier Mixing Circuit - implemented design

Therefore, when the relay is off (C6 connected to B6), pole C6 is at zero potential, the coil has no voltage across it, and the multiplexer relays are not activated. Referring to figures 4.6a and 4.6b, the mixed a.c./d.c. signal is sent to the calibration capacitor and the output from this component directed to the vea and thence to the lock-in amplifier; the sample has only the d.c. bias applied across it (one side is grounded). When relay 6 is on (C6 connected to A6), pole C6 is at +5V and since this appears across the coil the multiplexer relays will close. In this case, the a.c./d.c. mixer output is connected to the sample, and the resulting signal is sent to the vea (which it must be remembered is at approximately zero potential, ensuring that all of the d.c. bias voltage appears across the sample); the calibration capacitor is disconnected. Using a Fluke 8060A Multimeter (voltmeter mode), the regulated voltage appearing on pole A6 was measured as +5.2 volts, which was within the limits required for the relays to be activated by the coil. The operation of the switching circuit was checked by probing the input and output terminals with the multimeter (ohmmeter mode) to determine the high and low resistance paths for each relay in each position; comparing the observed connections with the circuit diagram (figure 4.6b) confirmed that the multiplexer was functioning correctly.

4.2.5 Sample chamber

The construction of a sample chamber should be such that

a) it provides a firm support for, and easy access to, the sample
b) it ensures good electrical contact with both back and top device electrodes
c) it can be hermetically sealed, with provision for evacuation and operation in different gas ambients
d) it does not corrode or otherwise react when exposed to these gases, as this might contaminate the atmosphere surrounding the sample

e) stray capacitance is minimised by careful design of electrical probe geometry, careful screening, etc.

To meet these criteria, the arrangement shown in figure 4.8 was constructed. The basic chamber and lid were made of brass and were chromium-plated to resist corrosion; a gas-tight seal was accomplished by tightening retaining screws on the lid to compress a rubber 'O' ring around the chamber. A glass window was incorporated into the chamber lid so that devices could be exposed to light if desired whilst remaining in the gas atmosphere and four gas input/exhaust ports were built into the wall of the chamber. All internal fitments were machined from polyteflofluoroethylene (PTFE) blocks or fabricated in stainless steel, the only exception being the brass mounting block needed to make good back contact to the samples.

To calibrate the phase-sensitive detectors accurately, and with minimal phase errors, there must be very little difference in stray capacitance between the calibration and sample channels. This was accomplished by mounting both the sample and the calibration capacitor within the chamber and ensuring that the arrangement was as symmetrical as possible. Two brass blocks were used as conducting ground planes. The sample (already mounted on a brass plate to give a good back contact and protection against damage) was screwed to one of these blocks, and to the other was fastened a turned-pin integrated circuit (i.c.) holder into which a range of calibration capacitors, each soldered to a similar holder, could be inserted ("piggy-back" style). Electrical connection was made to the capacitor through the i.c. holder by soldering one leg to the brass block and another to a shielded wire. The sample top contact was made with a gold ball attached to a micro-manipulator arm which enabled one of a number of top electrodes to be selected; back contact was via the brass base plate. Great care was taken to keep lead lengths equal and signal paths symmetrical, and when measured with a capacitance meter (Boonton Electronics model 72BD) the differential stray capacitance between sample and calibration channels was very low ($\sim$0.8 ($\pm$0.1) pF).

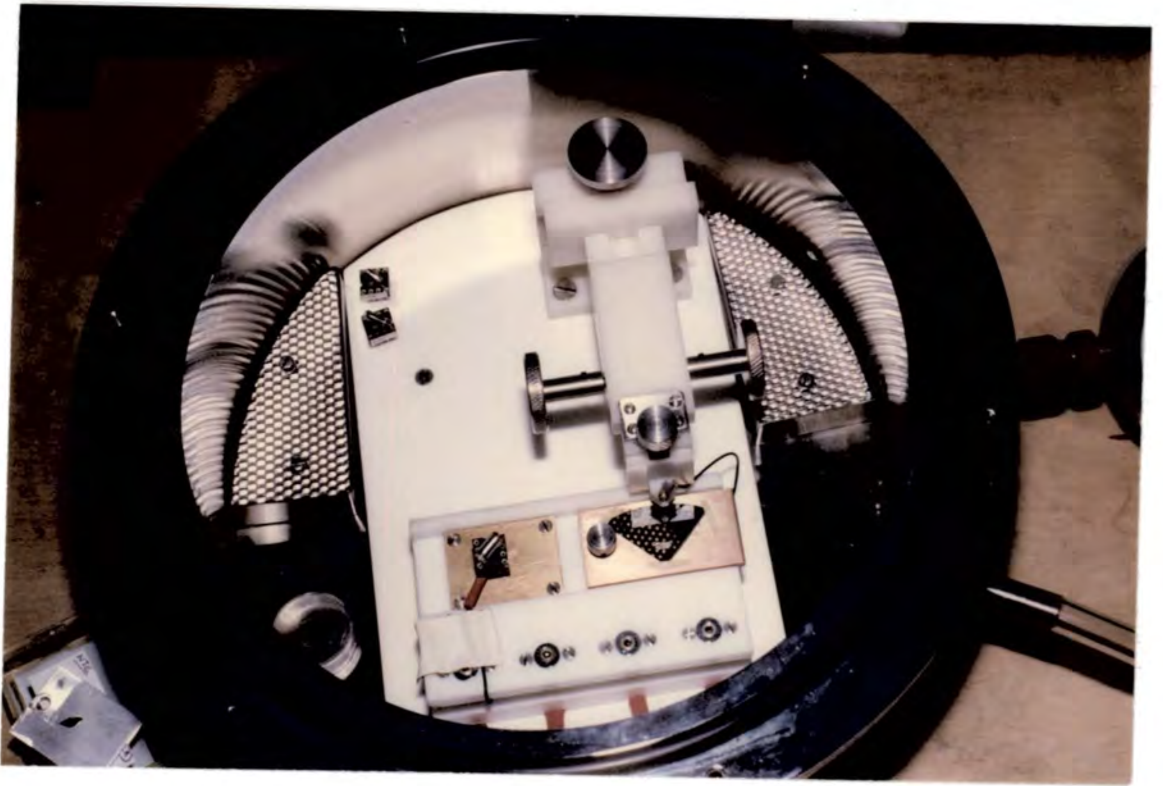


Figure 4.8 : Sample chamber

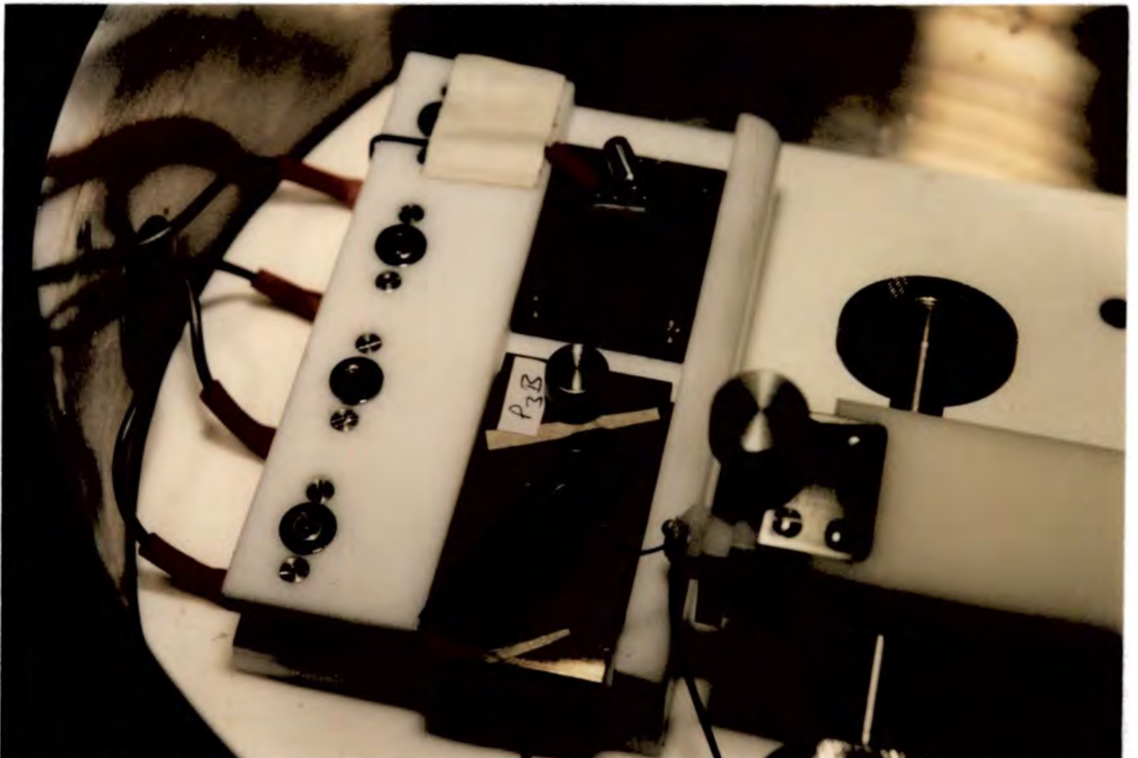


Figure 4.9 : Detail of sample tray, micromanipulator arrangement and electrical contacts

Another notable feature is the design of the sample tray, which may be removed from the chamber (figure 4.9). This avoids any restriction of working space when mounting the sample and attaching the calibration capacitor. Contact to the rest of the system is accomplished by 4mm "banana" plugs which are pushed into sockets inside the chamber. A diagram showing the electrical connections within the sample chamber is shown in figure 4.10.

The sample chamber was connected by means of the gas inlet and exhaust ports to a vacuum pump, a pressure gauge, a dry nitrogen cylinder, and to the output of a signal 8525 Gas Blender. This last instrument was used to mix two gases in a preset ratio so that the atmosphere within the chamber was carefully controlled. In addition, two stainless steel trays filled with silica gel were placed inside the chamber to absorb moisture; if dry nitrogen were pumped into the chamber, samples within could be kept dry without having to be removed to a separate desiccator.

4.2.6 Virtual earth amplifier circuit

To measure the admittance of a MIS device the a.c. current which emerges from the sample chamber and contains the capacitance and conductance information must be converted into a complex voltage in order to provide a suitable input to the phase-sensitive detectors.

A number of types of circuit may be used to perform the required current-voltage transformation. The simplest of these (Fig. 4.11a) involves measuring the voltage across a large capacitor, C_o. If v_i is the a.c. voltage input the sample, v_o the output voltage and C_m the measured sample capacitance, then for the capacitive (in-phase) signal component

$$v_o = v_i \frac{C_m}{C_m + C_o} \qquad (4.2)$$

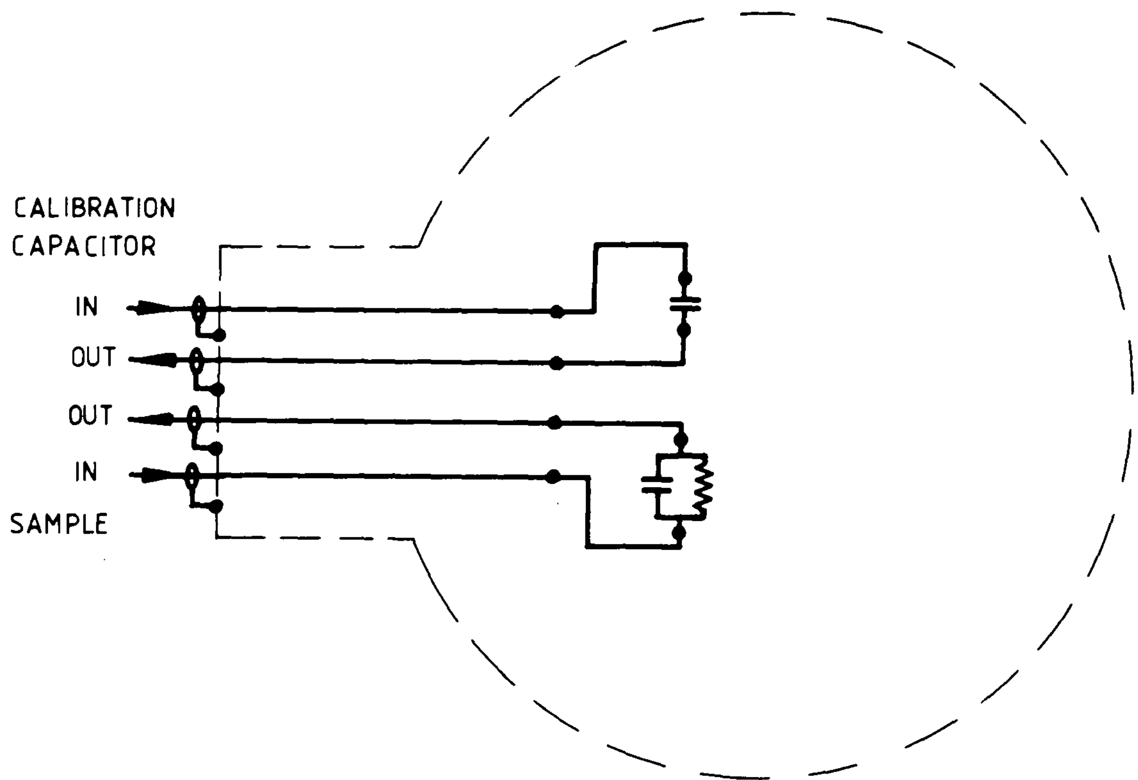


Figure 4.10 : Electrical connections within sample chamber

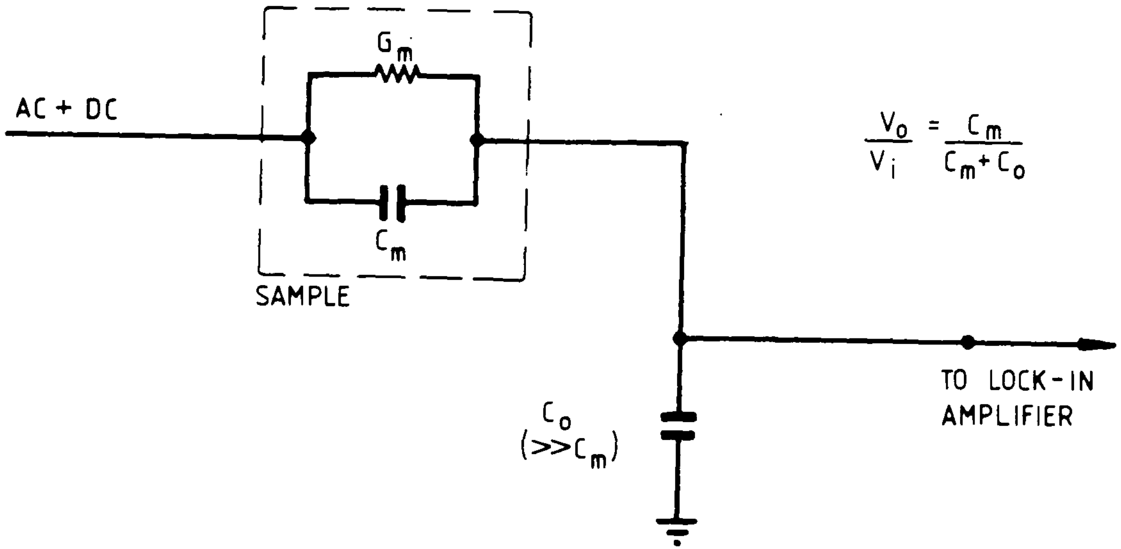


Figure 4.11a : Charge-sensitive a.c. detector circuit

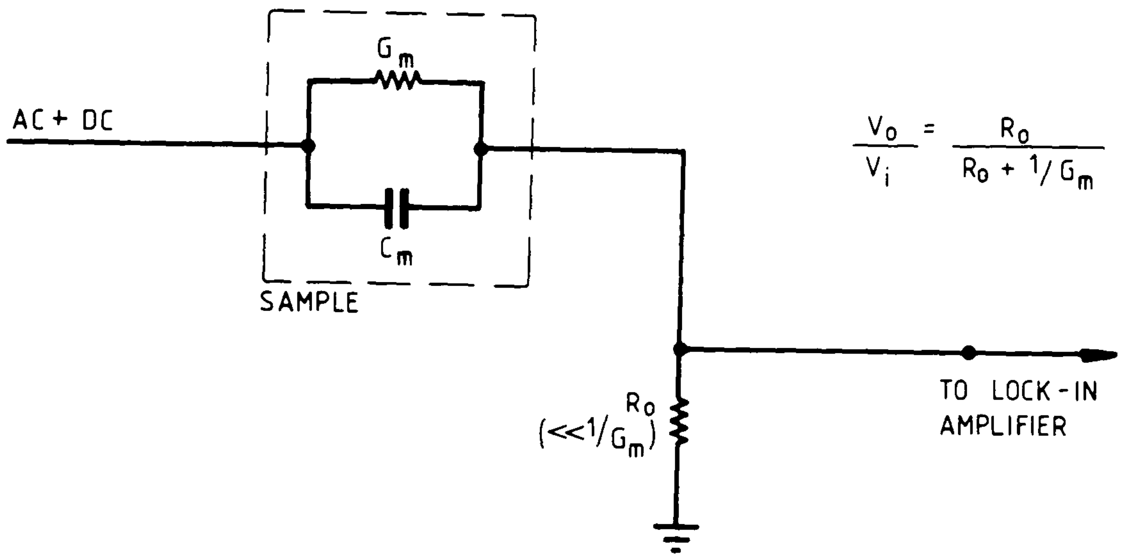


Figure 4.11b : Current-sensitive a.c. detector circuit

which if $C_o >> C_m$ yields

$$C_m = C_o \left(\frac{v_o}{v_i}\right) \tag{4.3}$$

For the conductance (orthogonal) signal component, if $G_m << \omega C_o$, similarly

$$G_m = -j\omega C_o \left(\frac{v_o}{v_i}\right) \tag{4.4}$$

Although in theory the capacitance and conductance can be determined, the large value of C_o required to ensure that C_m and G_m/ω are insignificant in comparison means that the voltage v_o will be very small. (Considering an example where the sample capacitance is 200pF, C_o must be at least 20nF and as v_i is 8mV rms, v_o will be of the order of 80μV rms).

Another similar configuration uses a small resistor R_o (>> $1/G_m$) in place of C_o (Fig. 4.11b). This circuit is current sensitive rather than charge sensitive in that the conductive-current vector is in phase with the applied voltage and the capacitive-current vector is orthogonal, and a resistor similar in value to the sample resistance is used to calibrate the lock-in amplifier. As the conductance of a MIS sample is frequency dependent ($G/\omega \sim$ constant), this means that a number of calibration resistors may be needed for measurements over a wide range of frequencies whereas the charge sensitive circuit requires only one calibration capacitor (as sample capacitance $\sim$ constant and is independent of frequency). However, the problem of low output voltage is still apparent.

A better solution is to use a buffer amplifier with capacitive feedback which is of the order of the sample capacitance. A suitable operational amplifier is the Analog Devices AD48K, a very fast, FET-input device which has a d.c. gain of 10^5 and a unity gain bandwidth of 15MHz.

For the circuit shown in figure 4.12a,

$$\frac{v_o}{v_i} = - \frac{C_m}{C_f} \tag{4.5}$$

where C_f is the value of the feedback capacitance. However, as the operational amplifier has a large d.c. gain it is possible that the d.c. output level, which is due to current leakage through the sample, may latch to the negative supply rail. This can be prevented by providing a d.c. feedback loop as in figure 4.12b. Unfortunately, the time constant of the circuit is some 2×10^4 seconds, which is unacceptable for fast data acquisition. This could be improved upon by reducing the value of the large feedback resistor, but such action would introduce an additional feedback path for the a.c. signal resulting in unacceptable phase deviations.

A configuration designed by Boudry (6) and shown in figure 4.13 reduces the time constant of the circuit by using a different d.c. feedback path which includes an additional FET-input operational amplifier and a unity gain buffer inverter. The filter circuit across the FET amplifier provides low-frequency roll-off and thus better stability at low signal frequencies; the values of the filter components were calculated to give roll-off at approximately 0.3Hz (since this is close to the minimum signal frequency which can be measured by the lock-in amplifier). The relaxation time of this circuit is of the order of tens of milliseconds, which is less than that of the rest of the system. The input of the vea appears to the sample as a 30Ω resistor in series with a 10μF capacitor, and the effects of these upon the a.c. signal are negligable.

One disadvantage of this circuit is that it can only provide a d.c. path for a small amount of d.c. current. This can be seen by considering the 741 operational amplifier in the d.c. feedback loop of figure 4.13; maximum voltage output = 15V, $R = 10^{10}\Omega$ and so maximum voltage current = 1.5 nA. Although this is sufficient

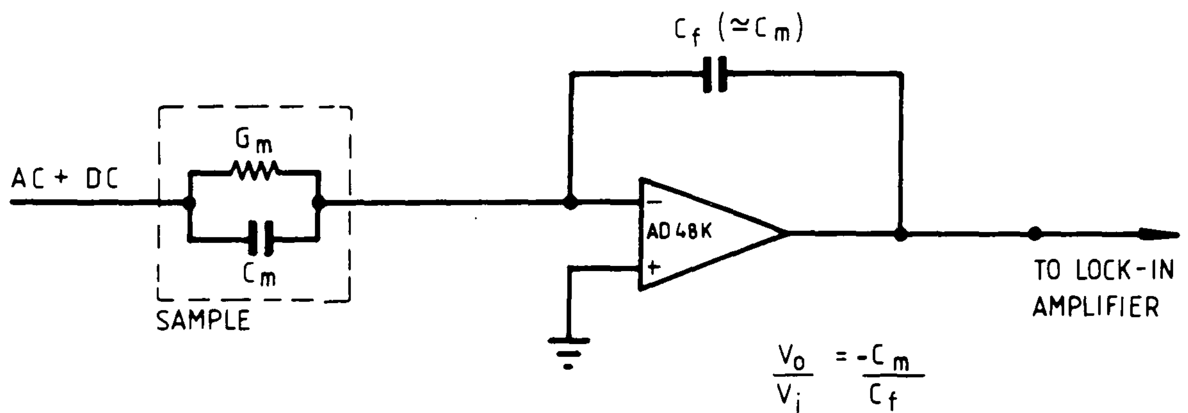


Figure 4.12a : Virtual earth amplifier - basic circuit

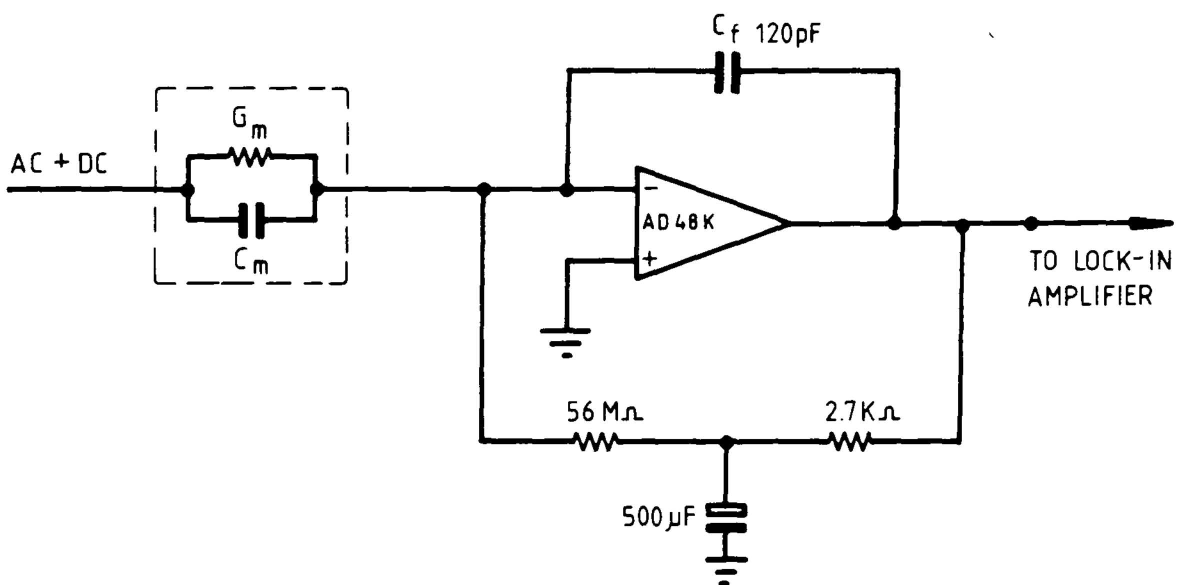


Figure 4.12b : Virtual earth amplifier with d.c. feedback path

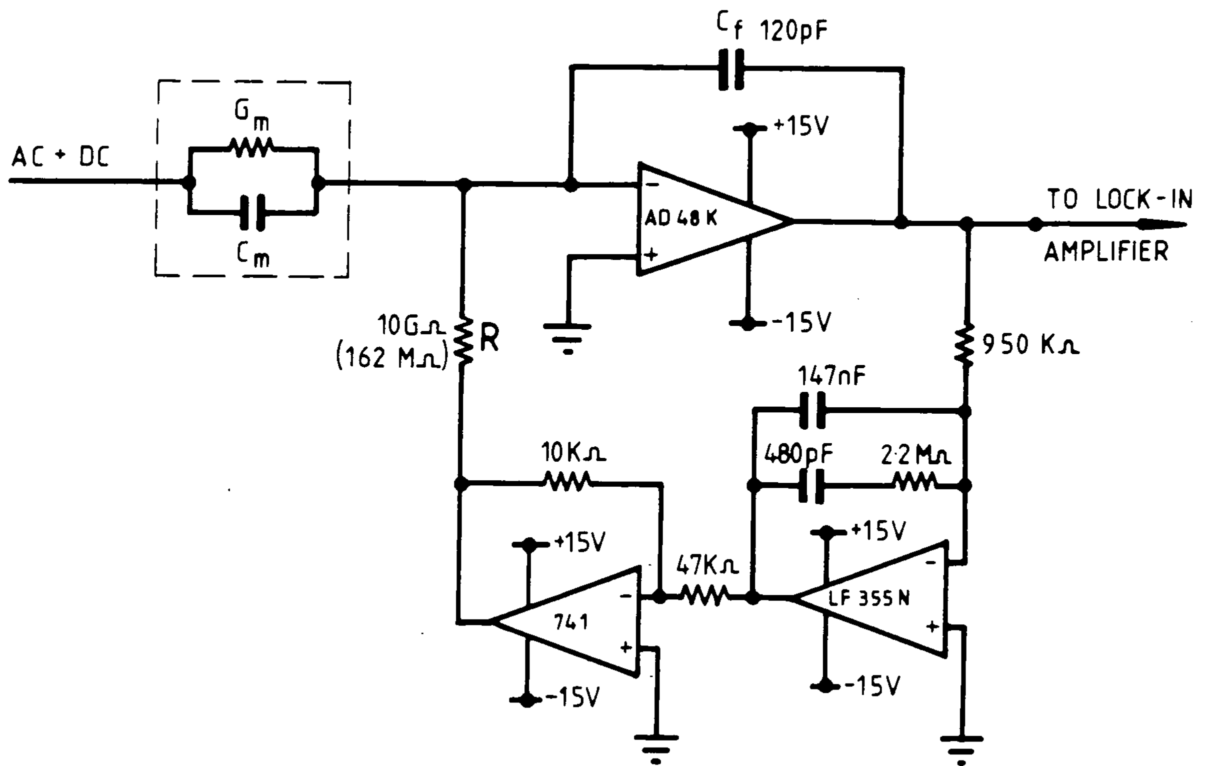


Figure 4.13 : Virtual earth amplifier with low-frequency roll-off and d.c. feedback

for the highly-insulating thick SiO_2 MIS samples (which will have very low d.c. leakage) used by Boudry and for which the circuit was developed, it is inadequate for use with more highly conducting structures such as Schottky barrier devices or those with thin film insulators[9]. Consequently, in the implementation of this circuit, the value of R was reduced to 162MΩ (this is shown in brackets on figure 4.13) to increase the current handling capability by about 60 times. Even so, if it is desired to measure samples which have very high d.c. leakage paths (e.g. thin, leaky oxides or Schottky barrier devices, etc.), the vea circuit described here will not function correctly and a charge- or current-sensing configuration such as those described in figures 4.11a and 4.11b will have to be used.

In practice, the vea was incorporated with the mixing and switching circuitry, as detailed in the next section.

4.2.7 Practical circuit considerations

In order to ensure that the signal remained at all times as free as possible from spurious noise and interference produced by external sources and other parts of the system, a number of preventitive measures were taken when designing the layout of the system and circuit boards.

Long cables are prone to pick up noise, especially as the signal level is small ($\sim$ 8mV rms), and so all interconnections were kept as short as possible. BNC connectors and single-core coaxial cable were used to carry the a.c. signal, even within the circuit box, and a common ground was adopted for the shielding; great care was taken with circuit layout so as not to produce earth loops. These measures are also important to reduce to a minimum frequency-dependent phase deviations which will be inherent in different stages of the system[6] due to lead capacitance, non-ideal components, stray capacitances, etc.

Protection from interference for the signal processing circuitry is accomplished by mounting the individual printed circuit boards in a shielded die-cast metal box. The circuit as implemented for the mixing, multiplexing and virtual earth amplifier stages is shown in figure 4.14. This circuit diagram includes details of the operational amplifier power supply (stablished $\pm$15V d.c. derived from 240V a.c. mains), which was carefully screened from the rest of the circuit by a metal plate. The lid of the box was marked with a schematic representation of the circuitry enclosed and each of the BNC sockets was labelled (figure 4.15).

4.2.8 The microcomputer controller

The instrumentation system described in the preceding sections is controlled by a Hewlett-Packard model 85 microcomputer[10] via a IEEE-488 digital interface. The basic microcomputer comes complete with integral screen and thermal printer, and this was fitted with a number of options; these include a 16 kilobyte Memory Module (giving 32 kilobytes total memory) and plug-in read-only memory (ROM) chips, which control the operation of the IEEE interface card and the HP9872C Graphics Plotter used to display the results.

The microcomputer can control a wide range of commercially-available instruments fitted with a suitable interface by using the IEEE-488 data bus[11], and this avoids having to write machine code driver routines to control individual devices. Both control codes and data can be transmitted to and from the controller (in this case the HP85) and instruments on the bus. These transfers are governed by the program being executed by the HP85. All programs were written in the high-level programming language BASIC; these are described in detail in the following chapter (section 5.1.4).

4.3 Summary

The technique of a.c. admittance measurement using a dual-phase lock-in amplifier has been discussed above, and it has been shown that the disadvantages inherent in using manually-operated equipment may be overcome by utilising a microprocessor to control instrumentation for data acquisition and interpretation. In this chapter, we have

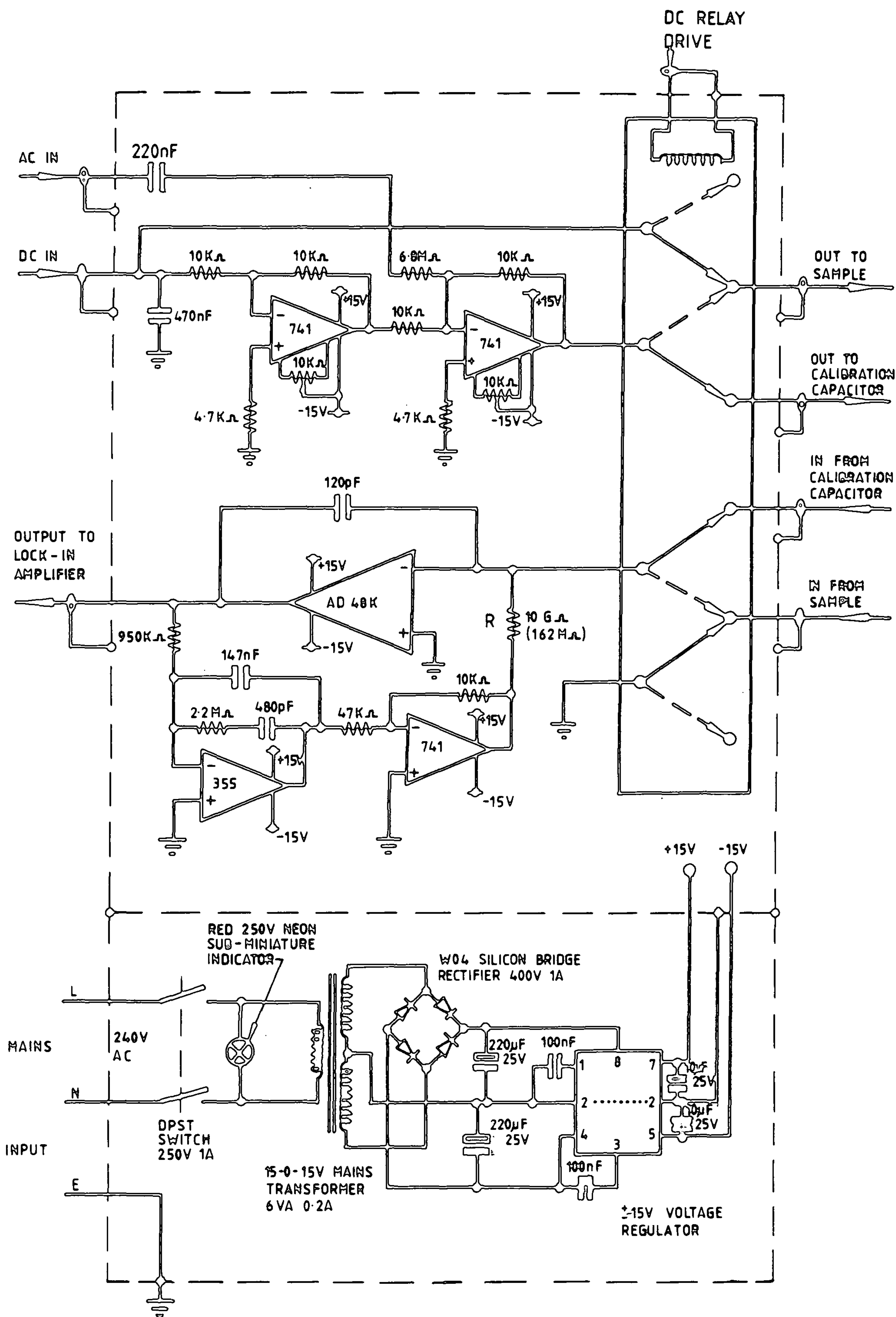


Figure 4.14 : Signal processing circuitry - implemented design

Figure 4.15 : Sample chamber and electronics box

Figure 4.16 : Instrumentation arrangement for automated a.c. admittance measurement

seen how such an admittance measurement system has been developed, and have considered in detail the operation of the whole system and each of its component parts. A photograph of the complete experimental arrangement is shown in figure 4.16.

Significant improvements have been incorporated into this instrumentation system. By careful consideration of sample chamber layout and electrical shielding, the problems of stray capacitance and noise interference have been greatly reduced. Also, by redesigning the a.c./d.c. mixing circuit the equipment is able to analyse MIS samples with thin or highly-conductive ("leaky") insulating layers (e.g. Langmuir-Blodgett films, as investigated in chapters 7 and 8), which could not before be measured by this technique.

The hardware information given here is complemented by chapter 5, which considers the operational procedure and software developed to both control the measurement of a.c. admittance and to determine the surface state density distribution of real MIS devices.

CHAPTER 5 : SYSTEM PERFORMANCE AND EXPERIMENTAL RESULTS

5.0 Introduction

The instrumentation system described in the previous chapter uses a microcomputer to automate the collection of a.c. admittance data over a wide range of signal frequencies and bias voltages. The programs written for this purpose are explained in this chapter along with the experimental procedures followed. The development of additional software to enable surface state desnity and surface potential information to be extracted from the basic admittance measurements is also discussed. Finally, the performance of the system is reviewed by analysing the surface state spectrum of a real MOS device and comparing the results with those obtained using proven, manual admittance measurement equipment; this culminates in a critical appraisal of the application of the technique for interface state analysis.

5.1 Operational procedure and software

The instrumentation system developed for admittance measurement (chapter 4) may be operated in either fixed-frequency, swept-voltage mode or fixed-voltage, frequency-scanned mode. In each of these two programs it is necessary to calibrate the apparatus at every new operating frequency to avoid phase errors in the psd reading of the in-phase and orthogonal signal components. However, the procedure for acquiring the basic C and G data for each point on the voltage-frequency map is the same for either mode of operation.

It should be noted that although the system has been developed primarily to enable C-ω and G-ω curves to be quickly obtained for N_{ss} analysis, the swept frequency mode will not be used exclusively. For example, C-V plots can provide valuable information about MIS samples which is not available from frequency scans, such as flat-band voltage, doping density, and insulator charge distribution (see section 3.1).

5.1.1 PSD calibration routine

The procedure to set up the lock-in amplifier at each new frequency is as follows:

Step 1 : Set new internal oscillator frequency and select appropriate time constant for phase sensitive detectors.

Step 2 : Select calibration capacitor and run "AUTOSET" routine (which zeroes Channel 2).

Step 3 : Read and calibrate Channel 1 (in terms of calibration capacitor value).

Step 4 : Apply $-\pi/2$ phase shift (exchanges channels).

Step 5 : Read and calibrate Channel 2 (psd channels are now set up so that Channel 1 displays G/ω and Channel 2 reads C)

If this procedure is being run as part of a voltage-scan program, the sample will now be switched in, the d.c. voltage generator will be swept between the limits set and the C-V, G-V readings taken (c.f. manually-operated system, section 4.1). However, if in swept-frequency mode the voltage will already have been fixed at the required value and the above routine will be repeated at each programmed frequency in order to record the C-ω and G-ω data. Further details of the programs are given in section 5.1.4.

5.1.2 Data acquisition

Information is displayed on each of the psd channels as a voltage representing either the conductive or capacitive component of the signal coming from the sample chamber; these voltages must be converted to the equivalent C and G/ω values before further processing.

These data are obtained for each point by the following procedure:

Step 1 : Read Channel 1 and Channel 2.

Step 2 : Convert readings to G/ω and C values.

Step 3 : (for frequency-sweep mode only) Calculate parallel G_p,C_p values

For both modes of operation (C-V, G-V and C-ω , G-ω) it is necessary to measure C and G at every frequency with the sample biased into strong accumulation, as these data are needed to calculate G_p and C_p (from which the interface state details are extracted, as described in section 3.2.2).

When operating in voltage-scan mode, the information is stored as measured conductance (G_m) and capacitance (C_m) against voltage at fixed frequency. In the frequency-scan mode, the values are converted into G_p and C_p versus frequency for a fixed bias voltage, and are recorded in this format.

The programs for both C-V, G-V and C-ω, G-ω operation are listed in Appendix A, and are described more fully in section 5.1.4.

5.1.3 Analysis of data and N_{ss} determination

Stored values of C_m and G_m versus bias voltage can be plotted directly, or in reciprocal capacitance-voltage form. This enables general information about the sample or more specific parameters, such as flat-band voltage, doping concentration and insulator fixed charge, to be calculated (see section 3.1). By comparing the C-V curve for a voltage ramped from accumlation to inversion with a similar curve for a sweep from inversion to accumulation, the hysteresis associated with the sample may be inspected (this gives an indication of the amount of mobile ionic charge in the insulator; see section 3.1.2).

Data gathered from swept-frequency experiments are analysed using the a.c. conductance technique described in section 3.2.2. The maximum G_p/ω point $(G_p/\omega)_{max}$ and the corresponding C_p are determined by inspection of the G-ω, C-ω plot; the variance σg of the conductance curve is determined by recording the G_p/ω value for a frequency ten times or one tenth of the peak frequency (whichever is more appropriate for the data plotted) and referring to tables[1]. From this, the statistical function $f_N(\sigma g)$ can be extracted, and with knowledge of the top electrode area A and other device parameters (doping concentration, semiconductor permittivity, oxide capacitance, temperature) the density of surface states, N_{ss}, and the corresponding value of surface potential, ψ_s, may be calculated from equations 3.21 and 3.24.

Repeating this data analysis procedure for G-ω, C-ω curves recorded for a range of bias voltages where a G_p/ω peak can be found enables the ψ_s-V_{bias} relationship to be investigated and the distribution of interface states across the semiconductor bandgap to be determined. The programs for curve plotting and calculation of N_{ss} and ψ_s are detailed in section 5.1.4 and Appendix A.

5.1.4 Software

The five main progams which were written for instrumentation control ("VSCAN" and "FSCAN"), results plotting ("VPLOTm" and "FPLOTp") and data analysis ("NssCAL") are listed in Appendix A. Other routines were developed for testing the instrumentation operation, for $1/C^2$ vs. V plotting and for hysteresis measurements, but as these are either very similar to the main programs (for example, the hysteresis program is essentially a routine to run "VPLOTm" twice - once from +V to -V and again from -V to +V) or not of particular interest, their listings have been omitted.

Each major program is described briefly below. Device addresses are defined as:

Address 705 - Hewlett Packard 9872C Graphics Plotter
706 - Brookdeal 5206 Two-Phase Lock-In Amplifier
707 - Time Electronics 9814 Voltage Calibrator
709 - Hewlett Packard 59306A Relay Actuator

Programe "VSCAN" : This program applies a voltage ramp at a fixed frequency and records values of Cm and Gm versus V_{bias}.

Lines 10-110	: Initialise IEEE-488 interface and devices, set timeout, and dimension arrays
Lines 120-255	: Display screen prompts and input system parameters (frequency; accumulation voltage and time; voltage ramp limits, speed and step size; Channel 1 x10 on/off; calibration capacitance; results display/storage details).
Lines 260-280	: Run "AUTOSET" routine for calibration capacitor at 1kHz to set up lock-in amplifier.
Lines 290-350	: Select programmed frequency and prompt for (manual) set-up of time constant . Calculate settling time (T ms) between readings (depending upon time constant, sweep speed).
Lines 360-380	: Run "AUTOSET" at selected frequency.
Lines 400-440	: Disable front panel controls, wait for T ms, read Channel 1 and calibrate (in pF).
Lines 450-470	: Invoke $-\pi/2$ phase shift and wait until settled.
Lines 500-520	: Read and calibrate Channel 2 (pF).
Lines 550-570	: Set up microcomputer key k1 (subroutine 9900), switch Relay 6 to select sample.
Lines 600-610	: Apply accumulation voltage and wait for time selected.
Line 620	: Read Channel 1 and Channel 2, returning values of Cm and Gm and calculating Cox and Rs (subroutines 8500, 9600).
Lines 640-650	: Set up voltage ramp, start ramp and read Channel 1 and Channel 2, returning values of Cm and Gm and calculating corresponding Cp and Gp (subroutines 8600 or 8700, 8800, 8500, 9700) until ramping finished.
Lines 750-770	: Switch out sample, remove phase shift and re-enable front panel controls.
Lines 790-810	: Send zero volts and call file storage routine if selected (subroutine 9550).

Lines 820-870	: Display Gp/ω peak, corresponding Cp and V bias, Rs and Cox if required.
Line 1000	: End.
Subroutine 7550-7520	: Output to internal printer (if called from subroutine 8500).
Subroutine 8300-8350	: Calculate parameters and send to lock-in amplifier to set up frequency selected.
Subroutine 8500-8560	: Read Channel 1 and Channel 2. Return Cm, Gm, V, and store in arrays. Print data if required (subroutine 7500), calculate Rs and Cox if in accumulation (subroutine 9600) or Gp/ω and Cp (subroutine 9700).
Subroutine 8600-8650	: Sets up -ve voltage ramp and calls voltage output and reading routine (subroutine 8800).
Subroutine 8700-8750	: Sets up +ve voltage ramp and calls voltage output and reading routine (Subroutine 8800).
Subroutine 8800-8840	: Sends voltage, waits for selected delay time and calls reading subroutine (8500).
Subroutine 9000-9090	: Input/output routine for lock-in amplifier. Do serial poll; check for previous command done. Output command, read incoming data (if any) and check for command done.
Subroutine 9200-9220	: Serial poll routine (called from subroutine 9000).
Subroutine 9300-9360	: Temporary pause in execution (set up in subroutine 9900 and called when key k1 on microcomputer pressed).
Subroutine 9500-9545	: Prompt filename, create data file and store frequency value.
Subroutine 9550-9590	: Store Cm, Cm and V arrays in data file.
Subroutine 9600-9640	: Calculate Rs and Cox from Cm and Gm in accumulation (called from subroutine 8500).
Subroutine 9700-9750	: Calculate Gp/ω and Cp and determine Gp/ωmax (Called from subroutine 8500).
Subroutine 9900-9920	: Set up microcomputer key k1 for temporary pause function.

Program "FSCAN" : This routine is similar to "VSCAN", but records Gp/ω and Cp at different frequencies for the same bias voltage. Many subroutines are identical to those for "VSCAN", and shall not be described in detail.

Lines 10-115	: Initialise IEEE interface and devices, dimension data arrays.
Lines 120-256	: Display screen prompts and input system parameters (frequency scan limits and increments; accumulation voltage and time; measurement voltage; time between readings; Channel 1 x10 on/off; calibration capacitance; results display/storage details).
Lines 260-280	: Run "AUTOSET" on calibration capacitor at 1kHz to set up lock-in amplifier.
Lines 290-340	: Select initial frequency, calculate settling time (T_{ms}) and time constant.

Lines 350-370	: If not at initial frequency, calculate and send new frequency.
Lines 380-400	: Wait until settled, then run "AUTOSET" at set frequency.
Lines 410-450	: Disable front panel controls, wait for T ms, read Channel 1 and calibrate (pF).
Lines 460-480	: Invoke $-\pi/2$ phase shift and wait until settled.
Lines 500-520	: Read and calibrate Channel 2 (pF).
Lines 550-610	: Set up key kl, switch Relay 6 to select sample, apply accumlation voltage and wait for selected time.
Line 620	: Read Channel 1 and Channel 2, returning values of Rs and Cox (subroutines 8500, 9600)
Lines 630-640	: Apply measurement voltage and wait until settled.
Line 650	: Read Channel 1 and Channel 2, returning values of Cp and Gp/ω.
Lines 750-780	: Switch out sample and remove phase shift.
Line 790	: Repeat measurement procedure for next frequency (i.e. go back to step 350).
Lines 800-840	: Re-enable front panel controls, send zero volts, call file storage routine if selected (subroutine 9550).
Lines 850-890	: Display Gp/ω peak information, Rs and Cox
Line 1000	: End.

Subroutine 7000-7040	: Calculate logarithmic frequency increment.
Subroutine 7100-7140	: Calculate linear frequency increment.
Subroutine 7500-7520	: Output to internal printer.
Subroutine 8300-8390	: Calculate parameters for frequency and time constant and send to lock-in amplifier
Subroutine 8500-8540	: Read Cm and Gm/ω and calculate Rs and Cox in accumulation (subroutine 9600) or Cp and Gp/ω (subroutine 9700).
Subroutine 9000-9090	: Input/Output routine for lock-in amplifier.
Subroutine 9200-9220	: Serial poll routine.
Subroutine 9300-9360	: Temporary execution pause.
Subroutine 9500-9545	: Create data file; store measurement voltage.
Subroutine 9550-9590	: Store Gp/ω, Cp and F arrays in data file.
Subroutine 9600-9640	: Calculate Rs and Cox from Cm and Gm/ω in accumulation.
Subroutine 9700-9750	: Calculate Gp/ω, Cp, F at measurement voltage and store in arrays; determine Gp/ω max.
Subroutine 9900-9920	: Set up key kl for temporary pause.

Program "VPLOTm" : This program retrieves Gm, Cm and V information from a "VSCAN" data file and produces a plot of Cm and Gm/ω versus V_{bias}.

Lines 5-9	: Initialise plotter and prompt for data file name.
Lines 10-16	: Assign file as input; read frequency and calculate ω.
Lines 20-40	: Read in Gm, Cm and V data and determine maximum values of Gm/ω and Cm.

Lines 50-55	: Calculate scales for V, Cm, Gm/ω.
Lines 60-95	: Scale, draw and label x-axis and y-axis for Cm data.
Lines 100-152	: Read data and plot Cm versus Vbias.
Lines 153-157	: Scale, draw and label y-axis for Gm/ω data.
Lines 160-210	: Read data and plot Gm/ω versus V bias.
Lines 220-230	: If another plot is required, go back and complete plot.
Line 250	: End.

Program "FPLOTp" : Plots Gp/ω and Cp versus frequency from "FSCAN" data stored on file.

Lines 5-15	: Dimension data arrays and initialise plotter.
Lines 20-35	: Prompt for filename; assign file as input and read measurement voltage.
Lines 40-100	: Read Gp/ω, Cp and f data into arrays and determine maximum values of Gp/ω and Cp.
Lines 105-190	: Calculate scales for log f, Gp/ω and Cp. Scale , draw and label x-axis and y-axis for Gp/ω data.
Lines 200-230	: Read data arrays and plot Gp/ω vs.f.
Lines 250-320	: Scale, draw and label y-axis for Cp data.
Lines 325-360	: Read data arrays and plot Cp vs.f.
Lines 440-450	: Prompt for another plot or another copy. Execution terminated at line 450 if no more plots required.

Program "NssCAL" : This routine calculates Nss and ψ_s from data acquired from analysis of Gp/ω - ω curves.

Lines 10-60	: Enter device details (semiconductor permittivity, doping concentration, temperature, top electrode diameter) and copy to internal printer.
Line 70	: List of constants (k, q, εo).
Lines 80-130	: Prompt for plot details (plot reference, voltage, frequency and value of peak Gp/ω and corresponding Cp, variance function).
Line 140	: Calculate surface potential (ψ_s) in eV
Line 150	: Calculate surface state density (Nss) in cm^{-2} eV^{-1}.
Lines 160-200	: Print results and go back to enter details for next point.

5.2. Performance Assessment and Results with real MOS device

To ensure that the micrcomputer-controlled a.c. admittance instrumentation was functioning correctly and that an accurate determination of interface state density and surface potential was being obtained, the errors associated with the calculations and measurements were investigated (see section 5.2.1).

The operation of individual instruments in the system was tested with simple diagnostic equipment (signal generator, digital multimeter and oscilloscope as appropriate) and it was observed that each was functioning correctly (see section 4.2). In addition, the system as a whole was checked by performing C-V, G-V and C-ω, G-ω studies on a thick oxide MOS capacitor and comparing the results with those obtained for analysis of the same device with a manual a.c. admittance bridge (sections 5.2.2. and 5.2.3). The different measurement techniques are reviewed in section 5.2.4.

5.2.1. Accuracy of measurement

Referring to section 3.2.2., the degree of accuracy to which N_{ss} and ψ_s can be determined depends upon the errors in measuring the parameters from which these values are calculated.

Re-writing equations 3.21 and 3.24:

$$N_{ss} = \frac{1}{qA}\left(\frac{G_p}{\omega}\right)_{max} \Big/ f_N(\sigma_g) \tag{5.1}$$

$$\psi_s = \frac{kT}{q} + \frac{q\varepsilon_r\varepsilon_o N_d A^2}{2(C_p - qAN_{ss})^2} \tag{5.2}$$

Errors on k, q, ε_o, ε_r

These values are all constants (k = Boltzmann's constant, q = electronic charge, ε_o = permittivity of free space, ε_r = dielectric constant of silicon), and so the error associated with them is zero.

Error on T

All experiments were performed at room temperature (285-295°C), which was measured to an accuracy of ±0.5^{o}C. Therefore, the maximum possible error in determing T was ∿ 0.175% (±0.5^{o}C on 28.5^{o}C), which is negligable compared with the errors on other readings (see below).

Errors on A, A^2

For all MIS devices used in surface state analysis experiments, the same evaporation mask was used for top electrode deposition. The diameter of each top electrode was nominally 1.25mm ±0.01mm (a micrometer was used to measure the diameter of the drill bit used to machine the holes in the mask), but after careful examination of deposited electrodes with a travelling microscope, it was found that a small deviation in contact size was observed due to inconsistancies in machining and non-uniformity of the contacts evaporated onto the sample. As a result, the practical diameter of electrodes was taken as 1.25mm ±0.025mm, giving an error of 4% on device area, A, and 8% on A^2.

Error on N_d

The semiconductor doping concentration, N_d, is determined by examining C-V curves and referring to tables [2]; as an additional check, a plot of $1/C^2$ vs. V in depletion may be used to find N_d (section 3.1.3). C_{min} and C_{max} (=C_{ox}) for C-V curves may be measured very accurately by retrieving the original data stored

for the C-V run, and the C_{min}/C_{ox} ratio can be calculated to ±1%; from tables, N_d may be determined to ±3% or better. From the slope of $1/C^2$ vs. V response, N_d can be found from equation 3.5 with an accuracy of approximately ±7%.

Errors on $(G_p/\omega)_{max}$, Cp

These are measured from G_p/ω-ω and Cp-ω plots, and errors are typically ±0.5mm on 100mm (i.e. ±0.5%). Two measurements from each plot are needed to calculate absolute values (i.e. readings must be scaled), resulting in a total error of ±1% on each calculation of $(Gp/\omega)_{max}$ and corresponding Cp.

Error on $f_N(\sigma_g)$

After calculating curve variance σ_g from $(Gp/\omega)_{max}$ and Gp/ω at ten times or one tenth of the maximum frequency, $f_N(\sigma_g)$ may be found to an accuracy of ±2% or better.

Errors on determination of N_{ss} and ψ_s

Using the error values calculated above, the accuracy of surface state density, N_{ss}, is determined from equation 5.1 to be approximately ±6% or better. For equation 5.2, the percentage error on the second term is 15% at worst, and therefore the total error varies with the magnitude of ψ_s due to the constant first term (kT/q). This variation may be summarised approximately as follows:

For 0.03eV $<\psi_s>$ 0.05eV, error ∿ 1% - 7%
For 0.05eV $<\psi_s>$ 0.1 eV, error ∿ 7% - 10%
For 0.1 eV $<\psi_s>$ 0.2 eV, error ∿ 10% - 13%
For 0.2 eV $<\psi_s>$ 0.8 eV, error ∿ 13% - 14%

These error assessments were applied to all subsequent determinations of N_{ss} and ψ_s. However, it should be noted that these values apply only to absolute calculations of interface state density and surface potential. In practice, since only the relative position of these values is important when measuring the distribution of surface states, the effective errors will be for less. Because the same sample is being used for each evaluation of N_{ss} and ψ_s the values of N_d, A and A^2 will be constant, and errors in their calculation will not affect the relative positions of the points plotted on a graph of N_{ss} versus ψ_s (see section 5.2.2). Consquently, the N_{ss} - ψ_s relationship is known more accurately; by inspection of equations 5.1 and 5.2, N_{ss} is determined to within ± 2% and ψ_s to ±4% or better.

5.2.2. Characterisation of "standard" MOS Device

To test the correct operation of the automated instrumentation, a sample was prepared as described in Appendix B1 by depositing Pd top electrodes onto a 105nm thick layer of SiO_2 on bulk n-type silicon to which ohmic back contact had been made (sample N1). Measurements were carried out on this sample to determine the doping density N_d and the interface state density distribution N_{ss} across the bandgap.

The C-V relationship at 100kHz for this device is shown in figure 5.1. The maximum and minimum values of capacitance are 157.0pF and 401.2pF, giving a $C_{min}:C_{max}$ ratio of 0.390. From tables [(2)], this corresponds to a doping density of approximately 2.4×10^{15} cm^{-3} ($=2.4 \times 10^{21}$ m^{-3}).

The corresponding $1/C_D^2$ vs V plot for these data around the depletion region is presented in figure 5.2. It can be seen that in depletion the points lie on a straight line. From the slope of this line, the average doping density was determined as described in section 3.1.3. to be 2.8×10^5 cm^{-3} ($= 2.8 \times 10^{21}$ m^{-3}), which is in close agreement with that found using the $C_{min}:C_{max}$

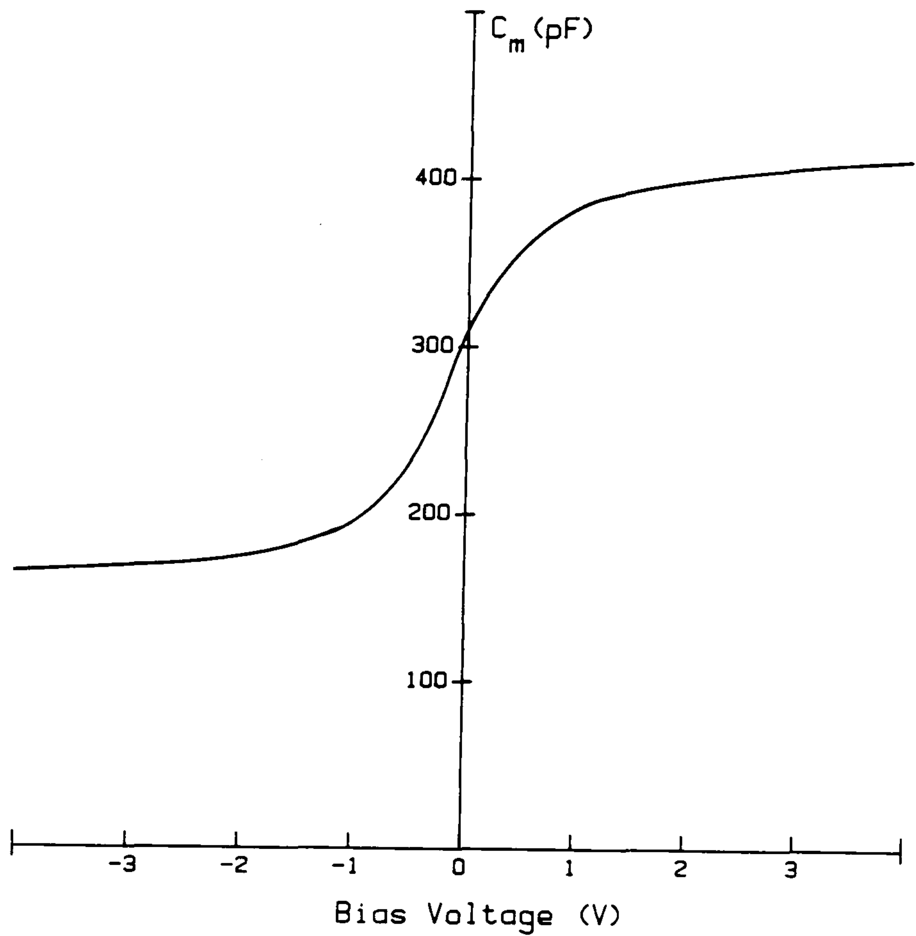


Figure 5.1 : Capacitance-voltage plot at 100 kHz for thick oxide MOS device (Sample N1)

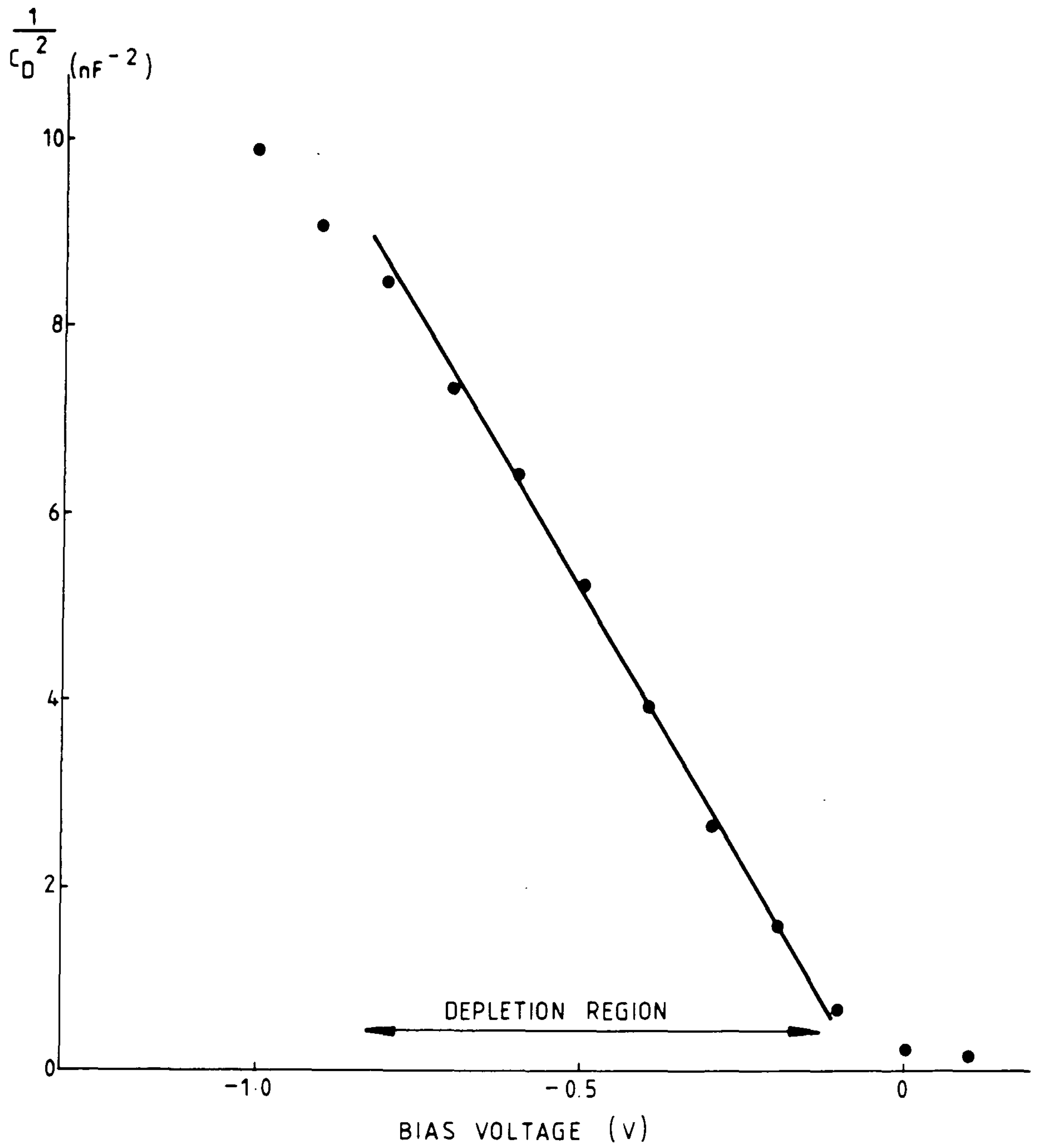


Figure 5.2 : Plot of $1/C_D^2$ versus bias voltage at 100 kHz for thick oxide MOS device (Sample N1)

technique. The value of doping density used in further calculations was the average of these two results, i.e. $N_d = 2.6 \times 10^{15}$ cm^{-3} (= 2.6×10^{21} m^{-3}).

The interface state density distribution was determined by performing a number of automated swept-frequency/constant-bias runs and recording the capacitance and conductance responses. Figure 5.3 depicts some of the resulting Gp/ω - f plots obtained from these sweeps; only eight of the total fifteen curves are shown for the sake of clarity. After finding the height and position of the Gp/ω peak and determining the curve variance and Cp value at $(Gp/\omega)_{max}$ (as described in section 5.1.3) for each graph, the ψ_s - V_{bias} and N_{ss} - ψ_s relationships were plotted.

In figure 5.4 the variation of surface potential with applied bias is shown. The shape of this curve agreed closely with the theoretical data computed by Goetzberger[2] for a device of similar oxide thickness and doping density, with only a lateral shift observed (which is attributable to trapped charge in the oxide); this gave a good indication that the system was operating correctly (or, at least, producing reasonable results!). By measuring ψ_s from the curve rather than from the individually-calculated readings, any possible errors due to surface potential fluctuations (see section 3.2.2) may be minimised.

Having determined ψ_s in this way, the interface state density distribution was plotted against energy position in the silicon bandgap (this may be obtained by evaluating the Si Fermi level, knowing impurity concentration and temperature[3], and relating to ψ_s; $\psi_s = \emptyset$ at the Fermi energy). The resulting graph appears as figure 5.5. This shows that the surface state density in the upper half of the silicon bandgap varies between approximately 3×10^{11} cm^{-2} eV^{-1} and 5×10^{11} cm^{-2} eV^{-1}; this is of the same order as N_{ss} determinations by other researchers [4, 5, 6] using the conductance technique and other methods. The inverted-V shape of the curve is characteristic of oxides grown in dry oxygen [7],

Figure 5.3 : G_p/ω versus frequency information recorded by automated system at different bias voltages (Sample N1)

Figure 5.4 : Surface potential versus bias voltage relationship for thick oxide MOS device (Sample N1)

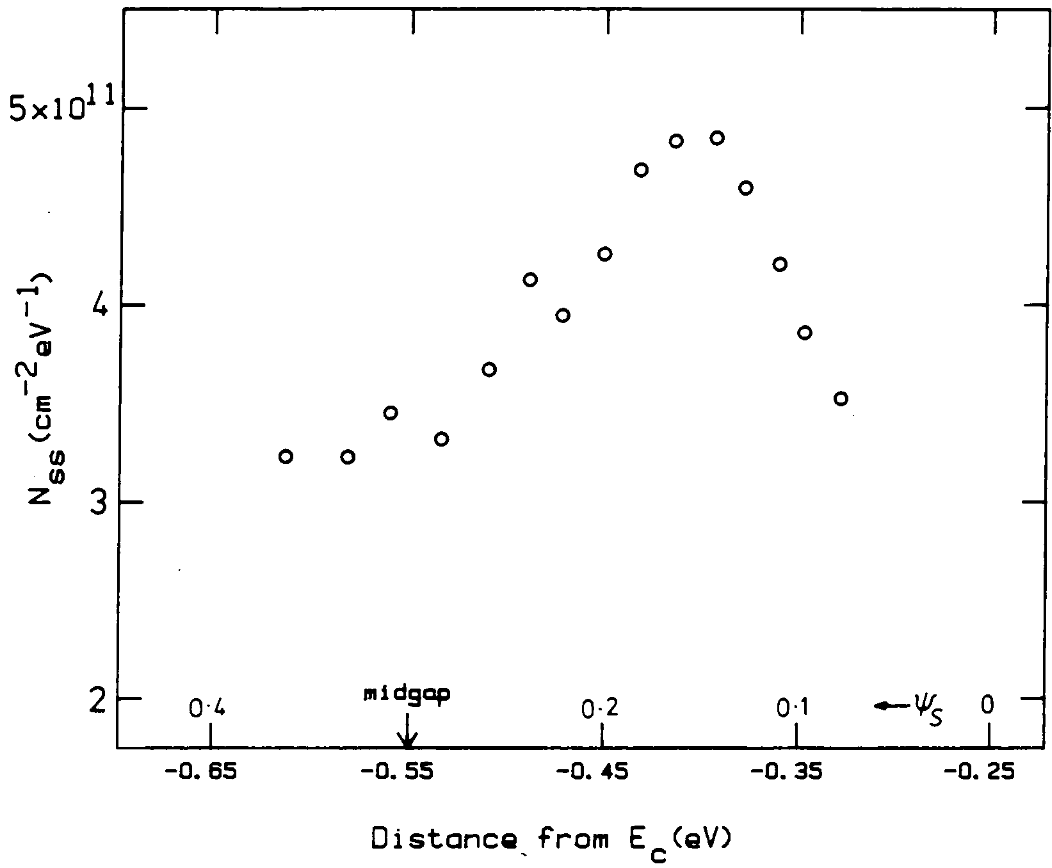


Figure 5.5 : N_{ss} - Ψ_s relationship recorded by automated system for sample N1 (thick oxide MOS)

which have a high interface trap density distribution across the silicon bandgap. This may be reduced, as discussed later (section 6.3.3), by annealing the sample.

Although the results presented above, obtained with the microcomputer-controlled measurement system, were in agreement with the work of other researchers, it was felt necessary to verify the accuracy of the system conclusively by performing similar experiments with a manual system as described in section 4.1.

5.2.3 Checking results with manual system

Using the experimental arrangement shown in figure 4.1., a number of manual C-V, G-V runs (section 4.1) were carried out on sample N1 (a 105 nm oxide Pd-SiO_2-Si MOS capacitor; see section 5.2.2) over a range of signal frequencies between 100Hz and 100kHz. From this information, C_m and G_m were measured at 0.1V intervals for each frequency and these data used to construct a G_p/ω versus frequency graph. At the peak conductance value, C_p and G_p/ω were calculated and the corresponding N_{ss} and ψ_s determined.

The resulting plots are shown as figures 5.6 (G_p/ω vs. f) and 5.7 (N_{ss} vs. ψ_s); for each graph the manually-determined points are superimposed onto the curves obtained previously with the automated system so that a direct comparison may be made. It can clearly be seen that there is very close agreement between the two sets of data; this verifies the ability of the microprocessor-controlled system to accurately measure a.c. admittance and to correctly calculate the interface state density versus surface potential information from the data thus obtained. Moreover, the advantages of the automated system in terms of efficiency of data collection and interpretation are clearly demonstrated when compared with the number of manual C-V/G-V plots required to extract the same information.

PREVIOUS RESULTS (AUTOMATED SYSTEM)

MANUAL RESULTS

□ −0·5V
● −0·4V
△ −0·3V
■ −0·2V
× −0·1V
○ 0·0V
+ 0·1V
▲ 0·2V

Gp/ω (pMho/Hz)

FREQUENCY (kHz)

Figure 5.6 : Comparison of G_p/ω - f information measured by automated and manual admittance measurement system

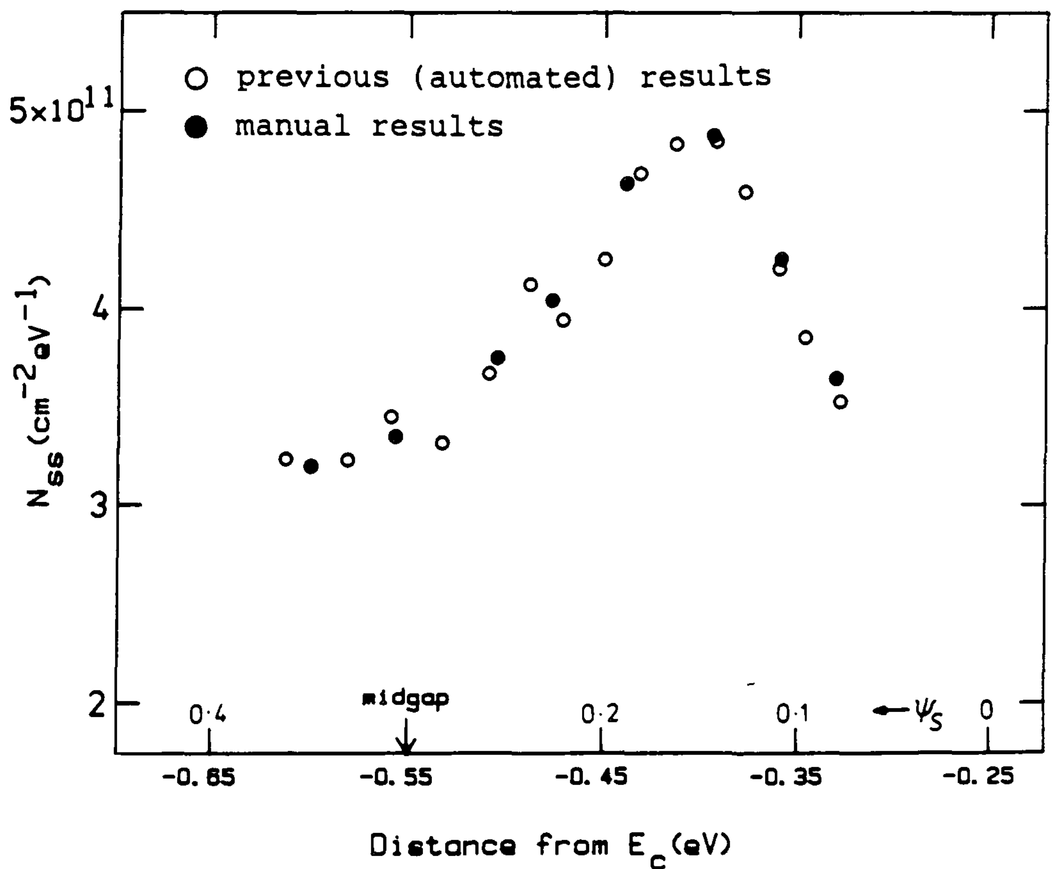


Figure 5.7 : Comparison of N_{ss} - ψ_s information recorded by automated and manual admittance measurement

5.2.4. Critical Appraisal of $N_{ss} - \psi_s$ determination methods

The most accurate method of interface state density evaluation is the conductance technique of Nicollian and Goetzberger [4], as discussed earlier (section 3.2.2), and this has been confirmed experimentally by these and other researchers [4, 8, 9]. However, care must be taken when applying this technique to investigate the interfacial properties of practical devices, due to the problems associated with taking measurements over a range of frequencies.

The conventional approach of performing a number of bias voltage scans at different frequencies is obviously wasteful as only a small amount of the information gathered for each scan will be of use; only those points where there is a parallel conductance peak within the frequency range of the equipment are required to calculate N_{ss} and ψ_s. By performing a frequency scan whilst maintaining constant bias, this redundancy may be reduced, but the equipment must be recalibrated at each new frequency and a protracted curve-fitting procedure must be followed. The Simmone[10] method simplifies this somewhat, but still requires the G_p/ω peak magnitude and frequency to be determined (see section 3.2.2). It has been suggested [11] that this technique may be improved by evaluating the conductance peak in the voltage domain, adjusting the frequency by a factor of 5 at the peak bias, and then finding the new value of G_p/ω, the information obtained being equivalent to that extracted from a frequency scan at the peak bias value. However, although these data may be acquired without the need for repeated recalibration of equipment, as frequency is only changed once, there is no proof that the conductance peak observed for a voltage scan at fixed frequency will be the same as the peak obtained from a swept-frequency experiment.

Figure 5.8 shows the relationship between G_p/ω, V_{bias} and frequency determined experimentally by performing a number of voltage sweeps at fixed frequency on a metal-oxide-semiconductor

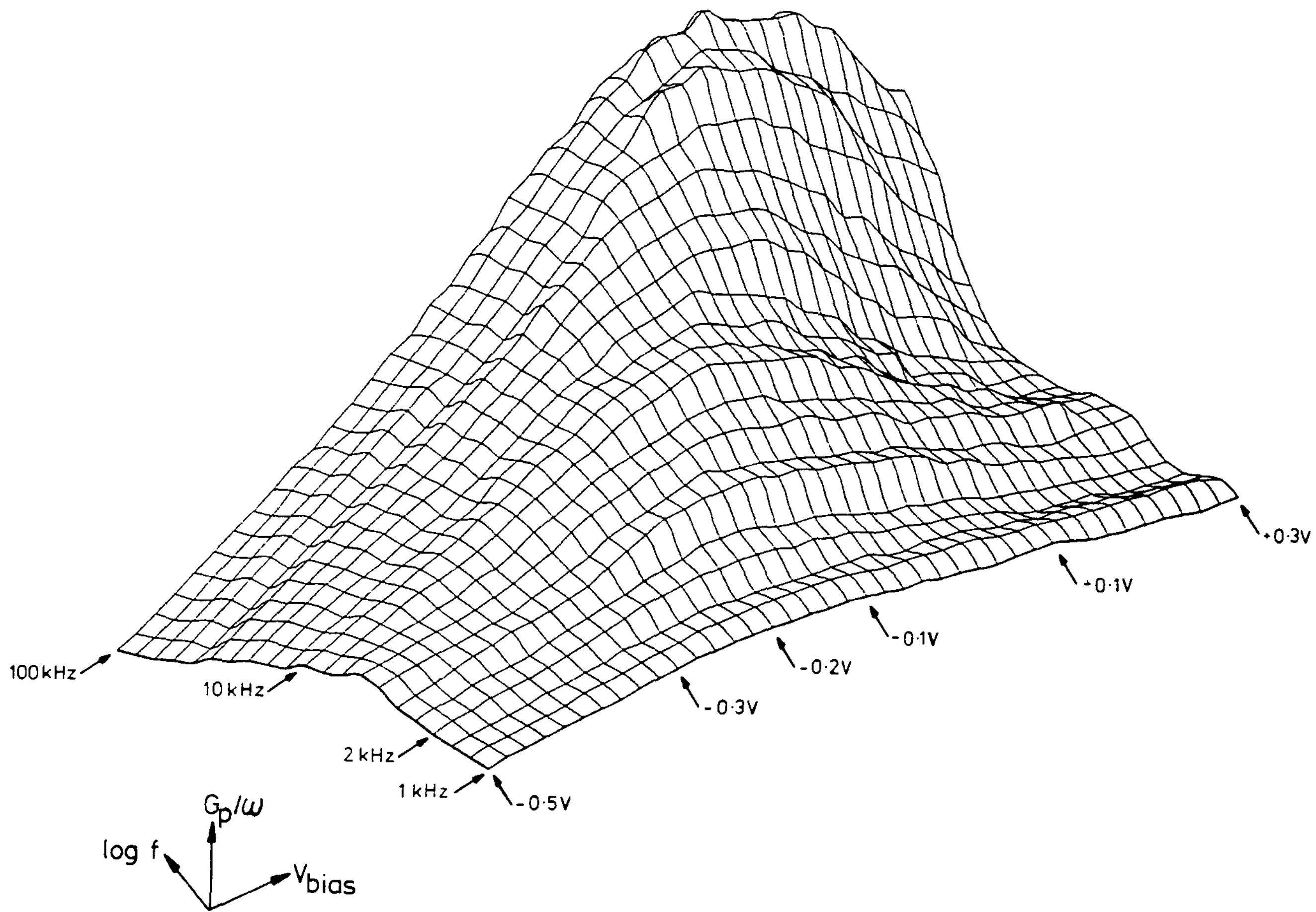


Figure 5.8 : G_p/ω - V_{bias} - log f relationship for thick oxide MOS device

device (sample N1). From this plot, it can be seen that a conductance peak identified from a voltage scan is not necessarily the peak value when operating in swept-frequency mode. For example, the G_p/ω peak for a swept-voltage experiment at 2kHz is at -0.2V; however, the conductance peak obtained from a frequency scan at -0.2V is not positioned at 2kHz but at 40kHz. Therefore, in order to correctly identify the conductance peak for N_{ss} and ψ_s determination it is essential to perform a frequency scan and follow the curve-fitting procedure described earlier. Unfortunately, there is no short-cut to obtain the required data, although it is possible to define a range of bias voltages for which a conductance peak will be observed when a frequency scan is performed. This is done by executing a high-frequency and a low-frequency voltage scan and recording the voltage at which the G_p/ω peak appears in each case; frequency sweeps at bias voltages between these limits will ensure that a peak is detected.

One further problem which occurs when measuring MOS structures is the need to correct the measured values of conductance and capacitance for the effects of oxide capacitance C_{ox} and series resistance R_s. C_{ox} may be considered to be constant (as the oxide permittivity is virtually frequency-independent), but R_s may vary considerably with frequency (section 3.2.2). This is particularly important in conductance measurements, as failure to compensate for series resistance can result in non-detection or incorrect identification of peak location and magnitude. Figures 5.9(a) and 5.9(b) show the high- and low-frequency variation of C_p-V and G_p/ω-V curves calculated with a range of R_s values compared with the correct value obtained from measurement in accumulation. It is clear that correct peak location is not possible without this information, as in the cases where R_s is either too large (and the peak height is reduced, if apparent at all) or too small (where the values of G_p/ω in accumulation are larger than the peak height); this is reinforced by the plot of series resistance versus frequency in figure 5.10 which shows that series resistance varies inversely with

Figure 5.9a : Variation of C_p - V and G_p/ω - V curves with changing R_s at 100 kHz

Figure 5.9b : Variation of C_p - V and G_p/ω - V curves with

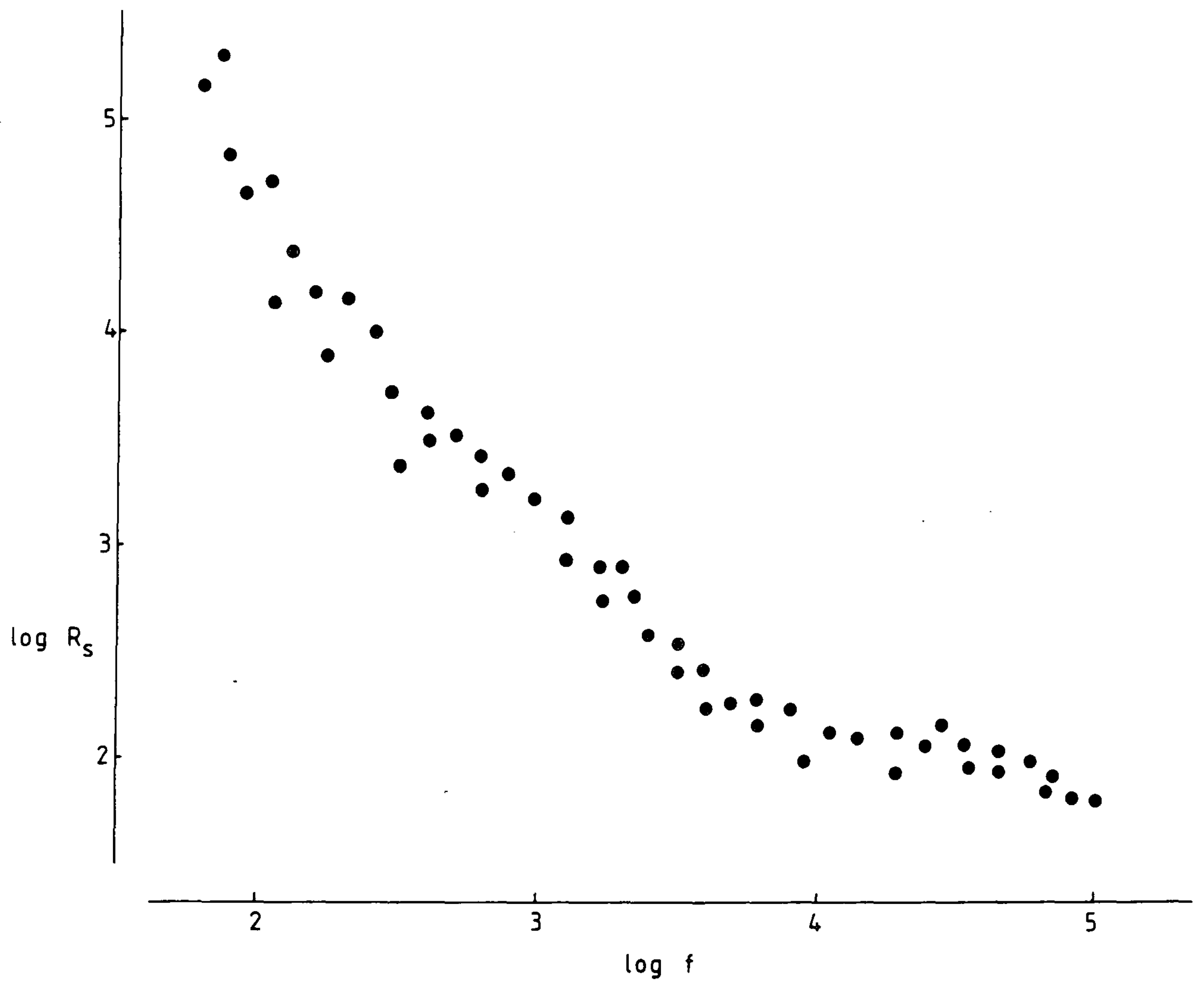


Figure 5.10 : Variation of R_s with frequency

frequency (which would be expected, since conductance is generally proportional to frequency), although this relationship is slightly non-linear.

In conclusion, then, it has been shown that in order to apply the conductance technique of Nicollian and Goetzberger, it is necessary to obtain the parallel conductance peak in the frequency domain as originally propounded; furthermore, the series resistance must be calculated at each new measurement frequency so that these conductance data may be correctly extracted from the measured readings as described in chapter 3 (section 3.2.2.). This procedure was followed for all interface state results presented in this thesis.

5.3 Summary

The instrumentation system developed in this work for a.c. admittance measurement and evaluation of surface state density of MIS devices has now been considered in detail. Chapter 4 described the hardware improvements made, and the present chapter has examined the software routines written to control the equipment and to process data.

The operational procedures for correct surface state analysis have been discussed, and the system has been proved capable of determining this information accurately. This was achieved by calculating the $N_{ss} - \psi_s$ relationship for a practical MOS device; the results obtained with the novel, automated system agreed very closely with the values calculated from similar experiments carried out on manual admittance measurement equipment. A detailed study of the method of calculating the surface state spectrum from admittance data has been presented, and the possible sources of error indicated; by careful analysis of results, these may be eliminated.

The automated system offers a great advantage over similar manual systems in that there is a large saving in operator time and effort; it is now possible to calculate the distribution of states at the insulator-semiconductor interface of a MIS structure in a matter of hours instead of days. In the following chapter , this system will be exploited to perform detailed analysis of the influences of different gases and of various sample treatment processes on the surface state density of palladium-gate MOS devices.

CHAPTER 6 : GAS EFFECTS ON PALLADIUM GATE MOS STRUCTURES

6.0 Introduction

When a gas comes into contact with a metal-insulator-semiconductor structure, any resultant change in the electrical properties of the device will be reflected in the capacitance-voltage characteristic. Considering the basic MIS device of figure 6.1, three possible areas of influence may be identified. In the case where gas affects only the top electrode metal and metal/insulator region it is likely that the work function of the device will change, resulting in a lateral shift in the C-V response (figure 6.2a) as considered in section 2.1.3. Should the gas influence the insulator properties (e.g. by altering insulator permittivity), the value of capacitance will be altered (as $C = A\varepsilon/d$; equation 3.6) and there will be a correspondning change in the vertical curve position (figure 6.2b). Alternatively, or in addition to either or both of the above, if the gas penetrates to the insulator/ semiconductor interface then surface states may be created or removed. This may result in a change in both the vertical and horizontal C-V characteristic (figure 6.2c), as discussed in section 3.2.1, and so the effect on surface states may only be fully quantified by the analysis technique introduced in chapter 3 (section 3.2.2).

The most extensively researched metal/gas system is that of palladium and hydrogen. A number of recent publications[1-4] have reported on the effects of hydrogen gas on MOS structures based on silicon/silicon dioxide with palladium metal top electrodes; some workers [5-7] have utilised this combination as a practical hydrogen sensor. There is a difference of opinion as to the degree of hydrogen interaction with $Pd/SiO_2/Si$ devices. It is not clear whether the gas influences just the metal-insulator surface or permeates the insulator and changes the distribution of states at the SiO_2/Si interface; the possible mechanisms are considered in more detail in section 6.1.

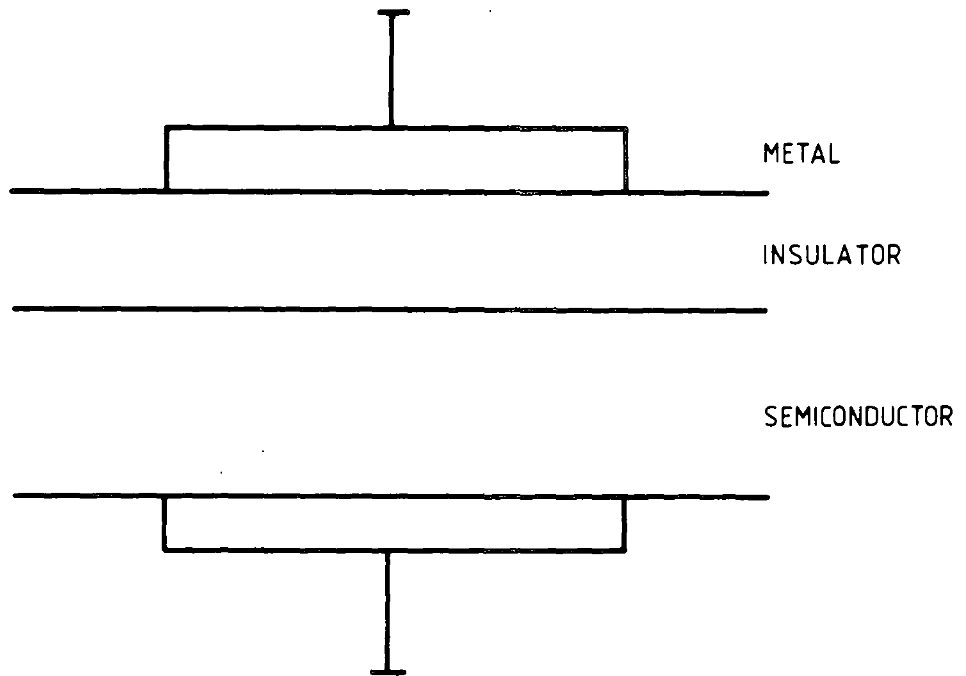


Figure 6.1 : Basic MIS Structure

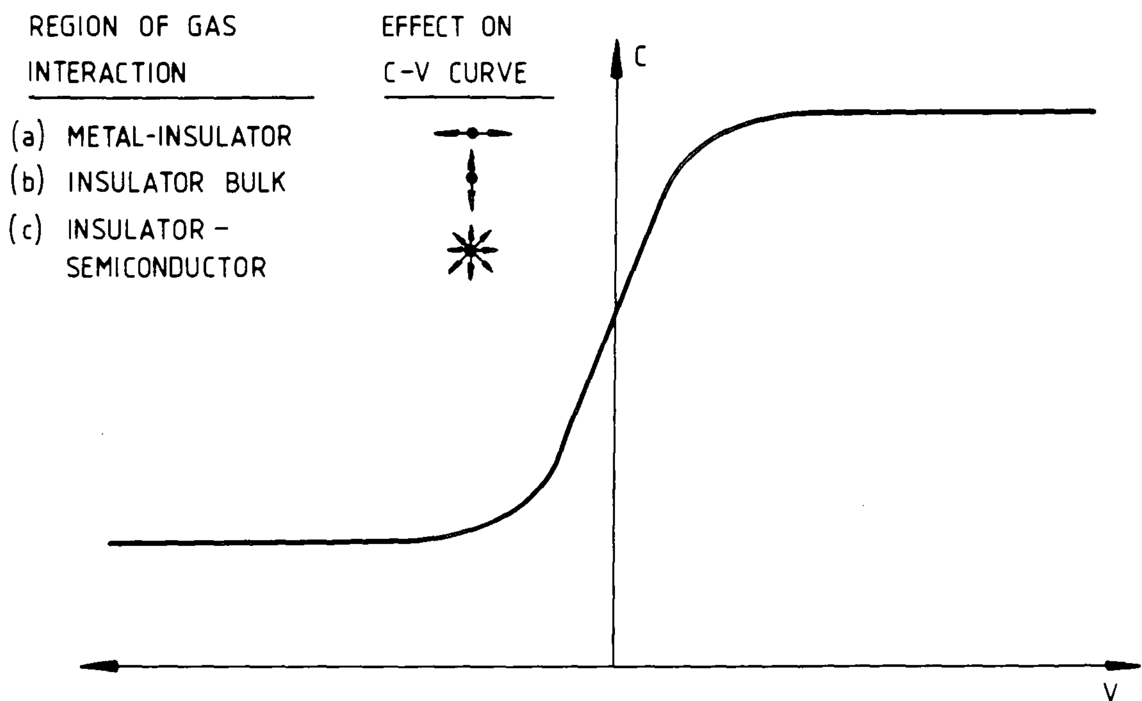


Figure 6.2 : Possible effects on C-V characteristics of gas interaction with various regions of MIS device

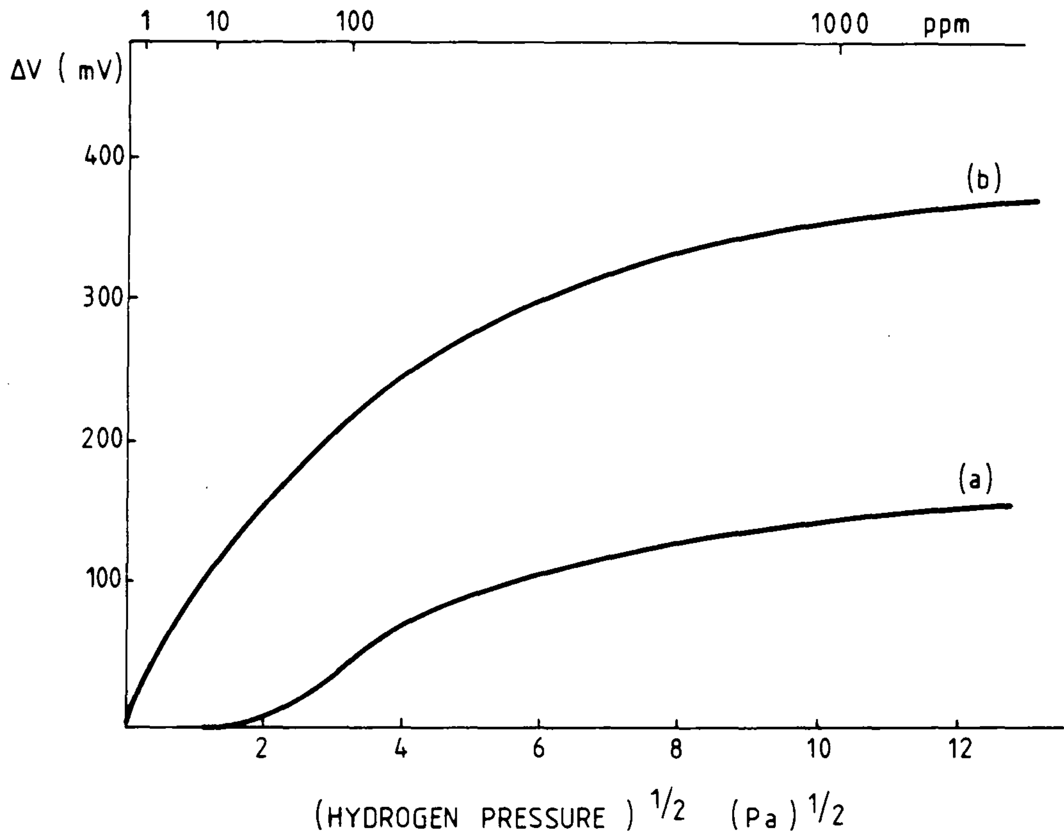
The equipment developed for MOS surface state analysis in different gas atmospheres has been used in an attempt to resolve this controversy, and the resulting effects of hydrogen gas on device properties are discussed below. Preliminary experiments carried out with other gases are also reported.

6.1 Hydrogen Interactions with Pd-gate MOS devices

Depending upon its oxide thickness, d_{ox}, a Pd/SiO_2/Si device may behave as a Schottky diode (d_{ox} <5nm) or as a MOS capacitor (d_{ox} >10nm). Although the precise nature of the physical processes involved in the adsorption and desorption of H_2 is not clear, it is now well established that exposure to the gas will result in a change in metal work function, altering the effective barrier height of the Schottky diode or the flat-band voltage, V_{FB}, of the MOS capacitor (figure 6.3); this is the principle of operation of some practical detectors [5-7] which are capable of measuring very low concentrations of hydrogen. It is also thought that the hydrogen may change the density of SiO_2/Si surface states in some way. These two mechanisms will be consdered below.

6.1.1 Work function changes

The flat-band voltage shift mentioned above has been attributed[8-11] to the catalytic dissociation of adsorbed H_2 gas at the palladium surface. It is believed that a fraction of the hydrogen atoms produced migrate through the metal to the Pd-SiO_2 interface, where they form a dipole layer, their electrons being displaced slightly towards the top electrode (figure 6.4,(a)). Consequently, the effective work function of the palladium is altered, and this is observed as a lateral shift towards negative voltage in the C-V and G-V responses of the MOS capacitor, as demonstrated in figure 6.5. This shift may be considered as a result of the dipole attracting negative charge to the Pd-SiO_2 surface. In an n-type device this will have the effect of producing accumulation of electrons under zero bias conditions, and the rise in capacitance



(a) Pd-SiO_2-Si SCHOTTKY DIODE

(d) Pd -GATE MOS CAPACITOR

<u>Figure 6.3 : Voltage shift observed in Pd - SiO_2 - Si structures due to exposure to hydrogen</u>

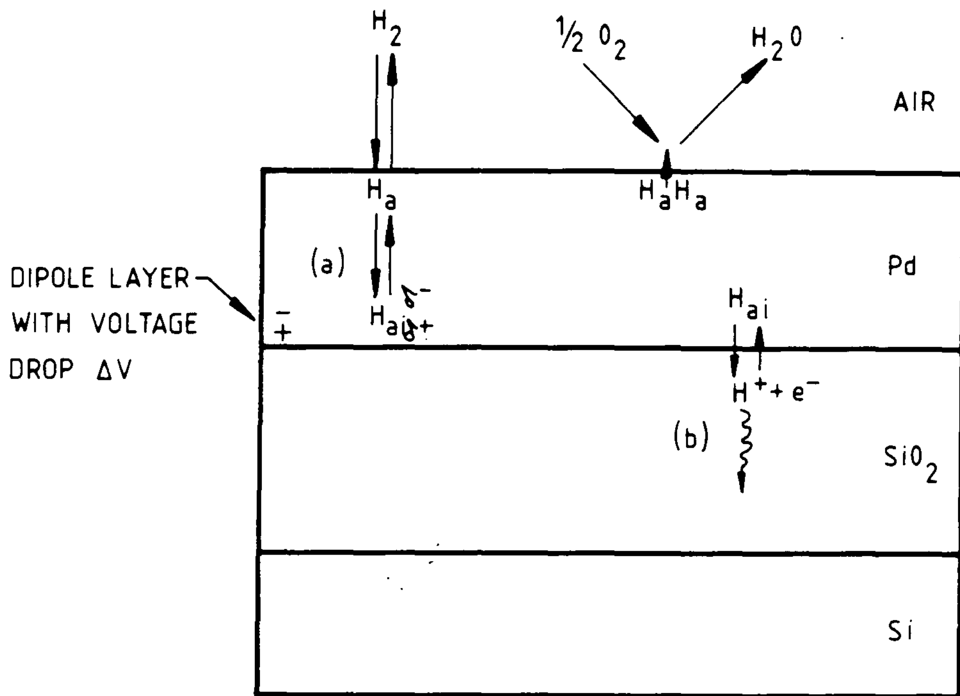


Figure 6.4 : Representation of possible mechanisms of hydrogen interaction with Pd - SiO_2 interface

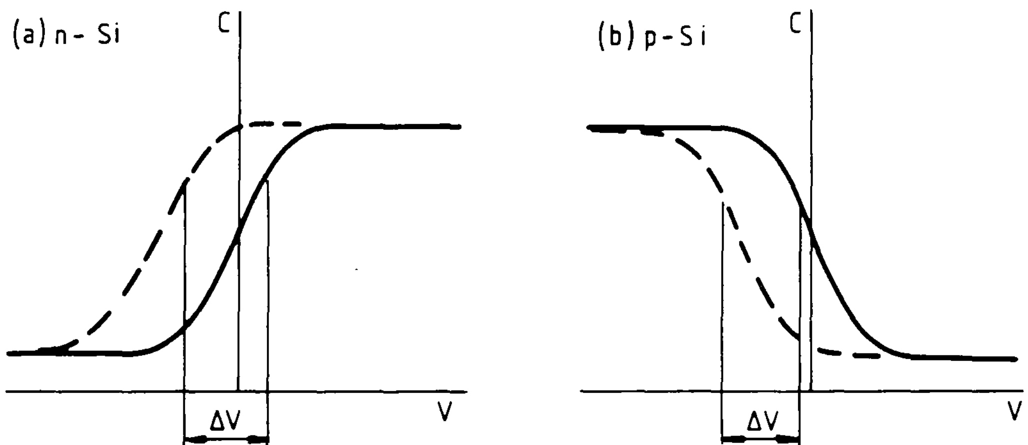


Figure 6.5 : Effects of hydrogen-induced dipole layer on C-V response of Pd-MOS capacitor

will correspond to a shift of the C-V curve towards inversion (figure 6.5a); a p-type device will be pushed into depletion, as holes will be repelled by the dipole, and the voltage shift will be in a similar direction (figure 6.5b).

Other researchers have shown that the situation may be more complicated [12, 13], the flat-band voltage shift arising from both a metal work function change and an effect due to hydrogen trapping in the oxide itself. This action has been attributed to the absorption of H^+ ions (protons) in the first few atomic layers of the oxide (figure 6.4,(b)); the protons diffuse through the structure until they bind to a SiO^-Na^+ defect, resulting in a negative shift of the C-V response and flat-band voltage. The instabilities introduced by this hydrogen-induced drift may be largely overcome by introducing an intermediate insulating layer (e.g. alumina) between oxide and metal before top contact deposition [13].

Very recent work [14, 15] suggests that the MIS structure may behave as a solid electrochmeical cell; however, this theory has yet to be fully reported and is not widely acknowledged at present.

6.1.2 Changes in surface state distribution

The theory outlined above assumes that the V_{FB} shift is due solely to the dissociation of adsorbed H_2 and associated effects, and does not consider any possibility of hydrogen atoms migrating through the oxide and influencing the SiO_2/Si interface states. However, on the basis of experiments with Schottky diode devices, some workers favour an alternative explanation [16-20]: it is believed that hydrogen alters the population of carrier trapping centres at the silicon/silicon dioxide interface. Two possible effects which would result in the observed lateral shift in the C-V response are the introduction of donor states or the removal of acceptor states. Keramati and Zemel [17, 18] have made measurements on thin tunnelling oxide devices and have proposed a model which suggests that two donor levels are introduced by hydrogen action (at 0.4 eV and 0.6 eV below the conduction band edge). Although other workers have produced evidence to support

this surface state model [16, 19], it has been noted [20] that it does not account for the surface state density reduction which results from low temperature annealing in H_2 gas. Furthermore, it cannot explain the fact that a lateral voltage shift is observed for thick oxide devices in which hydrogen is highly unlikely to penetrate to the oxide-semiconductor interface at all.

By making use of the automated admittance measurement system described in chapters 4 and 5 to perform surface state analysis of Pd-gate MIS devices, the mechanisms of hydrogen interaction may be more clearly understood.

6.2 Experimental Details

Two Pd/SiO_2/Si structures were prepared using n-type silicon wafers with oxides grown in dry O_2 at 1100°C to thicknesses of 105 (±2.5)nm and 12 (±1)nm, as measured by ellipsometry (samples N1 and N2). Back contacts of 20 nm Au/Sb alloy were deposited by evaporation and heat-treated in dry N_2 for 2 minutes at a temperature of 400°C to ensure that they were ohmic. Top electrodes of 20 nm Pd were evaporated onto each sample through a mask of 1.25 (±0.025) mm diameter holes. Full details of device history and treatment appear in Appendix B1. After preparation, the slices were kept within a desiccator in a dry N_2 atmosphere to avoid any moisture absorption.

Preliminary experiments were carried out to determine the time required to saturate the devices when exposed to hydrogen at room temperature. This was accomplished by measuring the capacitance-voltage characteristics of the samples in air and monitoring the change after evacuating the chamber and subsequently introducing 0.8% H_2 in N_2 at atmospheric pressure. The lateral shift in the C-V response was observed, and when no further change was recorded the device was deemed to have reached saturation; this was after approximately 30 minutes for both samples. In all subsequent evaluations of surface state density in hydrogen, a 0.8% H_2:N_2 concentration was used, and the above procedure was followed to ensure that the sample was completely saturated. After exposure

to the gas mixture the chamber was flushed with dry nitrogen and opened to air; the recovery time (typically 2 to 3 hours) was recorded by observing the C-V shift as before. All experiments reported in this work were conducted at room temperature.

The N_{ss} - ψ_s profile of each device was calculated intially in air and again when saturated with the hydrogen gas mixture. Finally the experiment was repeated in air after allowing the sample to recover from exposure. Each determination of N_{ss} was preceded with a high frequency (100 kHz) and low frequency (10 Hz) plot of capacitance and conductance against applied bias in order to determine the range of bias voltages over which a peak conductance value would be observed and to calculate the device doping density. A forward and reverse C-V scan was also performed to measure the degree of hysteresis (and hence the amount of mobile charge) present in the sample.

6.3 Results and Discussion

6.3.1 Device Characterisation

Thick oxide sample

The high and low frequency C-V and G-V characteristics recorded in air for the 105 nm oxide device (sample N1) are reproduced in figures 6.6 and 6.7 respectively. The "ledge" apparent in the low frequency C-V curve (6.7a) has been identified as being due to the charging of surface states at a particular value of surface potential [21] dependent on surface state density and voltage scan rate.

The determination of doping density N_d has been discussed in chapter 5.2. From the ratio of C_{min} to C_{max}, N_d was found [22] to be 2.4×10^{15} cm^{-3}, and from a plot of $1/C_D{}^2$ versus V a value of 2.8×10^{15} cm^{-3} was obtained (section 5.2.2); the average of these two figures was used for further calculations, i.e. $N_d = 2.6 \times 10^{15}$ cm^{-3} (= 2.6×10^{21} m^{-3}).

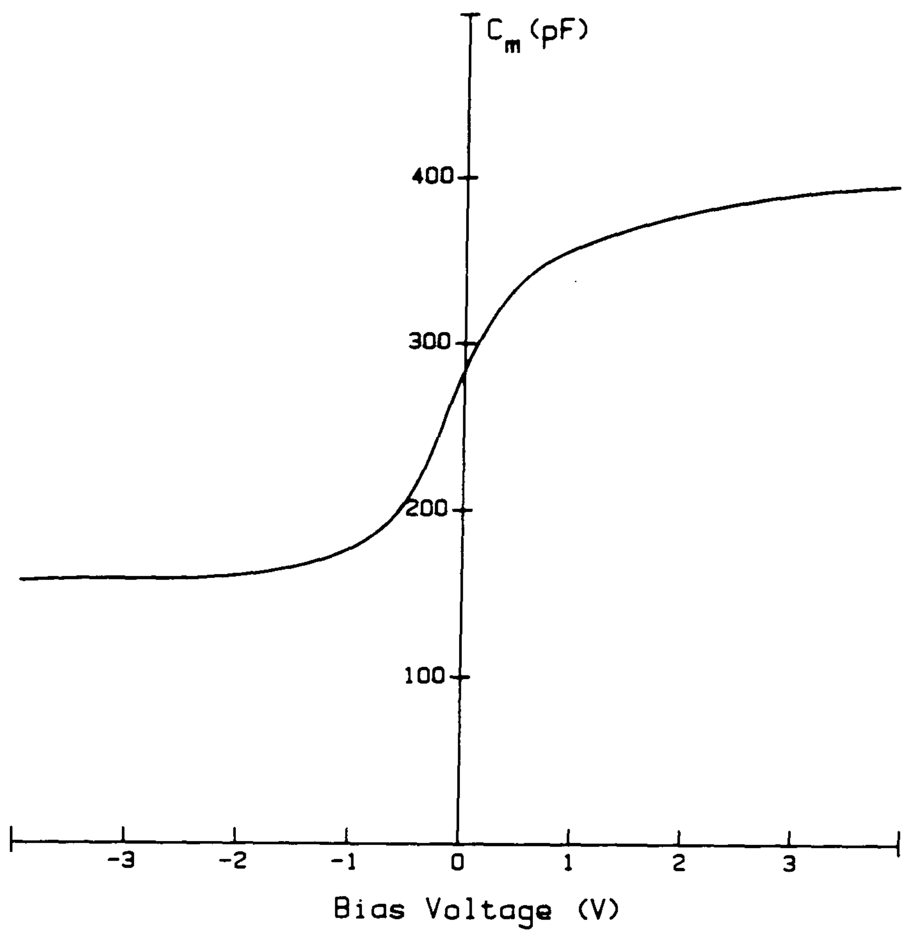


Figure 6.6a : C-V curve at 100 kHz for 105nm oxide device (in air)

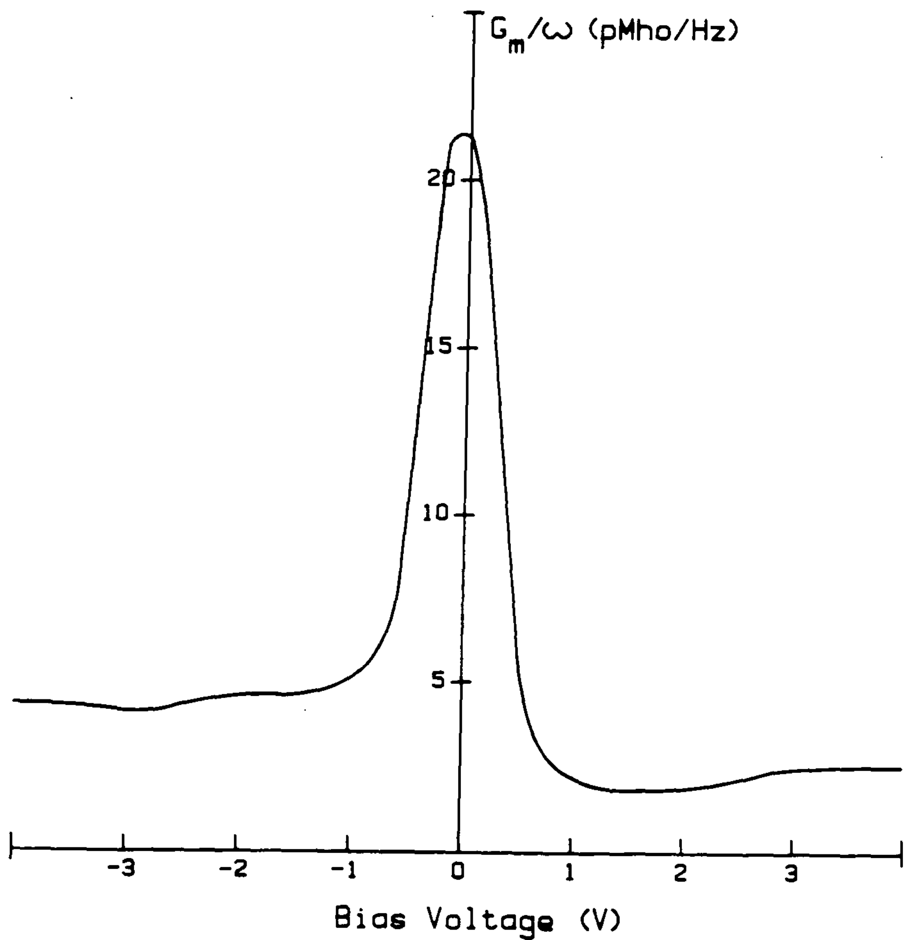


Figure 6.6b : G-V curve at 100 kHz for 105 nm oxide device (in air)

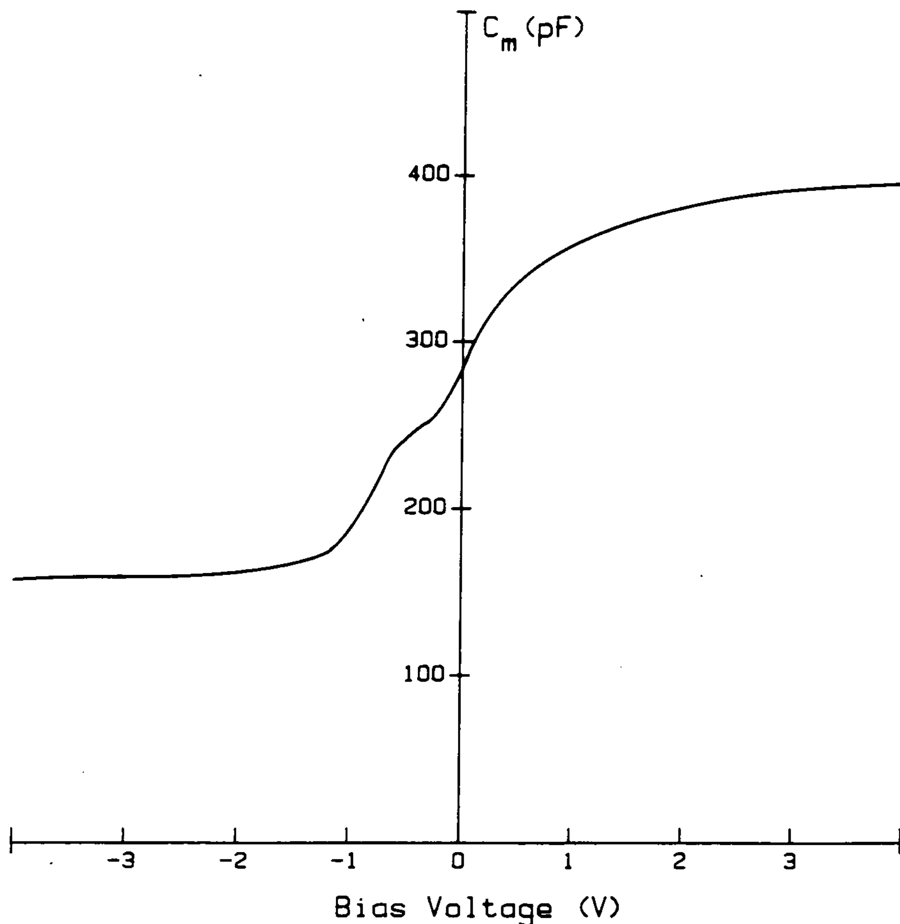


Figure 6.7a : C-V curve at 10 Hz for 105 nm oxide device (in air)

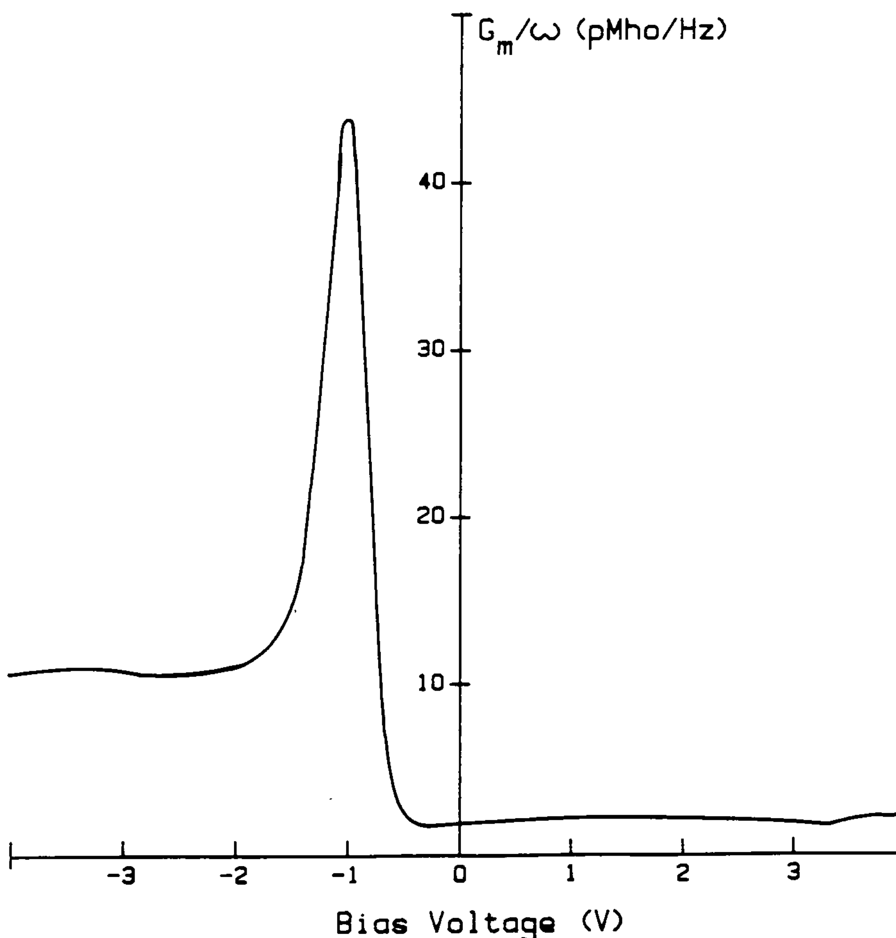


Figure 6.7b : G-V curve at 10 Hz for 105 nm oxide device (in air)

By observation of the position of the conductance peaks of the two plots, the range of bias voltage for which a conductance peak could be obtained was determined as -0.99V (at 10 Hz) to -0.04V (at 100 kHz). In other words, in order to be able to record a conductance peak in the frequency scan experiments used for N_{ss} determinations, a fixed bias voltage within the above range must be applied.

To measure the amount of mobile charge in the sample, the device was biased at -4V (inversion) for 5 minutes and the C-V response recorded at a slow sweep rate (10mV/second); after 5 minutes at +4V bias (accumulation) the scan was repeated in the opposite direction. From the resulting curves, shown in figure 6.8, it can be seen that there is a negligble amount of hysteresis and therefore a very low mobile charge density (as would be expected for a carefully prepared sample).

Thin oxide device

Similar experiments were performed on the 12 nm oxide device (sample N2). Figures 6.9 and 6.10 denote the high and low frequency C-V curves. The large value of conductance in accumulation is a result of carrier transport through the oxide under the high electric field [4 volts applied across 12 nm = 3.3 MV/cm].

The $C_{min} : C_{max}$ ratio was observed to be approximately 0.030, returning (22) a value of $N_d \sim 4.0 \times 10^{14}$ cm^{-3}, and from the $1/C^2$ versus V plots (figure 6.11) the calculated value was 3.9×10^{14} cm^{-3}; $N_d = 4 \times 10^{14}$ cm^{-3} (4×10^{20} m^{-3}) was taken for the figure to be used in later calculations.

The range of operating bias for conductance peak determination was found to be approximately 0V to +0.30V from the low frequency and high frequency peak conductance positions.

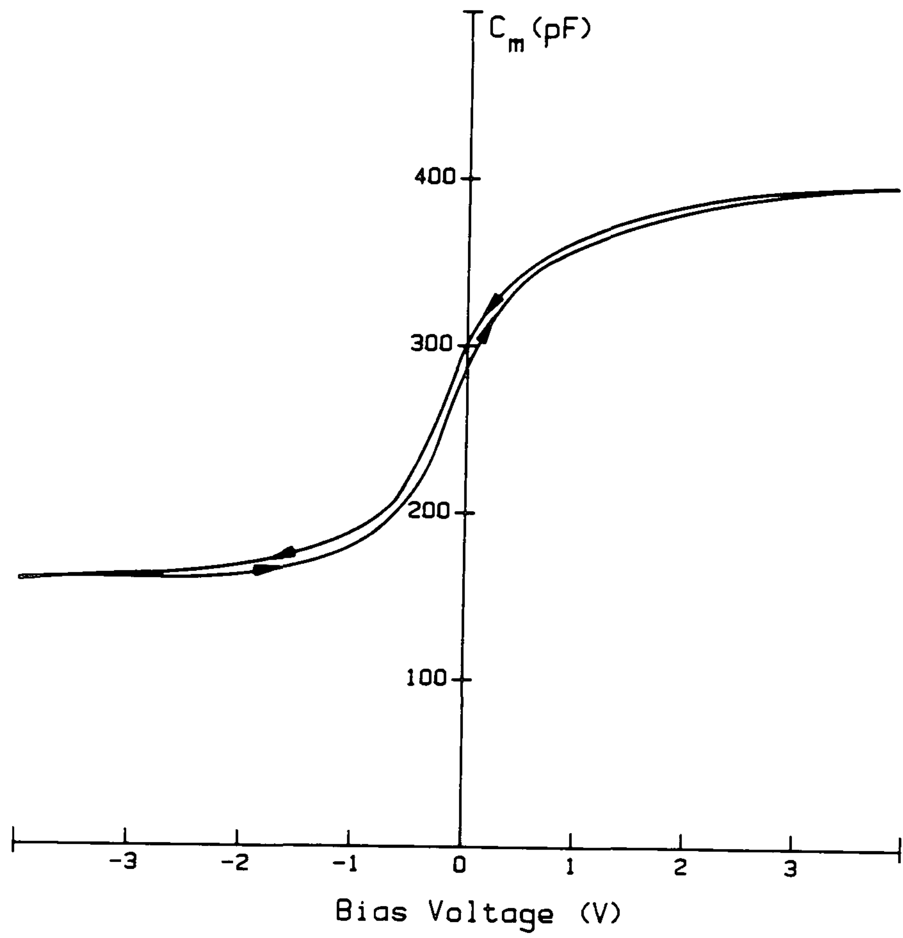


Figure 6.8 : Hysteresis C-V plot for 105 nm oxide device at 100 kHz (in air)

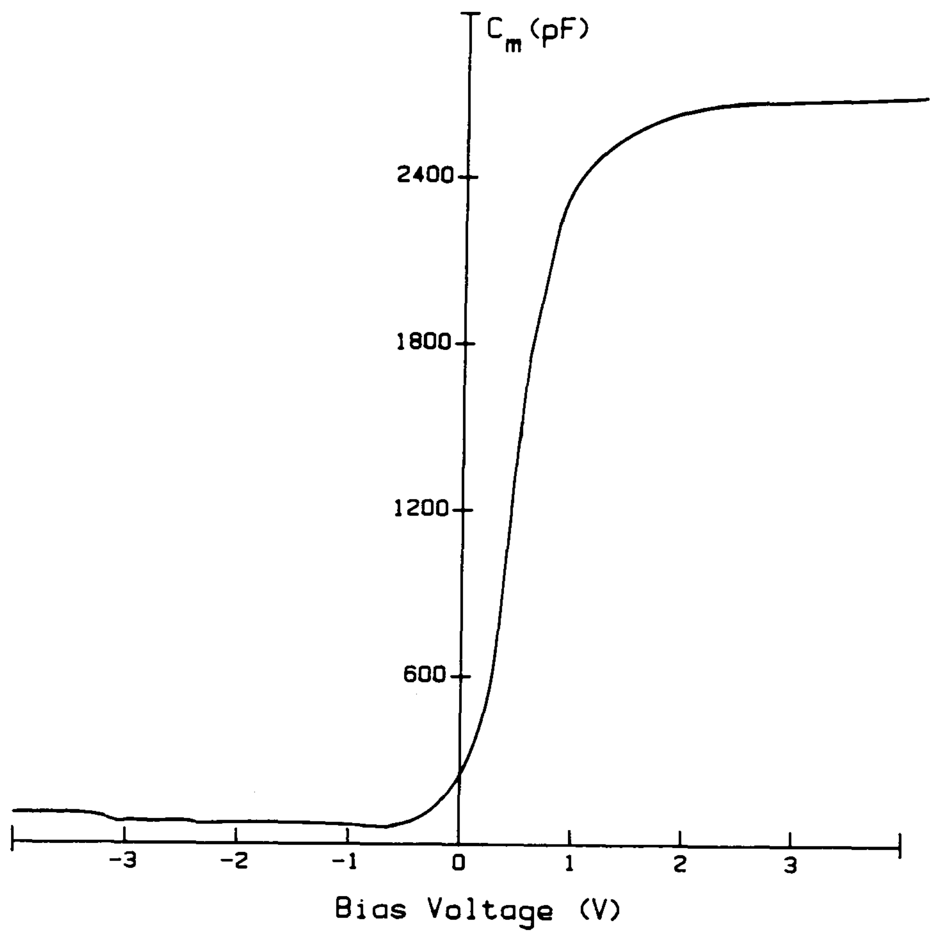


Figure 6.9a : C-V curve at 100 kHz for 12 nm oxide device (in air)

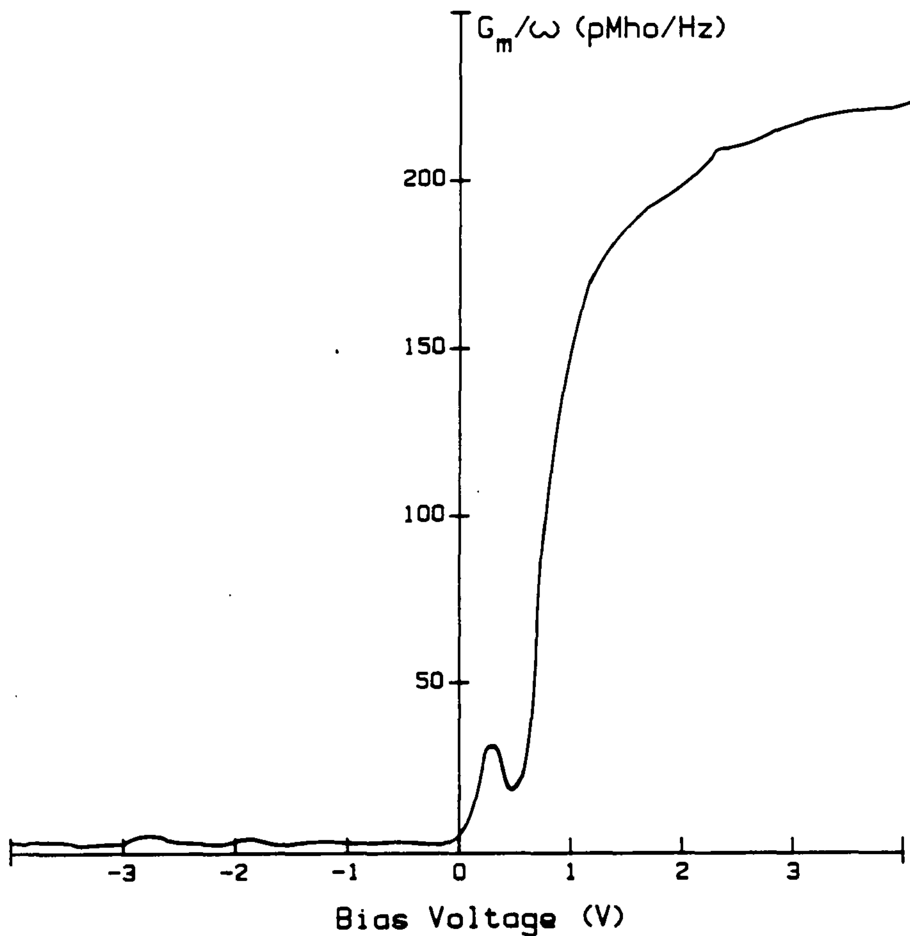


Figure 6.9b : G-V curve at 100 kHz for 12 nm oxide device (in air)

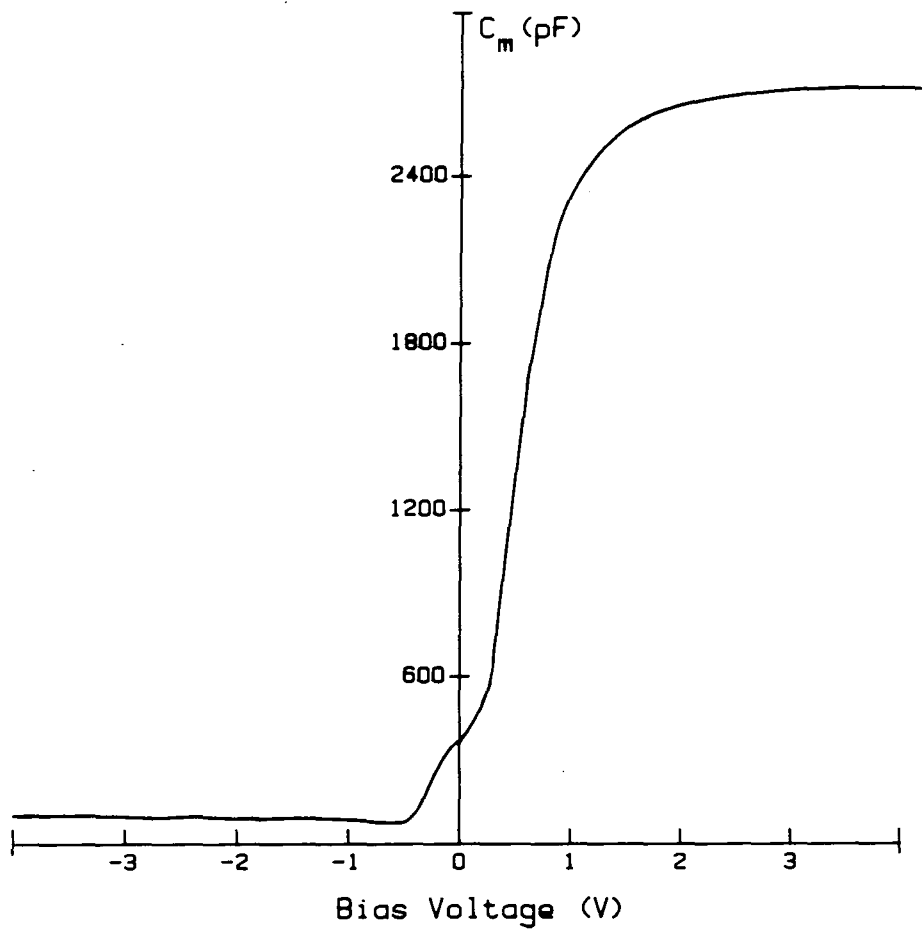


Figure 6.10a : C-V curve at 10 Hz for 12 nm oxide device (in air)

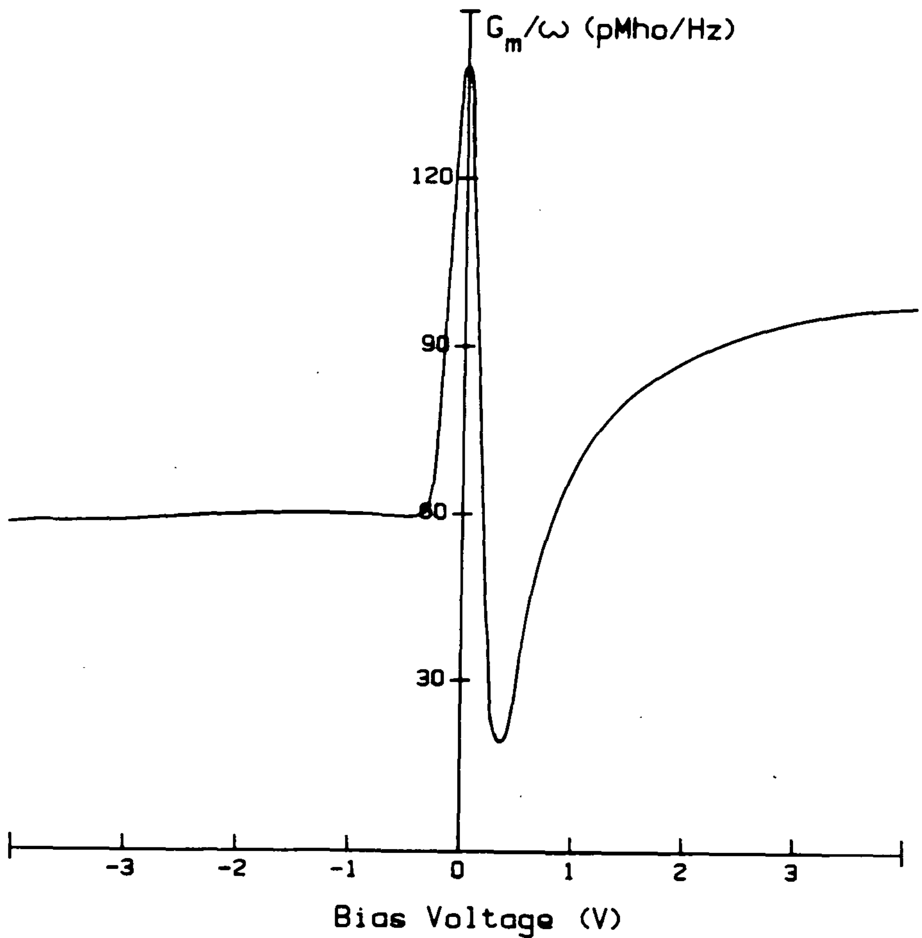


Figure 6.10b : G-V curve at 10 Hz for 12 nm oxide device (in air)

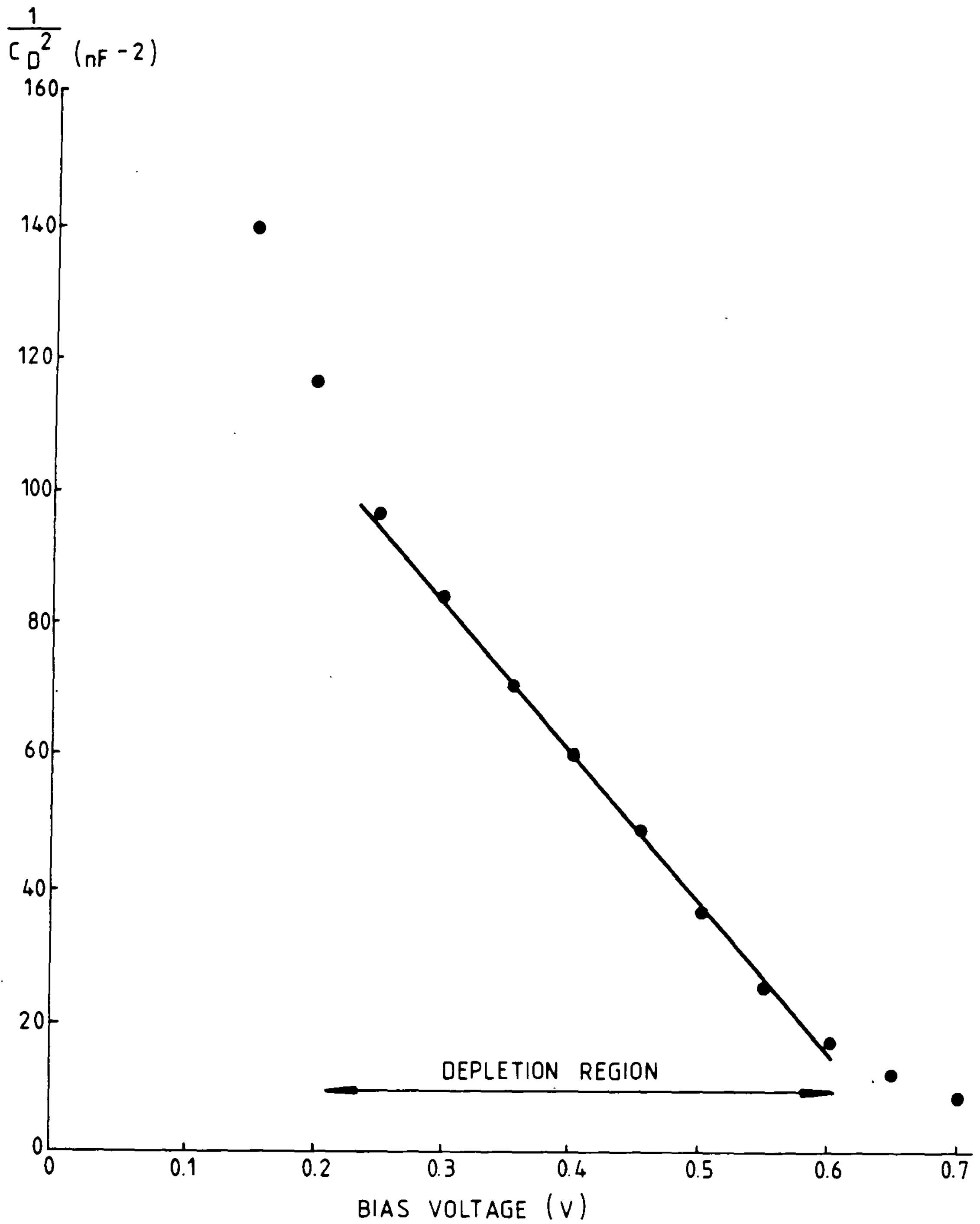


Figure 6.11 : $1/C_D^2$ versus bias voltage relationship for 12 nm oxide device at 100 kHz

Figure 6.12 shows the C-V plots determined under the same conditions as for figure 6.8; again, the hysteresis is very small, denoting a low concentration of mobile charge in the structure.

6.3.2 Influence of hydrogen on MOS devices

In the H_2/N_2 mixture the lateral voltage shift of the C-V and G-V responses was 0.90V (towards inversion) from the curves measured in air; this was true for both thick (105 nm) and thin (12 nm) oxide samples. For later measurements in air, the curves returned to their original positions.

Low frequency data for these devices are shown in figures 6.13 and 6.14. For the thick oxide device (figure 6.13), both capacitance and conductance responses are identical but laterally displaced along the voltage axis. However, for the thin oxide device (figure 6.14), the capacitance curve shape is identical but the height of the conductance peak is markedly reduced when in the hydrogen atmosphere. In air, $G_{peak} \sim 140$ pMho/Hz; in 0.8% H_2/N_2, $G_{peak} \sim 123$ pMho/Hz, a reduction of some 12%. It has already been established (chapter 2.2.3) that the value of the conductance peak is proportional to the surface state density, and so this change in peak height reflects a possible reduction in N_{ss} due to the presence of hydrogen. In order to quantify this change in interface state distribution, N_{ss} versus ψ_s plots were determined for both thick and thin oxide devices.

Figure 6.15 shows the measured surface state density values for the 105 nm oxide MOS device; the different data points reflect the initial evaluation in air and the N_{ss} distribution in the 0.8% $H_2:N_2$ atmosphere. From these results it can be seen that despite the distinct shift in the C-V and G-V curves shown in figure 6.13, the surface state density distribution for the thick oxide MOS structure is completely unaffected by the presence of hydrogen gas. This is in agreement with the findings of Poteat, Lalevic et al.[23, 3]. These workers have evaluated interface state densities for both Pd-gate and Pt-gate MOS structures (of oxide

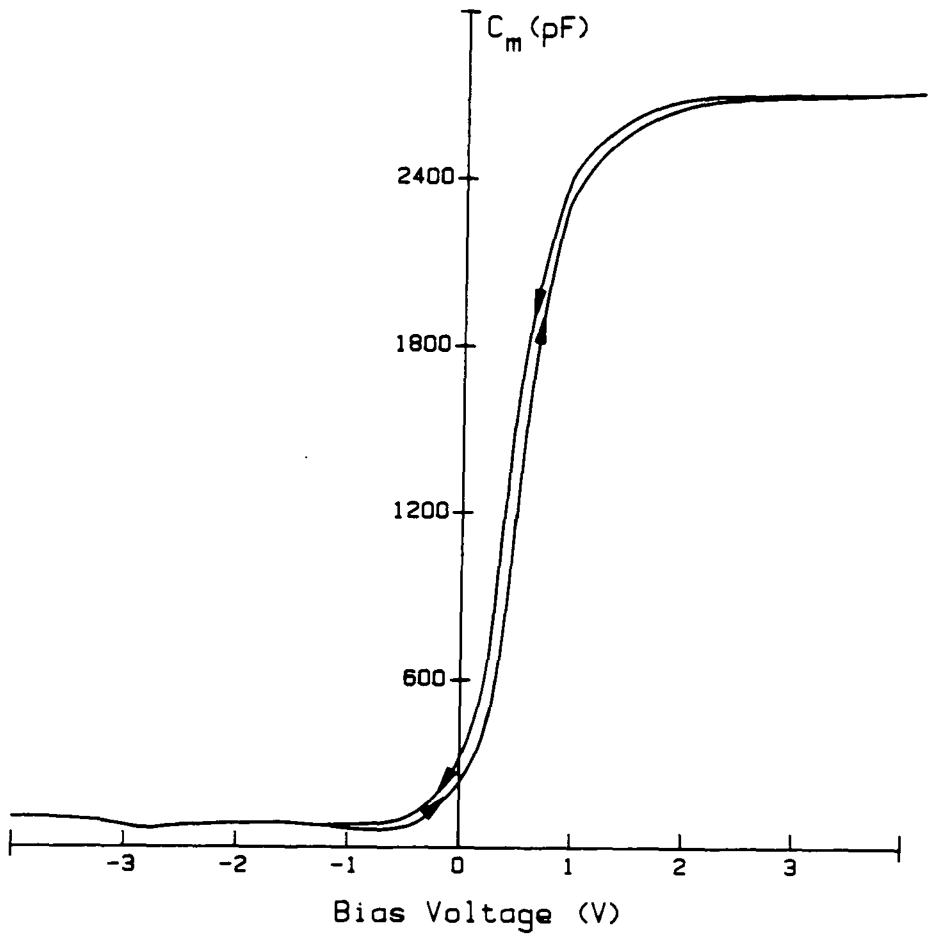


Figure 6.12 : Hysteresis C-V plot for 12 nm oxide device at 10 Hz (in air)

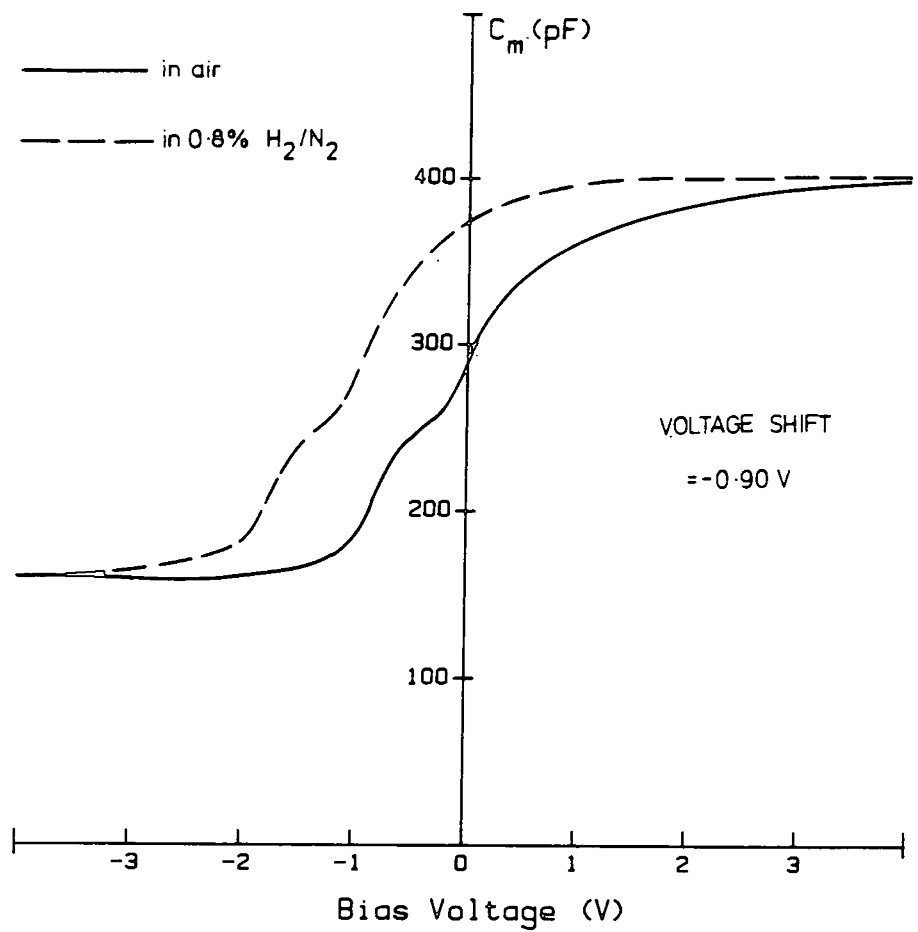


Figure 6.13a : Hydrogen effects on C-V curve for 105 nm oxide device (10 Hz)

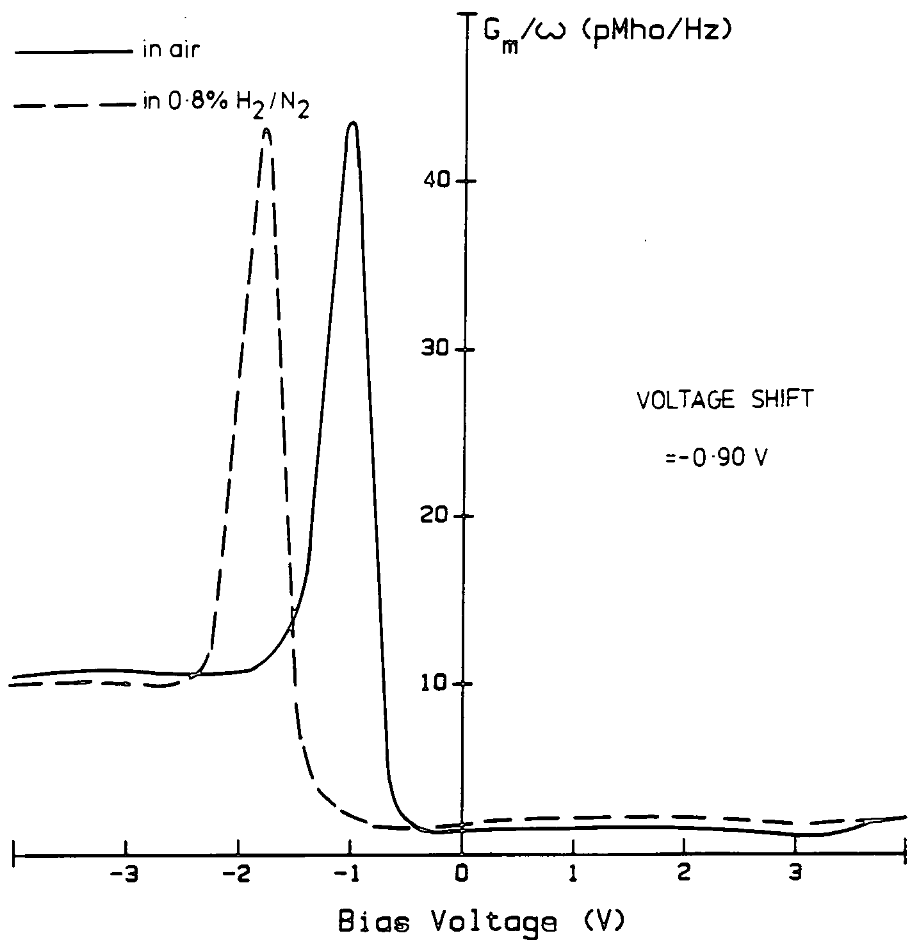


Figure 6.13b : Hydrogen effects on G-V curve for 105 nm oxide device (10 Hz)

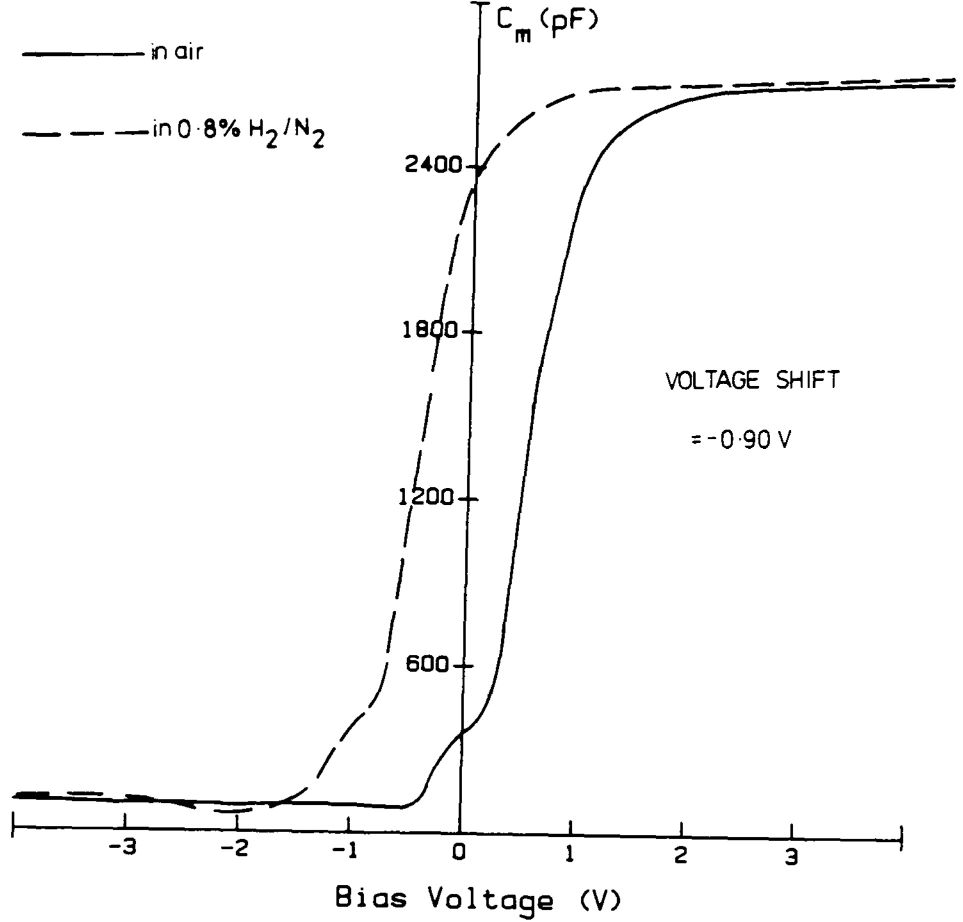


Figure 6.14a : Hydrogen effects on C-V curve for 12 nm oxide device (10 Hz)

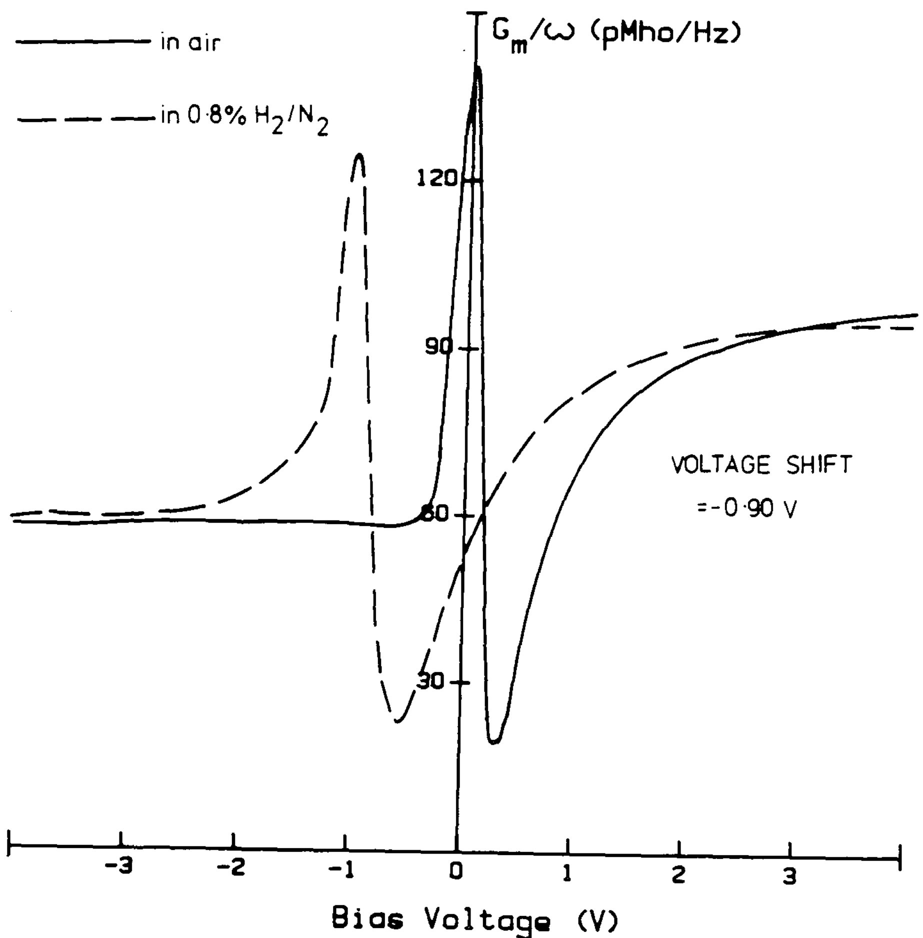


Figure 6.14b : Hydrogen effects on G-V curve for 12 nm oxide device (10 Hz)

thicknesses 50 nm and 100 nm) by integrating the low-frequency (10Hz) capacitance-voltage curve [24]. After H_2 exposure, no significant changes were found in either the density of surface states across the Si bandgap or in the number of states at mid-gap. Thus it may be concluded that the dominant H_2 effect in our thick oxide device is a simple work function change of the Pd metal.

The results obtained from experiments with the thin (12 nm) oxide MOS devices are shown in figure 6.16. In this case a change is observed in the surface state density spectrum after H_2 exposure; at room temperature this effect appears to be completely reversible. The presence of the H_2 gas reduces the number of interface traps in the mid-gap region. This phenomenon, which explains the decrease in the height of the conductance peak apparent in the G-V response (figure 6.14), is well-known to silicon technologists and is often exploited to control the density of traps at the SiO_2/Si interface in post-oxidation annealing processes [15, 26]; however, elevated temperatures are invariably used, and the effect is not reversible as indicated by the above results.

6.3.3 Effects of annealing

The "hump" shape of the surface state distribution shown in figures 6.15 and 6.16 is frequently observed for oxides grown in dry oxygen before annealing [25, 27]. To gain further insight into the hydrogen effect experiments were performed using MOS samples that had been deliberately annealed in order to change the surface state density spectrum. This process was performed on portions of the thick and thin oxide samples; these were heated to 400°C in a 35% H_2/N_2 atmosphere for 5 minutes. For both devices thus treated the number of interface states in the mid-gap region was reduced and the familiar U-shaped distribution [25] across the bandgap was observed. It should be noted that the presence of H_2 was essential for this annealing process; simply heating the devices in dry N_2 at 400°C (as was done in order to produce ohmic back contacts) did not appreciably change the surface state density distribution. Figures 6.17 and 6.18 show the results

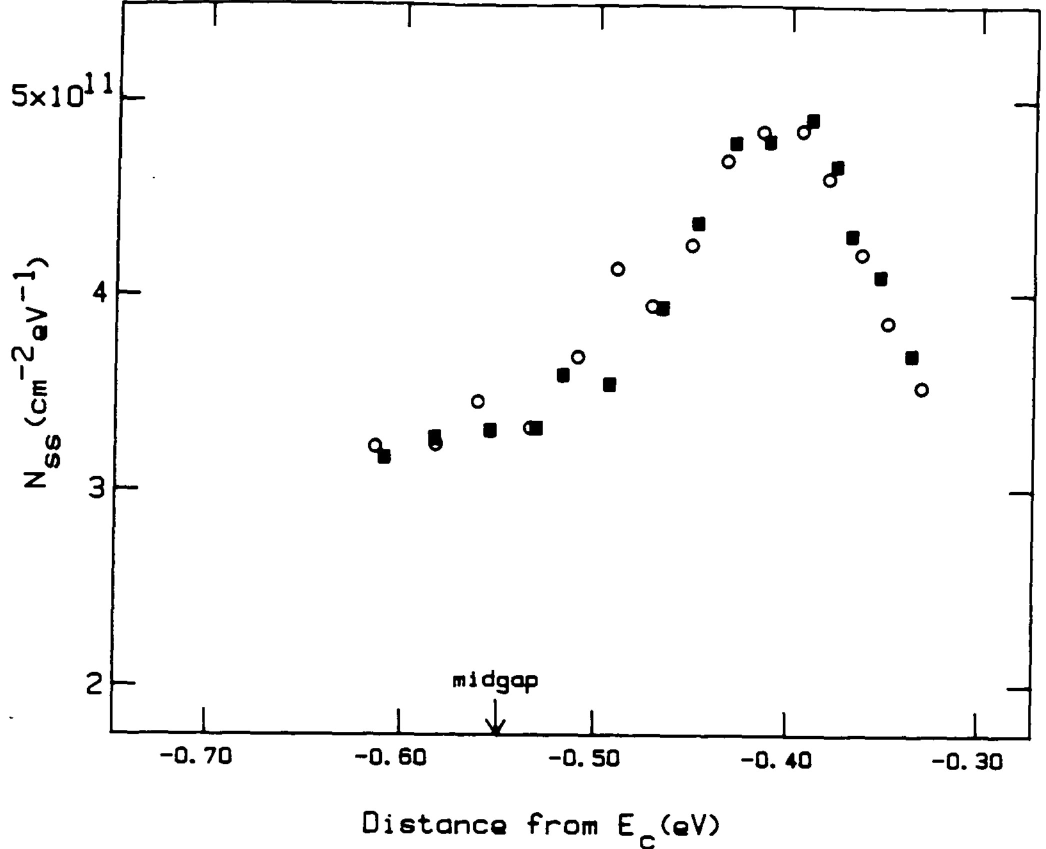


Figure 6.15 : N_{ss} versus bandgap position for 105 nm oxide MOS device (unannealed)

○ in air before exposure to hydrogen

■ in 0.8% hydrogen/nitrogen atmosphere

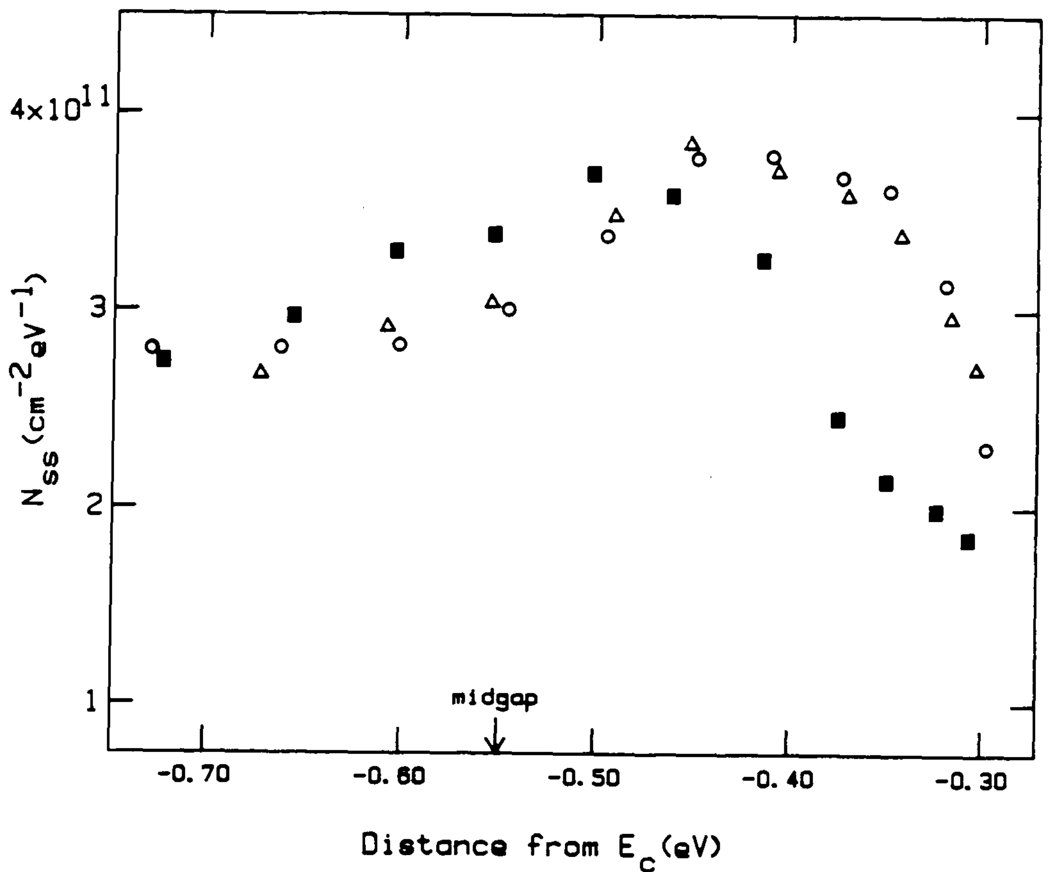


Figure 6.16 : N_{ss} versus bandgap position for 12 nm oxide MOS device (unannealed)

○ in air before exposure to hydrogen

■ in 0.8% hydrogen/nitrogen atmosphere

△ in air after exposure to hydrogen

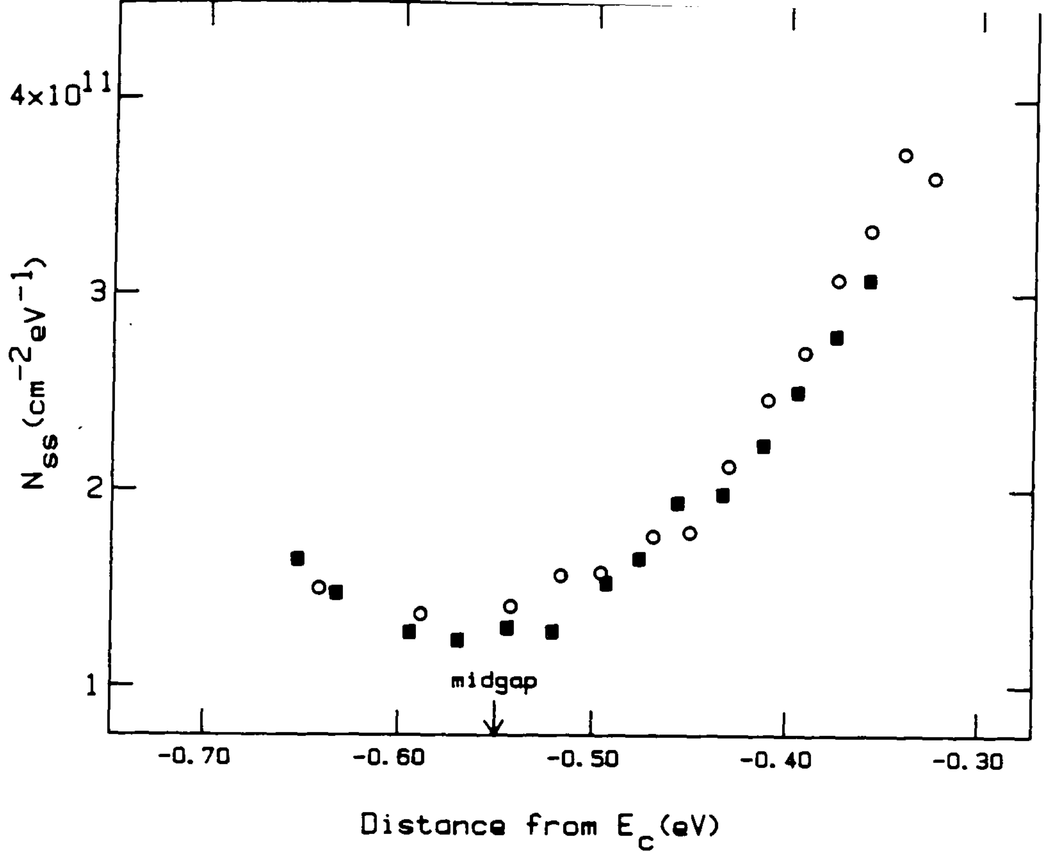


Figure 6.17 : N_{ss} versus bandgap position for 105 nm oxide MOS device (after annealing)

○ in air before exposure to hydrogen

■ in 0.8% hydrogen/nitrogen atmosphere

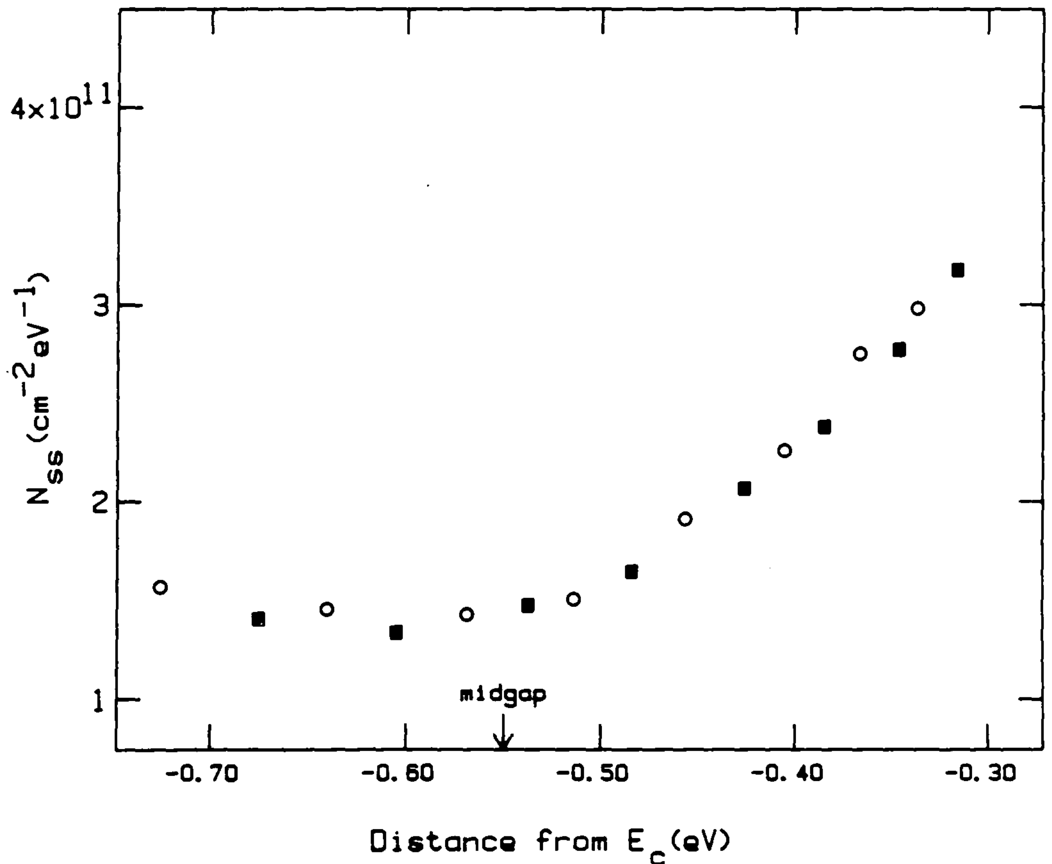


Figure 6.18 : N_{ss} versus bandgap position for 12 nm oxide MOS device (after annealing)

○ in air before exposure to hydrogen

■ in 0.8% hydrogen/nitrogen atmsphere

of subsequently exposing the annealed MOS structures to an atmosphere of 0.8% H_2 in N_2; no change in the surface state spectrum was observed for any of the devices. In addition, the low frequency C-V and G-V curves (figure 6.19) exhibit a smaller lateral voltage shift when exposed to hydrogen than before (0.77V as opposed to 0.90V) and the peak value of the conductance curve is much smaller (88 pMho/Hz); furthermore, there is no change in peak height when hydrogen is introduced. These results imply that in reducing the value of N_{ss}, the surface states responsible for the hydrogen effect revealed in figure 6.16 have been removed by the annealing procedure.

6.3.4 Discussion of hydrogen results

Low temperature (300 - 500°C) annealing in a hydrogen atmosphere is generally thought to result in the elimination of unpaired surface Si electrons (dangling bonds) and the formation of Si-H bonds [25, 27]. Atomic hydrogen is usually more effective than molecular hydrogen in annihilating such traps; in standard MOS processing, this is thought to be produced by the interaction of water with the aluminium gate metal [25].

The following model is suggested to explain the results detailed above. For both thick (∿100 nm) and thin (∿10 nm) Pd-gate MOS devices the primary effect upon exposure to hydrogen is a change in the work function of the palladium metal. However, the dry-oxidation of the silicon results in a relatively high surface state density distribution across the silicon bandgap. For thin oxide structures some of these surface states can be removed by hydrogen atoms (formed by dissociation in the Pd metal) penetrating to the Si/SiO_2 interface region; thick oxides will not allow this. It appears that at room temperature this reaction is completely reversible. Once the surface states have been removed by annealing in H_2 at an elevated temperature, the room temperature H_2 effect is no longer observed. The precise nature of the hydrogen interaction with the interface states cannot be precisely defined; however, one possibility is the silicon surface dangling bond which has been shown to produce

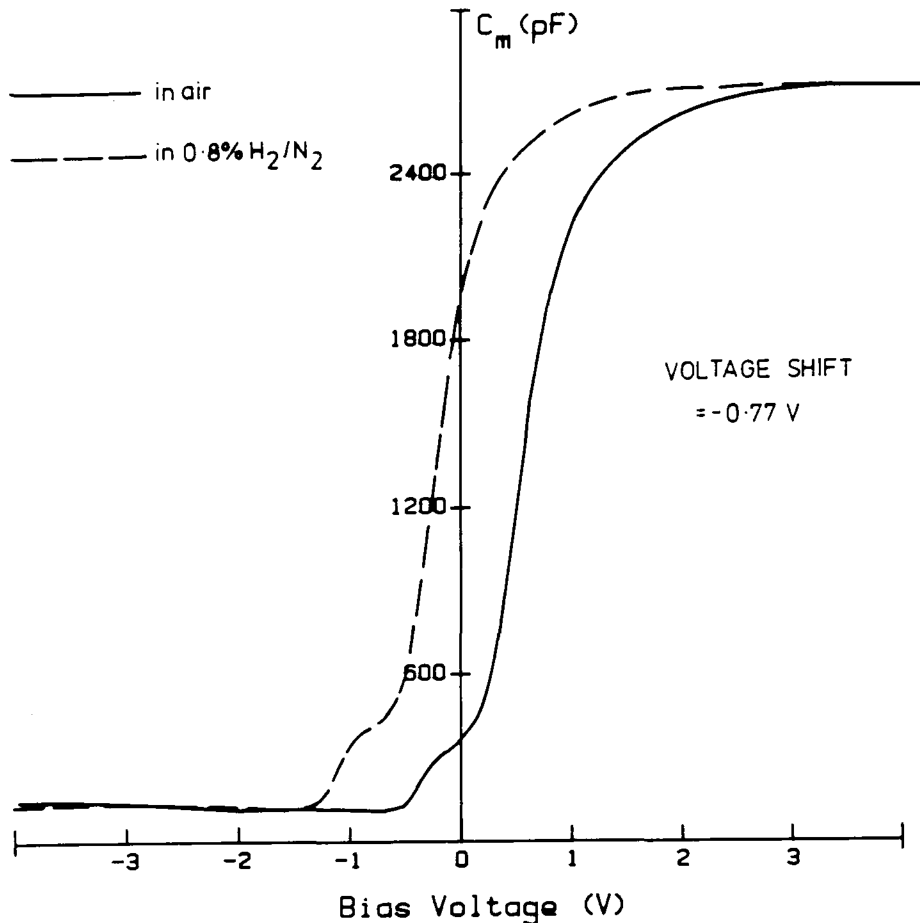


Figure 6.19a : Hydrogen effects on C-V curve for 12 nm oxide device after annealing (10 Hz)

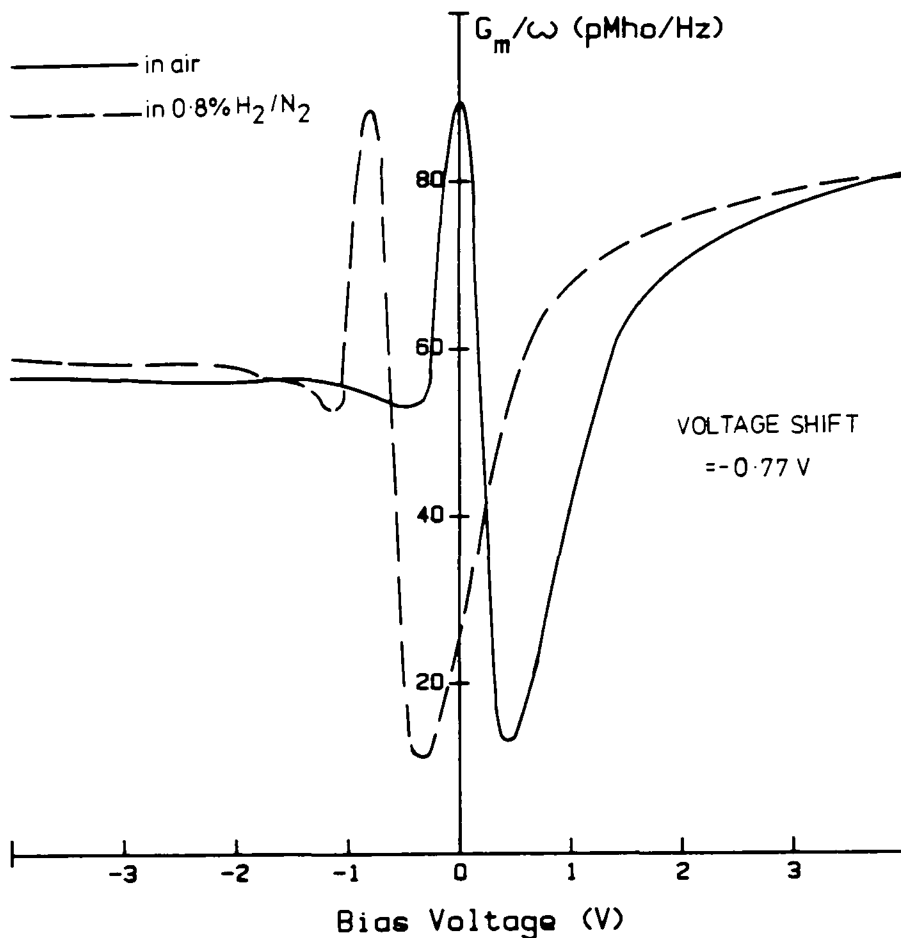


Figure 6.19b : Hydrogen effects on G-V curve for 12 nm oxide device after annealing (10 Hz)

trapping levels near mid-gap [25, 28, 29].

This model is in agreement with results obtained by other workers investigating both Pd-SiO_2-Si [17, 18] and electrolyte-SiO_2-Si systems [30]. It has also been pointed out [20] that surface state responses to hydrogen have only been observed by those researchers using thin oxide or Schottky barrier devices whose ideality factor is greater than unity; no effects on interface states have been recorded for thick oxide samples or devices with almost ideal diode characteristics, although the lateral voltage shift is observed.

From the results presented here it appears that the primary response of the Pd/SiO_2/Si system to hydrogen gas is due to a work function change at the metal-oxide interface. However, in some cases the interface state effects may become important, and it is clear the the method of growth of the silicon oxide layer will be crucial in determining the operation of any Pd-gate MOS device.

6.4 Summary and Suggestions for Further Work

The interface state densities of Pd/SiO_2/n-Si MOS devices have been measured by the a.c. conductance technique using the automated system developed for this purpose. Upon exposure to hydrogen gas, no change is observed for devices with thick (∿100nm) oxides; however, a variation is apparent for MOS structures in which the oxide thickness is approximately 12nm. This has been attributed to surface traps at, or very close to, the Si/SiO_2 interface produced during device fabrication; these traps may be effectively removed by a low temperature annealing process, producing MOS structures which no longer exhibit H_2-induced surface state density changes.

These results prove that the experimental system is capable of carrying out highly quantatitive measurement of surface state distribution at the insulator-semiconductor interface of a MIS device. Since the surface state charge can greatly influence the behaviour of practical microelectronic devices, the ability to monitor this parameter accurately is invaluable for assessment of the quality of devices. Consequently, this may be a useful method by which to monitor commercial wafer fabrication processes with a view to increasing yield and improving device performance.

Further applications of, and possible improvements to, the technique may now be considered. For example, the work presented above has considered only one gas/catalytic metal interaction and only one type of insulator-semiconductor structure; both these systems have exhibited a response to hydrogen gas. However, it is clear that other gases may be detected by these, or similar, combinations of materials [31]. If this is so, then it may be found that each gas affects the various insulator-semiconductor interface states in a slightly different way, and so by measurement of the change in device properties upon exposure, an unknown gas may be identified by its "fingerprint" on the surface state density. Preliminary experiments with other gases (NO_2,CH_4,CO) were carried out towards the end of these studies and changes in N_{ss} profile were observed which were of a different nature than those recorded for H_2 exposure. However, it has not yet been possible to quantify or confirm these results (owing to permanent damage caused to the devices when exposed to NO_2) and therefore these findings will not be published until further investigation has been carried out.

A number of alternatives were examined in an effort to improve the response of the devices. As a result of being operated at room temperature, the devices were taking some twenty minutes to respond fully when exposed to hydrogen; it has been shown that by raising the device temperature to around 150°C, the response time can be reduced to as little as ten seconds [31, 7]. Another

option which was considered was the use of a Field Effect Transistor (FET) device instead of the capacitor structure reported above; this concept has also been adopted by other workers, who have proved that the device can detect very low concentrations of hydrogen [6, 7, 31].

However, the approach which was finally selected has not been investigated by any other researchers (probably because the phenomenon is not widely recognised), i.e. that of deliberately <u>increasing</u> the surface state density in order to intensify the response to hydrogen gas identified above. The method by which this was accomplished, and details of the consequent experiments, are presented in the following chapter.

CHAPTER 7 : LANGMUIR-BLODGETT FILM DEVICES

7.0 Introduction

Until relatively recently, MIS devices have been fabricated almost exclusively from silicon, to take advantage of the almost ideal, insulating properties of its natural oxide. However, these devices may also be exploited for their transducing properties, as the electrical characteristics may be influenced by chemical (or physical) action on the MIS structure. The sensitivity and selectivity of the devices to different phenomena can be changed by careful selection of materials. Silicon dioxide is not an ideal choice as the insulator as it is chemically inert, and consequently there is currently a great deal of interest in the development of different insulator materials which may enhance the operation of these transducer devices. One possible solution is the Langmuir-Blodgett technique of building up a series of monolayers of suitable organic materials; the thin films produced in this way are very highly ordered and exhibit interesting electrical properties[1]. However, although the technique was originally developed some fifty years ago, it is only in the last decade that it has received any significant attention and investigation, and the precise nature of Langmuir-Blodgett (LB) multilayer formation is still not fully understood.

In this work, LB films of a relatively novel organic material, ω-tricosenoic acid, have been deposited on silicon as an alternative insulator to SiO_2. The results obtained with the devices so fabricated have enabled electrical properties of the film material to be characterised and have also given an insight into the influence of the film on the silicon surface states. The effects of hydrogen gas on the structures has also been investigated. These results are reported and discussed in this chapter after a description of the instrumentation and experimental procedure for producing Langmuir-Blodgett films.

7.1 Langmuir-Blodgett Film Preparation

By depositing a small quantity of a suitable organic material in solution onto the surface of purified water, a floating monomolecular layer may be formed. Once the solvent has evaporated, this may be compressed to form a quasi-solid one molecule thick - a Langmuir film (after Irving Langmuir, one of the first workers in the field). The floating monolayer may be transferred to a solid substrate by using a precision-engineered instrument (a Langmuir trough) to raise or lower the substrate through the compressed film; if this procedure is repeated, depositing an additional layer on the substrate at each pass through the quasi-solid surface, a multilayer assembly of the organic material may be built up. This technique was first exploited by Katherine Blodgett, a co-worker of Langmuir; thus the built-up multilayer structure is known as a Langmuir-Blodgett (LB) film. Because of the method of deposition, it is possible to control very precisely the thickness of the assembled film from as little as one monolayer (which may be as little as 1nm or so) to more than 1 μm. The LB films so produced exhibit a high degree of structural order, and are good electrical insulators. In addition, because the process is carried out at room temperature there is little disruption of the substrate surface; this contrasts with energetic deposition processes such as sputtering.

A comprehensive account of the early work on LB films has been published by Gaines [2], and recent reviews on the subject [3, 4] along with proceedings of the First International Conference on Langmuir-Blodgett Films (Durham, 1982) [5] are recommended for a detailed account of the advances in and possible applications of the technology.

7.1.1 LB Film Materials

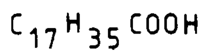
To be able to utilise the LB technique for depositing an organic monolayer onto a substrate, the molecular composition of the material msut be such that the molecules will orientate themselves on the water surface of the Langmuir trough. This is generally

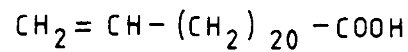
achieved by using substances such as the fatty acids; figure 7.1(a) shows a schematic of stearic acid, whose molecule possesses a long hydrophobic chain of sixteen CH_2 groups terminated by a hydrophilic carboxylic acid group. Other suitable materials may be synthesised by modification of these known molecules. One such material is ω-tricosenoic acid (figure 7.1(b)). This molecule has a longer chain length than stearic acid, and incorporates a terminal double bond which makes it polymerisable under low-energy electron beam radiation [(6)]; consequently it is of some interest as a microlithographic resist [(7, 8)]. Transmission electron diffraction experiments [(9)] have indicated a very high degree of order in ω-tricosenoic acid (ωTA) LB films, and it is an ideal material for deposition by this technique. Not only is it soluble in chloroform and highly stable on the surface of water, but unlike some substances fast deposition speeds may be achieved [(10)]. Highly-ordered, stable films are formed which adhere strongly to the substrate [(7)]; in addition, the material has been shown to be a good insulator [(11)].

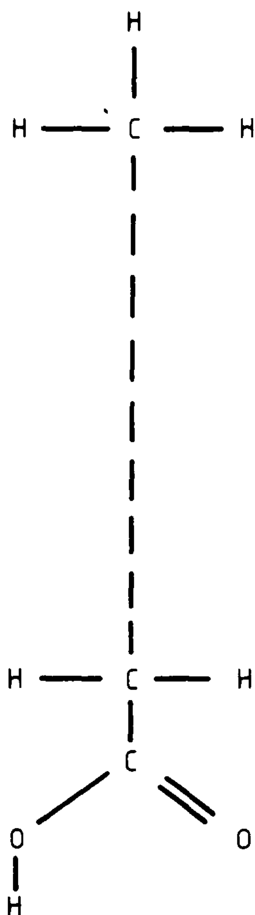
7.1.2 Langmuir trough instrumentation

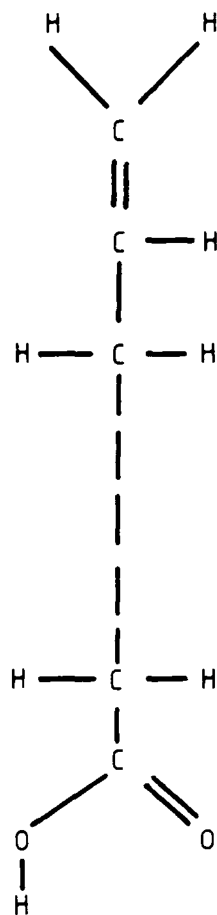
In order to maintain precise control over the composition and thickness of deposited organic monolayers, a highly sophisticated version of the early Langmuir trough is used [(12)]. A schematic representation of the apparatus is shown in figure 7.2a.

The trough consists of a large glass reservoir containing the subphase (highly purified water) onto which the monolayer is spread; the working film area is enclosed within a constant perimeter barrier (figure 7.2b) of PTFE-coated glass-fibre tape which is moved by a low-geared motor. The surface pressure of the subphase is continuously monitored by a Wilhelmy plate attached to a microbalance; this arrangement is used to control the barrier motor in order to maintain a constant film surface pressure whilst molecules are being removed from the subphase. The substrate to be coated is dipped into and out of the subphase, passing through the floating monolayer on each excursion, by means of a motorised micrometer screw arrangement. A photograph of the instrument used









STEARIC ACID

(a)

ω-TRICOSENOIC ACID

(b)

Figure 7.1 : Molecular structure of stearic acid and ω-tricosenoic acid

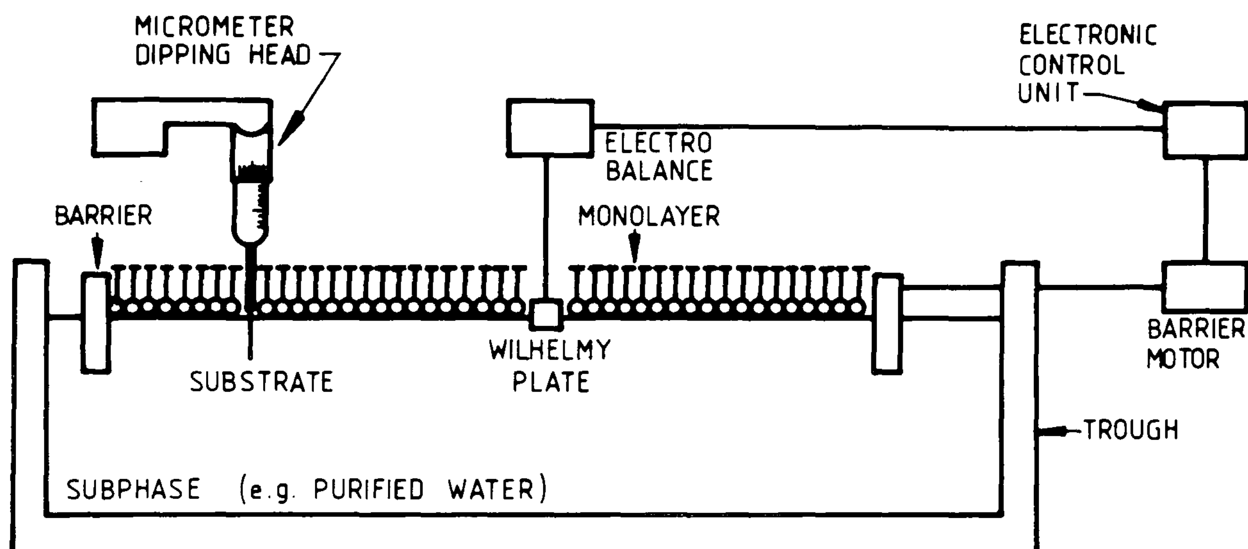


Figure 7.2a : Schematic diagram of Langmuir trough showing compressed monolayer on subphase surface

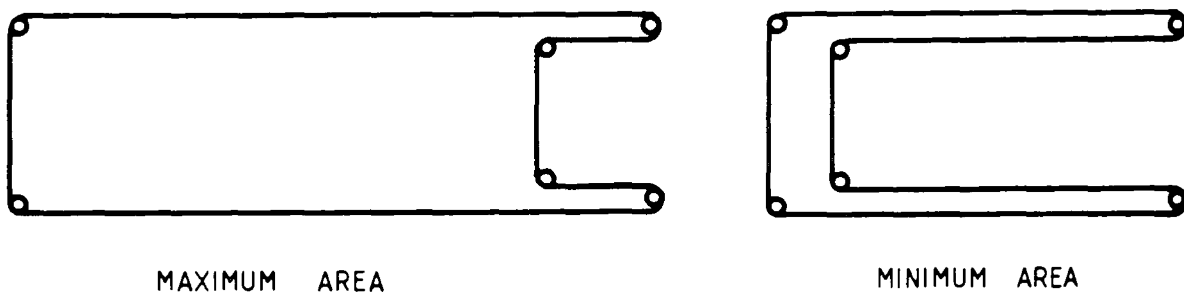


Figure 7.2b : Plan of constant perimeter PTFE barrier geometry

in this work is reproduced as figure 7.3(a); detail of the constant perimeter tape and substrate dipping assembly is shown in figure 7.3(b).

Recent investigation into Langmuir trough instrumentation has concentrated on alternative geometries [4] and upon ways of automating the deposition process [13] (see section 7.1.4). However, all the troughs produced so far have been for low-volume sample preparation for experimental purposes; a far greater understanding of the factors which influence the deposition process is required before any system for commercial deposition of LB films can be considered.

7.1.3 Film deposition procedure

Using the equipment described in the previous section, good quality LB films may be deposited on suitable substrates with a high degree of repeatability and control over film properties. This is achieved by taking great care when preparing materials and samples for dipping: the best commerical grade chemicals are used and the subphase water is filtered and purified (by a reverse osmosis system followed by a deionising unit). The Langmuir trough is normally kept in a dust-free environment (i.e. under microelectronic clean room conditions).

The following procedure is followed to characterise the monolayer spread on the surface of the subphase and to determine the optimum conditons for subsequently transferring this monolayer to a substrate. A known amount of organic material is dissolved in a suitable solvent (e.g. chloroform for ω-tricosenoic acid) and with the barriers opened to give the maximum working area, a measured volume of this solution is carefully placed on the subphase, whose pH and temperature have been previously adjusted as required and recorded. After the solvent has evaporated (some five to twenty minutes, dependent upon the solvent used), the area of the trough is decreased at a constant (known) rate to compress the monolayer and orientate the molecules. By monitoring the surface pressure

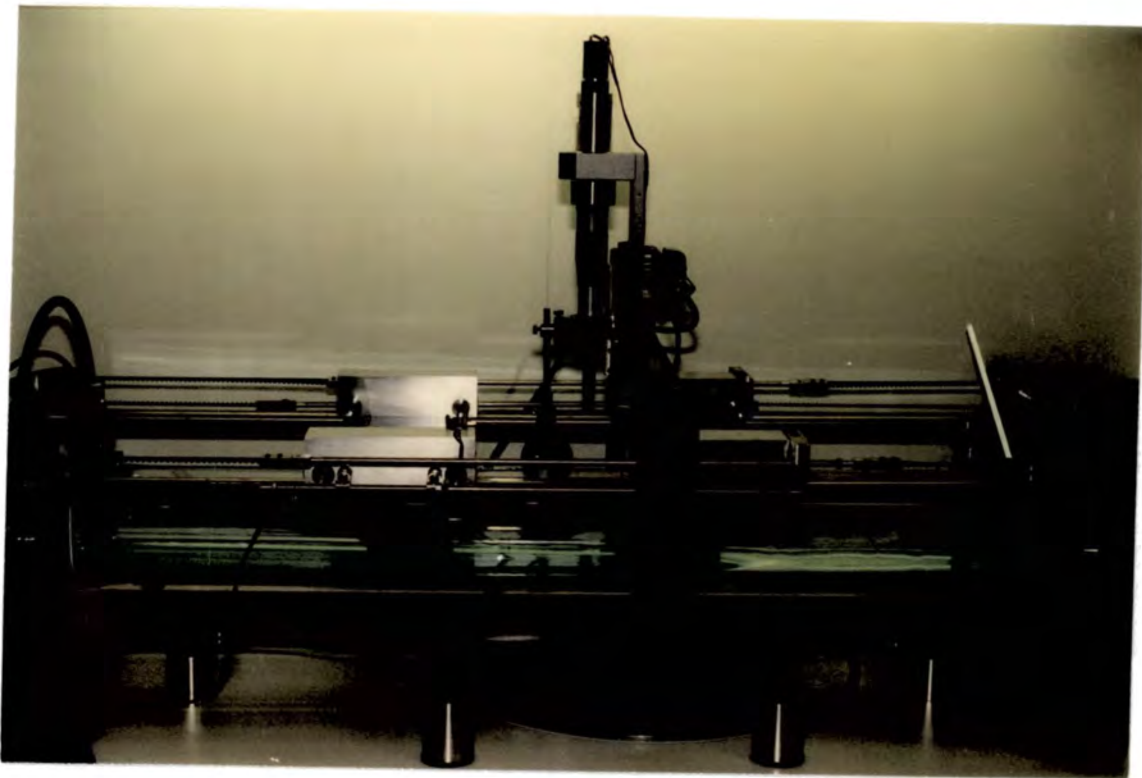


Figure 7.3a : Langmuir trough instrumentation

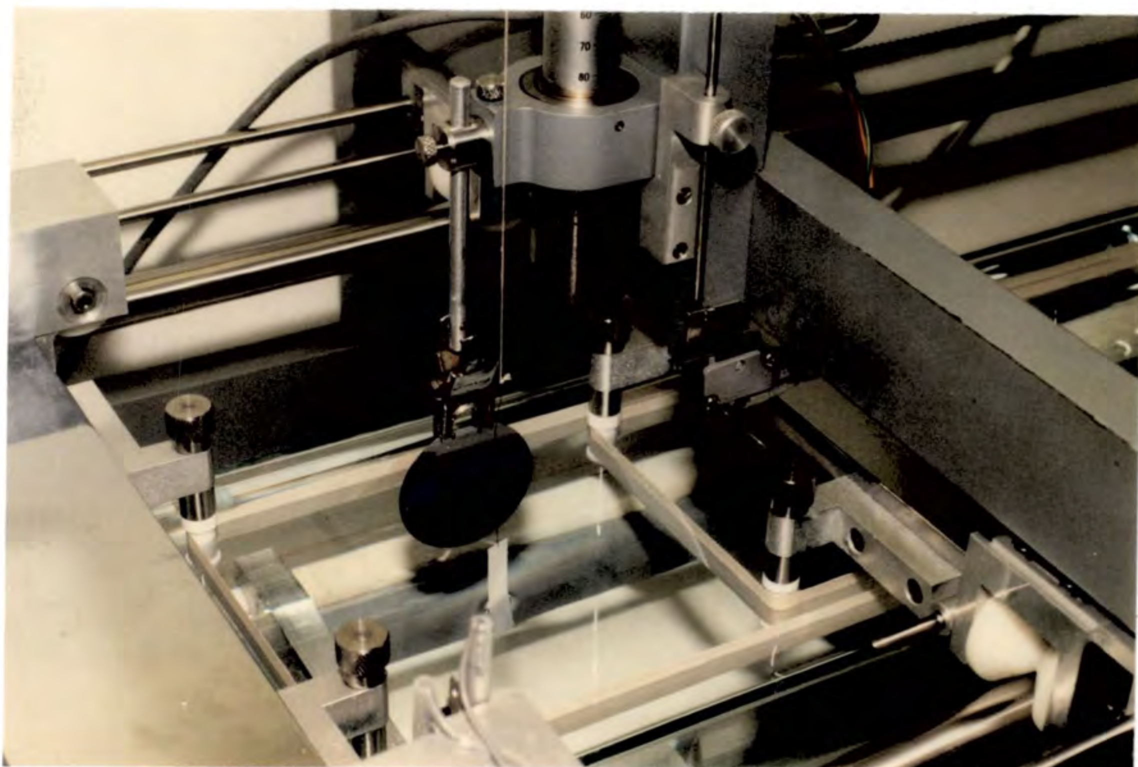


Figure 7.3b : Detail of dipping assembly (with substrate in position) and constant perimeter PTFE tape

and barrier position (and hence surface area) a pressure-area isotherm may be recorded on an X-Y chart recorder. A typical measured isotherm for stearic acid (which is a classic LB film material) is shown in figure 7.4; the horizontal axis may be calibrated in units of barrier area or area per molecule of the monolayer (if the volume of material spread is known). Three distinct regions of the curve are apparent, corresponding to the different phases of the film. When the film area is still large, the molecules are spread out in the "gas" phase; as the film is compressed, it passes through a "liquid" phase until all the molecules are upright (as shown in figure 7.2a), forming a quasi-solid which is increasingly difficult to compress further as denoted by the steep slope of the curve at the left-hand side of the plot. Eventually, the increasing surface pressure causes the film to buckle and collapse, as shown at the left of the quasi-solid region in figure 7.4. To ensure good transfer to a substrate, it is best to dip a film at a pressure corresponding to this quasi-solid region - as this may vary for different materials, the above procedure must be carried out to optimise the dipping conditions for each.

Transfer of the spread monolayer to a prepared substrate is accomplished by attaching the sample to the micrometer screw assembly and compressing the spread film to the desired surface pressure. The micrometer is then lowered and raised to dip the substrate into the subphase at a set rate, depositing a monolayer on each traversal of the surface; the surface pressure is kept constant by the differential feedback circuit, which controls the barrier motor so that the film area is reduced as molecules are transferred to the substrate.

The way in which the LB film is deposited depends upon the organic material, the substrate composition and preparation, and on the deposition conditions. Three modes of deposition have been identified; these are known as X-type, Y-type and Z-type as defined in figure 7.5. The common deposition mode, which was observed for all films deposited in this work, is Y-type, where

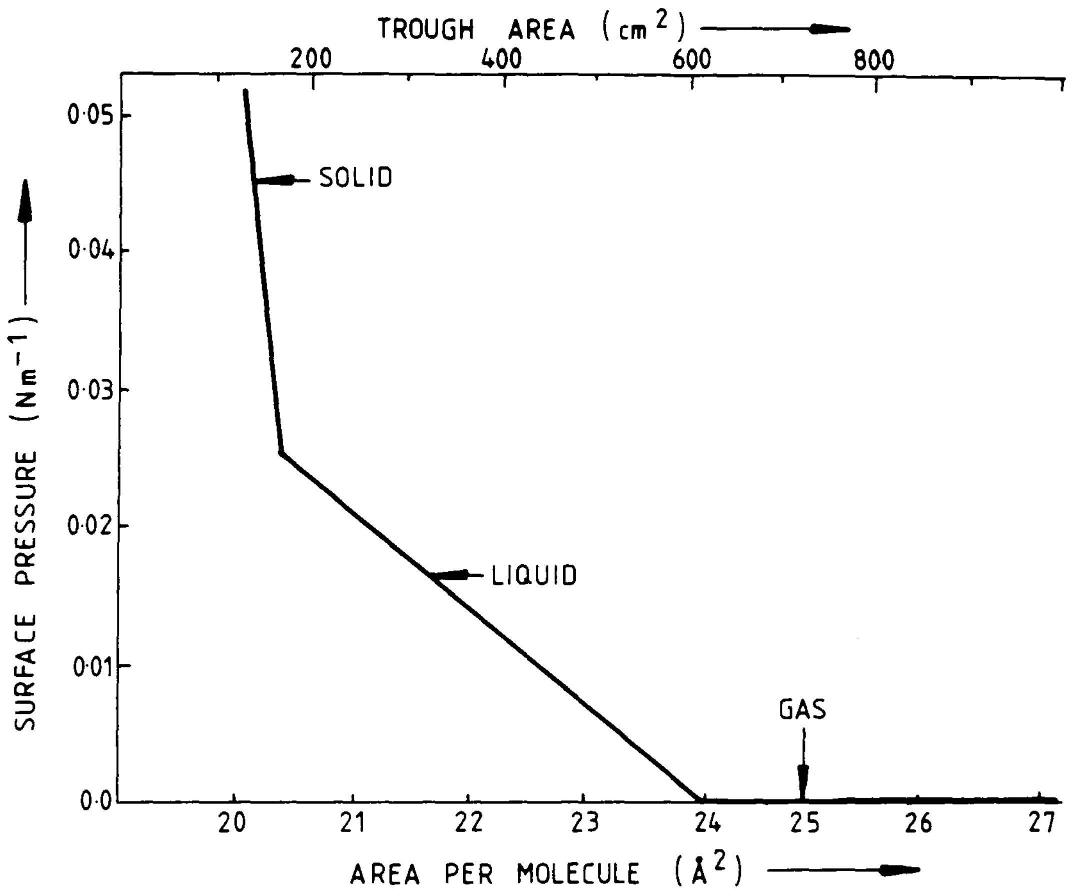


Figure 7.4 : Surface pressure versus trough area isotherm for stearic acid

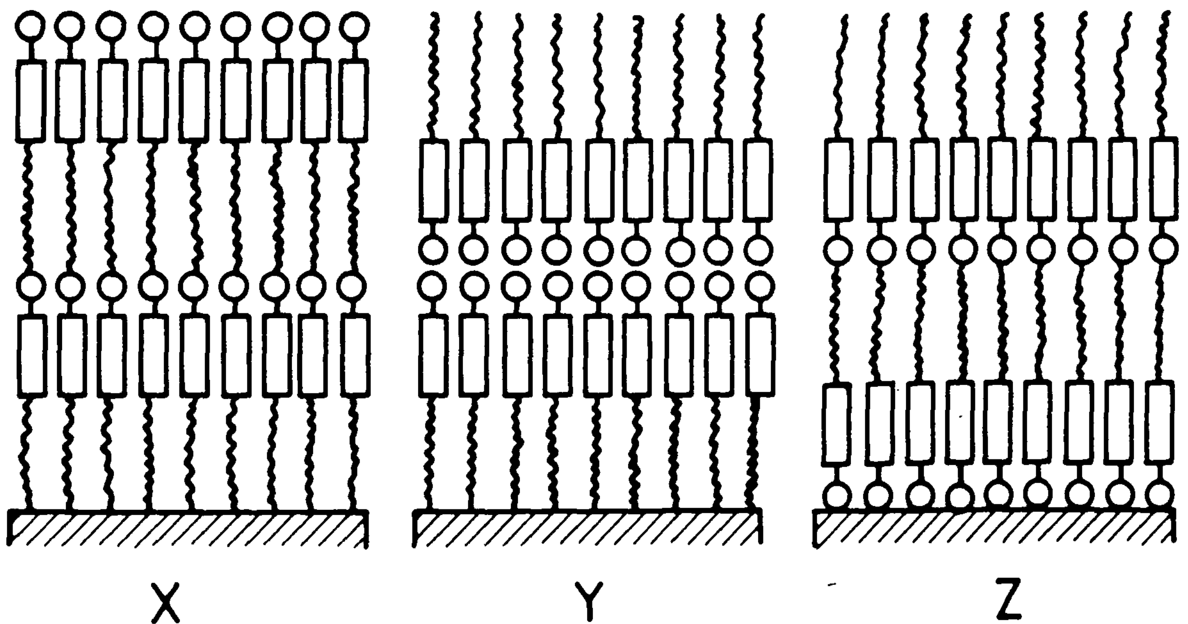


Figure 7.5 : LB Film deposition modes

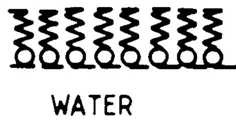
the molecules stack vertically in a head-to-head and tail-to-tail formation. However, the precise multilayer configuration is influenced by the properties of the substrate. The process of monolayer deposition onto a hydrophilic substrate (e.g. de-greased glass or silicon dioxide surfaces) is illustrated in figure 7.6. When the sample is introduced to the subphase, no deposition occurs (as the substrate surface is hydrophilic and the exposed film surface is hydrophobic); the first monolayer is coated on withdrawal as the hydrophilic end of the film comes into contact with the wetted substrate. Subsequent monolayers are deposited on each traversal through the film surface. For a substrate which has a hydrophobic surface (e.g. silanized silicon), the initial layer is picked up as soon as the sample is immersed in the subphase (i.e. on the first insertion); the procedure is otherwise similar to that described above.

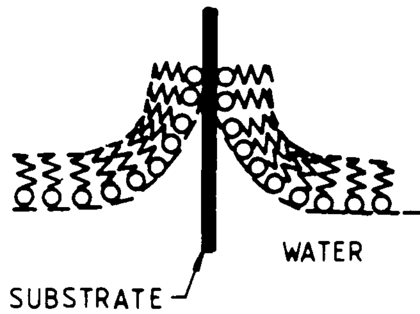
After deposition, samples should be desiccated in order to remove any excess water present in the multilayer film, and great care should be taken with device storage and handling (as with any thin film sample which may be easily scratched or otherwise damaged).

7.1.4 Automated LB film deposition

It is desirable to incorporate a degree of automation into the Langmuir trough instrumentation in order to maintain close control over the deposition process and to obtain easily-reproducible LB films. This has been achieved by interfacing the trough control electronics to an IBM Personal Computer. By means of digital-to-analogue (D-A) and analogue-to-digital (A-D) conversion circuitry, the computer may read in and send out analogue voltages to monitor and control the operation of the associated electronics.

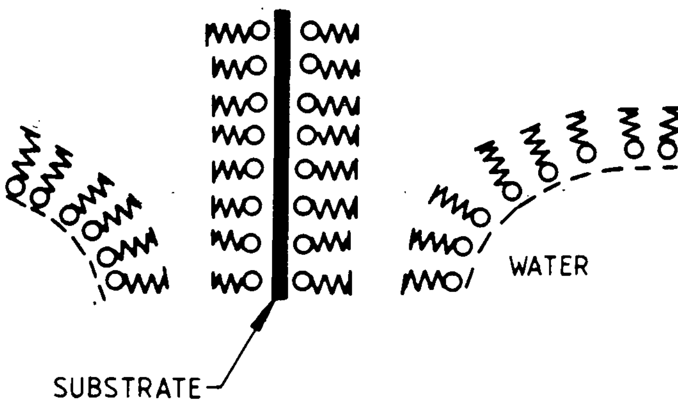
With computer control, the basic operation of the trough as outlined in sections 7.1.2. and 7.1.3. is greatly simplified. Self-contained programs, written in Advanced BASIC, were developed to enable calibration of trough geometry, electrobalance and dipping

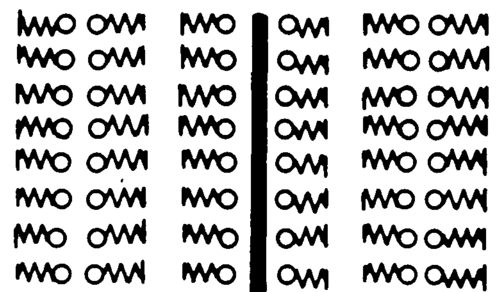




(a) MONOLAYER ON THE SURFACE OF THE WATER

(b.) FIRST LAYER ON WITHDRAWAL





(c) SECOND LAYER (2nd INSERTION)

(d) SUBSTRATE WITH THREE LAYERS (AFTER 2nd REMOVAL.)

Figure 7.6 : Schematic diagram of monolayer deposition onto a hydrophilic solid surface

speeds, to record pressure-area isotherms, to monitor film area over a period of time (in order to measure the stability of the spread monolayer), and to control the deposition of multilayer structures onto a substrate. All experimental parameters are stored on a floppy disc so that dipping conditions can be precisely reproduced at any later time.

The control programs allow the positions of the PTFE barrier and the micrometer dipping head to be continuously monitored, and also the directions and speeds of the barrier and dipping head motors to be precisely controlled; the surface pressure of the film is also measured. Additional programs were written to manipulate and produce graphical plots of the data recorded during isotherm measurement and film deposition experiments.

Further details of this automated experimental system, which is now available commercially, can be found in Appendix C.

7.2 Experimental Details

Before depositing LB films of ω-tricosenoic acid onto substrate materials, it was necessary to determine the optimum conditions for the dipping process. This was achieved by recording the surface pressure-area isotherm as described in the previous section and the resulting characteristic is shown in figure 7.7. By comparison with the stearic acid isotherm of figure 7.4 it is apparent that the points at which phase transition occurs are not so clearly defined. However, the quasi-solid region may be identified for a surface pressure range of approximately 15 to 40 mN/m, above which the monolayer collapses; this is in agreement with other workers investigating ωTA [6]. Consequently, a surface pressure of 35 mN/m was chosen for dipping LB films of the material.

To characterise the basic electrical properties of ωTA, LB films of varying thickness were deposited onto an aluminium-coated glass slide and top contacts of 20 nm Al plus 20 nm Au were evaporated onto this insulator to form a number of MIM capacitor structures.

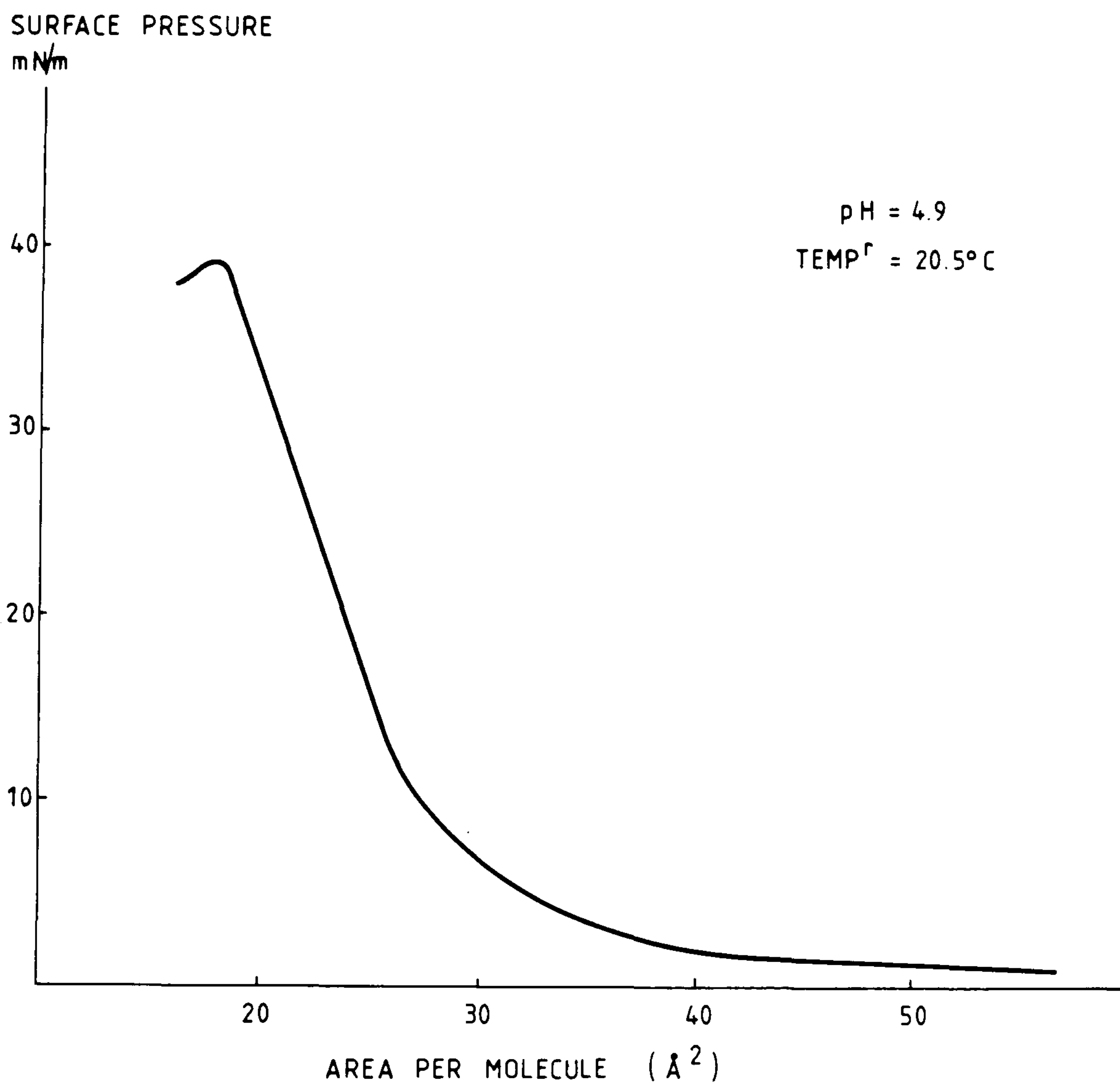


Figure 7.7 : Measured pressure-area isotherm for ω-tricosenoic acid

The reason for this two-stage process is that gold is the better metal to which to make external electrical contact (as it does not oxidise in air) but is very mobile and likely to penentrate and contaminate the thin ωTA insulator; by evaporating aluminium first, this may be largely avoided. It is important that the metal electrodes are deposited in stages (a few nm at a time at a very slow rate) in order to prevent excessive heating of the substrate which might damage the LB film. This procedure was followed for top electrode deposition onto all the LB film samples examined in this work.

Thin films of ωTA were also coated onto silicon substrates and top contacts of 20 nm Pd evaporated. These substrates varied in their composition and preparation: some were dipped immediately after etching in buffered (40% concentration) hydrofluoric acid (HF), others had ωTA deposited onto thin layers of SiO_2. The reasons for these differing treatments will become apparent in the ensuing results sections of this chapter where they will be fully discussed.

After preparation, all samples were kept under dry nitrogen in a desiccator (except where detailed later). Full details of device processing are given in Appendix B2.

The electrical measurements made on the various devices fall into three categories. To determine the dielectric permittivity of the LB film insulator, the capacitances of MIM structures of different thicknesses were recorded, and the 1/C versus N relationship plotted (section 3.1.4). C-V and G-V experiments were performed on the MIS samples to calculate the flat-band voltage and the amount of charge present in the insulator (as detailed in sections 3.1.1 and 3.1.2). Finally, full surface state analysis of the devices ($N_{ss} - \psi_s$ determination as in chapter 6.3) was attempted in air and also in a 0.8% hydrogen/nitrogen atmosphere. The results of these experiments are reported in the remainder of this chapter.

7.3 Results and Discussion

It was shown in the previous chapter that the influence of hydrogen on the energy states at the surface of silicon can be used as a means of detecting this gas. The density of these states present in practical devices is generally low, due to the properties of the natural oxide which forms a passivating layer on the bare silicon surface. Consequently only small changes in surface state population are observed due to the influence of hydrogen. If, however, the number of states at the surface can be increased by some means, then it is anticipated that a much larger hydrogen effect may be detected.

One possible cause of the interface traps mentioned above is the unpaired surface Si electron (dangling bond) created by imperfect lattice matching between the Si and SiO_2 regions (see chapter 2.2.1). Thus it is likely that by removing the passivating oxide completely the number of dangling bonds (and hence the surface state density) will be greatly increased.

7.3.1 Preliminary studies

In order to test this theory, part of a SiO_2-Si wafer was etched in buffered HF to remove the oxide layer and top electrodes were vacuum-evaporated onto the freshly-etched silicon surface (sample N3 : see Appendix B2). It should be noted that a true Schottky barrier is not formed by this process since a thin ($\sim$2nm) nascent oxide layer grows on the bare silicon immediately upon contact with the atmosphere [14]. Although this thin SiO_2 region cannot be prevented, its passivation properties are significantly inferior to those of a controlled-growth thick oxide and so a larger surface state density will result. An attempt was made to perform C-V measurements on this device, but this was not possible because the ultra-thin silicon dioxide layer would not support an applied voltage of larger than a few tens of millivolts without electrical breakdown. Consequently, surface state analysis was not possible since the device could not be biased into accumulation for oxide

capacitance and series resistance calculation (even if this were possible, it is likely that the high leakage current would obsure the detection of a conductance peak in a similar way to the series resistance effect as discussed in section 5.2.4).

To overcome this problem, it is necessary to find some sample treatment by which the surface state density is increased, whilst still retaining an insulator capable of supporting a bias voltage. Use of a LB film insulator was considered as a possible solution; other workers [15] have suggested that tunnelling is the predominant low-field conduction process in a LB film monolayer, and multilayer structures have been shown [11] to possess very good insulating properties.

Of the many organic materials suitable for depositing monolayers by the LB technique, ω-tricosenoic acid seems to offer a number of advantages for this purpose, as outlined in section 7.1.1. However, the most interesting aspect of ωTA is its apparent ability to seal off thin native oxides on silicon, as demonstrated by electron spin resonance (esr) experiments [16]. Not only does the ωTA film allow voltages to be applied to the device (enabling surface state analysis) but also retards the rate of oxide growth, which would normally take place in the atmosphere over several weeks. Consequently, ωTA was chosen as the most suitable material for depositing multilayer structures onto freshly-etched silicon substrates for the experiments to be preformed in this work.

7.3.2 Electrical characterisation of ωTA LB film insulators

The quality and reproducibility of LB multilayers can be indicated by recording the a.c. capacitance for a varying number of monolayers deposited in a MIM or MIS structure. Data obtained for ωTA films of different thicknesses sandwiched between 60nm Al (on glass) and 20nm Al/20nm Au top electrodes (sample M1: Appendix B2) are shown in figure 7.8 as a plot of 1/C versus N. The linear dependence demonstrates the degree of control over film thickness which can be achieved by depositing monolayers of this material. Later results for multilayer structures of ωTA incorporated into a MIS device (sample N6A) are recorded in figure 7.9; again a straight line dependence is observed for the reciprocal capacitance plot.

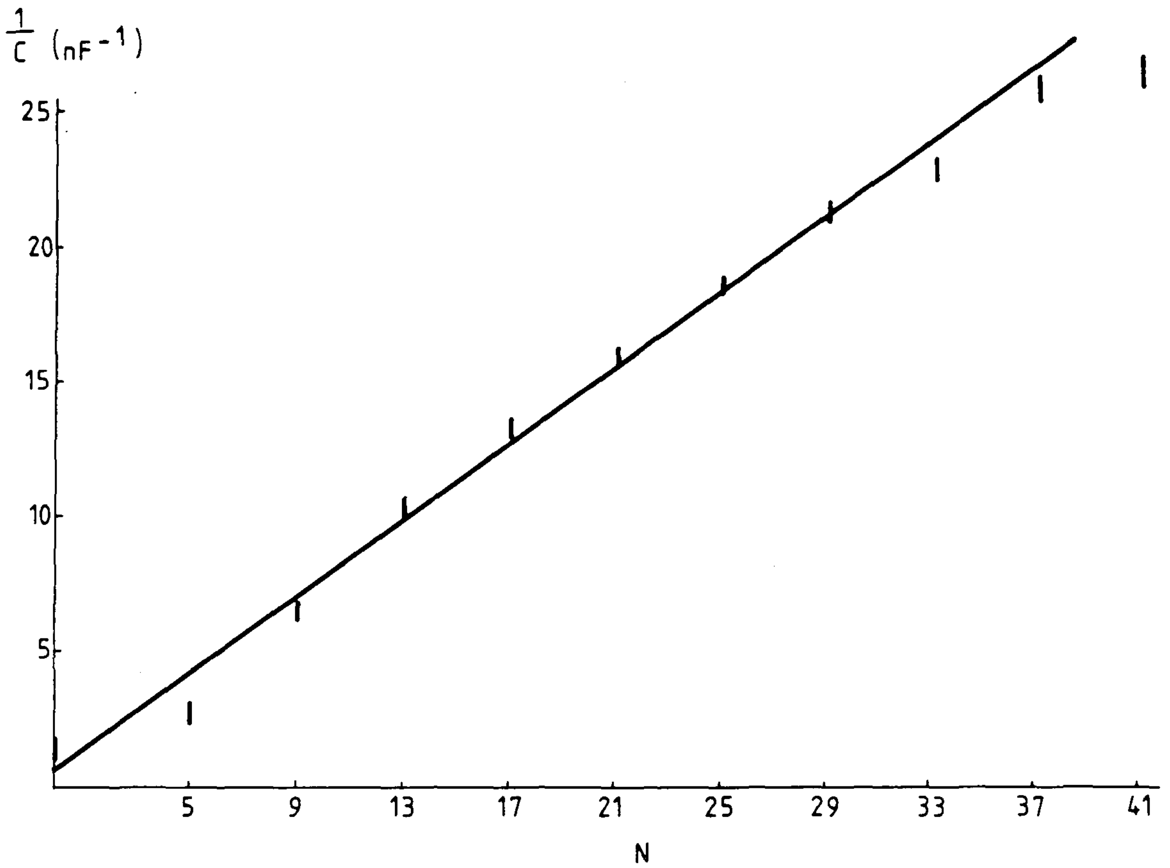


Figure 7.8 : Plot of 1/C versus N for MIM structure incorporating ωTA multilayer insulator (100 kHz)

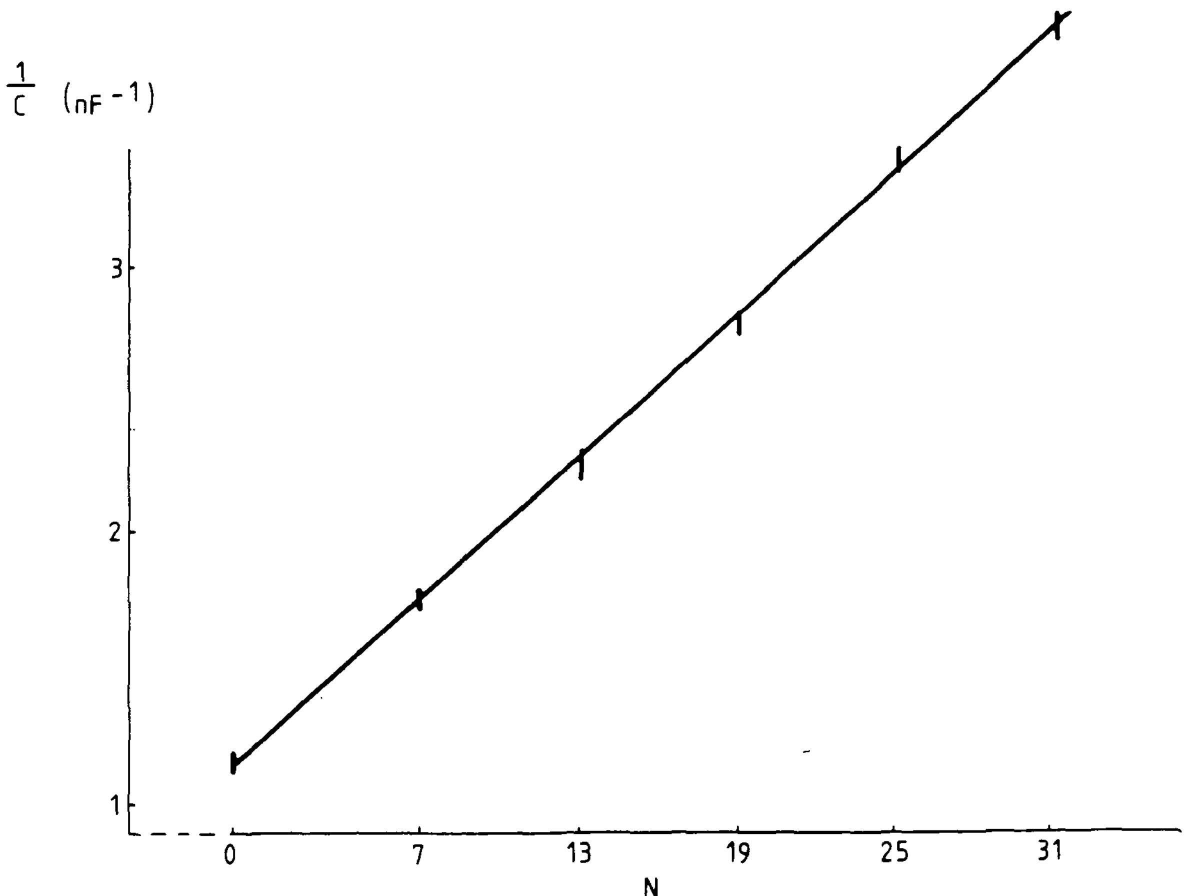


Figure 7.9 : 1/C versus N relationship for MIS structure incorporating ωTA multilayer insulator (100 kHz

From these straight line plots, further information about the insulator may be extracted. As described in section 3.1.4, the dielectric permittivity of the ωTA film may be calculated from the slope of the line (equation 3.7) if the monolayer thickness is known, and details of the interfacial layer between film and substrate can be obtained from the intercept (equation 3.8). Other workers have observed the thickness of a ωTA monolayer as 3nm [6]; applying this quantity to the above results returns closely agreeing values for the relative permittivity of 3.02 ± 0.15 and 3.04 ± 0.12 (for ωTA films deposited in MIM and MIS structures respectively). These values are both higher than would be expected for a molecule of 3nm in length. Results obtained with comparable materials [17, 18] are reproduced in Table 7.1; these suggest that the dielectric constant of ωTA would be approximately 2.4-2.5. One possible explanation for this discrepancy may be the way in which monolayers of ωTA are deposited. Electron diffraction studies have shown [19] that these monolayers are tilted at an angle of approximately 18° from the perpendicular when built up on a substrate, which will reduce the effective thickness of the deposited monolayers by a factor of cos 18° (∿0.95). The modified monolayer thickness is ∿ 2.8 nm, and this results in lower calculated values of relative permittivity of 2.82 ± 0.14 and 2.83 ± 0.11; these are still a little higher (although within error margins) than the comparable cadmium arachidate material (see Table 7.1), but this may be accounted for by the double bond in the ω-tricosenoic acid molecule. The non-zero intercept is due to the presence of an additional dielectric layer in the samples; for the MIS device this is the SiO_2 onto which the film was deposited, but in the MIM structure it is likely that this effect is caused by a thin layer of aluminium oxide formed during device processing. Assuming a value of between 4 and 8 for the relative permittivity of Al_2O_3, this implies that the metal oxide region is some 4.5 to 9nm in depth (from equation 3.8).

Having determined the dielectric permittivity of ω-tricosenoic acid monolayers, as required for interface state analysis, MIS structures with LB film insulators of this material were analysed more thoroughly to determine the effects of the film on electrical properties and silicon surface states.

Material	Monolayer Thickness	Relative Permittivity (at 1kHz)
Cadmium stearate (ref. 15)	2.58 nm	2.71 ± 0.17
(ref. 16)	2.58 nm	2.7 ± 0.3
Cadmium arachidate (ref. 15)	2.80 nm	2.52 ± 0.17
(ref. 16)	2.80 nm	2.5 ± 0.2

Table 7.1 : Monolayer thicknesses and relative permittivity values for LB films of long chain fatty acids

7.3.3 Effects of ωTA insulators on MIS device properties

Capacitance- and conductance-voltage experiments were performed on a MIS device fabricated by depositing ωTA multilayers of different thicknesses onto a freshly-etched n-type silicon substrate and evaporating top electrodes of 20 nm Pd (sample N4: see Appendix B2). Typical C-V and G-V characteristics for an insulating film of 8 monolayers for ω-tricosenoic acid are shown in figures 7.10a and 7.10b for a positive-going voltage sweep. These data indicate that the device may be biased into accumulation by applying a voltage of approximately +4V; the accumulation capacitance is 1353 pF, which agrees closely with that expected (1360 pF) for the insulator thickness, top electrode area and the value of permittivity calculated above. This shows that there is very little native SiO_2 on the silicon surface. Comparing the conductance curve (figure 7.10b) with that obtained for a device with a 12nm SiO_2 insulator (figure 6.9b) it can be seen that the G_m/ω peak is at approximately the same voltage position (∿+ 0.3V but that the peak height is some twenty times greater (∿600 pMho/Hz as opposed 30 pMho/Hz). This indicates the presence of a much higher interface state density.

Similar plots were obtained for various numbers of ωTA monolayers; these data are shown in figures 7.11a and 7.11b. The changing capacitance value is due solely to the different insulator thicknesses. One interesting feature of the C-V curves is the change in their position with respect to the voltage axis; as more layers are deposited, the curves exhibit a lateral shift in the positive voltage direction, which is indicative of negative charge accumulation in the insulator. This cannot be accounted for by mobile ions in the structure as the hysteresis C-V/G-V plots (figures 7.12a, b) show a 0.4V variation in voltage position, which is smaller than the 0.6V total shift of curve position in figures 7.11a and 7.11b. Therefore an amount of fixed negative charge must be trapped within the monolayers of ωTA deposited by the LB process. This phenomenon is considered in more detail in the following chapter.

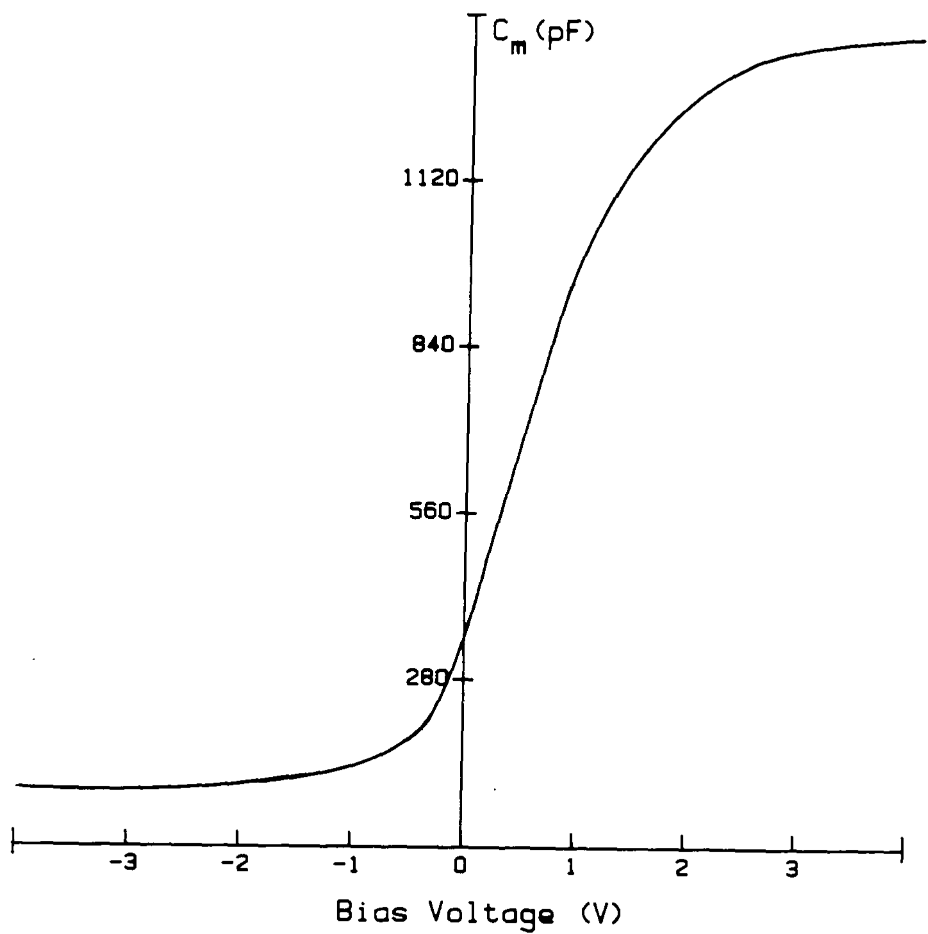


Figure 7.10a : C-V plot for MIS device with 8 layer ωTA insulator (100 kHz)

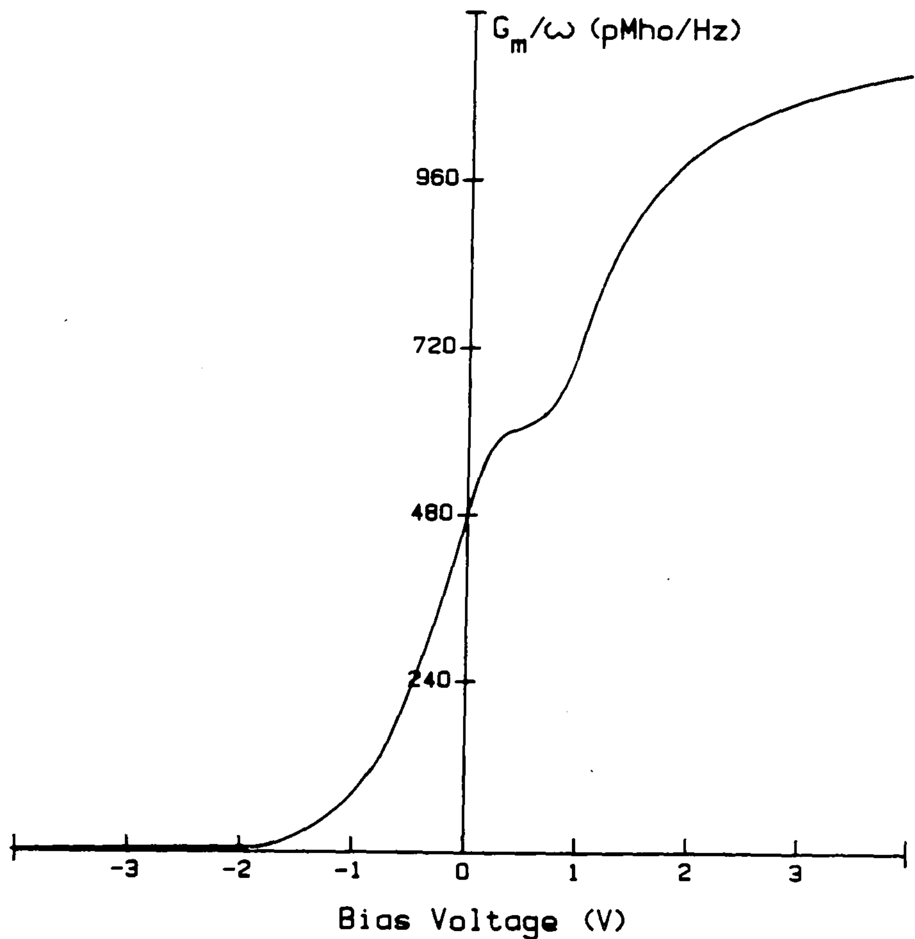


Figure 7.10b : G-V plot for MIS device with 8 layer ωTA insulator (100 kHz)

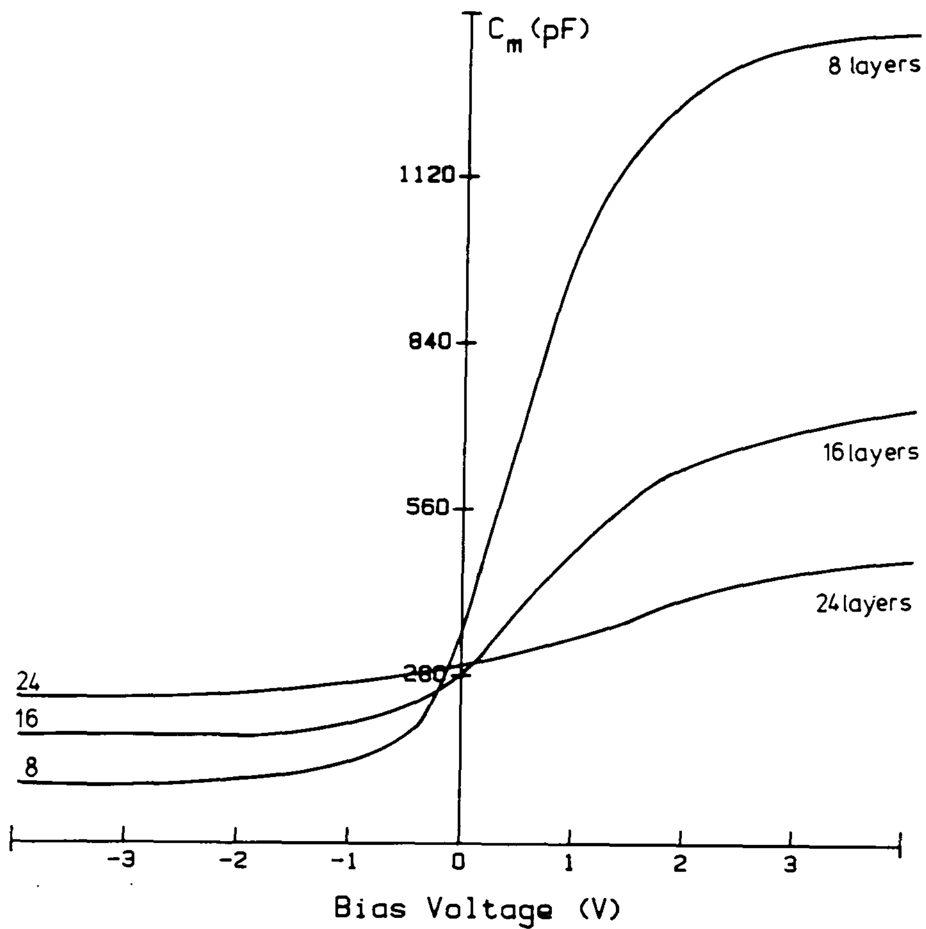


Figure 7.11a : C-V curves for MIS device with insulators of 8, 16 and 24 ωTA monolayers (100 kHz)

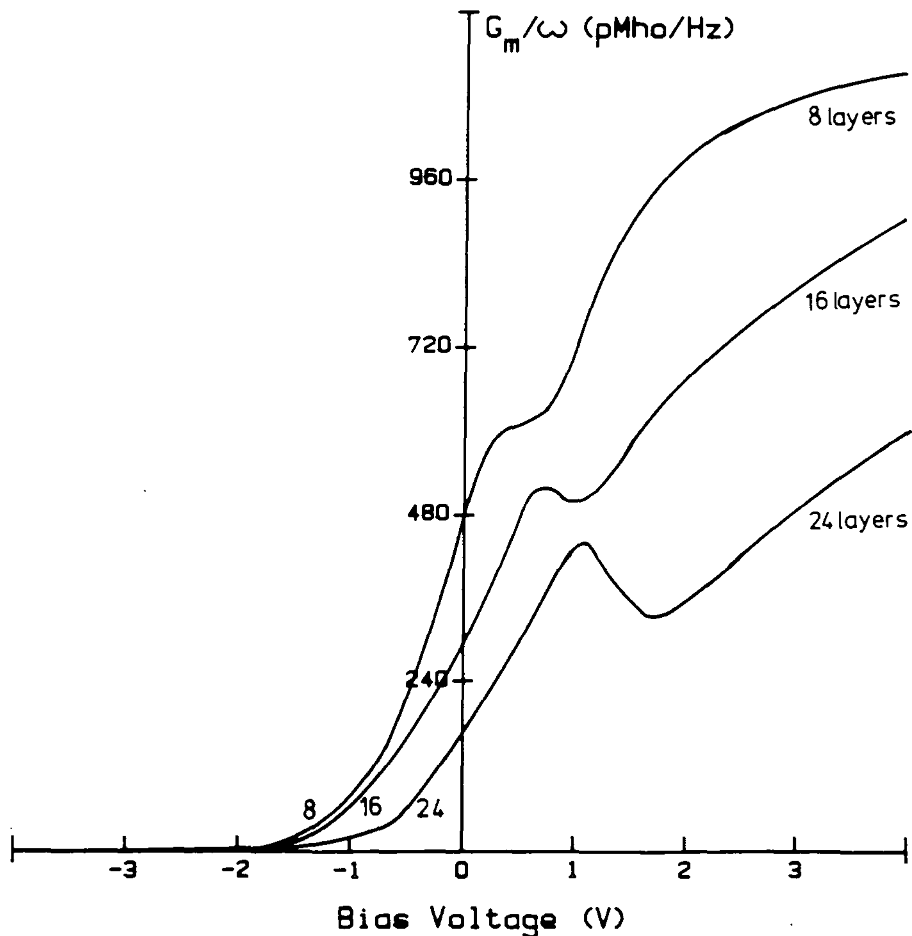


Figure 7.11b : G-V curves for MIS device with insulators of 8, 16 and 24 ωTA monolayers (100 kHz)

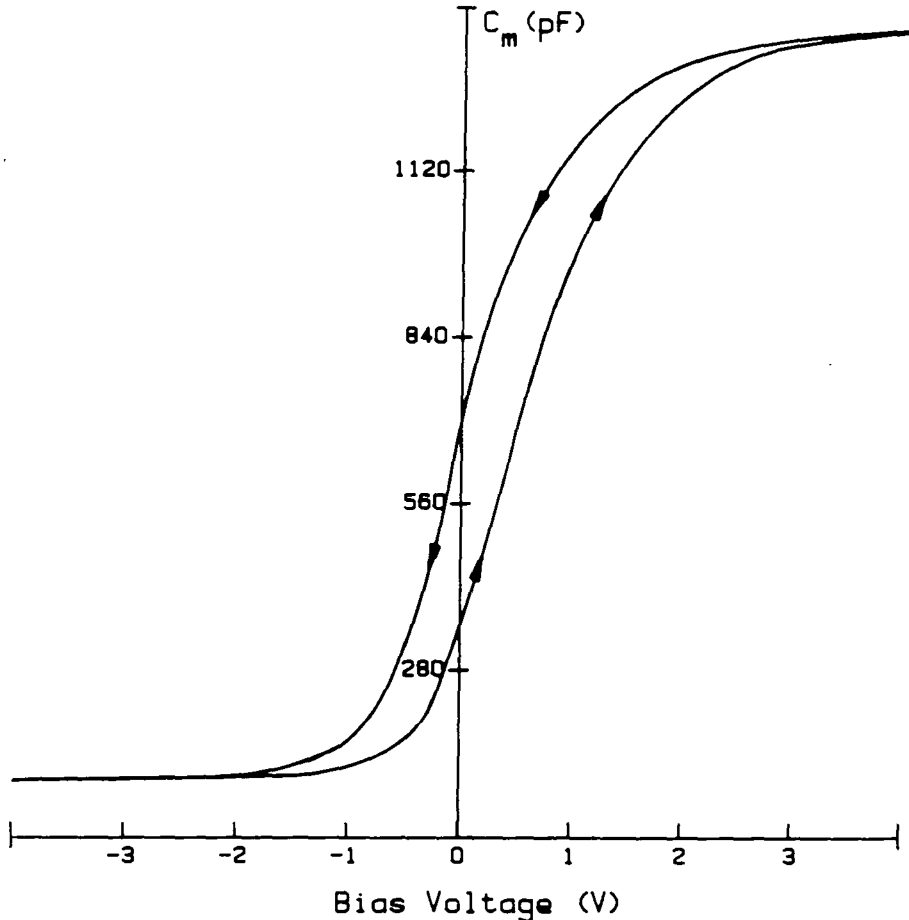


Figure 7.12a : Hysteresis C-V plot for MIS device with 8 layers ωTA insulator (100 kHz)

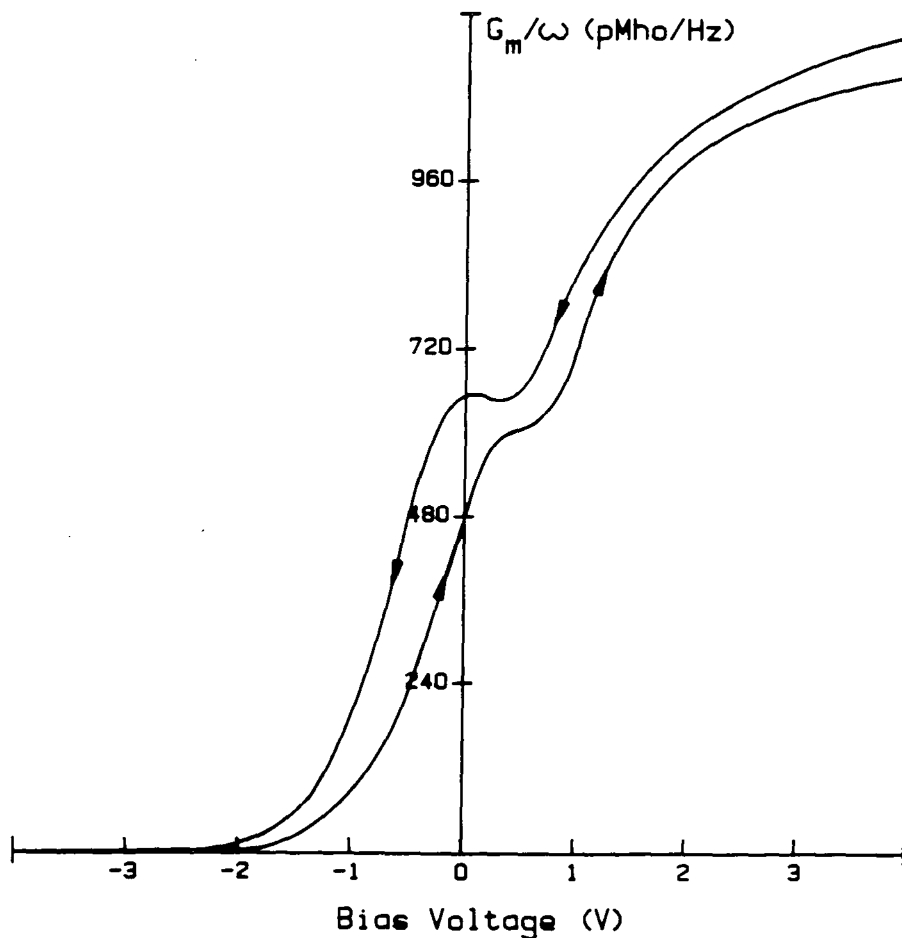


Figure 7.12b : Hysteresis G-V plot for MIS device with 8 layers ωTA insulator (100 kHz)

Further investigation into the surface state changes observed above was carried out, and the results obtained by applying the a.c. conductance technique to analyse these devices are presented below.

7.3.4 Influence of ωTA LB films on silicon surface states

Some difficulty was encountered when extracting the parallel capacitance and conductance values from the a.c. admittance data obtained from swept-frequency experiments (see section 3.2.2) due to the high value of conductance observed when approaching accumulation, as demonstrated in the previous section. This had the effect of obscuring some of the conductance peaks, and also made calculation of the series resistance difficult. In addition, the degree of hysteresis exhibited by the structure (figure 7.12) increased the error in measurement of surface potential, ψ_s, due to the possible variation of the ψ_s-V relationship. However, this problem was partially overcome by biasing the sample in accumulation for a few minutes before starting the frequency scan at the desired measurement voltage; this was done to remove most of the mobile ions from the insulating layer before performing the experiment. The surface state densities observed at different positions in the bandgap are recorded in figure 7.13; these are between 15 and 20 times greater than the N_{ss} density values recorded for the devices with thermally-grown oxides examined in chapter 6, and the plot follows the same general shape as those of the unannealed specimens analysed therein (figures 6.16 and 6.17). However, these results could not be readily reproduced: although surface state densities of the same order of magnitude as those determined above were obtained, there was a significant variation in the exact N_{ss}- ψ_s values calculated, as reflected in figure 7.14 which shows the wide range of recorded points for different fixed bias voltages; clearly, no changes in N_{ss} will be detected with any great degree of accuracy. This effect is attributable both to the uncertainty in calculation of surface potential introduced by the amount of mobile ionic charge in the insulator and to the fact that an unpassivated silicon surface is inherently less stable than one which has a thermally-grown oxide.

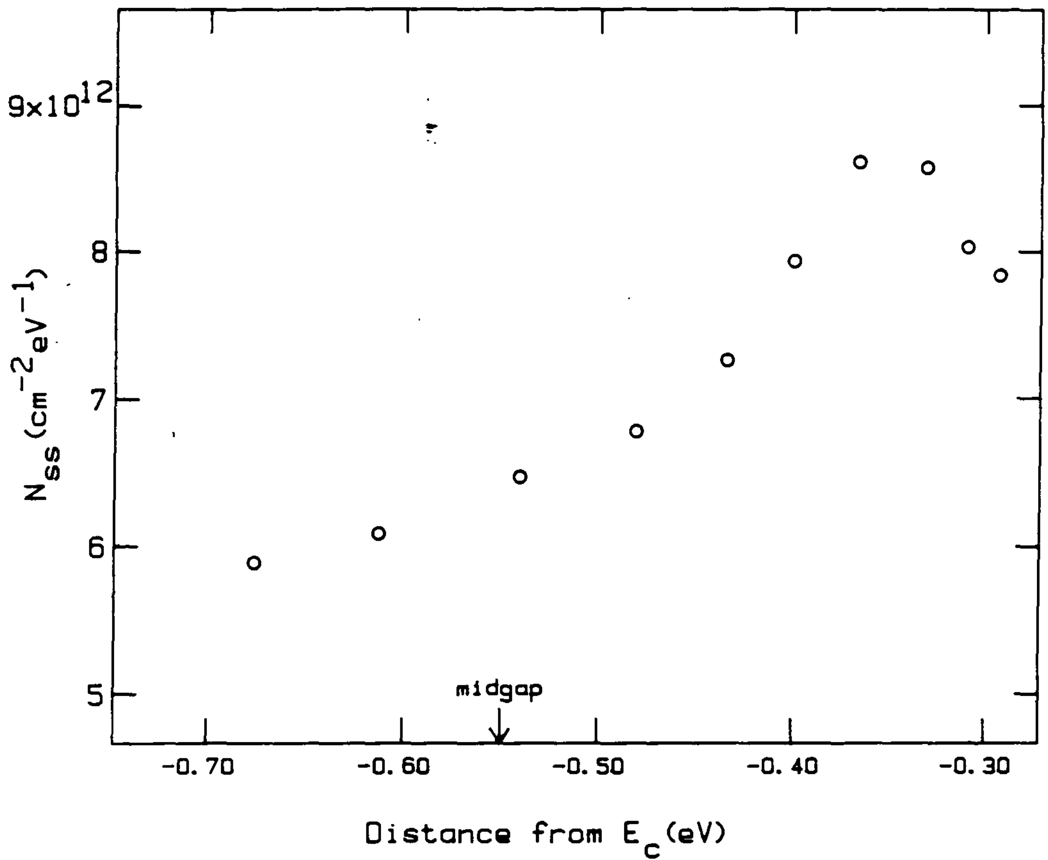


Figure 7.13 : N_{ss} profile for MIS device with 8 monolayers of ωTA

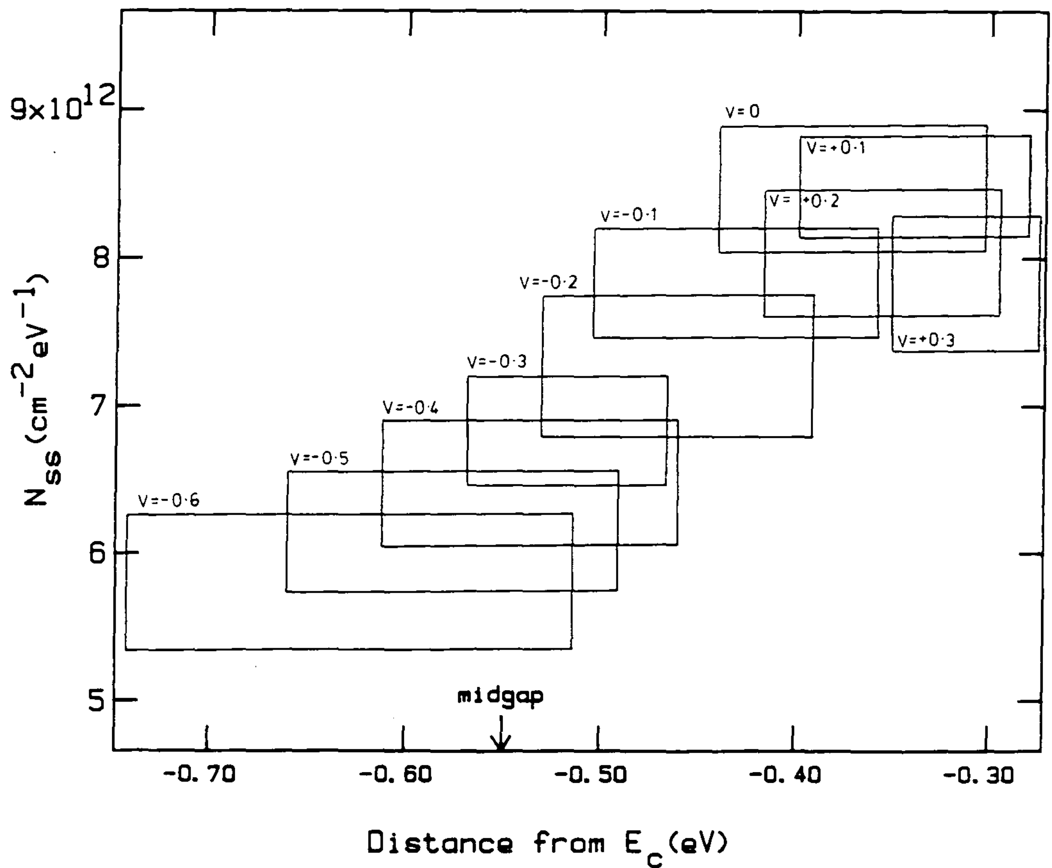


Figure 7.14 : Range of N_{ss} values obtained at different bias voltages for 8 layer ωTA MIS device

Consequently, the conductance technique for full interface state analysis cannot be applied to this device, and so quantitative measurement of the changes in surface state density distribution, as carried out in chapter 6, is not possible. However, the technique of C-V and G-V plotting may still be useful, because of the direct relationship between the G/ω peak height and the corresponding N_{ss} value which does not require ψ_s to be determined; therefore it should be possible to make qualitative observations of the external influences on N_{ss} by monitoring the changing G/ω peak. This procedure is utilised in the next two sections to determine the effects of aging and the influence of gases on the surface state density.

7.3.5 Aging effects on interface state density

The results of the esr experiments of Roberts et al.[16] mentioned earlier indicated that a LB film of ωTA deposited onto a freshly-etched silicon substrate may act a barrier to atmospheric oxygen and moisture, effectively sealing the bare silicon surface and retarding the growth of the natural oxide. These workers observed that on an uncoated sample there was evidence that oxide growth was well established some ten days after etching although a device coated with a LB multilayer of ωTA showed no such signs of oxide formation during this period.

To investigate the long term sealing ability of ωTA films, G-V measurements were performed on two devices: one dipped with 8 layers of ωTA as soon after etching as possible (<10 minutes in practice), and one dipped with the same number of layers 13 days after etching (samples N4 and N5). Figure 7.15 shows the G/ω-V plots recorded at 100 kHz for each device immediately after LB film deposition. A significantly larger peak signal is observed in the device coated soon after etching, denoting a higher surface state density and therefore little oxide formation compared with the sample dipped almost two weeks after the etching treatment. This experiment was repeated at various intervals over a period of one year; the samples were kept in a dust-free container (closed sample box) but left in the atmosphere. For all these subsequent G-V experiments, which

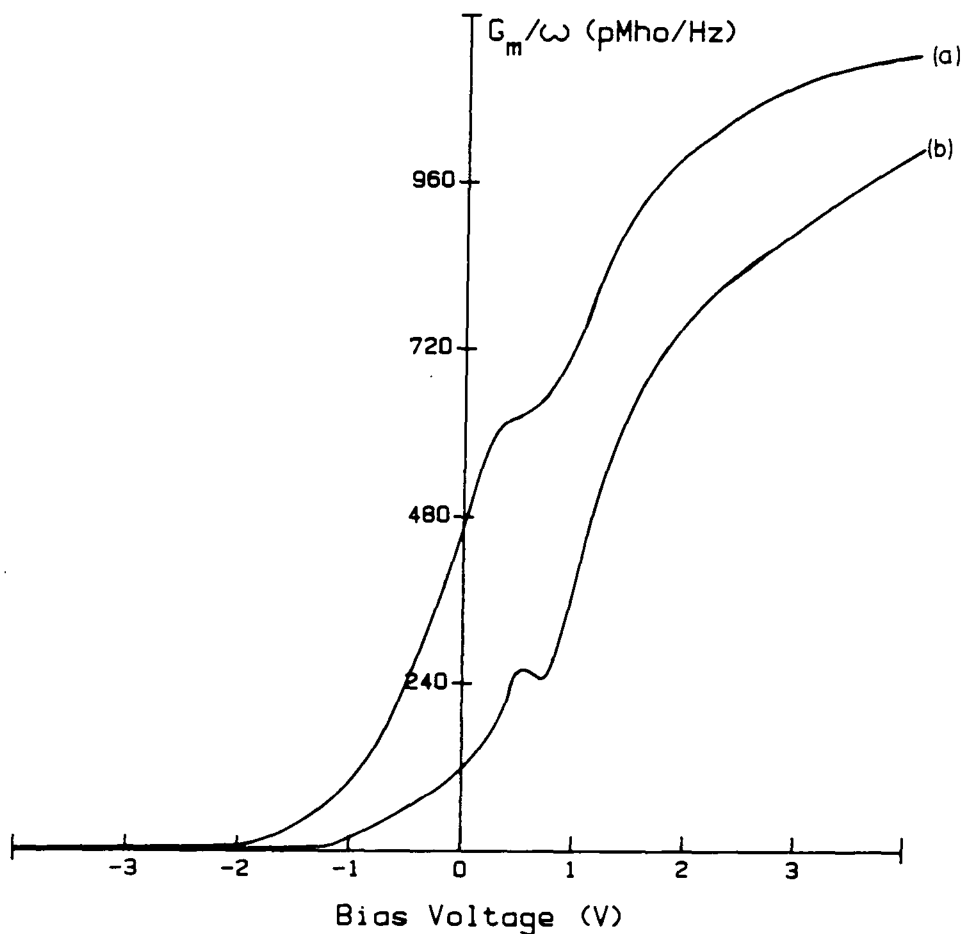


Figure 7.15 : Conductance-voltage response for freshly-etched and aged MIS devices at 100 kHz

(a) Sample N4 : 8 layers ωTA deposited <10 minutes after etching silicon substrate

(b) Sample N5 : 8 layers ωTA deposited 13 days after etching silicon substrate

were performed at a frequency of 100 kHz, the G/ω peak was observed at the same voltage position, and the change in G/ω height is recorded in figure 7.16 for the two devices.

These plots indicate that over the observation period the surface state density (as indicated by the G/ω height) decreases for both samples. For the device coated some time after etching, this change is slight (which would be expected since the native oxide grown in the time before film deposition would be reasonably mature). However, the sample coated immediately after etching exhibits a more marked decrease in peak height over the same period; even so, the measured signal remains much higher than the other sample and remains constant after some ten weeks or so. These results suggest that the ωTA film does indeed retard the rate of growth of an SiO_2 layer; moreover, the surface state density, after initially decreasing, remains at a constant value (albeit higher than the device with a matured oxide), signifying that no further oxide growth has occurred.

The above result is notable in that it establishes a method by which the surface state density of a MIS structure may be increased, which suggests a possible use as an enhanced mechamism for gas detection. This application is examined in the next section.

7.3.6 Effects of Hydrogen gas on ωTA LB film MIS devices

It has been demonstrated above that LB films of ω-tricosenoic acid coated onto a freshly-etched silicon substrate act as a barrier to oxygen (O_2), retarding oxide growth and enabling larger surface state densities to be obtained. If this structure allows smaller gas molecules, such as H_2, to penetrate to the insulator-semiconductor interface, it may be more sensitive than the devices analysed in the previous chapter, for which a limited surface state effect was observed upon exposure to hydrogen gas.

Figure 7.17 shows the results of C-V and G-V experiments performed on the Pd-gate MIS sample whose insulating layer was an 8 layer ω TA LB film dipped immediately after etching the silicon substrate with buffered HF (sample N4). When exposed to a 0.8% hydrogen/nitrogen atmosphere, both capacitance and conductance curves show a lateral

G_m/ω (pMho/Hz)

(a) SAMPLE N4

V = +0.3V

f = 100 kHz

600

400

200

12 24 36

TIME (WEEKS)

G_m/ω (pMho/Hz)

(b) SAMPLE N5

V = +0.3V

f = 100 kHz

300

200

100

12 24 36

TIME (WEEKS)

Figure 7.16 : Record of G_m/ω peak values versus time

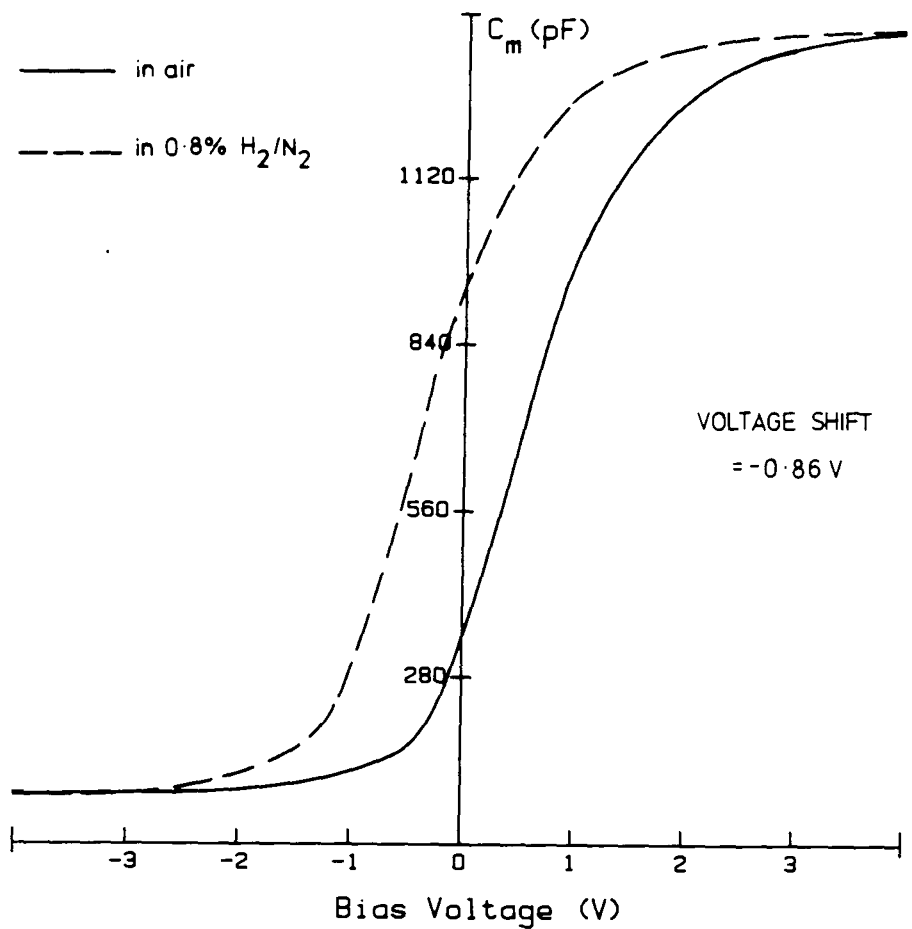


Figure 7.17a : Hydrogen effects on C-V curve for freshly-dipped 8 layer ωTA MIS device (100 kHz)

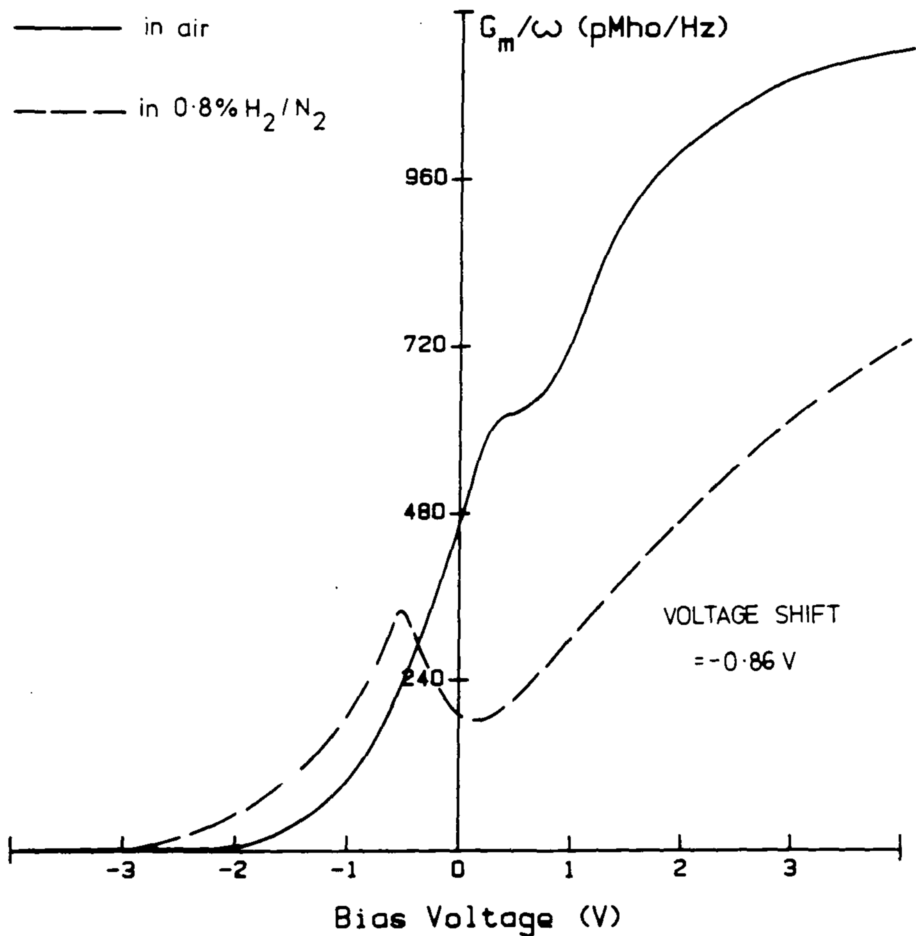


Figure 7.17b : Hydrogen effects on G-V curve for freshly-dipped 8 layer ωTA MIS device (100 kHz)

shift of -0.86V (towards inversion) which is very similar in magnitude to that recorded (-0.90V) for the MOS devices investigated in chapter 6. However, there is a significant decrease in the G/ω peak height, indicating that the gas-induced surface state change first observed in the last chapter (section 6.3.2) is much more pronounced in this device. This effect can be directly assigned to the increased surface state density produced by the ωTA deposited film, and shows that although this layer prevents the passage of oxygen, the smaller hydrogen gas molecules may permeate through it. Once again, the effect is reversible: the curves return to their original positions after the sample is removed from the hydrogen atmosphere, proving that the N_{ss} response is not due merely to some form of annealing process (see section 6.3.3).

7.4 Summary

In this chapter, the procedure for depositing LB films of an organic material has been discussed and the electrical properties of ω-tricosenoic acid multilayers have been investigated. The relative permittivity of this material has been experimentally determined, giving a value of $\varepsilon_r = 2.82 \pm 0.14$, and the effects of film aging have been reported.

Interface state analysis of MIS devices fabricated by depositing a LB multilayer of ωTA onto freshly-etched silicon to prevent formation of the natural passivating oxide has shown that the number of impurity states at the silicon surface is increased by this treatment. Furthermore, the sensitivity to hydrogen gas of these states is greatly improved (as propounded in chapter 6).

A degree of charge incorporation in the deposited multilayer structure has been indicated by some of these experiments; this aspect is considered in detail in the following chapter.

CHAPTER 8 : CHARGE INCORPORATION IN LB MONOLAYERS

8.0 Introduction

From the C-V results obtained for devices with an insulating layer of ω-tricosenoic acid, there is some evidence of a degree of negative charge being introduced into MIS structures incorporating Langmuir-Blodgett films of this material. This is clear in the C-V curves shown in figure 7.11, which exhibit a lateral voltage shift where ωTA monolayers are deposited; this shift is larger than that which can be attributed to mobile ions in the insulator (as indicated by the hysteresis plot of figure 7.12 for the same sample).

The additional charge may be a result of dipole layers in the multilayer insulator or alternatively to a point charge concentration within the structure. However, the mechanisms of charge incorporation are not clear, and the precise origins cannot be determined from the analysis of these C-V curves alone.

In order to investigate this phenomenon further, LB films of ωTA were deposited onto a number of n-type silicon substrates with a thermally-oxidised 32nm SiO_2 layer; the reason for dipping samples which already had an oxide present was to improve the device stability and to ensure that the number of surface states was relatively low. Different dipping parameters were employed for each substrate in an attempt to identify the influences on the amount of charge incorporated in the structure. The effects of moisture and storage conditions were also investigated.

The results of these experiments are presented in this chapter and the possible charge incorporation mechanisms are discussed; a new mathematical model for the charge distribution within a LB film MIS structure is suggested.

8.1 Sample preparation and preliminary experiments

Three MIOS (metal-insulator-oxide-semiconductor) samples were prepared from substrate N6 by depositing multilayer structures of ωTA at different values of subphase pH (pH = 7, 5.3, and 4), and one further device was dipped at a pH of 7 with counterions (Cd^{2+}) in the subphase. This information is summarised in Table 8.1; for full details of sample preparation and film deposition see Appendix B2. It should be noted that SiO_2 surfaces are hydrophilic and so the first layer was deposited upon withdrawal from the subphase, forming odd multiples of monolayers. Initial C-V experiments established that the capacitances of the various insulator regions corresponded to the electrode area and insulator thickness. (The theoretical capacitance was calculated assuming the value of ωTA dielectric constant determined in the preceding chapter , i.e. $\varepsilon_r = 2.82$, and using equations for the double dielectric structure of two serial parallel-plate capacitors [(1)]).

Hysteresis measurements on these devices indicate a very low degree of mobile ionic charge in the structure, as demonstrated in the typical plot (for 31 layers ωTA) of figure 8.1 which displays a lateral shift of only some 90 mV. This is greatly reduced from that observed in figure 7.12 for a ωTA multilayer deposited onto freshly-etched silicon (0.4V lateral shift). Consequently, it seems likely that the high mobile charge concentration in that device is a result of the greater number of impurities and defects which are present at the silicon surface due to the removal of the passivating oxide and which may be a source of additional mobile charge within the structure.

Figures 8.2 to 8.5 show the results of trapped charge measurements as a plot of flat-band voltage, V_{FB}, against number of ωTA multilayers, N, for each of the four devices. Each figure has three curves, corresponding to: a), the V_{FB} readings measured after dipping (before the device was placed in a desiccator to remove trapped water particles); b), after three days of storage

Sample	No. of monolayers	pH	Cd^{2+}	Plotted in :
N6A	0, 1, 3, 7, 13, 19, 25, 31	7.0	x	Fig. 8.2
N6B	0, 1, 3, 7, 13, 19, 25, 31	7.0	✓	Fig. 8.3
N6C	0, 1, 3, 7, 13, 19, 25, 31	5.3	x	Fig. 8.4
N6D	0, 1, 3, 7, 13, 19, 25, 31	4.0	x	Fig. 8.5

Table 8.1 : Summary of dipping parameters for ωTA LB film MIOS samples

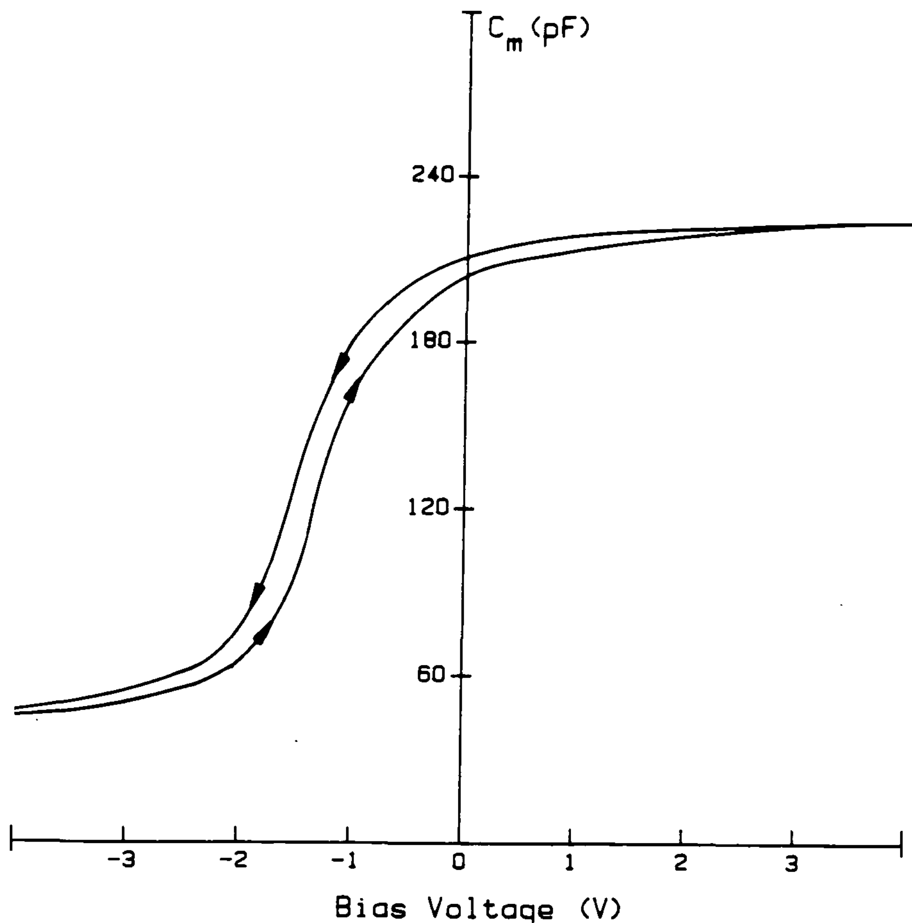


Figure 8.1a : Hysteresis C-V plot for MIOS device at 100 kHz

(31 layers ωTA on 32 nm SiO_2)

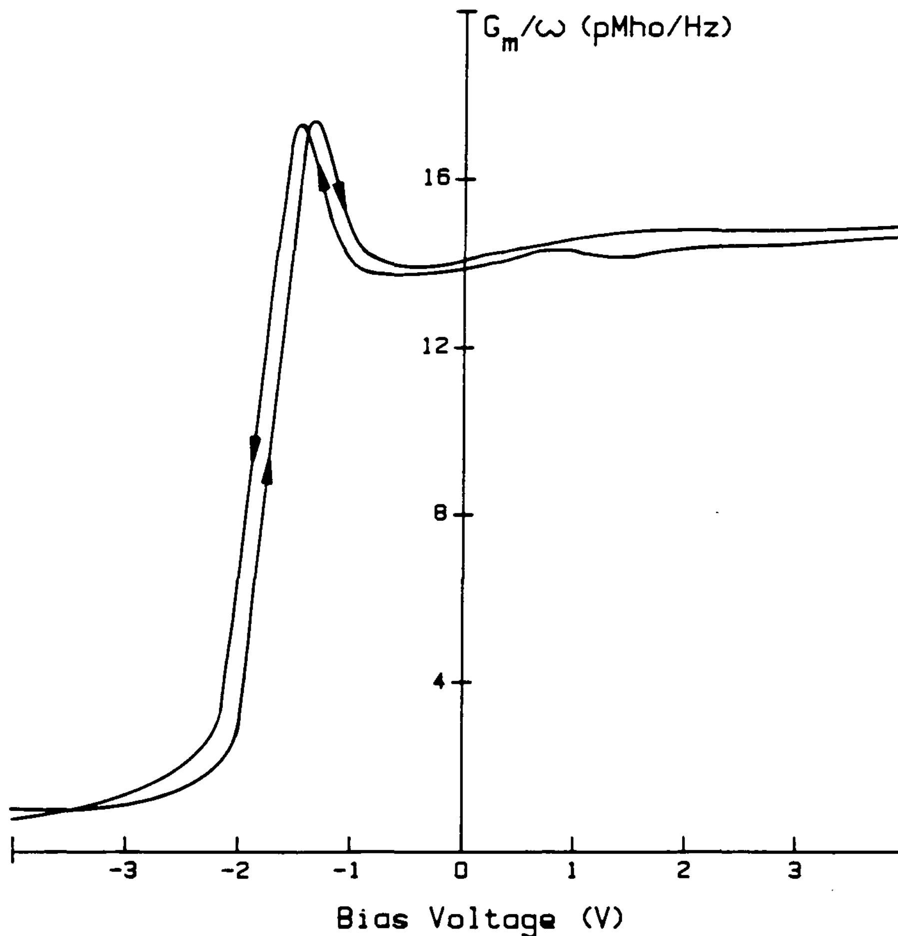


Figure 8.1b : Hysteresis G-V plot for MIOS device at 100 kHz

(31 layers ωTA on 32 nm SiO_2)

in a desiccator in dry N_2; and c), after subsequent exposure to air for five days. Later results recorded after again desiccating the samples, and then after further exposure to air, deviated only very slightly from the data points shown in curves (b) and (c) of figures 8.2 to 8.5.

8.2 Discussion of Experimental Results

From the results plotted in figures 8.2 to 8.5 it can be seen from the changing value of flat-band voltage [2] that there is an apparent charge concentration in the MIS structure when LB films of ωTA are deposited as an additional dielectric layer. This net charge may originate from dipoles incorporated in the LB insulator or from an excess point charge concentration within the structure. It also appears that the amount of effective charge varies with the number of deposited monolayers, and is influenced by the subphase pH and storage conditions. These effects are considered in detail below.

8.2.1 General observations

The polarity and quantity of charge present within the insulating layer of the MIS devices can be assessed approximately from inspection of the V_{FB} curves in figures 8.2 to 8.5. All these plots have the same basic shape : a negative V_{FB} value for the uncoated device and for the first deposited multilayer of ωTA, becoming more positive as more monolayers are accumulated; for each curve, the zero-layer V_{FB} ($V_{FB}(0)$) is approximately the same. This indicates a positive charge concentration within the SiO_2-Si substrate prior to LB film deposition which increases when the first layer is deposited; however, net negative charge is introduced to the system with each subsequent monolayer coated onto the device.

The agreement between the values of V_{FB} for each sample before dipping demonstrates that the positive charge contained in each is approximately equal; this may be attributed to the same amount of fixed charge present in the SiO_2 layer and to trapping states at the SiO_2-Si interface (see chapter 2). From equation 2.22 it is possible to determine the charge density corresponding to this

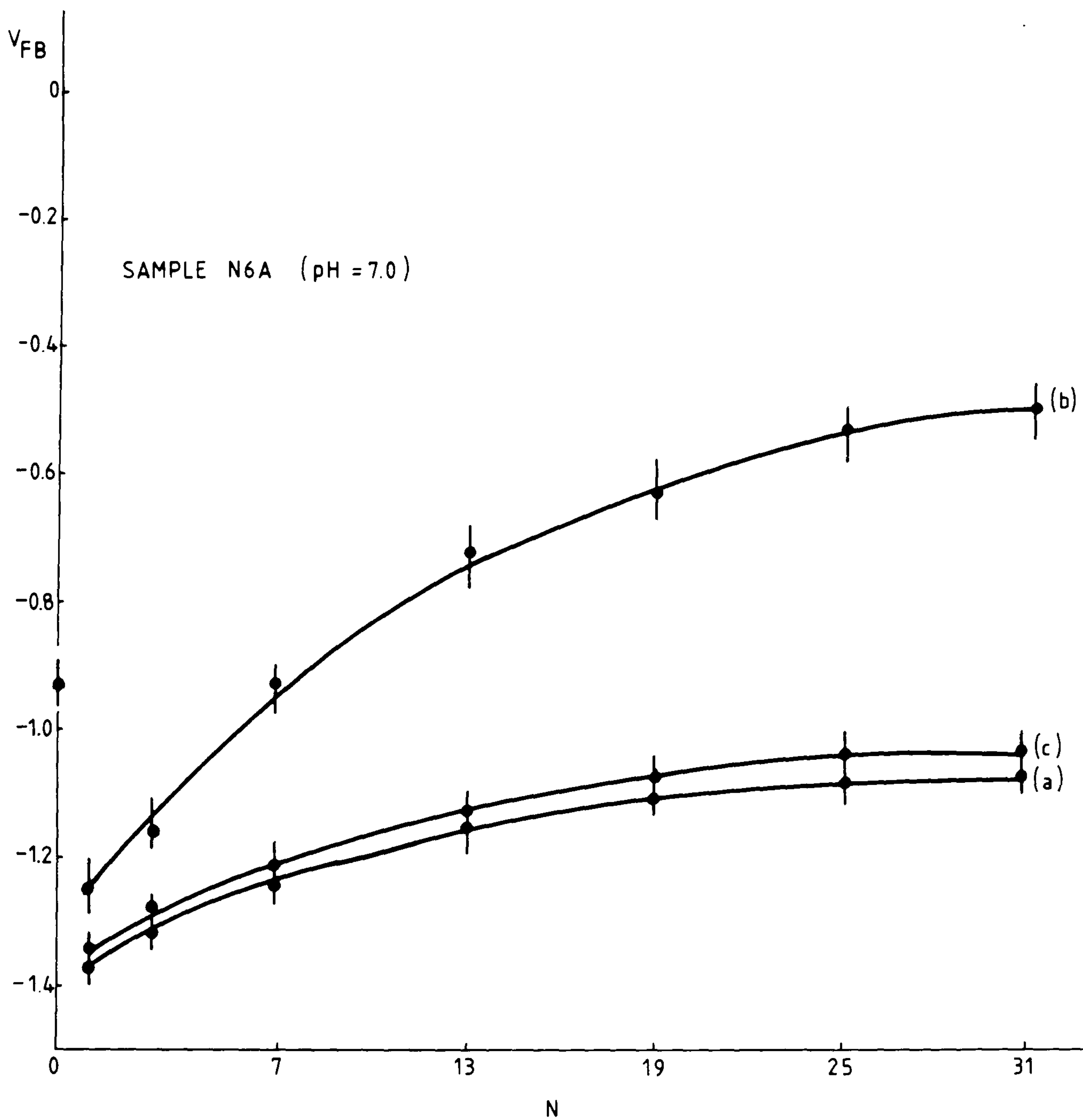


Figure 8.2 : V_{FB} versus N for MIOS device N6A

(a) before desiccation

(b) after desiccation (3 days)

(c) after exposure to air (5 days)

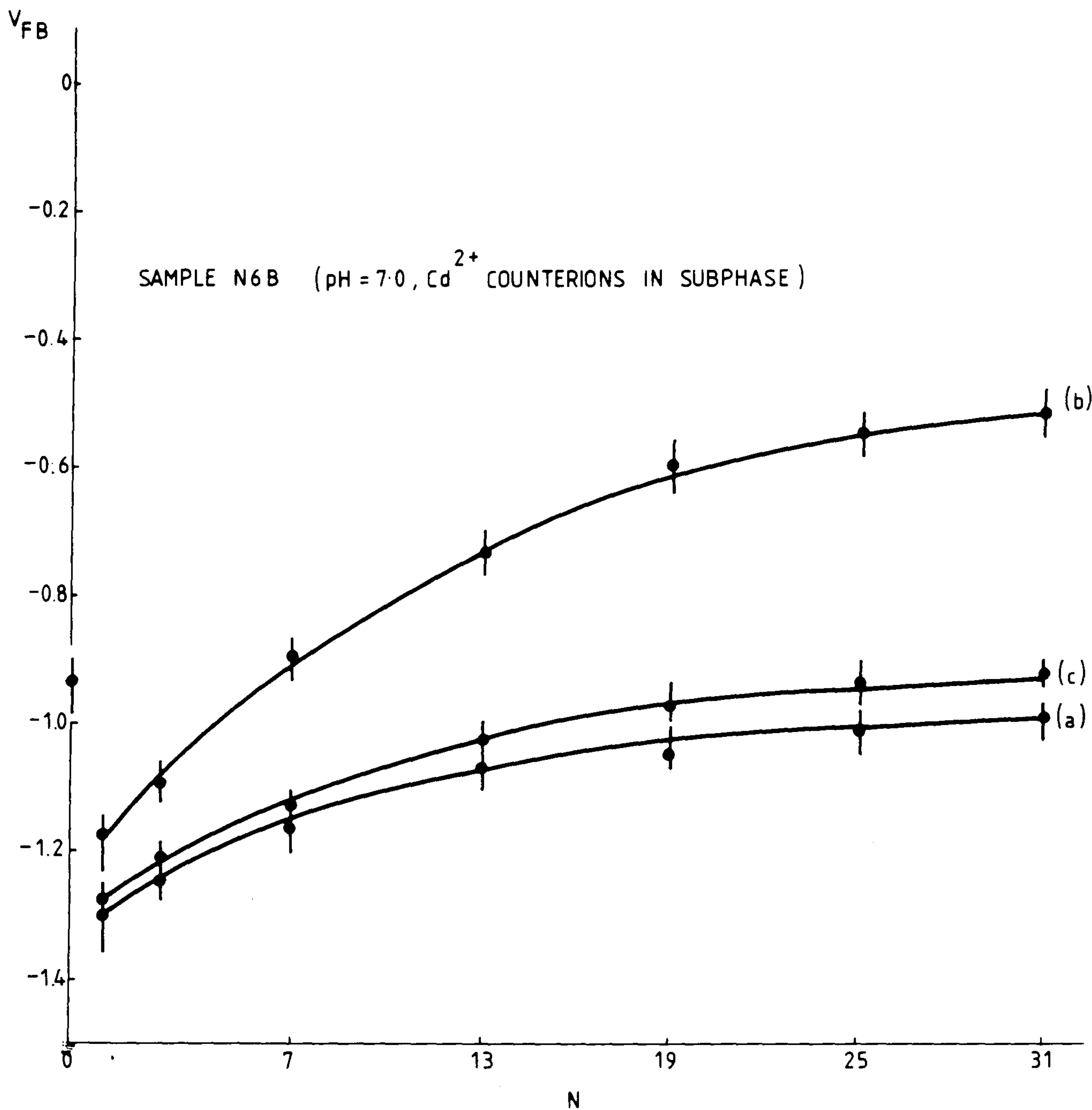


Figure 8.3 : V_{FB} versus N for MIOS device N6B

(a) before desiccation

(b) after desiccation (3 days)

(c) after exposure to air (5 days)

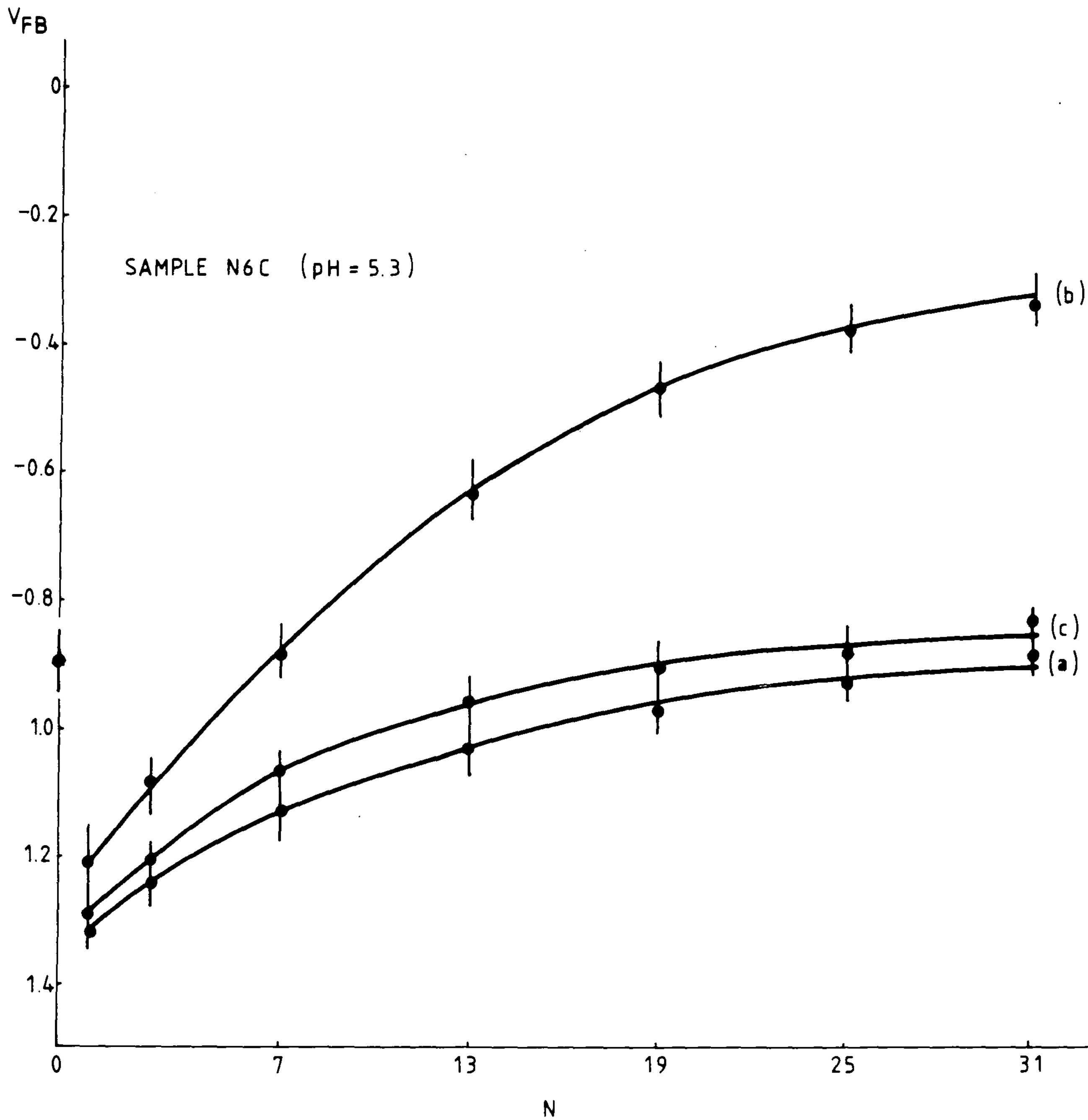


Figure 8.4 : V_{FB} versus N for MIOS device N6C

(a) before desiccation

(b) after desiccation (3 days)

(c) after exposure to air (5 days)

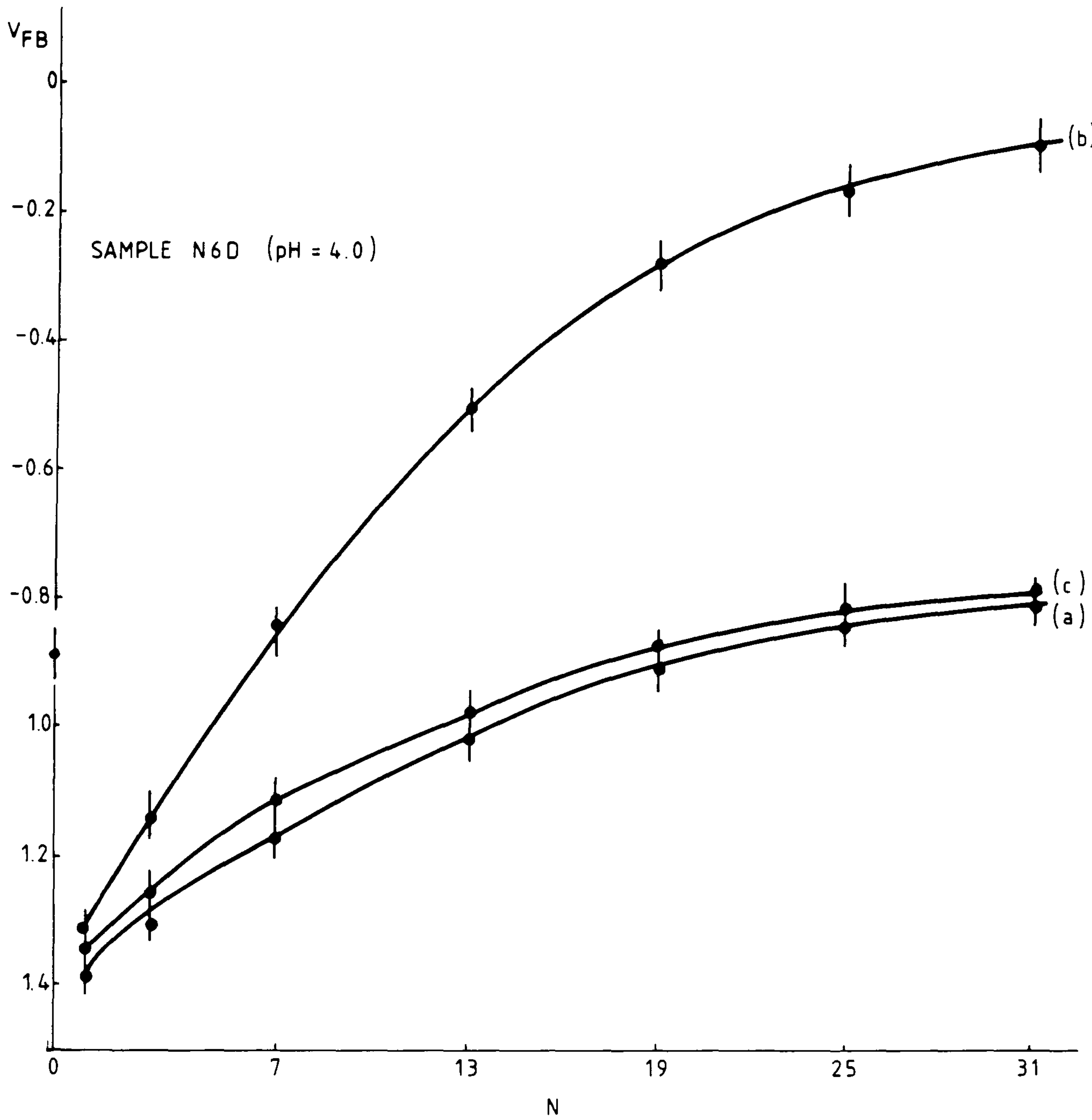


Figure 8.5 : V_{FB} versus N for MIOS device N6D

(a) before desiccation

(b) after desiccation (3 days)

(c) after exposure to air (5 days)

value of V_{FB}; this calculation is performed in section 8.3.2 and gives a density of states of approximately 10^{12} $cm^{-2}eV^{-1}$.

The negative shift in $V_{FB}(1)$, the flat-band voltage with one monolayer of ωTA, denotes a further positive contribution to the charge in the MIS structure. This is most likely due to impurities trapped at the SiO_2 surface by the ωTA coating (the results of section 7.3 have demonstrated the sealing properties of this film); these impurities may have been present at the substrate surface prior to dipping, or may have been picked up from the subphase when the LB monolayer was deposited. However, the value of $V_{FB}(1)$ is not significantly changed by the different dipping conditions employed, which seems to indicate the former interpretation.

In direct contrast to the effect on flat-band voltage of a single monolayer of ωTA, deposition of additional monolayers onto the SiO_2-Si substrate causes a positive shift in V_{FB}, denoting the presence of negative charge within these layers. This may be possibly attributed to the way in which the films are deposited: instead of each O^- ion at the hydrophilic end of the ωTA molecule being bound to an individual H^+ proton when transferred from the subphase to the substrate, as in figure 8.6a, protons may be more loosely attracted to the O^- sites (figure 8.6b). If these protons are not all transferred to the substrate when the LB film is deposited, there will be a net negative charge in this monolayer.

It is also noticeable that the change in V_{FB} is influenced by the storage conditions of the samples after preparation and by the pH of the subphase during the dipping process.

8.2.2 Moisture effects

Each of figures 8.2 to 8.5 shows three sets of V_{FB}-N data as described in section 8.2. For all four devices there is a very large (positive) change in V_{FB} after the removal of water from the

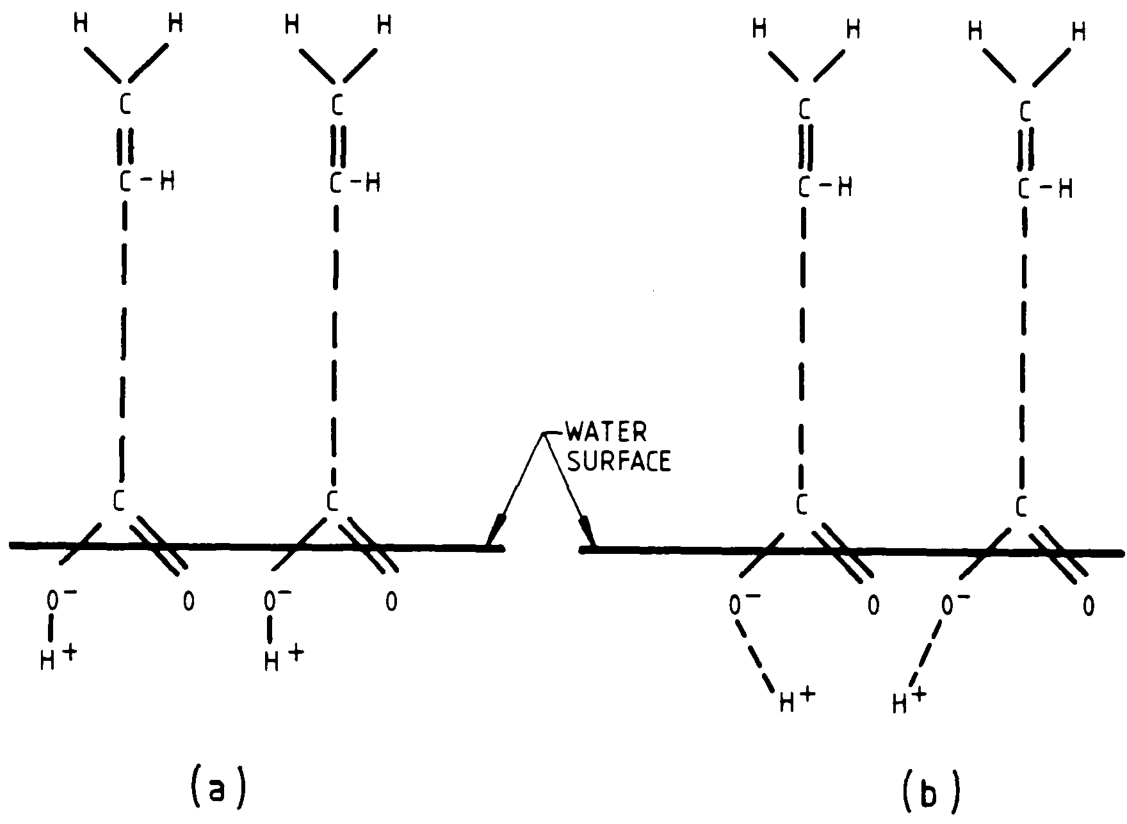


Figure 8.6 : Possible O^- - H^+ configuration for ωTA molecules on water surface

(a) one proton bound to each O^- ion

(b) protons less strongly attracted to O^- sites

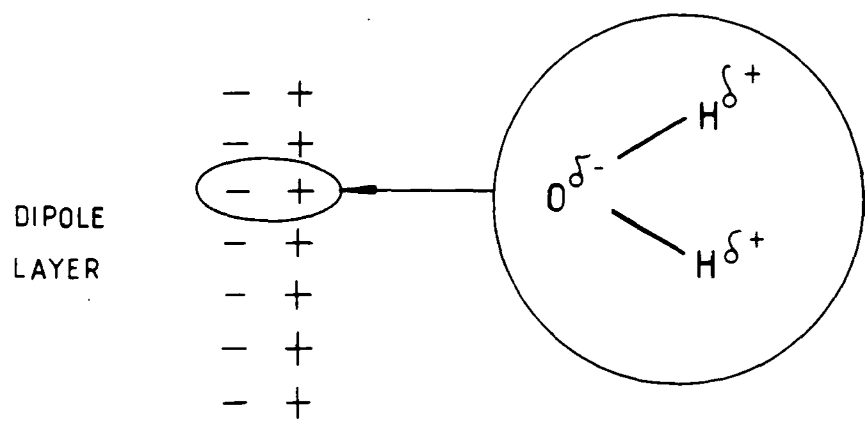


Figure 8.7 : Possible H_2O molecular geometry for dipole layer formation

ωTA film (by storage in a dry nitrogen-filled desiccator) when compared with the value observed after dipping (but before desiccation). Subsequently removing the samples from the water-free environment into normal (moist) air returns the V_{FB}-N curve very nearly to the original position, showing the effect of moisture penetrating back into the structure. These results indicate that the presence of water in the ωTA insulator greatly influences the amount of trapped charge in the film; by removing the water content, there is a large increase in the negative charge in the device which is reversed upon its replacement. (A more quantitative examination is undertaken in section 8.3.2). This suggests that a net positive charge contribution accompanies the incursion of H_2O into the structure, possibly caused by the water molecules orientating so as to form a dipole layer within the insulating film (3), as illustrated in figure 8.7. (It is most likely that these dipole layers will be between the polar groups rather than between the ends of the hydrophobic chains, as there is already a degree of polarisation due to the $H^+ - O^-$ pairing (section 8.2.1).

The undesirable influence of moisture on oxide charge in standard MOS devices has long been recognised (4) and steps are generally taken to reduce this in practice, both in the fabrication stages and in control of storage conditions (by desiccation, or even total encapsulation, of devices). However, the effect of water on LB film monolayers has not been extensively investigated; this is of great importance in the study of insulating structures of these materials since the presence of water is unavoidable due to the deposition method employed (unless an alternative subphase liquid is used).

8.2.3 Influence of subphase pH

Further analysis of the results plotted in figures 8.2 to 8.5 reveals the influence of subphase pH on the charge contained in the insulator. For all three sets of data in each figure (regardless of the amount of moisture in the film) V_{FB} becomes more positive,

denoting an increase in the negative charge density, as the subphase pH is lowered. This is not as would be expected, since a reduction in pH will promote ionization of the carboxylic acid end groups (see figure 8.8), increasing the amount of H^+ in the subphase. These H^+ ions can be solvated (i.e. can couple with hydroxyl groups or water molecules in solution), reducing the number transferred to the substrate during film deposition and resulting in a net negative charge concentration in the LB insulator, as observed above.

8.2.4 Effects of counterions in the subphase

Figures 8.2 and 8.3 show the V_{FB} versus N relationship for two samples coated with monolayers of ωTA at the same subphase pH, with and without Cd^{2+} counterions present. These divalent ions are added to the subphase to facilitate the production of the fatty acid salts of some organic materials; this process is necessary in order to form a compact monolayer which can be transferred to a substrate [5]. By replacing with a single Cd^{2+} ion the protons bound to two adjacent molecules (see figure 8.6a), the attractive forces are stronger and so the film molecules pack more closely together. Although LB films of ω-tricosenoic acid may be compressed and successfully deposited without counterions in the subphase, the experiment was performed to see if any effect on trapped charge was observed when added Cd^{2+} is present during the dipping process. Comparison of the two plots (8.2 and 8.3) shows that there is no appreciable change in the amount of charge incorporated in the insulator as a result of adding counterions, which further supports the theory that any change in trapped charge is due to the amount of water present.

8.2.5 Calculation of charge density

The sets of data plotted in figures 8.2 to 8.5 all exhibit the same general shape: a decrease in flat-band voltage from the initial (negative) value for one monolayer of ωTA, followed by a positive shift for subsequent layers. However, this increase in V_{FB} does not vary linearly with the number of deposited monolayers, as observed by other workers [6]. This

C + H_2O ⇌ C + H_3O^+

O OH O O^-

LOW pH HIGH pH

Figure 8.8 : Influence of subphase pH on degree of ionization of carboxylic acid groups (showing possible mechanism of H^+ solvation)

is because the LB film insulator was deposited onto a SiO_2 layer as opposed to the "bare" semiconductor surface, forming a double dielectric structure. Consequently the simple theory of Hickmott [2], which can be used to gain further information about the charge within the insulator or the dipoles present for single dielectric layers, must be modified in order to quantitatively assess the amount of charge incorporated in the ωTA films deposited onto SiO_2. These calculations are performed in the next section.

8.3 Theoretical model and calculation of trapped charge

The model of Hickmott [2] explains the influence of charge distributed within the SiO_2 layer of a MOS device by approximating the integral of the moments of each individual charge component to a centroid of charge at a fixed position from the metal-SiO_2 surface, as discussed in section 2.2.2 of this thesis. The resulting expression for the flat-band voltage (including surface states at the oxide-semiconductor interface) is given by equation 2.22, which for convenience is reproduced (and renumbered) here:

$$V_{FB} = \phi_{ms} - \frac{\sigma t}{\varepsilon_{ox}} - \frac{\bar{x}Q_o}{d_{ox}C_{ox}} - \frac{Q_{ss}}{C_{ox}} \qquad (8.1.)$$

where the third term represents the centroid of charge present in the oxide as defined in equation 2.15.

For a double dielectric layer, this expression must also take into account any additional charge trapped in the second insulator. The effects of both point charge distribution and dipole charge will be considered in this context.

8.3.1 Modified theory for double dielectric structure

If the integral of the moments of a charge distribution, $\rho(x)$, approximates to a centroid of charge Q at distance d from the metal top electrode of a MIS device, i.e.

$$Qd = \int x\rho(x)\,dx \tag{8.2}$$

then for a number of discrete charges,

$$Qd = (x_1Q_1+x_2Q_2+x_3Q_3+ \ldots) = \sum_{x=1} x_1Q_1 \tag{8.3}$$

Considering a multilayer insulator structure built up in steps of 1,3,5,7, etc. layers, with a charge distribution in each deposited bilayer which may be represented by a charge centroid Q_I at the film-film interface as illustrated in figure 8.9a, the charge moments will vary with the number of layers (which have thickness d):

For 1 layer, moment = Q_1d (8.4a)
(where Q_1 = charge density at film/substrate interface)

For 3 layers, moment $= \sum Qd = Q_1(3d)+Q_I(2d)$ (8.4b)

For 5 layers, moment $= \sum Qd = Q_1(5d)+Q_I(2d+4d)$ (8.4c)

Similarly, for N layers,

$$\text{moment} = \sum Qx = Q_1Nd+Q_I\,\frac{(N^2-1)d}{4} \tag{8.5}$$

If this multilayer insulator is now added to a SiO_2/Si device, then two extra charges are introduced, as shown in figure 8.9b. For N layers of insulator on this substrate,

$$\text{moment} = \sum Qx = Q_{ss}(d_{ox}+Nd)+Q_o(d_o+Nd)+Q_1Nd+Q_I\frac{(N^2-1)d}{4} \tag{8.6}$$

where Q_{ss}=interface state charge, d_{ox} = oxide thickness, Q_o = oxide charge centroid and d_o = position of oxide charge centroid; for carefully prepared MOS capacitors, Q_o can be reduced to zero [(2)] (see section 2.2.2).

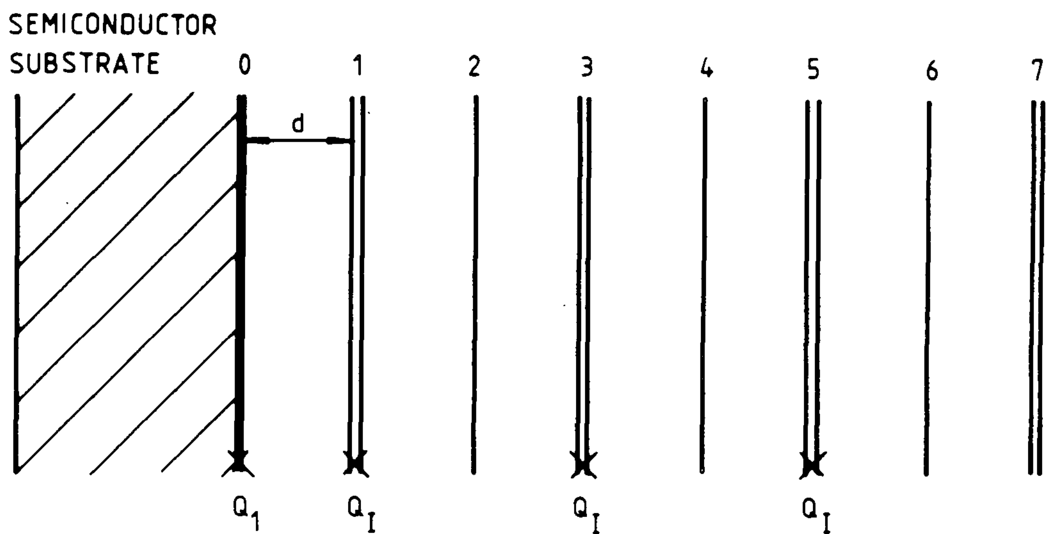


Figure 8.9a : Schematic diagram of charge incorporation in multilayer insulator deposited directly onto hydrophilic semiconductor substrate

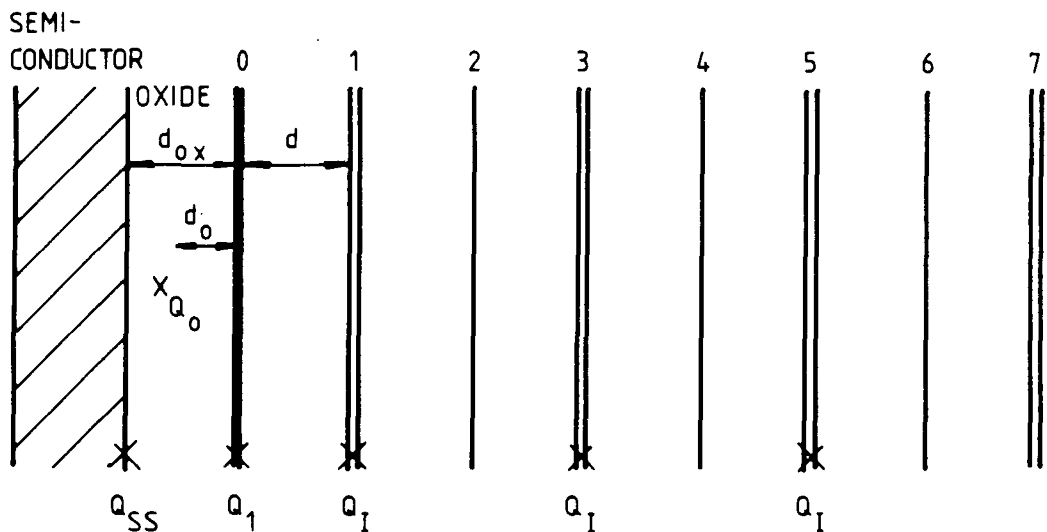


Figure 8.9b: Schematic diagram of charge incorporation in multilayer insulator deposited onto oxide/ semiconductor substrate

As $C = \varepsilon_o \varepsilon_r / x$ for unit area (from equation 3.6), the change in V_{FB} due to the charge represented in 8.6 will be (for N layers):

$$\Delta V_{FB} = -\frac{1}{\varepsilon_o} \sum \frac{Q_x}{\varepsilon_r}$$

$$= -\frac{1}{\varepsilon_o} \left\{ \frac{Q_{ss} d_{ox}}{\varepsilon_r(ox)} + \frac{d}{\varepsilon_r(ins)} \left[N(Q_{ss} + Q_1) + Q_I \frac{(N^2-1)}{4} \right] \right\} \tag{8.7}$$

Here, $\varepsilon_r(ox)$ and $\varepsilon_r(ins)$ are the relative permittivities of the oxide and insulator materials respectively.

Allowing for the presence of dipoles within each monolayer and substituting the term from equation 8.7 into the expression for flat-band voltage (8.1),

$$V_{FB} = \left(\phi_{ms} - \frac{\sigma_t}{\varepsilon_o \varepsilon_{r(ox)}} - \frac{N \sigma_1 t_1}{\varepsilon_o \varepsilon_{r(ins)}} - \frac{Q_{ss} d_{ox}}{\varepsilon_o \varepsilon_{r(ox)}} \right) - \frac{d}{\varepsilon_o \varepsilon_{r(ins)}} \left[N(Q_{ss} + Q_1) + Q_I \frac{(N^2-1)}{4} \right] \tag{8.8}$$

where $\sigma_1 t_1 / \varepsilon_o \varepsilon_{r(ins)}$ represents the dipole layers at the polar interface of the LB insulator. It should be noted that this expression is only valid for odd values of N greater than zero due to the way in which the insulator is built up (when N = 0 the second term vanishes, and there are no dipole layers as there is no additional insulator).

From the expression derived above for the flat-band voltage of a multilayer MIOS structure (equation 8.8) it should be possible to establish the nature of the charge incorporated in the LB insulator. If this is due to dipole layers in the structure, then the second term in equation 8.8 vanishes and there is a linear relationship between V_{FB} and number of layers N (i.e. a plot of V_{FB} versus N should give a straight line). However, if there is a point charge concentration in each LB bilayer,

the second term remains and the relationship is difficult to verify from a plot of V_{FB} versus N because of its non-linear dependence. This problem may be overcome by differentiating the expression with respect to N, which yields

$$\frac{dV_{FB}}{dN} = \frac{-d}{\varepsilon_o \varepsilon_{r(ins)}} \quad (Q_{ss} + Q_1) \quad + \frac{N}{2} Q_I \tag{8.9}$$

If the model is correct, a plot of dV_{FB}/dN against N should give a straight line of

$$\text{slope} = -\frac{dQ_I}{2\varepsilon_o \varepsilon_{r(ins)}} \tag{8.10}$$

In addition, the amount of charge present in interface states, Q_{ss} (and hence the surface state density, N_{ss}), may be calculated by rewriting equation 8.8 for zero LB film layers (i.e. N = 0):

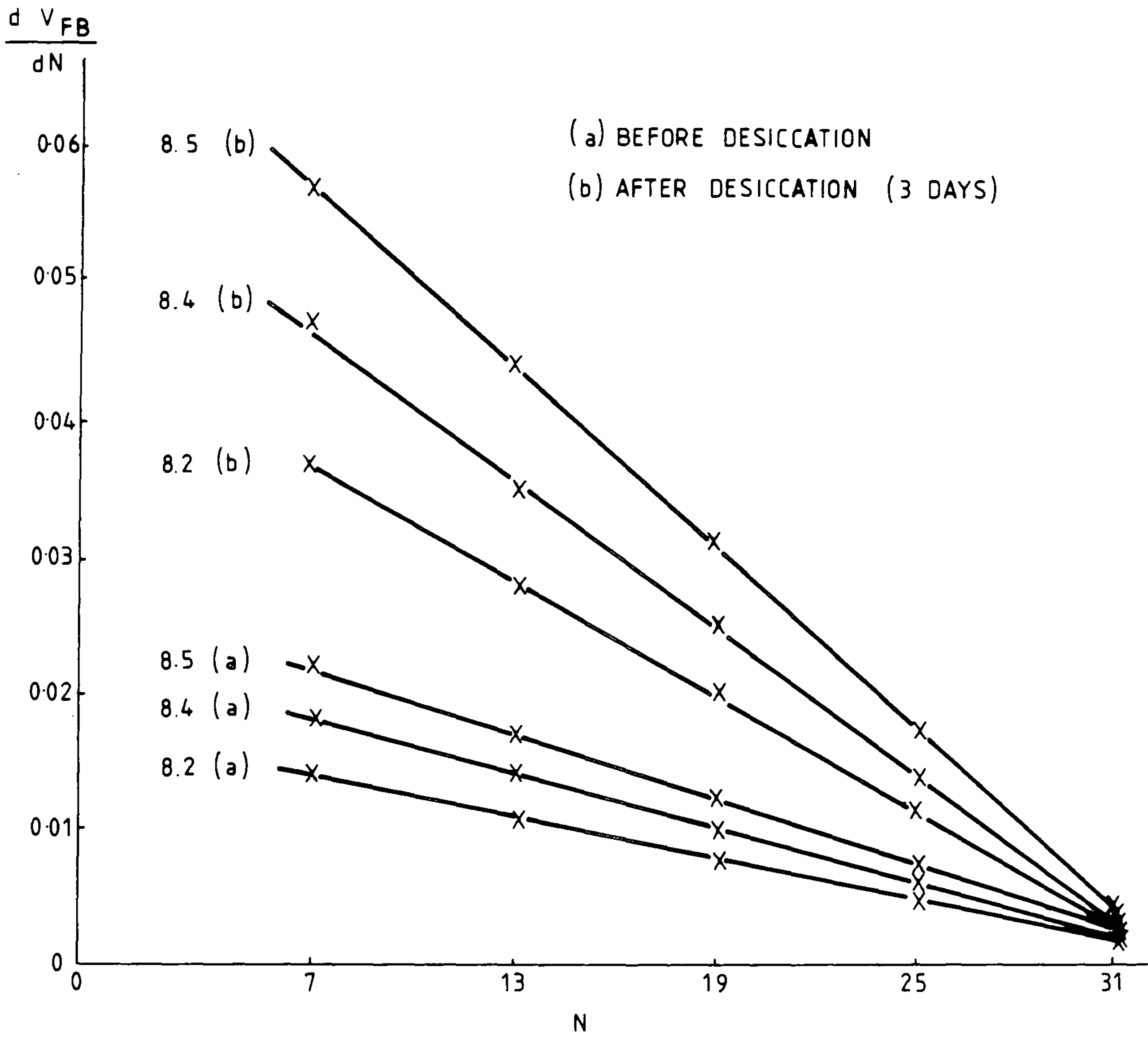
$$V_{FB(0)} = \phi_{ms} - \frac{Q_{ss} d_{ox}}{\varepsilon_o \varepsilon_{r(ox)}} \tag{8.11}$$

where $Q_{ss} = qN_{ss}$ (8.12)
(assuming monovalent charge for each state).

By comparing this N_{ss} value with that extracted from admittance measurements on the MOS structure (no LB film), as discussed in chapters 3 and 4, further evidence as to the validity of the model may be obtained.

8.3.2 Calculations and Results

From the curves plotted in figures 8.2 to 8.5 it is clear that there is not a linear relationship between V_{FB} and N, and so the change in V_{FB} is not satisfactorily explained by dipole effects. In order to follow up the point charge approach outlined above, the values of dV_{FB}/dN measured from the curves plotted in figures 8.2, 8.4 and 8.5 (a and b) are recorded in figure 8.10 as a



8.2 : SAMPLE N6A
8.4 : SAMPLE N6C
8.5 : SAMPLE N6D

Figure 8.10 : Plot of dV_{FB}/dN versus N for data of figures 8.2, 8.4 and 8.5 (curves a and b)

function of N. In each case, a good straight-line fit is obtained, which proves that the relationship between V_{FB} and N is influenced by a charge concentration in each LB bilayer and is of the form predicted by equation 8.8.

Furthermore, there is very close agreement between the value of N_{ss} determined by the conductance technique and that obtained from equation 8.11. From the value of $V_{FB}(0)$ observed from figures 8.2 to 8.5 ($\sim$0.9V), and with $\varepsilon_r(SiO_2) = 3.7$, d_{ox} = 32nm and ϕ_{ms} $\sim$0.72 (Al/Au top contacts), a figure for Q_{ss} of $\sim 1.66 \times 10^{-3} m^{-2}$ is obtained (positive charge). This corresponds to a surface state density of $\sim 1.04 \times 10^{16} m^{-2} eV^{-1}$ (i.e. $N_{ss} \sim 1.04 \times 10^{12} cm^{-2} eV^{-1}$), and is consistent with the figure calculated from a.c. admittance measurements taken at a bias voltage of -0.9V ($\sim V_{FB}(0)$), which indicated a value of $N_{ss} \sim 9.3 \times 10^{11} cm^{-2} eV^{-1}$. This result reinforces the credibility of the proposed model.

Referring to equation 8.10, the amount of charge present in each deposited bilayer may be calculated from the slope of the straight lines in figure 8.10. The equivalent charge density is tabulated in table 8.2 to demonstrate the effects of external influences such as subphase pH and the amount of moisture in the LB film. The value of $\varepsilon_{r(ins)}$ for these calculations was taken as 2.82, and the film monolayer thickness, d, was assumed to be 3 nm (see chapter 7). It is interesting to note that for all three samples the removal of moisture increases the negative charge density by a factor of approximately 2.7, although there is no apparent reason to suggest that this agreement is anything other than coincidental. In each case the density of charges trapped in the bilayer lies between $5.5 \times 10^9 cm^{-2} eV^{-1}$ and $22.6 \times 10^9 cm^{-2} eV^{-1}$, much less than the surface state density observed in the devices (~ 6-$9 \times 10^{12} cm^{-2} eV^{-1}$) which remains the dominant factor in determining the value of flat-band voltage; however, when a number of bilayers are deposited onto the substrate, the negative charge introduced will become significant in influencing V_{FB}.

pH	Q_I before desiccation	Q_I after desiccation (3 days)
7.0	(-) 5.5×10^9 $cm^{-2}eV^{-1}$	(-) 14.2×10^9 $cm^{-2}eV^{-1}$
5.3	(-) 7.3×10^9 $cm^{-2}eV^{-1}$	(-) 19.8×10^9 $cm^{-2}eV^{-1}$
4.0	(-) 8.4×10^9 $cm^{-2}eV^{-1}$	(-) 22.6×10^9 $cm^{-2}eV^{-1}$

Table 8.2 : Variation of Q_I with pH and degree of moisture content

8.4 Summary and Suggestions for further work

The work reported in this chapter is significant in that it demonstrates the many parameters which may influence the amount of trapped charge within multilayer films deposited by the LB technique; this has not previously been investigated. It has been shown for LB films of ω-tricosenoic acid that the dipping conditions are very important in determining the electrical properties of MIS devices fabricated with these organic multilayers as insulator. A model for the incorporation of charge in the LB film insulator has been propounded and the electrical effects on MIS device properties quantified; the possible physical origins of this charge have also been examined.

Additional research into the electrical properties of LB film insulators is necessary to determine the precise nature of the charge incorporated in these structures. It is also desirable to investigate more fully the influences on, and the mechanisms involved in altering, the charge density, and the possible uses of these phenomena. For example, a wider variation of subphase pH, combined with different organic materials and control of the moisture content of the film, may perhaps enable the flat-band voltage of a MIS device to be altered; this has potential applications in "tailoring" of devices to offset the V_{FB} shift due to interface states and oxide trapped charge, or even for adjusting the "turn-on" voltage of MIS switches.

There is obviously much more still to be learnt about the dipping process before devices incorporating organic multilayers can be produced with the degree of reproducibility required for commercial exploitation of the LB technique, but the number of advantages in many fields offered by the technology [7,8] make it worthy of further investigation.

CHAPTER 9: CONCLUSIONS

In this work, the response of various gas-sensitive metal-insulator-semiconductor devices has been investigated. In order to analyse the electrical properties of these MIS capacitors, an automated instrumentation system has been developed to measure their admittance characteristics. The associated microcomputer controls data acquisition and processing by means of software programs designed for this purpose. This system enables accurate determination of the density of energy states at the insulator-semiconductor interface by the a.c. conductance technique. The conventional procedure of gathering admittance data over the full range of signal frequencies and bias voltages produces a large amount of redundant information. This problem has been overcome by operating in a scanned-frequency mode, in which the microcomputer automatically recalibrates the instrumentation at each new signal frequency, thus greatly simplifying the measurement operation. In this way, rapid surface state analysis is possible, which may be of importance in the semiconductor industry for quality and process control where fast sample evaluation is desirable.

This system has been used to analyse the effects of different gas ambients on MIS structures. The investigation has concentrated on the palladium/silicon dioxide/silicon device because of the controversy over the role of surface states in the hydrogen response. It has been shown that there is a definite change in surface state distribution when thin ($\sim$12 nm) oxide samples are exposed to hydrogen gas; however, no change is observed for thick ($\sim$100 nm) oxide devices. This phenomenon has been attributed to surface traps at, or very close to, the SiO_2/Si interface which may be effectively removed by a low-temperature annealing process, producing MOS structures which no longer exhibit H_2-induced surface state density changes.

In an effort to increase the device sensitivity to hydrogen, organic multilayers of ω-tricosenoic acid have been deposited by the Langmuir-Blodgett technique onto a freshly-etched silicon

substrate before evaporation of the Pd top electrodes. This structure exhibited a larger surface state density distribution (due to the increased number of unpaired bonds at the semiconductor interface); although full surface state evaluation was not possible because of the non-ideal electrical properties of the LB film, the admittance experiments performed on these samples indicated a much larger surface state response to hydrogen gas.

The electrical characteristics of ω-tricosenoic acid LB films were measured, and the influences and effects of moisture, sample preparation process and storage conditions on these properties have been examined. In addition, work has been carried out on the development of an automated Langmuir trough.

The use of LB films for specialised sensor applications is very attractive owing to the unique properties of the organic materials employed. Most LB films are good insulators and are therefore suitable for use in field-effect semiconductor devices. Such a solid-state sensor for gas detection has been examined in this work, and other sensitive and selective transducers based on various LB film insulator and inorganic semiconductor combinations are anticipated. Furthermore, the interesting optical, physical and acoustical properties of some organic materials suggest the exploitation of these phenomena as sensing mechanisms, and the use of LB films as a means of incorporating specially-substituted molecules into field-effect devices points the way towards detection of specific biological species. However, it is likely that different device structures (e.g. field-effect transistors, surface acoustic wave devices) will be better suited to detection of these properties than the simple MIS capacitor, and investigation of these alternative configurations is desirable. In addition, there is a need for further examination of the electronic circuitry required to interface the basic sensor to a practical measurement system; if this can be accomplished in a relatively simple, cost-effective manner, there are many possible uses of these sensors in such areas as, for example, environmental monitoring and industrial process control.

For all these potential applications, the degree of control over the deposited monolayer afforded by the Langmuir-Blodgett technique is of utmost importance. However, as indicated by the studies performed in this work a considerable amount of research is still required into the stability of these films, and the external influences upon their properties, in order to determine the best materials for the fabrication of practical sensing devices.

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APPENDIX A : PROGRAM LISTINGS

PROGRAM 'VSCAN'

```
10 ! FREQ FIXED, VOLTAGE SCANNED
20 RESET 7 @ SET TIMEOUT 7;5000
30 OUTPUT 707 ; "RA" @ OUTPUT 707 ; 0 ! SENDS ZERO VOLTS
40 OUTPUT 709 ; "B123456" ! ALL RELAYS OFF
50 DIM A(100), G(500), C(500), V(500), C$[50]
60 C$="W 0;C 10" @ GOSUB 9000 ! SETS LINEFEED AS DELIMITER
70 G6=-1000 ! INITIALISES THE PEAK Gp/w VALUE
99 ! INITIALISE SYSTEM BEFORE TAKING READINGS
100 CLEAR @ DISP "FIXED FREQ, VOLTAGE SCAN MODE" @ DISP @ DISP "RESET LOCK-IN BY DEPRESSING BOTH"
110 DISP "'SELECT' AND 'SENSITIVITY' KEYS" @ DISP "AND PRESS CONT" @ PAUSE ! INITIALISES LOCK-IN
120 CLEAR @ DISP "FREQUENCY: 0.1 TO 100,000 Hz"; @ INPUT F@ W=2*PI*F @ GOSUB 8300
130 DISP @ DISP "ACCUMULATION VOLTS: -10 TO +10 V"; @ INPUT V0
140 DISP @ DISP "TIME IN ACCUMULATION (sec)"; @ INPUT T0@ T0=T0*1000
150 CLEAR @ DISP "INITIAL VOLTAGE"; @ INPUT V1
160 DISP @ DISP "FINAL VOLTAGE"; @ INPUT V2
170 CLEAR @ DISP "STEP SIZE (mV)"; @ INPUT V3@ V3=V3/1000
180 DISP @ DISP "TIME BETWEEN READINGS (sec)"; @ INPUT T1@ T1=T1*1000
190 CLEAR @ DISP "CH 1 x10 EXPAND ON OR OFF (1/0)"; @ INPUT X
200 DISP @ DISP "CALIBRATION CAPACITANCE (pF)"; @ INPUT C5
210 DISP @ DISP "CALCULATE Gp/w PEAK (Y/N)"; @ INPUT X$@ IF UPC$(X$[1,1])="Y" THEN P7=1 ELSE P7=0
220 N=10+ABS(V2-V1)/V3
230 DISP @ DISP "PRINT OUTPUT (Y/N)"; @ INPUT X$@ IF UPC$(X$[1,1])="Y" THEN P8=1 ELSE P8=0
240 IF P8=1 THEN CLEAR @ DISP "ENTER DETAILS"; @ INPUT N$@ PRINT N$ @ PRINT "Gm, Cm vs. V at";F;"Hz" @ PRINT
250 DISP @ DISP "STORE READINGS ON TAPE (Y/N)"; @ INPUT X$@ IF UPC$(X$[1,1])="Y" THEN P6=1 ELSE P6=0
255 IF P6=1 THEN GOSUB 9500
260 C$="J 100,1;R 2;F 1;T 6,1;A2 1" @ GOSUB 9000 ! RUNS AUTOSET ON CAL CAP AT 1kHz
270 C$="Z" @ GOSUB 9000 ! SCAN STATUS BYTE UNTIL SETTLED
280 IF BIT(A(1),5)=0 THEN 270
290 C$="J "&VAL$(F1)&","&VAL$(F2) @ GOSUB 9000 ! SET FREQ
300 C$="F "&VAL$(F3) @ GOSUB 9000 ! SET F BAND
310 CLEAR @ DISP "FREQ";F;"Hz SELECTED" @ DISP "SET UP TC AND dB/OCT: PRESS CONT" @ PAUSE
320 DISP @ DISP "TC= (sec)"; @ INPUT T
330 DISP @ DISP "dB/OCT= (6/12)"; @ INPUT T6@ T=T6*1000*T ! SETS TC DELAY
340 IF T1>T THEN T=T1
350 IF T>T0 THEN T0=T ! SELECTS LONGER DELAY TIME
360 C$="A2 1" @ GOSUB 9000 ! RUNS AUTOSET ON CAL CAP AT FREQ F
370 C$="Z" @ GOSUB 9000 ! CHECK FOR SETTLED STATUS BYTE
380 IF BIT(A(1),5)=0 THEN 370
400 ! READ AND CALIBRATE CHANNEL 1
410 C$="W 1" @ GOSUB 9000 ! SENDS LOCAL LOCKOUT
420 WAIT T
430 C$="Q1" @ GOSUB 9000
440 P1=C5*W/A(1) @ IF X=1 THEN P1=P1/10 ! ALLOWS FOR x10 EXPAND
450 C$="K 1;K 4;K 4;K 12" @ GOSUB 9000 ! PHASE SHIFT (-{/2)
460 C$="X "&VAL$(X) @ GOSUB 9000 ! SENDS x10 EXPAND IF REQUIRED
470 WAIT T
500 ! READ AND CALIBRATE CHANNEL 2
510 C$="Q2" @ GOSUB 9000
520 P2=C5/A(1)
550 ! SELECT SAMPLE AND SEND ACC VOLTAGE (V0)
560 GOSUB 9900
570 OUTPUT 709 ; "A6" ! ACTIVATES RELAY 6 (SAMPLE IN)
600 V=V0 @ OUTPUT 707 ; V
610 WAIT T0
620 I=0 @ GOSUB 8500
640 ! NEED TO SWOP VOLTAGE RAMP LIMITS?
650 IF V1>V2 THEN GOSUB 8600 ELSE GOSUB 8700
750 ! FINAL DISPLAYS, ETC.
760 OUTPUT 709 ; "B6" ! SWITCH OUT SAMPLE
770 C$="X 0;K 1;K 4;K 4;K 13;W 0" @ GOSUB 9000
790 OUTPUT 707 ; 0 ! SENDS ZERO VOLTS
800 CLEAR @ DISP "EXECUTION TERMINATED"
```

```
810 IF P6=1 THEN GOSUB 9550 ! TAPE STORAGE
820 IF P7=0 THEN 1000
830 CLEAR @ DISP "Gp/w PEAK INFORMATION: "
840 DISP @ DISP "Peak Gp/w value=" @ DISP G6; "pMho/Hz"
850 DISP "At Gp/w peak, Cp=" @ DISP C6; "pF"
860 DISP "Peak Voltage   =";V6; "Volts"
870 DISP @ DISP "Rs =";R0; "" @ DISP "Cox=";C0*1.E12; "pF"
1000 DISP @ DISP "END" @ END
7500 ! OUTPUT TO INTERNAL PRINTER
7510 PRINT G(I); "pMho" @ PRINT C(I); "pF" @ PRINT V; "Volts" @ PRINT
7520 RETURN
8300 ! FREQUENCY SET-UP
8305 IF F=100000 THEN F1=1000 @ F2=0 @ GOTO 8320
8310 F6=INT(LGT(F)) @ F2=4-F6 @ F9=10^(F6-2) @ F1=INT((F+.0001)/F9) @ F=F1*F9
8320 DISP "FREQ SET TO";F; "Hz"
8330 IF F2=2 THEN F3=1 ELSE F3=F2
8340 IF F2>2 THEN F3=2
8350 RETURN
8500 ! READ CH1 AND CH2
8510 C$="Q1;Q2" @ GOSUB 9000
8520 G(I)=A(1)*P1 @ C(I)=A(2)*P2 @ V(I)=V ! STORES G, C, &V IN ARRAYS
8530 G=G(I)*.000000000001 @ C=C(I)*.000000000001
8535 IF P8=1 THEN GOSUB 7500
8540 IF P7=0 THEN 8560
8550 IF I=0 THEN GOSUB 9600 ELSE GOSUB 9700
8560 RETURN
8600 ! SWOPS VOLTAGE RAMP LIMITS AND CALLS OUTPUT ROUTINE
8610 FOR V4=V2 TO V1 STEP V3
8620 V=V2+(V1-V4) @ GOSUB 8800
8630 NEXT V4
8640 G(I)=-999 ! SIGNIFIES END OF DATA
8650 RETURN
8700 ! CALLS OUTPUT ROUTINE (NO SWOP OF VOLTAGE LIMITS)
8710 FOR V=V1 TO V2 STEP V3
8720 GOSUB 8800
8730 NEXT V
8740 G(I)=-999 ! END OF DATA
8750 RETURN
8800 ! CALLS VOLTAGE OUTPUT ROUTINE AND READING ROUTINE
8810 OUTPUT 707 ;V
8820 I=I+1 @ IF I=1 THEN WAIT T0 ELSE WAIT T
8830 GOSUB 8500
8840 RETURN
9000 ! I/O ROUTINE FOR LOCK-IN
9010 GOSUB 9200 ! DO SERIAL POLL
9020 IF BIT(S9,0)=0 THEN 9010 ! WAIT FOR PREVIOUS COMMAND DONE
9030 OUTPUT 706 USING "K" ; C$
9040 I9=0
9050 GOSUB 9200 ! DO SERIAL POLL
9060 IF BIT(S9,7)=0 THEN 9080 ! CHECK FOR OUTPUT READY
9070 I9=I9+1 @ ENTER 706 ; A(I9)
9080 IF BIT(S9,0)=0 THEN 9050 ! CHECK FOR COMMAND DONE
9090 RETURN
9200 ! SERIAL POLL ROUTINE
9210 S9=SPOLL(706)
9220 RETURN
9300 ! TEMPORARY PAUSE ROUTINE
9310 BEEP @ BEEP @ CLEAR @ DISP "TEMPORARY PAUSE IN EXECUTION"
9320 DISP @ DISP "PRESS CONT TO CONTINUE"
9330 C$="W 0" @ PAUSE ! UNLOCKS FRONT PANEL AND PAUSES PROGRAM
9340 C$="W 1" ! RELOCKS FRONT PANEL
9350 GOSUB 9900
9360 RETURN
```

```
9500 ! TAPE FILE CREATION
9510 CLEAR @ DISP "INSERT DATA TAPE AND PRESS CONT" @ PAUSE
9520 DISP @ DISP "FILENAME"; @ INPUT X$
9530 CREATE X$, N, 24 @ ASSIGN# 1 TO X$
9540 DISP @ DISP X$; " CREATED" @ PRINT# 1 ; X$, F
9545 RETURN
9550 FOR I=0 TO N
9560 IF G(I)=-999 THEN PRINT# 1 ; G(I) @ GOTO 9590
9570 PRINT# 1 ; G(I), C(I), V(I)
9580 NEXT I
9590 RETURN
9600 ! CALCULATE Rs, Cox FROM G(0), C(0)
9610 R0=G/(G^2+W^2*C^2)
9620 IF R0<0 THEN R0=0
9630 C0=C*(1+G^2/(W^2*C^2))
9640 RETURN
9700 ! CALCULATE Gp/w AND Cp
9710 D=(W^2*C0*R0*C-G)^2+W^2*(C0-C-C0*R0*G)^2
9720 G1=W*C0^2*(G-W^2*C^2*R0-R0*G^2)*1.E12/D ! SGp/w in pMho/Hz (pF)
9730 IF G1<G6 THEN 9750
9740 G6=G1 @ V8=V @ C8=(W^2*C0*C*(C0-C)-C0*G^2)*1.E12/D ! SCp in pF
9750 RETURN
9900 CLEAR @ DISP "SAMPLE SWITCHED IN" @ BEEP
9910 DISP @ DISP "TO STOP EXECUTION TEMPORARILY" @ DISP "PRESS KEY k1" @ ON KEY# 1, "STOP" GOSUB 9300 @ KEY LABEL
9920 RETURN
```

PROGRAM 'FSCAN'

```
10 ! FREQ SCANNED, VOLTAGE FIXED
20 RESET 7 @ SET TIMEOUT 7;5000
30 OUTPUT 707 ;"RA" @ OUTPUT 707 ;0 ! SENDS ZERO VOLTS
40 OUTPUT 709 ;"B123456" ! ALL RELAYS OFF
50 DIM A(100),G(500),C(500),F(500),C$[50],N$[50]
60 C$="W 0;C 10" @ GOSUB 9000 ! SETS LINEFEED AS DELIMITER
70 G6=-1000 ! INITIALISES THE PEAK Gp/w VALUE
80 T(0)=100 @ T(1)=30 @ T(2)=10 @ T(3)=3 @ T(4)=1 @ T(5)=.3 @ T(6)=.1
99 ! INITIALISE SYSTEM BEFORE TAKING READINGS
100 CLEAR @ DISP "FIXED VOLTAGE, FREQ SCAN MODE" @ DISP @ DISP "RESET LOCK-IN BY DEPRESSING BOTH"
110 DISP "'SELECT' AND 'SENSITIVITY' KEYS, " @ DISP "SET PSU KEY-SWITCH TO 'REMOTE'"
115 DISP "AND PRESS CONT" @ PAUSE
120 CLEAR @ DISP "LOW FREQ LIMIT : 0.1 Hz min";@ INPUT F1
130 DISP @ DISP "HIGH FREQ LIMIT : 100,000 Hz max";@ INPUT F2@ IF F2<F1 THEN 120
140 DISP @ DISP "NO. OF FREQUENCY STEPS";@ INPUT N1
150 DISP @ DISP "LINEAR OR LOG. INTERVALS (1/0)";@ INPUT L6
155 DISP @ DISP "dB/OCT= (6/12)";@ INPUT T6@ IF T6=6 THEN T6$="1" ELSE T6$="0"
160 CLEAR @ DISP "ACCUMULATION VOLTS: -10 TO +10 V";@ INPUT V0
170 DISP @ DISP "TIME IN ACCUMULATION (sec)";@ INPUT T0@ T0=T0*1000
180 CLEAR @ DISP "VOLTAGE VALUE";@ INPUT V
190 DISP @ DISP "TIME BETWEEN READINGS (sec)";@ INPUT T1@ T1=T1*1000
200 CLEAR @ DISP "CH 1 x10 EXPAND ON OR OFF (1/0)";@ INPUT X
210 DISP @ DISP "CALIBRATION CAPACITANCE (pF)";@ INPUT C5
220 DISP @ DISP "CALCULATE Gp/w PEAK (Y/N)";@ INPUT X$@ IF UPC$(X$[1,1])="Y" THEN P7=1 ELSE P7=0
240 DISP @ DISP "PRINT OUTPUT (Y/N)";@ INPUT X$@ IF UPC$(X$[1,1])="Y" THEN P8=1 ELSE P8=0
245 IF P8=0 THEN 255
250 CLEAR @ DISP "ENTER DETAILS";@ INPUT N$@ PRINT N$ @ PRINT @ PRINT "Gp/w,Cp vs. F at";V;"Volts" @ PRINT
255 DISP @ DISP "STORE READINGS ON TAPE (Y/N)";@ INPUT X$@ IF UPC$(X$[1,1])="Y" THEN P6=1 ELSE P6=0
256 IF P6=1 THEN GOSUB 9500
260 C$="J 100,1;R 2;F 1;T 6,1;A2 1" @ GOSUB 9000 ! RUNS AUTOSET ON CAL CAP AT 1kHz
270 C$="Z" @ GOSUB 9000 ! SCAN STATUS BYTE UNTIL SETTLED
280 IF BIT(A(1),5)=0 THEN 270
290 F=F1 @ GOSUB 8300 ! SENDS INITIAL FREQ
300 T=T6*1000*T(T3) ! SETS DELAY TIME
320 IF T1>T THEN T=T1
330 IF T>T0 THEN T0=T ! SELECTS LONGER DELAY TIME
340 H1=LGT(F1) @ H2=LGT(F2) @ H0=H1 @ F0=F1 @ J=0
350 J=J+1 @ IF J=1 THEN 380
360 ON L6+1 GOSUB 7000,7100 ! CALL FREQ INC
370 GOSUB 8300
380 WAIT T @ C$="A2 1" @ GOSUB 9000 ! RUNS AUTOSET ON CAL CAP AT FREQ F
390 C$="Z" @ GOSUB 9000 ! CHECK FOR SETTLED STATUS BYTE
400 IF BIT(A(1),5)=0 THEN 390
410 ! READ AND CALIBRATE CHANNEL 1
420 C$="W 1" @ GOSUB 9000 ! SENDS LOCAL LOCKOUT
430 WAIT T
440 C$="Q1" @ GOSUB 9000
450 P1=C5*W/A(1) @ IF X=1 THEN P1=P1/10 ! ALLOWS FOR x10 EXPAND
460 C$="K 1;K 4;K 4;K 12" @ GOSUB 9000 ! PHASE SHIFT (-π/2)
470 C$="X "&VAL$(X) @ GOSUB 9000 ! SENDS x10 EXPAND IF REQUIRED
480 WAIT T
500 ! READ AND CALIBRATE CHANNEL 2
510 C$="Q2" @ GOSUB 9000
520 P2=C5/A(1)
550 ! SELECT SAMPLE AND SEND ACC VOLTAGE (V0)
560 GOSUB 9900
570 OUTPUT 709 ;"A6" ! ACTIVATES RELAY 6 (SAMPLE IN)
600 I=0 @ OUTPUT 707 ;V0
610 WAIT T0
620 GOSUB 8500
630 I=1 @ OUTPUT 707 ;V
640 WAIT T0
650 GOSUB 8500
```

```
750 ! FINAL DISPLAYS, ETC.
760 OUTPUT 709 ; "B6" ! SWITCH OUT SAMPLE
770 C$="X 0;K 1;K 4;K 4;K 13;W 0" @ GOSUB 9000 ! REMOVE PHASE SHIFT
790 GOTO 350
800 G(J)=-999 @ C$="W 0" @ GOSUB 9000 ! UNLOCK FRONT PANEL
820 OUTPUT 707 ;0 ! SENDS ZERO VOLTS
830 CLEAR @ DISP "EXECUTION TERMINATED"
840 IF P6=1 THEN GOSUB 9550 ! TAPE STORAGE
850 IF P7=0 THEN 1000
860 CLEAR @ DISP "Gp/w PEAK INFORMATION: "
870 DISP @ DISP "Peak Gp/w value=" @ DISP G6;"pMho/Hz"
880 DISP "At Gp/w peak, Cp=" @ DISP C6;"pF"
890 DISP "Peak Frequency =";F7;"Hz"
1000 DISP @ DISP "END" @ END
7000 ! LOG FREQ INC
7010 H=H0+(H2-H1)/(N1-1)
7020 IF H>H2 THEN 800
7030 F=10^H @ H0=H
7040 RETURN
7100 ! LINEAR FREQ INC
7110 F=F0+(F2-F1)/(N1-1)
7120 IF F>F2 THEN 800
7130 F0=F
7140 RETURN
7500 ! OUTPUT TO INTERNAL PRINTER
7510 PRINT G1;"pMho/Hz" @ PRINT C2;"pF" @ PRINT F6;"Hz" @ PRINT
7520 RETURN
8300 ! SEND FREQUENCY
8305 IF F=100000 THEN J1=1000 @ J2=0 @ F6=F @ GOTO 8320
8310 J6=INT(LGT(F)) @ J2=4-J6 @ J9=10^(J6-2) @ J1=INT((F+.0001)/J9) @ F6=J1*J9
8320 IF J2=2 THEN J3=1 ELSE J3=J2
8330 IF J2>2 THEN J3=2
8340 C$="J "&VAL$(J1)&", "&VAL$(J2) @ GOSUB 9000 ! SENDS FREQ
8350 C$="F "&VAL$(J3) @ GOSUB 9000 ! SETS BAND
8360 W=2*PI*F6
8370 T3=1+INT(LGT(F6))
8380 C$="T "&VAL$(T3)&", "&T6$ @ GOSUB 9000 ! SET TIME CONSTANT
8390 RETURN
8500 ! READ CH1 AND CH2
8510 C$="Q1;Q2" @ GOSUB 9000
8520 G=A(1)*P1*.000000000001 @ C=A(2)*P2*.000000000001
8530 IF I=0 THEN GOSUB 9600 ELSE GOSUB 9700
8540 RETURN
9000 ! I/O ROUTINE FOR LOCK-IN
9010 GOSUB 9200 ! DO SERIAL POLL
9020 IF BIT(S9,0)=0 THEN 9010 ! WAIT FOR PREVIOUS COMMAND DONE
9030 OUTPUT 706 USING "K" ; C$
9040 I9=0
9050 GOSUB 9200 ! DO SERIAL POLL
9060 IF BIT(S9,7)=0 THEN 9080 ! CHECK FOR OUTPUT READY
9070 I9=I9+1 @ ENTER 706 ; A(I9)
9080 IF BIT(S9,0)=0 THEN 9050 ! CHECK FOR COMMAND DONE
9090 RETURN
9200 ! SERIAL POLL ROUTINE
9210 S9=SPOLL(706)
9220 RETURN
9300 ! TEMPORARY PAUSE ROUTINE
9310 BEEP @ BEEP @ CLEAR @ DISP "TEMPORARY PAUSE IN EXECUTION"
9320 DISP @ DISP "PRESS CONT TO CONTINUE"
9330 C$="W 0" @ PAUSE ! UNLOCKS FRONT PANEL AND PAUSES PROGRAM
9340 C$="W 1" ! RELOCKS FRONT PANEL
9350 BEEP @ GOSUB 9900
9360 RETURN
```

```
9500 ! TAPE FILE CREATION
9510 CLEAR @ DISP "INSERT DATA TAPE AND PRESS CONT" @ PAUSE
9520 DISP @ DISP "FILENAME"; @ INPUT X$
9530 CREATE X$, N1+3, 24 @ ASSIGN# 1 TO X$
9540 DISP @ DISP X$; " CREATED" @ PRINT# 1 ; X$, V
9545 RETURN
9550 FOR I=1 TO J
9560 IF G(I)=-999 THEN PRINT# 1 ; G(I) @ GOTO 9590
9570 PRINT# 1 ; G(I), C(I), F(I)
9580 NEXT I
9590 RETURN
9600 ! CALCULATE Rs, Cox FROM G(0), C(0)
9610 R0=G/(G^2+W^2*C^2)
9620 IF R0<0 THEN R0=0
9630 C0=C*(1+G^2/(W^2*C^2))
9640 RETURN
9700 ! CALCULATE Gp/w AND Cp
9710 D=(W^2*C0*R0*C-G)^2+W^2*(C0-C-C0*R0*G)^2
9720 G1=W*C0^2*(G-W^2*C^2*R0-R0*G^2)*1.E12/D ! SGp/w in pMho/Hz (pF)
9730 C2=(W^2*C0*C*(C0-C)-C0*G^2)*1.E12/D ! SCp in pF
9732 G(J)=G1 @ C(J)=C2 @ F(J)=F8
9735 IF P8=1 THEN GOSUB 7500
9740 IF G1<G6 THEN 9750
9745 G6=G1 @ C6=C2 @ F7=F6
9750 RETURN
9900 CLEAR @ DISP "SAMPLE SWITCHED IN"
9910 DISP @ DISP "TO STOP EXECUTION TEMPORARILY" @ DISP "PRESS KEY k1" @ ON KEY# 1, "STOP" GOSUB 9300 @ KEY LABEL
9920 RETURN
```

PROGRAM 'VPLOTm'

```
5 N=1 @ CLEAR @ PLOTTER IS 705
7 DISP "INSERT DATA TAPE : OK"; @ INPUT X$@ IF UPC$(X$[1,1])#"Y" THEN CLEAR @ GOTO 7
8 DISP "DATAFILE NAME"; @ INPUT N$@ IF N=2 THEN 55
9 A=-1000 @ B=-1000
10 ASSIGN# 1 TO N$
15 READ# 1 ; L$,F
16 W=2*PI*F
20 M=0
25 M=M+1
30 READ# 1 ; G@ IF G=-999 THEN 40 ELSE READ# 1 ; C,V
31 G=G/W
32 IF M=2 THEN G1=G @ C1=C @ V1=V
33 A=MAX(G,A) @ B=MAX(C,B)
35 GOTO 25
40 ASSIGN# 1 TO *
50 P1=INT(V1) @ Q1=INT(V+1) @ R=-50 @ S=100*INT(1+B/100)
51 IF P1>Q1 THEN P=Q1-1 @ Q=P1 ELSE P=P1 @ Q=Q1
52 U=10*INT(1+A/10) @ T=U*(R/S)
55 SCALE P,Q,R,S
60 IF N=2 THEN PEN 3 @ GOTO 100
75 CSIZE 5 @ OUTPUT 705 ; "SP5"
76 XAXIS 0,.5
80 FOR I=P+1 TO Q-1
82 MOVE I,R/2 @ LABEL I; "V"
83 NEXT I
85 PEN 1 @ YAXIS 0,R/2
90 MOVE 0,S/4-2.5 @ LABEL ;S/4; "pF"
95 MOVE 0,S*3/4-2.5 @ LABEL ;S*3/4; "pF"
100 MOVE V1,C1
105 I=0 @ ASSIGN# 1 TO N$ @ READ# 1 ; L$,F
110 I=I+1
120 READ# 1 ; G@ IF G=-999 THEN 152 ELSE READ# 1 ; C,V
130 IF I=1 THEN 110
140 DRAW V,C
150 GOTO 110
152 ASSIGN# 1 TO *
153 SCALE P,Q,T,U
154 IF N=2 THEN PEN 4 @ GOTO 160
156 PEN 2 @ YAXIS 0,T
157 CSIZE 5 @ MOVE 0,U/2-.25 @ LABEL ;U/2; "pMho/Hz"
160 MOVE V1,G1
165 I=0 @ ASSIGN# 1 TO N$ @ READ# 1 ; L$,F@ W=2*PI*F
170 I=I+1
180 READ# 1 ; G@ IF G=-999 THEN 210 ELSE READ# 1 ; C,V
185 IF I=1 THEN 170
190 DRAW V,G/W
200 GOTO 170
210 ASSIGN# 1 TO *
220 IF N=2 THEN 250
225 CLEAR @ DISP "ANOTHER PLOT (Y/N)" @ INPUT X$
230 IF UPC$(X$[1,1])="Y" THEN N=2 @ GOTO 7
250 CLEAR @ DISP "END" @ END
```

PROGRAM 'NssCAL'

```
10 CLEAR @ DISP "MANUAL CALCULATION OF Nss AND "
20 DISP @ DISP "Enter ~s" @ INPUT E
30 DISP "Enter Nd in cm-3" @ INPUT D1@ D1=D1*1000000
40 DISP "Enter T in Kelvin" @ INPUT T
50 DISP "Enter top contact diameter in mm" @ INPUT S@ A=PI*(.001*S/2)^2
60 COPY
70 K=1.38E-23 @ Q=1.6E-19 @ E1=8.85*.000000000001
80 CLEAR @ DISP "Enter plot reference" @ INPUT J$@ PRINT J$
90 DISP @ DISP "Enter freq in Hz" @ INPUT F
100 DISP "Enter Vpeak in Volts" @ INPUT V
110 DISP "Enter variance function f()" @ INPUT Z
120 DISP @ DISP "Enter Gp/w peak (pMho/Hz)" @ INPUT G1@ G1=G1*.000000000001
130 DISP "Enter Cp value (pF)" @ INPUT C1@ C1=C1*.000000000001
140 P=K*T/Q+Q*E*E1*D1*A^2/(2*(C1-G1/Z)^2) !    in eV
150 N=G1*.0001/(A*Q*Z) !  Nss in cm-2 eV-1
160 PRINT "Freq=";F;"Hz";"     Vpeak=";V;"V"
170 PRINT "Nss=";N;"cm-2 eV-1"
180 PRINT "  =";P;"eV" @ PRINT
190 CLEAR @ DISP "PRESS CONT FOR ANOTHER POINT" @ PAUSE
200 GOTO 80
```

APPENDIX B1: SILICON Pd-MOS DEVICE PREPARATION

Sample N1 : Pd/105 nm SiO_2/n-Si device

Source : GEC plc

Substrate Details : n-Si <100>, 1-2 Ωcm, 3"

Oxide Details : 105 (±2.5) nm SiO_2 (grown in dry O_2 at 1100°C for 48 minutes). Measured by ellipsometer.

Back Contact Deposition : Surface wiped with 5% HF solution and rinsed clean with water. 60 nm Au/Sb alloy evaporated at ∿0.1 nm/second.

Back Contact Annealing : 400°C for 2 minutes in dry N_2. Ohmic contact produced.

Top Electrode Deposition : 20 nm Pd evaporated at ∿0.1 nm/second through mask of 1.25 (±0.025) mm diameter holes.

Hydrogen Annealing Procedure (part-wafer) : 400°C for 5 minutes in 35% H_2/N_2 atmosphere. Cooled in dry N_2 flow for 20 minutes.

Sample N2 : Pd/12 nm SiO_2/n-Si device

Source : RSRE

Substrate Details : n-Si <100>, 18-30 Ωcm, 3"

Oxide Details : 12 (±1) nm SiO_2 (grown in dry O_2 atmosphere). Measured by ellipsometer.

Back Contact Deposition : Surface wiped with 5% HF solution and rinsed clean with water. 60 nm Au/Sb alloy evaporated at ∿0.1 nm/second.

Back Contact Annealing : 400°C for 2 minutes in dry N_2. Ohmic contact produced.

Top Electrode Deposition : 20 nm Pd evaporated at ∿0.1 nm/second through mask of 1.25 (±0.025) mm diameter holes.

Hydrogen Annealing Procedure (part-wafer) : 400°C for 5 minutes in 35% H_2/N_2 atmosphere. Cooled in dry N_2 for 20 minutes.

APPENDIX B2 : LB FILM DEVICE PREPARATION

Sample M1 : Multilayer ωTA MIM device

Substrate Details : Glass cover slide, refluxed in IPA. 60 nm Al evaporated at ∿0.5 nm/second.

LB Film Material : ω-tricosenoic acid.

Film Deposition Parameters : Temperature = 20.5°C, subphase pH = 4.93, no counterions.

Multilayer Structure : 0, 5, 9, 13, 17, 21, 25, 29, 33, 37, 41 layer regions ωTA deposited.

Top Electrode Deposition : Mask of 0.45 (±0.025) mm diameter holes applied. 20 nm Al evaporated at ∿0.05 nm/second followed by 20 nm Au at ∿0.1 nm/second. Electrodes deposited in 5 nm stages, leaving 15 minutes between each stage.

Sample N3 : Au/Al/nascent oxide/n-Si device

Source : GEC plc

Substrate Details : n-Si <100>, 2 Ωcm, 3".

Back Contact Deposition : Surface wiped with 5% HF solution and rinsed clean with water. 60 nm Au/Sb alloy evaporated at ∿0.1 nm/second.

Back Contact Annealing : 400°C for 2 minutes in dry N_2. Ohmic contact produced.

Oxide Details : Grown oxide removed by 40% HF solution etch (1 minute) to leave nascent oxide.

Top Electrode Deposition : Contacts evaporated as soon as possible after above etching process. 20 nm Al (rate ∿0.05 nm/second) followed by 20 nm Au (rate ∿0.1 nm/second) evaporated in 5 nm stages through mask of 1.25 (±0.025) mm diameter holes.

Sample N4 : Pd/ωTA multilayer/n-Si device (freshly etched)

Source : GEC plc

Substrate Details : n-Si <100>, 2 Ωcm, 3".

Back Contact Details : Au/Sb alloy deposited and annealed as for sample N3.

Insulator Details : SiO_2 removed from substrate by 40% HF solution etch (1 minute). 8, 16, 24 layers of ωTA deposited as soon as possible after etching process (∿8 minutes in practice).

Film Deposition Parameters : Temperature = 18.0°C, subphase pH = 5.54, no counterions.

Top Electrode Deposition : 20 nm Pd evaporated in 5 nm stages through mask of 1.25 (±0.025) mm diameter holes. Rate ∿0.05 nm/second.

Sample N5 : Pd/ωTA multilayer/n-Si device (aged etch)

Source : GEC plc

Substrate Details : n-Si <100>, 2 Ωcm, 3".

Back Contact Details : Au/Sb alloy deposited and annealed as for sample N3.

Insulator Details : SiO_2 removed from substrate by 40% HF solution etch (1 minute). 8, 16, 24 layers of ωTA deposited 13 days after etching process.

Film Deposition Parameters: Temperature = 17.5^{o}C, subphase pH = 5.51, no counterions.

Top Electrode Deposition : 20 nm Pd evaporated as for sample N4.

Sample N6A, B, C, D: Au/Al/ωTA/SiO_2/n-Si MIOS devices

Source : GEC plc

Substrate Details : n-Si <100>, 2 Ωcm, 3".

Back Contact Details : Au/Sb alloy deposited and annealed as for sample N3.

Oxide Details : 32 (±1) nm SiO_2 (grown in dry O_2 at 950°C for 70 minutes). Measured by ellipsometer.

LB Film Material : ω-tricosenoic acid.

Film Deposition Parameters:

Sample N6A : Temperature = 17.7^{o}C, subphase pH = 6.96, no counterions

Sample N6B : Temperature = 19.2^{o}C, subphase pH = 6.98, with counterions

Sample N6C : Temperature = 19.4^{o}C, subphase pH = 5.30, no counterions

Sample N6D : Temperature = 18.6^{o}C, subphase pH = 3.97, no counterions

Top Electrode Deposition : 20 nm Al + 20 nm Au as for sample N3.

APPENDIX C

LANGMUIR TROUGH

Full computer control and monitoring for systematic research and production applications in Langmuir-Blodgett Film deposition.

Joyce-Loebl

A Vickers company

LANGMUIR

The new Langmuir Computer-Controlled Trough brings comprehensive programming, control and monitoring capability together with proven trough mechanics – creating a system for the production and study of Langmuir-Blodgett Films that fully meets the stringent criteria demanded by the growing number of full research facilities in the field.

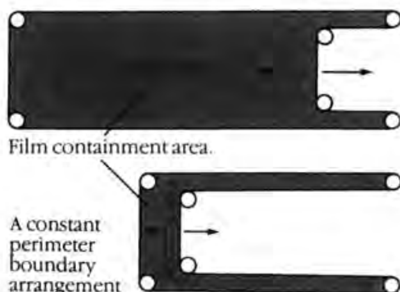
In pure research the substantial precision mechanics and fine control of the deposition parameters maximise the quality of Langmuir-Blodgett Films produced in controlled environments.

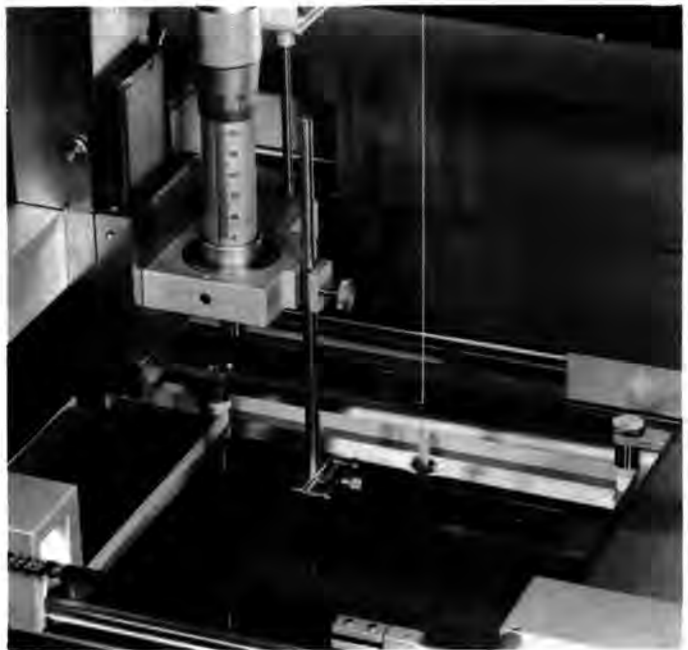
For applied work the programmable dipping sequences, multilayer capability and storage of process parameters allow easy production of high quality structures.

Overall, the provision of computer interaction not only optimises the deposition process but also allows rapid establishment of a previous set of deposition parameters to automatically reproduce a special dipping sequence or to compare multiple results.

Utilising trough hardware based on other Joyce-Loebl designs offers the proven advantages of constant perimeter barrier technology:

- easy access for cleaning or subphase exchange
- immunity from subphase evaporation or leakage effects
- simple replacement of key components
- low contamination risk





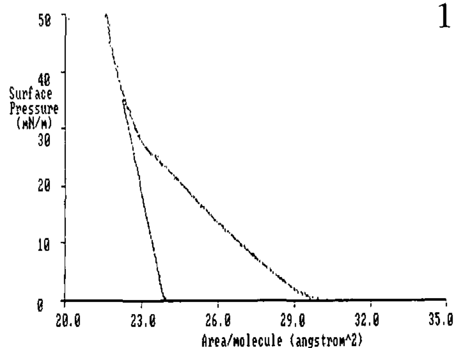
The open working area of a Langmuir Computer-Controlled Trough showing (l to r), micrometer dipping head, head position transducer, substrate holder/substrate and Wilhelmy plate which senses film surface pressure. The PTFE-coated glass fibre barrier tape can be seen semi-immersed in subphase.

Two subphase container trough designs are available: a glass full-depth version and Teflon FEP shallow version with dipping well for applications where subphase volume usage is critical.

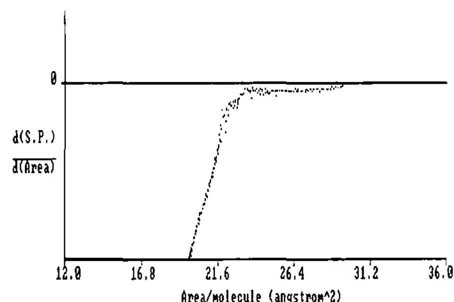
TROUGH

COMPUTER CONTROL

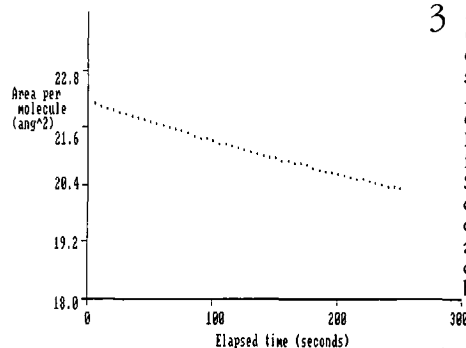
With computer control the basic operation of the trough is greatly simplified and numerous additional facilities are now available, which allow complete programmability, calibration, monitoring and graphical display of results. Operation of the trough is obtained via a number of self-contained programmes, written in Advanced BASIC. These are selectable from an easy-to-follow menu and are progressed via clear prompts. No detailed computer knowledge is necessary for complete operation, although ample remark statements and documentation enable users to develop their own related software for specialist applications.



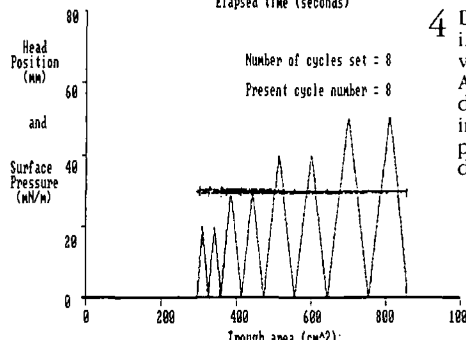
1 Isotherms can be automatically calibrated and output as Surface Pressure versus Trough Area or Area per molecule. In the latter case extrapolation routines are provided for accurate evaluation of the characteristic area per molecule.



2 Isotherms can also be differentiated to aid determination of the breakpoints on the pressure area curve.



3 Many time dependent plots can be obtained, such as Molecular Area, indicating collapse rate of Langmuir-Blodgett film material, and Surface Pressure to confirm constancy of pressure during an extended dipping sequence, below.



4 Deposition profiles, i.e. Head positions vs. Trough Film Area, can be displayed to indicate the progress of multi-dipping sequences.

Many derived results can be calculated to further aid analysis, for example deposition ratio, a valuable indicator of film quality. Review of results is facilitated by automatic scale expansion which allows close study of fine detail and at all stages hard copy output of screen displays can be obtained. Storage of experimental parameters is virtually automatic and can be easily referenced to allow comparison of results or repetition of the exact deposition sequence.

Facilities available in the MENU include:

- **Calibration** of system geometry, electro balance, dipping speeds and other mechanical parameters.
- Recording of pressure-area **Isotherm** including establishment of monolayer, graphical display and/or hard copy
- Monitoring of film **Area** vs. time
- **Multidip** sequences, including stepped structures, with display of deposition profile.
- Data storage of all experimental parameters
- **Plots** of Isotherms, Area changes or Deposition profile using stored data.

LANGMUIR COMPUTER-CONTROLLED TROUGH SPECIFICATIONS

APPROXIMATE DIMENSIONS:	Mechanical unit cabinet 116cm x 56cm x 84cm high Computer control unit 45cm x 45cm x 10cm high
APPROXIMATE WEIGHT:	Mechanical unit cabinet 180kg Computer control unit 5kg
AREA MEASURING SYSTEM:	Maximum working area 1000cm² Minimum working area 60cm² Rate of area change 0 – 120cm²/sec
FILM SURFACE PRESSURE:	Range 0 – 50mN/m Measurement ± 0.1mN/m Control accuracy ± 0.1mN/m (compression and expansion)
SAMPLE DIPPING:	Range 0-75mm, programmable dipping limits Maximum speed 1mm/sec Minimum speed 1mm/min
VIEWING LIGHT:	UV-Free fluorescent
TROUGH OPTIONS:	Glass, capacity 12 l (full depth) or Teflon FEP, capacity 5 l (shallow with dipping well, cross-section 90 x 30mm)
SUBPHASE TEMPERATURE CONTROL (optional):	+ 10 to + 40°C ± 1°C
CHART RECORDER OUTPUT:	Film Area 0 to + 2V nominal Film Pressure 0 to + 10V nominal Dipping Head Position + 2V to + 10V nominal
ELECTRIC SUPPLY:	110/240V, 50/60 Hz, 50 VA
COMPUTER SYSTEM:	**Hardware** ● IBM PC or compatible microcomputer with dual floppy disc drives, colour monitor, 96 kbyte memory, high resolution colour graphics card and two free slots for DI-AN interface cards ● Printer connected via parallel printer interface (e.g. Epson FX80). **Software** ● Standard IBM PC including DOS ● Joyce-Loebl software on floppy discs fully annotated and menu driven, written in Advanced BASIC ● Documentation
ANCILLARY EQUIPMENT:	● pH meter/digital thermometer ● Combined two pen YY-X or YY-t recorder (records pressure/area isotherms and deposition profiles or monitors pressure and area).

The Trough apparatus is available without computer control where manual operation is sufficient. The Joyce-Loebl Langmuir Trough is constructed from corrosion resistant materials to ensure long trouble-free operating life and is supplied mounted in a purpose-built glass fronted cabinet.

In line with the Joyce-Loebl policy of continuous product development we reserve the right to change specifications without prior notice

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For further details of Operating Principles and Applications see separate brochure.

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