The development of a detector system for mint object spectroscopy on the Isaac Newton telescope

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THE DEVELOPMENT OF A DETECTOR SYSTEM

FOR FAINT OBJECT SPECTROSCOPY

ON THE ISAAC NEWTON TELESCOPE

by

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A Thesis submitted to the University of Durham in candidature

for the Degree of Doctor of Philosophy

1987

To my parents, Audrey and Jack

ABSTRACT

The work reported in this thesis describes the development of the CCD instrumentation for the Faint Object Spectrograph on the 2.5m Isaac Newton Telescope at the Observatorio del Roque de los Muchachos, more commonly known as the La Palma Observatory.

The Faint Object Spectrograph is a highly efficient, fixed-format CCD spectrograph aimed at low resolution spectrophotometry (15-20 Å FWHM) over a wide spectral range (400-1050 nm). Its high throughput, compared with that of more conventional spectrographs, is due to the small number of optical surfaces, and the minimum vignetting which results from locating the CCD inside the spectrograph camera.

A CCD camera system is described which was developed primarily to test and commission the Faint Object Spectrograph, but also to assess the characteristics of the GEC P8603 CCD used in the spectrograph, and optimize its performance for this application.

The use of CCDs in astronomy is now commonplace but there still remains some uncertainty as to which aspects of their performance need to be most critically assessed when choosing a device for a particular application. It is argued that it is important to consider not only the obvious characteristics such as quantum efficiency, spectral coverage, readout noise and geometrical format, but also, and particularly at astronomically relevant low-light levels, the consequences of the more subtle properties such as charge transfer efficiency, threshold effects and chip defects.

The CCD detector in the Faint Object Spectrograph is located inside the spectrograph camera and needs to be positioned to high accuracy within the optical path. A microprocessor system is described which enables the CCD detector to be aligned remotely from the observer's control console.

Finally, the commissioning of the Faint Object Spectrograph on the Isaac Newton Telescope is described, and some of the first results obtained during commissioning are presented in order to illustrate its potential in the field of faint object spectroscopy.

ACKNOWLEDGEMENTS

I would like to thank Professor A W Wolfendale F.R.S. for the support of this work and the use of laboratory facilities in the Physics Department at Durham. Additionally, I am indebted to the Director of the RGO, Professor A Boksenberg F.R.S., and his staff for ensuring the success of the project.

I would also like to offer my sincere thanks to my supervisor, Dr J M Breare, both for his assistance throughout the duration of this work, and encouragement to complete this thesis.

Many people have participated in the development of the Faint Object Spectrograph, both at Durham and the RGO, and I would like to take this opportunity to thank all those involved for their assistance. Unfortunately, it is not possible to mention them all by name here, but I would like to thank my colleagues in Durham who, like myself, embarked on this project many years ago, namely, Richard Ellis, Graham Martin and Ian Parry. Special thanks go to John Webster for his skilled technical assistance and friendly encouragement.

I would particularly like to thank Dave Thorne, both for his friendship and his help, without which this thesis would never have been completed.

With regard to the production of the thesis, my sincere thanks go to Joy Hamblyn for her excellent typing, and patience, Monica Everest for many of the drawings, and Richard Worth and Dave Calvert for the photography.

The work has been supported by grants from the Science and Engineering Research Council.

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CHAPTER 1

INTRODUCTION

1.1 Introduction

This thesis reports the author's contribution towards the development of the 'Faint Object Spectrograph' (FOS) for the 2.5m Isaac Newton Telescope (INT) at the Observatorio del Roque de los Muchachos, more commonly and easily referred to as the La Palma Observatory (LPO).

FOS is a highly efficient, fixed-format CCD spectrograph aimed at low resolution (15-20 Å FWHM) spectrophotometry over a wide spectral range (400-1050 nm). Its peak efficiency including atmospheric absorption and telescope losses is 12% at 700 nm and a zenith distance of 27.5 degrees. It is a 'common-user' instrument and the result of a collaboration between the Royal Greenwich Observatory (RGO) and the Physics Department of Durham University.

The optical design is based on a Schmidt camera working, without a collimator, in the diverging f/15 beam from the telescope's Cassegrain focus. Dispersion is provided by a transmission grating and a cross-dispersing prism which together produce a two-order format covering 500-1050 nm in first order and 400-550 nm in second order. The high throughput of the system compared with that of more conventional spectrographs is due to the small number of optical surfaces, and the minimum vignetting which results from the location of the CCD detector inside the camera.

FOS enables the user to forego most of the tedious alignment and calibration procedures that afflict other instruments. The fixed spectral format has allowed the development of extensive on-line data reduction and analysis software which enables the user to flat-field, sky-subtract, flux and wavelength calibrate the data in tandem with further observing.

FOS is not to be regarded simply as a more efficient version of a general-purpose spectrograph. It works at a considerably lower dispersion (450 Å/mm) and consequently, its spectral resolution in first order is a factor of 2 or 3 coarser than the poorest available with more conventional spectrographs. FOS is however ideally suited to, and indeed primarily intended for, the spectral examination of the faintest of astronomical targets; those objects whose spectra could not realistically be obtained in a reasonable exposure period with any other instrument. The question arises of course as to the purpose of pursuing such observations.

1.2 The Purpose of Faint Object Spectroscopy

The central problems in astronomical research today are undoubtedly those of a cosmological nature involving the large scale structure of the universe, its age and its evolution. To resolve these questions, it is necessary to study the universe at different moments in its history. Inherent in the concept of the big bang is the inference that the most distant galaxies appear to us as they were when closer to the origin of the universe. The measurement of their distances is possible by accepting Hubble's law - that all galaxies are receding from us, and the further away an object, the greater its velocity of recession. Redshift, interpreted as a Doppler shift, can be used as a measure of velocity and therefore as a distance indicator, thus placing the object at its appropriate epoch. The ability to measure the redshifts of the faintest and most distant objects is essential in order to probe earlier epochs of the universe.

1.2.1 The Large Scale Structure of the Universe

The basic question is whether the universe is infinite or finite, i.e. whether it is open or closed. Both the geometry and the dynamics of the universe are an integral part of this problem.

The geometry can be studied by mapping the 3-D distribution of astronomical bodies and looking for deviations from Euclidean laws. It may of course be that the objects are not uniformly distributed in co-moving volume, in which case the cosmic evolution of the population is superimposed on the volume geometry, and both geometry and evolution are studied simultaneously. The examination of the most distant objects is paramount to any investigation of this type.

The mass density of the universe is the essential datum determining whether the universe is open or closed. There are two ways in which this may be determined more or less directly: through observations of the clustering properties of galaxies and the motions within clusters, and through observation of deviations from a Euclidean Hubble relation. Both approaches demand redshifts for faint galaxies in large numbers.

1.2.2 Age

Calculations of the age of the universe are dependent on estimates of its rate of expansion. By extrapolating this rate back into the past, one arrives at the time the expansion began. Hubble's constant (Ho) gives the present rate of expansion, but widely differing estimates of its value lead to inverse Hubble constant ages ranging from 10 to 20 billion years. It is certain, however, that the mutual gravitational attraction of galaxies, the positive mass density of the universe, has slowed the expansion and therefore 1/Ho provides only upper limits to the age. It is believed that the rate at which the expansion is decelerating is large. A relatively large value for the mass density, an appreciable fraction of the closure density as is commonly accepted now, would imply that even for the lowest value of Ho the universe is only between 10 to 15 billion years old. This value is itself uncomfortably low when compared with ages calculated from globular cluster data. Globular clusters are among the oldest objects known; studies of their colour and luminosity together with stellar evolutionary theory suggest their age to be $\sim 16 \pm 3 \times 10^9$ years. The age problem is intrinsically linked with the geometry problem; the mass density (or deceleration) is crucial in both, and makes instruments such as FOS prime observational tools in the quest.

1.2.3 Evolution and Galaxy Formation

Evolutionary trends in the properties of galaxies can be deduced from epoch variations in the colours of galaxies and in the optical luminosity function. To study the former, deep and complete samples are required with redshifts and calibrated spectra. To study the latter, the form of the luminosity function, it is necessary to obtain number counts of complete samples of very faint galaxies, and likewise the redshifts for these samples. In survey work of this nature, large numbers of observations are required if statistically significant results are to be obtained. At the same time, radio-surveys at different frequencies, together with programmes of optical identification and redshift measurement, enable comparisons to be made between optical and radio properties. Studies of QSOs and radio galaxies provide the best chance of establishing a redshift cut-off corresponding to an epoch of galaxy formation, while studies of the complete samples of (optically-selected) galaxies are essential to map the spatial evolution and the stellar evolution subsequent to formation.

1.3 The Design of a Faint Object Spectrograph

The optical system of a conventional spectrograph comprises three main sections: the collimator, the dispersion system and an optical camera to focus the spectrum onto a detector. Light losses are incurred, however, both from refracting and reflecting optical surfaces and so the overall efficiency of the system diminishes at each successive air-glass interface. High reflectivity mirror surfaces and anti-reflection multilayer coatings on transmission elements can be effective over a small spectral range, but do not maintain their efficiencies over the wide range of wavelengths required by astronomers (typically, from wavelengths of the atmospheric cut-off in the ultraviolet (~300 nm) to 1000 nm or longer in the infrared). It is therefore desirable that the number of optical surfaces used in the design of a spectrograph intended for the spectral examination of the faintest of astronomical targets over a wide spectral range should be kept to a minimum. Wynne (1982a) has described how this goal may be approached in a spectrograph using a transmission grating which is replicated on the front face of a cemented assembly of a cross-dispersing prism and the aspheric corrector plate of a flat-field, wide-aperture, single-mirror camera with a solid-state detector at its focus.

The recent availability of solid-state image sensors, CCDs and the like, of high quantum efficiency over a wide spectral range and of small physical size has allowed the possibility of locating a detector directly at the focus of a single-mirror camera of the Schmidt type. In contrast, image-tube detectors which have been, and still are, widely used for astronomical spectroscopy have large physical bulk in relation to their photosensitive area. Such detectors are too large to be accommodated inside a single-mirror spectrograph camera and so a second optical surface, with an inevitable further loss of light, has hitherto been necessary to divert the beam to an accessible position.

To make the most efficient use of a detector, the image which it receives of the spectrograph slit should be of the same order of size as the detector's resolution. For faint object work, the slit will normally be set to be about the same width as that of the seeing disc. It follows that on a large telescope, a spectrograph camera of large numerical aperture is required, increasingly so as detectors with smaller pixel size are considered.

The image spread arising from aberrations within the optical system should obviously be smaller than the detector's resolution, but this is difficult to achieve over a wide spectral range in a wide aperture camera with few optical surfaces. The conventional Schmidt camera, comprising a spherical mirror and an aspheric corrector plate at its radius of curvature, provides good aberration correction over an extended field at large numerical aperture, but over a wide spectral range, its performance suffers from chromatic difference of spherical aberration. It also gives rise to a curved image surface which must be corrected if a solid-state detector is to be used. Wynne (1977) has described how in a modification of the Schmidt camera, the field curvature of the mirror may be corrected by a self-achromatic lens (i.e. a lens for which the coefficients of chromatic difference of focus at the two surfaces are made equal and opposite) placed some distance in front of the camera focus. While correcting the field curvature, the lens also introduces spherical aberration, coma and astigmatism. The spherical aberration may be cancelled, however, by modifying the asphericity of the Schmidt plate. The coma and astigmatism are corrected by an appropriate choice of the front curvature of the lens and by a reduced separation between the mirror and aspheric plate compared to a normal Schmidt camera. Chromatic difference of spherical aberration from the Schmidt plate is largely offset by that arising from the field-flattening lens.

The design of a spectrograph camera is complicated still further by the diffraction grating which sets the effective aperture stop of the system. If, as is usual in a spectrograph, the dispersion is provided by a reflection grating, its separation from the camera must be sufficient to allow the collimator beam to reach the grating without obstruction. However, for wide aperture cameras, the aberrations of oblique imaging generally increase as the stop distance is increased. At low dispersion, the use of a transmission grating instead of a reflection grating has the advantages of greater efficiency, and of allowing the stop to be positioned immediately in front of the camera. Over a wide spectral range in which more than an octave is to be recorded simultaneously, cross-dispersion is also required to separate the otherwise overlapping first and second orders. These dispersions can be provided with minimal loss of light by having a transmission grating replicated on the entrance face of a cross-dispersion prism, the exit face of which is cemented to the aspheric plate of the camera. This, of course, gives rise to a system with a fixed spectral format but with high throughput; the grating, cross-disperser and camera aspheric have together only two air-glass surfaces. In contrast, a general-purpose spectrograph usually allows the user to choose from a range of gratings and hence dispersions but, inevitably, has lower overall efficiency.

In order to reduce light losses in a spectrograph still further, Wynne (1982b) has shown that if the collimator optics are dispensed with, then the aberrations arising from the grating in a diverging beam from the slit may be either corrected or reduced over a wide spectral range (350-1100 nm) and, for moderate slit widths, by further modification of the camera optics. To reduce coma, the aspheric plate has to be displaced in the direction of dispersion relative to the axis of the camera mirror and field-flattening lens. The compensation for astigmatism depends on the angle of incidence of the diverging beam upon the grating, necessitating either the introduction of a cylindrical refracting surface within a compound aspheric plate assembly or a tilt of the focal surface of the camera.

In a diverging beam, a single cross-dispersing prism cannot be used because the oblique incidence on the prism face introduces serious aberrations. However, if a compound prism is used instead (constructed from two or more prisms made from glasses of approximately the same refractive index for a mean wavelength, but with differing dispersions and with the entrance and exit faces normal to the axis of the diverging beam) then the aberrations arising in addition to those produced by a plane parallel block of glass in a diverging beam are relatively small and can be corrected in the following camera system. The disadvantage of the compound prism is that it precludes transmission down to the atmospheric ultraviolet cut-off because there are no suitable glasses available; a reasonable transmission can however be obtained down to 350 nm.

1.4 Background to the RGO-Durham University Collaboration

The RGO-Durham University collaboration to develop a faint object spectrograph for the LPO 2.5m INT commenced early in 1981. It arose from the enthusiasm expressed for the design proposed by Wynne (1982b) for the LPO 4.2m telescope.

The concept of a ´fast´ spectrograph aimed specifically at the examination of astronomically faint objects created much interest amongst RGO and Durham University astronomers wishing to pursue faint object programmes of a statistical nature. At that time, it was clear that the demand for ´survey´ type programmes on the 4.2m telescope would far exceed the observing time available. Thus, early in 1981, the need for a similar instrument for the LPO 2.5m INT was discussed. Besides the obvious desirability of providing the INT with a spectrograph of maximum possible efficiency, it was considered that the INT would offer more opportunities for longer-term survey programmes, programmes which would provide appropriate reference studies for understanding those objects accessible only to a 4m class telescope. It was also recognized that the experience gained from operating a FOS on the INT, scheduled to be commissioned a few years in advance of the 4.2m telescope, would be invaluable for finalizing the design of the 4.2m FOS.

An application to the SERC from Durham University and the RGO requesting funds to develop the 2.5m FOS to ´common-user´ level was partially successful; SERC provided half of that requested in an attempt to get the project started. The progress from the initial discussions to the current working system suffered from financial, mechanical, detector and weather frustrations. Nevertheless, the successful outcome of the project serves to demonstrate the effectiveness of the collaboration.

The project was set up with R A E Fosbury (RGO) and J M Breare (Durham) as joint project scientists, joined by R S Ellis (Durham) and I G van Breda (RGO) as project collaborators. J R Powell (RGO) was appointed general project manager.

C G Wynne (RGO) assisted by S P Worswick (RGO) modified the original optical design for operation at the INT´s f/15 Cassegrain focus.

D W Gellatly (RGO) was responsible for the overall mechanical design of the instrument and its interface to the INT´s existing Cassegrain instrumentation. J M Breare and J Webster (Durham) supervised the manufacture in Durham University Physics Department workshops.

The author was responsible for the design and construction of a CCD camera and data acquisition system to test CCD chips for FOS, assess their characteristics and to commission FOS on the INT. He was also responsible for the development of drive electronics and their control from a microprocessor to enable remote focus adjustment of the CCD detector inside the FOS camera.

G P Martin (Durham) wrote the data acquisition and instrument control software. I R Parry (Durham) wrote the extensive on-line data reduction and analysis software, assisted latterly by A Purvis (Durham).

FOS was assembled and optically tested at the RGO over the winter 1983/84 under the supervision of C M Lowne (RGO). It was shipped to La Palma in May 1984 and subsequently commissioned on three separate observing runs in July and December 1984 and in May 1985.

During the last commissioning run, the Durham University CCD camera electronics were exchanged for a standard LPO camera system (developed by P R Jorden (RGO) and D J Thorne (RGO)) to facilitate on-site maintenance. W F Lupton (RGO) brought about the integration of the FOS software with that of the INT's other instrumentation.

The involvement of all those mentioned (and many more) was generally much broader than the specific roles suggest, particularly during commissioning, confirming that the project has been very much a team effort.

FOS is now a common-user instrument and in regular use.

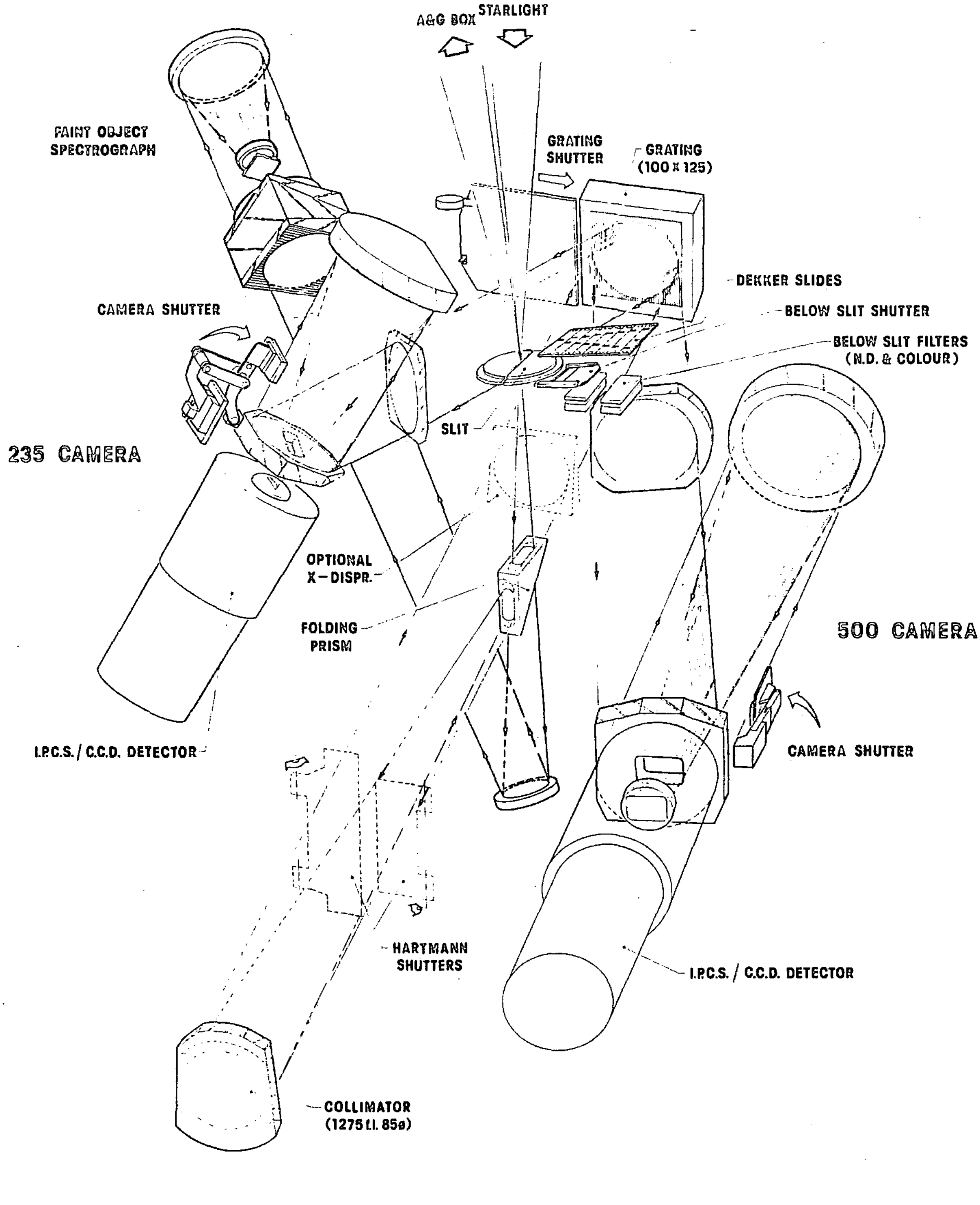
1.5 The 2.5m Faint Object Spectrograph

The optical components of the INT's Cassegrain spectrographs, the Intermediate Dispersion Spectrograph (IDS) and the Faint Object Spectrograph (FOS), are shown in Figure 1.1. Figure 1.2 is a sketch illustrating the mechanical arrangement of the two spectrographs. Relevant parameters of FOS are collected in Table 1.1.

FOS uses the slit, slit shutter and dekker slide within the IDS together with the TV acquisition and autoguider systems, comparison lamps and filter slides provided for the IDS in the Acquisition and Guidance Unit.

A single folding prism beneath the slit assembly has to be removed to allow the diverging beam from the slit to enter FOS. Changing operation from one spectrograph to the other takes around 30 minutes, and so both spectrographs can be used consecutively during the same night.

Because of the limited clearance between the IDS and the dome observing floor, a folding-flat mirror had to be introduced to accommodate the long path length of the f/15 beam. An extended blue response silver



SPECTROGRAPH OPTICAL SYSTEMS

2·5m TELESCOPE CASSEGRAIN SPECTROGRAPH (L.P.O.)

Figure 1.1

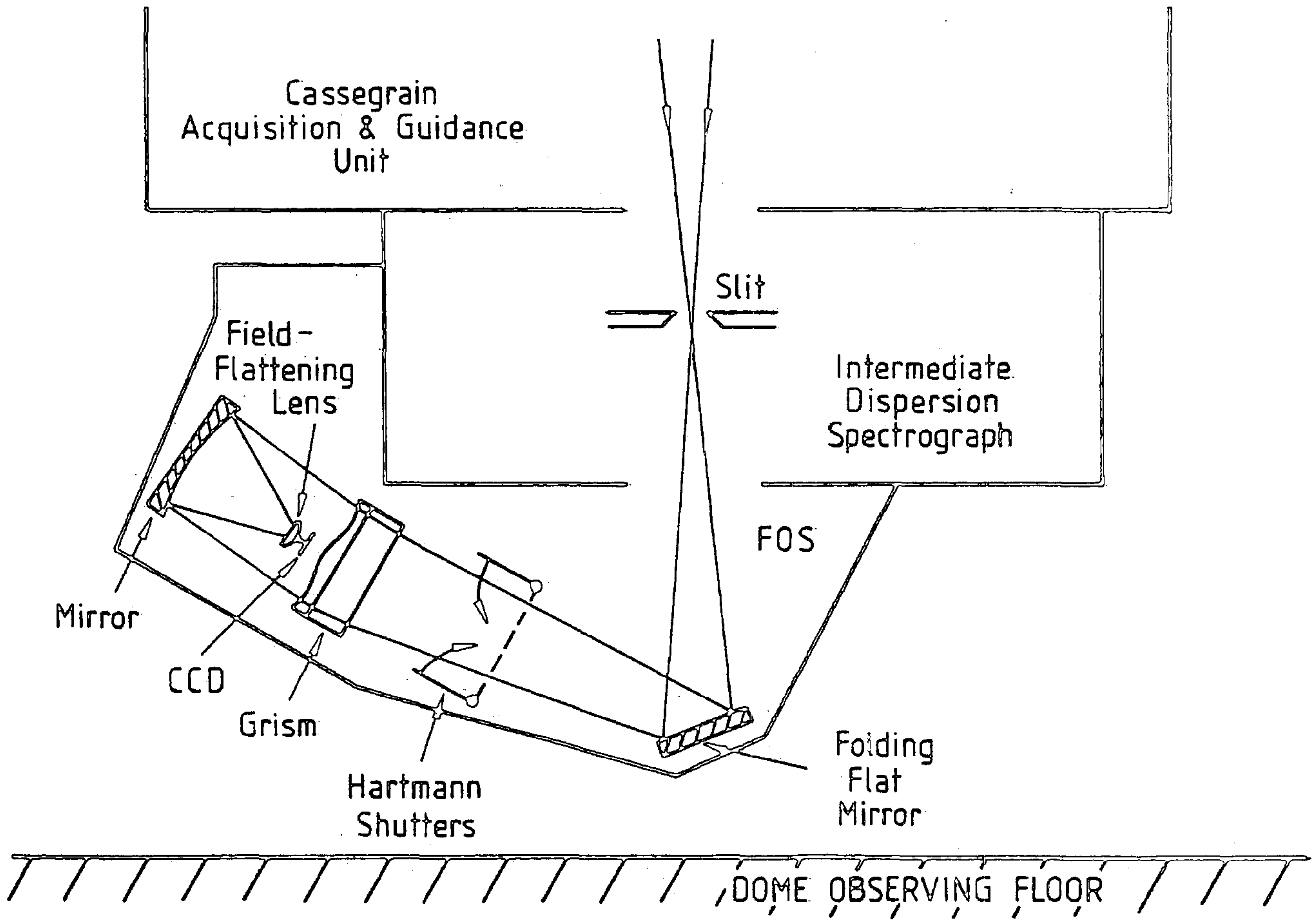

Cassegrain
Acquisition & Guidance
Unit
Slit
Intermediate
Dispersion
Spectrograph
FOS
Field-
Flattening
Lens
Mirror
CCD
Grism
Hartmann
Shutters
Folding
Flat
Mirror
DOME OBSERVING FLOOR

Figure 1.2

coating helps to reduce the inevitable loss of light from this additional optical surface. The mirror is mounted with a tilt facility which, during the initial alignment procedure, allows some movement of the spectrum on the detector so that defects inherent in the particular CCD chip may be avoided.

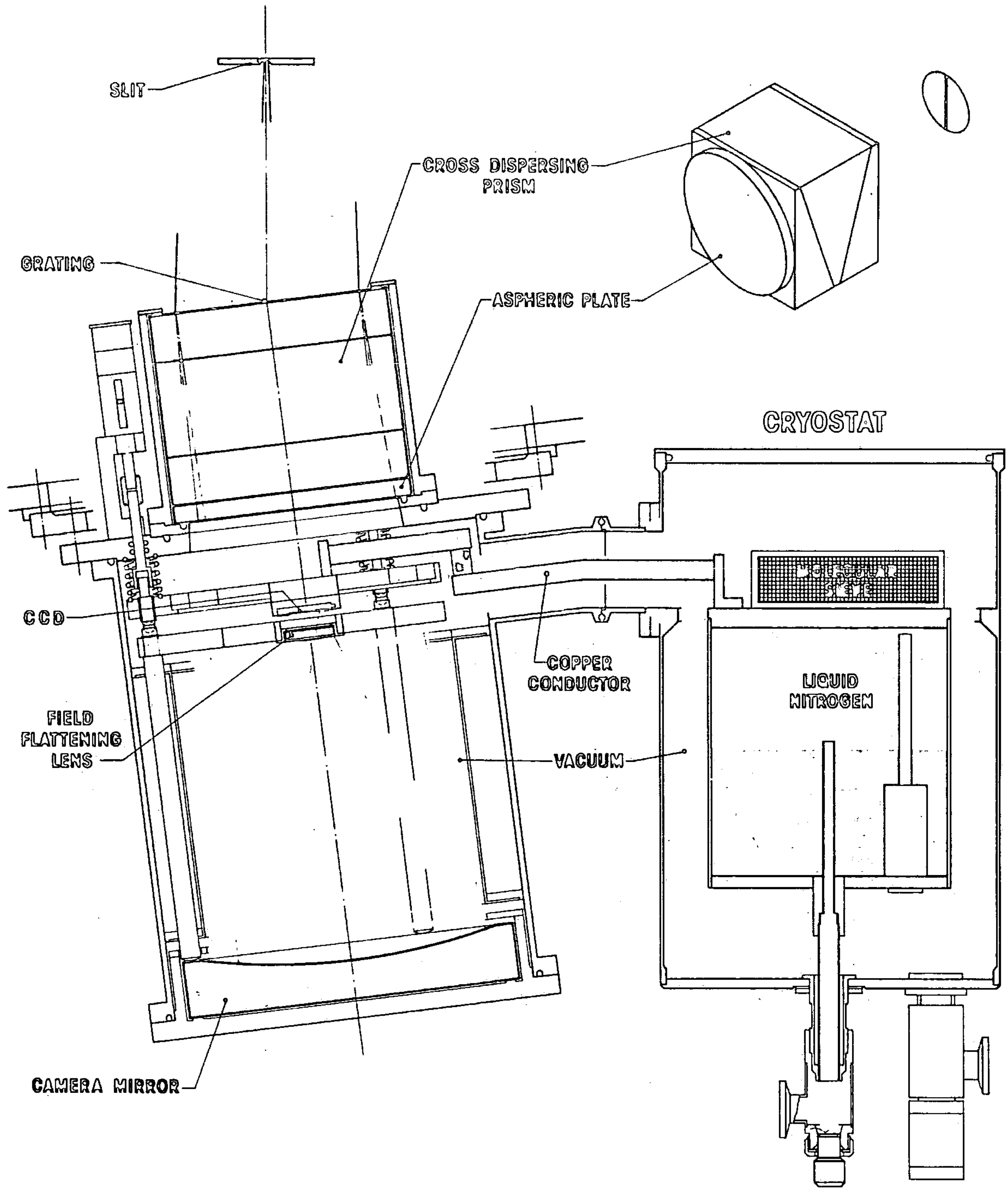
FOS is equipped with its own Hartmann shutters to facilitate focussing of the CCD detector (being a late addition to the system, these are not shown in Figure 1.1). The shutter blades are pneumatically driven under the control of a microprocessor which is operated from the observer's console through the INT's instrumentation computer.

The spectrograph camera, shown in cross-section in Figure 1.3, provides a first order dispersion of 450 Å/mm and a focal ratio at the detector of f/1.4. A transmission grating of 150 lines/mm is replicated on the front face of a cemented assembly of three cross-dispersing prisms (constructed from Schott SK5 and LF5 glasses) and the aspheric corrector plate of the camera (constructed from Schott K10 glass). This is mounted off the faceplate of the camera body which houses the camera mirror, the field-flattening lens and the CCD detector.

The CCD is a GEC P8603 of 578 x 385 pixels, each 22 x 22 μm. A typical device has a quantum efficiency with a peak value of ~ 40% at 740 nm, 10% points at ~ 460 nm and ~ 930 nm and 1% points at ~ 390 nm and ~ 1020 nm. The advantageous characteristic of the GEC chip is its low inherent readout noise; a value in the range 5-10 electrons rms can usually be achieved with careful optimization of its operating conditions and of the readout electronics.

The grating and cross-disperser, together, provide dispersion in a two-order format covering the wavelength ranges 500-1050 nm in first order and 400-550 nm in second order with a minimum order separation of 20 pixels which corresponds to 25 arcsec on the sky. First order dispersion is sampled at 10.7 Å/pixel. Figure 1.4 illustrates the fixed-format of the spectrum as projected onto the CCD.

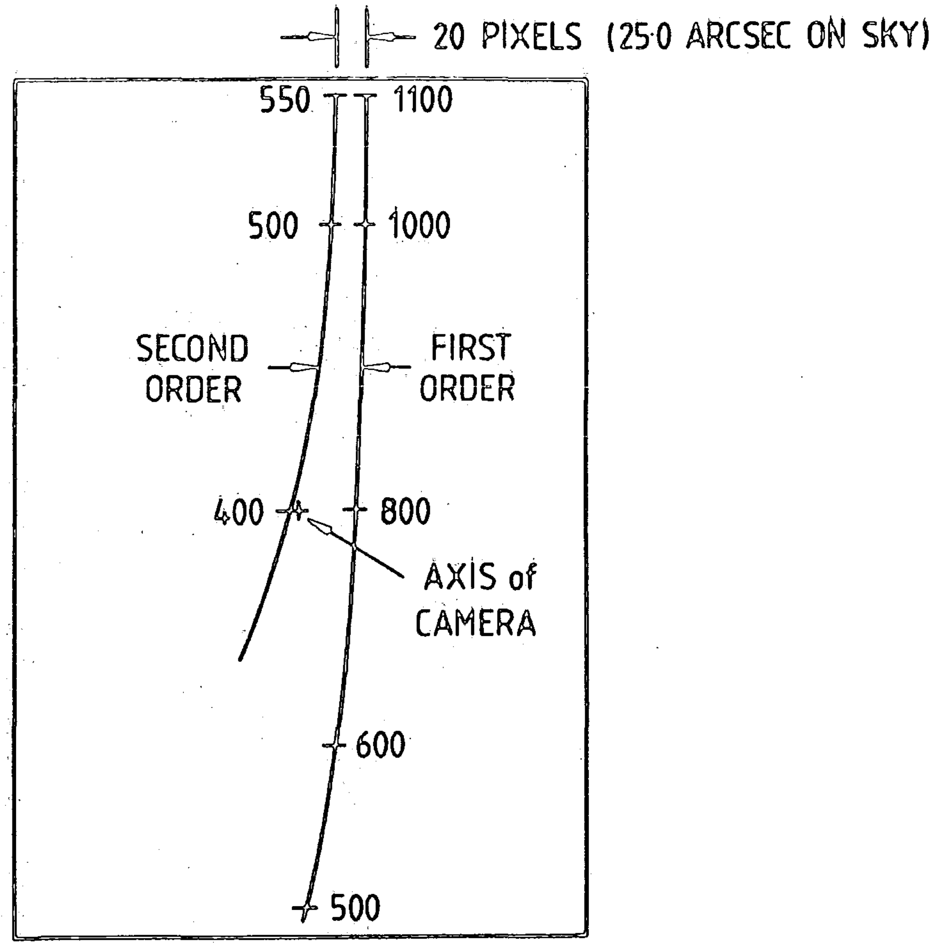
The small physical size of the GEC CCD has enabled it, and the printed circuit board upon which it is mounted, to be located within the central



R.G.O. DURHAM UNIVERSITY L.P.O. 2·5m.
FAINT OBJECT SPECTROGRAPH.

Figure 1.3

SPECTRUM AS PROJECTED ONTO THE CCD



WAVELENGTHS ARE IN nm

Figure 1.4

obscuration from the telescope's secondary mirror and so no additional vignetting is introduced.

The CCD is held against a copper block which is cooled from a liquid nitrogen cryostat, appended to the camera body, by conduction through a system of 'cold-finger' linkages and copper braid. Servo amplifier electronics mounted outside the camera vessel maintain the CCD at a nominal operating temperature of 150 K (at which the thermal generation of electrons within the CCD is negligible) with a stability of better than ±0.05 K.

The field-flattening lens is supported in the camera by four slender fibreglass arms which are attached to an outer annular ring, itself spaced off the camera mirror by three invar rods of low thermal expansivity. A similar arrangement of fibreglass arms and a second annular ring supports the CCD behind the lens. Whereas the lens is held in the beam in a position fixed by the optical design, a system of three motor driven micrometers (controlled from the previously mentioned microprocessor) enable axial and tilt displacement of the CCD with respect to the lens for precise focus adjustment.

The camera vessel, cryostat, folding-flat mirror and Hartmann shutters are held in position in an open-frame structure constructed from 3 mm steel plate. Its attachment to the IDS provides additional rigidity. Flexure tests of the structure on the INT have shown that the image of a spectral line shifts by only 0.03 pixels/hour in the direction of dispersion as the telescope tracks through the zenith.

Table 1.1 BASIC PARAMETERS OF THE 2.5m FAINT OBJECT SPECTROGRAPH

Image scale at the slit (f/15 Cass.)		5.4138 arcsec/mm
Slit-to-detector reduction factor		10.5
Camera focal ratio at the detector		f/1.4
GEC P8603 CCD format		578 x 385 pixels 12.67 x 8.47 mm 12.00 x 8.03 arcmin
Pixel size		22 x 22 μm 1.25 x 1.25 arcsec
Wavelength coverage:	first order	500 - 1050 nm
	second order	400 - 550 nm
Dispersion:	first order	10.7 Å/pixel
	second order	5.4 Å/pixel
Minimum order separation		20 pixels 25.0 arcsec
First order grating blaze		700 nm

1.6 Structure of the Thesis

This thesis is concerned primarily with the description of a CCD camera system, its use to assess the characteristics of the GEC P8603 type CCD image sensor and to commission the 2.5m FOS.

The use of CCD image sensors for optical astronomy is now commonplace. Chapter 2 briefly reviews why they are used and the way in which they are operated. The reasons for choosing to use the GEC P8603 CCD in FOS and a description of the chip are also given.

Chapter 3 is devoted to a technical description of the CCD camera system and in particular, the electronics to generate the necessary waveforms to drive the CCD and to convey digitized data to a computer. Chapter 4 concentrates on the all important task of extracting the video signal from the CCD, maximizing as far as possible the CCD's output signal-to-noise ratio, and the use of analogue signal processing electronics to attenuate the readout noise inherent in the CCD's on-chip charge detection circuitry.

The results of laboratory investigations of the GEC CCD's imaging characteristics are presented in Chapter 5. It is argued that in selecting a CCD for a particular application, it is important to consider not only the obvious characteristics of quantum efficiency and spectral range, readout noise and geometrical format, but also, and particularly at astronomically relevant low-light levels, the consequences of the more subtle properties of charge transfer efficiency, threshold effects, chip defects and temperature dependence.

Chapter 6 is devoted to a technical description of the mechanisms incorporated in FOS to enable remote focus adjustment of the CCD detector, their drive electronics and their control from a microprocessor.

Chapter 7 turns to the commissioning of FOS on the INT and an assessment of its performance. Some of the first astronomical data obtained from the instrument are presented in Chapter 8.

Conclusions from this work and suggestions for the future are collected in Chapter 9.

CHAPTER 2

CCD IMAGE SENSORS AND THEIR USE IN OPTICAL ASTRONOMY

2.1 Introduction

The concept of the charge-coupled device (CCD) was proposed by Boyle and Smith (1970) and emerged from their research for a silicon-based electrical equivalent of magnetic bubble memories.

In its simplest implementation, the CCD structure consists of a series of closely spaced electrodes separated from an underlying semiconductor substrate by a thin insulating (oxide) layer. When a bias voltage is applied to an electrode, a depletion region is formed in the semiconductor immediately beneath it. The depletion region is, in effect, a 'potential well' which can store information in the form of an electrical charge packet. By pulsing the electrodes in an appropriate sequence, the potential well and hence its charge packet, can be transferred through the semiconductor. With the addition of a point for introducing charge packets, and another for detecting them, a shift register or delay line can be realized.

Although CCDs were originally conceived as devices to store digital information, it is in the field of analogue electronics that they have made their greatest impact to date. It was immediately evident that because the CCD's potential wells were capable of storing variable quantities of charge, they could be used to convey analogue signals. As a result, CCDs have been applied to various analogue signal processing functions including simple delay lines, transverse filters, multiplexers and correlators. It is in their use as solid-state image sensors, however, that CCDs have made their greatest contribution.

There already exist several texts which describe the concepts, physics and operation of the basic CCD structure, its variations and its numerous applications including that of the solid-state image sensor (see for example: Séquin and Tompsett, 1975; Beynon and Lamb, 1980). The purpose of this chapter, therefore, is not to attempt to add another résume to the literature but instead, to review briefly what a CCD image sensor is, why such devices are invaluable for optical astronomy and how they are operated. The reasons for choosing to use a GEC P8603 CCD in FOS are summarized and a brief description of the chip is given.

2.2 CCD Image Sensors

Electron-beam scanned TV camera tubes have been in existence and continuous development for several decades with the result that many advances have been made in the quality of broadcast television. A solid-state equivalent to match their performance has long been sought after by the semiconductor industry, the aim being to exploit the advantages usually associated with solid-state devices, namely, compactness, low weight and ruggedness, low voltage operation and low power consumption. However, despite much development, it is only with the advent of the CCD that realistic means have been available to approach the performance of the camera tube (Weimer, 1975). Previous work in this field was focussed upon the use of an integrated matrix of addressable photodiodes. These devices and variations thereof, however, could provide only limited resolution and their performance suffered from excessive fixed-pattern picture noise.

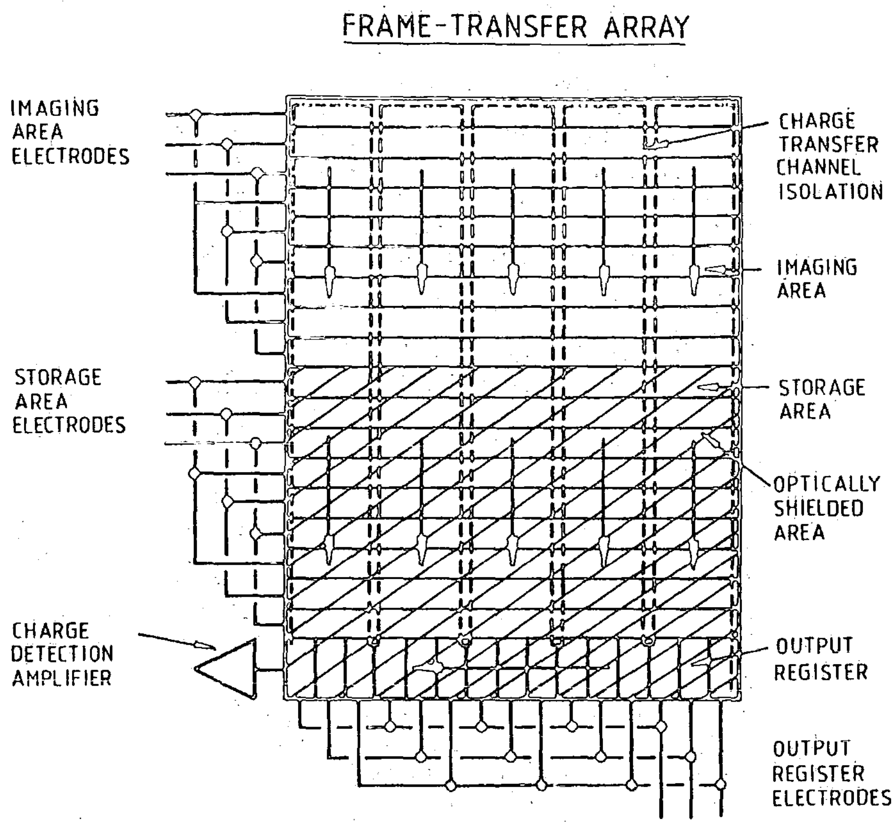
A CCD image sensor basically consists of a mosaic of potential wells formed from an array of electrodes running at right angles to a series of isolated charge transfer channels. Each potential well serves as a collection site or pixel for charge carriers created within the semiconductor by incident photons. An image charge pattern is allowed to accumulate in the CCD by holding the electrodes at appropriate bias potentials. At the end of the integration period, the electrodes are clocked so as to transfer the signal from each pixel serially to a low capacitance charge sensing circuit.

The majority of CCD image sensors have been designed to produce a picture format and readout sequence which matches the conventional line-scanned TV display. An important consideration has been the necessity to minimize the optical smearing of an integrated image charge pattern as it is read out across illuminated parts of the array. This requires that the integration period is long in comparison to the readout time and has been achieved by having separate imaging and optically shielded storage areas. A frame of photon-generated charge is allowed to collect in the imaging area for a given exposure time and is then transferred rapidly into the storage area during the vertical retrace period of the TV display system. The image is then retrieved from the storage area, line by line, at the standard TV rate while the next frame accumulates in the imaging area. The two most successful array organizations to have emerged are the frame-transfer array (Séquin et al., 1973) and the interline transfer array (Walsh and Dyck, 1973). These are shown schematically in Figure 2.1.

The frame-transfer array's imaging and storage areas are defined by two groups of horizontal electrodes formed upon isolated vertical charge transfer channels. A horizontal output register at the bottom of the array serves for sequential line-by-line readout from the storage area to a charge sensing circuit. The direction of charge transfer is indicated by arrows. For normal operation, all parts of the array other than the imaging area are shielded from incident illumination either by an external mask or by a metal overlay deposited upon the chip. Following the integration of an image charge pattern, the whole frame is moved down into the storage area by applying clocks to both the imaging and storage area electrodes. While the next frame is imaged, the storage area is read out one line at a time through the output register and charge detection amplifier.

The interline transfer array differs from the frame-transfer array in that its storage area charge transfer channels are spaced between the imaging area columns. Each imaging column consists of isolated charge collection sites defined beneath a single photogate. An integrated image charge pattern is transferred horizontally in one step into the storage area by clocking the photogates. A horizontal output register is used for serial readout of the storage area in a similar manner to the frame-transfer array. The advantage of the interline transfer array is that image smear is reduced to a minimum. However, the storage areas must be shielded by a metal overlay on the chip and this, of course, means that imaging area columns have optically insensitive regions between them.

When the concept of the CCD was proposed in 1970, MOS technologies


FRAME-TRANSFER ARRAY
IMAGING AREA ELECTRODES
CHARGE TRANSFER CHANNEL ISOLATION
IMAGING AREA
STORAGE AREA ELECTRODES
STORAGE AREA
OPTICALLY SHIELDED AREA
CHARGE DETECTION AMPLIFIER
OUTPUT REGISTER
OUTPUT REGISTER ELECTRODES

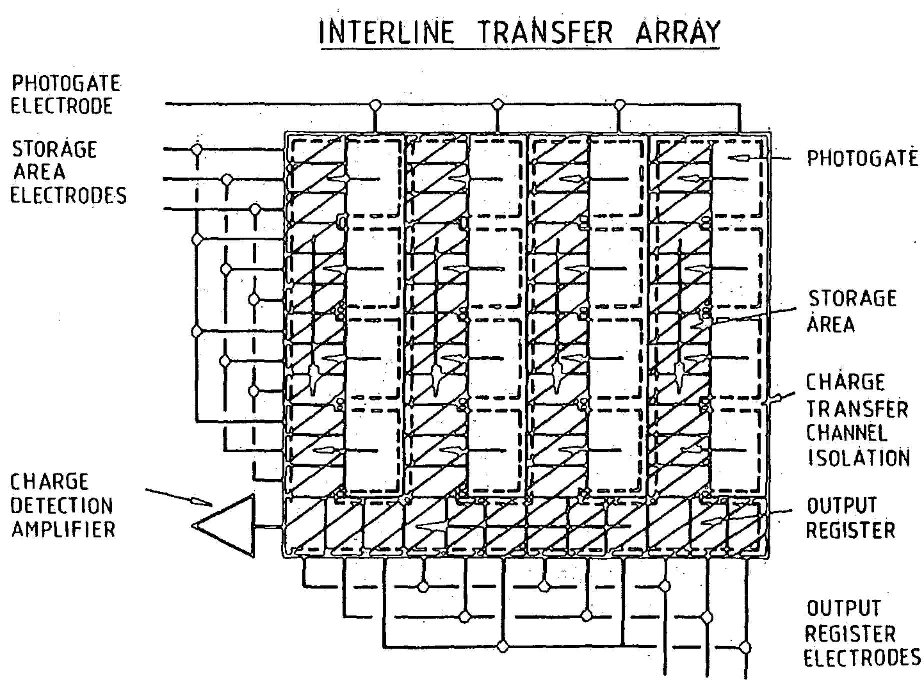

INTERLINE TRANSFER ARRAY
PHOTOGATE ELECTRODE
STORAGE AREA ELECTRODES
PHOTOGATE
STORAGE AREA
CHARGE TRANSFER CHANNEL ISOLATION
CHARGE DETECTION AMPLIFIER
OUTPUT REGISTER
OUTPUT REGISTER ELECTRODES

Figure 2.1

suitable for device fabrication were already well developed, and so the progress towards the realization of a CCD image sensor was rapid. (See for example: Bertram et al., 1972; Kovac et al., 1973; Séquin et al., 1974). By 1974, a 320 x 512 pixel frame-transfer array had been demonstrated (Rogers, 1974), providing more than an order of magnitude increase in the number of pixels that had been achieved with photodiode arrays and sufficient image resolution to meet the requirements of the USA TV standard.

CCD fabrication technologies have, of course, undergone continuous development and refinement in order to improve performance. Of importance has been the development of thinned, back-illuminated CCDs for increased spectral responsivity. To date, most CCDs have employed semi-transparent polysilicon electrodes (Bertram et al., 1974) to allow front illumination through the electrode structure. Light losses are incurred, however, increasingly so with decreasing wavelength, both from absorption, and multiple reflections at the various Si-SiO_2 interfaces, within the electrode structure. To overcome this, a few manufacturers, notably RCA, have developed fabrication techniques for thinning the CCD substrate to a thickness of ~ 10-20 μm to allow illumination through the back of the chip rather than through its electrodes. This can result in very high responsivity, particularly in the blue, as illustrated in Figure 2.2 which shows curves for a front-illuminated GEC CCD and a thinned, back-illuminated RCA chip. An unfavourable characteristic of thinned CCDs, however, is the occurrence of interference fringe effects when illuminated with narrow band light, a result of multiple reflections within the thinned silicon (Oke, 1981).

Several companies have now developed CCD image sensors, mostly of the frame-transfer type, for TV imaging applications (examples include Fairchild, GEC, Philips, RCA, Sony and Thomson-CSF). Although fabrication problems still make it difficult to produce CCDs of sufficient cosmetic quality to satisfy the demands of broadcast television, the applications of CCDs are many and wide ranging. They include surveillance, industrial process control and TV cameras for the home video market. Astronomers were among the first to recognize their scientific potential.

RESPONSIVE QUANTUM EFFICIENCIES OF A THINNED, BACK-ILLUMINATED RCA CCD
AND A FRONT-ILLUMINATED GEC CCD

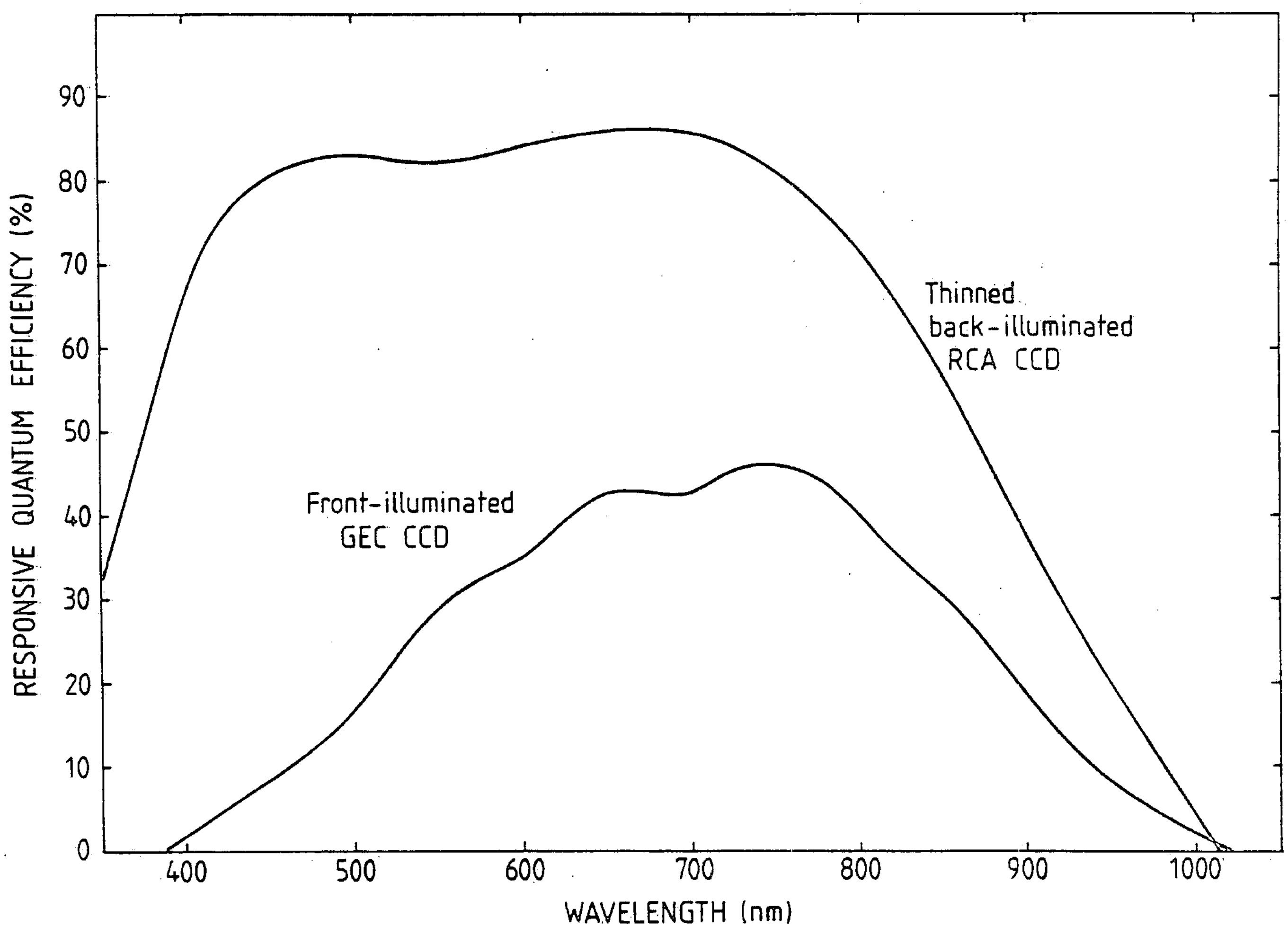


Figure 2.2

2.3 The Use of CCDs in Optical Astronomy

The use of CCDs in optical astronomy began in the late 1970s when a number of astronomical research groups started development of camera systems using the first commercially available CCD TV image sensors from Fairchild (Loh, 1977; Marcus et al., 1979; Leach et al., 1980). Since then, CCDs have gone into use at all major ground-based observatories where, for many applications, they are now chosen in preference to photographic plates and intensifier tube detectors. CCDs have also been applied to space astronomy, being incorporated for example in NASA's Galileo-Jupiter Orbiter (Janesick et al., 1981), the Hubble Space Telescope (Blouke et al., 1983) and ESA's Giotto probe to Comet Halley.

A comprehensive review and comparison of detector systems for optical astronomy has been given by Timothy (1983) and so will not be repeated here. It is, however, important to note the combination of qualities which CCDs offer that has led to their increasing use in this field:

(i) high responsive quantum efficiency (RQE)

- RQE curves reported of a thinned, back-illuminated RCA CCD (Geary and Kent, 1981) and a front-illuminated GEC CCD (Thorne et al., 1986a) are shown in Figure 2.2. Peak values are:

  $\sim$ 86% at $\sim$ 680 nm (RCA CCD)

  $\sim$ 46% at $\sim$ 740 nm (GEC CCD)

(ii) wide spectral coverage

- ranging from $\lesssim$ 300 nm in the near ultraviolet to $\gtrsim$ 1000 nm in the near infrared (Figure 2.2).

(iii) large dynamic range

- it is convenient to define the dynamic range of a CCD as the ratio of its pixel full well charge capacity to the readout noise inherent in the detection of the charge collected within a pixel. A ratio of $\sim$ 38,000 has been reported of GEC CCDs (Thorne et al., 1986a).

(iv) linear responsivity (unity gamma)

- the number of electrons created in a CCD is directly proportional to the number of absorbed photons.

(v) well defined, spatially quantized and stable pixel geometry

- the CCD provides stable, spatially quantized image information, defined by the physical structure of the chip, and is therefore well suited as a transducer for optical input to a computer.

(vi) direct readout into a computer

- with appropriate drive electronics to read out and digitize the signal charge collected in each CCD pixel, CCDs are ideally suited to computer control, enabling immediate on-line data display and reduction at the telescope.

2.4 The Operation of CCDs in Optical Astronomy

The operation of a CCD in optical astronomy differs from that of TV imaging applications in the following aspects:

(i) exposure period.

Long exposure periods ranging from milliseconds to hours are required which necessitates that the chip is cooled in order to reduce ´dark current´.

Dark current arises from the intrinsic thermal generation of charge carriers which occurs in semiconductors at non-zero temperatures. In CCDs, it provides an undesired source of charges which steadily accumulate in the potential wells and which cannot be distinguished from photon-generated charges. Dark current therefore imposes a maximum on the useful integration time of the CCD.

At room temperature, the rate of dark current generation is typically $\sim 10^5$ electrons/pixel/second which, although tolerable at TV readout rates, prohibits the long exposure periods required in astronomy. Dark current is, however, a strong function of temperature (decreasing by a factor of 2 for every 6-10°C reduction in operating temperature) and can be reduced to a negligible rate (~0.1-1.0 electrons/pixel/minute) by cooling the CCD to cryogenic temperatures (~100-150 K). The usual method is to cool the chip from a liquid nitrogen reservoir, both of which are housed within an evacuated enclosure in order to reduce conduction and convection losses. CCDs are in general not operated at liquid nitrogen temperature itself (77 K), but instead, at some higher temperature in the range 100-150 K, the optimum value of which depends on other chip characteristics as discussed in Chapter 5.

(ii) illumination options.

Frame-transfer CCDs are usually supplied with an external mask fitted over the chip's storage area to shield it from illumination. Removal of the mask enables operation in a 'full-frame' imaging mode in which both the imaging and storage areas are used to collect photon-generated charges thereby doubling the area normally available for imaging.

Use of the storage area for imaging in interline transfer arrays is not possible because, in these arrays, the mask has to be defined by strips of metal overlay deposited on the chip. Goad and Ball (1981) have, however, reported the use of a Fairchild interline transfer CCD which was supplied specially to KPNO without metal overlay.

(iii) shuttered exposure.

It is usual to incorporate an electronically operated shutter within the light path to the CCD to control its exposure to illumination and thereby avoid optical smearing of an integrated image charge pattern as it is read out of the array.

(iv) exposure and readout sequence

In contrast to TV imaging applications in which the CCD is continuously read out, the exposure and subsequent readout follows an operational sequence in which:

(i) prior to an exposure, the CCD is read out several times in darkness (i.e. with the shutter closed) in order to ensure a complete erasure of charge from the array imaging area.

(ii) the shutter is opened for the desired exposure period during which a photon-generated charge pattern is collected within the imaging area.

(iii) the shutter is closed and the image charge pattern is read out.

Assuming that dark current has been reduced to a rate where it is negligible, the only constraint on the duration of an exposure is that of the collection of spurious charges created by ionising radiation, the main source of which is the cosmic ray particle background.

The effects of cosmic rays in CCDs were first reported by Marcus et al. (1979) and have been attributed to cosmic ray muons and electrons of ~10-1000 MeV leaving ionizing trails in the substrate (Leach and Gursky, 1979). The ionizing power of muons is almost constant over this range of energies and in silicon, corresponds to the production of ~80 e-h pairs for each micron travelled. Therefore, the quantity of charge created by a cosmic ray depends on:

(i) the active thickness of the CCD's substrate.

(ii) its path length within the substrate which is dependent on the particle's angle of incidence to the chip's surface.

In a comparison of the events seen in thinned and thick substrate RCA CCDs, Fowler et al. (1981) have reported electron-number event distributions with a mean of ~800 electrons/event for a thinned chip compared to ~5000 electrons/event for a thick chip.

Cosmic rays appear in several forms which again are largely dependent on the thickness of the substrate:

(i) diffuse distributions of charge spread over several pixels which are attributed to carriers being created deep inside a substrate and diffusing laterally before collection in potential wells. Events of this type are frequently seen in thick substrate chips but seldom in thinned ones.

(ii) charge packets confined to a single pixel, common only in thinned chips.

(iii) tracks created by particles incident obliquely upon a chip.

The event rate is typically $\sim 0.04/cm^2/second$ and thus an important consideration for astronomically relevant exposure periods; a frame-transfer CCD of size 1 cm^2 would be expected to collect ~24 events within only a 10 minute exposure. Still higher rates have been reported for some RCA CCDs but in these cases, the excess has been attributed to local radioactivity either within the CCD, its carrier or in the materials surrounding it (Fowler et al., 1981; Thorne et al., 1986a).

(v) pixel readout rate.

At a pixel readout rate of ~5-7 MHz as required for TV imaging applications, the pixel readout noise inherent in the operation of a CCD's on-chip charge detection amplifier is ~200 electrons rms.

Slowing the pixel readout rate down to ~10-100 KHz enables the use of external analogue signal processing electronics to filter this noise with the result that, in the best CCDs, a pixel readout noise $\lesssim 10$ electrons rms and a pixel dynamic range $\gtrsim 10^4$ can be achieved.

(vi) signal digitization, computer control and data acquisition.

For scientific applications, the objective is to encode the signal charge collected in each CCD pixel as a digital number for input to a computer for subsequent display, analysis and storage. Digitization to 16 bit accuracy is usually employed in order to exploit the large dynamic range attainable from slow-scan operation.

It is usual to make the computer also provide the control of the CCD's drive electronics required for the execution of the exposure sequence outlined above.

2.5 Reasons for Choosing to Use a GEC CCD in FOS

The decision of which type of CCD to use in FOS had to be made before a detailed optical and mechanical design of the spectrograph could be completed. At that time only two chips of interest were readily available to research groups within the UK:

(i) the RCA SID53612

(ii) the GEC P8600

The most favourable characteristic of the RCA CCD was recognized as its high quantum efficiency over a wide spectral range (Figure 2.2) and in particular, its response in the near ultraviolet (Geary and Kent 1981; Fowler et al., 1981). It was also known, however, to exhibit high readout noise ~70 electrons rms, and to show interference fringing effects when illuminated with narrow band light. In contrast, the GEC CCD had been reported as having a low readout noise (~10-20 electrons rms) but was also known to have a lower overall responsivity compared to the RCA chip (Wright and Mackay, 1981).

The basic question which had to be addressed, therefore, was that of whether the lower readout noise of the GEC CCD would more than compensate for its lower responsivity. The anticipated performance of FOS assuming an RCA CCD as the detector was first calculated by Wall et al. (1981). This work was pursued by Martin and Parry (1981) to compare the figures with those to be expected using the GEC chip instead.

The throughput efficiencies which were estimated for the atmosphere, the telescope, and the FOS optical components, together with the responsivities of the two CCDs which had been reported at that time, are collected in Table 2.1. These values were used to predict the S/N which could be achieved in a given exposure period as functions of wavelength and magnitude. A simple method of sky subtraction was assumed using identical object+sky and sky apertures. Figure 2.3 shows plots of the S/N anticipated in 10 Å resolution elements after a 1000 seconds integration and assuming that the object signal is spread laterally over 3 pixels. Estimates of the sky brightness (magnitudes/arcsec) at the wavelengths of interest are also listed.

Examination of the curves shows:

(i) for an object fainter than m = 18, the GEC CCD achieves a better

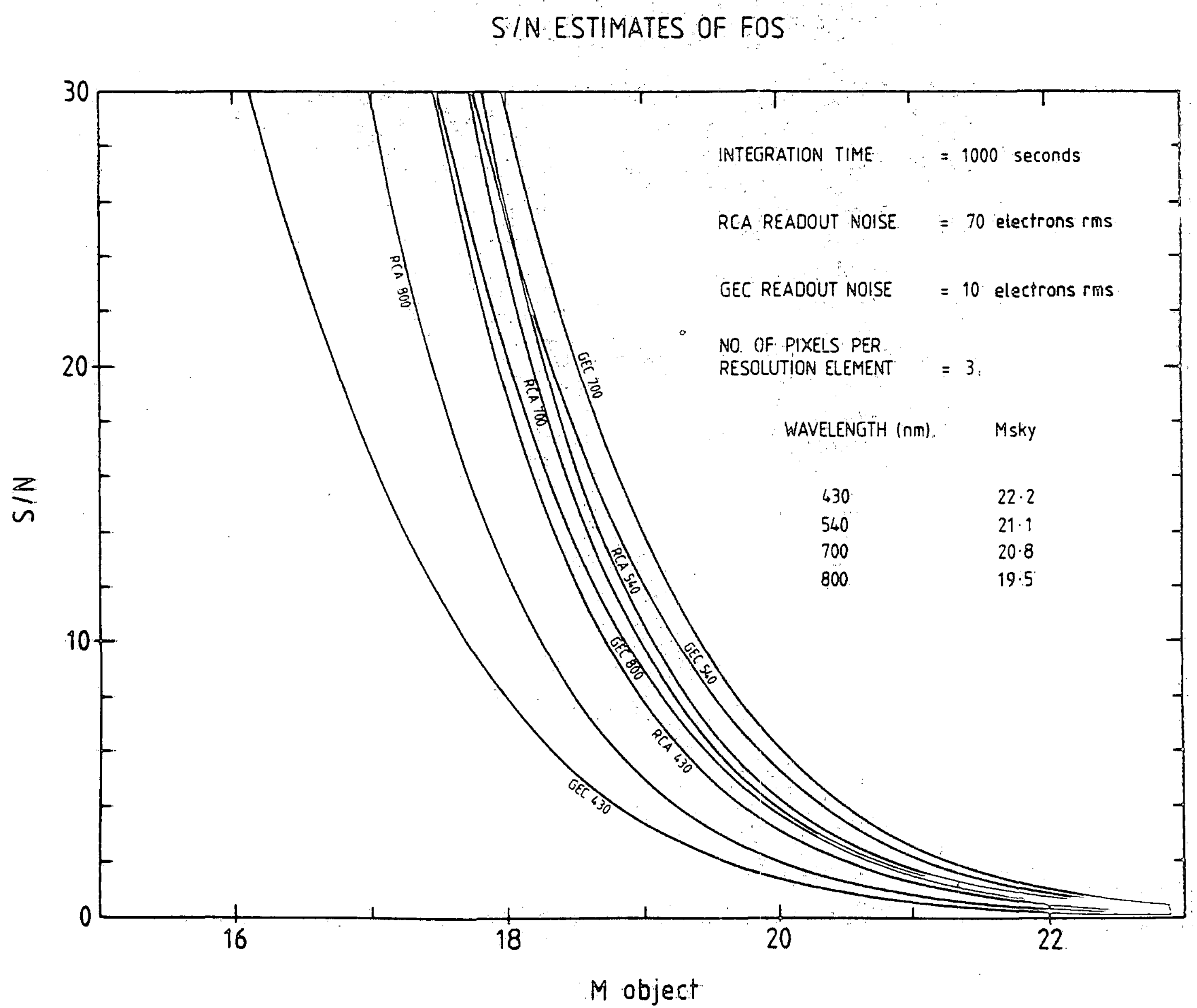

S/N ESTIMATES OF FOS
INTEGRATION TIME = 1000 seconds
RCA READOUT NOISE = 70 electrons rms
GEC READOUT NOISE = 10 electrons rms
NO. OF PIXELS PER RESOLUTION ELEMENT = 3
WAVELENGTH (nm) Msky
430 22·2
540 21·1
700 20·8
800 19·5
RCA 800
GEC 700
RCA 700
RCA 540
GEC 800
GEC 540
RCA 430
GEC 430
S/N
M object
30
20
10
0
16
18
20
22

Figure 2.3

S/N performance compared to the RCA chip at wavelengths > 540 nm. The high quantum efficiency of the RCA chip is largely wasted because of its high readout noise which is still significant in comparison to the photon shot noise. The result is reversed in the 430 nm wavelength curves, however, because the responsivity of the RCA CCD is many times better than that of the GEC chip (Figure 2.2).

(ii) as an object brighter than m = 18 is considered, the S/N curves start to converge (as can be seen in the 540 nm wavelength curves for example). Here, the readout noise of the RCA CCD is now becoming less significant in comparison to the photon shot noise. In the situation when both chips are, in effect, limited only by shot noise, the S/N of the RCA CCD is better than that of the GEC because it detects more of the incident photons.

Although the curves are of course specific to the characteristics assumed of the two CCDs, and to the values chosen for the exposure period and for the number of pixels over which the object signal is sampled, their general form is, however, representative of the many other curves produced by Martin and Parry to show the dependence of parameters such as the exposure period and CCD readout noise. In interpreting the results, it has to be remembered that FOS was conceived as a means of pursuing survey type work with maximum possible efficiency, and for attempting observations of those objects whose spectra could not realistically be obtained in a reasonable exposure period with a conventional spectrograph. In such programmes, a low S/N will often suffice provided that key spectral lines can be identified (to enable a redshift to be determined for example). An adequate classification of broad feature objects (e.g. QSOs and emission line galaxies) might only require a S/N ~10. In view of this, the GEC CCD was concluded to be the better of the two chips since, over most of the spectral range recorded by FOS, it would be expected to yield an astronomically relevant acceptable S/N within a shorter exposure period compared to that required using the RCA CCD.

From a more practical point of view, the arguments in favour of using the GEC chip were strengthened by its shorter delivery time and its cost; at that time, about four times less than an RCA CCD with a similar blemish specification.

Table 2.1 ESTIMATED FOS SYSTEM EFFICIENCY

		EFFICIENCY AT SAMPLE WAVELENGTHS				
		430 nm	540 nm	700 nm	800 nm	900 nm
Atmosphere (z.d. = 45)		0.66	0.79	0.88	0.90	0.92
Telescope		0.67	0.67	0.67	0.67	0.67
Spectrograph:	First order	0.08	0.38	0.45	0.41	0.34
	Second order	0.25	0.18	-	-	-
RCA SID53612 (reported)		0.75	0.81	0.82	0.62	0.32
GEC P8600 (reported)		0.03	0.20	0.31	0.30	0.10
System total	First order	0.026	0.162	0.217	0.153	0.067
RCA CCD:	Second order	0.082	0.079	-	-	-
System total	First order	0.001	0.040	0.082	0.074	0.020
GEC CCD:	Second order	0.003	0.019	-	-	-

2.6 GEC P8603 CCD

GEC's frame-transfer CCD image sensor was developed at the GEC Hirst Research Centre, Wembley and is currently marketed by English Electric Valve (EEV), Chelmsford. It is primarily intended for TV applications conforming to the European 625-line TV standard, providing 576 lines, each of 385 pixels, in two interlaced fields (Burt, 1980). The image area is 8.5 x 6.4 mm, comparable in size to that available from a 2/3 inch vidicon camera tube.

One of the CCDs in the P8600 series, the P8603, is classed as a 'scientific grade' chip and it is this device which was eventually selected for use in FOS. The silicon die is identical to that used in the earlier P8600 device but its chip carrier packaging is considerably smaller (19.4 x 15 mm compared to the P8600's 38 x 23 mm). It is also tested under cooled, slow-scan, full-frame operating conditions before despatch and graded by the cosmetic quality seen in low light level images with peak signals of ~1000 electrons/pixel.

A schematic of the CCD is shown in Figure 2.4. The design makes use of 3-phase overlapping polysilicon electrode technology (Bertram et al., 1974) and channel-stop diffusions to confine the charge transfer channels. Appropriate biasing of the electrode phases (Ø1, Ø2, Ø3) confines adjacent elements within a charge transfer channel. The electrodes are grouped in the conventional frame-transfer organization, dividing the array into an imaging area, a storage area and an output register to transfer signals serially to the on-chip charge detection amplifier.

The imaging area consists of 288 lines each of 385 pixels (i.e. 385 array columns) and is front-illuminated (i.e. light must pass through the electrode structure). The pixel size is 22 x 22 μm. Burt (1980) has described how, in its use as a TV image sensor, the number of image lines may, in effect, be doubled by collecting alternate frames under IØ1 electrodes and then under IØ2 and IØ3 electrodes. This moves the centres of charge collection back and forth between frames in a 2:1 interlace, thus satisfying the requirements of the standard 625-line interlaced TV picture format; 575 active lines are usually displayed, the remaining 50 are used for the field-blanking periods. When used in the frame-transfer mode, all parts of the array other than the imaging area are optically shielded by an external mask. Anti-blooming control is provided only in the form of a gate-drain diode structure (bias connections: V_{ABG}, V_{ABD}) at the top of the imaging area to 'sink' excess charge that has already spread along columns.

The storage area consists of 290 lines, again, each of 385 elements. The two extra lines are to accommodate any residual charge that might arise through inefficient transfer from the imaging area. Although normally masked, the form and dimensions of the elements are identical to those in the imaging area and can equally well be used to collect photon-generated charge.

GEC P8603 CHARGE COUPLED DEVICE

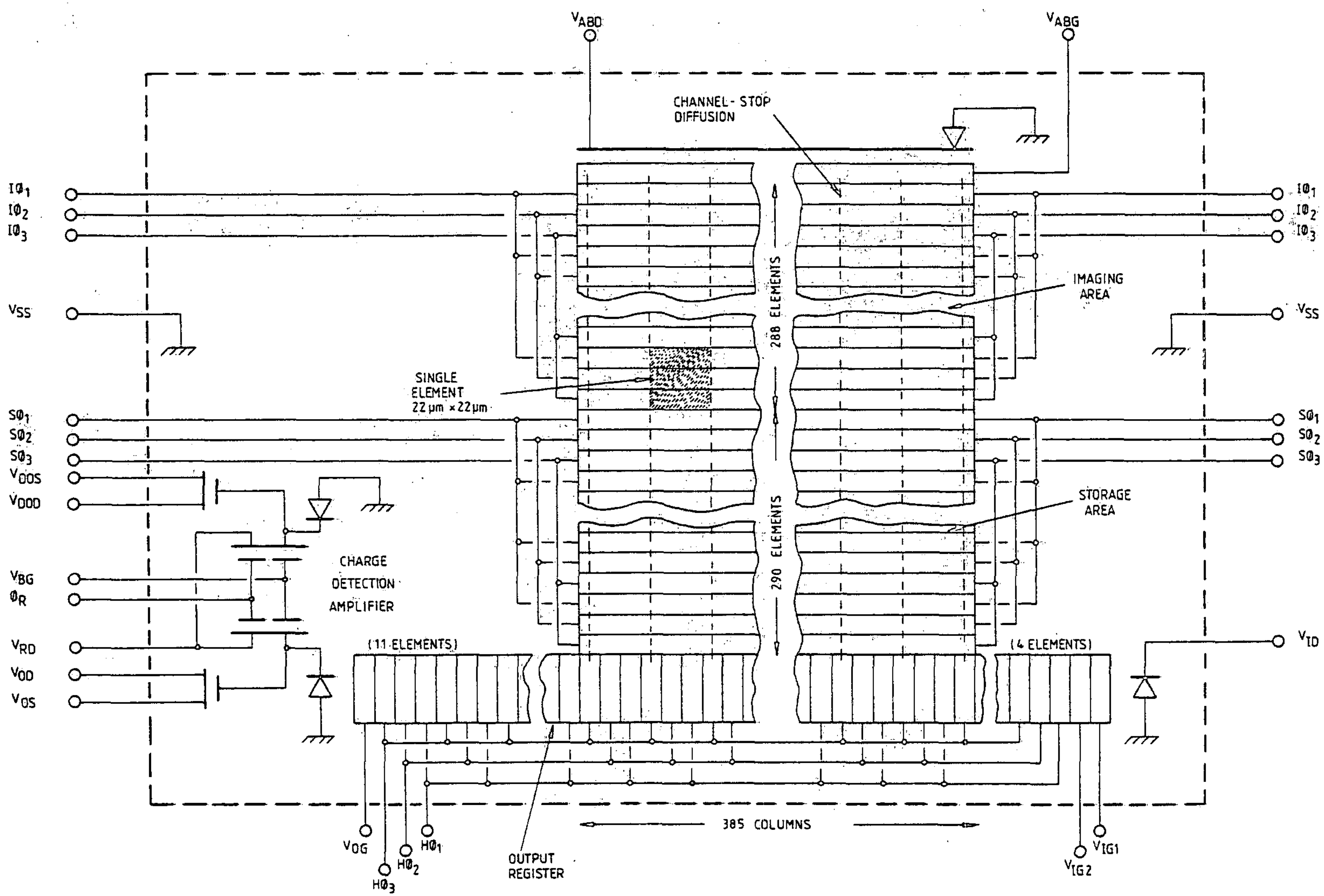


Figure 2.4

The output register has a total of 400 elements, 385 of which are coupled to the array columns. The remaining elements, 11 at the end of the register and 4 at the input, are to allow a 'black' reference level to be established within the video output. Charge may be injected into the register from an input diode for test purposes. For normal operation, however, the diode and the associated gates (bias connections: V_{ID}, V_{IG1}, V_{IG2}) are biased so as to prevent spurious charge input.

The charge detection amplifier is of the 'floating-diffusion' type (see for example: Beynon and Lamb, 1980). A reverse-biased diode located at the end of the output register serves to convert the signal charge extracted from the array into a signal voltage by virtue of its capacitance (~ 0.1 pF). In operation, the diode capacitance is recharged to a reference potential through a transistor switch prior to the deposition of each pixel's charge. An output transistor, operated as a source-follower, buffers the signal voltage on the capacitance, providing a low impedance output to drive external video amplification circuitry.

The GEC CCD operates in the buried-channel mode in which charge transfer takes place inside the substrate and away from surface-state trapping sites at the $Si-SiO_2$ interface (Walden et al., 1972). Fabrication is by ion-implantation of an n-type channel within a p-type substrate with p(+)-type channel-stop diffusions and n-type source and drain diffusions.

The P8603 is built on an epitaxial substrate which consists of a thin (25 μm) surface layer of p-type silicon formed upon a thicker supporting layer of p-type material of far greater doping concentration (EEV Technical Note No. 7, 1982). In such a substrate, any charge carriers created in the underlying highly doped silicon are likely to recombine before they can diffuse to a potential well, i.e. the active thickness of the substrate is, in effect, confined to that of the thin epitaxial layer. This offers two main advantages over a 'bulk' substrate which is uniformly doped throughout its depth (as available in earlier GEC CCDs):

(i) it suffers less image resolution loss from the lateral diffusion of charge created deep inside the substrate by long ($\gtrsim$ 800 nm) wavelength light. This, however, is at the expense of a reduced sensitivity to this light. (Image resolution and responsivity curves for GEC's bulk and epitaxial substrate chips are given in EEV Technical Note No. 7, 1982.)

(ii) it has a lower and different responsivity to cosmic ray particle interactions. In a bulk substrate chip, cosmic ray events appear, generally, as a diffuse charge packet collected over several pixels (see for example: Marcus et al., 1979). The thin epitaxial substrate, however, confines the event to a few pixels, similar in form to those seen in thinned CCDs (see for example: Geary and Kent, 1981).

2.6.1 P8603 Full-Frame Operation

The P8603 CCD is operated in a full-frame imaging mode by removing the external mask normally covering the chip storage area and by making common connections between the corresponding electrode phases of the imaging and storage areas. This enables a continuous photosensitive area of 578 x 385 pixels and size 12.7 x 8.5 mm.

The readout of a full-frame image follows a sequence in which each of the 578 image lines is read out in turn. Each line is, itself, read out in a sequence in which:

(i) the imaging and storage area electrodes are clocked so as to move the image down the array by one line element, the lowest line being transferred into the output register.

(ii) the output register's electrodes are clocked so as to transfer the contents of each of its 400 elements sequentially into the charge detection amplifier.

Full-frame operation of the P8603 is considered in subsequent chapters of this thesis and so in order to make clear the distinction between this and frame-transfer operation, commoned imaging and storage area electrodes will be referred to as 'vertical' electrodes (VØ).

CHAPTER 3

THE CCD CAMERA

3.1 Introduction

This chapter is concerned with the description of a cooled, slow-scan, full-frame imaging CCD camera system. In particular it concentrates upon the electronics to drive the CCD and their control from a computer. Where appropriate the operation of the camera is illustrated with block diagrams while complete circuit details are given in Appendix A.

3.2 Design Goals

The motivation for designing and constructing a CCD camera resulted from the following objectives:

(i) to evaluate the P8603 CCD, confirm its suitability for operation in FOS and investigate the attainment of minimal chip readout noise.

(ii) to facilitate the optical alignment of FOS and to assess its performance before shipment to La Palma.

(iii) to commission FOS on the INT prior to it becoming a common-user instrument.

3.3 Overview of the Laboratory CCD Camera System

The laboratory CCD imaging system is illustrated in Figure 3.1 while a more detailed schematic of the camera electronics is shown in Figure 3.2.

The liquid nitrogen cooled cryostat is designed to accommodate the GEC P8603 CCD image sensor and is fitted with a computer controlled electronic shutter. A temperature controlling circuit mounted adjacent to the cryostat maintains the CCD's nominal operating temperature of 150 K to a stability of better than ±0.05 K.

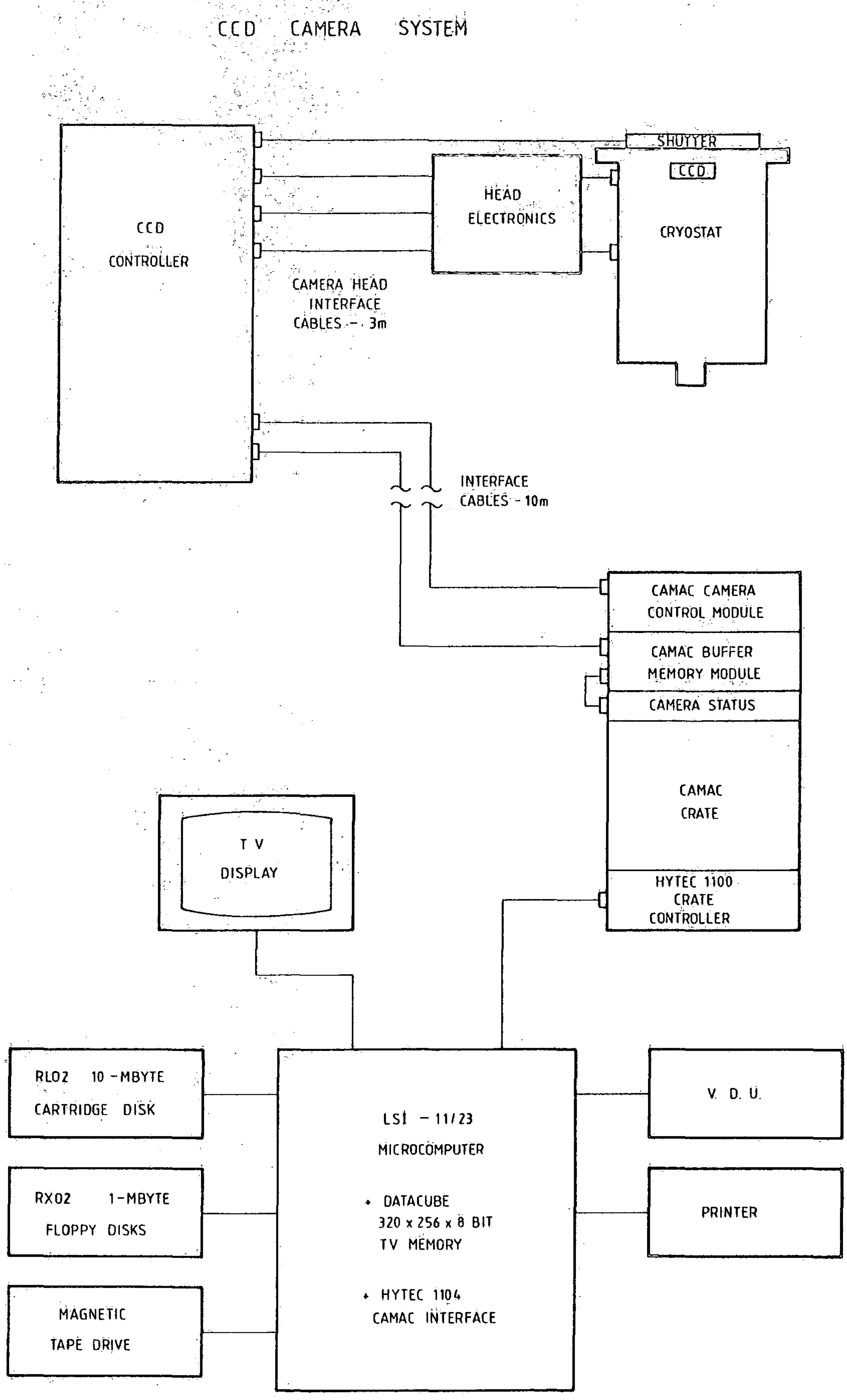

CCD CAMERA SYSTEM
CCD CONTROLLER
HEAD ELECTRONICS
SHUTTER
CCD
CRYOSTAT
CAMERA HEAD INTERFACE CABLES - 3m
INTERFACE CABLES - 10m
CAMAC CAMERA CONTROL MODULE
CAMAC BUFFER MEMORY MODULE
CAMERA STATUS
CAMAC CRATE
HYTEC 1100 CRATE CONTROLLER
T V DISPLAY
RL02 10-MBYTE CARTRIDGE DISK
RX02 1-MBYTE FLOPPY DISKS
MAGNETIC TAPE DRIVE
LSI - 11/23 MICROCOMPUTER
+ DATACUBE 320 x 256 x 8 BIT TV MEMORY
+ HYTEC 1104 CAMAC INTERFACE
V. D. U.
PRINTER

Figure 3.1

CCD CAMERA ELECTRONICS

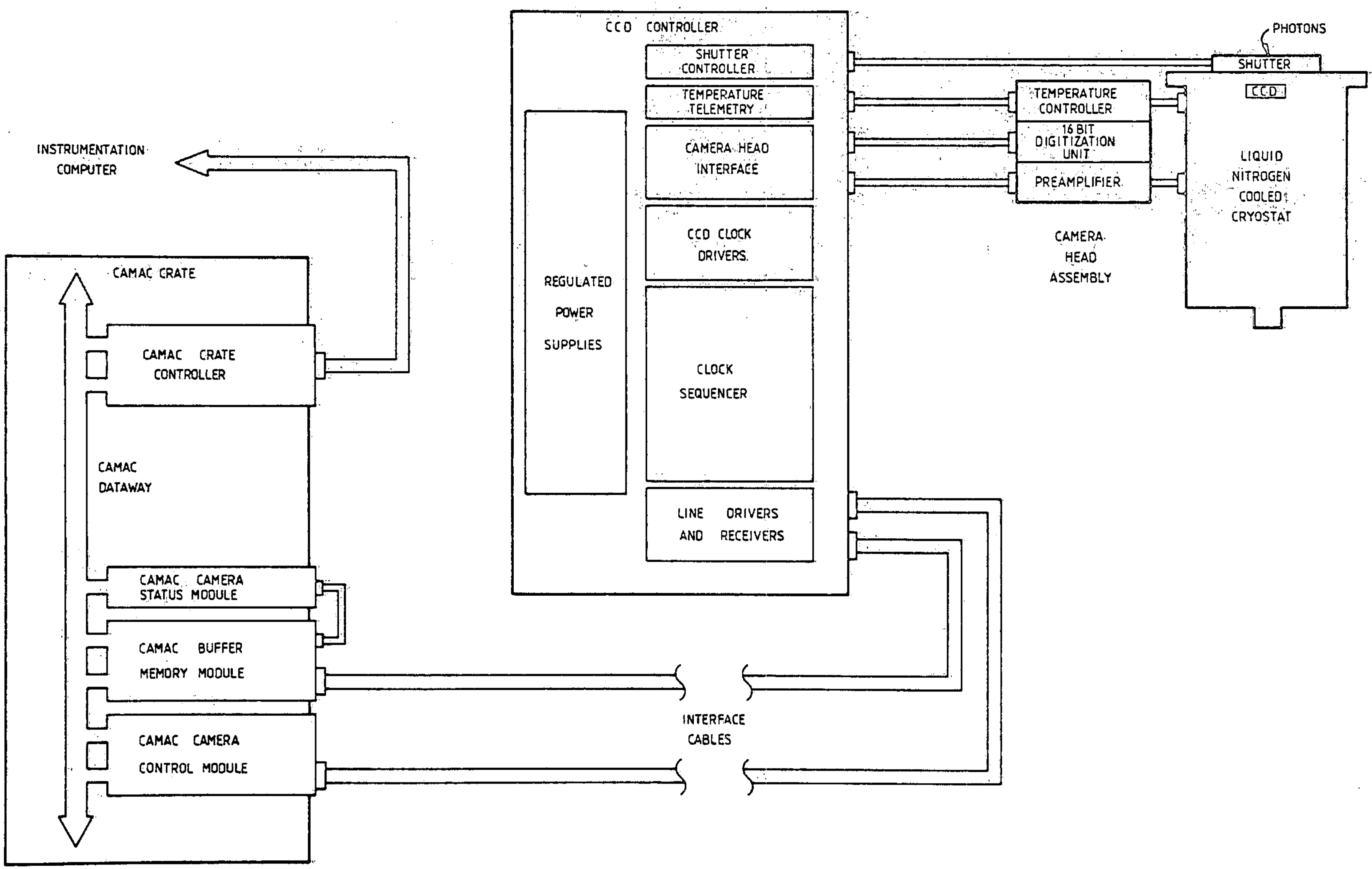


Figure 3.2

The CCD video electronics, including a 16 bit analogue-to-digital converter, are also located at the camera head thereby enabling those cables which convey low-level analogue signals to be of minimal length. The preamplifier incorporates the now well-established correlated double sampling signal processing technique and also the circuitry needed to generate the CCD's DC bias voltage supplies.

The CCD controller (located within 3 m of the camera head) generates all the waveform patterns and control signals needed to operate the camera in a slow-scan imaging mode. The clock sequencer uses a combination of counters and a control register to address EPROMs which are programmed with the waveform patterns required to read out the CCD. Some of its outputs are conveyed to the CCD clock drivers which translate the logic signals from TTL voltage levels to analogue waveforms of appropriate amplitude and shape to drive the CCD's electrodes. Additional waveforms are used to control the video signal processing electronics and to transmit the digitized data to a CAMAC computer interface.

Electronics to control the camera shutter and to provide telemetry of the CCD's operating temperature are also housed within the CCD controller. The chassis is powered from linear voltage supplies with additional regulation provided for those supplies which are conveyed to the camera head.

All communication signals between the CCD controller and the CAMAC interface are transmitted differentially over multiple twisted-pair cabling thereby permitting operation at up to 100 m separation. This capability was designed into the camera specifically for commissioning FOS on the INT, although for convenience the same line driver and receiver components are also used within the laboratory where 10 m cables suffice.

Three CAMAC modules provide a communications interface between the CCD controller and any computer hardware with the capability of driving a CAMAC crate. An interrupt driven handshake, and instructions to control the camera electronics, are conveyed through the CAMAC camera control module. Camera data are transmitted to the CAMAC buffer memory module which provides temporary storage for each line of CCD image data before its subsequent retrieval by the computer. The CAMAC camera status module provides the computer with access to the current state of the camera shutter and of the CCD's operating temperature. Communication signals between the modules and the CCD controller are opto-isolated in order to prevent ground loops and to minimize the feedthrough of noise generated within the computer system.

A DEC LSI-11/23 microcomputer supervises the control of the camera and the acquisition, display and reduction of data. Application programmes are loaded from a DEC RX02 floppy disc drive while CCD images are stored on a DEC RL02 10 Mbyte cartridge disc. Images are displayed on a monochrome TV monitor which is driven from a Datacube digital frame store of 320 x 256 pixels, each to 8 bits depth. Magnetic tape may be used to archive data and also to transfer images to a VAX Starlink computer node for further analysis. The CAMAC crate is connected to the computer through a Hytec 1104 interface card and a Hytec 1100 crate controller module.

The computer runs Fortran software in conjunction with DEC's RT-11 operating system. RT-11 supports the disc and tape drives but additional device handlers had to be written for the CAMAC interface and the Datacube display.

A single menu-driven programme supervises the entire CCD imaging system (Martin, 1980). The camera control commands allow the user to specify the duration of an exposure, the format of the image to be read and the destination for the resulting data, i.e. disc and/or the display. A compiler translates the user's high-level commands to low-level instructions to control the electronics and to schedule the appropriate data storage device(s).

The image display software is tailored to the Datacube and enables the user to display any 8 bits of the original 16 bit video data from any 320 x 256 pixel window of the CCD image. A full-frame image may also be displayed, albeit with a reduction in picture resolution, using a 2:1 image compression. Routines to generate plots through an image are also available and may be used to calculate the FWHM of a feature which facilitates focussing of the detector. A software cursor facility enables the identification of individual pixel data and the marking of features of particular interest.

The data reduction software supports arithmetic operations between images and between an image and a numerical constant thereby enabling flat-fielding and instrumental DC bias frame subtraction. Statistical functions allow the calculation of the mean and variance of any selected pixel matrix for the purposes of photometric calibration of the detector and the measurement of chip readout noise.

3.4 Camera Head Subassemblies

3.4.1 CCD Cryostat

The liquid nitrogen cryostat, shown in cross-section in Figure 3.3, was originally constructed for operation of a cooled Plessey linear diode array on the Wise Observatory's 1m telescope (Campbell, 1981). In modifying the dewar to accommodate the P8603 CCD, the primary design goal was to produce a general purpose test facility for laboratory CCD evaluation, rather than attempting to engineer the system to a level of performance acceptable to telescope operation. In particular:

(i) the mechanical arrangement to support the CCD was designed to facilitate assembly at the expense of rigidity.

(ii) the problem of prolonging the hold-time of the cryostat by minimizing the rate of nitrogen boil-off was not researched in any depth.

The nitrogen coolant is contained within a cylindrical copper bottle which is held inside an evacuated enclosure by its fill-tube assembly and a plastic support ring. A zeolite getter material contained within a sieve mounted below the nitrogen bottle helps to maintain an adequate vacuum inside the cryostat, and thereby prolong the period for which it will operate before re-pumping becomes necessary. Radiation between the outer and inner vessels is reduced by several layers of aluminized Mylar wrapped around their opposing surfaces.

CRYOSTAT

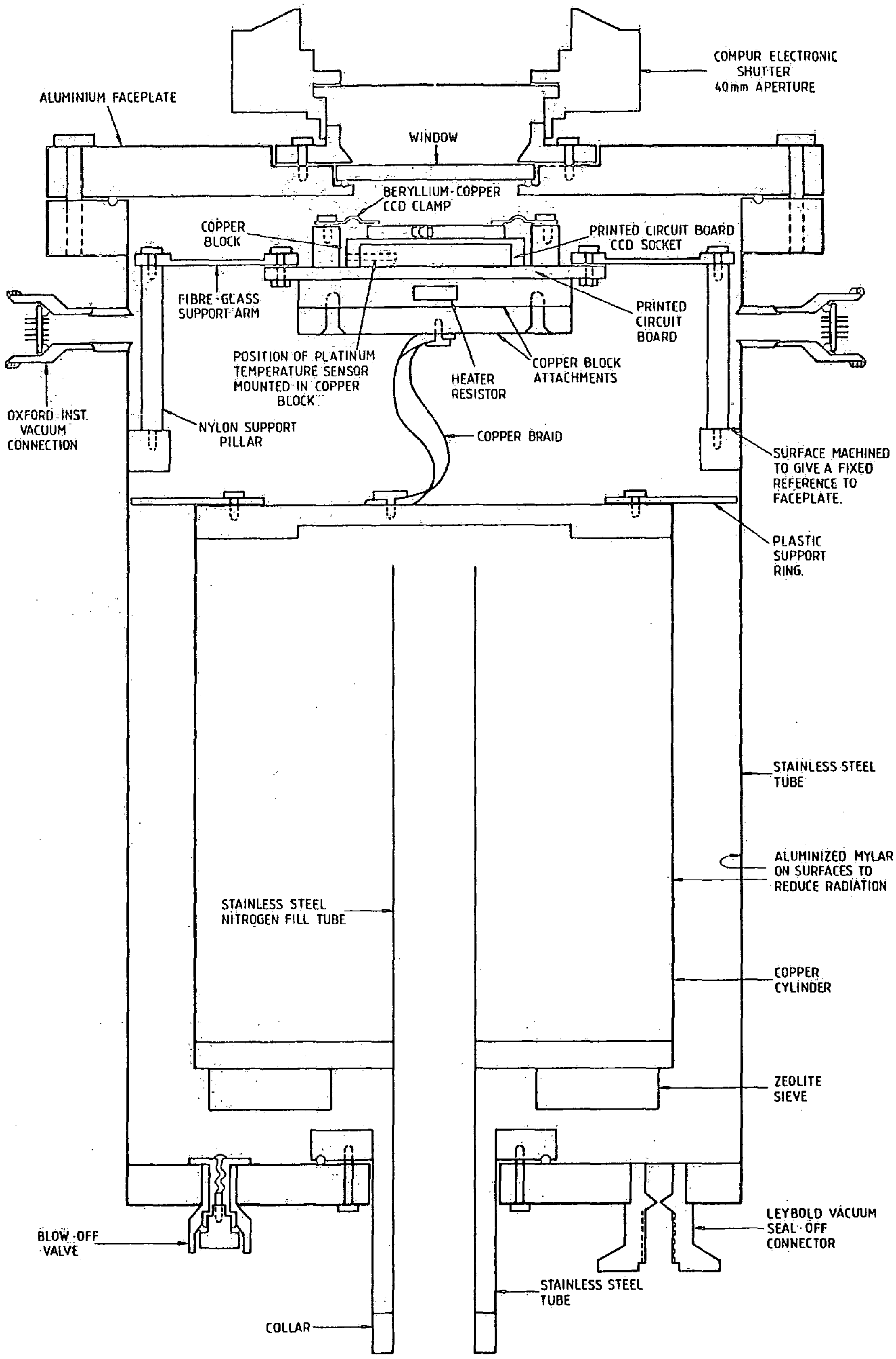


Figure 3.3

The resulting hold-time of the cryostat is 3-4 hours which is rather less than could be hoped for given its 1.5 litres cryogen capacity. This somewhat excessive boil-off rate is largely attributable to thermal coupling through the double-pipe nitrogen fill-tube assembly, despite its fabrication from an austenitic grade of stainless steel of relatively low thermal conductivity. Most of the remaining excess dissipation is a result of radiation from the cryostat faceplate, and could be significantly reduced by fitting a radiation shield between the faceplate and the CCD chip support assembly. Contributions from electrical wires to the CCD and from regulation of the chip's operating temperature were calculated to be minimal by comparison.

The modifications made to the original dewar for CCD operation were:

(i) to construct a cooled support assembly for the P8603 with a printed circuit board to facilitate electrical connections to the chip.

(ii) to incorporate a temperature sensor and a heater resistor within the chip support assembly to allow active regulation of the CCD's operating temperature, in conjunction with servo electronics mounted outside the cryostat.

(iii) to fit a Compur electronic shutter of 40 mm aperture to the cryostat faceplate to allow computer control of an exposure.

The CCD chip is mounted on a shaped two-piece copper block which is cooled by conduction through a flexible copper braid connecting it to the cold face of the nitrogen bottle. Two small clamps are used to hold the CCD against the copper block and thereby ensure a good thermal contact. The thickness and length of copper braid was selected so that without active temperature regulation, the CCD is cooled to ~ 110 K. This value is rather low for optimal performance of the P8603 (see Chapter 5) but provides a wide range for experimentation.

Electrical connections to the CCD are made through a special socket supplied with the chip. This is soldered to a printed circuit board with tracks configured to link those pins which require a common signal; for example, image and storage area drive clock lines. Capacitors for decoupling of DC bias voltage supplies to the chip are also mounted on the PCB. Connections from the PCB to the external camera drive electronics are made through three Oxford Instruments vacuum feedthrough ports.

3.4.2 Temperature Control

The CCD's operating temperature is maintained to within ±0.05 K of a selected value by the servo amplifier shown schematically in Figure 3.4. Its design follows that of a system developed by Jorden et al. (1982) for the AAT CCD camera.

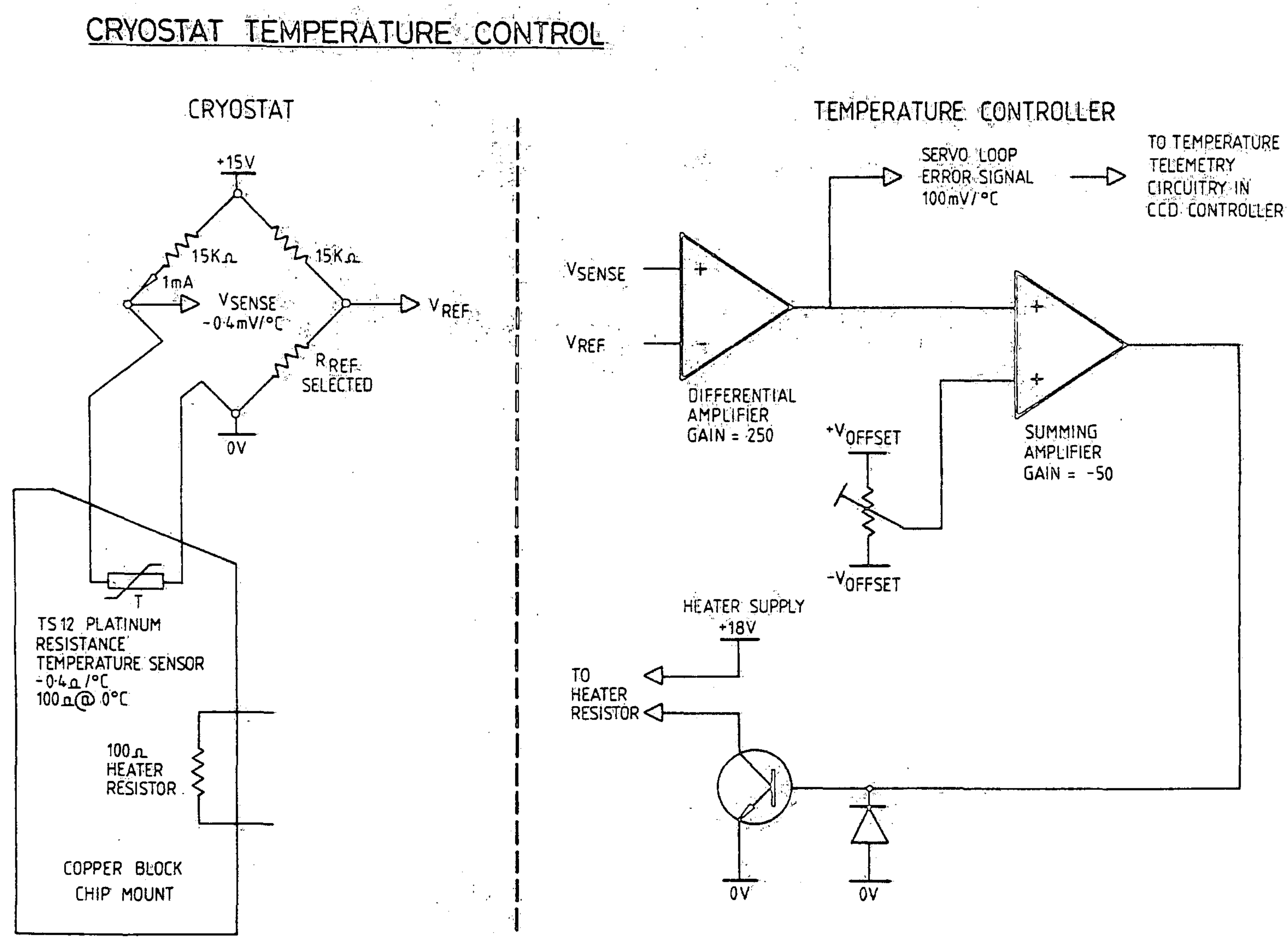
The temperature sense element embedded inside the CCD's support block is an Oxford Instruments platinum resistance thermometer (type TS12). This device has a characteristic temperature coefficient of 0.4 $\Omega/^{o}C$ and a nominal value of 100 Ω at $0^{o}C$. It is operated in one arm of a Wheatstone bridge circuit which is configured to provide a voltage output characteristic (Vsense) of 0.4 $mV/^{o}C$.

The desired CCD operating temperature (To) is defined in the first instance by a selected reference resistor (Rref) which is operated in the opposing bridge arm and which provides a reference voltage (Vref) for comparison with Vsense.

$$\mathrm{Rref}(\Omega) = \frac{\mathrm{To}(K) - 23}{2.5}$$

Optimal performance of P8603 CCDs was obtained at approximately 150 K with Rref = 51 Ω (see Chapter 5).

Vref and Vsense are conveyed to the inputs of the servo electronics mounted adjacent to the cryostat. A first stage differential amplifier (voltage gain = 250) subtracts Vref from Vsense to generate a bridge error signal of 100 $mV/^{o}C$. Measurement of this



CRYOSTAT TEMPERATURE CONTROL
CRYOSTAT
TEMPERATURE CONTROLLER
+15V
15KΩ
15KΩ
1mA
VSENSE
-0·4mV/°C
VREF
RREF
SELECTED
0V
T
TS 12 PLATINUM
RESISTANCE
TEMPERATURE SENSOR
-0·4Ω/°C
100Ω@ 0°C
100Ω
HEATER
RESISTOR
COPPER BLOCK
CHIP MOUNT
SERVO LOOP
ERROR SIGNAL
100mV/°C
TO TEMPERATURE
TELEMETRY
CIRCUITRY IN
CCD CONTROLLER
VSENSE
VREF
+
−
DIFFERENTIAL
AMPLIFIER
GAIN = 250
+
+
SUMMING
AMPLIFIER
GAIN = -50
+VOFFSET
-VOFFSET
HEATER SUPPLY
+18V
TO
HEATER
RESISTOR
0V
0V

Figure 3.4

signal may be used for temperature telemetry about a point relative to the set temperature. The second stage of the servo is a summing amplifier (voltage gain = −50) which allows for fine adjustment of the set temperature (~ ±15^{o}C) relative to that defined by Rref by the addition of a variable offset voltage into the bridge error signal. The resulting output is used to drive a common-emitter transistor which supplies a varying drive current through a 100 Ω heater resistor embedded inside the CCD´s support block. The transistor is biased so that when the bridge is in balance a nominal current of ~ 120 mA flows through the heater thereby dissipating ~ 1.4 W. This current will vary under servo control by ~ ±30 mA so as to compensate for fluctuations in the CCD´s operating temperature.

3.4.3 Preamplifier and Digitization Electronics

The description of the CCD video signal processing and digitization electronics is deferred until Chapter 4 where they will be discussed within the context of P8603 charge detection and signal processing. However, the components of these camera head subassemblies are listed below for reasons of completeness:

(i) CCD preamplifier
- video signal amplification and correlated double sampling circuitry.
- circuitry to generate the CCD´s DC bias voltage supplies.

(ii) digitization unit
- sample-and-hold amplifier.
- 16 bit analogue-to-digital converter.

3.5 CCD Controller Subassemblies

3.5.1 Waveform Generation

The readout of a full-frame image from a P8603 CCD may be considered in terms of two basic ´transfer sequence´ waveform patterns:

(i) a 'vertical transfer sequence'

(ii) a 'horizontal transfer sequence'

The component waveforms required within each of these transfer sequences are outlined below and are illustrated in a timing diagram in Figure 3.5

(i) Vertical transfer sequence

(a) **CCD VERTICAL DRIVE CLOCKS (V∅1, V∅2, V∅3)**

- 3-phase CCD drive clocks to transfer an image charge pattern through the array by one line element.

(b) **RESET CLOCK (∅R)**

- a drive clock to the CCD's charge detection amplifier to clamp the DC potential of the output node during line transfer and to ensure that the node is ready to receive charge from the first pixel when the CCD output register is read out.

(ii) Horizontal transfer sequence

(a) **CCD HORIZONTAL DRIVE CLOCKS (H∅1, H∅2, H∅3)**

- 3-phase CCD drive clocks to transfer charge along the CCD output register by one pixel element.

(b) **RESET CLOCK (∅R)**

- to recharge the output node so that it is ready to receive charge from the next pixel.

(c) **INTEGRATOR (RAMP-UP), INTEGRATOR (RAMP-DOWN)**

- timing signals associated with the video signal processing electronics. The output node is sampled before and after signal charge is transferred into it by **RAMP-UP** and **RAMP-DOWN** respectively (see Chapter 4).

VERTICAL AND HORIZONTAL TRANSFER SEQUENCES

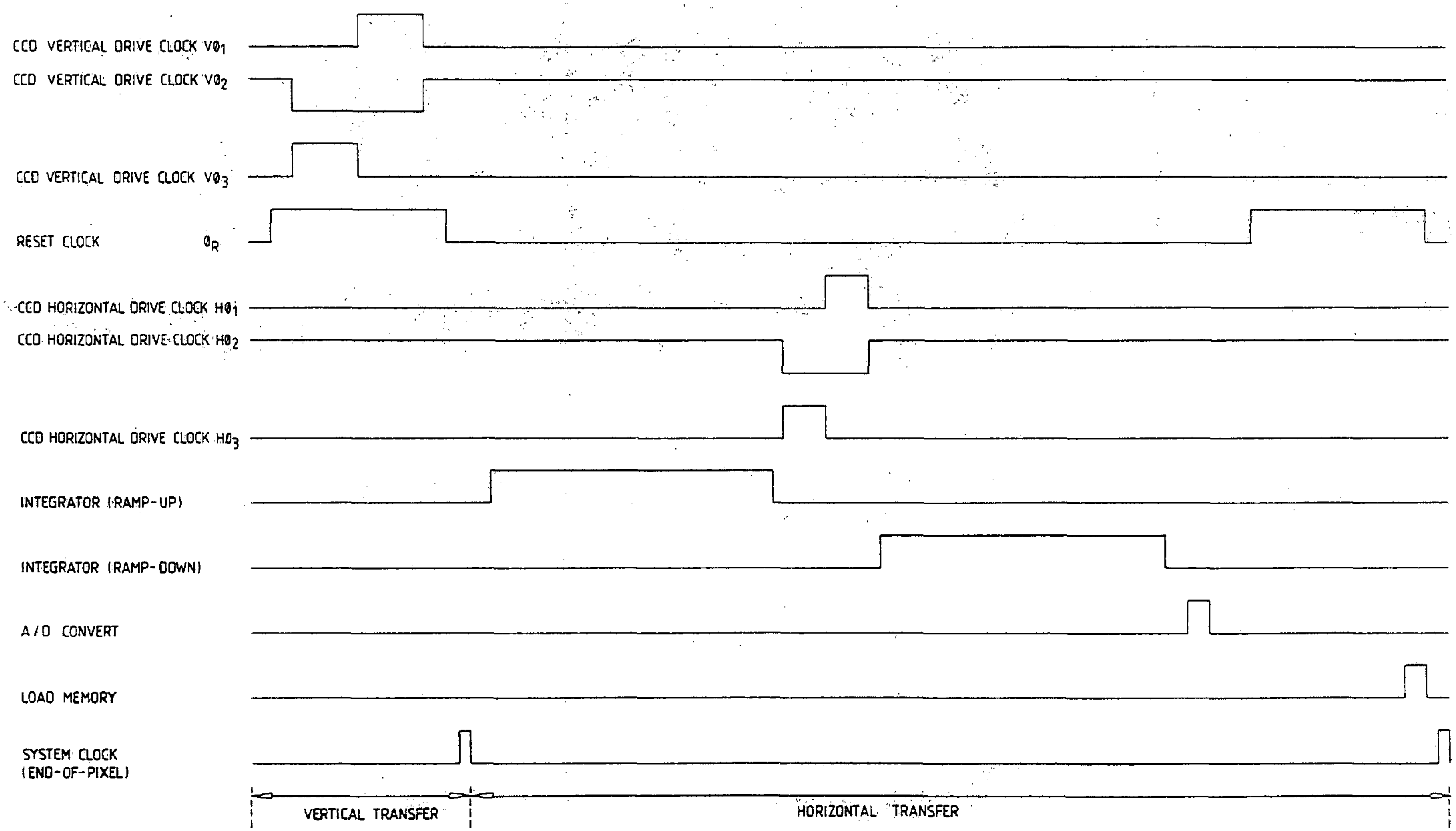


Figure 3.5

(d) A/D TRIGGER

- initiates analogue-to-digital conversion of the sampled video signal.

(e) LOAD MEMORY

- strobes the digitized pixel data to the computer interface.

The readout of each line of a P8603 CCD image requires that vertical and horizontal transfer sequence waveforms are generated within a higher order sequence which consists of:

(i) a single vertical transfer sequence

(ii) 400 consecutive horizontal transfer sequences.

This sequence will be referred to as a 'one-line-sequence' and is illustrated in Figure 3.6.

Electronics to generate waveform patterns similar to those outlined above have been described by several groups; see for example: Marcus et al. (1979); Gunn and Westphal (1981); Loh (1981); McLean et al. (1981); Wright and Mackay (1981); Jorden et al. (1982); Gudehus and Hegyi (1985). The systems described by Marcus et al. and Gunn and Westphal are of particular interest since they highlight extremes in the sophistication of waveform generating circuitry.

Gunn and Westphal described a CCD camera developed at the California Institute of Technology in which the CCD readout waveforms are generated from hardwired logic. A counter-divider chain and wire-wrapped programmed RS flip-flops are used to define waveforms of the desired duration and phase. The limitation of this and of hardwired solutions in general, however, is that changing the timing of an individual waveform necessitates rewiring the logic and therefore makes the evaluation of different or phase-adjusted waveform patterns rather tedious.

ONE - LINE - SEQUENCE TIMING

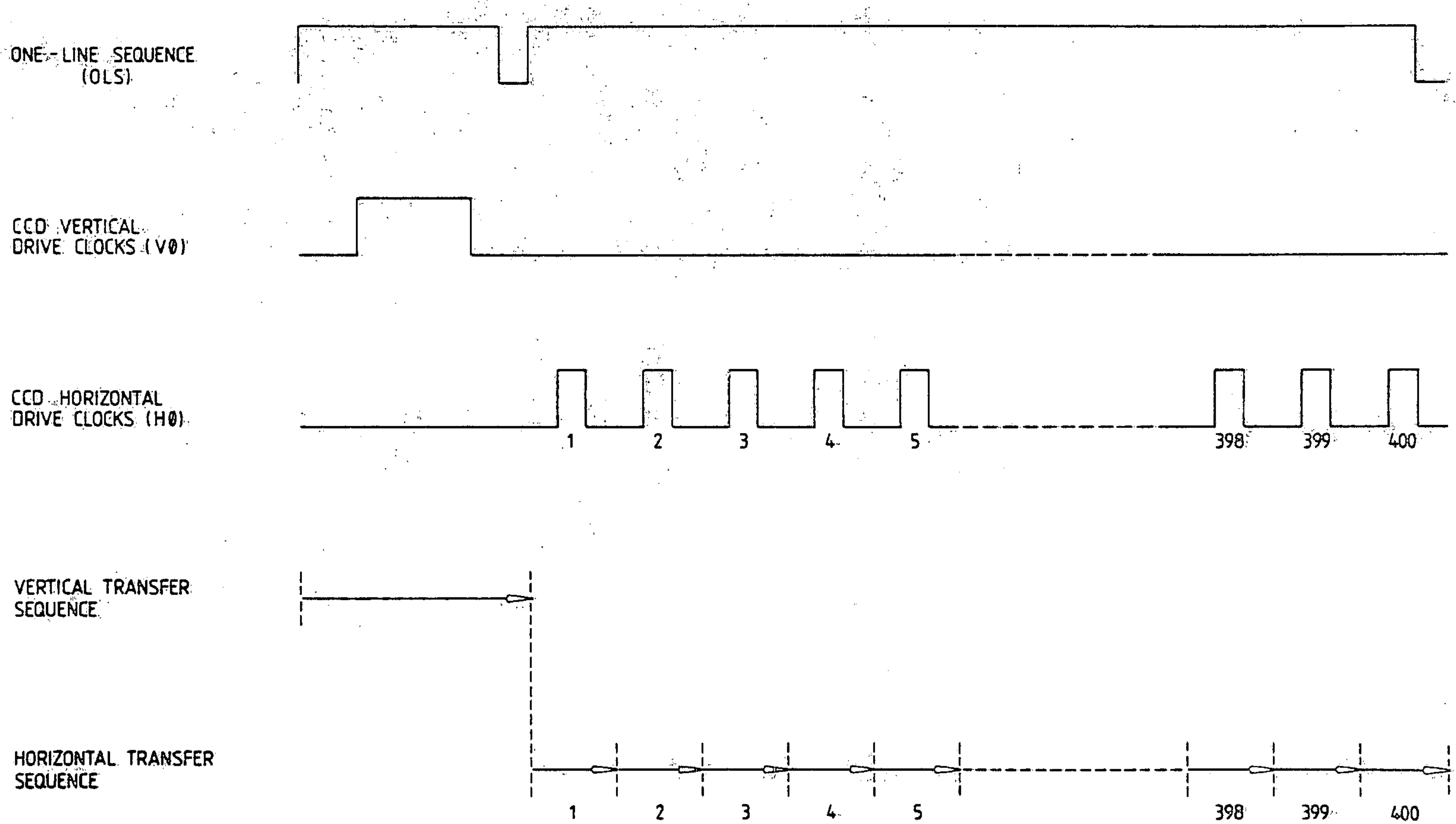


Figure 3.6

In contrast, the CCD camera developed at KPNO is designed to facilitate waveform modification (Marcus et al, 1979). Data corresponding to the desired waveform patterns are compiled within the control software of a host computer and downloaded into the read-write memory of a bit-slice microprocessor sequencer. Waveforms may be modified by editing the software at the computer terminal and downloading the new data into the microprocessor's memory. The advantage of this system, therefore, is the convenience of defining waveform patterns in software; its disadvantage is the elaborate logic circuitry required to support the bit-slice microprocessor electronics. There was neither the expertise nor sufficient time available to develop a similar design for the FOS CCD camera. Instead, a sequencer was designed to satisfy the following requirements:

(i) vertical and horizontal transfer sequence waveforms to be generated within a higher order one-line-sequence pattern.

(ii) waveforms to be programmable without resorting to modification of hardwired logic.

(iii) the overall waveform sequencing logic to be a relatively simple hardwired solution without resorting to bit-slice microprocessor techniques.

3.5.2 Clock Sequencer

A block diagram of the clock sequencer logic is shown in Figure 3.7. Data corresponding to the vertical and horizontal transfer sequence waveform patterns are stored within a 24 bit wide, 2K bit deep, 'erasable programmable read-only memory' (EPROM). This permits the modification of waveform timing by the erasure and reprogramming of appropriate EPROM. The memory is addressed by the combined output of two sources:

(i) the vertical transfer control logic: A8-A10

(ii) the address counter: A0-A7

CCD CLOCK SEQUENCER

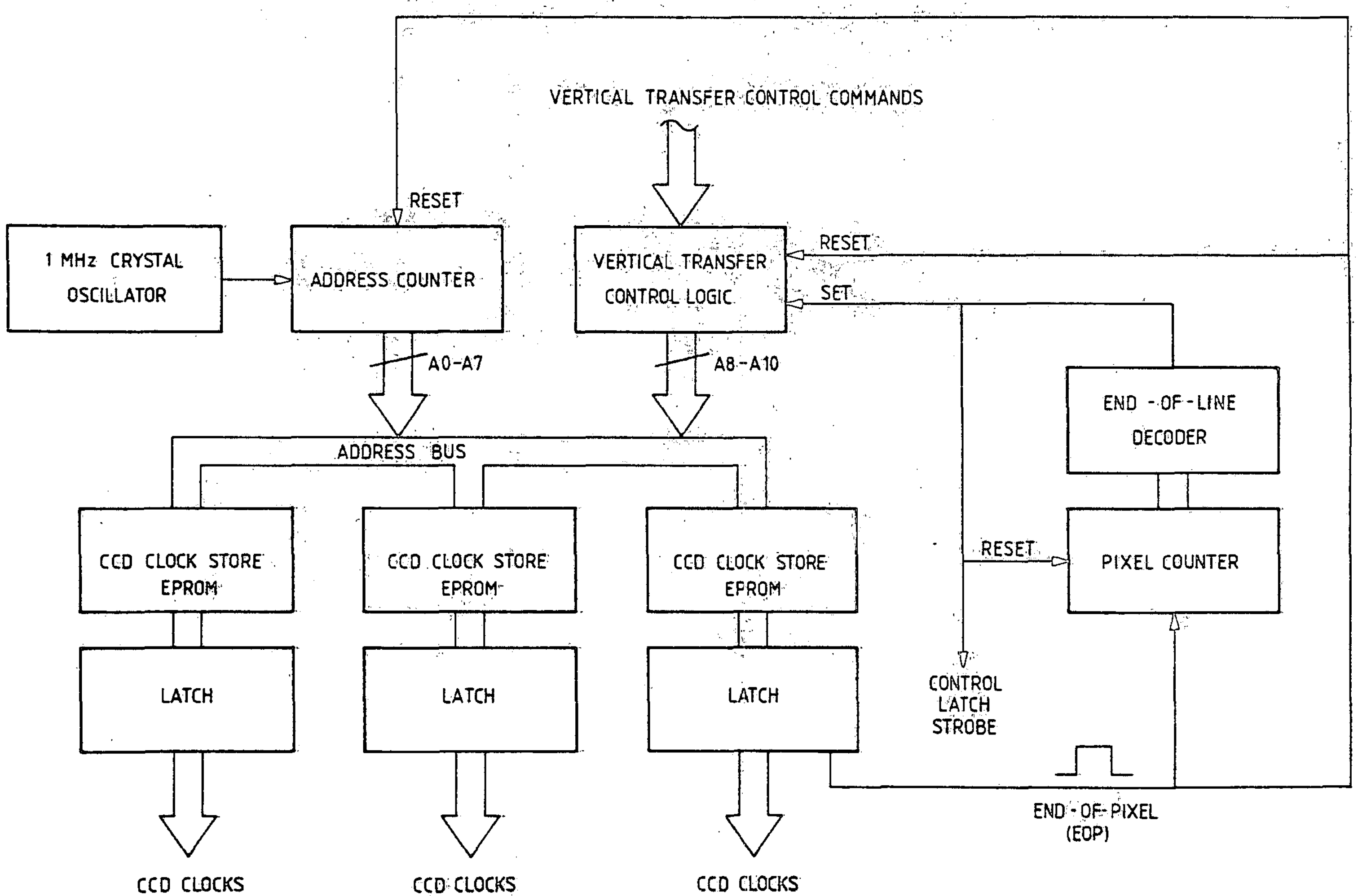


Figure 3.7

Address lines A8–A10 subdivide the memory into a series of 'fields' each of which is programmed with a transfer sequence waveform pattern as illustrated in Figure 3.8. Waveforms are strobed out of the memory by the address counter, the outputs of which increment sequentially through lower order address lines A0–A7. The counter is clocked by a 1 MHz crystal oscillator and so the minimum duration possible for a waveform state is 1 μs. Each data word is latched as it is strobed out of the memory to ensure that the waveforms remain stable as the memory address changes.

The generation of a one-line-sequence from an assembly of a vertical transfer sequence and of repeated horizontal transfer sequences is described below; an accompanying timing diagram is shown in Figure 3.9.

A horizontal transfer sequence waveform pattern is strobed out of the memory as the address counter increments from address A0–A10=0 onwards. One of the clocks generated by the sequencer, **END-OF-PIXEL** (EOP), is dedicated to system control. The memory is programmed so that an EOP pulse is generated at the end of the horizontal transfer sequence (Figure 3.5). It has two functions:

(i) it resets the address counter to zero.

(ii) it increments a second counter, the pixel counter, which registers the number of horizontal transfer sequences generated within the current one-line-sequence period.

By resetting the address counter, EOP initiates the generation of a second horizontal transfer sequence. Waveform sequencing repeats with EOP incrementing the pixel counter each time a horizontal transfer sequence is completed.

The outputs from the pixel counter are fed to the end-of-line decoder logic. This provides an output signal, **CONTROL LATCH STROBE**, which changes state when the number of horizontal transfer sequences required of the one-line-sequence have been generated (400 in the case of the P8603 CCD). The decoder is switch

CLOCK SEQUENCE MEMORY - TRANSFER SEQUENCE FIELDS

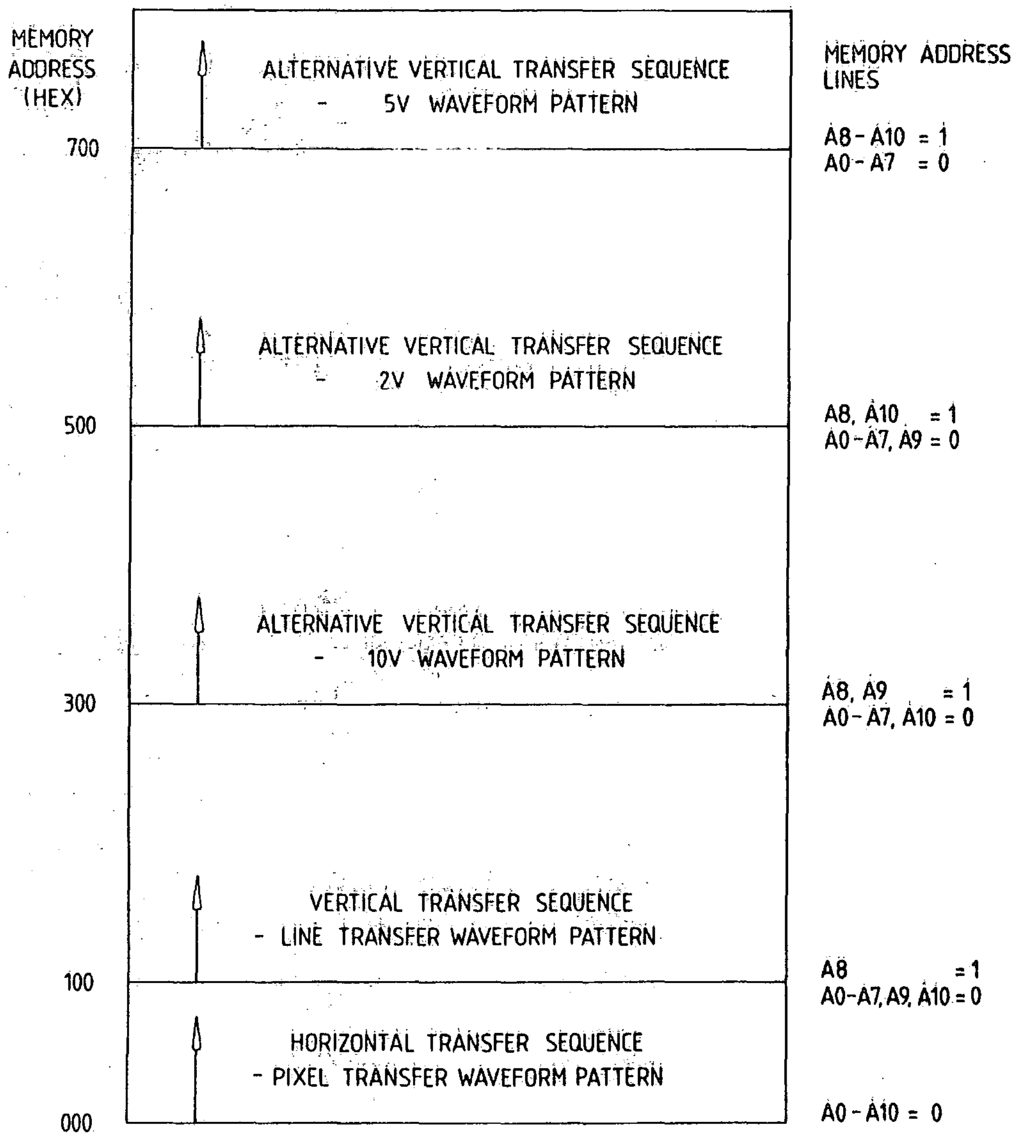


Figure 3.8

CLOCK SEQUENCER TIMING

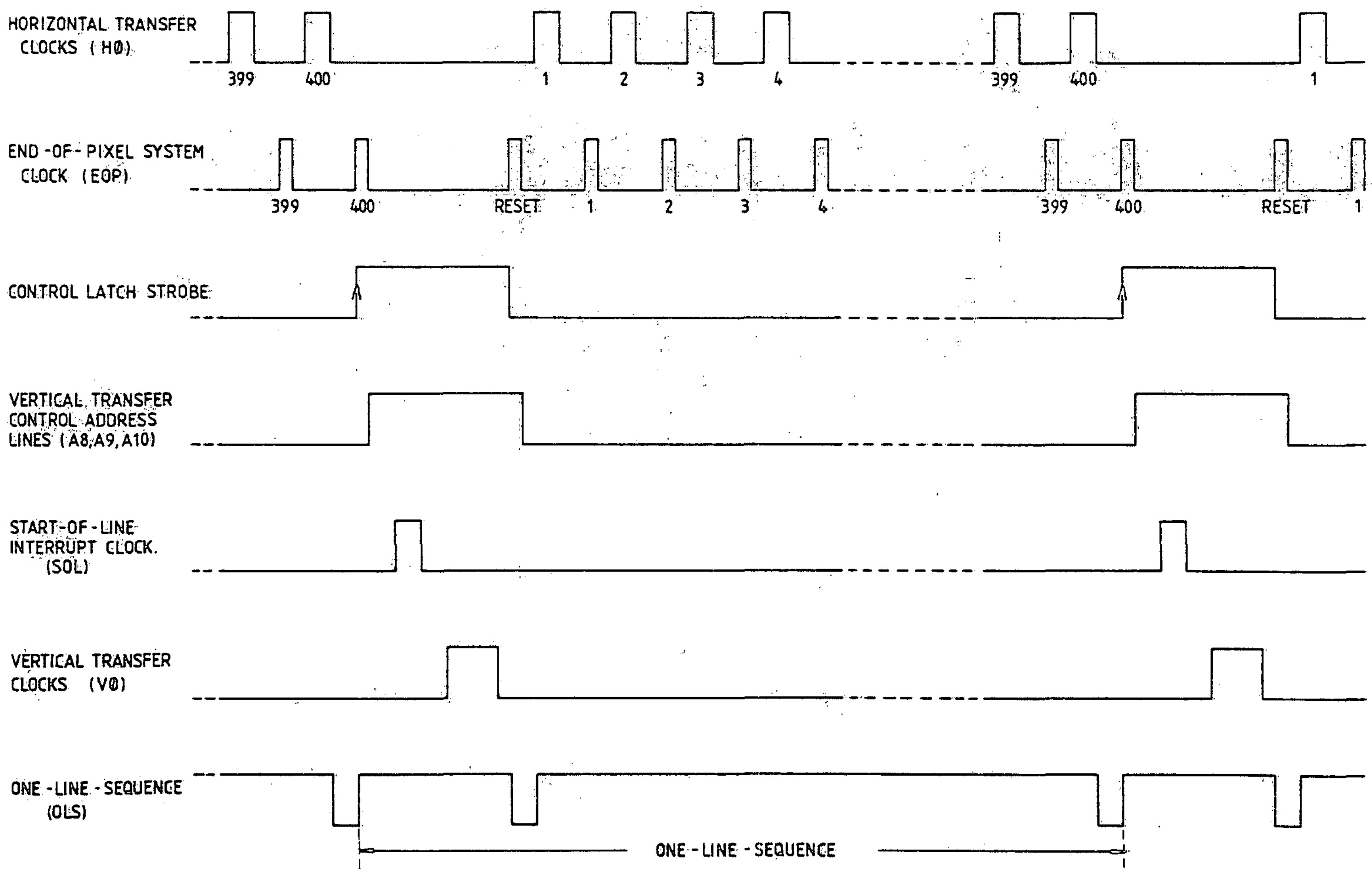


Figure 3.9

programmable to cater for operation of other manufacturers' CCDs having a different image format, for example the RCA SID53612 with 320 pixels per line.

The assertion of the CONTROL LATCH STROBE is defined as the start of a new one-line-sequence period (Figure 3.9). Its low-to-high transition sets a latch within the vertical transfer control logic, the output of which asserts memory address line A8=1. Since the last EOP pulse has reset the address counter, the memory is now sequenced from address A8=1, A0-A7=0 onwards. This field contains the vertical transfer sequence waveform pattern which is now strobed out of the memory. An EOP pulse is also used to mark the end of this transfer sequence (Figure 3.5) although its action is slightly different:

(i) It resets the address counter as before.

(ii) It resets the pixel counter rather than incrementing it by virtue of the state of CONTROL LATCH STROBE on the counter reset line during the vertical transfer sequence (Figure 3.9).

(iii) It resets the latch within the vertical transfer control logic and thereby resets memory address line A8=0.

The memory is now sequenced from address A0-A10=0 onwards, the start of the first horizontal transfer sequence of the new one-line-sequence.

The transfer sequence waveform patterns currently programmed into the sequencer EPROMS to run the P8603 CCD have readout times of:

(i) 60 μs for a horizontal transfer sequence

(ii) 20 μs for a vertical transfer sequence

The duration of a one-line-sequence period is therefore:

$$20\ \mu s + (400 \times 60\ \mu s) \simeq 24\ ms$$

Figure 3.8 shows that the sequencer memory is also programmed with a series of 'alternative vertical transfer sequences' in higher order address fields. One of these transfer sequences may be generated in place of the normal (default) vertical transfer sequence by operating the sequencer in a special mode in which address lines A9 and/or A10 are asserted with A8. These address lines are set by an external control input to the sequencer; the vertical transfer control logic ensures that they are only asserted when A8=1. The waveform patterns generated within each of the alternative vertical transfer sequences are outlined below:

(i) 10V waveform pattern: A8=1, A9=1, A10=0

- a sequence of 10 3-phase **VERTICAL CCD DRIVE CLOCKS** are generated thereby binning 10 CCD image lines within the CCD output register before line readout. This sequence may be used to effect an increased rate of charge erasure from the chip prior to an exposure.

(ii) 2V waveform pattern: A8=1, A9=0, A10=1

- a sequence of 2 3-phase **VERTICAL CCD DRIVE CLOCKS** are generated. This transfer sequence has no immediate application but was included for future investigation of line binning during chip readout.

(iii) 5V waveform pattern: A8=1, A9=1, A10=1

- a sequence of 5 3-phase **VERTICAL CCD DRIVE CLOCKS** are generated. Again, this transfer sequence has no immediate application.

3.5.3 Camera Control

The exposure and subsequent full-frame readout of a cooled CCD follows a sequence (noted in Chapter 2) in which:

(i) the CCD is read out several times prior to an exposure in order to clear any residual charge.

(ii) the **VERTICAL CCD DRIVE CLOCKS** (**V∅**) to the array imaging area are inhibited. The camera shutter is opened for the desired exposure period during which an image charge pattern is collected.

(iii) each line of the image charge pattern is read out in turn. The digitized video data are sent to a host computer for storage, display and analysis.

This sequence may be realized by appropriate control and gating of transfer sequence waveforms.

A block diagram of the camera control system is shown in Figure 3.10. The waveforms generated by the clock sequencer are bussed to electronics subassemblies within the CCD controller; specifically:

(i) CCD drive waveforms to the clock driver control logic through which they are gated to the CCD clock drivers.

(ii) video signal processing and digitization control clocks to the preamplifier clock drivers for transmission to the camera head.

(iii) **LOAD MEMORY** clocks to the camera data interface to strobe data to the computer's CAMAC buffer memory module interface.

Camera control is provided by the host computer's data acquisition software. The synchronization required between real-time programme execution and waveform generation is accomplished with a control handshake which consists of:

(i) an interrupt input to the computer through a CAMAC interrupt facility by a system clock, **START-OF-LINE**, generated at the beginning of each one-line-sequence period (Figure 3.9).

(ii) the execution of an interrupt service routine within the computer's data acquisition programme. The routine tests real-time condition flags within the overall programme structure to determine what control action is required.

CCD CAMERA CONTROL SYSTEM

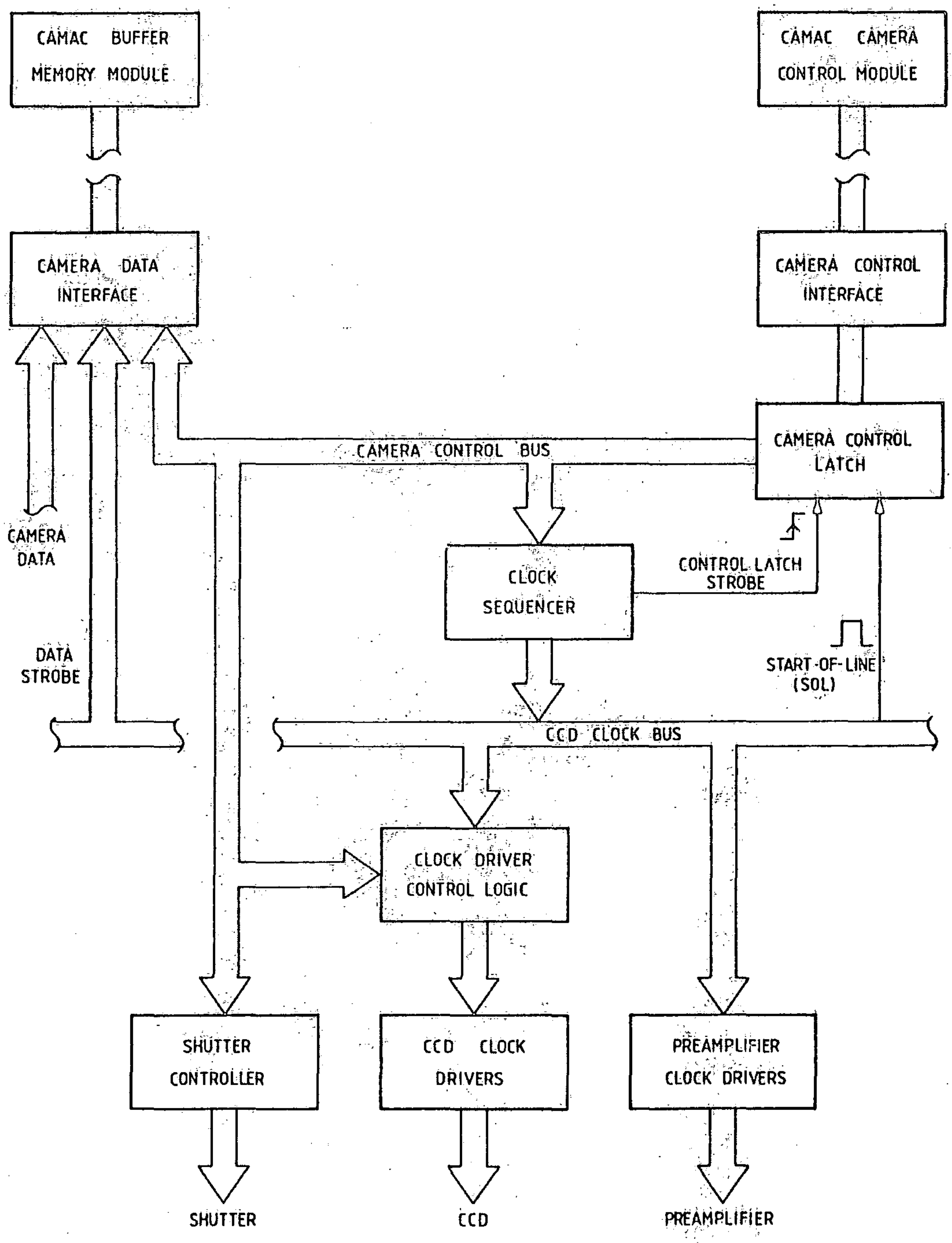


Figure 3.10

(iii) the output from the computer of a 16 bit wide camera control instruction. Each bit of the instruction controls a specific feature of the electronics hardware; a description of the control assigned to each bit is given in Table 3.1.

Because of the asynchronous nature of a software interrupt service routine, it is inevitable that there will be an ill-defined period between the arrival of an interrupt and the availability of the control output. The instruction data are therefore passed through a double-latch control pipeline (Figure 3.11) which synchronizes the control to the beginning of a one-line-sequence period.

In response to, for example, the nth interrupt input to the computer, the control software generates a camera control instruction appropriate to the control action required during the (n+1)th one-line-sequence period. The computer loads the instruction into a storage register within the CAMAC camera control module where it is held until updated. The only constraint upon the timing of this operation is that the data are loaded into the register during the nth one-line-sequence period and before the arrival of the (n+1)th interrupt.

At the beginning of the (n+1)th one-line-sequence, **CONTROL LATCH STROBE** causes the contents of the storage register to be copied into a control register within the camera control latch subassembly. The control, which is now synchronized to waveforms generated within the (n+1)th one-line-sequence period, and which is operative for its duration, is bussed from the outputs of the control register to electronics subassemblies within the CCD controller, specifically:

(i) commands to the clock driver control logic to enable CCD drive waveforms through to the clock driver circuitry.

(ii) commands to the sequencer to generate alternative vertical transfer sequence waveforms.

(iii) commands to the camera data interface to enable **LOAD MEMORY** clocks to strobe data into the CAMAC buffer memory module.

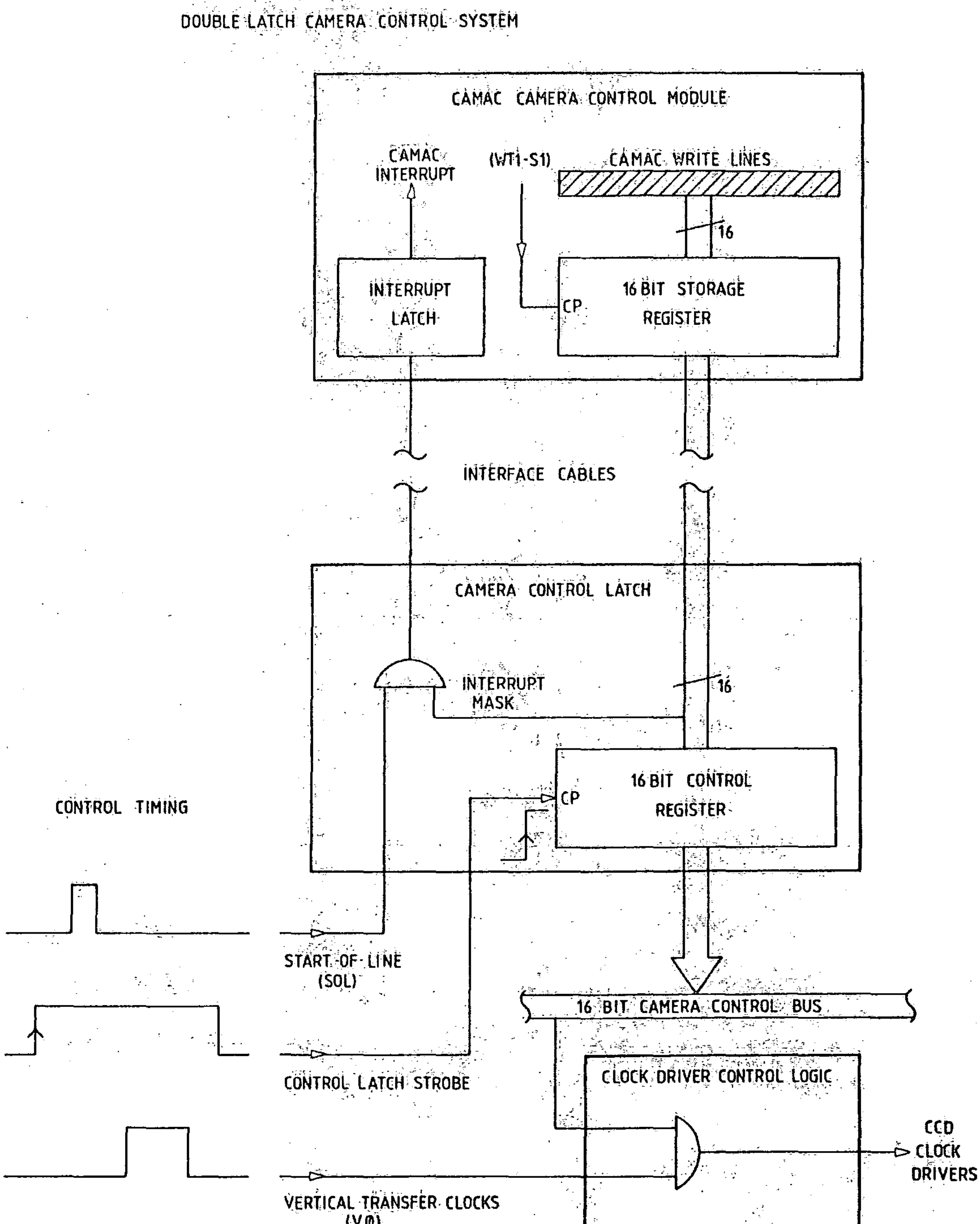

DOUBLE LATCH CAMERA CONTROL SYSTEM
CAMAC CAMERA CONTROL MODULE
CAMAC INTERRUPT
(WT1-S1)
CAMAC WRITE LINES
16
INTERRUPT LATCH
CP
16 BIT STORAGE REGISTER
INTERFACE CABLES
CAMERA CONTROL LATCH
INTERRUPT MASK
16
CONTROL TIMING
CP
16 BIT CONTROL REGISTER
START-OF-LINE (SOL)
16 BIT CAMERA CONTROL BUS
CONTROL LATCH STROBE
CLOCK DRIVER CONTROL LOGIC
CCD CLOCK DRIVERS
VERTICAL TRANSFER CLOCKS (VØ)

Figure 3.11

(iv) commands to operate the camera's electronic shutter.

The use of two registers within the control pipeline is necessary because control instruction data must not change midway through the readout of a CCD image line. This system gives rise to deferred control action in which the nth interrupt requests control for the (n+1)th one-line-sequence period and must be allowed for within the control software. However, it has the advantage of allowing the software sufficient time to acknowledge the interrupt and load the appropriate control instruction data into the CAMAC camera control module before it is required to become operative.

Table 3.1 CAMERA CONTROL INSTRUCTION BIT ASSIGNMENT

Bit 1: **ENABLE INTERRUPTS**

- unmasks a gate within the camera control latch subassembly to enable the START-OF-LINE interrupt pulse from the sequencer through to the interrupt input circuitry within the CAMAC camera control module (Figure 3.11).

Bit 2: **VERTICAL TRANSFER ENABLE**

- unmasks gates within the clock driver control logic to enable **VERTICAL CCD DRIVE CLOCKS (VØ)** through to the CCD clock drivers and thereby enable line transfer through the CCD imaging area (Figure 3.11).

Bit 3: **LOAD MEMORY ENABLE**

- unmasks gates within the camera data interface to enable **LOAD MEMORY** clocks to strobe digitized pixel data into the CAMAC buffer memory module (Figure 3.10). Bit 3 is normally set with bit 2 during line readout of an image charge pattern.

Bit 4: **SPARE**

- those bits which are designated as spare remain available from the camera control bus for future expansion of the system.

Bit 5: **SPARE**

Bit 6: **HORIZONTAL RESET**

- permits masking of the **HORIZONTAL CCD DRIVE CLOCKS (HØ)** from the CCD clock drivers thereby inhibiting readout of the CCD output register.

Bit 7: **INTEGRATE/CLOCKING**

- enables the upper level of **VERTICAL CCD DRIVE CLOCKS** to be switched to a second voltage reference (see 3.5.5 CCD Clock Drivers).

Bit 8: VERTICAL CLOCK PHASE

- enables the direction in which an image charge pattern is transferred through the array to be reversed, i.e. charge is clocked away from the CCD output register rather than towards it.

Bit 9: 10V TRANSFER ENABLE

- sets the clock sequencer to the special mode in which 10 3-phase VERTICAL CCD DRIVE CLOCKS are generated at the beginning of a one-line-sequence period.

Bit 10: ALTERNATIVE VERTICAL TRANSFER ENABLE

- enables 5 3-phase VERTICAL CCD DRIVE CLOCK waveform generation within a one-line-sequence if set with bit 9.
- enables 2 3-phase VERTICAL CCD DRIVE CLOCK waveform generation within a one-line-sequence if set without bit 9.

Bit 11: OPEN SHUTTER

- activates a control line to the shutter controller to open the shutter.

Bit 12: CLOSE SHUTTER

- activates a control line to the shutter controller to close the shutter.

Bit 13: SPARE

Bit 14: SPARE

Bit 15: SPARE

Bit 16: SPARE

3.5.4 Computer Camera Control of a CCD Exposure

The computer's control of an exposure and the subsequent readout of a full-frame CCD image is outlined below. Taking each stage of the sequence in turn:

(i) Erasure of residual charge

Several full-frame readouts of the CCD in preparation for an exposure ensures the erasure of any residual charge from the array imaging area. Since this operation reduces the overall time for which the CCD may be employed for useful observation, it is desirable to reduce its execution time to a minimum. This may be accomplished by operating the sequencer in the special mode in which 10 3-phase **VERTICAL CCD DRIVE CLOCKS** are generated at the beginning of a one-line-sequence, thereby effectively increasing the rate of line readout by 10 times that of normal line readout. Running the P8603, a total line transfer equivalent to the readout of 5 full-frame images is obtained by sequencing 289 consecutive one-line-sequences with the following bits set within the camera control instruction:

Bit 1: **ENABLE INTERRRUPTS**

- to maintain a programme count of how many one-line-sequences have been generated.

Bit 9: **10V TRANSFER ENABLE**

Under routine observing conditions, the data obtained from an erasure has no useful application and is therefore not sent to the host computer.

(ii) Exposure

Camera control of an exposure follows a sequence in which:

(a) line transfer is inhibited.

(b) the camera shutter is opened for the desired exposure period using camera control instruction bits 11 (OPEN SHUTTER) and 12 (CLOSE SHUTTER).

Line transfer is automatically inhibited by the default of not enabling the VERTICAL CCD DRIVE CLOCKS. In the absence of ´clocking luminescence defects´ (see Chapter 5), it is normal to run the output register HORIZONTAL CCD DRIVE CLOCKS (HØ) continuously during an exposure as this will clear any charge which might arise from spurious injection either from the serial input circuitry, the charge detection amplifier or from dark current within the output register itself. If clocking luminescence defects are present, the HØ clocks can be inhibited during the exposure by setting bit 6 (HORIZONTAL RESET) within the camera control instruction.

The host computer´s internal system clock is used to time the exposure period. Interrupt input to the computer is inhibited during the exposure thereby releasing the control programme to other tasks; for example, the display and reduction of previously acquired data.

(iii) Full-frame readout and data acquisition

The control of full-frame readout can be considered as a procedure of consecutive line readout operations for each of which:

(a) the image is transferred through the array by a single line element so that the lowest line is clocked into the CCD output register.

(b) digitized pixel data generated by the sequential readout of the CCD output register are strobed into the CAMAC buffer memory module.

(c) further line readout is inhibited.

(d) the data are retrieved from the buffer memory by the computer for storage and/or display.

(e) line readout is re-enabled for the retrieval of the next image line.

The computer must retrieve the data of one line before initiating the readout of the next because of the somewhat ´primitive´ design of the CAMAC buffer memory module as a single channel read-write memory (see 3.6.3 CAMAC Buffer Memory Module).

To start the readout sequence, the computer´s control software enables START-OF-LINE interrupts so that real-time programme execution can synchronize to one-line-sequence waveform generation. The camera control required for retrieving each image line is best described by considering the control action within consecutive one-line-sequence periods. An accompanying timing diagram is shown in Figure 3.12.

(a) nth interrupt input to the computer

In this example, it will be assumed that image line m is to be read out of the CCD during the (n+1)th one-line-sequence period. Therefore the nth interrupt input to the computer has to be recognized by the control software as a request for control appropriate to line readout during the (n+1)th one-line-sequence period. A camera control instruction with the following control bits set is required:

Bit 1: **ENABLE INTERRUPTS**

- to maintain synchronization of real-time programme execution.

Bit 2: **VERTICAL TRANSFER ENABLE**

- to enable a single line transfer at the beginning of the (n+1)th one-line-sequence.

Bit 3: **LOAD MEMORY ENABLE**

- to enable (n+1)th one-line-sequence period LOAD MEMORY clocks to strobe the digitized pixel data of image line m into the buffer memory.

CCD READOUT CONTROL TIMING

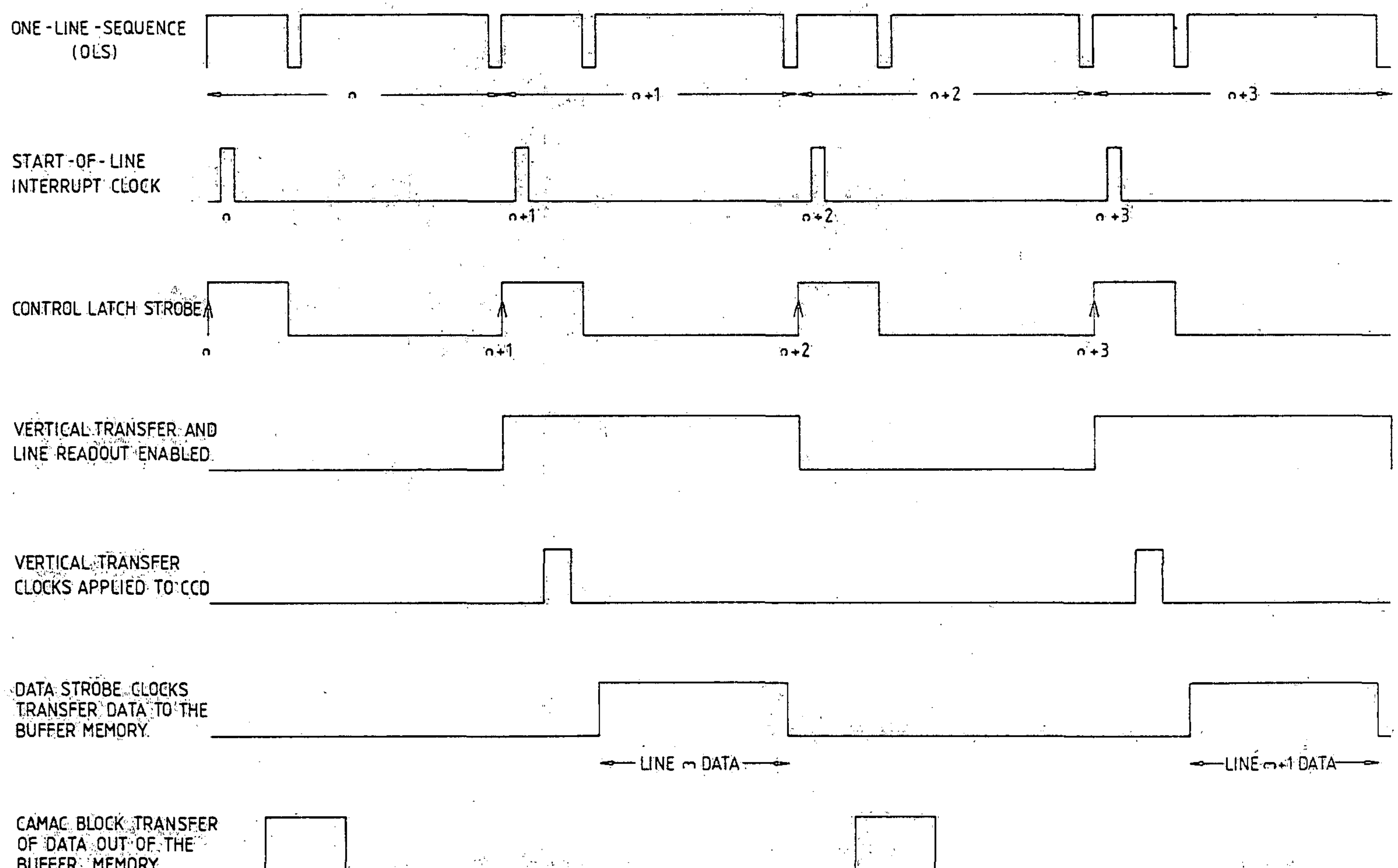


Figure 3.12

(b) (n+1)th interrupt input to the computer

The camera control software assumes that the camera control instruction outlined above is now operative and that the data of image line m are being strobed into the buffer memory. Given that the computer has to retrieve this data from the memory during the (n+2)th one-line-sequence period, further line readout must be inhibited. The appropriate camera control instruction requires that only Bit 1 (ENABLE INTERRUPTS) is set thereby masking line transfer and data transfer enabling functions.

(c) (n+2)th interrupt input to the computer.

The control software recognizes that image line m data are now held within the buffer memory and may be retrieved for storage and/or display by a CAMAC block data transfer. Upon completion of this data transfer, the programme still has sufficient time to enable the readout of image line m+1 during the (n+3)th one-line-sequence period and accordingly loads the same camera control instruction as outlined for the nth interrupt into the CAMAC camera control module.

The above sequence is repeated until all 578 image lines have been read out.

It will be apparent that because two one-line-sequence periods are needed to read out each image line, there is an inherent overhead in the total readout time of an image. A more elaborate data acquisition system could improve this situation but there was insufficient time available for its development within the timescales of the project.

3.5.5 CCD Clock Drivers

The characteristics typically required of the drive waveforms to transfer charge through a CCD are outlined below:

(i) voltage amplitude ~ 10 V.

(ii) high current drive capability because of a CCD's high electrode capacitance.

(iii) slow (~ few μs) rising and/or falling edges, beneficial to the attainment of good charge transfer efficiency.

(iv) a well defined period of overlap between adjacent clock phases. The percentage of phase overlap required to maximize charge transfer efficiency largely depends upon the form of a CCD's electrode structure.

(v) 'clean' waveforms generated from well regulated power supplies to avoid the feedthrough of electrical noise to the CCD's charge detection circuitry.

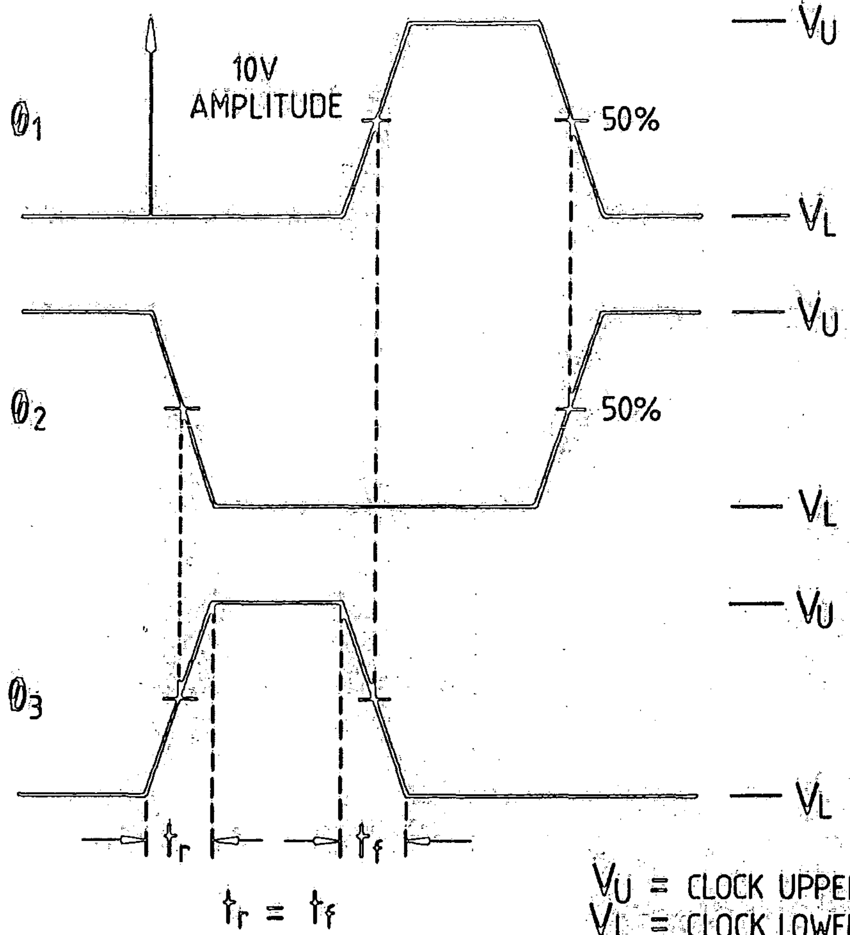
The precise nature of the drive waveforms required for optimal charge transfer efficiency varies between different CCDs of the same type, and to a much greater extent between chips from different manufacturers. In particular, the RCA SID53612 and the GEC P8603 need to be driven in completely different ways.

In the case of the RCA SID53612, its non-overlapping electrode structure calls for asymmetric drive clocks with fast (~ 100 ns) rising edges and slow (~ 5 μs) falling edges in order to maximize charge transfer efficiency within the chip's imaging area (Thorne, 1981; Jorden et al., 1982). A 100% overlap of adjacent clock phases is needed to ensure that the potential well beneath a receiving electrode is fully created before the donor well under the preceding electrode is destroyed.

In contrast, the GEC P8603 employs an overlapping electrode structure to facilitate charge transfer and requires symmetric drive clock waveforms with 50% phase overlap as illustrated in Figure 3.13 (EEV Technical Note No. 6, 1982).

A basic requirement of the CCD clock drivers was that they should permit the operation of both RCA and GEC CCDs, thereby allowing the use of either chip within FOS. In order to minimize the time

GEC CCD DRIVE CLOCK WAVEFORMS



V_U = CLOCK UPPER VOLTAGE LEVEL
V_L = CLOCK LOWER VOLTAGE LEVEL
t_r = CLOCK RISE TIME
t_f = CLOCK FALL TIME

	SYMBOL	tr, tf (µs)	$V_U - V_L$
VERTICAL	VØ	~ 1 - 5	~ 10V
HORIZONTAL	HØ	~ 1 - 2	~ 10V
RESET	ØR	~ 0 - 0·5	~ 10V

Figure 3.13

needed to develop the circuits, it was decided to incorporate copies of the driver circuitry designed by Thorne (1983) for the RGO AAT CCD camera.

Figure 3.14 shows a schematic of a single clock driver channel. It allows the independent adjustment of the following parameters:

(i) clock rise time.

(ii) clock fall time.

(iii) upper clock voltage level.

(iv) lower clock voltage level.

Linear clock transitions are generated using a high speed integrator whose input is switched between two independently adjustable voltage references of opposite polarity (V_R, V_F). This causes the integrator output (Vi) to swing between the power supply rails at rates defined by V_R and V_F. The desired upper and lower clock voltage levels are obtained by clipping Vi by means of a pair of diodes and voltage references V_U and V_L. To obtain the necessary current to drive a CCD's capacitive load, the clipped waveform is passed through a unity voltage gain, high current amplification booster.

The multiple drive channels required for a CCD's VØ, HØ and ØR clocks are constructed on two cards:

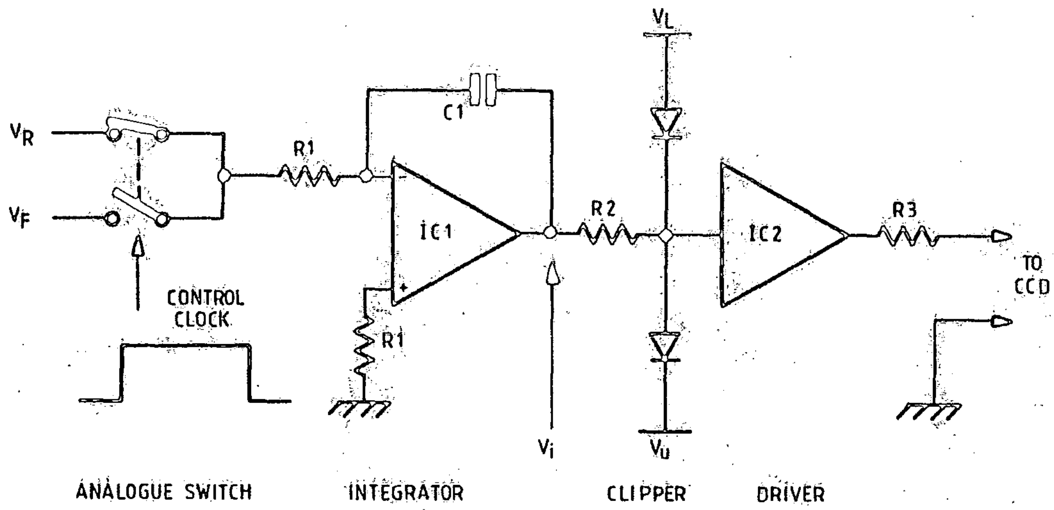
(i) vertical clock drivers.

(ii) horizontal and reset clock drivers.

These cards are of similar design although the vertical clock driver circuitry does include some additional features:

(i) the upper voltage level of the clocks (V_U) can be switched between two references by a clock output from the sequencer

CLOCK DRIVER SCHEMATIC AND OPERATION



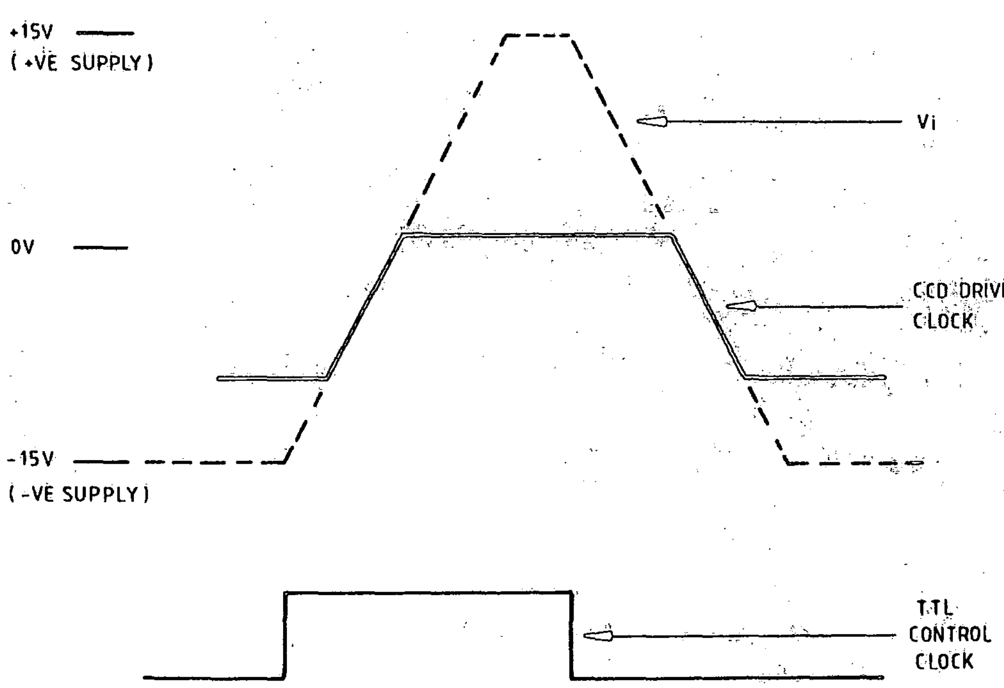


Figure 3.14

and by setting bit 7 (INTEGRATE/CLOCKING) within the camera control instruction. This enables the voltage differential between the upper and lower levels of the clocks to be reduced whenever they are not transferring charge which can be useful in minimizing the effect of ´light emitting defects´ found in some P8603s (see Chapter 5). In these cases, control bit 7 has to be set within all camera control instructions, i.e. during charge erasure, the exposure and frame readout.

(ii) the TTL trigger pulses to the V∅1 and V∅3 clock phases may be swapped at the input to the card by bit 8 (VERTICAL CLOCK PHASE) of the camera control instruction. This enables the direction in which charge is transferred through the CCD´s imaging area to be reversed (back-clocking).

3.5.6 Camera Head Interface

The electronics interface to the camera head consists of:

(i) a ±20 V regulated supply to power the CCD video signal processing electronics.

(ii) open-collector preamplifier clock drivers to buffer those waveforms output from the sequencer which are passed to the video signal sampling and digitization circuitry.

The attainment of an overall low readout noise performance of a P8603 is dependent upon the noise floor of its succeeding video signal processing electronics (see Chapter 4). It is essential, therefore, that the power supplies to the video circuitry and also the circuitry responsible for generating DC bias supplies to the CCD are ´clean´ and well regulated. This is particularly true of those supplies to the on-chip charge detection amplifier, namely, the output transistor drain, the reset transistor drain and its associated bias gates. Power supplies to the signal processing electronics which are derived from central ±24 V analogue supplies within the CCD controller are therefore further regulated to ±20 V before being conveyed to the camera head.

The CCD video signal being measured at the camera head is of very low level (1 electron ≃ 1 μV at the CCD output) and so a clean earth return and a good earthing configuration are essential to avoid ground loops and mains pick-up. A technique of referencing the ground returns from electronics sub-assemblies within the CCD controller and from the camera head to a single 'star' earth point (see for example: Morrison, 1977) was found to provide the most satisfactory solution. In particular, ground returns from analogue and digital circuitry are kept separate throughout the system and are only connected at the star earth.

A good performance of the CCD signal processing electronics also relies upon the video sampling circuitry receiving control signals with well defined clock transitions. Any jitter within these timing signals limits the possibility of achieving a low noise from the electronics alone. The signals which are derived from the sequencer are therefore driven from the CCD controller through open-collector buffers and are terminated close to the sampling circuitry switching elements at the camera head.

3.5.7 Temperature Telemetry

The temperature telemetry circuitry provides a simple indication of whether the cooled CCD is working at the desired operating temperature or not. It monitors the 100 mV/k servo loop error signal generated within the temperature controller to produce a single bit digital status word which changes state if the chip operating temperature deviates from within ±0.5 K of its defined value. The circuit consists of:

(i) an input buffer amplifier to receive the servo error signal conveyed from the camera head.

(ii) a pair of voltage discriminators configured to register non-zero servo error signals deviating from an adjustable 'acceptance window' set to the equivalent of ±0.5 K. The digital output is conveyed to the host computer through the camera data interface.

3.5.8 Shutter Controller

The Compur electronic shutter fitted to the CCD cyrostat houses two electromagnets for open and close actuation and a microswitch to permit remote monitoring of its status. Shutter actuation requires a drive pulse of 24 V amplitude and of 20 ms duration to be applied to the appropriate electromagnet.

The electronics to operate the shutter from the camera control bus incorporate a drive channel for each electromagnet and logic to read the microswitch.

Each drive channel consists of:

(i) a monostable configured to generate a 20 ms pulse when triggered by the assertion of the appropriate camera control instruction bit.

(ii) an opto-coupled Darlington driver to deliver the necessary drive current to the electromagnet. An independent and floating 24 V supply accommodated within the CCD controller chassis provides power to the isolated drive stages.

Shutter status is conveyed to the host computer through the camera data interface.

3.5.9 Line Drivers and Receivers

In considering the problem as to how the CCD camera should be installed on the INT to commission FOS, it was recognized that the CCD controller would need to be operable at up to 100 m from its CAMAC interface. This constraint was imposed by what could be identified at that time as being the most probable organization of the INT's systems electronics installation. Briefly, it was anticipated that:

(i) the CCD controller would be mounted at Cassegrain so as to be in close proximity to FOS and its head electronics.

(ii) the CAMAC modules would be housed in a crate located within a 'Control, Logic, Interconnection and Power' complex (CLIP centre), some 70 m cabling distance from the Cassegrain focus.

Multiple twisted-pair cabling to link the CLIP centre with the Cassegrain focus had already been installed to accommodate RGO-designed instrumentation. To utilize these cables, RS422 differential line drivers and receivers were incorporated into the design of both the CCD controller and its CAMAC interface. Within the CCD controller, these components are fitted to two cards; their functions are listed below:

(i) camera control interface (Figure 3.10)
- 16 receivers for camera control instruction data conveyed from the CAMAC camera control module.
- a single drive channel to transmit the START-OF-LINE interrupt clock to the CAMAC camera control module.

(ii) camera data interface
- 16 drivers to transmit digitized CCD video data to the CAMAC buffer memory module.
- 2 drivers to transmit LOAD MEMORY clocks to the buffer memory. The gating logic to inhibit these clocks is also included on this card.
- 2 drivers to transmit camera status of the CCD operating temperature and of the electronic shutter.

3.6 CAMAC Interface Subassemblies

3.6.1 Selection of the Camera's Computer Interface

From its inception the CCD camera was designed to interface to its control computer through CAMAC. CAMAC had already been adopted at the LPO as the interface between the INT's instrumentation and its Perkin Elmer computer control system (Beale and Smith, 1978) and so compatibility would therefore enable the operation of FOS to be integrated with that of the telescope's IDS and A&G facilities. CAMAC had also been employed in Durham during previous solid-state detector development (Campbell, 1981). An appropriate interface to a DEC LSI-11/23 computer was available and so this configuration was chosen for laboratory operation of the camera.

3.6.2 CAMAC Camera Control Module

A block diagram of the camera control interface is shown in Figure 3.15. START-OF-LINE interrupt pulses conveyed from the camera's sequencing logic are registered within the module through an interrupt input latch. The output of this latch is gated with that of an interrupt mask which is configured under programme control with CAMAC enable (F26 or ENB) and disable (F24 or DIS) instructions. By disabling the mask, the interrupt signal is prevented from asserting the CAMAC dataway's interrupt (or look-at-me) line (L) thereby inhibiting interrupt input to the computer.

In accordance with a mandatory CAMAC specification (ESONE Committee, 1972), the presence of an interrupt request may also be examined using the CAMAC test-look-at-me (F8 or TLM) instruction.

The camera control instruction data generated as a result of an interrupt request are loaded into the module's 16 bit storage register with a CAMAC write (F16 or WT1) instruction. This instruction automatically clears the interrupt input latch so that it can again be triggered upon the arrival of the next START-OF-LINE pulse. CAMAC clear (F10 or CLM) and initialize (Z) instructions may also be used to reset the latch.

The remaining logic decodes CAMAC function (F) and subaddress (A) data and generates CAMAC X for successfully decoded commands. These are listed in Table 3.2 together with a summary of their functions.

The control interface is fitted to the first of two CAMAC cards housed within a double-width module. The second of these cards is populated with RS422 differential drivers, a receiver and opto-

CAMAC CAMERA CONTROL MODULE

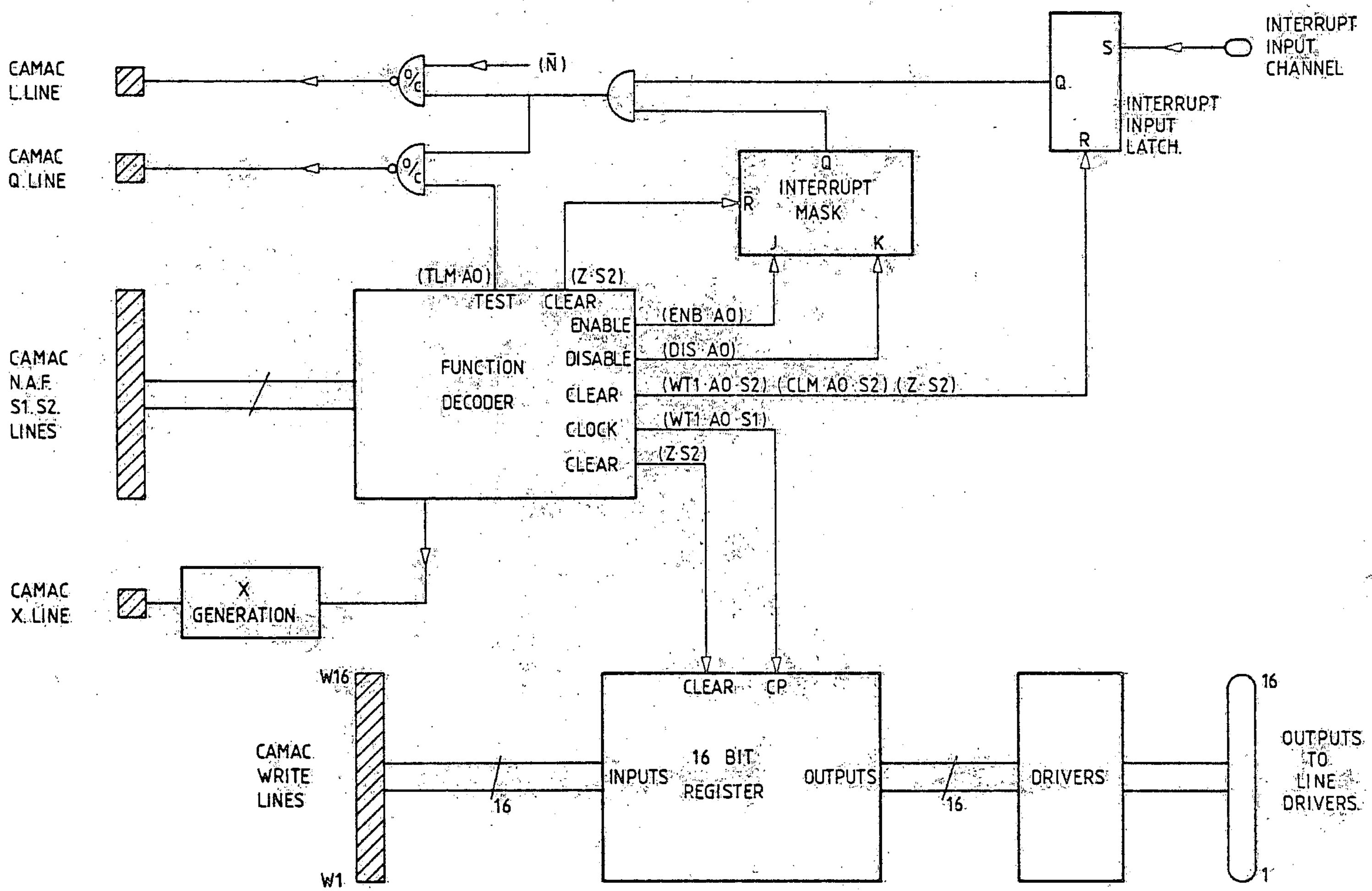


Figure 3.15

Table 3.2 CAMAC CAMERA CONTROL MODULE COMMANDS

CAMAC FUNCTION (F) AND SUBADDRESS (A) (MNEMONIC)	FUNCTION WITHIN THE MODULE
F16. A0 + DATA (WT1. A0)	a) Loads camera control instruction data into the 16 bit storage register. b) Clears the interrupt input latch.
F26. A0 (ENB.A0)	Enables the CAMAC interrupt mask.
F24.A0 (DIS.A0)	Disables the CAMAC interrupt mask. - interrupt requests to the computer are inhibited.
F10.A0 (CLM.A0)	Clears the interrupt input latch.
F8.A0 (TLM.A0)	Tests the logical AND of the interrupt input latch and interrupt mask outputs. Q=1 Interrupt requested. Q=0 Invalid interrupt request.
Z (INITIALIZE)	a) Clears the interrupt input latch. b) Erases the 16 bit storage register. c) Disables the CAMAC interrupt mask. - can be used at system initialization to reset the module.

isolators for remote communication and electrical isolation between the control card and its corresponding interface within the CCD controller.

3.6.3 CAMAC Buffer Memory Module

Digitized video data are generated by the camera at a rate determined by the 60 μs readout period of a single pixel. At this data rate, and because of the synchronous nature of the resulting data stream, a full handshake procedure in which the computer reads each data value into its memory under programme control is impracticable. The computer's acquisition of data will inevitably be an asynchronous operation with the possibility of it failing to read a data value before the arrival of the next because of the additional requirement for it to supervise camera control and periodically, the block transfer of previously acquired data to disc and/or the display. Data could be written directly into the computer's memory at the required rate using DMA but this necessitates both sophisticated hardware and software techniques for which there was insufficient experience available during this phase of the development programme. An alternative system of data acquisition was therefore adopted instead.

Since one line of a CCD image typically consists of only 300–400 pixels (depending upon the chip type) it was considered practical to write all the data from an image line firstly into a temporary buffer store from which the computer can later recover them asynchronously and before it initiates the readout of the next image line. A limitation of this system, however, is the additional time incurred in the readout of the complete CCD image because the computer is not permitted to read the buffer at the same time as data are being written into it. The employment of a double-buffer store to overcome this problem was considered, but was not in fact developed because the extended readout time of the single channel system was in practice found to be quite acceptable for laboratory operation.

To retain hardware independence in the type of computer needed to control the CCD electronics, the buffer was designed to interface through CAMAC with data transfer into the computer via the CAMAC dataway. Its construction is similar to that of the CAMAC camera control module in that two CAMAC cards are housed within a double-width module. RS422 differential line receivers and opto-isolators are fitted to the first of these cards for remote communication and electrical isolation between the buffer and the CCD controller. The buffer's memory and its CAMAC interface components are fitted to the second card of which a block diagram is shown in Figure 3.16.

The memory is designed around a 2048 x 16 bit static RAM and therefore has the capacity to store the data from a CCD image with up to 2048 pixels per line. Its multiplexed input/output data lines are bussed to:

(i) tri-state input buffers through which data conveyed from the CCD controller, via the line receivers and opto-isolators, are strobed into memory.

(ii) gated open-collector output buffers through which data are read from memory onto the CAMAC dataway.

The memory is addressed by the output of an 11 bit binary counter. This is clocked during both read and write cycle operations in order to address consecutive memory locations and is zeroed by a CAMAC generated reset command.

Read and write cycle operations are illustrated in Figure 3.17. The digitized data of each pixel are written into the memory under the control of two management pulses, **STROBE** and **INCREMENT** (previously denoted as a single **LOAD MEMORY** clock - Figure 3.5). These are generated as part of the horizontal transfer sequence waveform pattern by the camera's sequencing logic and are programmed to occur after the completion of the analogue-to-digital conversion. The function of the **STROBE** pulse is to:

CAMAC 16 BIT BUFFER MEMORY

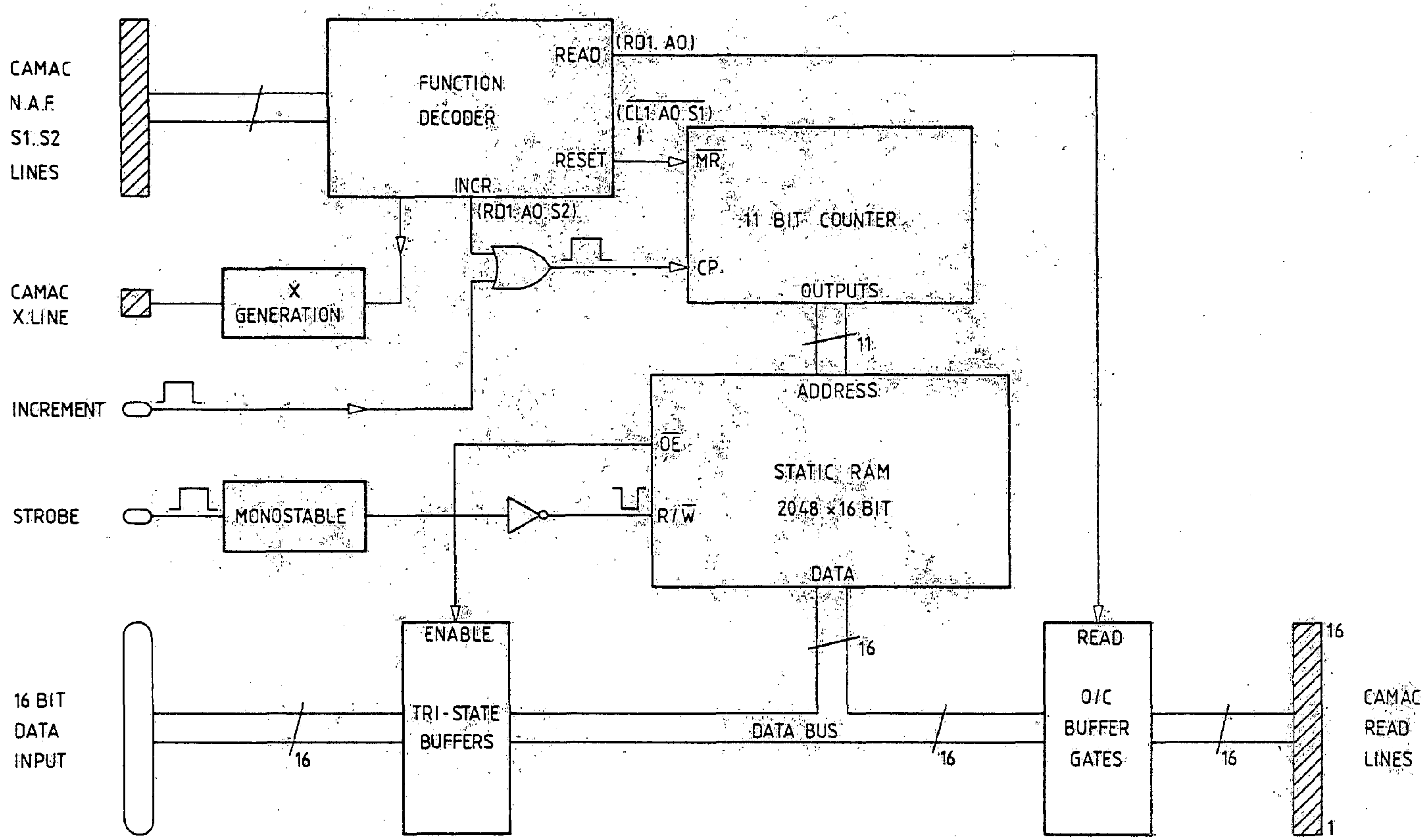


Figure 3.16

CAMAC BUFFER MEMORY MODULE READ AND WRITE CYCLE TIMING

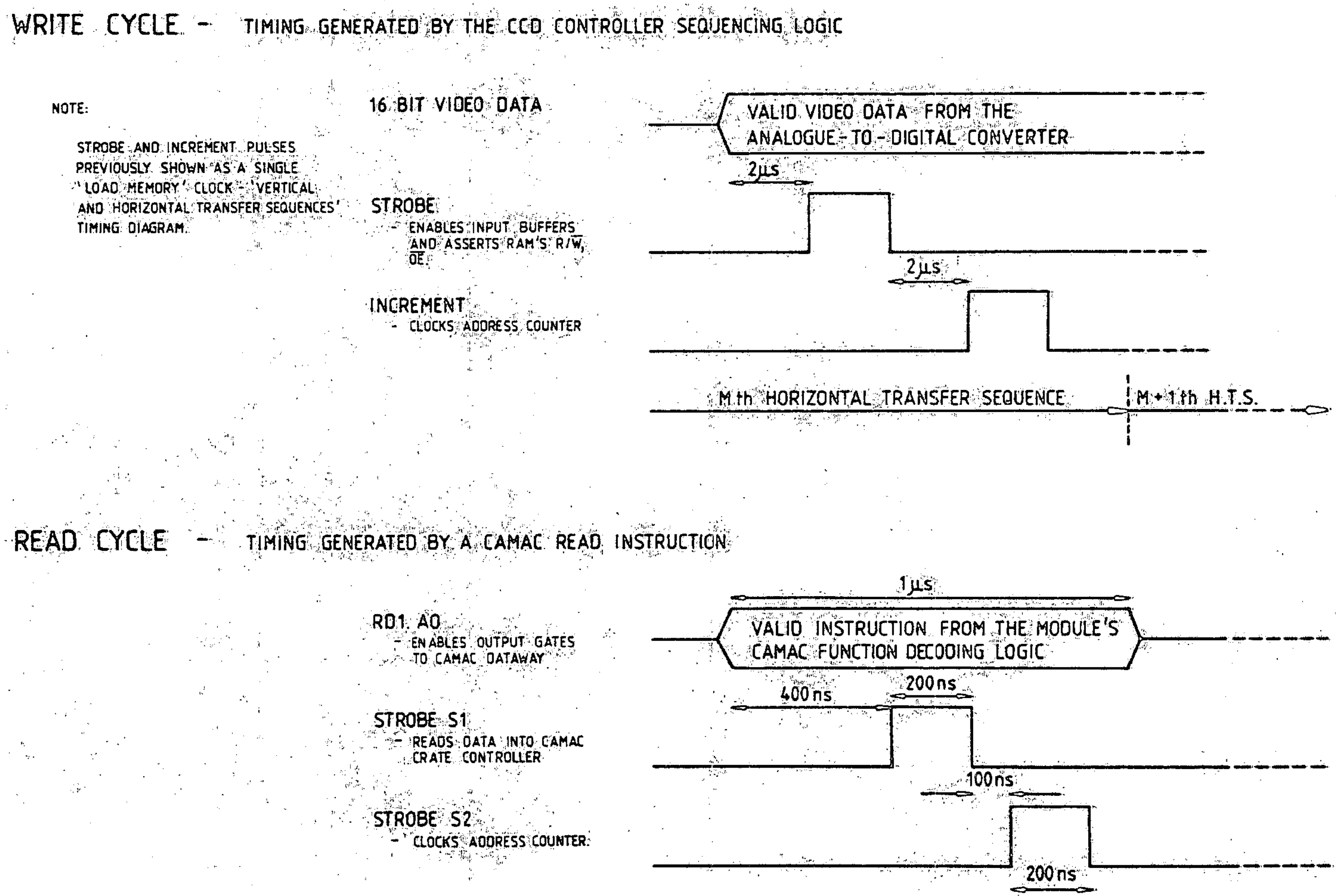


Figure 3.17

(i) enable the tri-state input buffers to convey the data onto the RAM's data bus.

(ii) disable the RAM's internal data output buffers.

(iii) assert the RAM's read/write control line to a write state so that the data present on the data bus are written into the memory location defined by the current output of the address counter.

INCREMENT is generated 2 μs after STROBE and is used to clock the address counter so that data from the next pixel will be written into the next available memory location. The computer must zero the address counter before it initiates line readout from the CCD and also before it recovers the data from the buffer memory.

Data are retrieved from the buffer under programme control using a CAMAC block data transfer operation which consists of a pre-programmed sequence of consecutive CAMAC read (F0 or RD1) cycles. When a valid CAMAC read instruction is decoded by the module, it enables the open-collector output gates so that the data present on the RAM's data bus are also made available to the CAMAC dataway.

Two strobe pulses, S1 and S2, are generated within the 1 μs CAMAC read cycle. Strobe S1 is used by the CAMAC crate's system controller to read the data present on the dataway into its own internal logic for subsequent throughput to the computer. Strobe S2 is used within the buffer memory to increment the address counter so that it points to the next memory location which is to be read in the next CAMAC read cycle i.e. in this system, the memory address auto-increments on a CAMAC read cycle.

Table 3.3 summarizes the CAMAC commands and subaddress data decoded by the buffer memory module together with their functions.

Table 3.3 CAMAC BUFFER MEMORY MODULE COMMANDS

CAMAC FUNCTION (F) AND SUBADDRESS (A) (MNEMONIC)	FUNCTION WITHIN THE MODULE
F0.A0 (RD1.A0)	a) Reads a 16 bit data word from the RAM memory location defined by the current output of the memory address counter. b) Increments the address counter on RD1.A0.S2
F9.A0	Resets the address counter to zero.

3.6.4 CAMAC Camera Status Module

This module provides the computer with the current status of the CCD's operating temperature and of the camera's electronic shutter. The status data is in the form of two single bit logic words and is conveyed to the module through two of the differential line driver/receiver channels linking the CCD controller to the CAMAC buffer memory module. A combination of the CAMAC test-status (F27 or TST) command and subaddress decoding to differentiate between the two channels is used to generate a CAMAC Q response as listed in Table 3.4. Front panel LEDs are also provided for a visual indication of the status.

Table 3.4 CAMAC CAMERA STATUS MODULE COMMANDS

CAMAC FUNCTION (F) AND SUBADDRESS (A) (MNEMONIC)	FUNCTION WITHIN THE MODULE
F27.A0 (TST.A0)	Tests the current status of the electronic shutter. Q=1 Shutter open. Q=0 Shutter closed.
F27.A1	Tests the current status of the CCD's operating temperature. Q=1 Temperature is correct. Q=0 Temperature is outside the accepted range.

3.7 Suggestions for Camera Improvement

So far this chapter has been concerned with the current design of the CCD camera and in particular with its drive electronics and their control from a computer. However, the experience gained through working with the system and maintaining its hardware over a three year period naturally prompts suggestions for its improvement and these are discussed within the remaining sections of this chapter. Some of these ideas are being incorporated into the new generation of CCD controllers being developed for the LPO 4.2m telescope (Bregman and Waltham, 1986).

3.7.1 Serial Communication

One of the most problematic features of the camera in terms of its maintenance has been the large number of twisted-pair cables needed for communication between the CCD controller and its remote CAMAC interface. Currently, both 16 bit camera control instruction data and 16 bit video data are transmitted in a parallel format and this has necessitated multiple opto-isolated line driver/receiver pairs. An obvious refinement, therefore, would be to incorporate serial communication links in order to reduce the cabling requirements and component count while at the same time enhancing reliability.

The rate at which control data must be conveyed to the camera is dictated by the 24 ms duration of a one-line-sequence period. This is a relatively low transmission rate and is easily attainable using RS232C communication although its use would require several modifications to the electronics hardware:

(i) the incorporation of logic within the CCD controller to receive the RS232C serial data stream and convert it to a parallel format. A good solution would be to use one of the many commercially available single-board microprocessors which include both serial and parallel communication ports.

(ii) the redesign of the double latch camera control system to include both the storage and control registers within the CCD controller's subassemblies.

(iii) an interface to the control computer through a standard CAMAC RS232C communication module in order to retain the current independence in the computer hardware needed to operate the camera.

(iv) an interrupt input channel to the computer would still be required and this could be realized using a commercially available CAMAC interrupt input module.

The serial transmission of CCD video data requires a much higher data transfer rate (a 16 bit data value per 60 μs pixel readout period) and this could not be realized using RS232C. However, the analogue-to-digital converter used within the camera does provide serial data, clock and end-of-conversion output signals and so a dedicated 3-wire link could be incorporated by designing a serial to parallel converter into the input stage of the CAMAC buffer memory. Alternatively, the data link could be further reduced to a single channel using the Manchester encoding technique. (See for example: Sanders, 1982; Haung and Moseley, 1984). In this system, the serial data and its clock are combined into a single phase-encoded signal for transmission and then reconstructed within the receiver by phase-locked loop circuitry.

3.7.2 Fibre Optic Data Links

By reducing the number of communication links needed between the CCD controller and its CAMAC interface, the employment of fibre optics to replace the twisted-pair cabling becomes an attractive proposition for the following reasons:

(i) complete electrical isolation between the CCD controller and the CAMAC and computer interface.

(ii) immunity from electromagnetic interference, noise and crosstalk between adjacent channels.

The prohibitive feature of fibre optics, however, is that their cost is still relatively high compared to a conventional RS422 system although the differential is being reduced as the new technology becomes more widely accepted.

3.7.3 Data Buffer

The additional time required to read out a CCD image imposed because of the simple read-write operation of the CAMAC buffer memory has already been discussed. A double-buffer store to replace the current single channel system has been suggested but perhaps a more elegant solution would be to employ a true First-In-First-Out (FIFO) memory which would enable read and write operations to occur simultaneously. The possibility of the computer failing to read a data value because of its asynchronous input rate is avoided provided that:

(i) the FIFO is deep enough to store all the incoming data between computer read operations.

(ii) the average rate of data input to the computer is greater than the readout rate of the camera.

Since the data interface was first designed, several new FIFO I.C.'s have become available which allow the construction of very deep memories with more than sufficient capacity to store the data of a few CCD image lines. Using these devices the computer should always have sufficient time to read the FIFO before it becomes full and therefore incapable of accepting more data.

3.7.4 Telemetry

Experience gained through using the camera has shown that a useful addition would be to incorporate a means of monitoring the absolute operating temperature of the CCD. This could be accomplished by conveying the servo loop error signal from the temperature controller to an analogue-to-digital converter which could be linked to the microprocessor suggested for receiving serial camera control instruction data. In this mode the microprocessor would then have the additional task of accepting requests for telemetry data (over the RS232C control link) and transmitting it back to the computer.

Jorden et al. (1982) have pursued the concept of camera telemetry to include a multi-channel system which also monitors some of the analogue drive voltages applied to the CCD. The computer's ability to read the CCD's operating voltages has an obvious advantage during chip setup and therefore an equivalent system could be considered for this camera.

CHAPTER 4

P8603 CCD CHARGE DETECTION AND VIDEO SIGNAL PROCESSING

4.1 Introduction

The output S/N of a CCD's on-chip charge detection circuitry is dependent upon its characteristics and the conditions under which it is operated. For scientific applications, a cooled CCD camera system operated at a pixel readout rate of ~ 10-100 kHz allows the use of external signal processing electronics to maximize the S/N.

This chapter is concerned with the P8603 CCD's charge detection amplifier, its charge to output voltage conversion sensitivity and the sources of noise inherent in the charge detection process. The requirements of a slow-scan camera system in which the video signal extracted from the P8603 is digitized and conveyed to a computer are discussed. Various techniques are described to maximize the CCD's charge to output voltage conversion sensitivity and its output S/N. Finally, the practical design of the CCD camera video signal processing electronics and their typical performance characteristics are described.

4.2 P8603 CCD Charge Detection Amplifier

The P8603's output amplifier is of the 'floating diffusion' type (Beynon and Lamb, 1980) in which the charge in each pixel is sensed in turn on the capacitance of a reverse-biased diode. Shown schematically in Figure 4.1, the output diode located at the end of the CCD output register is connected to:

(i) the source of a dual gate MOS 'reset transistor' switch. In operation, the capacitance associated with the output node (Co) is charged to a reference potential prior to the readout of each pixel's signal charge.

(ii) the gate of an MOS 'output transistor' which senses the change in potential on the node capacitance as charge is transferred onto it.

P8603 CCD CHARGE DETECTION AMPLIFIER

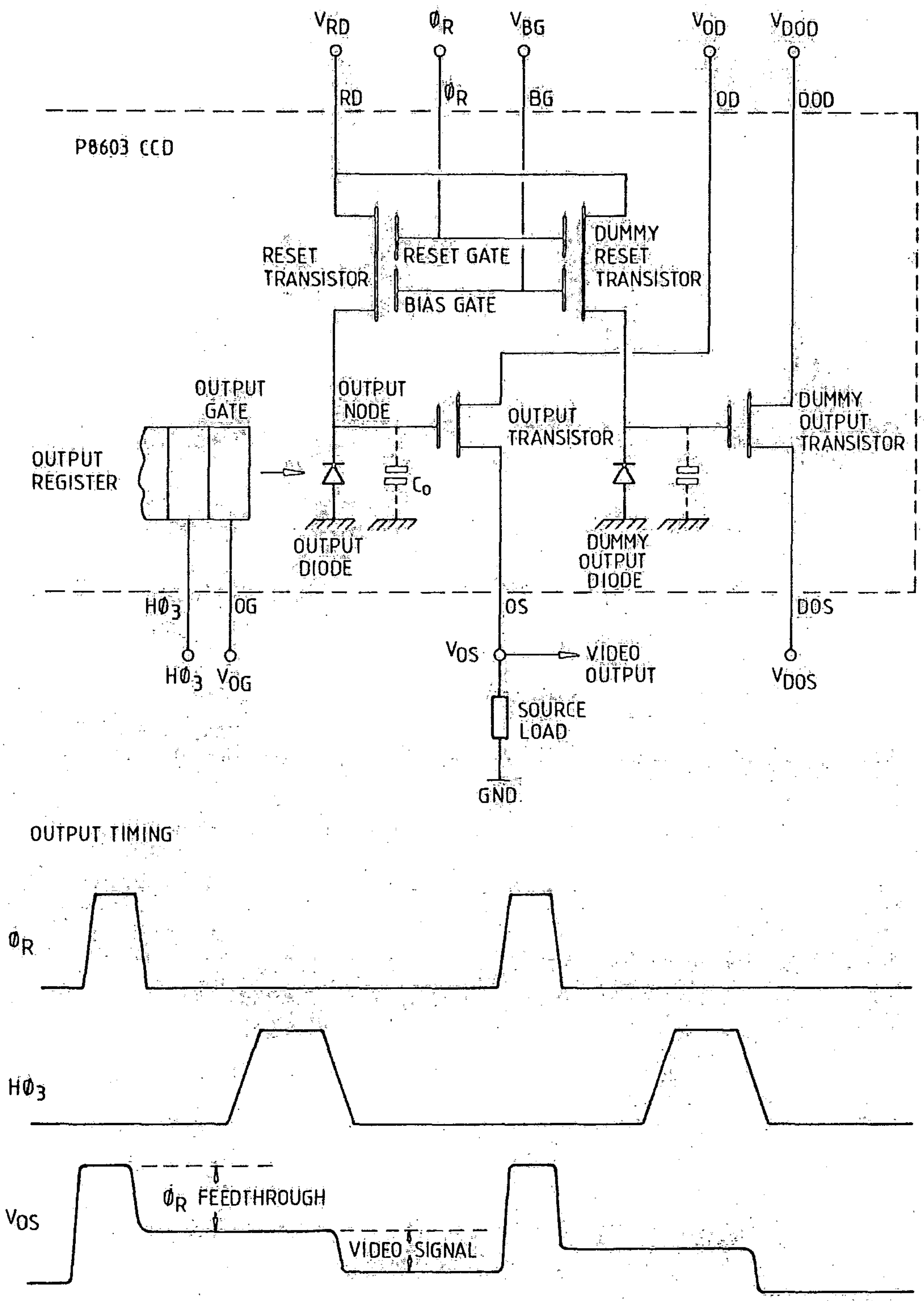


Figure 4.1

The transistor, which is normally operated in the source-follower mode, buffers the high impedance diode to provide a low impedance voltage output at its source to drive following video amplification circuitry.

The output node capacitance is recharged by a reset clock ($\emptyset_R$) applied to one of the reset transistor's gates. $\emptyset_r$ switches the transistor on so that it conducts and thereby charges Co to the potential on the reset transistor's drain (V_{RD}). Feedthrough of the reset clock to the output node partially discharges Co on the falling transition of $\emptyset_R$ which is reflected in the voltage waveform observed on the output transistor's source (V_{OS}). The reset transistor's bias gate, which is held at a fixed DC potential, serves to minimize this feedthrough by partially screening Co from $\emptyset_R$.

Signal charge held under the last $H\emptyset_3$ output register electrode is transferred onto the output node on the falling transition of the $H\emptyset_3$ drive clock. The output gate located between the $H\emptyset_3$ electrode and the output diode serves two functions:

(i) by holding it at a fixed DC voltage (~ 2 V more positive than the lower level of the $H\emptyset_3$ drive clock) it forms a potential barrier (Figure 4.2a) which prevents the signal charge under the $H\emptyset_3$ electrode from spilling onto the output node until the $H\emptyset_3$ potential well is destroyed.

(ii) it isolates the output node from the output register to prevent feedthrough of the $H\emptyset_3$ drive clock.

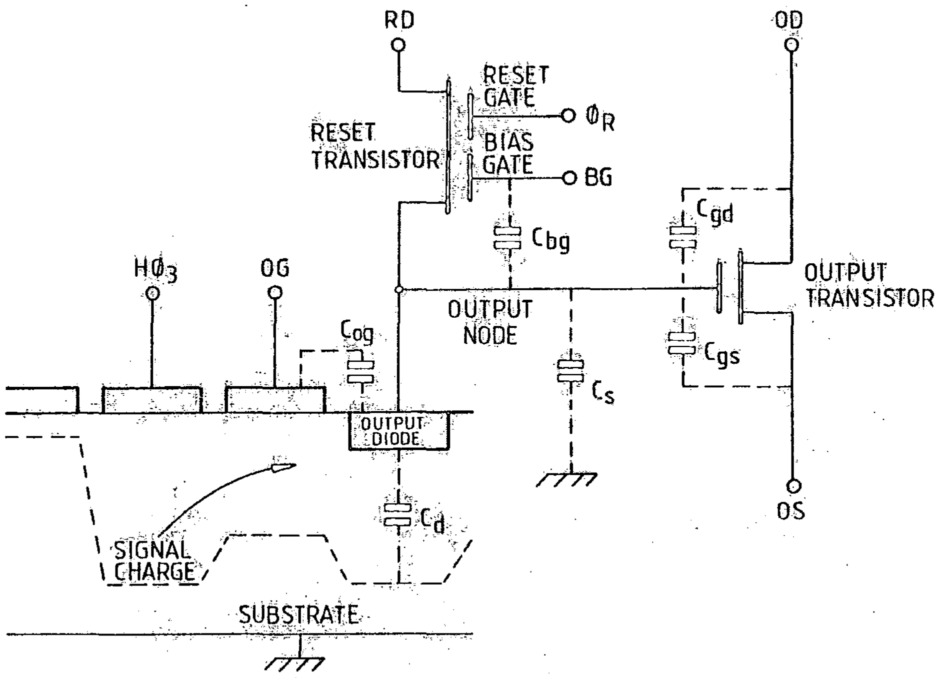
A signal charge Qo discharges the output node capacitance with a resultant change in the node potential (ΔVg) and a corresponding change in the output transistor's source voltage (ΔV_{OS}) given by:

$$\Delta Vg = Qo/Co \tag{4.1}$$

$$\Delta V_{OS} = GQo/Co \tag{4.2}$$

where G = voltage gain of the output transistor.

a) COMPONENTS OF OUTPUT NODE CAPACITANCE



b) P8603 OUTPUT TRANSISTOR CHARACTERISTICS

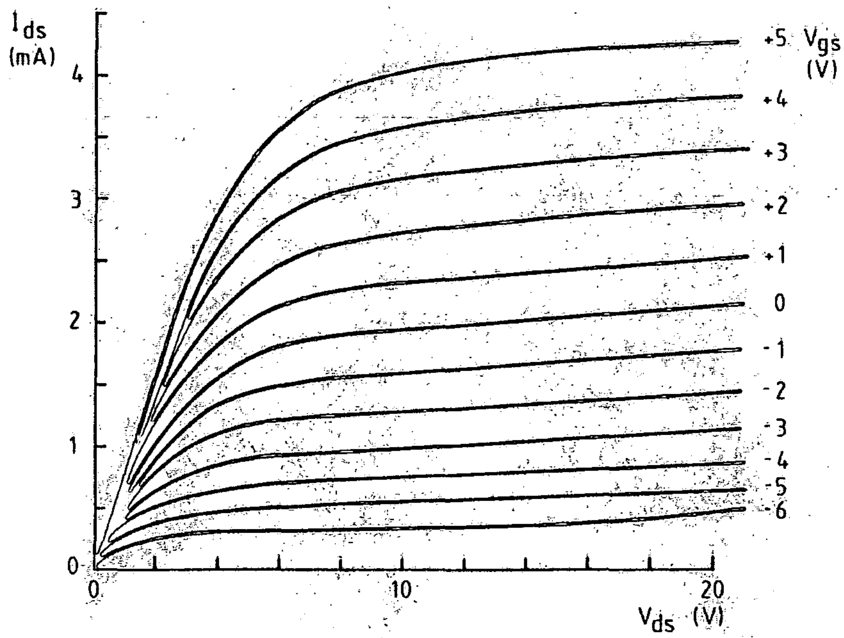


Figure 4.2

The P8603's charge detection circuitry also incorporates a 'dummy' output amplifier. Its design is the same as that of the signal charge detection amplifier with the exception that the dummy output diode is not connected to the CCD output register and therefore does not receive signal charge. Since the dummy reset transistor is also clocked by $\emptyset_R$, the resultant clock feedthroughs within the waveforms on the output transistor source (V_{OS}) and the dummy output transistor source (V_{DOS}) are similar. If required, both outputs may be conveyed to an external differential amplifier in order to cancel the $\emptyset_R$ feedthrough in the video waveform.

4.2.1 Charge Detection Sensitivity

The change in the output transistor's source voltage as a result of each electron detected upon the CCD output node is given by:

$$\Delta V_{OS} = Ge/Co \quad \text{Volts/electron} \qquad (4.3)$$

Increased charge to output voltage conversion sensitivity is therefore attained through increased output transistor voltage gain (G) and/or decreased output node capacitance (Co).

A schematic of the charge detection amplifier illustrating the principal components of capacitance contributing to the total node capacitance is shown in Figure 4.2a. Approximate values for these components and an expression for Co are taken from an EEV publication (EEV Technical Note No. 3, 1982):

Cd ~	0.012 pF	Cbg ~	0.024 pF
Cog ~	0.006 pF	Cgd ~	0.014 pF
Cs ~	0.054 pF	Cgs ~	0.080 pF

$$Co \simeq Cd + Cog + Cs + Cbg + Cgd + (1-G)Cgs \qquad (4.4)$$

Examination of Equation (4.4) reveals that increased output transistor voltage gain is desirable not only to increase the CCD's charge to output voltage conversion sensitivity, but also to reduce the total node capacitance because of the term related to the output transistor's gate-source capacitance (Cgs).

The voltage gain attainable from the output transistor depends on its operating conditions. To ensure maximum gain it is essential that the transistor is operated in the saturated part of its characteristic. Figure 4.2b, reproduced from EEV Technical Note No. 3, shows a set of DC characteristics for a typical device from which EEV recommend standard operating conditions applicable to the requirements of a TV compatible readout rate:

(i) $V_{RD} \sim 17$ V (assuming the lower level of the HØ drive clocks is ~ 0 V) to ensure that the potential to which the output node is recharged is sufficiently positive to extract signal charge from the CCD output register.

(ii) an output transistor drain current (Ids) of $\sim$ 4 mA when operated with an external source load resistor of 3.3 KΩ. From Figure 4.2b, the transistor will be saturated provided that its drain-source voltage (Vds) is $\gtrsim$ 9 V.

The voltage gain theoretically attainable from the output transistor can be calculated (see for example: Gosling et al., 1971) from:

$$G = gm\, RL/(1 + gmRL) \qquad (4.5)$$

where gm = mutual transconductance

RL = effective load resistance, i.e. the value of the source load resistance in parallel with the incremental channel resistance (r_{ds}).

Figure 4.2b shows that for Ids $\sim$ 4 mA, Vds $\sim$ 9 V then gm $\sim$ 0.4 mA/V and $r_{ds} \sim$ 15 KΩ. Hence from Equations (4.5), (4.4) and (4.3), estimates of the output transistor's voltage gain, the output node capacitance and the charge to output voltage conversion sensitivity are:

$$G \simeq 0.5$$

$$Co \simeq 0.14 \text{ pF}$$

$$\Delta V_{OS} \simeq 0.57 \ \mu V/\text{electron}$$

4.2.2 Noise

The output S/N of the charge detection process is limited by the readout noise inherent in the charge detection circuitry and its operation. There are two principal noise sources: reset noise and output transistor noise.

(i) Reset Noise

Reset noise is the uncertainty in the potential to which the CCD output node is recharged prior to the detection of each pixel's signal charge.

When the reset clock ($\emptyset_R$) switches the reset transistor on, the output node capacitance (Co) is charged to the potential on the reset transistor's drain (V_{RD}) as shown in Figure 4.3. Thermal noise associated with the reset transistor's channel resistance (R) is superimposed upon the exponential charging curve. Barbe (1975) has shown that the mean square deviation from the mean node potential at time t (assuming $\emptyset_R$ is applied at t = 0) is given by:

$$\overline{Vn^2} = \frac{KT}{Co}(1-e^{-2t/RCo}) \tag{4.6}$$

where K = Boltzmann's constant

T = temperature

In the 'on' state, the reset transistor's channel resistance (R) is ~ 10^4 Ω (EEV Technical Note No. 3, 1982) and so taking Co ~ 0.1 pF, then RCo ~ 10^{-9} seconds. Hence, provided the reset clock is of sufficient duration (i.e. >> 10^{-9} seconds), the output node capacitance is charged to a mean DC potential (V_{RD}) with a fluctuating noise voltage superimposed upon it:

$$\overline{Vn^2} \simeq KT/Co$$

RESET NOISE

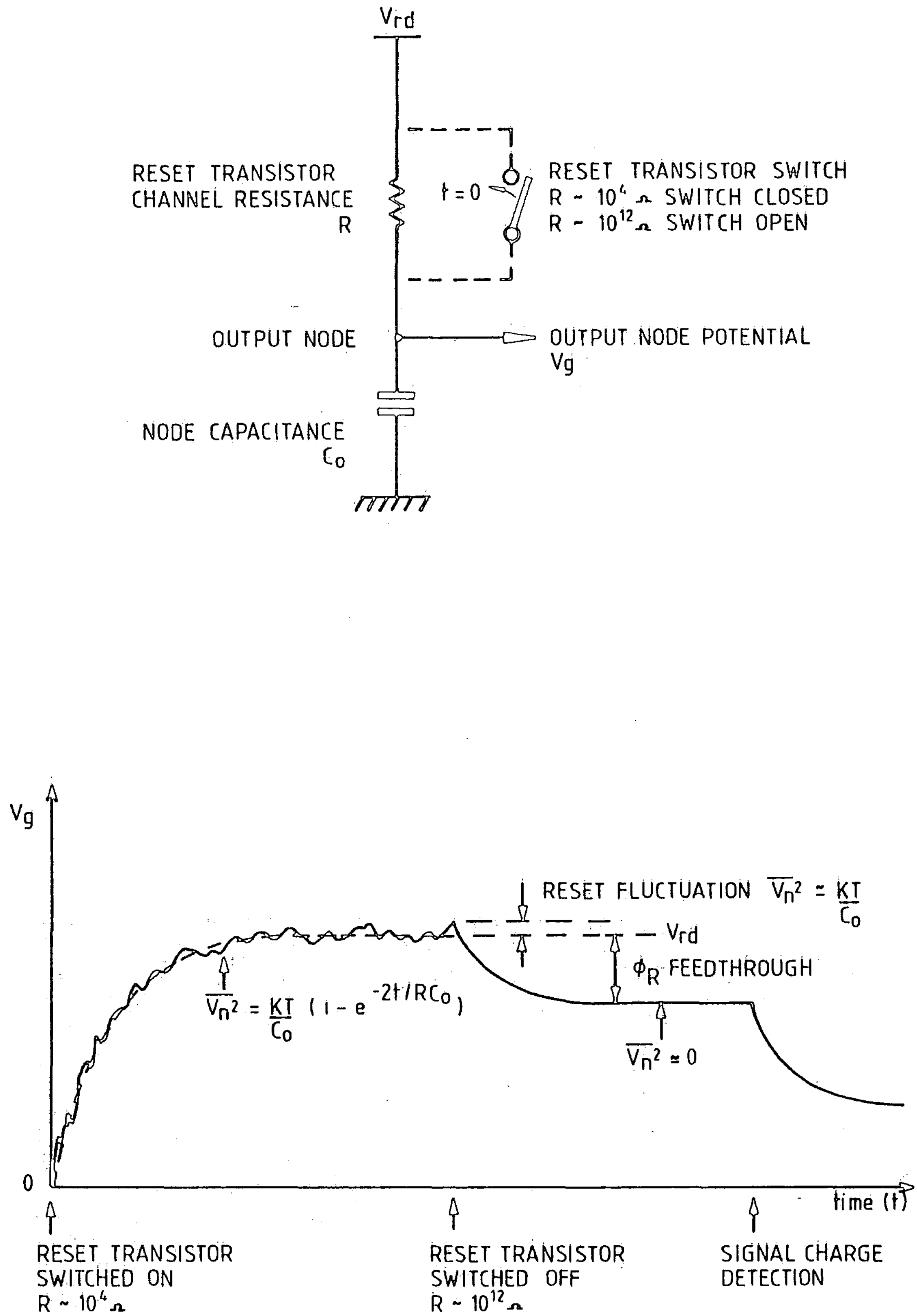


Figure 4.3

Feedthrough of the reset clock partially discharges the node capacitance as the reset transistor is switched off. In the 'off' state, the channel resistance is ~ 10^{12} Ω and so RCo ~ 0.1 seconds. For all practical operating frequencies (i.e. 2t < 0.1 seconds), the mean square deviation from the mean node potential is now, from Equation (4.6), given by:

$$\overline{Vn^2} \approx 0 \tag{4.7}$$

In effect, the potential present on the output node at the instant the reset transistor is switched off is sampled and held on the node capacitance until it is recharged again in the next pixel readout cycle. The output node is therefore reset to a mean DC potential with a fixed noise voltage superimposed upon it of variance:

$$\overline{Vn^2} = KT/Co$$

The rms noise voltage is:

$$(\overline{Vn^2})^{\frac{1}{2}} = (KT/Co)^{\frac{1}{2}}$$

which is equivalent to an rms noise charge:

$$(\overline{Qn^2})^{\frac{1}{2}} = (KTCo)^{\frac{1}{2}}$$

At room temperature, a more practical expression is:

$$\begin{aligned}(\overline{Qn^2})^{\frac{1}{2}} &= 400(\text{Co in pF})^{\frac{1}{2}} \text{ electrons}\\ &\simeq 150 \text{ electrons (taking Co = 0.14 pF).}\end{aligned}$$

(ii) Output Transistor Noise

The P8603's output transistor is a MOSFET. Figure 4.4 illustrates the general form of a MOSFET's noise spectrum which is attributable to two principal noise sources:

(i) 1/f (or 'flicker') noise.

GENERAL FORM OF A MOSFET NOISE SPECTRUM

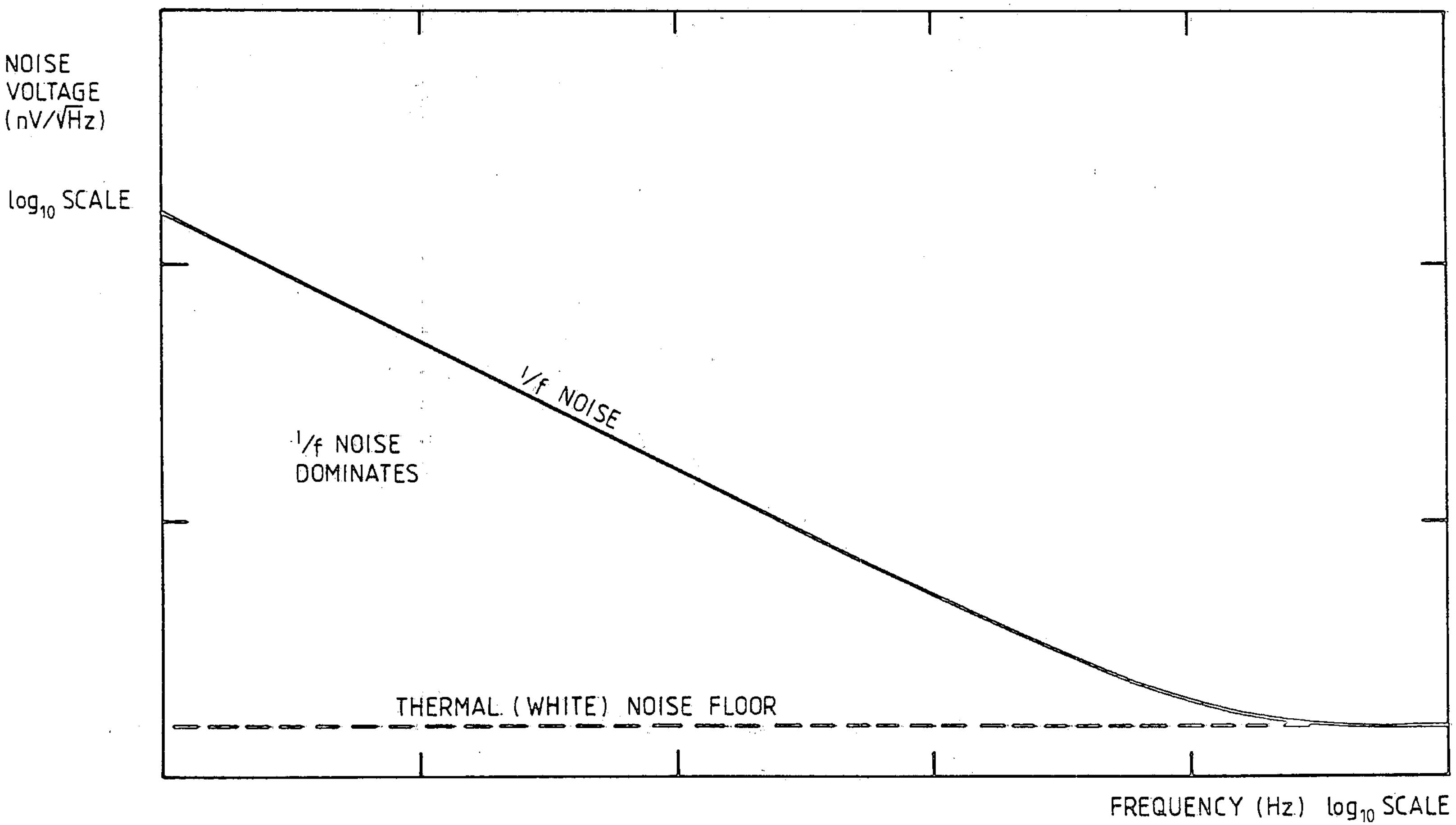


Figure 4.4

(ii) thermal noise.

1/f noise is characterized by a $1/f^{\alpha}$ spectrum (where $\alpha \simeq 1$) and is therefore, as its name implies, dominant at low frequencies. Many review articles and several formal theories have been published which attempt to explain its origin.

In MOSFETs, it is attributed to the communication of carriers within the channel with surface-state trapping levels (Van der Ziel, 1970). Fluctuations in the occupancy of these traps gives rise to an irregular carrier concentration which is observed on a DC channel current as a superimposed noise. A tunneling mechanism with traps at varying depths within the surface oxide layer can explain the wide distribution in time constants required of a 1/f type spectrum.

Thermal noise is generated within the MOSFET's channel resistance and depends on the transconductance at the chosen operating point (Wallmark and Johnson, 1966). In contrast to 1/f noise, its spectral noise density is essentially white (i.e. flat) in character.

The relative powers of 1/f and thermal noise will depend on the characteristics and operation of the particular MOSFET. In the presence of a large 1/f component, thermal noise will only become dominant at high frequencies, above the 1/f 'knee' (i.e. that frequency at which the powers of 1/f and thermal noise are equal). Since a MOSFET is a surface-channel device in which the oxide traps can interact with conduction along the entire channel, 1/f noise tends to dominate over a wider frequency range than in for example planar bipolar and junction field-effect transistors.

The P8603 MOSFET's noise spectrum has been reported to be essentially 1/f in character, only decreasing to a white noise floor (depending on its operating conditions) at MHz frequencies (EEV Technical Note No. 3, 1982). Similar characteristics have also been reported of MOSFETs incorporated within other manufacturers' CCDs (see for example: Janesick et al., 1984).

Since the contribution of white noise to a CCD MOSFET's total output noise may be limited by restricting the signal measurement bandwidth, it is the power of the 1/f noise which can therefore be expected to limit the readout noise floor that can ultimately be achieved.

4.3 Slow-Scan Operation

Typically, the objective in cooled, slow-scan CCD camera systems intended for scientific applications is to encode the signal charge collected in each pixel as a digital number for input to a computer. Operation of the CCD at readout rates of ~ 10-100 kHz allows the use of external signal processing electronics to suppress the readout noise inherent in the charge detection process. Figure 4.5 provides an overview of the signal transfer function, tracing the conversion of the signal charge to a voltage waveform on the CCD output node through to the eventual digitization of the processed video. The parameters to be considered within the system design are:

(i) the sensitivity of charge to voltage conversion on the CCD output node.

(ii) the readout noise inherent in the charge detection process.

(iii) the amplification and signal processing of the video waveform required prior to digitization.

(iv) the quantization and dynamic range of the digitization expressed in equivalent signal charge.

The video signal retrieved from the P8603 is of the order of 1 μV/electron and contaminated by the unavoidable reset noise introduced during the charge detection process. Reset noise, however, may be signal-processed out of the video waveform so that in its absence, the dominant noise source within the charge detection amplifier is that of the output transistor itself. 1/f noise arising in this component may be substantially reduced by careful optimization of its operating conditions. Any increase which can be obtained in the CCD's charge to

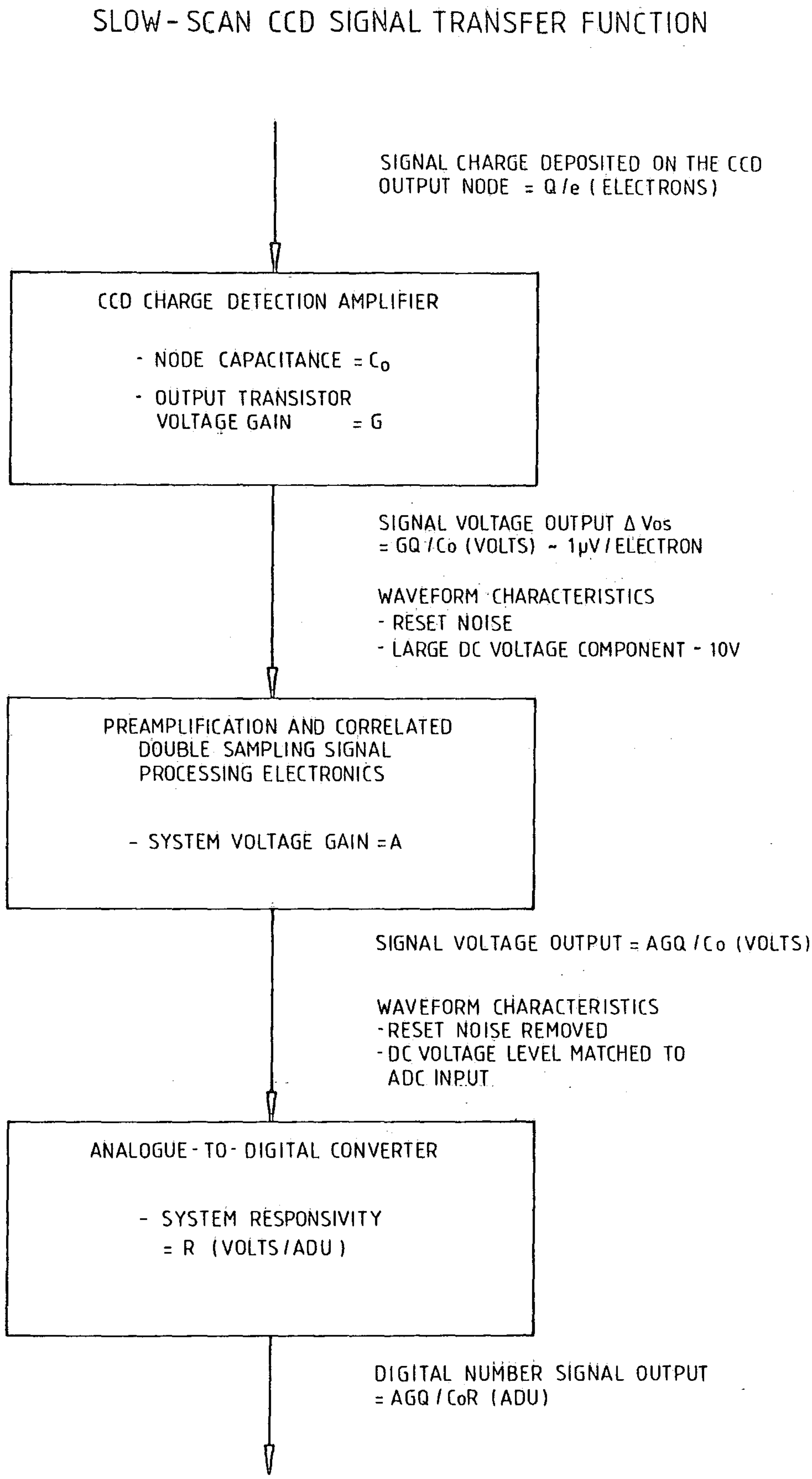

SLOW-SCAN CCD SIGNAL TRANSFER FUNCTION
SIGNAL CHARGE DEPOSITED ON THE CCD OUTPUT NODE = Q/e (ELECTRONS)
CCD CHARGE DETECTION AMPLIFIER
- NODE CAPACITANCE = C_0
- OUTPUT TRANSISTOR VOLTAGE GAIN = G
SIGNAL VOLTAGE OUTPUT ΔV_{os} = GQ/Co (VOLTS) ~ 1μV/ELECTRON
WAVEFORM CHARACTERISTICS
- RESET NOISE
- LARGE DC VOLTAGE COMPONENT - 10V
PREAMPLIFICATION AND CORRELATED DOUBLE SAMPLING SIGNAL PROCESSING ELECTRONICS
- SYSTEM VOLTAGE GAIN = A
SIGNAL VOLTAGE OUTPUT = AGQ/Co (VOLTS)
WAVEFORM CHARACTERISTICS
- RESET NOISE REMOVED
- DC VOLTAGE LEVEL MATCHED TO ADC INPUT
ANALOGUE-TO-DIGITAL CONVERTER
- SYSTEM RESPONSIVITY = R (VOLTS/ADU)
DIGITAL NUMBER SIGNAL OUTPUT = AGQ/CoR (ADU)

Figure 4.5

output voltage conversion sensitivity is desirable in order to maximize the output S/N ratio of the charge detection process. Improvements are to be anticipated from:

(i) minimizing the capacitance of the output node.

(ii) maximizing the voltage gain of the output transistor source follower.

The ~ 1 μV/electron signal voltage on the output transistor's source is superimposed upon a large DC voltage component (~ 10 V), inherent in the transistor's operation. Since the video signal must be amplified prior to its digitization, it is necessary that this DC component is much reduced (to ~ 100 mV) at the input to the preamplification electronics in order to avoid amplifier saturation. Following preamplification, the reset noise within the video waveform may be cancelled using a signal processing technique known as 'correlated double sampling' (White et al., 1974) which takes account of the uncertainty in the potential on the CCD output node arising from its recharge. The resultant waveform will in general require the addition of a small DC offset voltage in order that the final output voltage corresponding to zero detected signal charge matches the input to the digitization electronics.

The optimum preamplifier voltage gain depends on the signal transfer function's system noise floor. Ideally, the total system noise should be dominated by the contribution of readout noise from the CCD itself. In particular, noise added by the uncertainty in the digitization process (±0.5 ADU) should be kept small. This becomes increasingly important when any subsequent analysis of image data is considered, for example, sky subtraction and flat-fielding. For digital quantization error to be negligible, the system gain must satisfy the condition:

$$1 \text{ ADU} \ll g\sigma_{tot}$$

where g = system responsivity expressed in ADUs per detected signal charge.

σtot = total system noise expressed in equivalent signal charge.

However, adjusting the system gain such that the system noise is very much greater than the quantization error, limits the signal dynamic range which can be registered by an analogue-to-digital converter of given precision (i.e. number of bits). Hence the quantity of signal charge which might be collected within any one CCD pixel must also be considered with regard to the application. Commercially available high resolution converters working within a reasonable conversion period (~ 20 μs) are currently limited to 16 bit accuracy and hence a maximum digital count of 65,535 ADU.

In anticipation of reducing the P8603's readout noise to ~ 5-10 electrons rms, a reasonable setting of the system gain would be for a quantization of ~ 1 electron/ADU. This would mean that the peak signal charge within any one pixel which could be measured with a 16 bit converter would be limited to 65535 electrons. The usable dynamic range, again for any one pixel, would then be given by:

$$\text{Dynamic range} = 65535/g\sigma tot$$
$$\sim 6500\text{-}13000 \text{ (assuming } g\sigma tot \sim 5\text{-}10 \text{ ADU rms)}$$

It is necessary to consider whether this is adequate with regard to the application of this system to faint object spectroscopy.

FOS is primarily intended for low S/N (~ 10) observations of faint objects for which the sky background signal can be expected to be at least comparable to that of the object signal. It is therefore important to estimate how long an exposure could be undertaken before the sky background would be expected to cause the system to saturate.

Parry (1982) estimated that the sky background continuum would produce of the order of 0.47 electrons/pixel/second at 800 nm. However, the night sky spectrum is highly structured, and it is the peak signals from the bright sky emission lines which are important if the data from an observation is subsequently to have the sky background subtracted properly.

Early results from the AAT FORS (Gillingham, 1984) proved useful here, showing that the brightest sky lines produce peak signals up to an order of magnitude greater than the continuum (Ellis, 1983). Thus in the case of FOS, a better estimate for the peak signal from the sky is ~ 5 electrons/pixel/second. This would cause the system to saturate after ~ 13000 seconds integration. However, CCD exposures are typically limited to ~ 1000 seconds to avoid excessive contamination of the data by cosmic ray events. In this time the maximum signal from a sky emission line would be only ~ 5000 electrons/pixel. A pixel capacity of 65535 electrons/pixel is therefore more than adequate in this application.

With this background, correlated double sampling signal processing and the optimization of the P8603's operation can now be considered in more detail.

4.3.1 Correlated Double Sampling

Correlated double sampling (CDS) signal processing within each CCD pixel readout cycle enables the reset noise inherent within the video waveform to be removed while also attenuating low-frequency noise (White et al., 1974).

The concept of CDS is to take the difference between measurements of the video waveform before and after the pixel signal charge is sensed on the CCD output node as illustrated in Figure 4.6. Its success is dependent upon the effectively zero mean square deviation from the mean potential remaining on the output node after its recharge (Equation (4.7)). For all practical operating frequencies, the uncertainty of the reset potential within two samples of the video waveform is correlated and may therefore be cancelled by their subtraction.

The sampling used to measure the video waveform can take several forms:

(i) DC restoration (or clamping)

(ii) point sampling

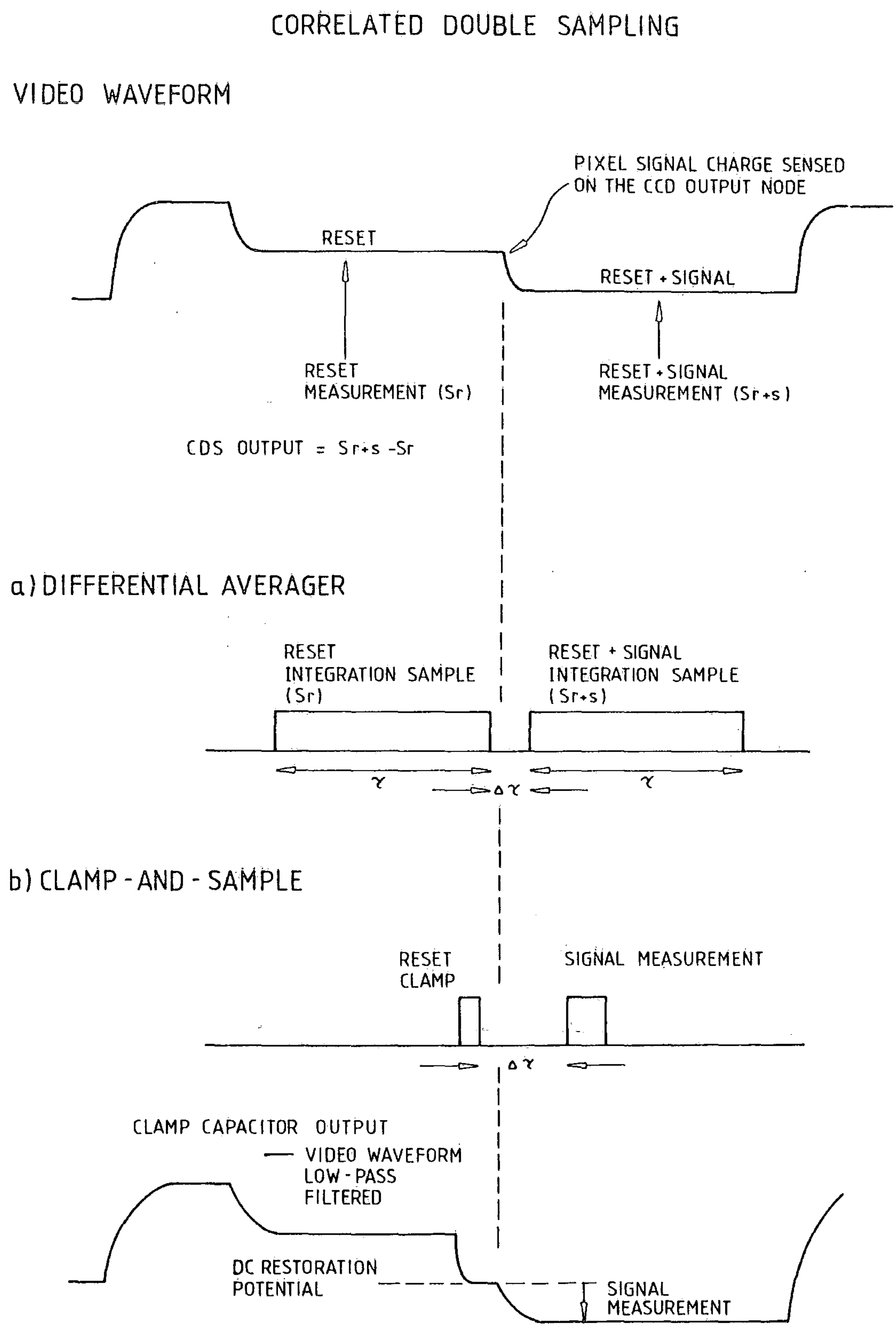

CORRELATED DOUBLE SAMPLING
VIDEO WAVEFORM
PIXEL SIGNAL CHARGE SENSED ON THE CCD OUTPUT NODE
RESET
RESET + SIGNAL
RESET MEASUREMENT (Sr)
RESET + SIGNAL MEASUREMENT (Sr+s)
CDS OUTPUT = Sr+s -Sr
a) DIFFERENTIAL AVERAGER
RESET INTEGRATION SAMPLE (Sr)
RESET + SIGNAL INTEGRATION SAMPLE (Sr+s)
τ
Δτ
τ
b) CLAMP - AND - SAMPLE
RESET CLAMP
SIGNAL MEASUREMENT
Δτ
CLAMP CAPACITOR OUTPUT
— VIDEO WAVEFORM LOW - PASS FILTERED
DC RESTORATION POTENTIAL
SIGNAL MEASUREMENT

Figure 4.6

(iii) integration (or averaging)

Combinations of these sampling techniques enable the implementation of a variety of CDS processor schemes. Hopkinson and Lumb (1982) have reviewed the various possibilities and their relative merits in the presence of white, $1/f$ and $1/f^2$ noise components, the relative contributions of which will depend on the characteristics and operation of the particular CCD. Optimal performance will be obtained from that CDS processor which most closely approaches the ideal of a matched filter whose transfer function is inversely proportional to the CCD's noise power spectral density.

The CDS processor which appears to have been more widely adopted is the 'differential averager' (Marcus et al., 1979; Loh, 1981; Gunn and Westphal, 1981) for which the sampling scheme is shown in Figure 4.6a.

- the video RESET level is sampled by integration over a period τ so as to obtain a measure of its average value.
- a delay $\Delta\tau$ is allowed for the transfer of the pixel signal charge onto the CCD output node.
- the video RESET + SIGNAL level is sampled by integration over a second period τ.
- taking the difference of the two integration samples cancels the uncertainty of the output node's reset potential to yield a measure of the change in video waveform potential arising from the pixel signal charge.

It has a response which:

- attenuates components of high-frequency noise whose corresponding periods are shorter than the sampling period (τ) by virtue of the integration.
- attenuates components of low-frequency noise whose corresponding periods are longer than the CDS cycle interval.

The optimum integration period (τ) depends on the precise nature of the CCD's noise sources. In the presence of white, 1/f and $1/f^2$ noise, the output noise variance of the differential averager (after correction for changes in gain with varying τ) is:

- for white noise $\propto 1/\tau$
- for 1/f noise independent of τ
- for $1/f^2$ noise $\propto \tau$

Hence, there will be an optimum value for τ at which the output noise powers arising from the white and $1/f^2$ components are equal and the maximum S/N is achieved.

For white (i.e. uncorrelated) noise, the output S/N is independent of the gap ($\Delta\tau$) between the two integration samples. However, in the presence of 1/f noise, $\Delta\tau$ must be kept small in comparison to τ so as not to degrade noise performance (Hegyi and Burrows, 1980).

An alternative CDS processor is the 'clamp-and-sample' technique (White et al., 1974) as shown in Figure 4.6b.

- the video waveform is low-pass filtered to attenuate components of high-frequency noise.
- the video RESET level is DC restored by clamping through a capacitor to either ground or a reference potential.
- the clamp is released and the pixel signal charge is transferred onto the CCD output node during the interval $\Delta\tau$.
- the resultant change in the video waveform potential arising from the pixel signal charge produces a change in the voltage across the clamp capacitor which is then sampled.

The disadvantage of this scheme is that the low-pass filtering to limit the system bandwidth and hence attenuate high-frequency noise also reduces the slew-rate response of the resultant video waveform. A large $\Delta\tau$ may then be necessary to allow for settling of the video RESET + SIGNAL level before it is sampled in order to avoid signal attenuation. This is in conflict with the desire to keep $\Delta\tau$ as small as possible to discriminate against low-frequency noise. The differential averager overcomes this problem since the high-frequency noise attenuation is provided by the integration rather than a low-pass filter and thus permits a small $\Delta\tau$.

4.3.2 Dummy Charge Detection Amplifier

The unavoidable presence of ϕ_R feedthrough within the CCD video waveform is rejected by a CDS processor. The use of the P8603's dummy charge detection amplifier to provide a signal-free equivalent video waveform for subsequent differential subtraction of the feedthrough is therefore unnecessary. Combining both the real and dummy video waveforms would in fact decrease the output S/N from the CCD by a factor of $\sqrt{2}$ compared to that of single-ended output operation. Hence the dummy charge detection amplifier serves no useful application in a slow-scan camera system in which the maximum possible charge detection S/N is required and therefore need not be considered further.

4.3.3 Reset Transistor Gate Connections

The bias gate on the reset transistor (Figure 4.1) helps to screen the CCD output node from reset clock feedthrough. Examination of Equation (4.4) reveals that the capacitance associated with this bias gate (Cbg) contributes to the total node capacitance (Co). At the expense of increasing the reset clock feedthrough, the Cbg component may be eliminated by reversing the connections to the bias and reset clock gates. In this mode:

$$Co \simeq Cd + Cog + Cs + Cgd + (1-G)Cgs \qquad (4.8)$$

which yields Co $\simeq$ 0.13 pF compared to Co $\simeq$ 0.14 pF as estimated in Section 4.2.1. The charge to output voltage conversion sensitivity is increased proportionally.

Reset clock feedthrough is rejected by a CDS processor and the increased charge detection sensitivity is desirable since it increases the output S/N. Reversed connections to the bias and reset clock gates will therefore be assumed in following discussion of slow-scan operation.

4.3.4 Output Transistor Source Load

The voltage gain of the output transistor can be increased so that it more closely approaches unity by using a constant current source load instead of a resistor to increase the effective load resistance (Equation (4.5)). Charge to output voltage conversion sensitivity is increased and so this mode of operation is favoured provided that any additional noise introduced by the constant current circuitry is negligible.

4.3.5 Output Transistor Operating Conditions

Morcom (1981) has shown that the noise spectrum of the P8603's MOSFET output transistor depends on its operating conditions. In particular, a significant reduction in 1/f noise is attainable by operating the transistor at a lower drain current (Ids ≈ 1 mA) than that advocated by EEV in their recommended standard operating conditions as outlined in Section 4.2.1.

Taken from Morcom's results, Figure 4.7 shows output noise spectra obtained from a typical device when operated with Ids = 1 mA and Ids = 4 mA. At the lower drain current, the characteristic of the 1/f dependent noise is altered to that of one approaching $1/f^2$ behaviour. The low-frequency noise 'knee' at which the powers of white and low-frequency noise are equal is reduced and the total output noise in the measured bandwidth (750 KHz) is also reduced. Hopkinson and Lumb (1982) have reported similar results from GEC CCDs.

The effect is thought to be attributable to a change in the MOSFET from surface to buried-channel operation. Carrier conduction within the channel is shifted away from its surface into its bulk with the result that the interaction of carriers with surface-state trapping levels is much reduced. The carrier concentration within the MOSFET's channel and hence the quantity of charge which can communicate with surface-state traps is greatest at its source. Morcom therefore relates the transition from surface to buried-channel operation to a threshold gate-source voltage at which

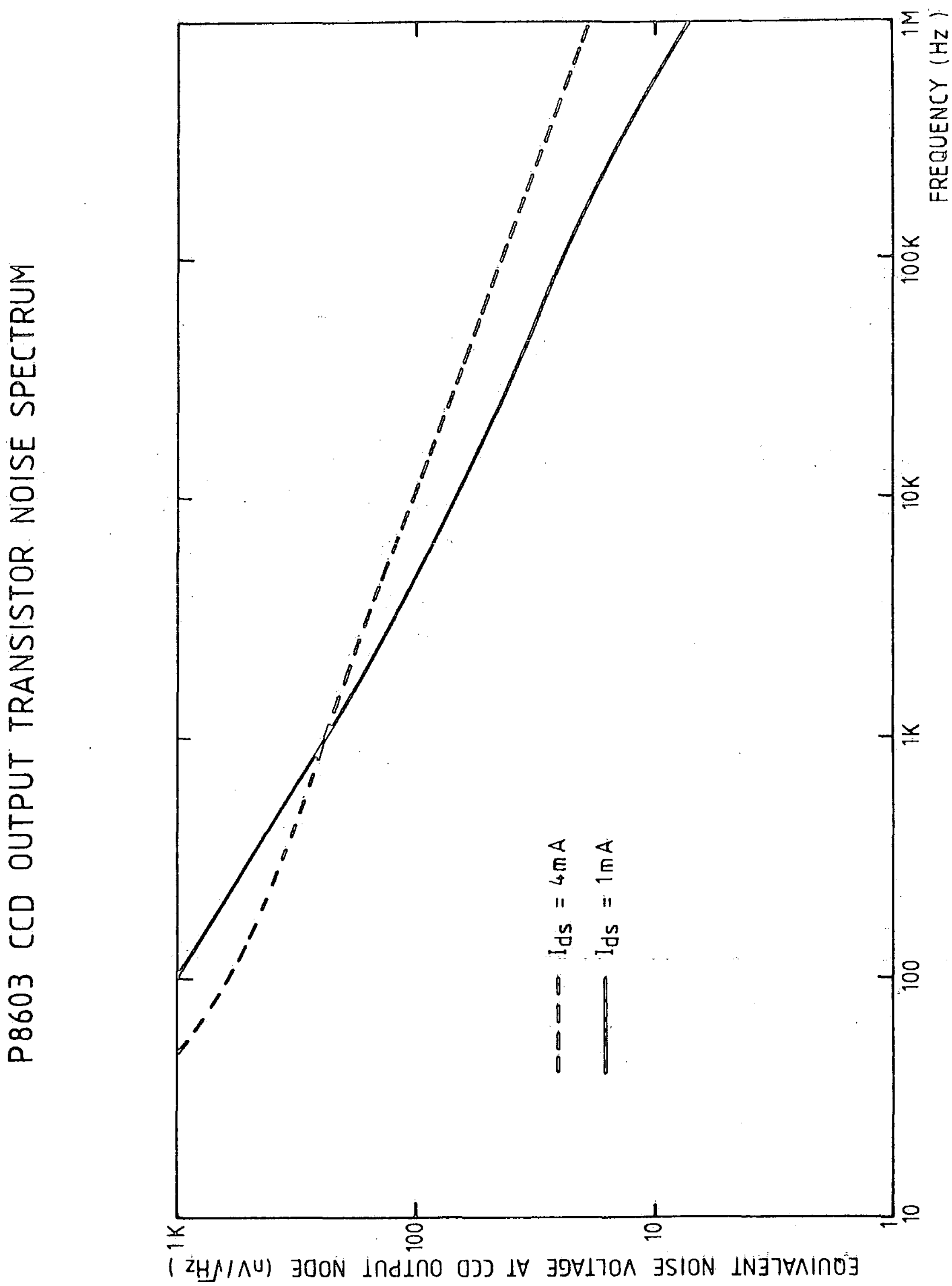

P8603 CCD OUTPUT TRANSISTOR NOISE SPECTRUM
Ids = 4mA
Ids = 1mA
FREQUENCY (Hz)
10
100
1K
10K
100K
1M
EQUIVALENT NOISE VOLTAGE AT CCD OUTPUT NODE (nV/√Hz)
1
10
100
1K

Figure 4.7

carriers in the vicinity of the source first come into contact with the surface. Typically, buried-channel operation is ensured if:

(i) Vgs ≤ -3 V

(ii) Ids ≃ 1 mA (at room temperature)

Once these conditions are established, the remaining consideration is that of the MOSFET's drain-source voltage (Vds). Although the cause is not understood, the output noise attainable in the buried-channel mode has been observed to increase again if Vds ≥ 4 V (EEV Technical Note No. 6, 1982).

Hence, to maximize the output S/N of the MOSFET, values of Vg (i.e. V_{RD}) and V_{OD} are required for which:

(i) Vgs ≤ -3 V

(ii) Ids ≃ 1 mA (at room temperature)

(iii) the MOSFET operates in the saturated part of its characteristic to ensure maximum voltage gain.

(iv) Vds ≤ 4 V.

4.4 Camera Head Video Signal Processing Electronics

As outlined in Chapter 3, the CCD camera head video signal processing electronics consist of a preamplifier and a 16 bit analogue-to-digital converter. Both are located at the camera head in order that their interconnections and in particular those with the CCD itself may be of minimal length, thus helping to reduce the possibility of extraneous noise pickup.

From its inception, the preamplifier was designed to incorporate the video preamplification and CDS signal processing circuity and also the electronics to generate the various DC bias voltage supplies needed to drive the P8603 CCD. Considerable development of the prototype was necessary before arriving at the design to be described. This was partially motivated by the enthusiasm of a team at the RGO to acquire a low input noise preamplifier designed specifically for operation of the GEC CCD; their initial work had been directed towards supplying an RCA CCD based camera system to the AAT (Jorden et al., 1982). Several copies of this new preamplifier design have since been incorporated within the CCD camera systems now operational on the LPO 2.5m and 1m telescopes.

4.4.1 Video Preamplification and CDS Signal Processing Circuitry

Figure 4.8 is a schematic of the preamplifier video electronics in which four stages are identified: the output transistor source load, the first stage amplifier, the CDS processor and the output buffer. Figure 4.9 shows the relative timing of all the CCD drive clock waveforms and control clocks to read out each pixel.

(i) Output Transistor Source Load

The video waveform from the CCD output transistor is conveyed via screened coax to the preamplifier input where either a resistor or a constant current source load may be selected. Additional preamplifier input noise added by the current source was found to be negligible.

Several P8603 samples were tested to compare the small signal voltage gain (G) attainable from the output transistor with load type. The voltage gain was calibrated by measuring the DC potential on the output transistor source (V_{OS}) with varying potential on the reset transistor drain (V_{RD}) over a range typically ±0.3 V from nominal. Both load types were adjusted for an output transistor drain current Ids ≃ 1 mA. The CCD was cooled and back-clocked in darkness in order to prevent any spurious charge within the CCD from affecting the potential assumed to be present on the output node (i.e. V_{RD}). General conclusions drawn from those CCDs examined were:

VIDEO PREAMPLIFICATION AND CDS SIGNAL PROCESSING ELECTRONICS

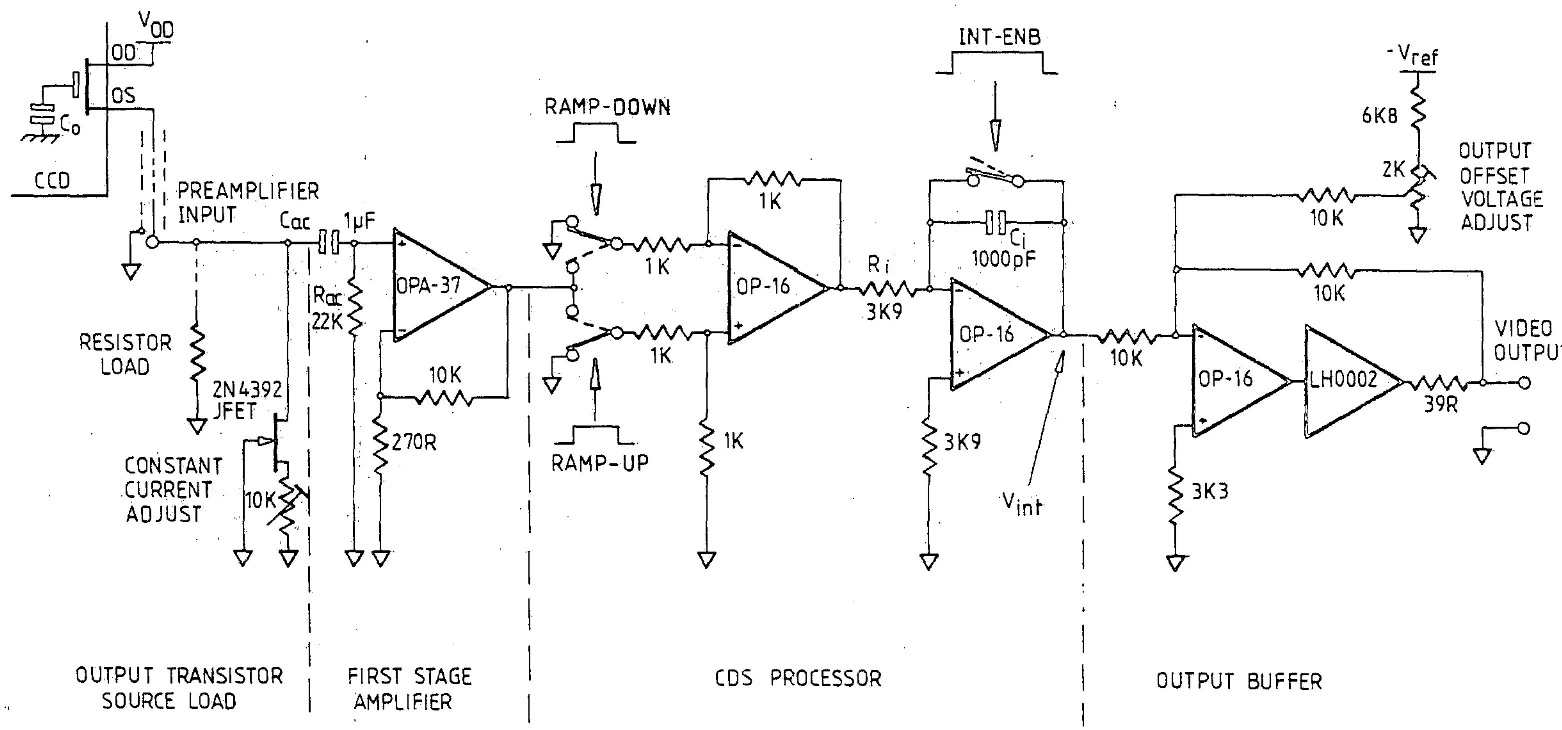


Figure 4.8

CCD CAMERA P8603 CCD PIXEL READOUT TIMING

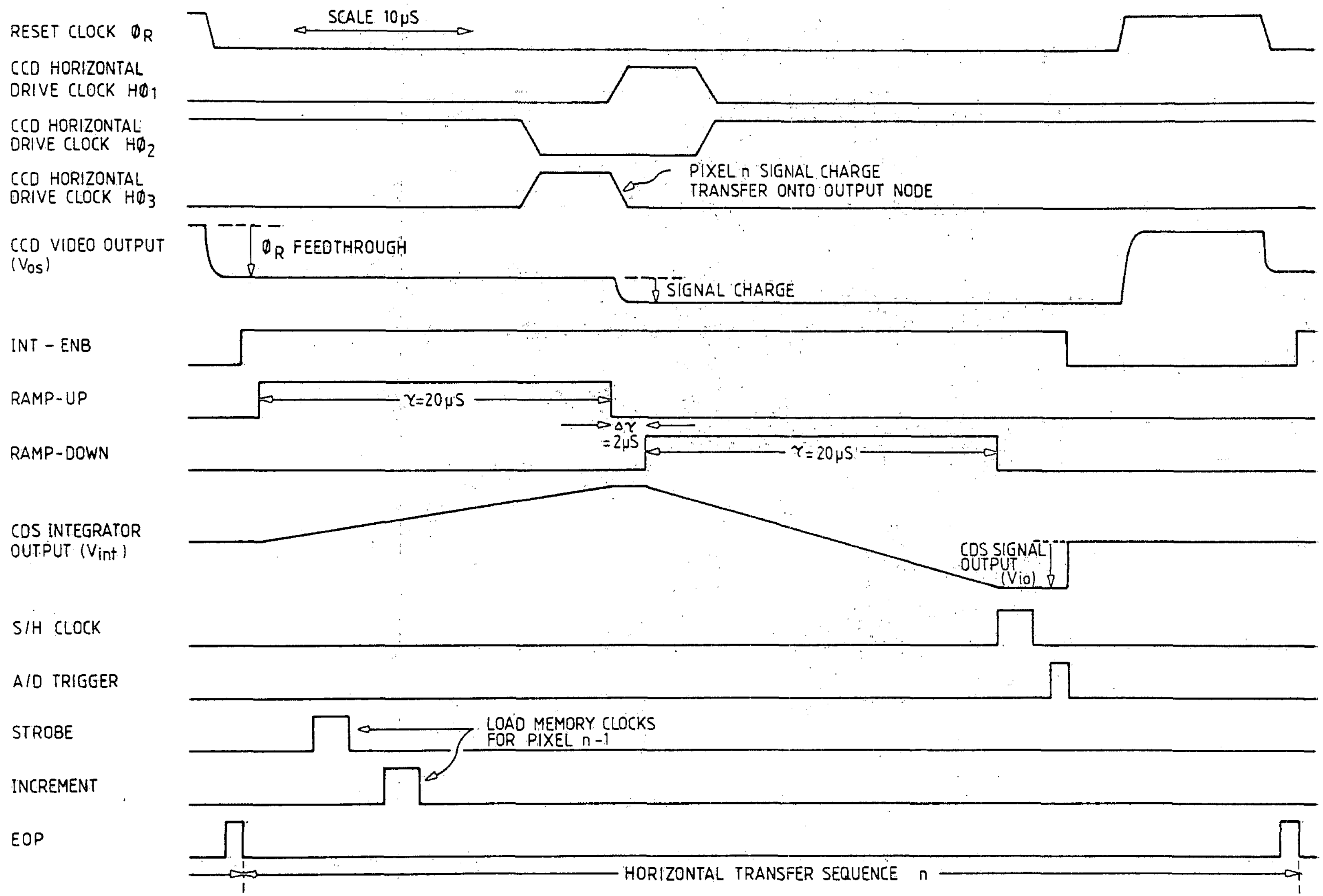


Figure 4.9

(i) using a resistor source load:

$$G = 0.50 - 0.55$$

(ii) using a constant current source load:

$$G = 0.65 - 0.70$$

Constant current source load operation was therefore adopted in order to maximize the charge to output voltage conversion sensitivity.

(ii) First Stage Amplifier

The CCD's video signal waveform on the output transistor source load is superimposed upon a large DC voltage component which must be substantially reduced prior to first stage preamplification in order to avoid amplifier saturation.

In the prototype design the video waveform was DC coupled into the first stage amplifier. Additional circuitry was used to introduce an adjustable DC offset voltage into the amplifier's input to cancel the video's DC component. However, it was found necessary to readjust this offset voltage when varying the CCD's operating temperature and when testing new CCD chips. This proved to be rather inconvenient and so the AC coupled design shown in Figure 4.8 was therefore adopted instead.

AC coupling has the effect of reducing white and 1/f noise but also of reducing the signal and the resultant S/N (Hegyi and Burrows, 1980). However, the degradation in S/N may be kept small provided that the time constant of the AC coupling (τac) is made large in comparison to the sampling period (τ) employed within a following CDS differential averager. Components Rac, Cac were therefore selected to provide an AC coupling time constant $\tau ac = 22$ ms which is of the same order as a one-line-sequence readout period (24 ms).

First stage preamplification is provided by an OPA-37 type op-amp, chosen for its low input noise specification (~ 3 nV/$\sqrt{\text{Hz}}$ at 1 KHz). The circuit is configured to provide a voltage gain $\simeq$ 38.

The input noise of this first stage op-amp is the dominant contribution to the total system noise of the preamplifier electronics. This however was not the case of earlier preamplifier designs in which a lower first stage voltage gain of ~ 10 was employed instead. A substantial proportion of the total system noise was found to originate at the inputs to the following differential averager and a redesign of this stage was necessary to reduce it. The first stage voltage gain was then increased to its current value to improve the preamplifier's signal transfer S/N still further.

(iii) CDS Processor

The CDS processor is of the differential averager type (or 'dual-slope integrator' after the method of its implementation). Based on a design by Marcus et al. (1979), it consists of:

- an op-amp configured as a unity voltage gain differential amplifier which in conjunction with analogue switches forms a switchable inverter.
- an op-amp integrator of time constant RiCi = 3.9 μs with a reset switch across its sampling capacitor.

With reference to Figure 4.9, the CDS signal processing within each pixel readout cycle follows a sequence in which:

- control clock **INT-ENB** enables the integrator by opening its reset switch.
- control clock **RAMP-UP** samples the video RESET potential over a period τ = 20 μs by switching the non-inverted video waveform output from the first stage amplifier through to the integrator. During this sampling period, the voltage output from the integrator (Vint) increases in the form of a linear ramp. The effective voltage gain developed is given by 20 μs/3.9 μs = 5.1.
- an interval $\Delta\tau$ = 2 μs is allowed for the transfer of the pixel's signal charge onto the CCD output node and settling of the video waveform.

- control clock RAMP-DOWN samples the video RESET + SIGNAL potential over an equivalent period τ = 20 μs. RAMP-DOWN switches the inverse of the video waveform from the first stage through to the integrator so that this time its output ramps negatively. Digitization of the preamplifier output is timed to succeed the completion of this second integration sample.
- the CCD output node is reset by $\emptyset_R$ and the CDS integrator is reset by INT-ENB prior to the next pixel's readout cycle.

The resultant voltage output from the integrator (Vio) after both samples may be expressed as:

$$Vio = -5.1\ Vs + Voff$$

where Vs = the step in the video waveform potential at the output of the first stage amplifier resulting from the pixel signal charge deposited on the CCD output node.

Voff = a small signal independent offset voltage (or output pedestal) arising in practice from clock feedthrough within the analogue switches.

In the absence of a signal charge step within the video waveform, the voltage ramps within the integrator are dependent upon the component of DC voltage present on the input to the switchable inverter. A large DC component will result in large voltage swings. Ideally, this should have no effect on the CDS output S/N provided that the integrator is not saturated. In practice, however, additional noise can be introduced because of unequal gains in the two integrations. In this case, a DC restoration (or clamping) of the video waveform prior to its input to the differential averager can improve the noise performance (Hopkinson and Lumb, 1982).

In this design (Figure 4.8), the DC component within the CCD video waveform is largely rejected by the AC coupling at the input to the preamplifier. Even with a first stage voltage gain ~ 40, the voltage ramps within the integrator are of ~ few volts only. More importantly, the input noise of the first stage amplifier was found to be large in comparison to the noise introduced by the differential averager. An initial DC restoration was therefore not considered to be necessary.

(iv) Output Buffer

The output buffer provides inverted unity voltage gain of the waveform output from the integrator. An adjustable DC offset voltage is introduced at its input to compensate for the integrator's output pedestal, and to enable a small positive DC offset to be added into the video signal conveyed to the digitization unit. A current driver was incorporated within the output circuitry largely for compatibility with RGO CCD camera systems in which the preamplifier is required to drive ~ 3 m cabling to a remote analogue-to-digital converter.

4.4.2 DC Bias Voltage Supplies

A schematic of the P8603 illustrating the connections of the drive clocks and the various DC bias voltage supplies needed to operate the chip is shown in Figure 4.10. The voltage levels required for a typical device are collected in Table 4.1.

The DC bias voltage supplies can be divided into two categories:

(i) supplies to the charge detection amplifier (V_{OD}, V_{RD}) and chip substrate (V_{SS}) which are required to be of high stability and minimal noise with ~ mA drive capability.

(ii) less critical supplies to gates at the extremities of the CCD charge transfer registers (V_{ABD}, V_{ABG}, V_{OG}) and the bias gate on the reset transistor (V_{BG}).

Details of the circuitry used to generate these supplies are shown within a complete schematic of the preamplifier electronics in

P8603 CCD BIAS VOLTAGE AND CLOCK CONNECTIONS

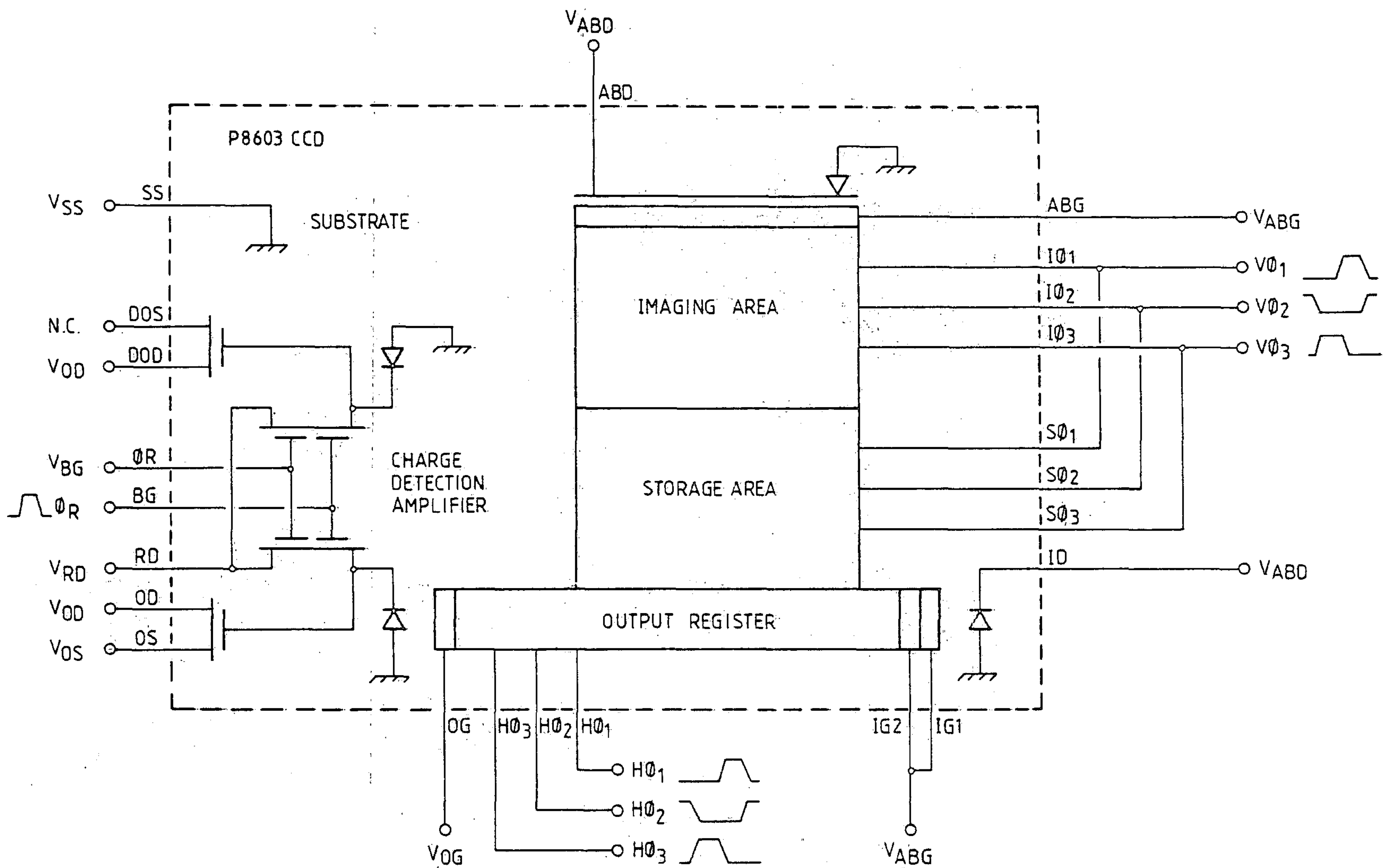


Figure 4.10

Figure 4.11. Those supplies for which a high stability is required are derived from a low noise precision voltage reference (LM299AH) the output of which is buffered and inverted to provide two higher drive current references (+Vref, -Vref). V_{OD}, V_{RD} and V_{SS} supplies are then generated from low noise op-amps (NE5533AN) which are configured as non-inverting amplifiers with adjustable input voltage sources utilising +Vref and -Vref. The use of a capacitor within the op-amp feedback loop provides a degree of low-pass filtering. Less critical supplies are derived from filtered potentiometer networks fed from the preamplifier's ±15 V supply rails. An op-amp provides a buffered current drive for the V_{ABD} supply.

CCD PREAMPLIFIER

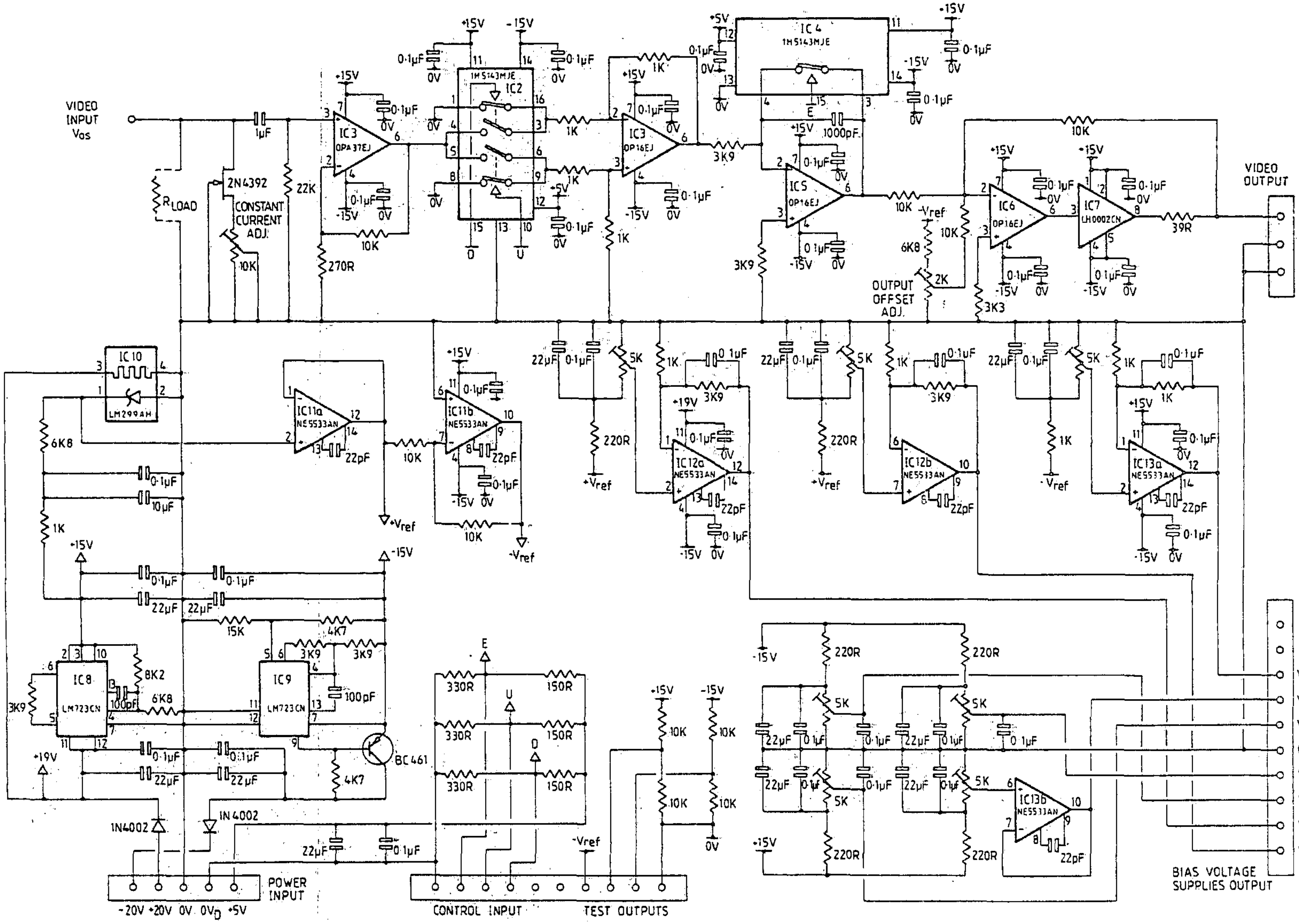


Figure 4.11

Table 4.1 TYPICAL P8603 CCD OPERATING VOLTAGES

P8603 CONNECTION	FUNCTION	CONNECTION	VOLTAGE (VOLTS)
$I\emptyset_1$ $I\emptyset_2$ $I\emptyset_3$	imaging area drive clock phases	$V\emptyset_1$ $V\emptyset_2$ $V\emptyset_3$	lower level -9 upper level +1 (1)
$S\emptyset_1$ $S\emptyset_2$ $S\emptyset_3$	storage area drive clock phases	$V\emptyset_1$ $V\emptyset_2$ $V\emptyset_3$	(1)
$H\emptyset_1$ $H\emptyset_2$ $H\emptyset_3$	output register drive clock phases	$H\emptyset_1$ $H\emptyset_2$ $H\emptyset_3$	lower level -9 upper level +1
$\emptyset_R$	reset clock	V_{BG}	14
SS	substrate	V_{SS}	-3
OD	output transistor drain	V_{OD}	17 (2)
OS	output transistor source	video o/p	~15.5
DOD	dummy output transistor drain	V_{OD}	(2)
DOS	dummy output transistor source	N.C.	-
RD	reset transistor drain	V_{RD}	7
BG	reset transistor bias gate	$\emptyset_R$	lower level -9 upper level +1
OG	output register output gate	V_{OG}	-7
ABD	anti-blooming drain	V_{ABD}	14 (3)
ABG	anti-blooming gate	V_{ABG}	-9 (4)
ID	output register input diode	V_{ABD}	(3)
IG_1	output register input gate 1	V_{ABG}	(4)
IG_2	output register input gate 2	V_{ABG}	(4)

4.4.3 Digitization Electronics

A schematic of the video digitization electronics is shown in Figure 4.12. The principal components are an Analogic MP271 sample-and-hold (S/H) amplifier and an Analogic MP8016 16 bit successive-approximation analogue-to-digital converter (ADC). The Analogic ADC was chosen since at that stage in the development programme, its linearity, accuracy and drift specifications were as good as any, but its conversion time (16 μs) was shorter than other comparable products. A discrete S/H was required and the MP271 was the natural choice as this unit is intended to complement Analogic's high resolution ADCs.

The ADC is operated in its unipolar mode over an input range 0-10 V (1 ADU ≡ 153 μV). Parallel data become available on the converter's outputs 16 μs after a conversion is initiated by a trigger pulse. The data are conveyed back to the CCD controller through output drivers which also provide some short-circuit protection of the relatively expensive ADC module. The MP271 S/H has a specified acquisition time of 1.1 μs to achieve ±0.005% accuracy of a 20 V input step. Its droop rate (2 μV/μs) is equivalent to ≈ 0.2 ADU over 16 μs and is therefore not a significant source of error.

The video output from the preamplifier is conveyed to the digitization electronics via a screened twisted-pair cable. To reduce the effects of any pickup in this cabling, the signal is fed into a differential amplifier contained within the ADC module. A direct connection to the S/H would have been preferable had the MP271 also incorporated differential inputs. Once the signal leaves the differential amplifier it is single-ended and so any pickup in the wiring to and from the S/H must be avoided. Miniature screened coax was employed in preference to PCB track connections.

Figure 4.9 shows the timing of the digitization electronics in relation to that of the preamplifier. On completion of the dual-slope integration, the resultant waveform is sampled over a 2 μs

CCD VIDEO DIGITIZATION ELECTRONICS

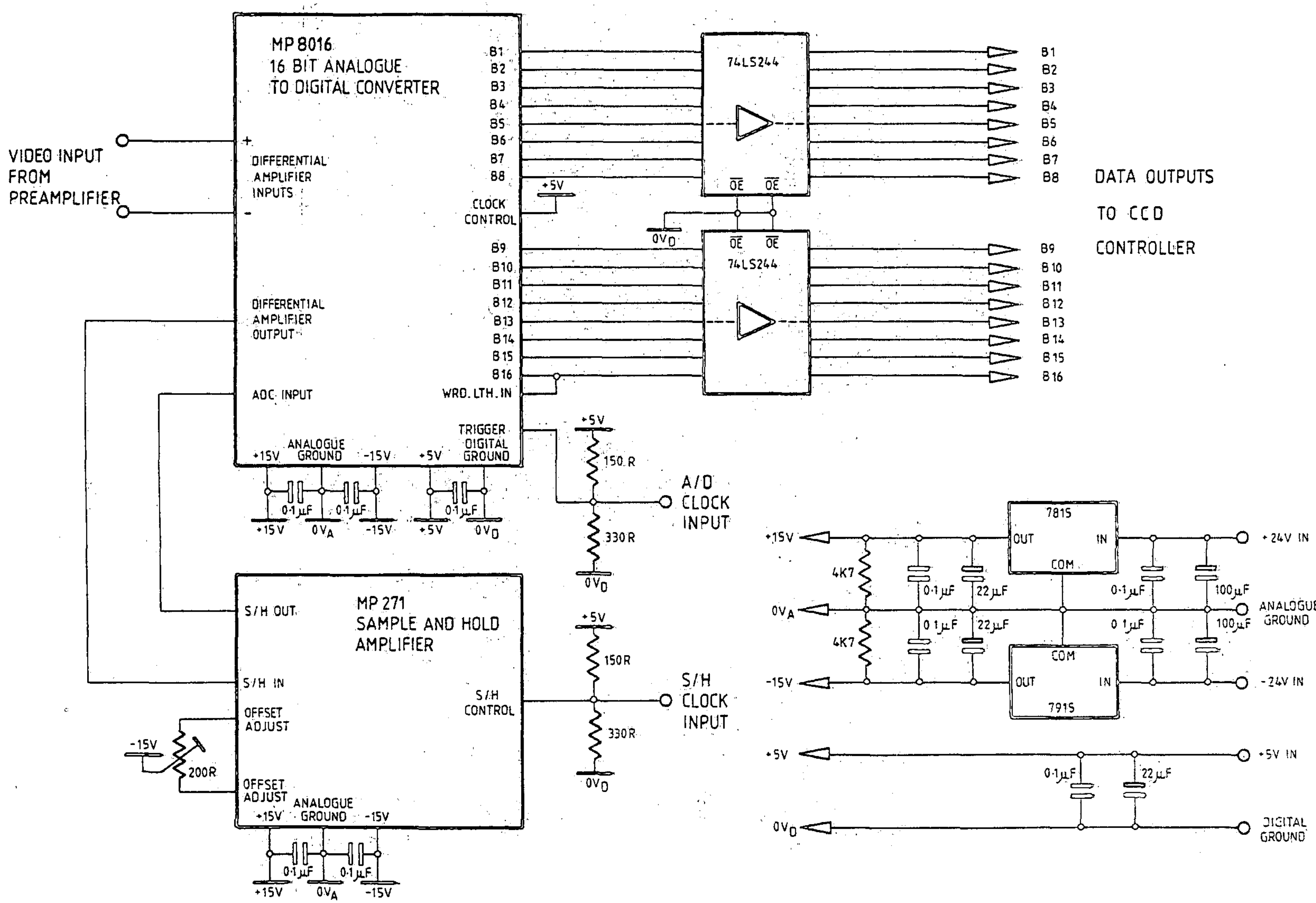


Figure 4.12

period under the control of a clock (S/H CLOCK) supplied to the MP271 from the camera's sequencing electronics. An independent 1 μs clock pulse (A/D TRIGGER) is used to trigger the ADC which digitizes the sampled video now held on the S/H output. Data are transferred through the CCD controller and into the CAMAC buffer memory module under the control of STROBE and INCREMENT clocks (see Chapter 3). In practice, the digital conversion and data transfer are overlapped with other operations within the pixel readout sequence in order to minimize the cycle time. In particular, data obtained from pixel n-1 are loaded into the memory by clocks generated within the nth horizontal transfer sequence.

4.4.4 Performance

The output S/N of the video signal processing electronics is determined by:

(i) the input noise of the first stage of the signal amplification circuitry.

(ii) the signal measurement bandwidth which is constrained by the CDS differential averager sampling period (τ).

With τ = 20 μs it was found that the input noise of the preamplifier corresponds to ≃ 1.54 μV rms and that this could be reduced by increasing τ so as to restrict the signal measurement bandwidth. The contribution to the total system readout noise (i.e. that of the CCD + electronics) from the readout noise of the CCD is however expected to dominate that from the electronics. Hence, the optimum value of τ which maximizes the output S/N of the system will depend on the output noise spectrum of the particular chip and should be set accordingly.

The input noise voltage of the electronics can only be expressed as an equivalent signal charge noise by referring it to the charge to output voltage conversion sensitivity of the CCD and this will vary from one chip to another. To illustrate typically achieved performance characteristics, results obtained from one particular

P8603 sample (serial no. 2055/15/13), in fact the chip used to commission FOS on the INT, are collected in Table 4.2. For this chip, the input noise of the electronics (with τ = 20 μs) can be expressed as an equivalent signal charge noise = 1.97 electrons rms. The total measured system noise was 7 electrons rms.

It was found that the value of τ = 20 μs is rather low with respect to minimizing the measured readout noise of P8603 CCDs. A better noise performance can be realized with τ = 40 μs as borne out by results presented in Chapter 5. In fact, τ had to be set at a value lower than optimal in order to avoid an inconveniently long chip readout time. A 60 μs pixel readout period was necessary to allow τ = 20 μs and so, ideally, this should yield a full-frame readout period given by:

$$400 \text{ pixels} \times 578 \text{ pixels} \times 60\ \mu\text{s} \simeq 14 \text{ seconds}$$

In practice, however, the 2:1 overhead in the CCD camera's data acquisition system (see Chapter 3) results in a total readout time ≃ 28 seconds.

With τ = 40 μs the total system noise was reduced to ≃ 6 electrons rms but the chip readout time was increased to ≃ 1 minute. Having discussed this with colleagues, it was decided not to exploit this improvement in noise performance while attempting to commission FOS on the INT because it was concluded that it would not justify the increased chip readout time.

Table 4.2 TYPICAL P8603 AND PREAMPLIFIER PERFORMANCE CHARACTERISTICS

(i) P8603 CCD (serial no. 2055/15/13) characteristics

charge to output voltage conversion sensitivity (ΔV_{OS})	= 0.78 μV/electron
measured output transistor voltage gain (G)	= 0.64
calculated output node capacitance (Co)	= 0.13 pF

(ii) video signal processing electronics configuration and performance

preamplifier first stage voltage gain	= 38
CDS processor voltage gain	= 5.1
total preamplifier voltage gain (A)	= 195
CDS integration period (τ)	= 20 μs
CDS sampling interval ($\Delta\tau$)	= 2 μs
digitization resolution	= 16 bits
digitization input	= 153 μV/ADU
measured preamplifier input noise	= 1.97 ADU rms
"	= 1.54 μV rms

(iii) combined performance of the CCD and the electronics

measured signal-to-ADU system responsivity (1/g)	= 1.0 electrons/ADU
measured preamplifier input noise (σip) in equivalent signal charge	= 1.97 electrons rms
measured system readout noise (σt) in equivalent signal charge	= 7 electrons rms
calculated readout noise of the CCD alone = $\sqrt{(\sigma t^2 - \sigma ip^2)}$	= 6.7 electrons rms

CHAPTER 5

LABORATORY EVALUATION OF THE GEC P8603 CCD

5.1 Introduction

The first questions asked about a CCD when assessing its suitability for an astronomical project are usually those concerning its quantum efficiency, spectral coverage and readout noise. It is arguable, however, that there are other aspects of a CCD's performance which are equally important, particularly with regard to its imaging characteristics at astronomically relevant light levels. An important requirement, for example, is that there is no deterioration in the charge transfer efficiency of a device at low signal levels, since this may give rise to a non-linear response in low light level applications.

As part of the FOS development programme, a series of investigations was undertaken in order to characterize the imaging properties of the GEC P8603 CCD, determine its limitations and optimize those aspects of its performance over which there is some control. In this chapter, the ways in which the characteristics were measured, the results and their implications are discussed.

The programme was embarked upon in earnest in mid 1983 while FOS was still being manufactured in Durham. In September 1983, the author left Durham to take up a post at the RGO, enabling him to see FOS through to completion and to engage in further work with CCDs. The latter has entailed laboratory evaluation and comparison of RCA, Thomson-CSF and GEC CCDs. This work has already been described (Thorne et al., 1986a) but it is appropriate that some of the results relevant to the P8603 (some of which were obtained after FOS had been commissioned on the INT) should be included here in order that a full report of the P8603's characteristics can be given.

5.2 Responsive Quantum Efficiency and Spectral Range

One of the main advantages of CCDs compared to other detectors used in optical astronomy is their high responsive quantum efficiency, particularly in the red, and their wide spectral coverage.

The spectral response of the GEC CCD was measured at the RGO with the aid of a low light level calibrated source developed by Jelley (1983). The wavelength was defined using a set of narrow band filters of $\Delta\lambda = 5$ nm spaced at ~50 nm intervals.

Curves for several P8603s are shown in Figure 5.1. The results can be summarized as follows:

(i) peak RQE ~42-46% at ~740 nm.

(ii) 10% points occur at ~460 nm and ~930 nm.

(iii) 1% points occur at ~390 nm and ~1020 nm.

It should be noted that the overall responsivity was found to be greater than that assumed for the GEC CCD when the estimates of the throughput efficiency of FOS were first calculated (see Chapter 2), but there is some evidence that the RQE did improve over this period (Thorne, 1986).

One of the chips (serial number 2047/3/20) has subsequently been coated at the European Southern Observatory (ESO) with a fluorescent plastic film designed to increase the responsivity of GEC CCDs in the blue (Cullum et al., 1985). It was found that its RQE had been increased to ~8-13% between 310 and 450 nm and that its response at wavelengths greater than 500 nm had not been significantly affected by the coating. No tests have so far been performed to determine whether or not a single electron per photon process is involved, and the possibility of hysteresis effects needs to be investigated. Nevertheless, the results do show the potential of the coating process for obtaining some blue and near ultraviolet response from a front-illuminated CCD.

The results reported so far were obtained with the CCDs' operating temperature set to 150 K which was found to be the optimum value with respect to minimizing readout noise while maximizing charge transfer efficiency. Quantum efficiency is known, however, to be a function of a CCD's operating temperature; it decreases with decreasing temperature because of an increase in the band gap energy of silicon and a reduction in the density of phonons necessary for indirect transitions (EEV

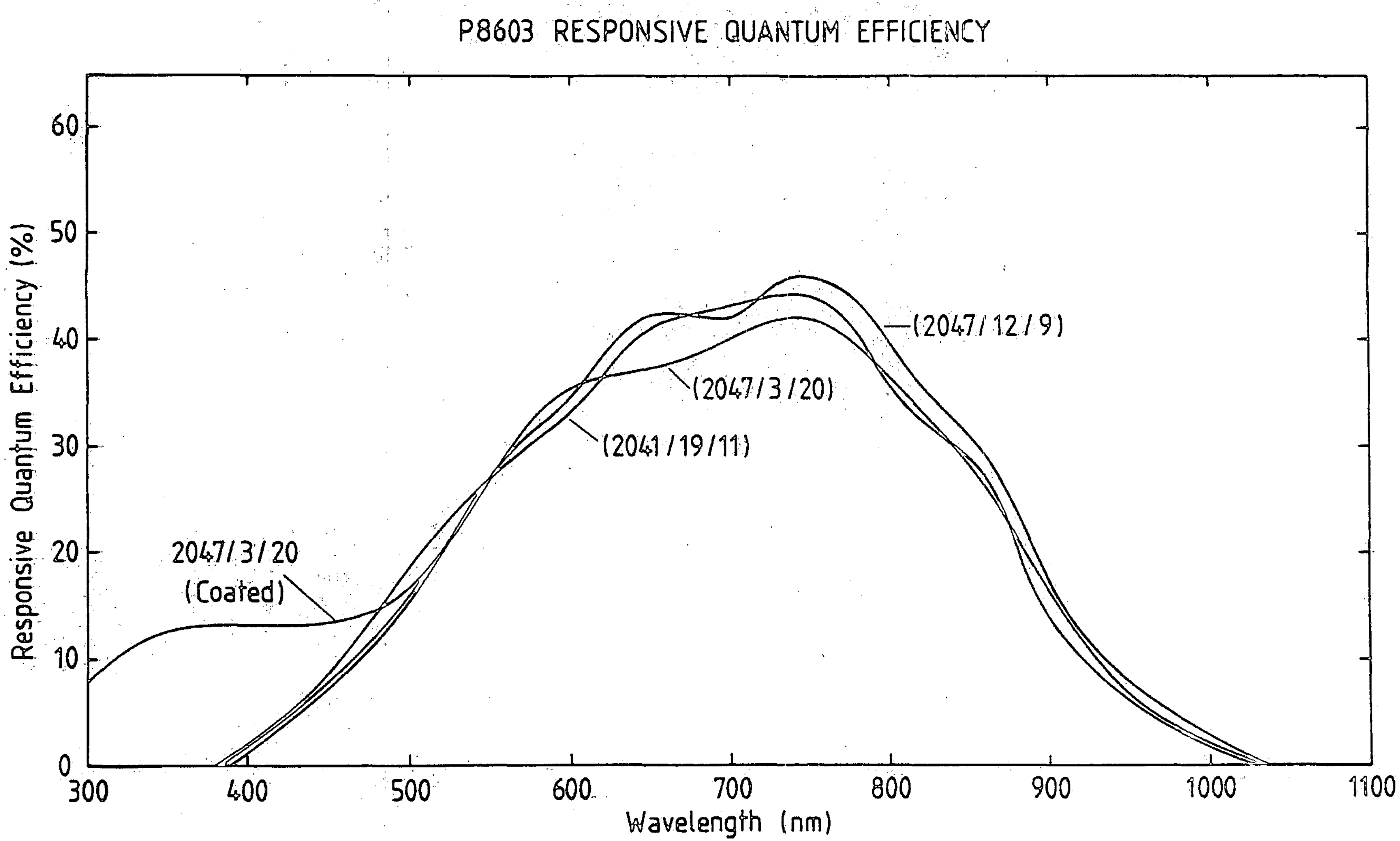

P8603 RESPONSIVE QUANTUM EFFICIENCY
Responsive Quantum Efficiency (%)
0
10
20
30
40
50
60
300
400
500
600
700
800
900
1000
1100
Wavelength (nm)
2047/3/20
(Coated)
(2047/12/9)
(2047/3/20)
(2041/19/11)

Figure 5.1

Technical Note No. 6, 1982; Dash and Newman, 1955). Variations in the P8603's RQE with temperature have been investigated (Thorne et al., 1986b) and the results for one chip are shown in Figure 5.2. Although the effect is not large, it is measurable and suggests, as expected, that the CCD should be operated at as high a temperature as possible in order to maximize its responsivity in the red.

5.3 Readout Noise

The readout noise of the P8603 was measured by:

(i) obtaining a value of the readout noise in analogue-to-digital units (ADUs) by measuring the noise within a 20 x 20 pixel array on an erase frame, i.e. a frame with zero signal charge obtained by reading out the CCD in darkness immediately after clearing the chip of any residual charge.

(ii) calibrating the charge to ADU conversion sensitivity of the CCD and signal processing electronics system to enable the value of readout noise obtained from the erase frame to be converted to an equivalent signal charge noise figure.

The calibration procedure was performed in the following manner:

(i) with the CCD uniformly illuminated, a pair of exposures of equal integration period were taken for various exposure times.

(ii) for each pair, one frame was subtracted from the other in order to correct for pixel to pixel non-uniformities.

(iii) the mean signal level for each pair of exposures and the variance within a 20 x 20 pixel array from each subtracted pair were measured. Care was taken to ensure that the 20 x 20 pixel array was chosen within a 'clean' area of the chip, i.e. an area free of 'traps' and 'column defects' (see Section 5.5).

(iv) variance was plotted as a function of the mean signal level after allowing for the factor of two increase in variance introduced in

P8603 RQE AS A FUNCTION OF TEMPERATURE

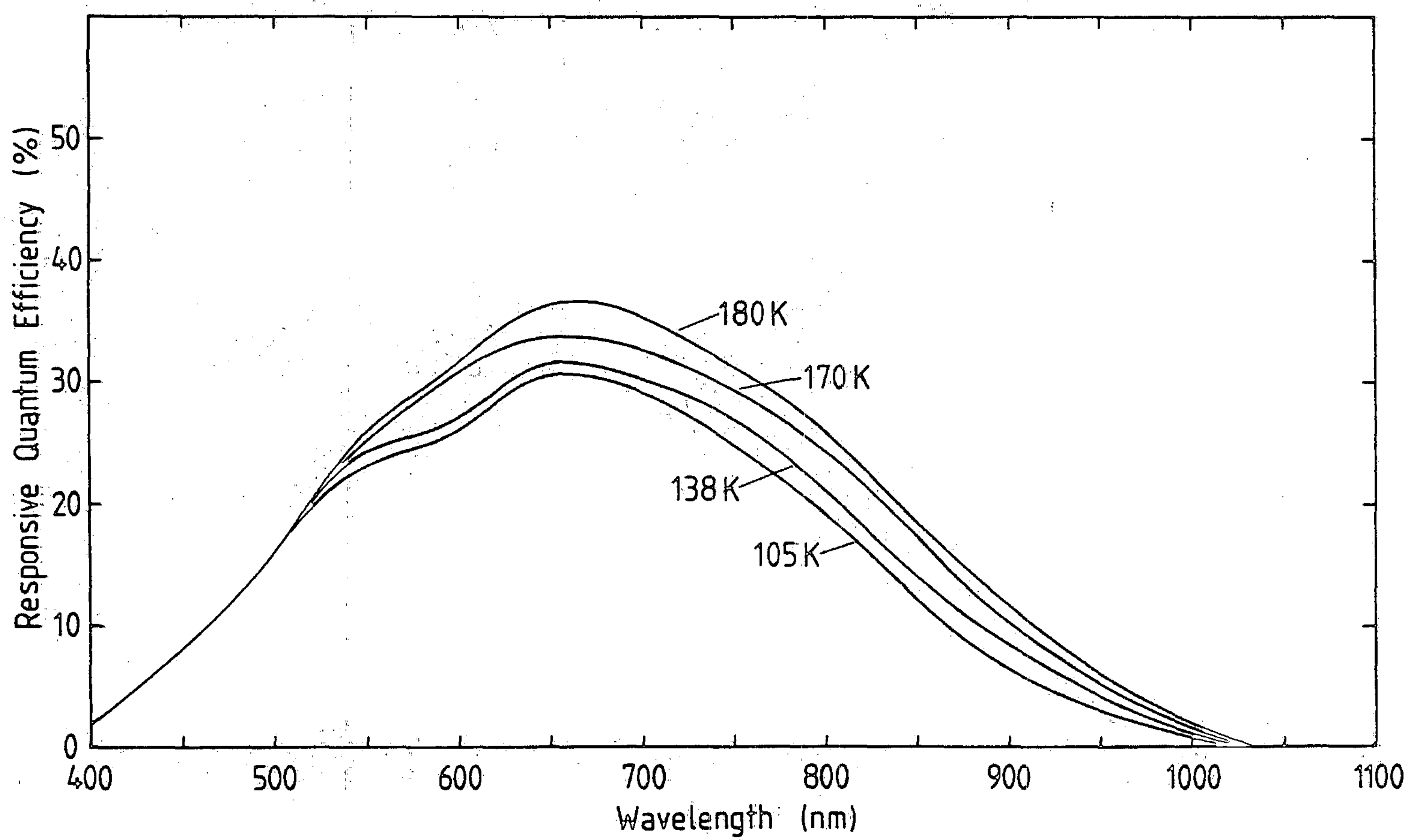


Figure 5.2

the subtraction process. This yields a straight line with gradient equal to the system gain expressed in ADUs per electron.

The readout noise of the P8603 was expected to be a function of the operating conditions of its output transistor (i.e. its drain-source current) and of the sampling period (τ) employed within the correlated double sampling (CDS) signal processing electronics (see Chapter 4). However, it was also discovered to be a function of its operating temperature with a dependence of a previously unreported nature.

(i) Temperature dependence

The temperature dependence of readout noise was in fact discovered by accident when the operating temperature of a CCD rose as a result of the cryostat unexpectedly running out of coolant. Other chips were subsequently investigated and found to show a similar effect, albeit to varying degrees. Curves for several P8603s are shown in Figure 5.3.

All chips were found to show a peak in their readout noise at a temperature of ~120–130 K but the magnitude of the peak with respect to the lowest level was found to vary from chip to chip. The possibility of the effect being due to a change in the voltage gain of the CCD's output transistor was investigated but found not to be the cause. A satisfactory explanation of this effect has not so far been established.

The curves show that there are two regions which offer the lowest readout noise:

(i) $T \lesssim 110$ K

(ii) $T \gtrsim 145$ K

Whether to operate in the higher or the lower range largely depends on other chip characteristics, namely quantum efficiency, dark current and charge transfer efficiency. With regard to these:

(i) Quantum efficiency, as has already been noted, increases with increasing temperature.

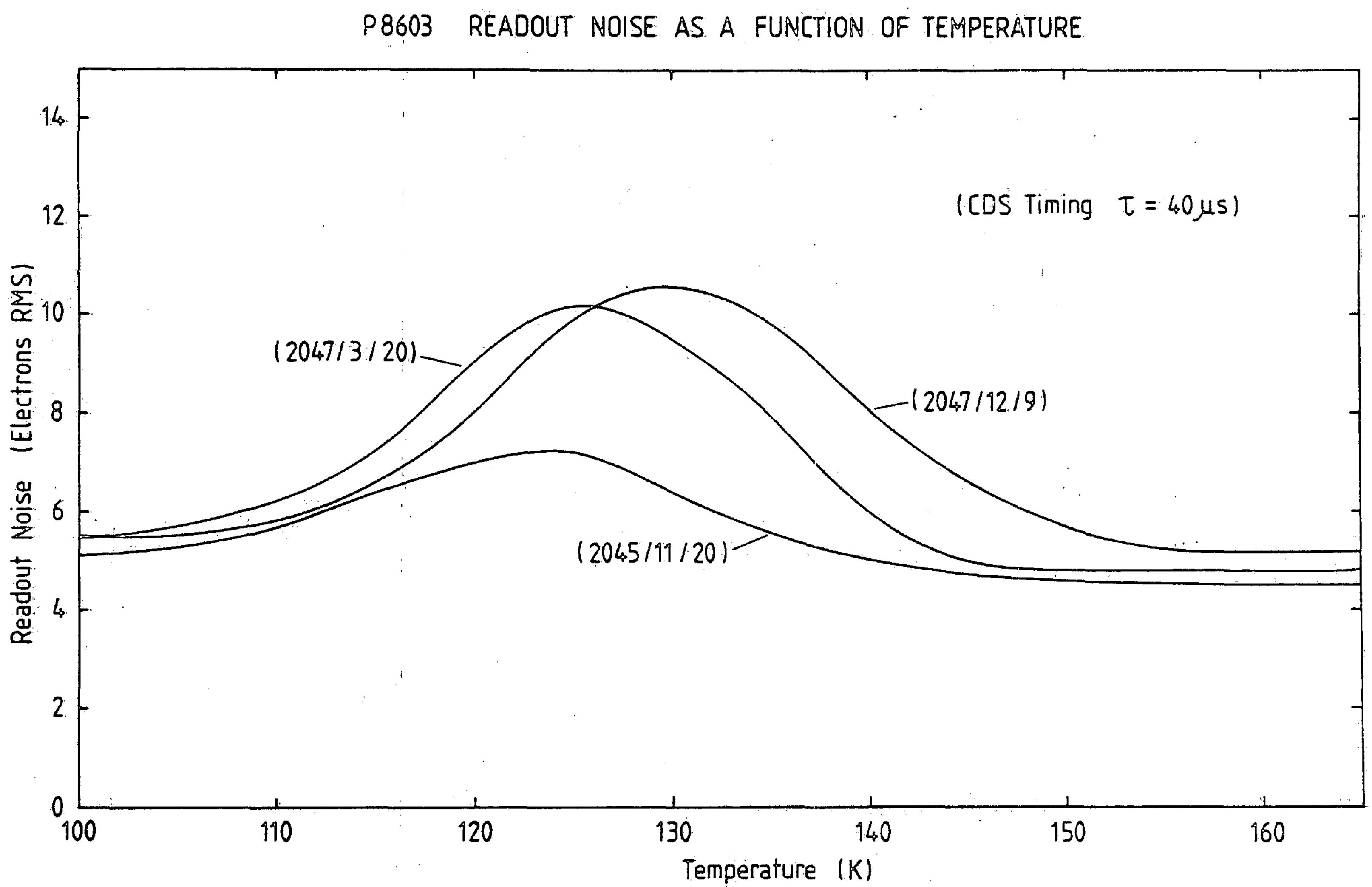

P8603 READOUT NOISE AS A FUNCTION OF TEMPERATURE
(CDS Timing τ = 40 µs)
(2047/3/20)
(2047/12/9)
(2045/11/20)
Readout Noise (Electrons RMS)
Temperature (K)
0
2
4
6
8
10
12
14
100
110
120
130
140
150
160

Figure 5.3

(ii) Dark current was found to be still negligible at a temperature of 150 K.

(iii) Some chips were found to exhibit a deterioration in their charge transfer efficiency with decreasing temperature when comparisons were made in the two temperature ranges of interest.

These additional considerations suggest, therefore, that for optimum performance, the P8603 should be operated in the higher temperature range at ~ 150 K.

(ii) CDS sampling period (τ) dependence

The curves shown in Figure 5.4 are a representative sample of the results obtained from measuring readout noise as a function of the sampling period (τ) used within the CDS signal processing electronics. The overall results can be summarized as follows:

(i) In the range $\tau \lesssim 40$ μs, readout noise was found to decrease with increasing τ which is attributable to an increasing attenuation of white noise as the system bandwidth is reduced.

(ii) In the range τ = 40-60 μs, the dependence was found to vary from chip to chip. Many chips were found to exhibit a further but small decrease. For others, the noise was observed to have become independent of τ (as exhibited by chip 2047/3/20, for example, in the range τ = 40-50 μs), revealing the noise floor of the system which is characterized by the power of 1/f noise in the output transistor.

(iii) In the range $\tau \gtrsim 50$ μs, readout noise was sometimes observed to start to increase with increasing τ, which is attributable to $1/f^2$ noise becoming dominant with respect to the 1/f noise (see Chapter 4). The value of τ for which this effect starts to occur, however, was found to vary markedly from chip to chip. Chip 2047/3/20, for example, was found to exhibit a slight increase in its noise in the range τ = 50-60 μs, while for other chips, no such effect was observed with τ as long as 80 μs.

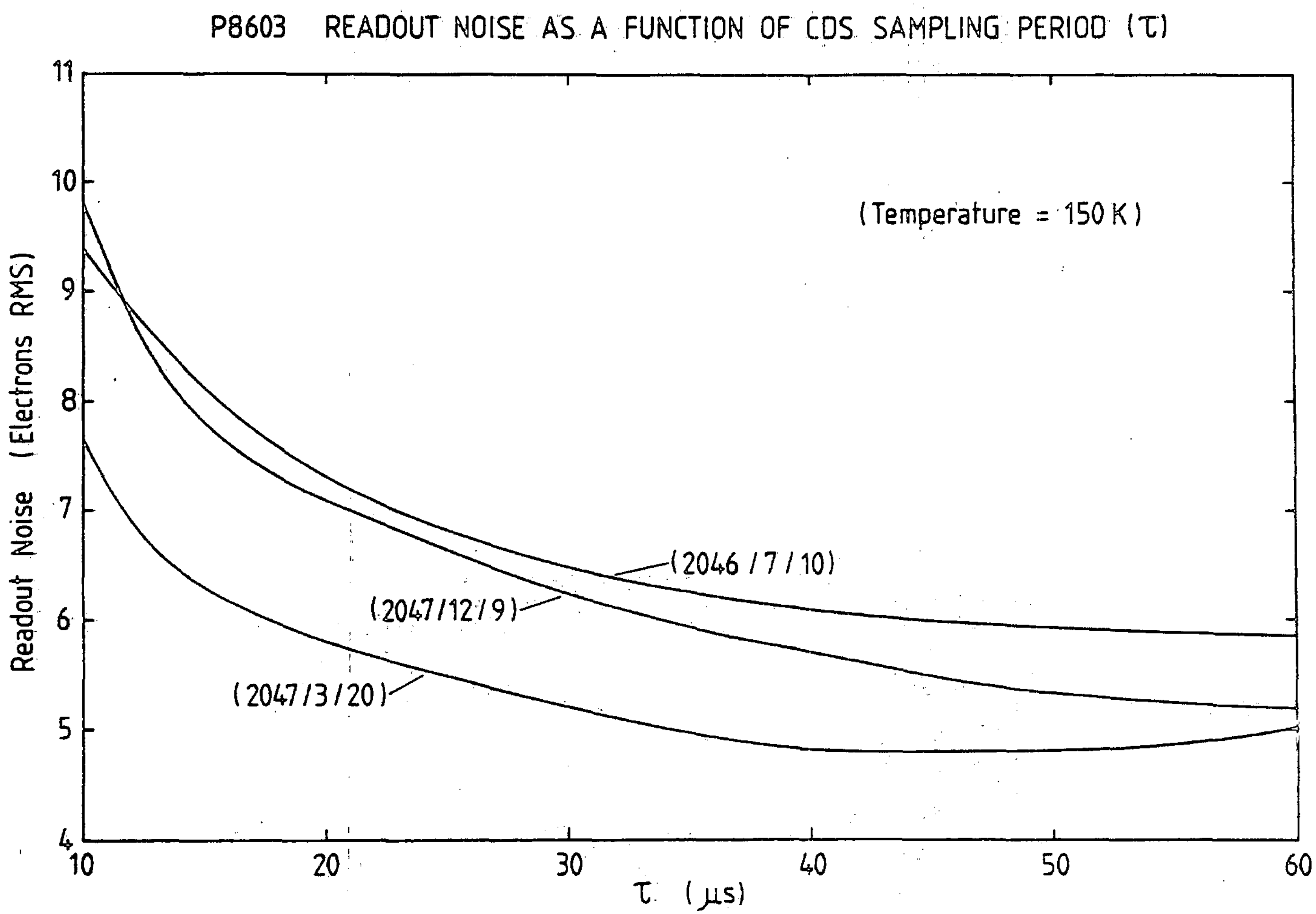

P8603 READOUT NOISE AS A FUNCTION OF CDS SAMPLING PERIOD (τ)
(Temperature = 150 K)
Readout Noise (Electrons RMS)
τ (μs)
(2046 / 7 / 10)
(2047/12/9)
(2047/3/20)
4
5
6
7
8
9
10
11
10
20
30
40
50
60

Figure 5.4

The value of τ to use largely depends, therefore, on the output noise spectrum exhibited by the particular chip in question. Often, it may well have to be a compromise between that necessary to achieve the lowest readout noise possible, and a somewhat lower value chosen to avoid making the time required to read out the chip inconveniently long. Considerations of this nature, however, are of course application dependent.

(iii) CCD output transistor drain-source current

It was expected that the GEC CCD would show a transition in its output noise when changing from surface to buried-channel operation, dependent on the bias voltages applied to the output transistor (see Chapter 4). In general, P8603s have been operated with Ids $\simeq$ 1 mA which satisfies the conditions necessary to ensure buried-channel operation. A factor of two increase in noise was observed by increasing the current above 2 mA (at T $\simeq$ 150 K). No significant decrease in noise was observed by operating with Ids < 1 mA.

As a result of optimization with respect to all of the factors discussed above, a readout noise of ~5 electrons rms was achieved with most P8603s tested. Some chips were found to exhibit slightly worse noise in the range 6-10 electrons rms, while the best device tested to date was measured at 3.5 electrons rms.

5.4 Charge Transfer Efficiency and Threshold Effects

The most important aspect of a CCD's performance is arguably its charge transfer efficiency (CTE); the ability of the device to transfer a charge packet from one potential well to the next. Incomplete transfer results in some charge being left behind, which appears in the readout as a deferred charge 'tail' in pixels trailing that within which the packet was originally collected.

The CTE performance quoted of the best devices available to date is typically ~0.99995/transfer. It is now recognized, however, amongst those developing CCD systems for optical astronomy, that the CTE quoted by a CCD manufacturer can usually be taken only as a figure for the performance to be expected at moderately high illumination levels (i.e. $\gtrsim 10^3$ electrons/pixel). At the lowest signal levels typically encountered in astronomical work (~ 10-100s electrons/pixel), CTE is often found to be much worse (see for example: Gursky et al., 1980; Geary and Kent, 1981; Gunn and Westphal, 1981; Blouke et al., 1983; Thorne et al., 1986a).

Poor CTE at low signal levels has been attributed to the presence within a device of 'spurious potential pockets' (see for example: Janesick et al., 1984). These are localized either within or adjacent to the charge transfer channels and are generally found to occur either at the interface between a chip's imaging area and its readout register, or within the pixels themselves. The effect of an empty pocket is to capture charge until it is full. The fact that a certain amount of charge is needed to fill the pocket before any further charge can be transferred past it means that it gives rise to a 'threshold effect'. The subsequent release of charge from the pocket into empty, trailing pixels is seen as a deferred charge tail and therefore as poor CTE.

The CTE performance with regard to GEC CCDs was found to vary from chip to chip but the overall conclusions can be summarized as follows:

(i) vertical CTE (i.e. CTE along the imaging area columns)

- it was found that a certain amount of smearing of a charge packet detected on a zero background (i.e. otherwise empty potential wells) is not uncommon. This is most clearly observed in the smearing of cosmic ray events detected on a chip with zero background charge (Figures 5.5 and 5.6).

(ii) horizontal CTE (i.e. CTE along the output register)

- horizontal CTE was found to be generally good, independent of whether there is any background charge present or not. However, one particular chip was found to exhibit quite poor CTE with cosmic ray events being smeared over many pixels (Figure 5.7). The cause of this was eventually traced to a 'trap' defect located within the output register quite close

VERTICAL SMEARING OF COSMIC RAY EVENTS

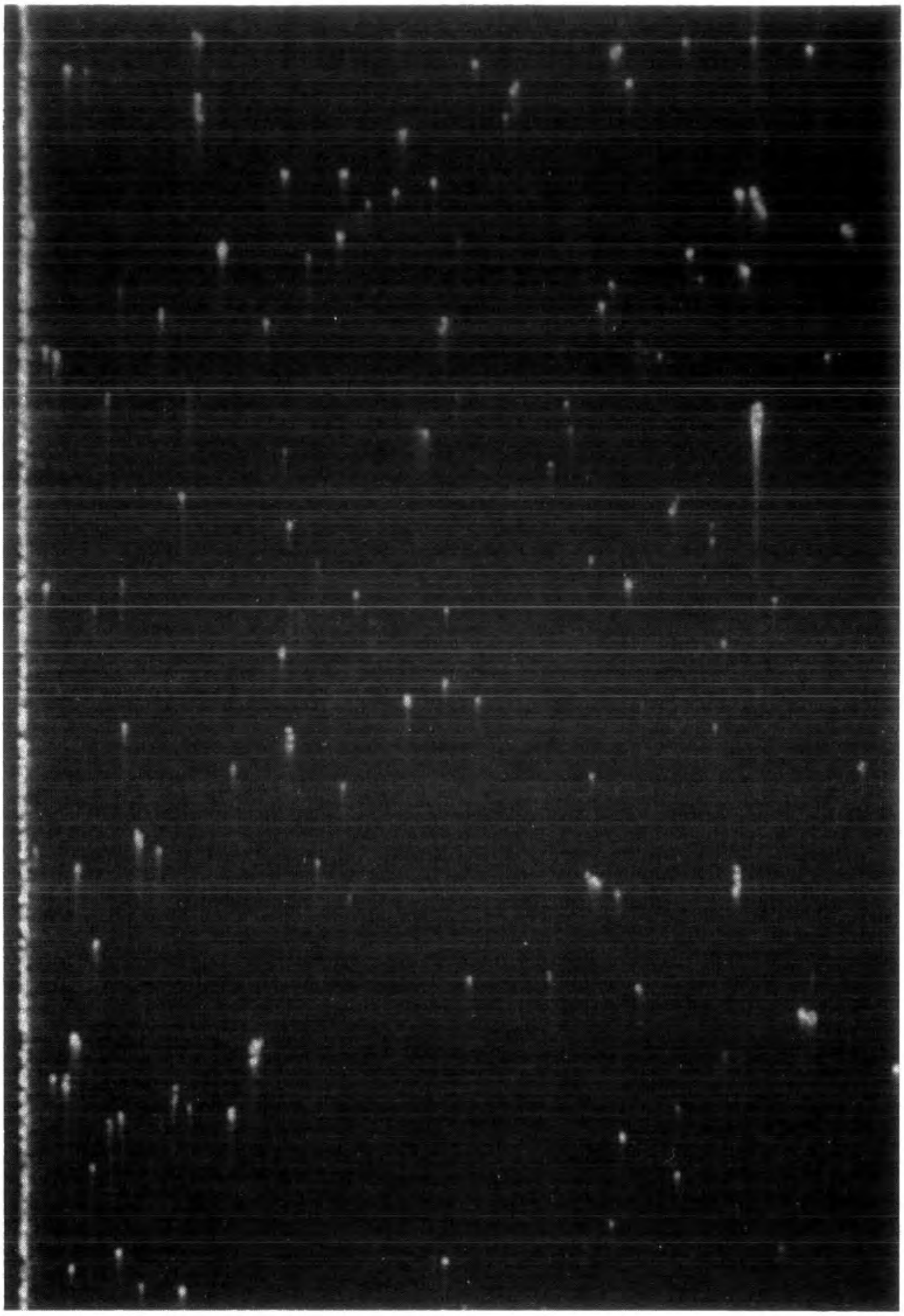


Figure 5.5

VERTICAL SMEARING OF COSMIC RAY EVENTS

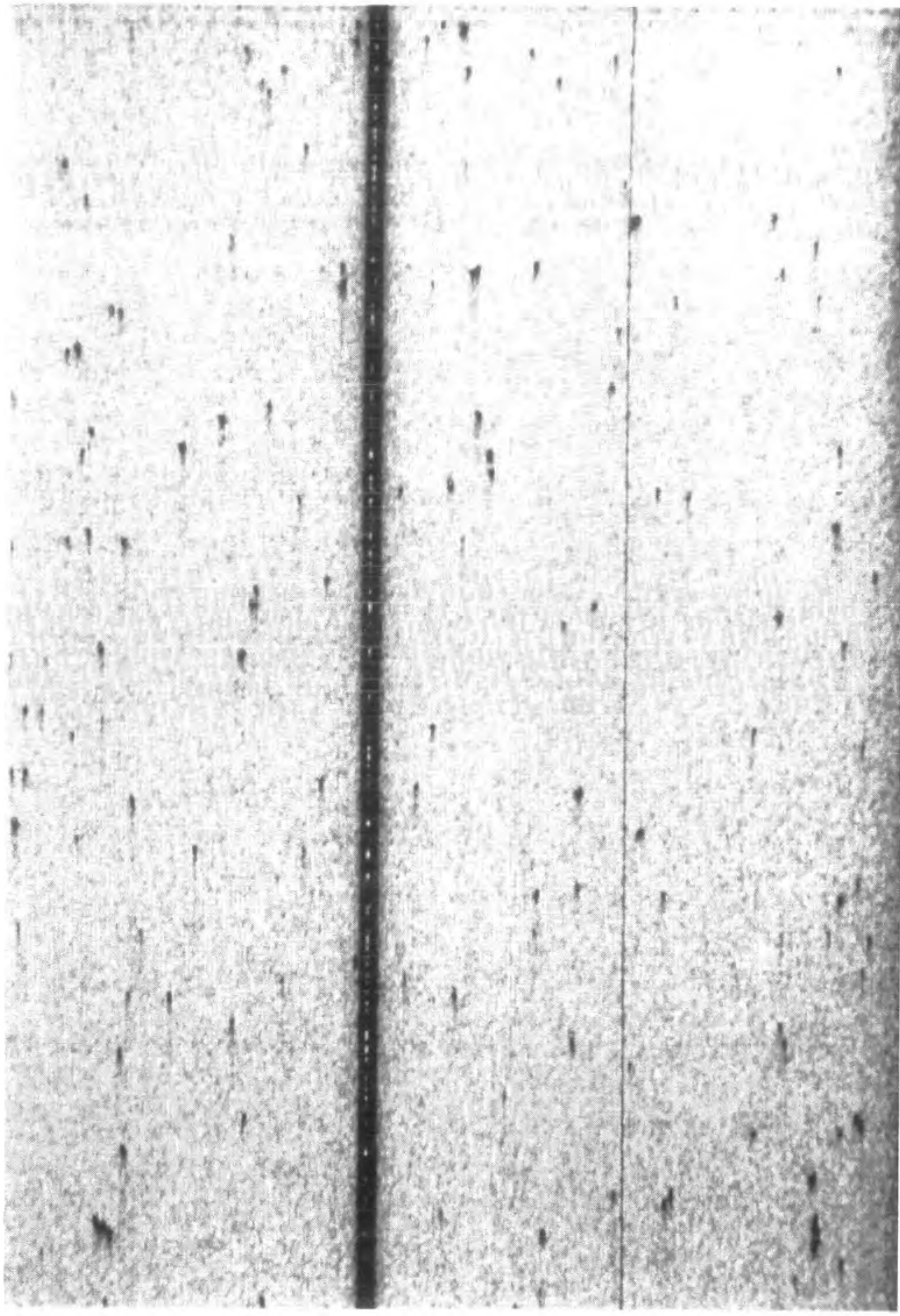


Figure 5.6

HORIZONTAL SMEARING OF COSMIC RAY EVENTS

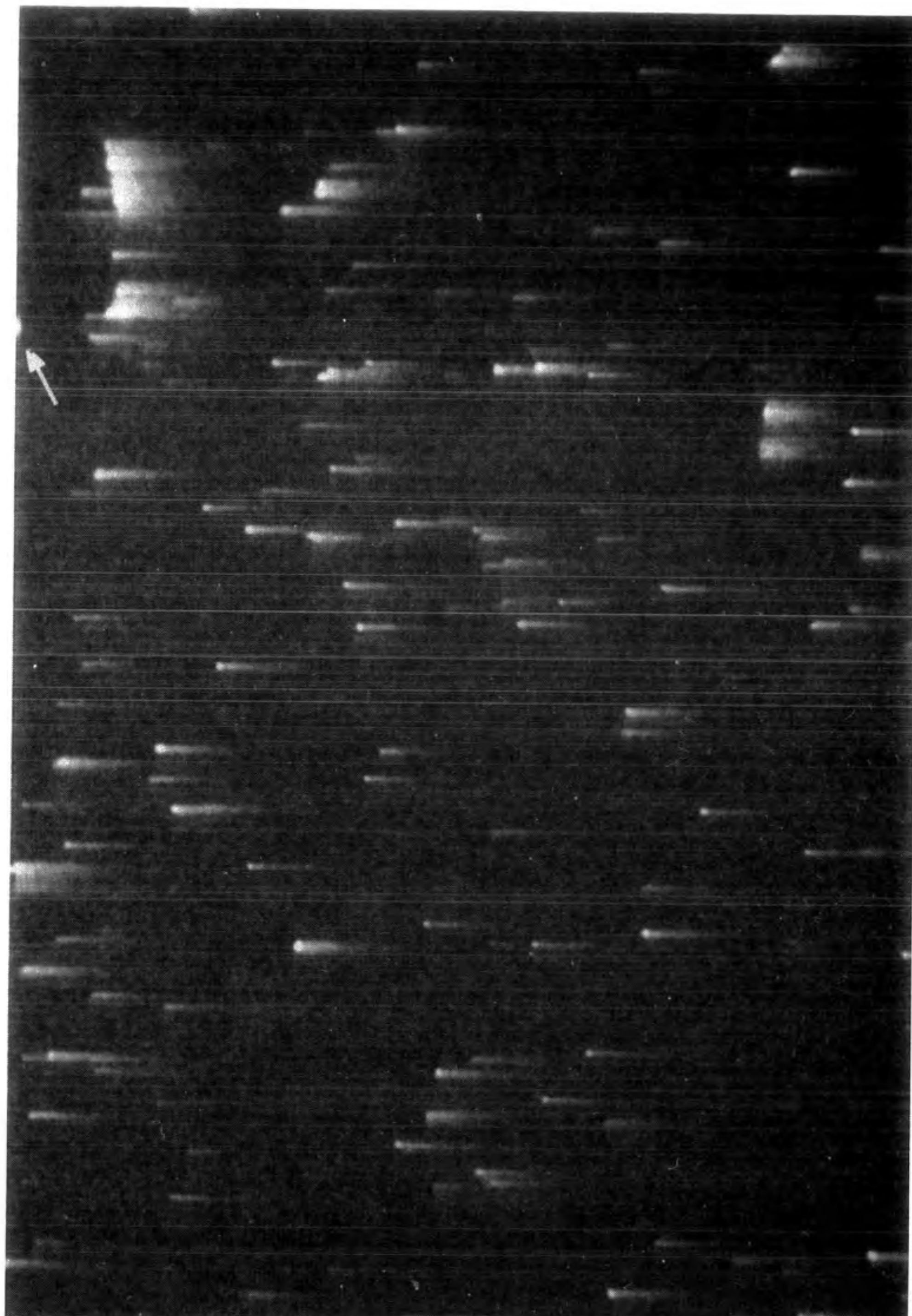


Figure 5.7

to the charge detection amplifier. This is demonstrated by the single cosmic ray event (marked in Figure 5.7) read out on the output side of this trap which shows no deferred charge tail.

The more serious problem, therefore, is the vertical smearing of charge on a zero background. This may cause severe non-linear distortions in line profiles in low light level spectroscopic applications if the dispersion is in the vertical direction. It was thought that this problem could be attributable to:

(i) bulk trapping states (Mohsen and Tompsett, 1974) within the imaging area, and/or

(ii) the transfer from the imaging area into the output register.

However, because there was found to be no significant difference in the extent to which cosmic ray events were being smeared at opposing ends of the imaging area, it was suspected that the problem was arising not in the imaging area itself, but instead, at the interface between the imaging area and the output register (to be referred to as the 'V→H' interface). To investigate this further, a series of low level uniform illumination exposures were taken; the images reproduced in Figures 5.8 and 5.9 show examples of the results. Charge has clearly been lost from the first few rows to be read out (i.e. those closest to the output register at the top of the image) which is symptomatic of a threshold effect. There is also some column to column variation in the severity of the problem as shown by the jaggedness of the threshold edge. When exposures of differing illumination level were taken, the product of the exposure level (i.e. electrons/pixel) and the mean number of empty rows was found to be constant and this was defined as the threshold level. Not all GEC CCDs were found to show this effect but for those that did, the threshold level was ~ 300 electrons.

The questions which then arise are:

(i) what can be done to overcome the presence of a V→H threshold.

V→H THRESHOLD

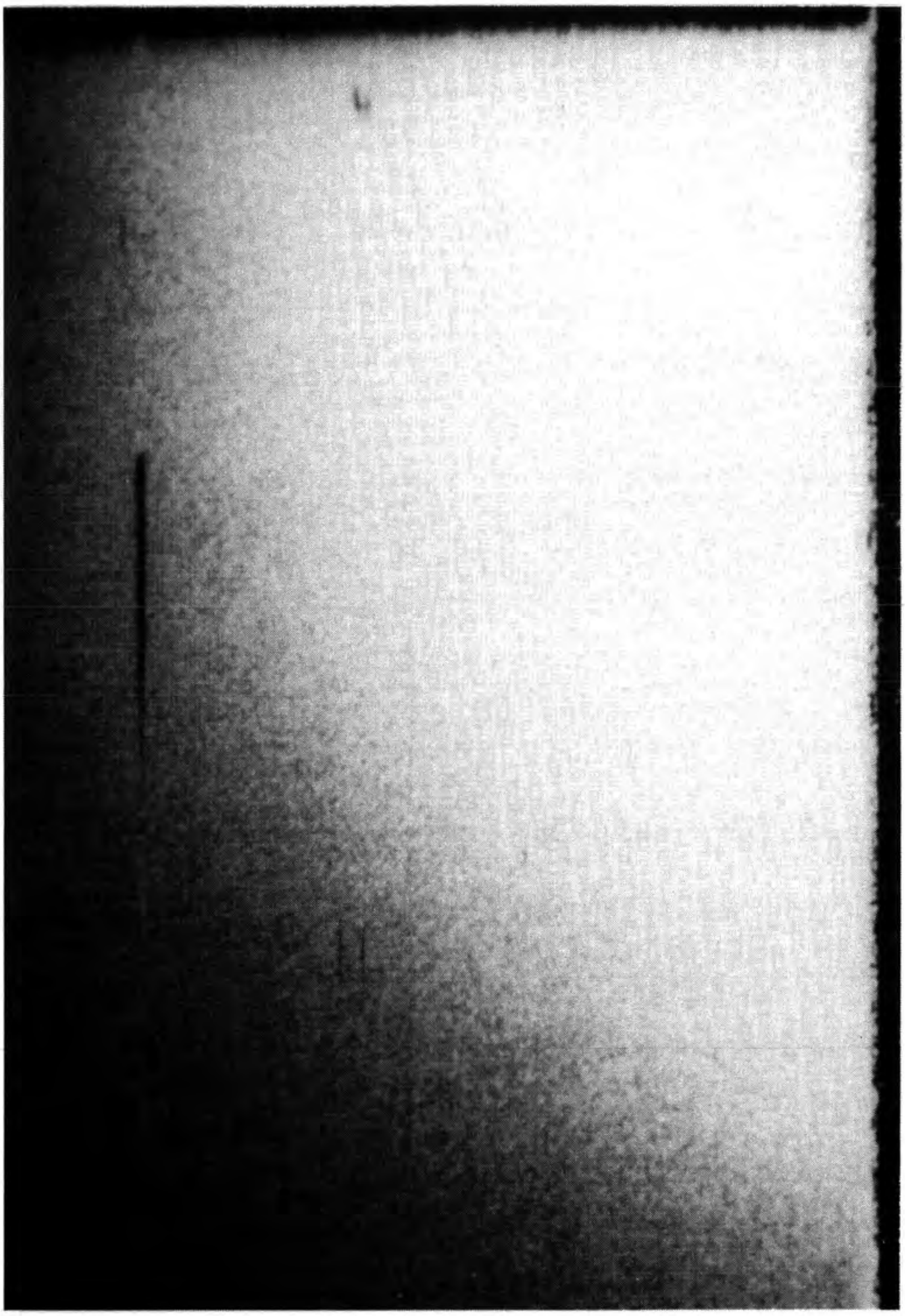


Figure 5.8

V→H THRESHOLD

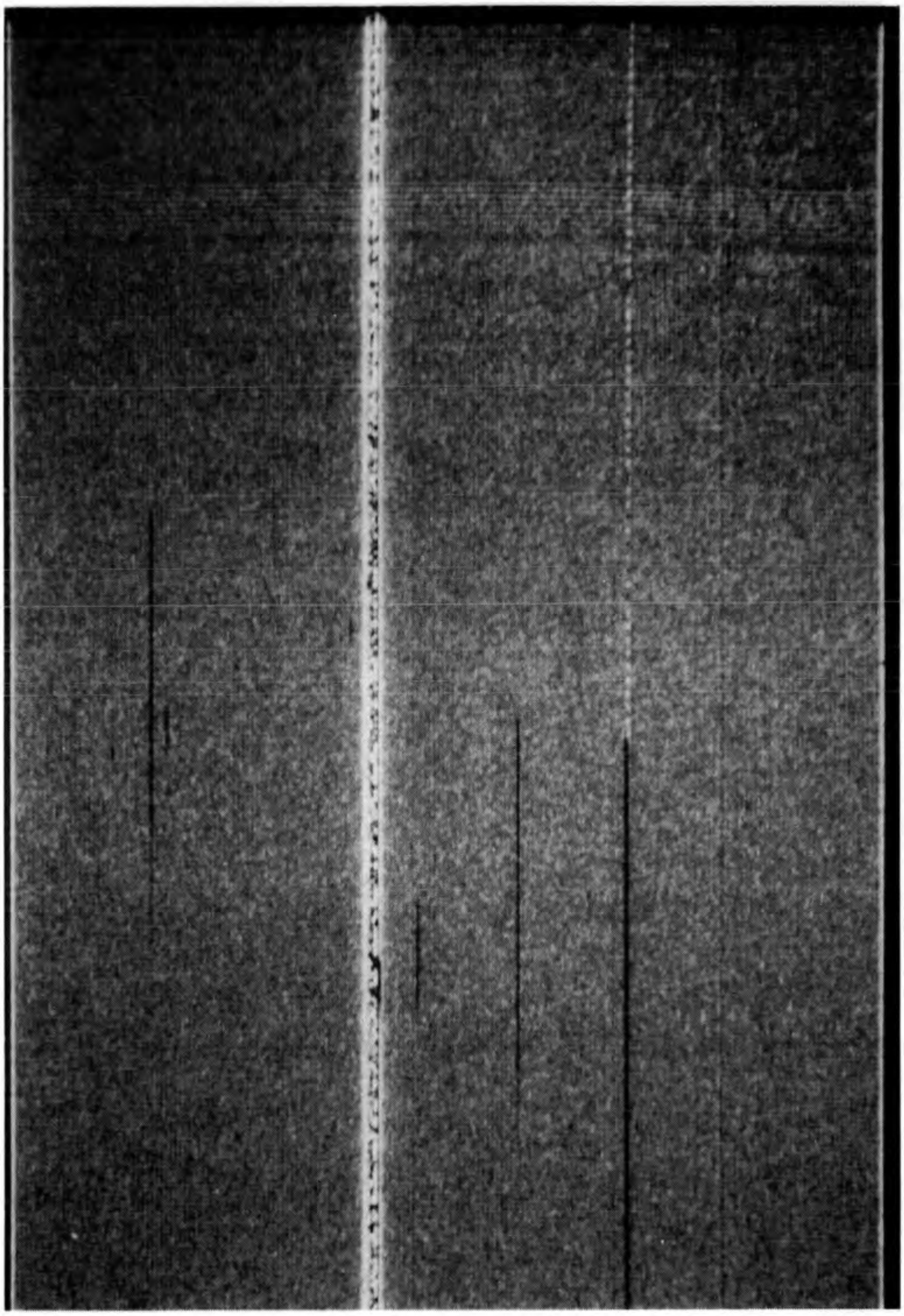


Figure 5.9

(ii) what factors affect CTE performance.

It was expected that the precise form of the CCD drive clock waveforms would have some bearing on CTE. It was also found, however, that the temperature at which the chip is operated is of some importance.

(i) drive clock waveforms

The important parameters of the drive clock waveforms are:

(i) clock amplitude

(ii) clock rise and fall times

(iii) clock phase overlap

(iv) the relative levels of the vertical (VØ) and horizontal (HØ) clocks

A useful test when attempting to optimize the drive clock waveforms is to look for asymmetry in the profiles of cosmic ray events. In doing so, however, one has to be careful not to confuse an apparently poor CTE arising from a V→H threshold with the inefficient transfer of a charge packet along a charge transfer channel.

The clocks were initially set so as to be similar in form to those recommended by GEC (EEV Technical Note No. 6, 1982). Some experimentation was then undertaken in order to establish how each of the above parameters affected, firstly, CTE performance in general, and secondly, V→H threshold level. The overall conclusions can be summarized as follows:

(i) clock amplitude

It was found that there was no advantage in making the amplitude of either the (VØ) or the (HØ) clocks any greater than 10 V as recommended by GEC. It did not, for example, help to improve poor transfer efficiency or reduce V→H threshold level. There was also discovered to be a critical amplitude of ~ 8.5 V below which the clocks would not operate satisfactorily.

(ii) clock rise and fall times

Symmetrical clocks were adopted (i.e. equal rise and fall times) with transition times of ~ 1 μs for the HØ clocks and a slightly longer time of ~ 2μs for the VØ clocks. It was discovered that the transition times were not too critical, and in particular, that times in the range 1-2 μs gave as good a transfer efficiency as could possibly be achieved. Adjusting the transition time of the VØ clocks was also found to have no effect on V→H threshold level.

(iii) clock phase overlap

GEC suggest a 50% overlap between adjacent clock phases but it was found that, in general, an overlap of 75% gave better results and that fine tuning of the overlap could give some improvement in CTE.

(iv) the relative levels of the VØ and HØ clocks

In order to be sure of preventing a spillage of charge from the output register back into the array imaging area, it was found necessary to make the lower level of the VØ clocks ~ 0.5 V more negative (i.e. more 'off') than the lower level of the HØ clocks. Adjusting the relative levels appeared to make no impact on a chip exhibiting poor CTE or on V→H threshold level.

To summarize, it was found that provided that the drive clock waveforms are basically to the form specified by GEC (EEV Technical Note No. 6, 1982), then none of the parameters is too critical. In particular, it was found that fine tuning of the clocks was unlikely to improve transfer efficiency significantly in a CCD exhibiting very poor CTE and did not reduce the quantity of charge captured by a V→H threshold.

(ii) temperature considerations

CTE was found to be a function of operating temperature in that some P8603s were seen to exhibit a marked smearing of charge when operated at temperatures below ~ 110 K. Because this was found to be worse at regions furthest from the output node, it was concluded that the problem was arising within the charge transfer channels rather than at the V→H interface. Degradation in CTE with decreasing operating temperature has been attributed to a reduction in thermal energy necessary to provide phonon assistance for electron emission from spurious potential pockets (Janesick et al., 1984).

The problem remains, of course, of what to do about the presence of a V→H threshold. One solution is to illuminate (preflash) the device prior to an exposure with an optical bias charge (fat-zero) so as to provide a background charge which fills the potential pockets when the real image is subsequently read out. A preflash of 100 electrons per pixel would leave only a few rows affected, but over the remainder of the imaging area, would add significantly to the read noise of the device due to its own shot noise (10 electrons rms). With the realization of a charge detection amplifier readout noise of 5 electrons rms, a preflash background charge in excess of 25 electrons/pixel provides the greater contribution to the total system readout noise. The precise level of the preflash is therefore of some importance. What is required is a method which enables the V→H threshold to be filled without placing a significant background charge throughout the remainder of the imaging area. The following procedure has been devised to achieve this:

Following a preflash of ~ 200 electrons/pixel, all but the last two rows of the preflash image are read out. The idea is that the two remaining rows contain sufficient charge to fill the threshold when the real image is subsequently read out. However, if the real exposure results in a zero background close to the interface such that ′zero′ charge is repeatedly transferred into the output register during the readout, then the threshold would soon empty and the problem of charge ′stealing′ would re-occur. Therefore, a second, lower level (~ 20 electrons/pixel) preflash is done prior to the real exposure which, while contributing only slightly to the readout noise, provides sufficient background charge to prevent the threshold's pockets from emptying.

A further refinement would be to read out all 578 lines of the first preflash image and to inhibit the horizontal drive clocks during the real exposure so that the charge held within the threshold's potential pockets is not cleared out.

This technique has yet to be tried with the P8603 but some early results with a Thomson-CSF CCD (with a similar V+H threshold problem) suggest that it will be successful (Thorne et al., 1986a).

5.5 Defects

The defects (or blemish artifacts) found in P8603 CCDs fall into several categories:

(i) traps

(ii) column defects

(iii) luminescence defects:
- a) blemish luminescence
- b) diffusion luminescence
- c) clocking luminescence

In the case of traps and column defects, there is nothing that can be done to overcome them and so the number of these to be expected in a typical device is of importance. The effects of luminescence defects, on the other hand, can usually be either significantly reduced or eliminated altogether by some optimization of the drive clock waveforms or the bias voltages supplied to the chip.

(i) traps

A trap is a point defect within a charge transfer channel which absorbs the first n electrons which are transferred through it, leaving behind it what appears as a 'dark streak'. It is similar in its behaviour, therefore, to that of the previously described potential pockets of a V→H threshold. Traps are most easily observed by taking a low-level (~ 100 electrons/pixel) uniform illumination exposure and inspecting the resulting image for dark streaks. The image reproduced in Figure 5.10 is an example of such an exposure. A profile through a trap, illustrating its threshold-like behaviour, is shown in Figure 5.11.

The number of rows which are affected behind a trap has been found to vary markedly from one trap to another and to decrease with increasing exposure level, i.e. the length of a dark streak shortens with increasing quantities of background charge, again symptomatic of threshold-like behaviour. Some traps have been found to affect only a few rows on a background of ~ 100 electrons/pixel whereas others have been seen to affect $\gtrsim$ 100 rows on a background of $\gtrsim$ 1000 electrons/pixel. In view of this, it is not sensible to attempt to ascribe a number to characterize the 'depth' of a typical trap, i.e. the number of electrons which it absorbs.

Given their large capacity and non-linear nature, it would not appear possible to correct for traps with subsequent data processing. All that can be done, therefore, is to note the positions of traps within a device (i.e. produce a 'defect map') and to ignore the data from those pixels read out from behind them.

The number of traps will determine the largest 'clean' area of the chip available. Again, it is difficult to give a typical number because of the large variation found from chip to chip and the problem of characterizing their severity; it has often been found to bear no relation to the cosmetic quality grading of the device purchased. One of the 'cleanest' P8603s examined (in fact the chip used to commission FOS) was found to have a total of 7 traps. The image reproduced in Figure 5.10, on the other hand, is seen to contain 16 traps while other devices have been found to possess even more.

(ii) column defects

The term 'column defect' is used here to refer to a defect which either

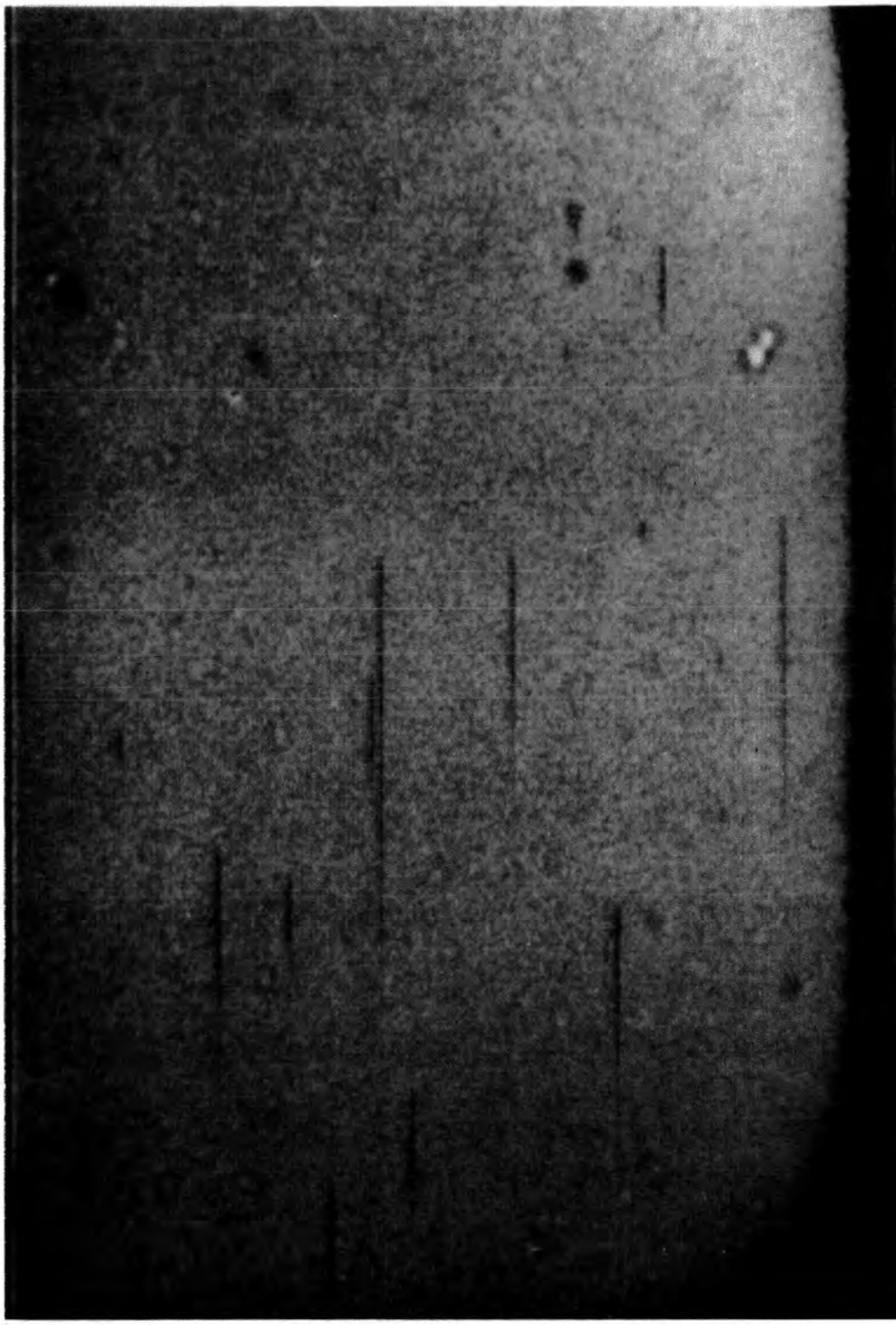


Figure 5.10

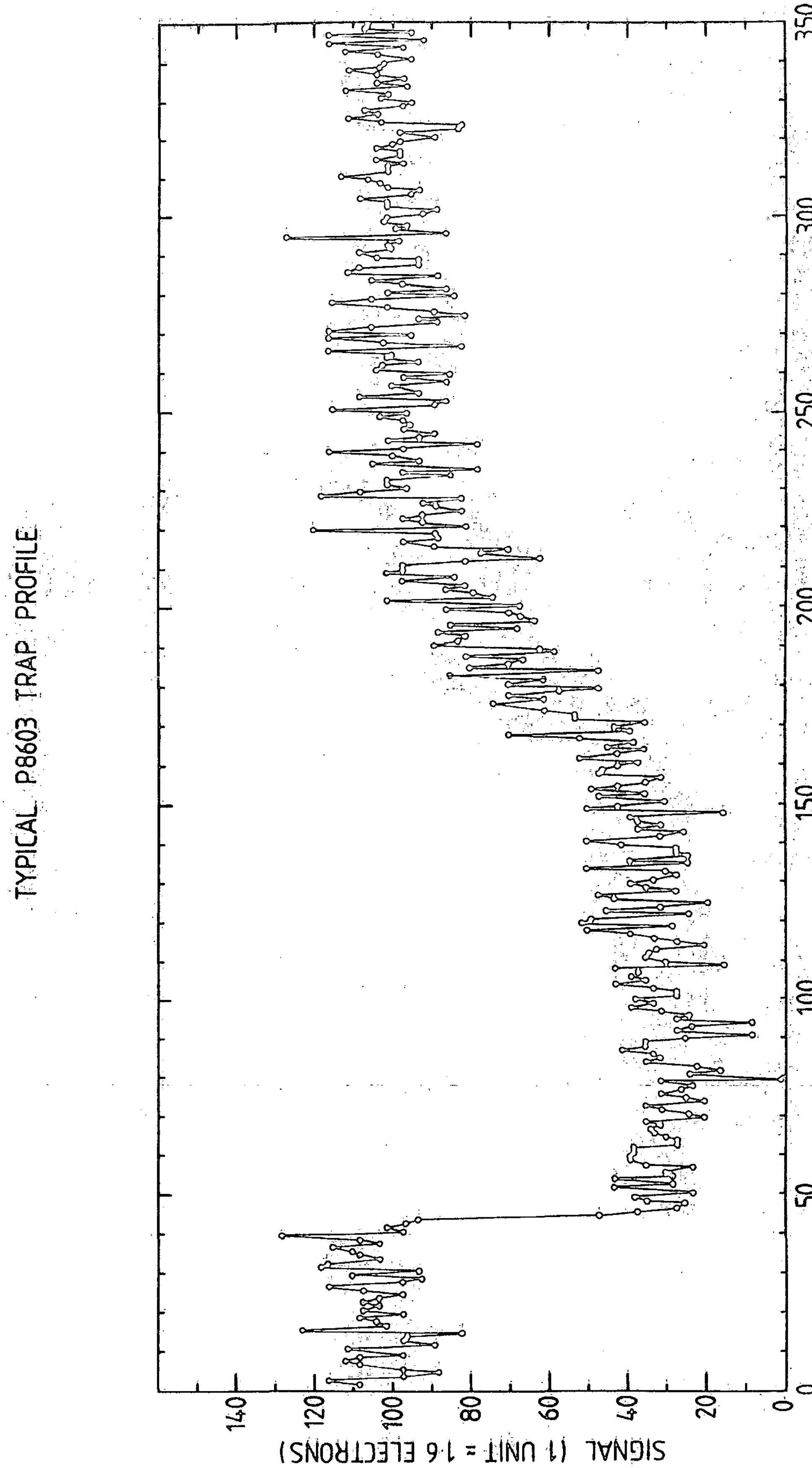

TYPICAL P8603 TRAP PROFILE
SIGNAL (1 UNIT = 1·6 ELECTRONS)
PIXELS
0
20
40
60
80
100
120
140
0
50
100
150
200
250
300
350

Figure 5.11

partially or completely renders a column within a chip's imaging area unusable but in a way that differs from that of a trap defect. Several forms of column defect have been seen in P8603 CCDs:

a) 'dead' columns

b) 'partially dead' columns and 'black-and-white pairs'

c) 'hot' columns

A dead column is one which shows no sign of having integrated any charge, no matter how much it has received from an exposure, and thus appears as a 'black' line in the resulting image. In some cases, a column may be affected along its entire length whereas in other cases, it may only be partially affected. Examples of completely dead and partially dead columns are evident within the images reproduced in Figures 5.6, 5.9 and 5.15.

Another form of the partially dead column defect which has been found to be quite common in P8603s is that of the 'black-and-white pair'. The dead column is accompanied by an adjacent column of equal length which contain an excess of spurious charge; an example can be seen in Figure 5.15. The effect is attributable to the charge from the dead column having leaked across into the adjacent column.

In contrast, a 'hot' column is one which is simply found to contain excess spurious charge and thus appears as a 'white' line within an image.

Like traps, the number of column defects likely to be found in a typical device is obviously important. In the case of column defects, however, a correlation was observed between the number of bad columns within a device and its cosmetic quality grading. Again, it is difficult to give a typical number but most devices examined to date have been found to possess at least one column defect of one sort or another.

(iii) luminescence defects

Luminescence defects have the characteristic of being light emitting which results in the creation of unwanted spurious charge. Blemish luminescence defects have been found to be quite common in P8603 CCDs whereas diffusion and clocking luminescence have only occasionally been observed.

a) blemish luminescence

A blemish luminescence defect (often referred to as a 'light emitting defect' or 'LED') originates within a single pixel and is a very strong source of light emission. In some cases, a LED can cause a large proportion of a chip's imaging area to become saturated with charge within a matter of only a few seconds. A LED is distinguished from a 'dark current spike' in that it shows no temperature dependence.

LEDs occur because of a low impedance and a resulting electrical breakdown within a pixel between either:

(i) two adjacent vertical clock electrode phases, one being held at the 'high' clocking voltage level, the other at the 'low' clocking voltage level; or,

(ii) the electrode being held at the 'high' clocking voltage level and the underlying substrate.

It was discovered that the light emission from a LED could be significantly curtailed by adopting the tri-level clocking scheme shown in Figure 5.12. While it was found necessary to have a 10 V clock amplitude to ensure proper charge transfer, it was also found that holding the VØ2 electrode (i.e. that under which charge is collected during an exposure) at a lower 'integrating level' (V_I), ~ 2 V more positive than the lower voltage level (V_L) of the vertical drive clocks, is sufficient for charge integration and stops the light emission from a LED. The light emission will re-occur, however, when the voltage applied to the VØ2 electrode is raised from the 'integrating level' to the 'clocking level' during readout. This residual effect, however, is

TRI-LEVEL VERTICAL CLOCKING TO COMBAT LIGHT EMITTING DEFECTS

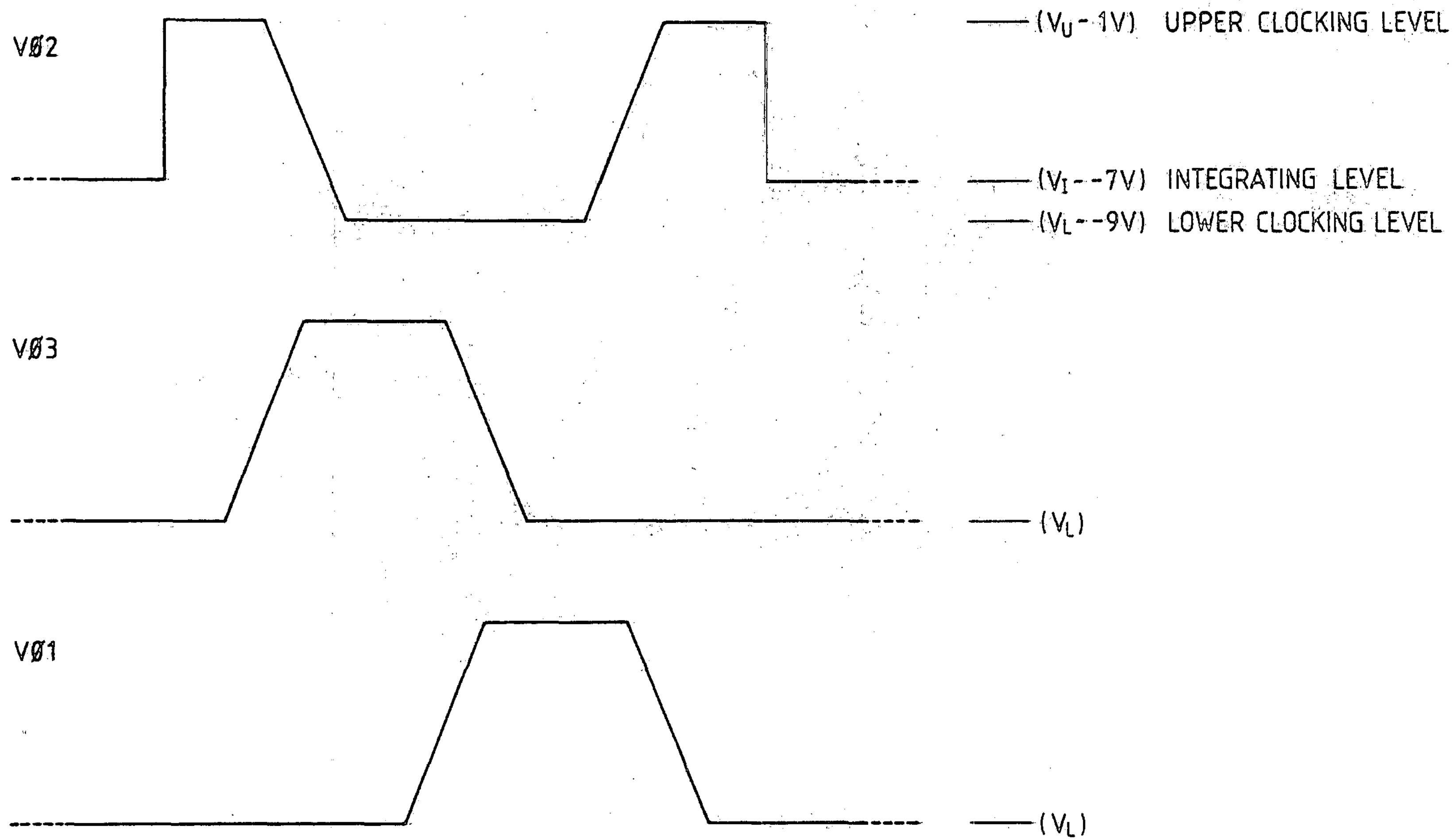


Figure 5.12

confined to the column containing the LED which then appears as a 'hot column' in the resulting image. The white line on the left-hand side of the image reproduced in Figure 5.5 is an example of a 'hot column' arising from a LED defect which has been controlled with tri-level clocking.

b) diffusion luminescence

Diffusion luminescence originates within the p-n junctions of a CCD's input/output structures. Its cause has been attributed to the differential bias voltage to a junction approaching a state of avalanche breakdown, resulting in impact ionization causing generation-recombination of e-h pairs and light emission (Janesick et al., 1984).

The effect has only been observed in one P8603 in which it was found that a small amount of charge was being continually injected into the chip's imaging area from the anti-blooming gate-drain structure at the top of the array (i.e. the end opposite to the output register) giving the appearance of a jagged edge of excess dark current charge. Lowering the voltage differential ($V_{ABD}-V_{ABG}$) from 24 V to ~ 22 V was found to stop the injection.

c) clocking luminescence

Clocking luminescence is a source of light emission which results simply from the action of clocking electrodes. It has only occasionally been observed in P8603 CCDs, occurring within the output register, and resulting in an injection of charge into the chip's imaging area. The white jagged edge seen at the top of the image reproduced in Figure 5.13 is a result of clocking luminescence. Inhibiting the horizontal drive clocks during an exposure has been found to overcome the effect.

5.6 Full Well Capacity and Dynamic Range

An important aspect of a CCD's imaging characteristics is its full well capacity, i.e. the quantity of charge which can be collected within a pixel before it saturates. Taken in conjunction with the readout noise of the device, it defines the dynamic range which can be achieved.

CLOCKING LUMINESCENCE

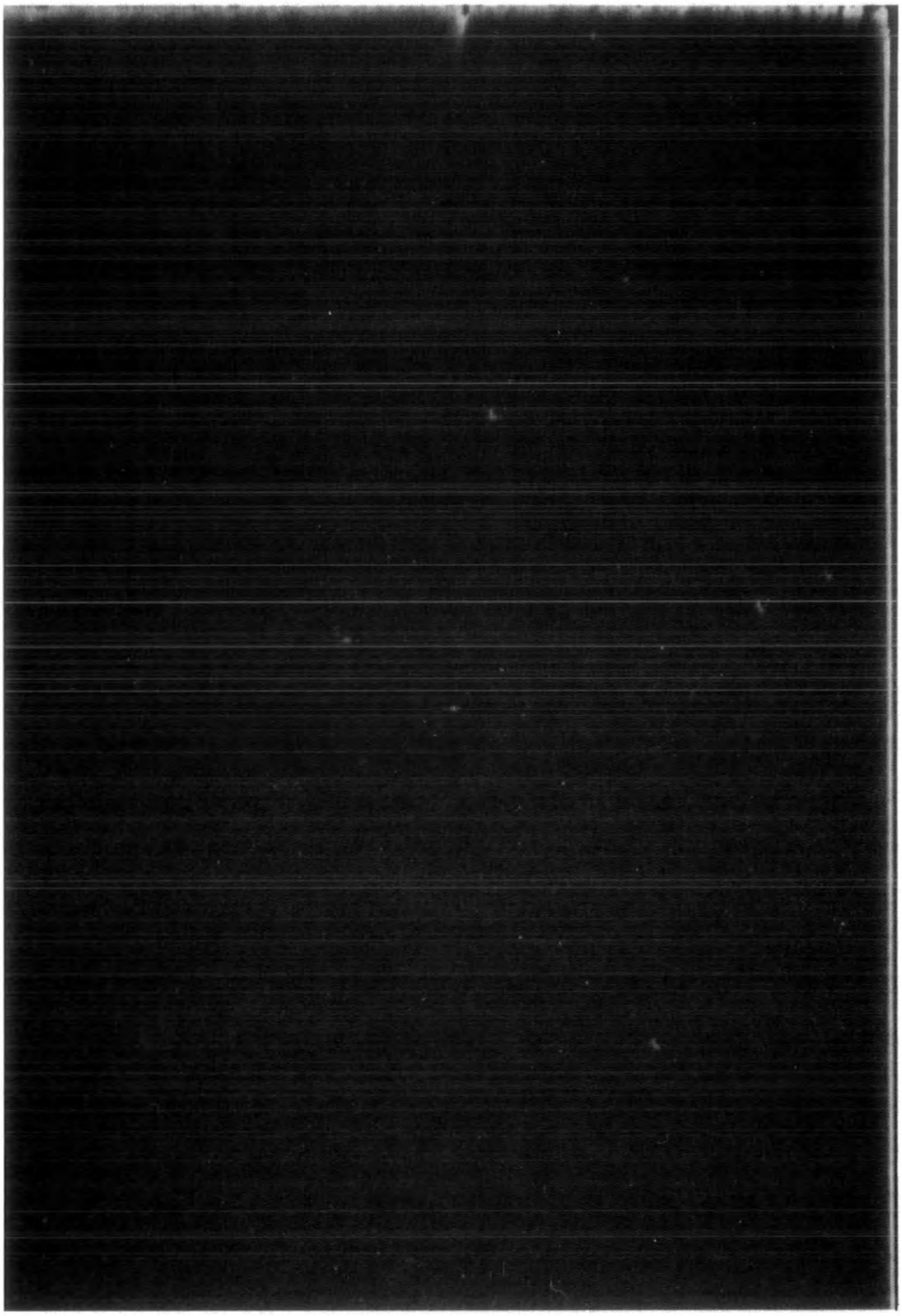


Figure 5.13

Full well capacity is defined here as that quantity of charge for which a plot of variance against signal level departs from linearity. For the P8603, this was found to be ~ 190,000 electrons (Figure 5.14) which, with a readout noise of 5 electrons rms, gives a dynamic range of ~ 38,000.

A consequence of adopting the previously described tri-level vertical clocking scheme to combat light emitting defects is that it can have a severe effect on the full well capacity of a device. The critical parameter is the voltage differential (V_I-V_L) between the integrating voltage level (V_I) of the VØ2 clock (i.e. that phase under which the potential wells are formed and charge is collected) and the lower voltage level (V_L) of the clocks (see Figure 5.12). It appears that there is a threshold value of V_I-V_L in the range 1.5-2.0 V above which the well capacity is constant but below which it decreases with decreasing V_I-V_L.

This effect was observed in the P8603 used to commission FOS which was found to possess a particularly severe light emitting defect. Setting V_I-V_L to 2.0 V was not sufficient to prevent the luminescence from creating charge in many columns even within a relatively short exposure of ~ 1 minute. It was found that a lower value of 1.5 V was necessary to confine the charge to a single column but that this also had the effect of reducing the well capacity to ~ 27,000 electrons as shown in Figure 5.14.

5.7 Uniformity of Response

Pixel to pixel and large scale variations in the responsivity of the P8603 were investigated with the aid of a uniform source of illumination and a set of broad band filters.

The pixel to pixel non-uniformity was determined by measuring the variations in signal level recorded within an array of 20 x 20 pixels with an intensity of illumination such that these dominated over shot noise. Large scale non-uniformity was measured by obtaining several 20 x 20 pixel arrays from all areas of the chip, calculating the mean signal level for each array, finding the difference between the maximum

VARIANCE AS A FUNCTION OF SIGNAL LEVEL

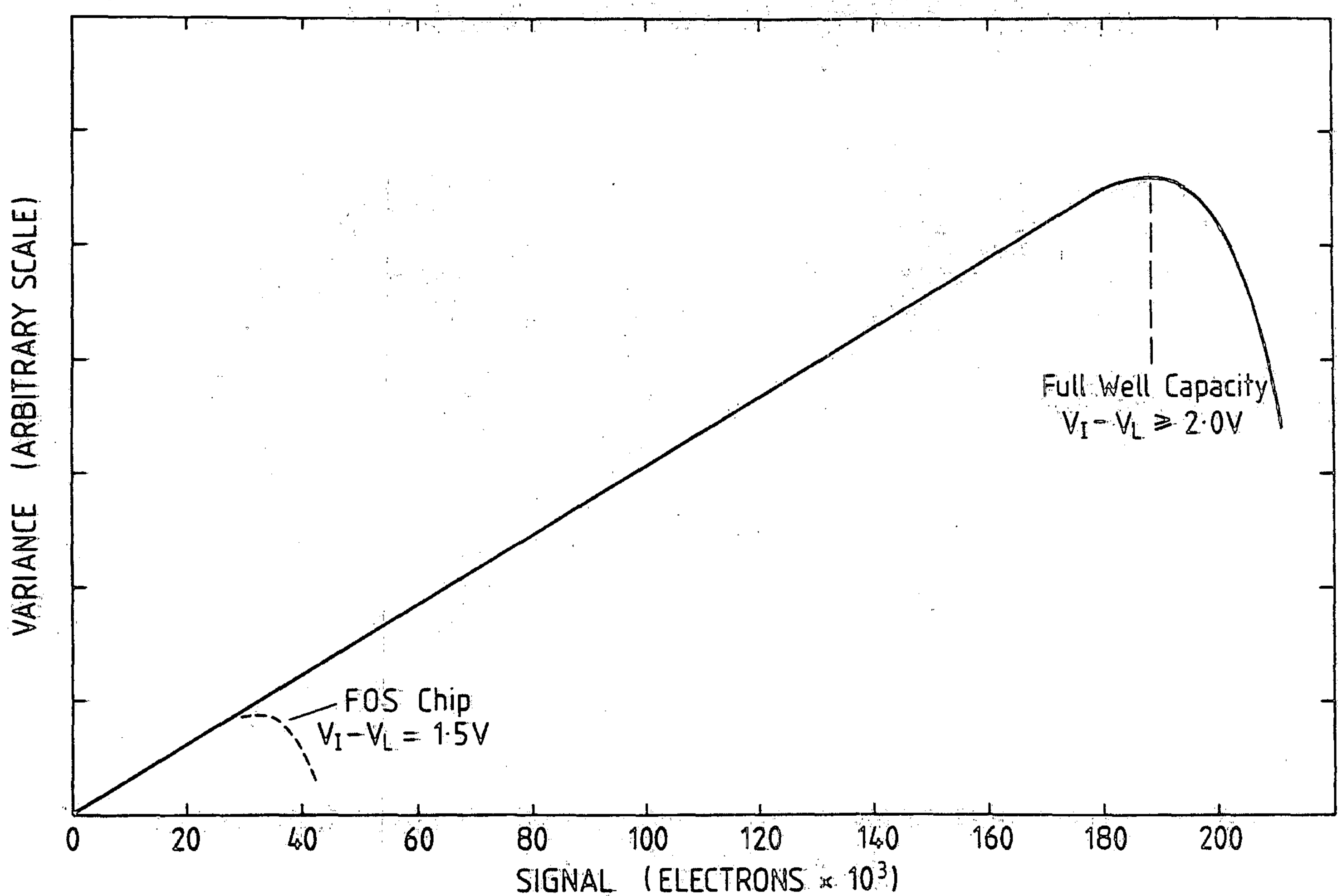


Figure 5.14

and minimum values of these means, and finally dividing by the mean signal level of the image as a whole. The results are given below:

Colour	B	V	R	I	Z
Pixel to pixel non-uniformity (%)	2.6	1.8	1.5	1.2	1.2
Large scale variations (%)	7.6	4.2	3.8	2.6	2.4

Both pixel to pixel and large scale non-uniformity was found to be greatest in the blue which can be attributed to variations in electrode thickness giving rise to variations in photon absorption. At longer wavelengths, the absorption by the electrodes is less significant and therefore the uniformity is much less dependent on the electrode structure. The remaining non-uniformity at near infrared wavelengths is presumably due to small variations in pixel size.

Interference fringes which are a characteristic of thinned chips, but have also been observed in some front-illuminated RCA CCDs (Fowler et al., 1981), were not evident in the P8603.

5.8 Dark Current and Surface-State Effects

In principle, the measurement of a CCD's dark current should be straightforward. At first, however, it proved extremely difficult to obtain consistent results. At an operating temperature of 150 K, there were found to be two circumstances under which there was a measurable, but over a period of ~ 1-2 hours, steadily decreasing rate of dark current generation:

(i) after first switching the system on.

(ii) after exposing the chip to full room light and thereby saturating it.

The effect can be attributed to charge having reached surface-state trapping sites at the $Si-SiO_2$ interface and subsequently being slowly released into the device. Buried-channel operation normally prevents the interaction of signal charge with the $Si-SiO_2$ interface, but it would appear that the above are two cases where charge is injected into the surface.

Having recognized the problem, it was possible to obtain consistent measurements of the P8603's dark current characteristic. At an operating temperature of 150 K, there was found to be no detectable dark current charge after a collection period of 30 minutes. This places an upper limit on the rate of dark current generation of ~ 0.07 electrons/pixel/minute. The noise associated with the dark current charge will therefore be insignificant compared to the readout noise for collection periods of at least 2 hours. The first evidence of a non-zero dark current, seen in the form of dark current 'spikes' (i.e. individual pixels with a notably higher rate of dark current generation, sometimes referred to a 'hot pixels') was observed at operating temperatures in the range 160-170 K.

In summary, the dark current charge generated within the P8603 at operating temperatures below 160 K can be neglected over collection periods of ~ 2 hours.

The problem of charge being slowly released into a chip from the $Si-SiO_2$ interface as a result of over illumination warrants further discussion because it reveals the possibility that if pixels become saturated with charge during an exposure, a residual image may develop some time after the real image has been read out. To investigate this further, a small source of bright illumination was projected onto a CCD. Following an exposure of sufficient duration to ensure that those pixels imaging the source would saturate, the CCD was read out and then immediately read out a second time. No residual charge was observed in the second image but a small quantity (~ 30 electrons/pixel) was detected when the CCD was read out a third time, approximately 15 minutes after the second readout. It would appear that a signal of ~ 5×10^5 electrons/pixel is required to produce the effect but further work is necessary to quantify this more reliably. The implication, however, is that over illumination, possibly from a calibration arc source or a strong emission line feature, could affect the subsequent exposure.

5.9 Cosmic Ray Events

In the absence of a significant rate of dark current generation, cosmic ray events are likely to be the limiting factor in determining the longest exposure which can be made with a CCD. Since there is nothing that can be done about cosmic rays, the rate at which events are detected and their size (i.e. the number of pixels over which the charge is spread) needs to be known.

The event rate for the P8603 was measured at 0.039 events/cm^2/second which is consistent with the expected rate as calculated by Leach and Gursky (1979). In the absence of charge smearing resulting from poor charge transfer efficiency and/or the effects of a V+H threshold, typical events were found to occupy ~ 2-4 pixels. Tracks with charge deposited in many more pixels, a result of particles incident obliquely upon a chip, have also been occasionally observed (Figure 5.15).

Using the figure for the measured event rate, it is a fairly simply matter to estimate the duration of an exposure undertaken with FOS for which it could be expected that one cosmic ray will have passed through that portion of the chip imaging the spectrum. For the simple case of a first order spectrum only, with the object signal spread laterally over 3 pixels, this works out to be ~ 1500 seconds (assuming each event to affect 2 pixels).

It is obviously important that no additional events are introduced by any local radioactivity within the materials of the cryostat. One particular copper block used inside the cryostat was found to have just this effect, making the event rate apparently four times higher than usual. Some care is therefore necessary to ensure that this problem is avoided when developing new instrumentation.

5.10 Conclusions

The characteristics of the P8603 CCD are summarized in Table 5.1 It is important to consider their implications with regard to the use of a P8603 CCD in FOS. Here, and in spectroscopic applications in general, low signal levels are to be expected and so the important aspects of a CCD's performance are:

COSMIC RAY EVENTS

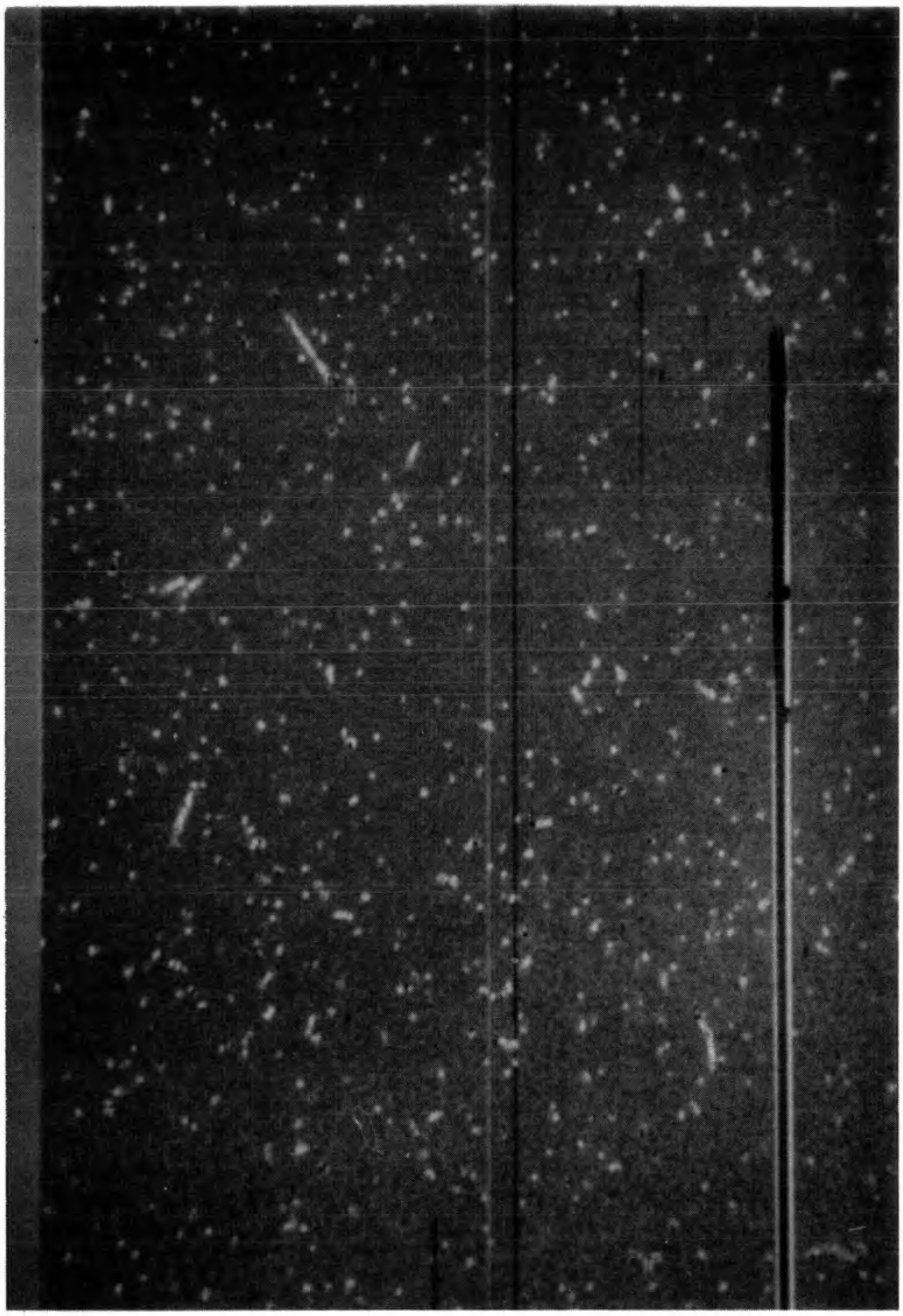


Figure 5.15

(i) readout noise.

(ii) charge transfer efficiency.

(iii) low signal level non-linearity arising from the effects of a threshold.

(iv) cosmetic quality. This is particularly important in applications such as FOS where the optical design dictates that the image is projected onto a specific area of the chip.

The typical performance of P8603 CCDs with regard to each of these aspects can be summarized as follows:

(i) a readout noise of 5-10 electrons rms was achieved in almost all cases, which is at least as low as that of any other currently available CCD. In this respect, therefore, the P8603 is well suited to the application.

(ii) charge transfer efficiency was found to be good.

(iii) some chips were found to have a threshold which can give rise to an apparently poor low signal level charge transfer efficiency.

(iv) cosmetic quality was found to vary from chip to chip, often bearing no relation to the commercial grading of the device.

The selection of a chip should therefore ideally be based on the following criteria; these being the only ones showing a significant chip to chip variation:

(i) ideally, the chip should have no threshold. The use of a preflash background charge prior to an exposure can overcome the problems associated with a threshold, but this will inevitably result in some increase in the effective readout noise due to its own shot noise. Furthermore, it is important that the preflash illumination is uniform across the chip and repeatable for the purposes of calibration, which may present some practical problems. Further work on the new preflash technique described earlier may provide a partial solution to the problem.

(ii) it should be of acceptable cosmetic quality.

However, at the time that a CCD had to be installed in FOS for commissioning, only two chips were available to choose from, and much of the work with regard to threshold effects had yet to be done. Of these:

(i) the first chip was very obviously unsuitable because of its poor cosmetic quality.

(ii) the second chip, on the other hand, was found to be remarkably free of defects within the centre of its imaging area, and was therefore chosen.

The selected chip was known to exhibit some smearing of cosmic ray events in the vertical direction (i.e. in the direction of dispersion) which was later attributed to a threshold problem. However, its implications were only fully appreciated after the first few commissioning runs when FOS was first used to observe very faint objects, and so it is more appropriate that these results should be discussed with regard to its performance with real astronomical data.

Table 5.1 P8603 CCD CHARACTERISTICS

Quantum efficiency	
peak	42-46% at 740 nm
10% points	460 nm, 930 nm
1% points	390 nm, 1020 nm
readout noise	5-10 electrons rms
charge transfer efficiency	good in the absence of a V→H threshold
V→H threshold	~ 300 electrons
Traps	$\gtrsim$ 7
Column defects	$\gtrsim$ 1
Full well capacity	~ 190,000 electrons
Dynamic range (pixel)	~ 38,000 (σ = 5 e rms)
Uniformity of response (blue - infrared)	
pixel-pixel (%)	2.6-1.2
large scale (%)	7.6-2.4
interference fringes	none
Dark current (at 150 K)	$\lesssim$ 0.07 e/pixel/min.
Cosmic ray event rate	~ 0.039 events/cm^2/sec.

CHAPTER 6

AUTOMATION OF FOS CCD FOCUS ADJUSTMENT

6.1 Introduction

FOS has been designed with a novel facility to allow remote focus adjustment of its CCD detector with the spectrograph mounted in position on the telescope and operational.

The objective was to ease the optical alignment of the instrument by incorporating automated drive mechanisms which would permit the position of the CCD within the camera to be adjustable with the CCD cooled and running. The operation of these drive mechanisms with simple commands from the telescope's instrumentation control computer further simplifies the alignment procedure by allowing focussing to be carried out from the observer's control console. Hartmann shutters were also incorporated to enable the focus to be assessed by taking CCD exposures of a comparison arc lamp and examining the Hartmann shift of spectral lines.

This chapter is concerned with a technical description of the automated mechanisms, the development of their drive electronics and control from a microprocessor.

6.2 Microprocessor Control of Telescope Instrumentation

The recent trend towards the automation of telescope instrumentation has greatly increased the efficiency and ease with which astronomical data may be obtained. An important development in this field has been the application of microprocessors to instrument control (van Breda and Parker, 1983). Figure 6.1 illustrates how this concept has been realized at the LPO.

Where appropriate, an instrument's mechanisms are automated with electromechanical actuators and transducers. The 'low-level' control and monitoring for these mechanisms is provided by a microprocessor mounted either within or alongside the instrument on the telescope. An RS232C asynchronous serial link is used for carrying 'high-level'

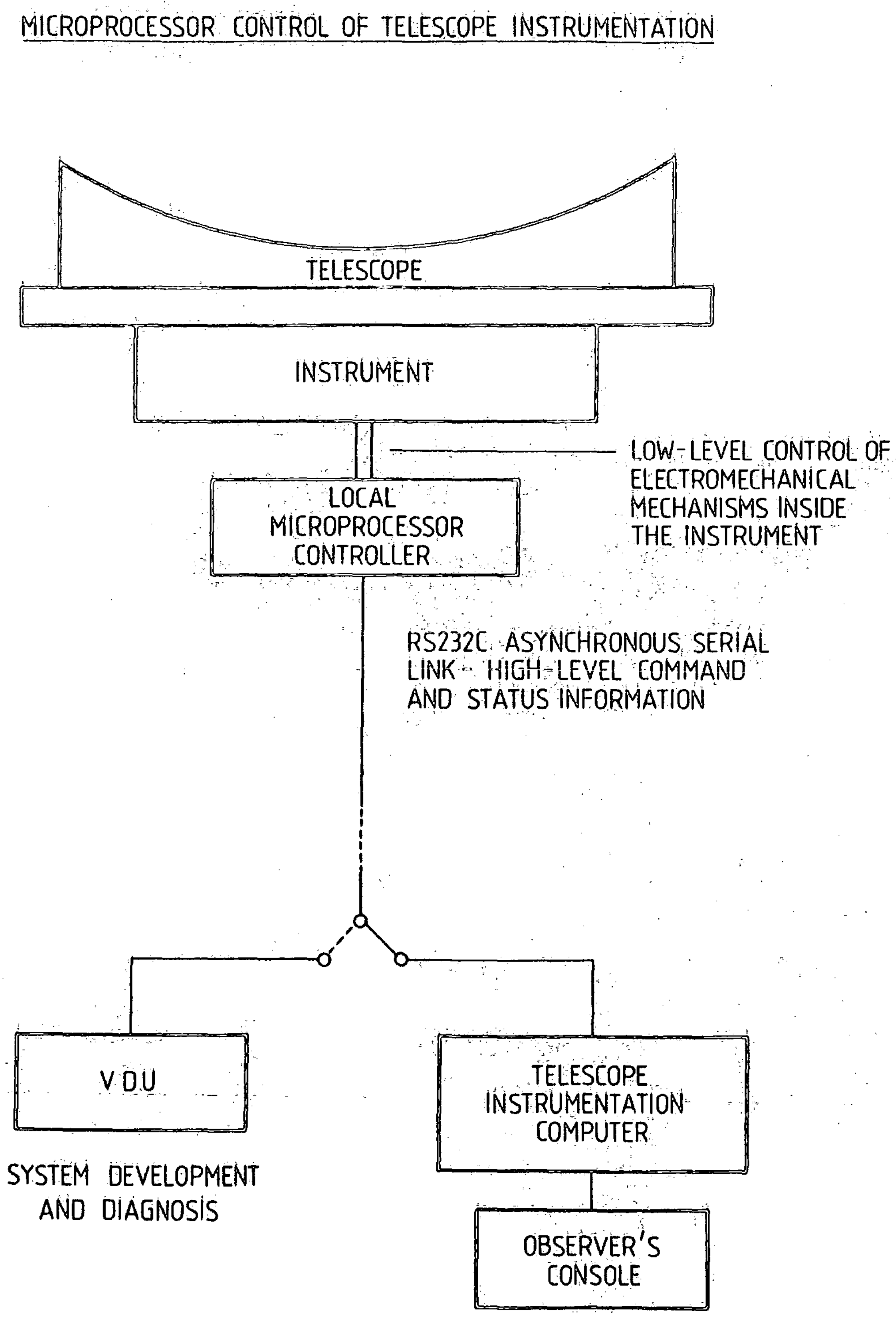

MICROPROCESSOR CONTROL OF TELESCOPE INSTRUMENTATION
TELESCOPE
INSTRUMENT
LOW-LEVEL CONTROL OF ELECTROMECHANICAL MECHANISMS INSIDE THE INSTRUMENT
LOCAL MICROPROCESSOR CONTROLLER
RS232C ASYNCHRONOUS SERIAL LINK - HIGH-LEVEL COMMAND AND STATUS INFORMATION
V.D.U
SYSTEM DEVELOPMENT AND DIAGNOSIS
TELESCOPE INSTRUMENTATION COMPUTER
OBSERVER'S CONSOLE

Figure 6.1

command and status information between the microprocessor and the outside world. This will normally be connected to the telescope's instrumentation control computer thereby permitting operation from the observer's console. However, an RS232C interface also allows the microprocessor to be operated in a stand-alone mode from a VDU for instrument development and diagnostic purposes.

The distributed intelligence gained from the employment of microprocessors relieves the demand for low-level control from the instrumentation computer. In turn, this allows more efficient use of the computer in running more complicated tasks such as high-speed data acquisition from detectors, data display and reduction, and providing a 'user-friendly' interface between the instrumentation and the astronomer. In this way, the role of the computer may be orientated more towards the scientific requirements of the observer.

6.3 Microprocessor Electronics Hardware and Software

A brief introduction to the microprocessor electronics hardware and software used in this project is given in following sections as a foreword to a detailed description of the spectrograph's automated mechanisms and the design of their control electronics.

6.3.1 Modular Microprocessor System (MMS)

The MMS is an RGO-designed microprocessor system for the control of instrumentation on the INT (Fisher, 1980). Its function is to provide standard microprocessing hardware in a modular form from which applications with quite different requirements can be assembled. The aim is to reduce the problems of providing a general support and repair service at a remote site, allowing the replacement of cards to be used as an initial approach to fault diagnosis.

The MMS is designed around the Motorola 6800 microprocessor and its family of peripheral interface and support devices. Eurocard standards are used throughout the system with connections through a purpose-designed microprocessor bus backplane. A basic system consists of a processor, memory and an interface for RS232C serial communication. Additional cards for driving stepper motors or for reading encoders may then be added as required.

6.3.2 <u>MMS FORTH Software</u>

The MMS runs FORTH software, chosen for its combination of high execution speed, efficiency and powerful interactive command structure.

FORTH was invented in the late 1960s for use with a radio telescope at the Kitt Peak National Observatory (Moore, 1974). Since then, it has been adopted at many observatories for a variety of applications ranging from telescope control to data acquisition and analysis.

A good introductory text to the FORTH language has been written by Brodie (1981). Some of its more important concepts and the implementation of FORTH on the MMS are described briefly.

(i) the dictionary

FORTH is an interactive language that uses a linked ´dictionary´ for interpreting words input from a terminal. Each word (or definition) in the dictionary defines a procedure for the execution of previously entered words lower in the dictionary.

A FORTH system contains a basic dictionary that includes definitions used by most applications. Programming consists of adding further definitions to the dictionary to form an ´application vocabulary´. Definitions may be entered either through the terminal or, more usually, loaded from a disc. Logical jumps and loops, both definite and indefinite can all be implemented within dictionary definitions.

Good FORTH programmes are constructed from definitions containing only a few logical structures. Because all definitions remain accessible to the user, each part of a programme may be checked individually in a simple interactive way. This is of great assistance in programme debugging and makes FORTH ideally suited to the development of instrument control systems at an engineering level.

(ii) the parameter stack

A parameter stack is usually used for the communication of data between sections of programme. Numbers input from the terminal are also stored temporarily on the stack from where they can be recovered later by a definition. The use of a stack gives rise to reverse polish notation where arguments precede their operators.

(iii) Promforth

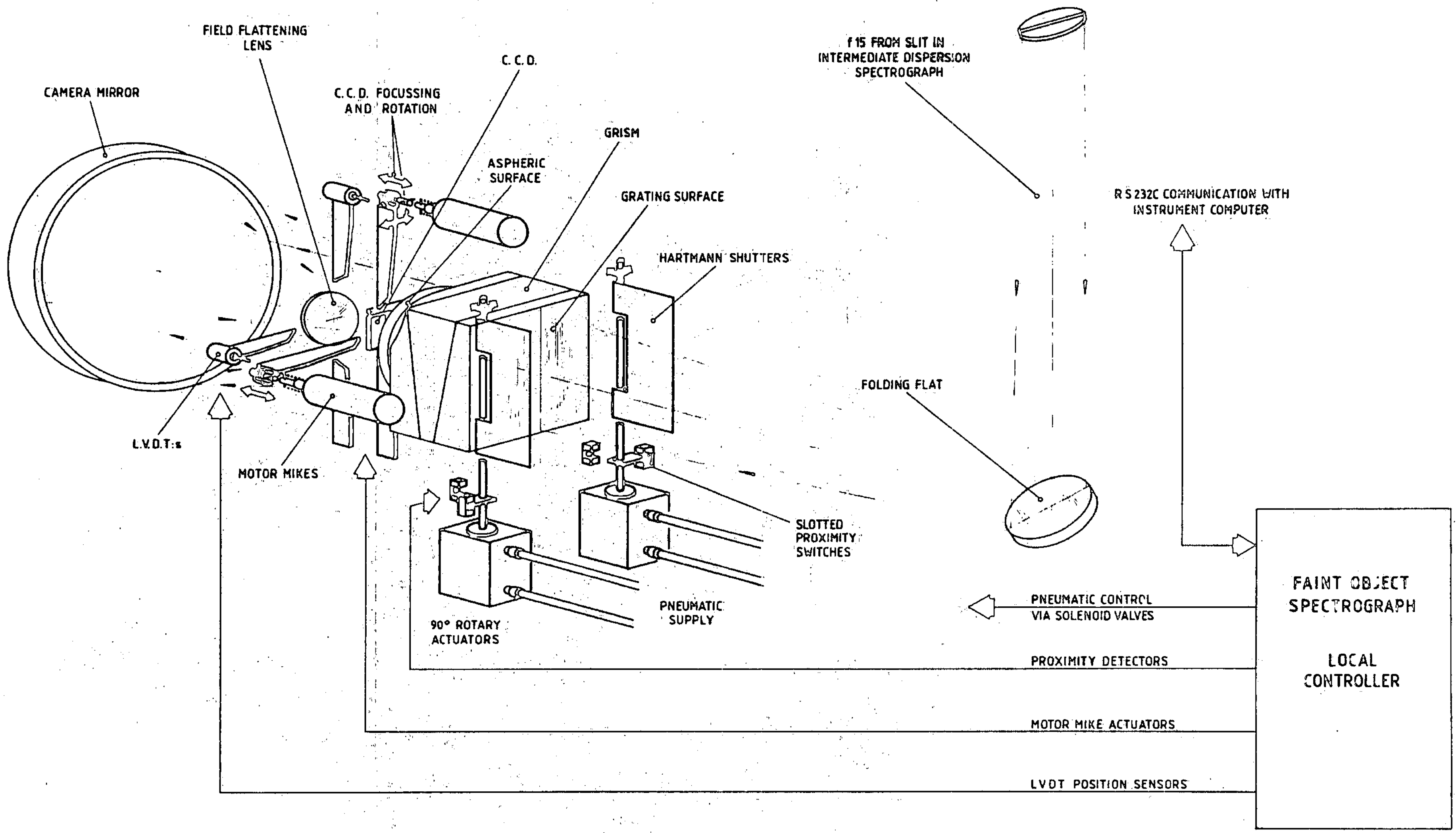
The FORTH software implemented on the MMS is called Promforth (Parker, 1981). It contains all the standard features of FORTH but has been designed to run from a dictionary stored in read-only memory. The software is configured so that on power-up, the microprocessor jumps to the head of the application dictionary and commences programme execution. This enables the development of a self-contained instrument control system which will run from switch-on and which requires no additional programming by the user.

6.4 Automation of FOS CCD Focus Adjustment

Figure 6.2 is a schematic showing the optical assembly of FOS, the actuators and encoders of its automated mechanisms, and their connection to a local microprocessor controller. The automated mechanisms are treated as belonging to two independent subassemblies: the spectrograph camera and the Hartmann shutters.

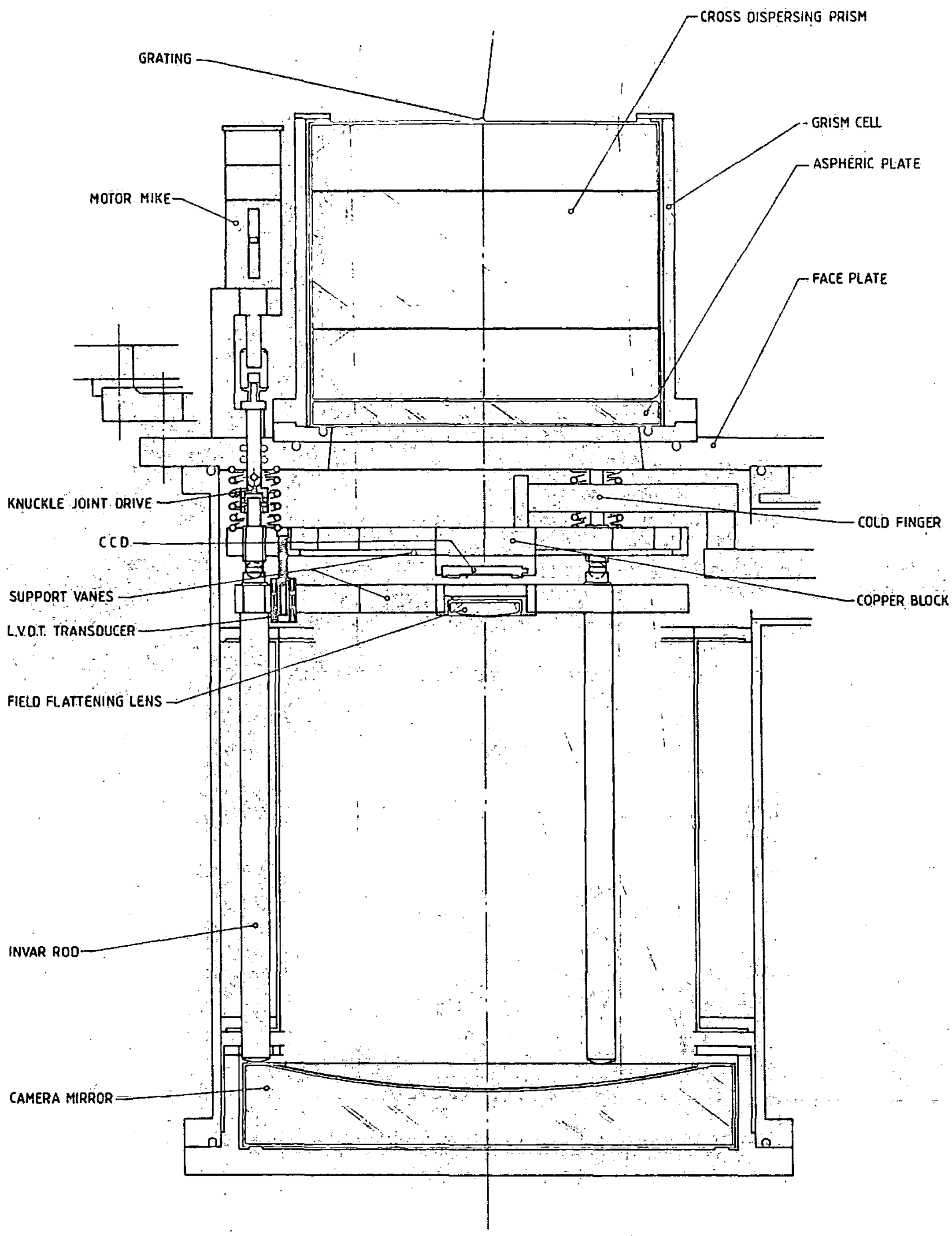
6.5 Spectrograph Camera Assembly

The spectrograph camera assembly houses the optical components, the CCD and the focus adjustment drive mechanisms. A cross-section through the camera enclosure is illustrated in Figure 6.3 and a photograph showing an external view of the assembly is reproduced in Figure 6.4.



2.5m FAINT OBJECT SPECTROGRAPH INSTRUMENT CONTROL

Figure 6.2



SPECTROGRAPH CAMERA ASSEMBLY

Figure 6.3

SPECTROGRAPH CAMERA

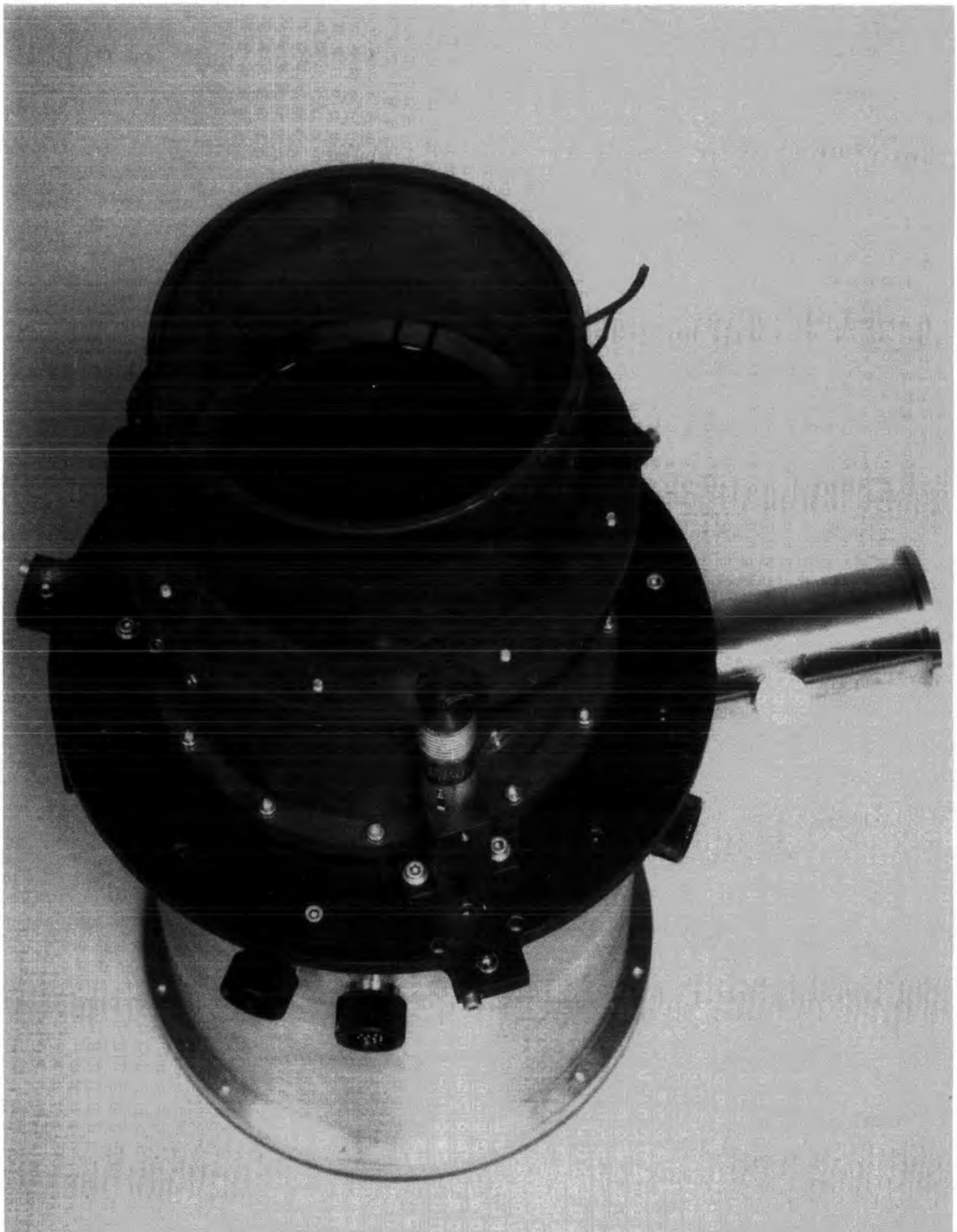


Figure 6.4

The camera faceplate supports the grism cell containing the cemented assembly of grating, cross-dispersing prism and aspheric corrector plate. The camera mirror is mounted at the opposite end of the enclosure. Its flat annular edge is used as a reference surface for locating the field-flattening lens in a position specified by the optical design.

A fibreglass vane structure supports the field-flattening lens in the centre of the beam (Figure 6.5). The vanes are clamped to an annular ring, referenced from the camera mirror by three invar rods. A second annular ring and fibreglass vane structure supports a copper block and the CCD behind the field-flattening lens. The CCD is clamped to the front face of this block to ensure a good thermal contact.

In operation, the CCD is cooled by conduction through a cold finger emanating from the copper block. This is connected via a flexible copper braid and a copper rod to the liquid nitrogen cryostat appended to the camera enclosure. The block is regulated to a temperature of 150 K by an external servo amplifier of the type described in Chapter 3.

A small printed circuit board mounted beneath the CCD provides electrical connections from the drive electronics.

With a camera focal ratio of f/1.4, a precise optical alignment of the CCD is essential. The focus is adjustable by axial and tilt displacement of the CCD with respect to the field-flattening lens. This is achieved by means of three independent micrometer screws spaced equally around the CCD support ring at positions above the invar rods. A bearing is located in the base of each of the male micrometer screws and the set of three bearings are registered in a kinematic seating arrangement at the ends of the invar rods. The matching female micrometer threads are fixed inside the CCD support ring, enabling the CCD to be displaced by rotating the screws.

6.5.1 Motorized Focus Adjustment

The camera's focus adjustment mechanisms are motorized to enable their remote operation. Oriel Motor Mike actuators were chosen for

CCD AND FIELD-FLATTENING LENS SUPPORT

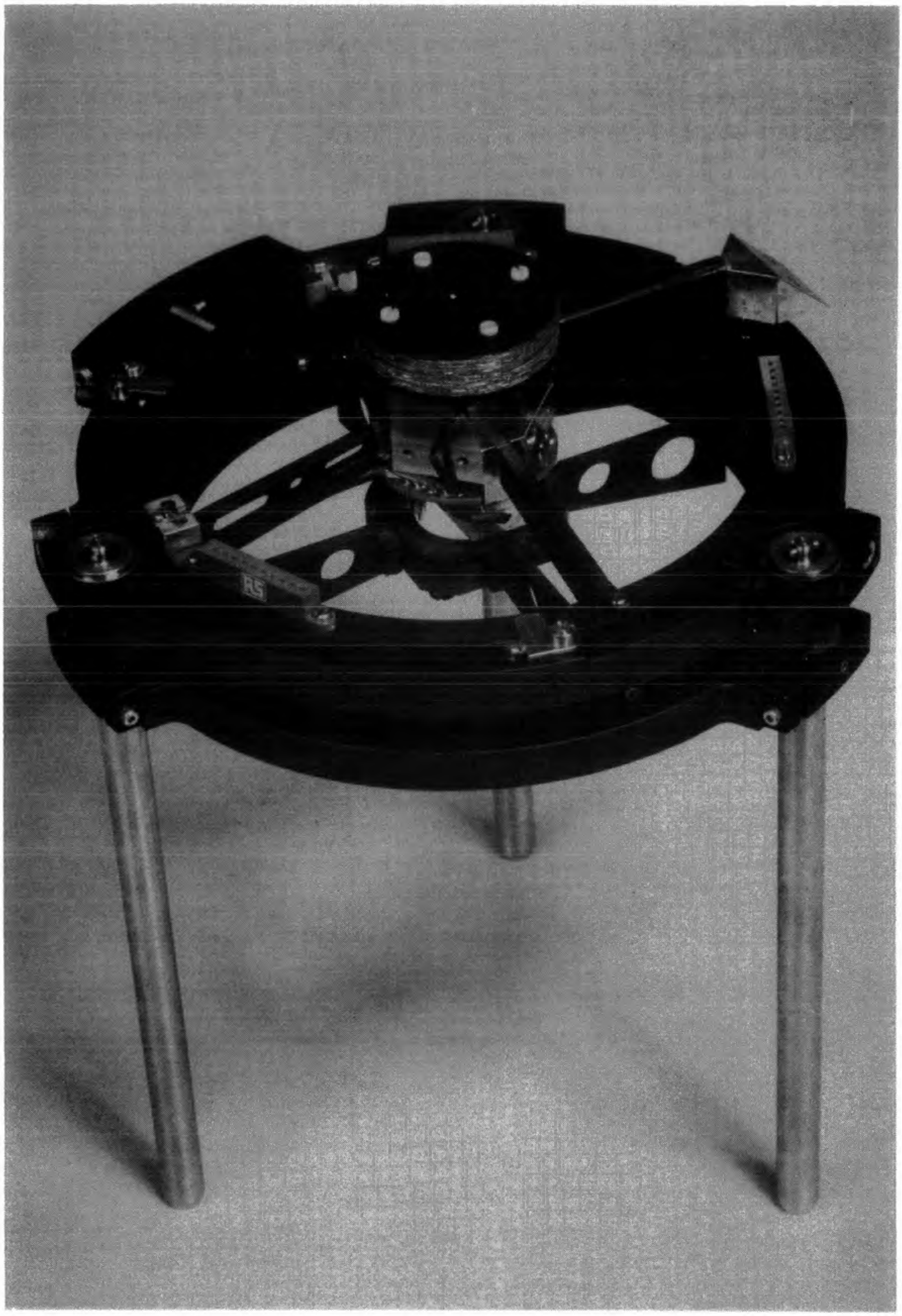


Figure 6.5

this application because of their design for precision positioning coupled with the small physical size of their packaging. The employment of stepper motors was excluded by the limitations of the space envelope surrounding the camera faceplate and grism cell (Figure 6.4).

The Oriel Motor Mike combines a miniature DC motor with integral 485:1 reduction gearing to rotate a fine-pitch micrometer screw in a precision threaded nut. The components are housed in a package similar in size to a conventional manual micrometer.

High resolution positioning is achieved by stepping the motor with drive pulses of 12 V DC amplitude. Speed is dependent on drive pulse width and duty cycle. Drive pulse polarity must be reversed to change the direction of travel.

The Motor Mikes are mounted outside the camera enclosure off the faceplate, and in this application, they are used as precision shaft rotators. Each is coupled to its corresponding focus adjustment micrometer by a linkage consisting of a shaft passing through the faceplate, a double knuckle joint and splines. O-ring seals located within the faceplate ensure that the vacuum inside the enclosure is maintained. A photograph showing the complete assembly of Motor Mikes, linkages and focus adjustment mechanisms is reproduced in Figure 6.6.

6.5.2 Evaluation of Motor Mike Performance

The design objectives for focus adjustment called for:

(i) axial displacement of the CCD over a 2 mm range.

(ii) positioning to a resolution of 5 μm.

The manufacturer's specifications of the Motor Mike suggested its performance to be more than adequate for this application, claiming unidirectional positioning to 0.01 μm resolution. Initially it was proposed that the focus position could be inferred from a count

MOTOR MIKE FOCUS ADJUSTMENT MECHANISMS

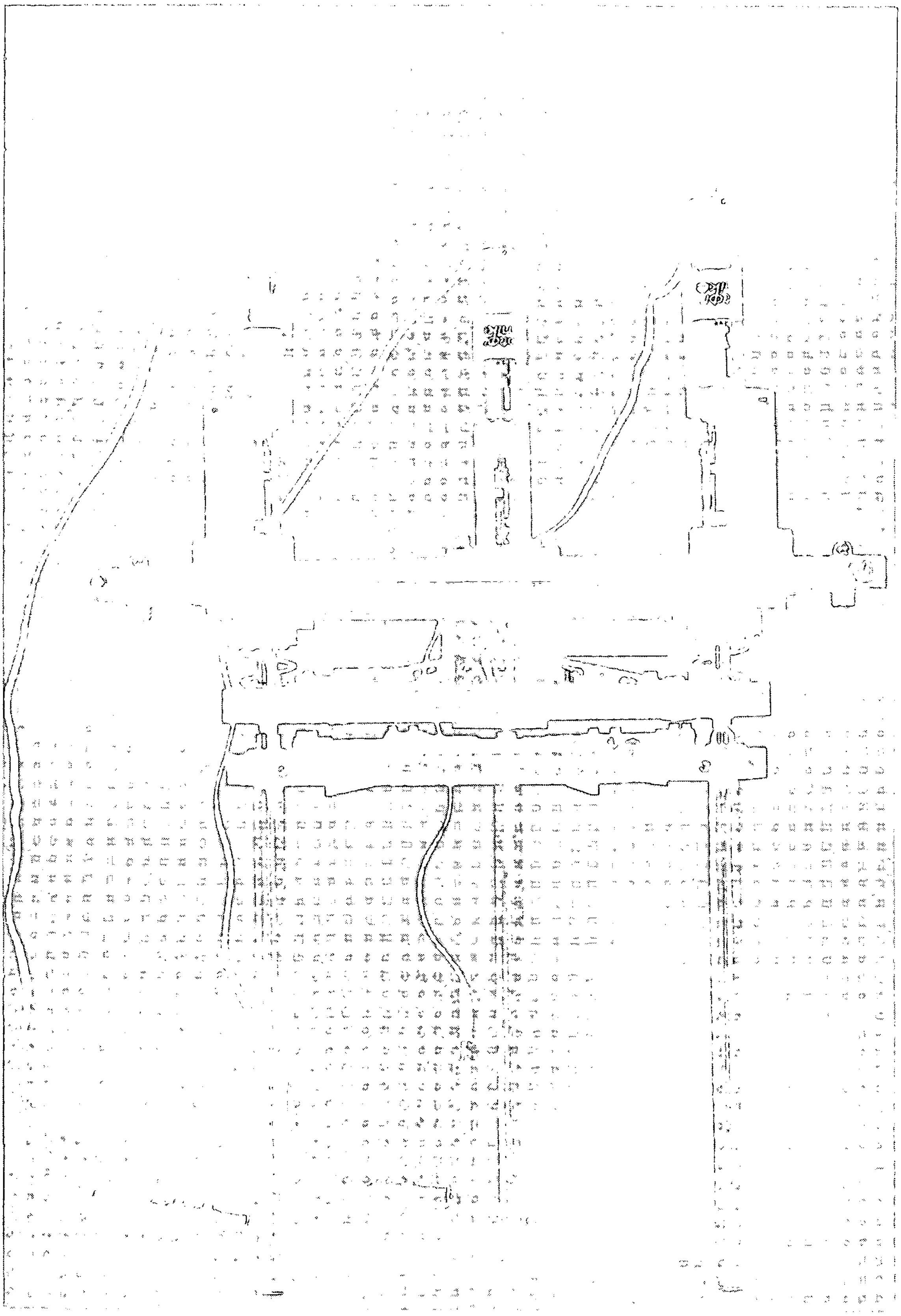


Figure 6.6

of drive pulses applied to the motor, obviating the necessity for additional position encoding. However, some doubt was expressed concerning the repeatability of positioning in the presence of a varying drive load and, in particular, backlash encountered both in the Motor Mikes and the linkage couplings to the focus adjustment micrometers. An extensive investigation of the Motor Mike's performance was therefore undertaken, the aim being to observe the variation in incremental displacement with drive pulse width and axial load, and also the severity of backlash and the repeatability of positioning.

Figure 6.7 shows selected examples of unidirectional drive characteristics obtained with a dial gauge attached to a Motor Mike spindle to measure displacement. A pulse generator working in the 'one-shot' mode was used to drive the Motor.

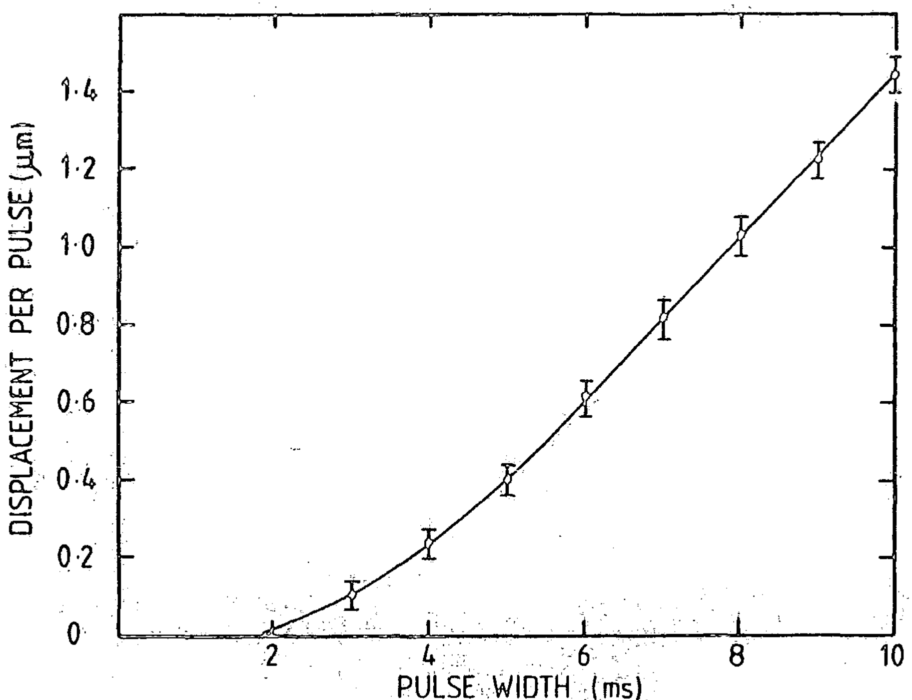
The conclusions drawn from this work were:

- a Motor Mike is capable of positioning to a resolution better than 1 μm.
- driving a 2 Kg load, the incremental displacement is proportional to drive pulse width for pulses of width greater than 4 ms.
- for a given pulse width (10 ms @ 12 V amplitude), the incremental displacement decreases non-linearly with increasing axial load.
- the backlash encountered in reversing the direction of Motor Mike travel is of order of 6 μm and load dependent. An attempt to calibrate it in terms of a fixed number of drive pulses proved unsuccessful.

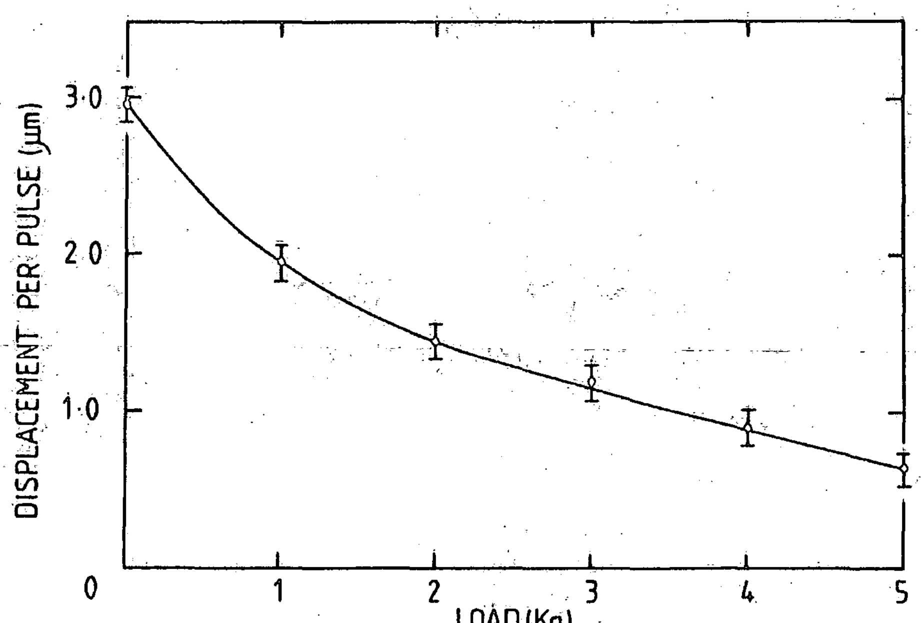
Therefore, although small incremental displacements can be achieved, the load dependence and the effects of backlash render repeatable positioning impossible without additional encoding, especially in consideration of the complex loading presented by the focus adjustment micrometers and their linkages. The overall conclusions were:

- position encoders should be incorporated within the focus adjustment mechanisms.

MOTOR MIKE DRIVE CHARACTERISTICS



LINEAR DISPLACEMENT AGAINST PULSE WIDTH
FOR A MOTOR MIKE DRIVING A 2 Kg LOAD



LINEAR DISPLACEMENT AGAINST LOAD
FOR 10 ms DRIVING PULSES

Figure 6.7

- the design of electronics to drive the Motor Mike from the local microprocessor controller should permit complete software control of drive pulse generation, thereby allowing the implementation of a 'closed-loop' control system for focus adjustment.

6.5.3 Motor Mike Drive Electronics

The design of the electronics to drive the Motor Mikes was largely dictated by the requirements for:

- microprocessor software control of drive pulse width.
- software control of drive pulse polarity to enable bidirectional travel.
- independent control for each Motor Mike.
- compatibility with the MMS standard.

A schematic of a single Motor Mike drive channel is shown in Figure 6.8. Analogue switches are used to generate the drive pulses and define their polarity.

- Switches SW3 and SW4 enable the selection of either a positive or a negative 12 V DC drive voltage depending on the logical state of DRIVE DIRECTION CONTROL.
- Switches SW1 and SW2 enable the selection of either the ±12 V drive voltage or ground depending on the logical state of DRIVE PULSE CONTROL.

Table 6.1 summarizes the control required to generate a drive pulse.

The drive voltage signal output from SW1 and SW2 is passed to a unity voltage gain, high current amplification booster (MC1438R). This device incorporates an adjustable current limit to ±300 mA and is well suited to driving the reactive load presented by a Motor Mike.

An MMS compatible Eurocard was designed to enable three Motor Mike drive channels to be independently controlled from a Motorola 6821

MOTOR MIKE DRIVER

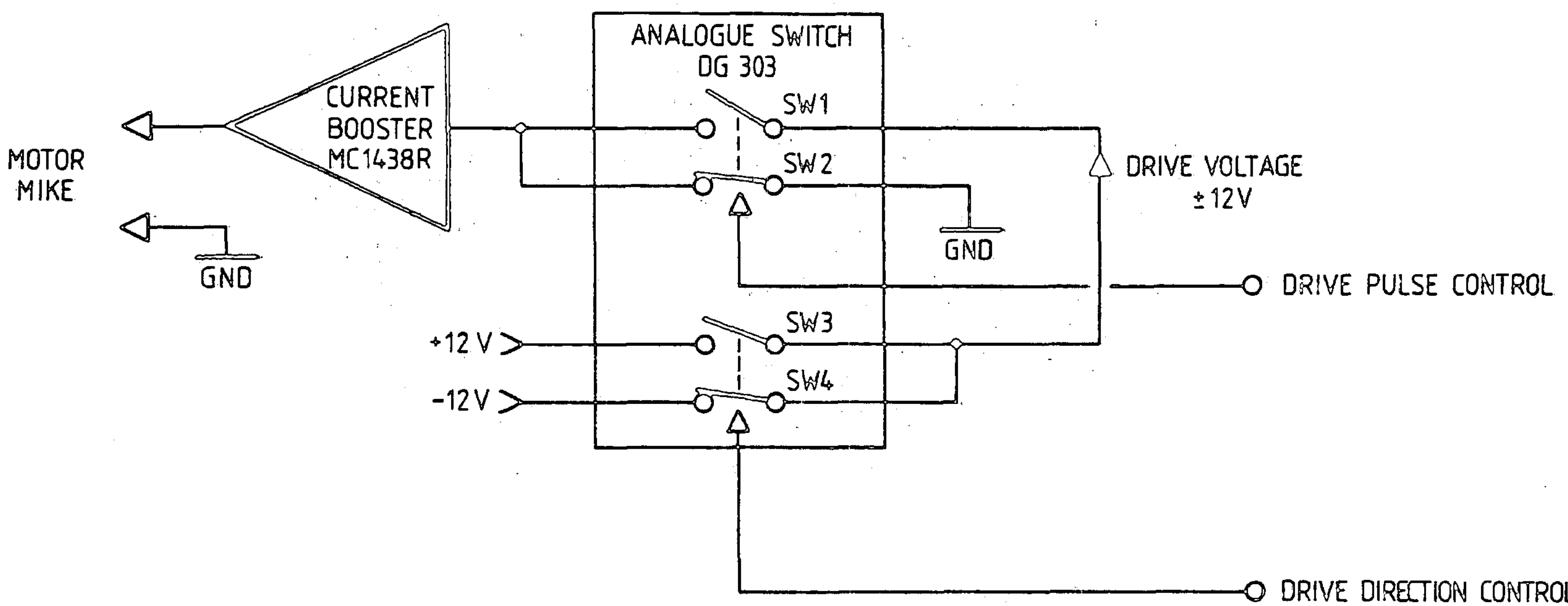


Figure 6.8

peripheral interface adaptor (PIA), (Figure 6.9). One of the PIA's registers is configured as an output port to provide DRIVE PULSE WIDTH and DRIVE DIRECTION CONTROL for each drive channel (Table 6.2). A combination of hardware address decoding (A2-A15) and microprocessor programme control (A0, A1) is used to select the PIA's internal registers. These are configured during system initialization; thereafter, the Motor Mikes are controlled by loading instruction data into the appropriate register.

Table 6.1 MOTOR MIKE DRIVE CONTROL

DRIVE PULSE CONTROL	DRIVE DIRECTION CONTROL	CONTROL OPERATION
0	0	No motion
0	1	No motion
1	0	-12 V drive voltage applied (backward motion)
1	1	+12 V drive voltage applied (forward motion)

Table 6.2 MOTOR MIKE PIA DRIVE CONTROL BIT ASSIGNMENT

	CHANNEL 1		CHANNEL 2		CHANNEL 3	
PIA REGISTER BIT	D0	D1	D2	D3	D4	D5
FUNCTION	DIRECTION	DRIVE	DIRECTION	DRIVE	DIRECTION	DRIVE

MOTOR MIKE DRIVER CARD

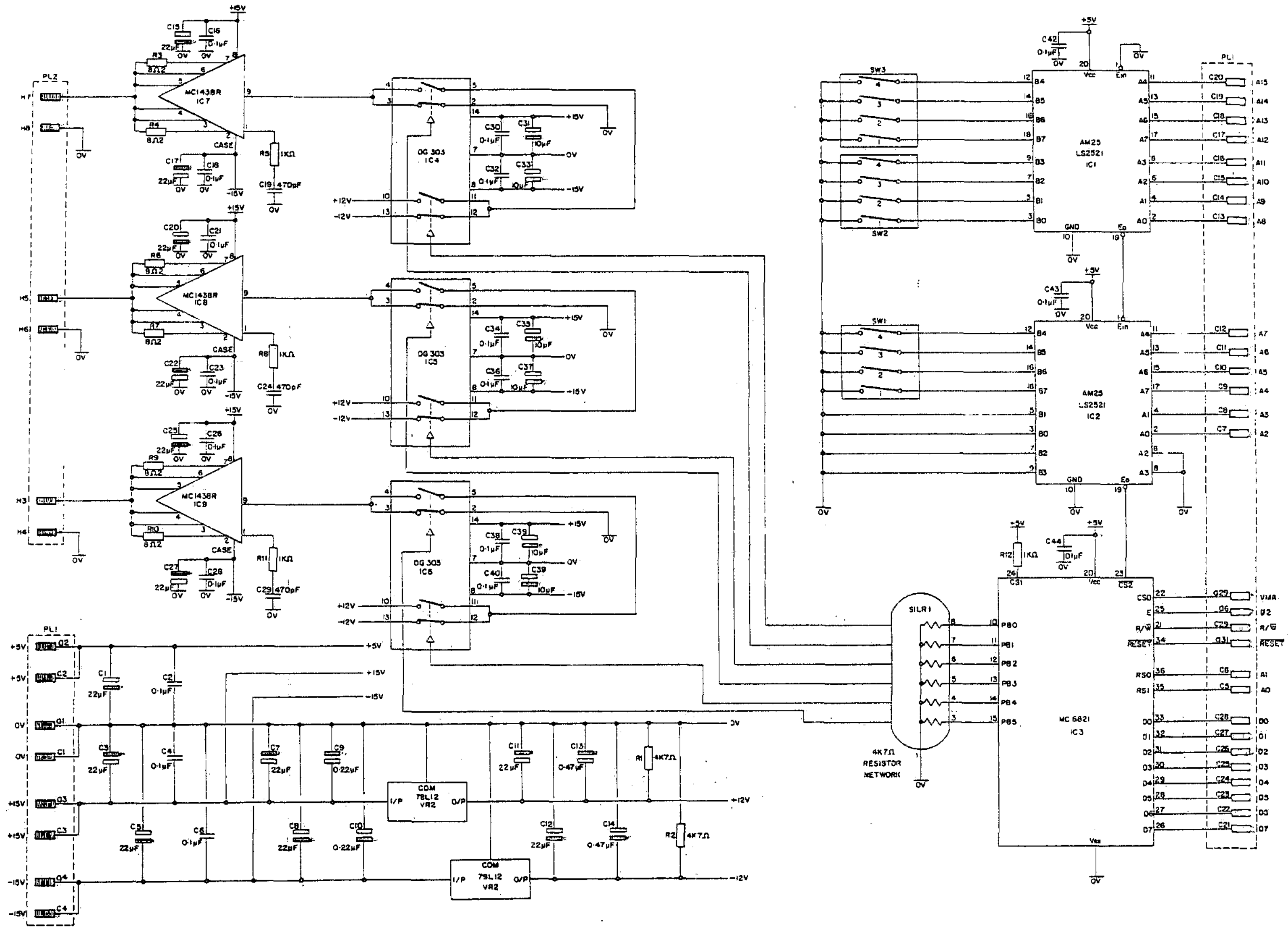


Figure 6.9

6.5.4 Focus Adjustment Position Encoding

The focus adjustment position encoding is provided by miniature Linear Variable Differential Transformer (LVDT) transducers supplied by RDP Electronics (type 222-0050).

Figure 6.10 shows a schematic of the LVDT, its control electronics and electromechanical output characteristic. The transducer consists of a primary coil and two secondary coils symmetrically spaced on a cylindrical former. A rod-shaped armature which is free to move inside the coil assembly provides a path for magnetic flux linking the primary and secondary windings.

The primary coil is energized by a 5 V, 5 kHz AC supply provided by the transducer's external control electronics (RDP Electronics - oscillator and demodulator, type D7). This induces a voltage in each of the secondary windings. These are connected series opposing so that the two voltages are of opposite polarity. The net output of the transducer is the difference between these voltages, which is zero when the armature is in the central (or null) position, and which varies linearly with armature displacement.

The differential output is cabled to a phase-sensitive demodulator in the control electronics. This generates an analogue DC voltage output, proportional both in magnitude and polarity to the armature's displacement from null. A 10 kΩ output load impedance is needed for correct operation of the demodulator. Output gain and offset are adjustable to allow user alignment and calibration. In this application, it was convenient to use only ±1.024 mm of the transducer's nominal working range of ±1.25 mm in order that the range of position encoding should match the binary output encoding of an analogue-to-digital converter. The control electronics were adjusted to give ±4 V DC output over this range.

The transducers are mounted inside the camera enclosure, one adjacent to each of the focus adjustment micrometers. Their coil housings are fixed in the field-flattening lens support ring and

LVDT POSITION ENCODER

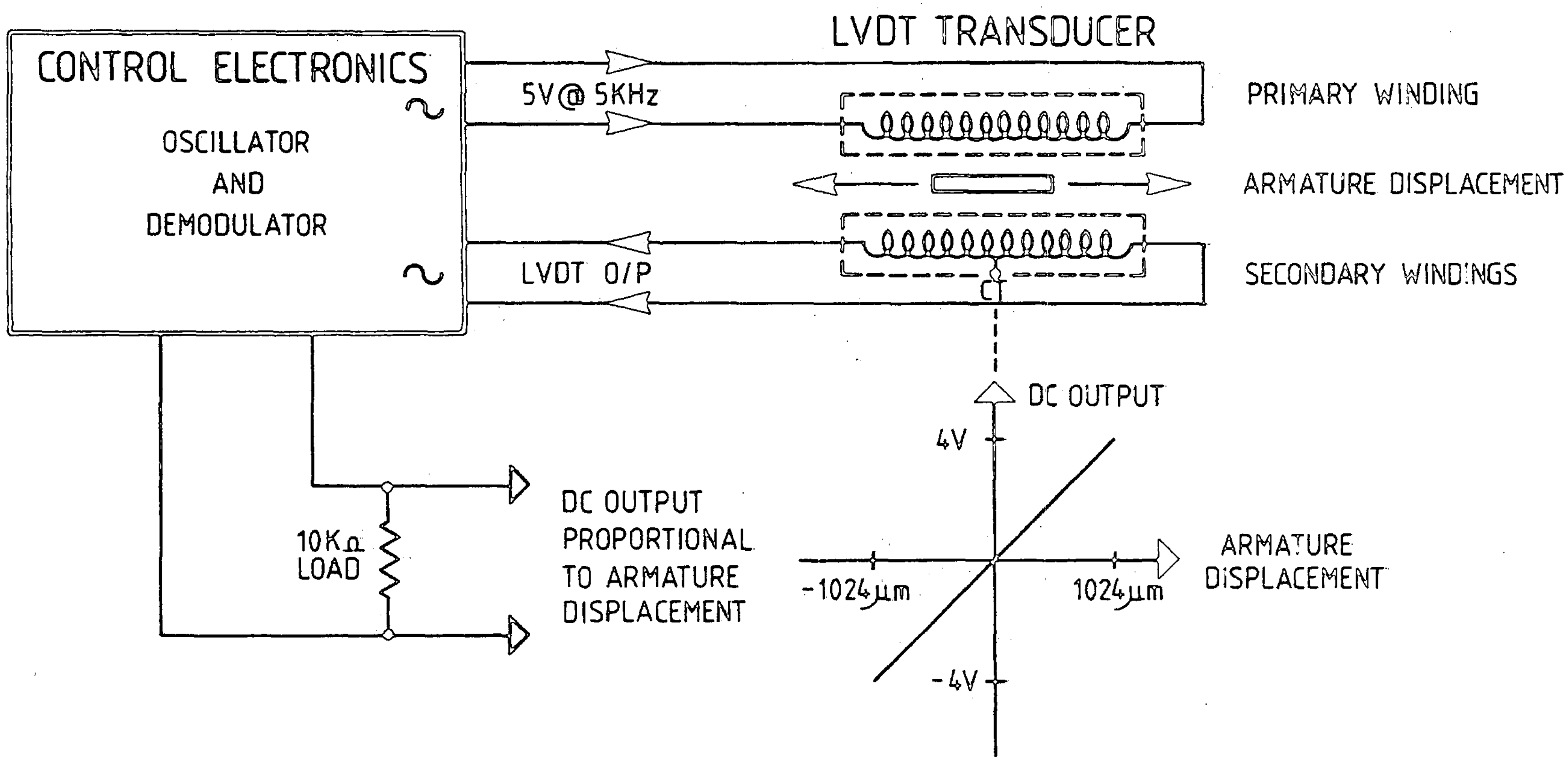


Figure 6.10

their armatures are located by nylon screws mounted off the CCD support ring. The screws permit the alignment of each transducer during final stages of camera assembly. Rotating the focus adjustment micrometers displaces the CCD support ring, and hence the LVDT armatures, resulting in a corresponding change in the encoder outputs. (Note - the LVDTs were not fitted when the photographs reproduced in Figures 6.5 and 6.6 were taken).

6.5.5 LVDT Signal Conditioning and Digitization

The analogue outputs from the LVDT demodulators have to be digitized in order that the microprocessor can read the focus position. An MMS analogue-to-digital converter (ADC) card was chosen for this purpose.

Examination of the analogue output from the LVDT's demodulator unit revealed an inherent noise component of 40 mV peak-peak, attributable to the 5 KHz AC supply to the transducer's primary winding (see the upper trace of the scope photograph reproduced in Figure 6.11). For maximum encoder resolution, this noise must be attenuated prior to digitization. Signal conditioning electronics incorporating a low-pass filter were designed for this purpose, taking into account the following aspects of the system.

(i) The design objectives of the focus adjustment system are satisfied by a design with positioning to 4 μm resolution over a range 0-2044 μm. Analogue-to-digital conversion of at least 9 bits precision is therefore required.

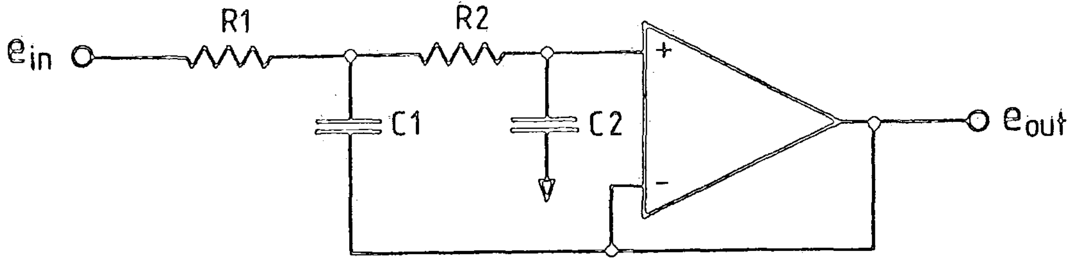
(ii) The specifications of the MMS ADC:
- 16 input channels to a sample-and-hold amplifier (3 channels are needed)
- sample acquisition time = 18 μs
- 12 bit analogue-to-digital conversion
- input signal range, -5 V to +5 V
- 1 analogue-to-digital conversion unit (1 ADU or LSB) = 2.44 mV

(iii) 12 bit digitization over a 0-2044 μm range provides position encoding to 0.5 μm resolution. This permits the design of a closed-loop microprocessor software control system that attempts to position to 0.5 μm accuracy, but which recognizes that an encoder readout satisfying the user requested position to 4 μm resolution is acceptable, i.e. the software only has to position to one of the 0.5 μm positions within a 4 μm window. The advantage of this system is that the possibility of drive control hunting to a position defined by least significant bit data is much reduced by having a range of values which are acceptable within the window. Repeatable 12 bit analogue-to-digital conversion (neglecting ±0.5 LSB conversion error) necessitates that the noise from the LVDT is attenuated to a level of less than 0.5 ADUs.

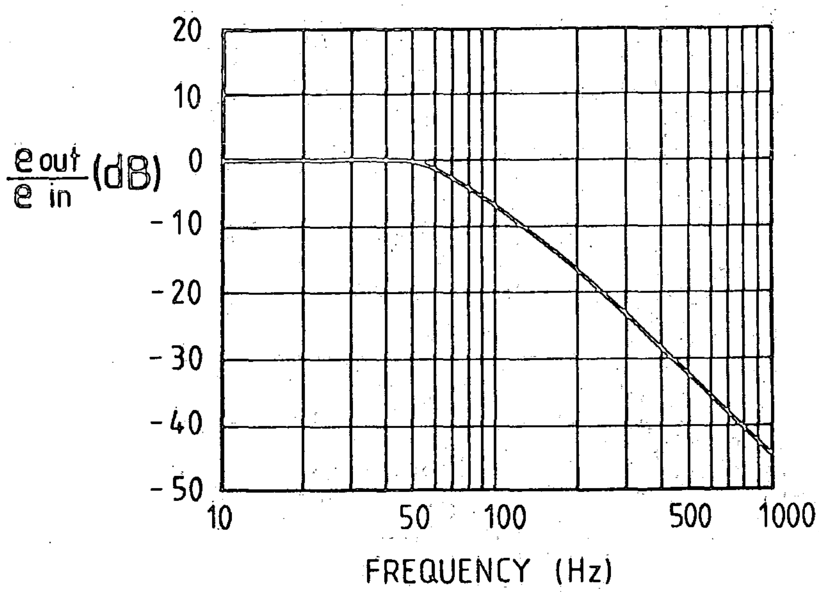
(iv) The LVDT demodulator output of ±4 V has to be scaled to match the ±5 V input range of the MMS ADC (i.e. a voltage gain = 1.25 is required). This means that the LVDT noise will be scaled proportionally to 50 mV peak-peak at 5 KHz (200 μs period). Digitization to 12 bits precision with a sample acquisition time of 18 μs, which is much smaller than the time period of the noise, will result in non-repeatable conversion amounting to 20 ADU peak-peak which is equivalent to 10 μm position resolution. The aim is to attenuate the noise to below 0.5 ADU at 5 KHz (i.e. to below 1.2 mV) while maintaining unity voltage gain at low frequencies so as to preserve the response time of the system at frequencies relevant to the servo control system.

A Butterworth second-order, low-pass active filter (see for example: Hilburn and Johnson, 1973) was chosen to provide the necessary attenuation of the LVDT's noise. A circuit diagram is shown in Figure 6.11. The components were selected to give a cut-off frequency of 78 Hz, which is greater than the maximum digitization rate and which, with a voltage gain response characteristic of -12 dB per octave, gives 75 dB signal attenuation at 5 KHz. The response characteristic of the filter is shown in Figure 6.11.

SECOND-ORDER LOW-PASS FILTER



LOW-PASS FILTER FREQUENCY RESPONSE



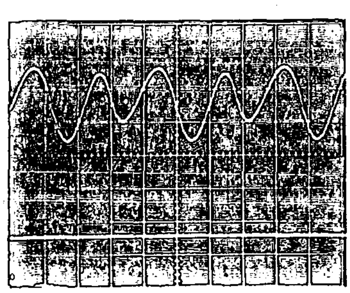
R1 = R2 = 15KΩ

C1 = 0·22µF

C2 = 0·10µF

$$f_o = \frac{1}{2\pi\sqrt{R1\,R2\,C1\,C2}}$$

= 72 Hz



20 mV/DIV. LVDT DEMODULATOR OUTPUT

5mV/DIV. SIGNAL CONDITIONING ELECTRONICS OUTPUT

50µs/DIV.

Figure 6.11

The filter was found to have the desired effect, attenuating the LVDT's noise such that it could not be detected against ±0.5 LSB digitization error. For comparison, the scope photograph reproduced in Figure 6.11 shows the filter's input and output signals and the resultant attenuation of the LVDT's noise.

6.5.6 Signal Conditioning Electronics

The design of the LVDT signal conditioning electronics is shown in Figure 6.12. There are three stages in the signal chain:

(i) Input Buffer
- a differential amplifier of unity voltage gain. This provides common-mode rejection of any extraneous noise induced in the cabling from the LVDT demodulator unit. The 10 kΩ load resistance needed for correct operation of the demodulator is connected across the inputs to the amplifier.

(ii) Low-pass active filter (as described above)

(iii) Scaling amplifier
- an amplifier of voltage gain = 1.25 to scale the demodulator's ±4 V output to the ±5 V input range of the MMS ADC.

An MMS compatible Eurocard was designed to accommodate three signal conditioning channels. A circuit diagram is shown in Figure 6.13.

6.6 Hartmann Shutter Assembly

The Hartmann shutters provide a means of assessing the camera focus by taking CCD exposures of a comparison arc lamp and examining the Hartmann shift of spectral lines. The shutters are located in the f/15 diverging beam between the folding-flat mirror and the spectrograph camera. A photograph of the assembly is reproduced in Figure 6.14.

Each shutter blade is connected by a shaft to a pneumatically operated 95^{o} rotary actuator (Kuhnke, type 701.000). The shaft is rotated by the

LVDT SIGNAL CONDITIONING

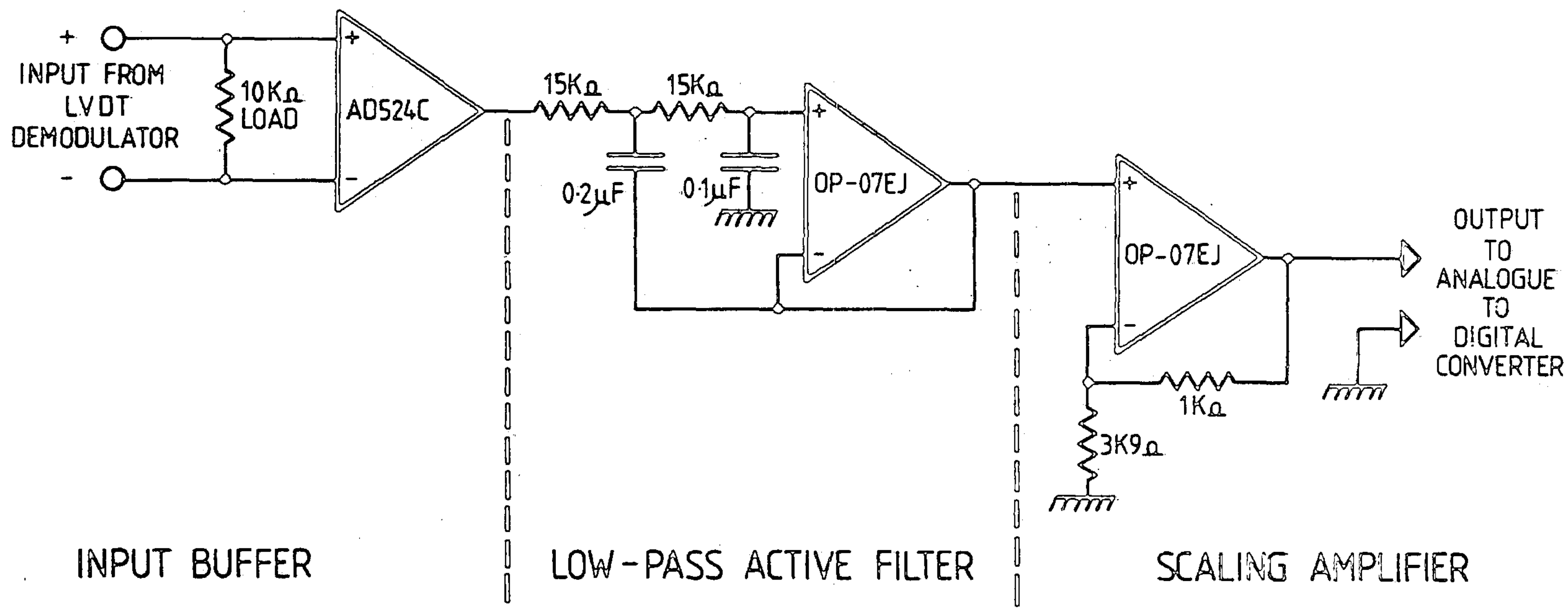


Figure 6.12

LVDT SIGNAL CONDITIONING CARD

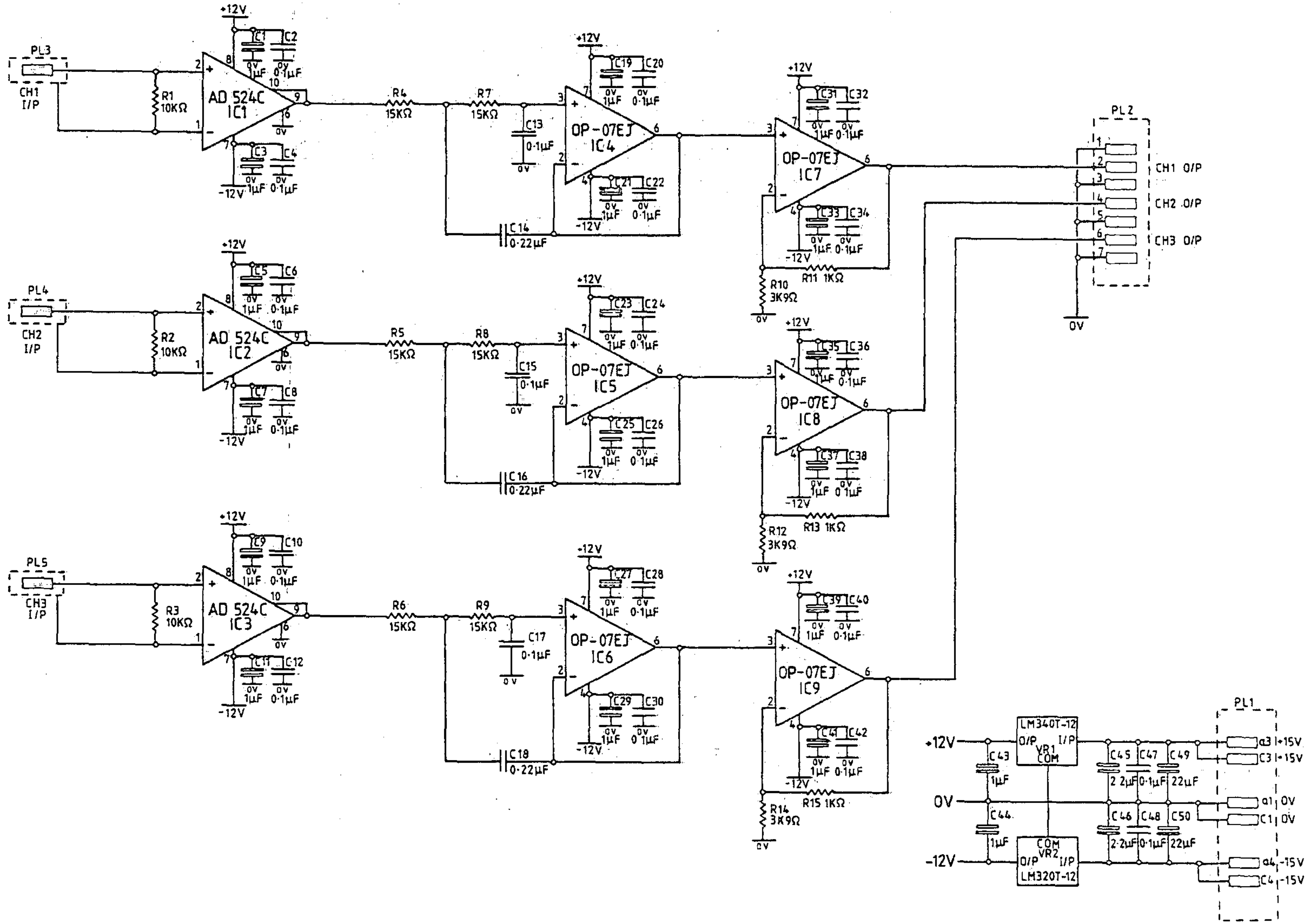


Figure 6.13

HARTMANN SHUTTERS

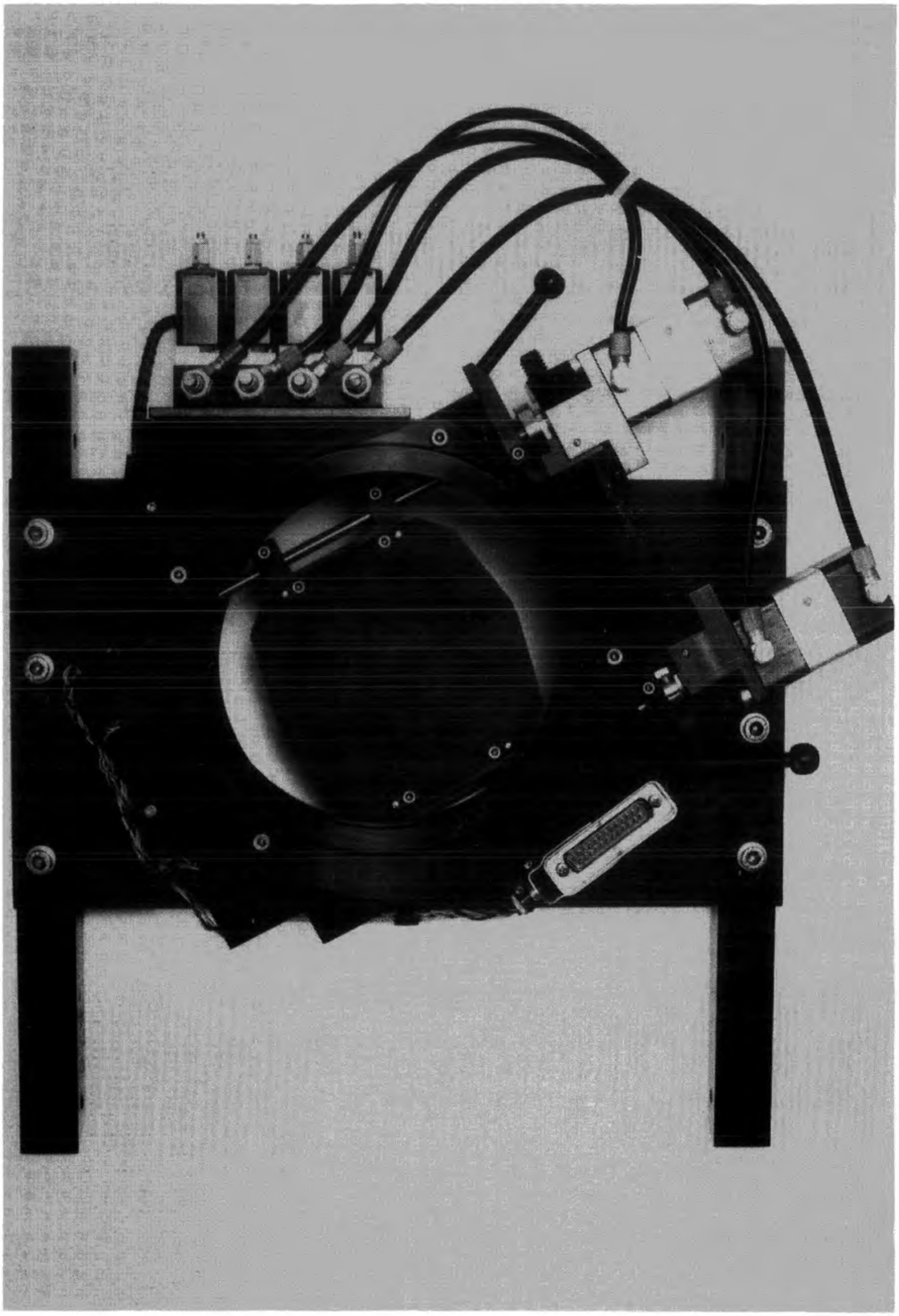


Figure 6.14

application of compressed air through one of two pneumatic supply inlets. The direction of rotation is determined by which of the two inlets the supply is applied to.

Solenoid valves (Kuhnke, type 65.111) gate the compressed air supply to the actuator inlets. Gas pressure need only be maintained for the period of shaft rotation (approximately 2 seconds with a pneumatic supply of pressure 70 psi). In operation, the compressed air supply to the solenoid valves is obtained from an outlet on the IDS.

Slotted proximity switches (Hettich, type SO 35 A/R) are used to encode the open and closed positions of each Hartmann shutter. The switch contains a miniature oscillator and a detector positioned on either side of a slot. The oscillator induces a signal in the detector which is interrupted by the insertion of a metal blade inside the slot, thereby causing the switch output to change state.

Two proximity switches and a metal blade attached to the rotary actuator shaft encode the position of each shutter. The design ensures that the metal blade is located inside one switch when the shutter is open and the other switch when the shutter is closed. An open, closed or intermediate position of the shutter may therefore be determined by reading the output status of each switch.

6.6.1 Microprocessor Control

The Hartmann shutters are interfaced to the local microprocessor controller through an MMS peripheral interface adaptor (PIA) card (Figure 6.15).

Port B of the PIA is configured as an output register. Bits PB0-PB3 are connected to the solenoid valves via open-collector buffers and enable independent drive control for each valve. To open or close a shutter, the microprocessor is instructed to set the appropriate register bit for a period which is sufficient for the pneumatic supply to complete the rotation of the actuator shaft.

Port A of the PIA is configured as an input register. Bits PA0-PA3 are connected to the proximity switches from which the microprocessor can read the position status of each shutter.

CONTROL OF THE HARTMANN SHUTTERS

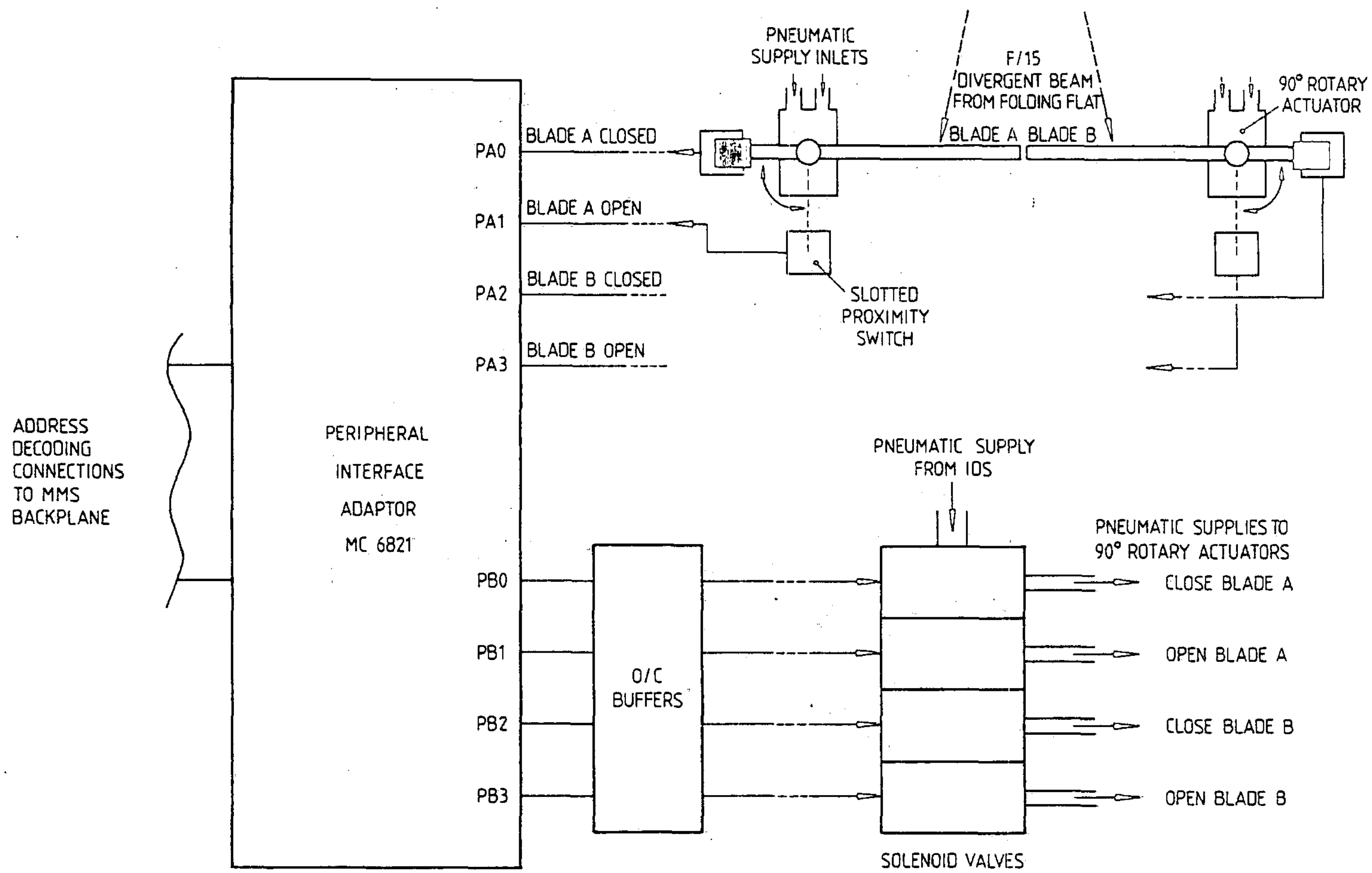


Figure 6.15

6.7 Local Microprocessor Controller Electronics

A block diagram of the local microprocessor controller electronics is shown in Figure 6.16. The components and their functions are listed below:

(i) MMS microprocessor card - Motorola 6800 microprocessor.

(ii) MMS 16 Kbytes memory card (1) - populated as follows:
- 8 Kbytes EPROM (Hex C000 - DFFF) containing Promforth. (A memory map is shown in Figure 6.17)
- 2 Kbytes EPROM (Hex F800 - FFFF) containing microprocessor reset and interrupt vectors.

(iii) MMS 16 Kbytes memory card (2) - populated as follows:
- 4 Kbytes RAM (Hex 0000-0FFF) containing FORTH stacks, variables and system variables.
- 6 Kbytes EPROM (Hex 1000-2FFF) containing the application dictionary.
- 4 Kbytes RAM (Hex 3000-3FFF) containing FORTH disc buffers and any additional application dictionary entered from the engineer's terminal.

(iv) MMS buffer, reset, timer card - only the reset circuitry is used; its function is to activate the microprocessor reset line on switch-on. This causes the microprocessor to access its reset vector from which programme execution is directed to the head of the FORTH application dictionary.

(v) MMS ACIA card - populated with two Motorola 6850 ACIAs each of which is configured to operate at 9600 baud. One channel is dedicated to command and status communication with the telescope's instrumentation control computer. The other channel remains available for the connection of an engineer's terminal for diagnostic testing of the controller.

(vi) MMS PIA card - for control of the Hartmann shutter assembly.

FAINT OBJECT SPECTROGRAPH LOCAL MICROPROCESSOR CONTROLLER

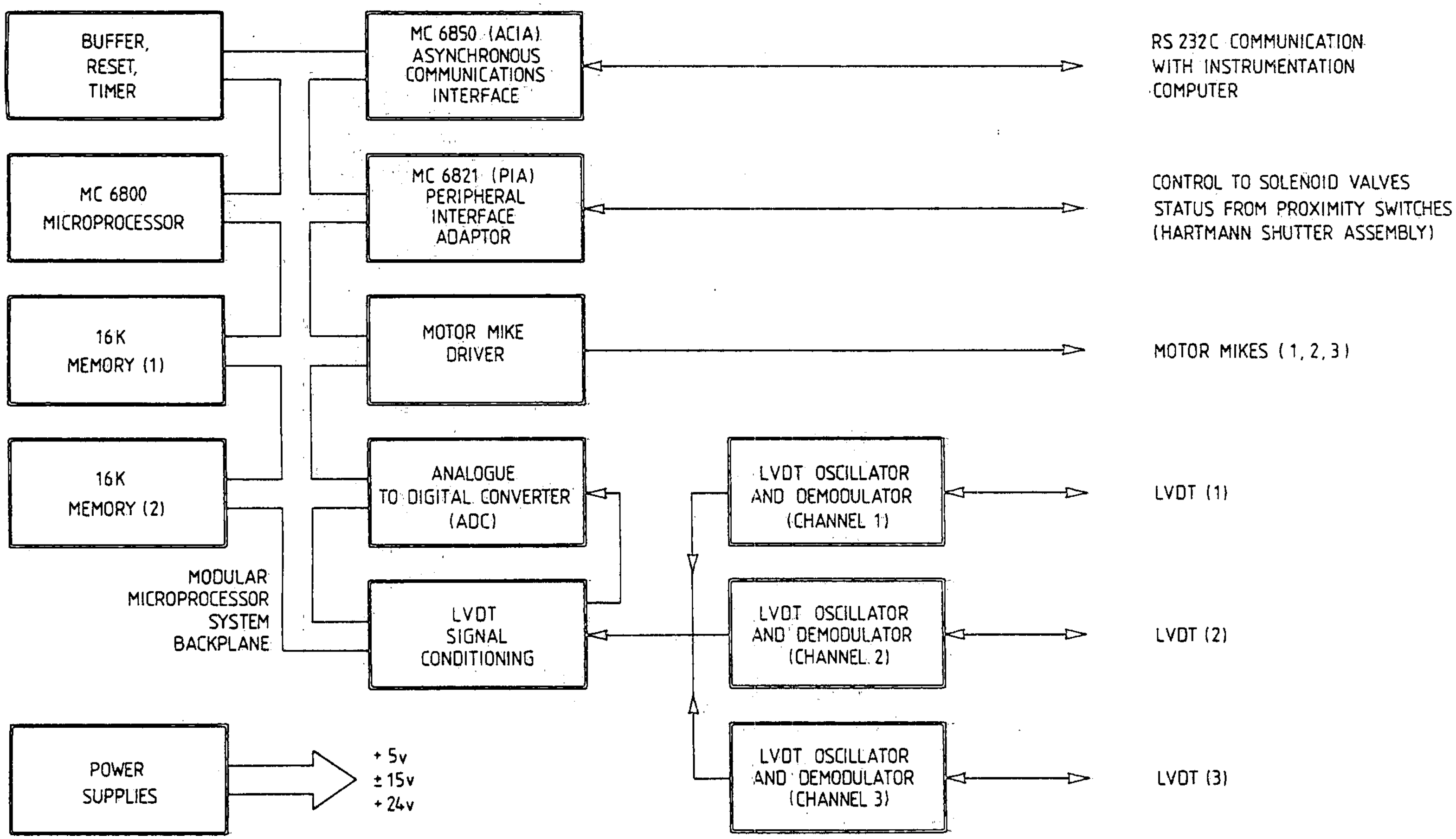


Figure 6.16

FAINT OBJECT SPECTROGRAPH LOCAL CONTROLLER MEMORY MAP

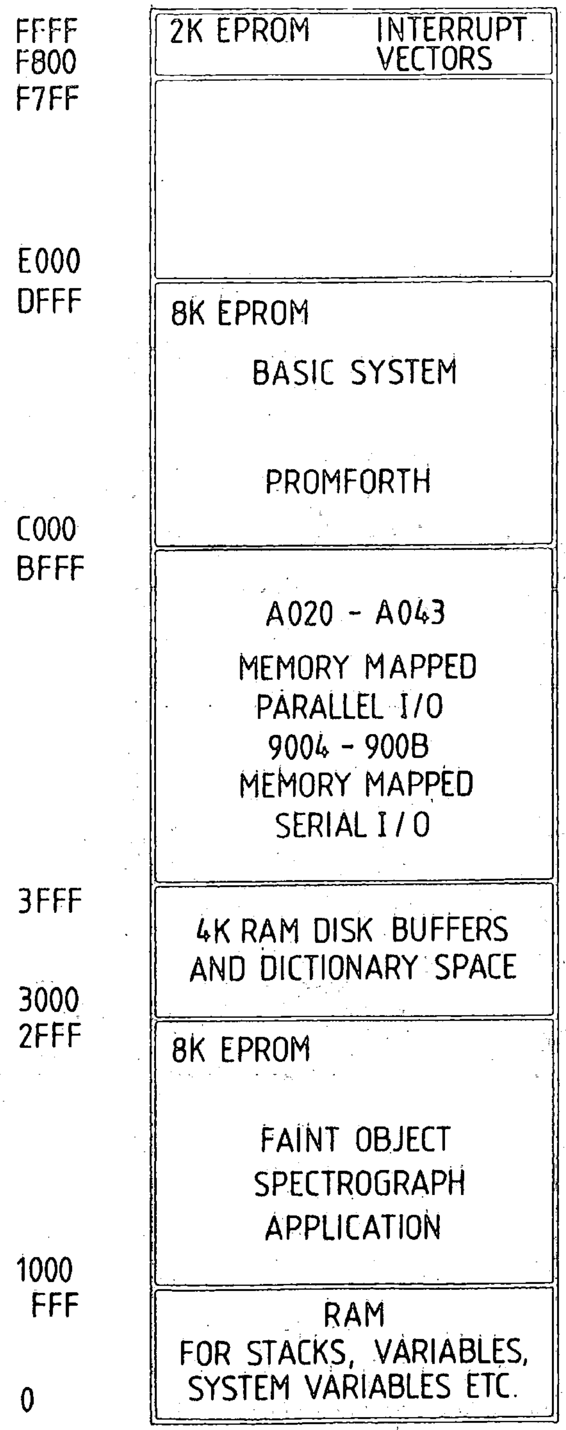


Figure 6.17

(vii) Motor Mike driver card.

(viii) LVDT signal conditioning card.

(ix) MMS analogue-to-digital converter card.

A Eurocard chassis houses the MMS components, the LVDT oscillator and demodulator units and power supplies. Military Pattern 105 connectors mounted on the rear panel provide the wiring interface to the spectrograph camera, the Hartmann shutters and the instrumentation control computer.

6.8 Software Development

The local microprocessor controller software was developed on a Motorola Exorciser. This was connected through a User System Evaluation (USE) module to an MMS chassis housing the electronics needed to drive the Motor Mikes, read the LVDTs and control the Hartmann shutter assembly. In this configuration, the microprocessor within the MMS chassis is replaced by the USE module so that programme execution and peripheral addressing is directed through the Exorciser's internal microprocessor. Floppy discs were used for programme storage. The procedure used to develop the target application software is outlined below:

(i) The software was written on the Exorciser using its facilities for programme editing. A compiled FORTH application dictionary was generated to run in RAM located within the Exorciser and its basic operation was tested.

(ii) The software was modified to allow the generation of a dictionary which could be copied to RAM located within the MMS chassis to work in conjunction with Promforth.

(iii) A copy of the MMS RAM-based application dictionary was modified to link its header to the microprocessor's reset vector thereby creating a system which would run in a stand-alone mode from switch-on. This software was programmed into EPROMs and installed within the MMS. The USE module was removed and replaced by an MMS microprocessor card thus completing the target system.

6.9 Application Programme

Figure 6.18 shows the organization of the local microprocessor controller application programme. It consists of an interrupt service routine and five background tasks which are executed in a round-robin sequence.

The interrupt service routine reacts to command messages received on the RS232C serial communication link with the telescope's instrumentation computer. It checks the format of a received message to ensure that its instrument and task identification characters are valid (see 6.9.1 Communication Protocol). The data of accepted command messages are copied into a variable array referred to as the Command Table (SETTAB).

The spectrograph's mechanisms are controlled by four background tasks; three are dedicated to the Motor Mikes, the fourth to the Hartmann shutter assembly. Each task interrogates the Command Table for new instructions, performs any necessary control action and enters mechanism status in a common variable array, the Status Table (STAT).

The fifth background task (RETURN) supervises the transmission of status messages on the serial link in response to status request commands entered in SETTAB. Character transmission from the controller's ACIA channel is interrupt driven. A mechanism's status is sent either immediately or when the mechanism has completed its current operation depending on the nature of the status request command.

6.9.1 Communication Protocol

A protocol was defined for command and status communication between the INT's instrumentation computer and the FOS microprocessor controller. Each message consists of a string of ASCII characters as outlined below:

LOCAL MICROPROCESSOR CONTROLLER APPLICATION PROGRAMME

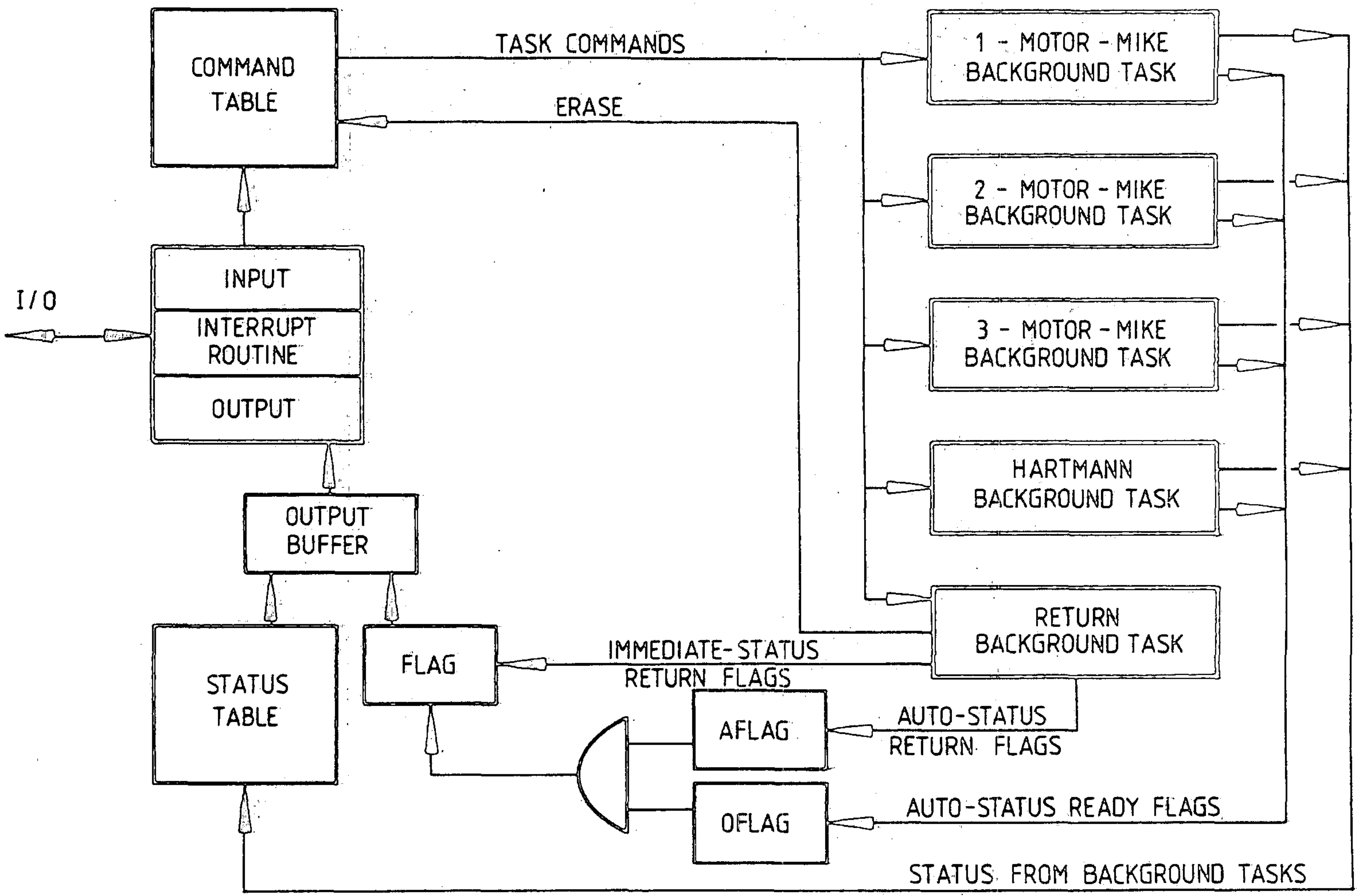


Figure 6.18

(1) Command Messages

Command messages are divided into two categories (mechanism and status) but are of a similar format:

Command message: (Xxxxxxx

´(´ open-bracket is an instrument identification character for FOS and is treated by the controller as the start of a new command message.

´X´ X = A,B,C, or D is an identification character to one of the mechanism background tasks. X = S identifies a request for status.

´xxxxxx´ six hexadecimal data digits which define the command type and the instruction data.

(1a) Mechanism commands

There are three commands available for the control of each mechanism:

(i) STOP: (X000000
STOP aborts the mechanism´s current control action and sets it to an inactive (default) state.

(ii) AUTOMATIC MOVE: (X10xxxx
AUTOMATIC MOVE instructs the mechanism´s control task to initiate movement to a position xxxx. The task checks the instruction data to ensure that the requested position is valid, i.e. within a predefined range. It monitors the progress of the movement and checks for possible system failure. When the instruction has been completed, AUTOMATIC MOVE is aborted and the mechanism is set to its default STOP state.

(iii) ENGINEERS: (X30000P

ENGINEERS is available for hardware diagnosis, enabling each component of a mechanism to be checked individually. The data ´P´ defines how the mechanism is to be driven.

(1b) Status request commands

Two commands are available to request the controller to return mechanism status:

(i) AUTOMATIC STATUS: (S10xxxx

Status may be requested for any number or combination of mechanisms using a single command. Each bit of xxxx identifies a different mechanism. AUTOMATIC STATUS instructs the background task RETURN to transmit the status of the mechanisms when they are set in a STOP state. If a mechanism is currently executing an AUTOMATIC MOVE command, RETURN waits for the move to be completed before sending the status.

(ii) IMMEDIATE STATUS: (S30xxxx

IMMEDIATE STATUS instructs RETURN to transmit the status of mechanisms identified by xxxx immediately, regardless of whether they are currently executing an AUTOMATIC MOVE command.

(2) Status messages

Status messages transmitted from the controller are of the form:

Status message:)XP0xxxx CR LF

´)´ close-bracket is an instrument identification character showing that the message was transmitted by the FOS microprocessor controller.

´X´ X = A,B,C or D identifies to which mechanism the status belongs.

´P´ P = 0 shows the mechanism was set to a STOP state when the status was transmitted.

P = 1 shows the mechanism was executing an AUTOMATIC MOVE when the status was transmitted.

´xxxx´ four hexadecimal data digits which are the mechanism´s status data.

´CR LF´ status messages are terminated with carriage-return, line-feed characters.

6.9.2 1-MOTOR-MIKE Background Task

1-MOTOR-MIKE is a background task dedicated to the control of one of the spectrograph camera focus adjustment micrometers. The other micrometers are controlled by similar background tasks: 2-MOTOR-MIKE and 3-MOTOR-MIKE.

1-MOTOR-MIKE (mechanism identifier = ´A´) enables focus adjustment in response to STOP, AUTOMATIC MOVE and ENGINEERS commands:

(i) STOP: (A000000

- disables the drive voltage supply to the Motor Mike. (Default state).

(ii) AUTOMATIC MOVE: (A100xxxx

- enables focus adjustment to a position xxx as encoded by the Motor Mike´s LVDT. xxx is in units of 4 μm in the range 0-2044 μm (Hex 0-1FF). The following are monitored during command execution:

  (a) The total time for which the procedure has been in progress. If a system failure occurs which prevents the Motor Mike driving to the requested position, for example mechanical seizure, then a software timer aborts the procedure to prevent programme execution from cycling indefinitely.

(b) The number of direction changes which occur during command execution. This is to prevent excessive hunting should the Motor Mike continually overshoot the requested position.

(c) Once the Motor Mike has driven to the requested position, a period is allowed for mechanical settling in the mechanism before control is aborted. During this period, any instability in the rest position shown by a changing LVDT reading causes positioning to be reactivated.

(iii) ENGINEERS: (A30000P

- enables the Motor Mike to be tested by allowing direct access to its drive electronics.

P = 0 or 1 disables the drive voltage.
P = 2 applies a forward motion drive voltage.
P = 3 applies a backward motion drive voltage.

The LVDT is not monitored and so it is possible to drive the focus adjustment micrometer outside the allowed range. The intention, therefore, is that this command should only be used to test the Motor Mike after it has been removed from the spectrograph camera so as not to risk damaging the internal components.

Figure 6.19 shows a structure diagram of **1-MOTOR-MIKE**. The task is organized as an indefinite loop, executed within a round-robin sequence with the other background tasks. The main programme structures and FORTH definitions are outlined below:

1-MOTOR-MIKE - the background task definition. At execution time, the task's parameter stack is constructed from default instruction data in the Command Table and some run-time condition flags. This is followed by entry of an indefinite loop.

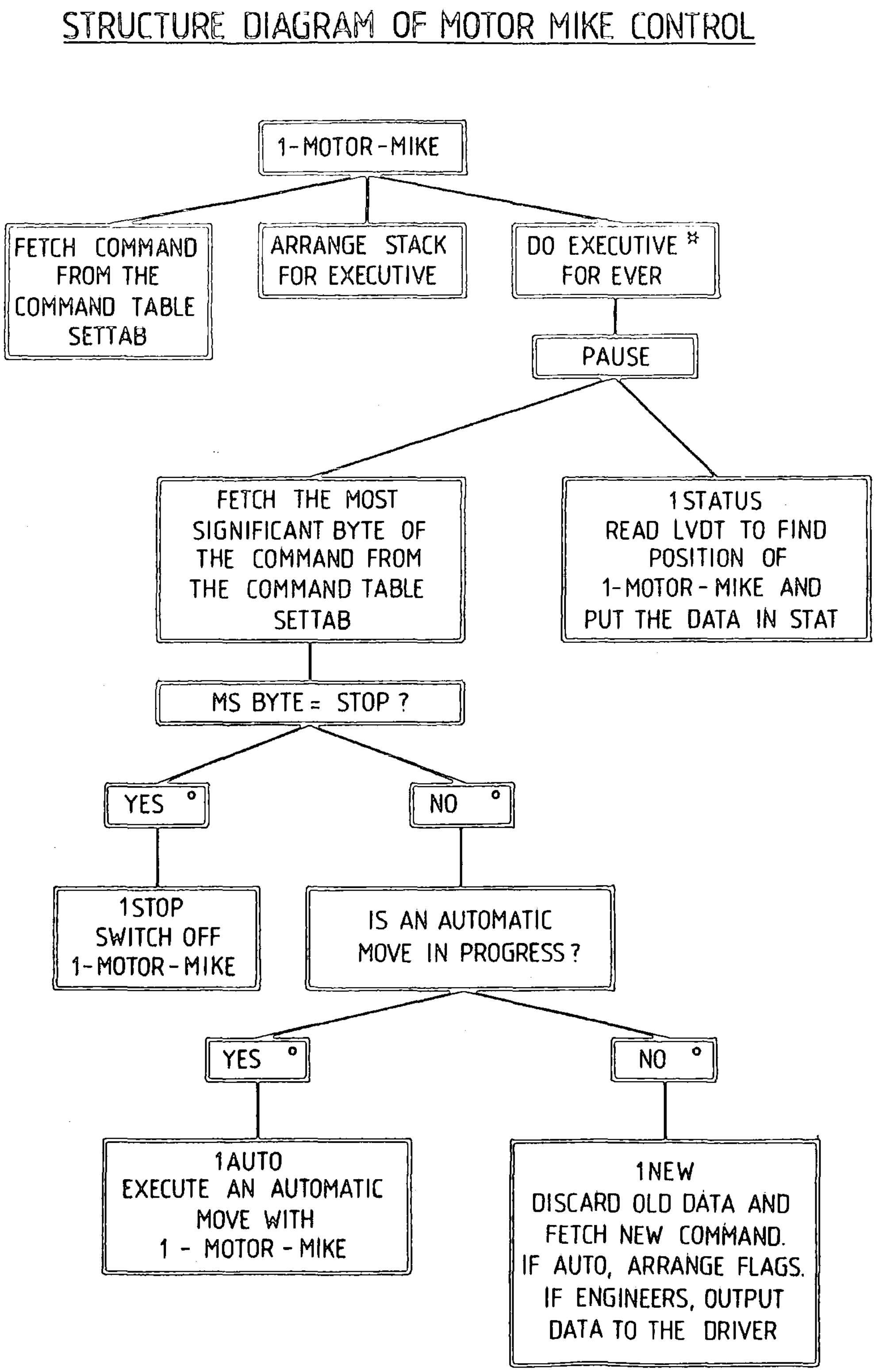

STRUCTURE DIAGRAM OF MOTOR MIKE CONTROL
1-MOTOR-MIKE
FETCH COMMAND FROM THE COMMAND TABLE SETTAB
ARRANGE STACK FOR EXECUTIVE
DO EXECUTIVE * FOR EVER
PAUSE
FETCH THE MOST SIGNIFICANT BYTE OF THE COMMAND FROM THE COMMAND TABLE SETTAB
1STATUS READ LVDT TO FIND POSITION OF 1-MOTOR-MIKE AND PUT THE DATA IN STAT
MS BYTE = STOP ?
YES °
NO °
1STOP SWITCH OFF 1-MOTOR-MIKE
IS AN AUTOMATIC MOVE IN PROGRESS?
YES °
NO °
1AUTO EXECUTE AN AUTOMATIC MOVE WITH 1 - MOTOR - MIKE
1NEW DISCARD OLD DATA AND FETCH NEW COMMAND. IF AUTO, ARRANGE FLAGS. IF ENGINEERS, OUTPUT DATA TO THE DRIVER

Figure 6.19

PAUSE - a FORTH definition which instructs programme execution to jump to the next background task in the round-robin sequence. Programme execution proceeds from **PAUSE** when it returns to **1-MOTOR-MIKE**.

The most significant byte of the instruction data currently held in the Command Table is tested to see if it is a STOP command. If true, **1STOP** is executed.

1STOP - disables the drive voltage supply to the Motor Mike.

A non-valid STOP command causes a run-time flag held on the stack to be tested to see whether an AUTOMATIC MOVE procedure is currently active. If true, programme execution is directed to **1AUTO**.

1AUTO - a structure diagram is shown in Figure 6.20. The command data is checked to ensure that the requested position is valid, i.e. xxx is in the range Hex 0-1FF. If not, the AUTOMATIC MOVE procedure is aborted and the instruction in the Command Table is erased.

1TIMER - maintains a count of the number of times **1AUTO** has been executed during the current AUTOMATIC MOVE procedure. System failure resulting in a count ´timeout´ causes the procedure to be aborted.

1AGO - reads the LVDT to determine the current position and compares it for equality with the position requested in the AUTOMATIC MOVE command.

1SETTLED - executed if the equality tested in **1AGO** is satisfied. A counter of successive **1SETTLED** execution is incremented. The counter ´timeout´ limit indicates mechanical stability in the mechanism in which case, the AUTOMTIC MOVE procedure is aborted.

STRUCTURE DIAGRAM OF MOTOR MIKE AUTOMATIC MOVE

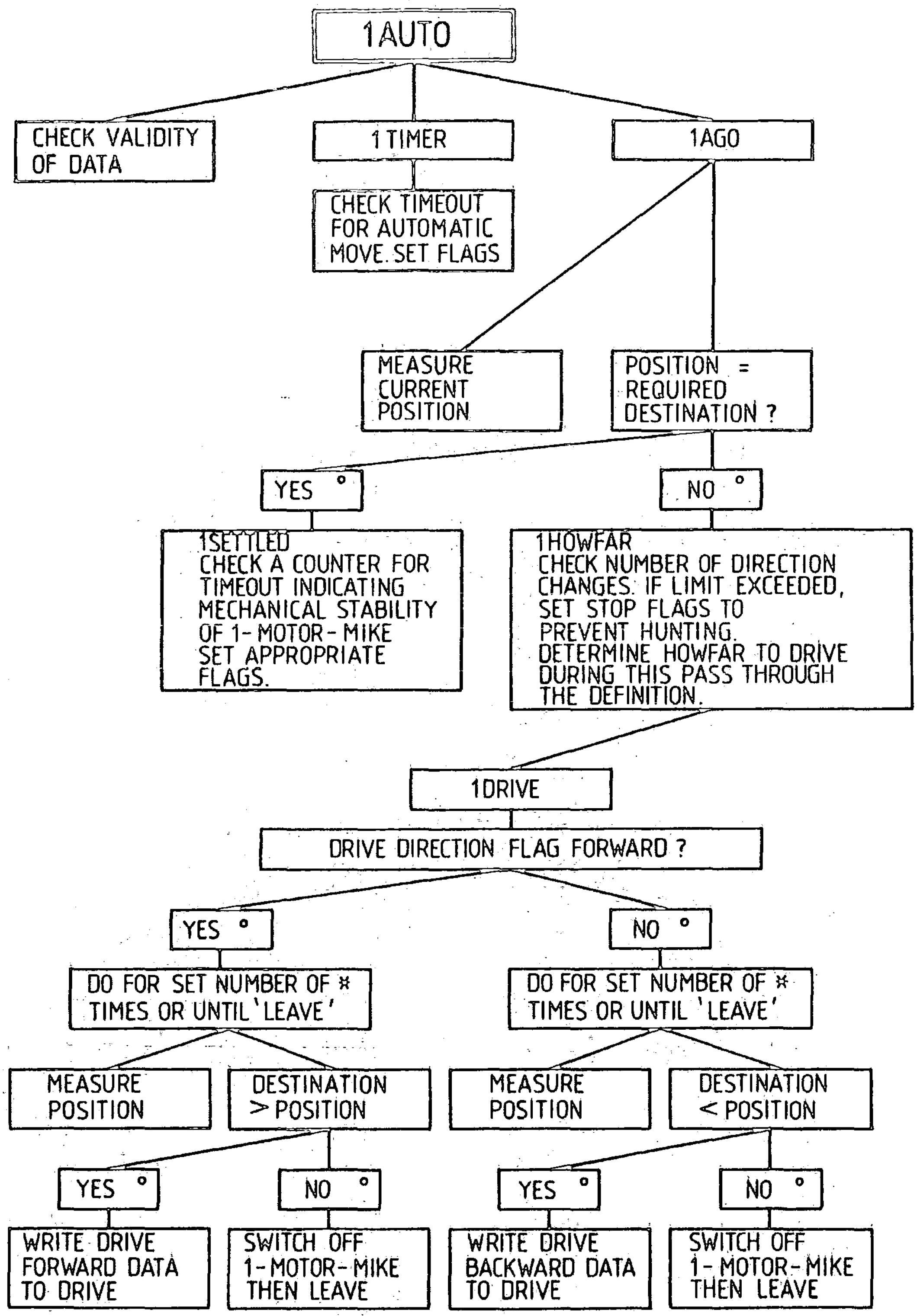


Figure 6.20

1HOWFAR - executed if the equality tested in 1AGO is not satisfied. The number of direction changes which have occurred during the current AUTOMATIC MOVE procedure is checked. A limit indicating excessive Motor Mike hunting causes the procedure to be aborted next time **1HOWFAR** is executed. The difference between the current and requested position is calculated and a drive direction flag determined. The speed at which the Motor Mike is driven towards its target is decreased as it approaches to help prevent overshoot. **1HOWFAR** calculates how far to drive the motor in the current execution of **1AUTO**.

1DRIVE - executes a loop in which power is applied to the motor and the current and destination positions are tested for equality. The loop is terminated when the equality is satisfied.

1NEW - executed if the instruction data in the Command Table is not that of a STOP command and the run-time flag on the stack shows that an AUTOMATIC MOVE command is not currently in progress (Figure 6.19). New command data is retrieved from the Command Table and tested to determine the command type. For a new AUTOMATIC MOVE command, the run-time flag on the stack is set. For an ENGINEERS command, the instruction data are written directly to the Motor Mike's drive electronics.

1STATUS - reads the LVDT encoder and writes the data into the Status Table. A subsequent status request command results in the transmission of a status message of the form:

)APOOxxx CR LF

xxx	the LVDT reading in units of 4 μm in the range 0-2044 μm (Hex 0-1FF).
P = 0	indicates that the Motor Mike is in a STOP state.
P = 1	indicates that the Motor Mike is currently engaged in an AUTOMATIC MOVE procedure.

6.9.3 HARTMANN Background Task

HARTMANN is the background task dedicated to the control of the Hartmann shutter assembly. (Mechanism identifier = ´D´). Its programme structure (Figure 6.21) is similar to that of 1-MOTOR-MIKE, organized as an indefinite loop with similar stack construction before loop entry and PAUSE control of task execution. The commands, the main task definitions and the status returned are outlined below:

commands:

(i) STOP: (D000000
- closes the solenoid valves thereby inhibiting the pneumatic supply to the rotary actuators. (default state)

(ii) AUTOMATIC MOVE: (D10000nm
- enables each shutter to be opened or closed.

m = 1 - close shutter A   n = 1 - close shutter B

m = 2 - open shutter A   n = 2 - open shutter B

(iii) ENGINEERS: (D30000P
- enables each solenoid valve to be tested individually.

P = 1 - open valve to close shutter A

P = 2 - open valve to open shutter A

P = 3 - open valve to close shutter B

P = 4 - open valve to open shutter A

task definitions and status:

4STOP - closes all solenoid valves.

4AUTO - opens the solenoid valves as instructed in the command data thereby enabling the pneumatic supply to the rotary actuators. It maintains a count of the number of times **4AUTO** has been executed during the current AUTOMATIC

STRUCTURE DIAGRAM OF HARTMANN SHUTTER CONTROL

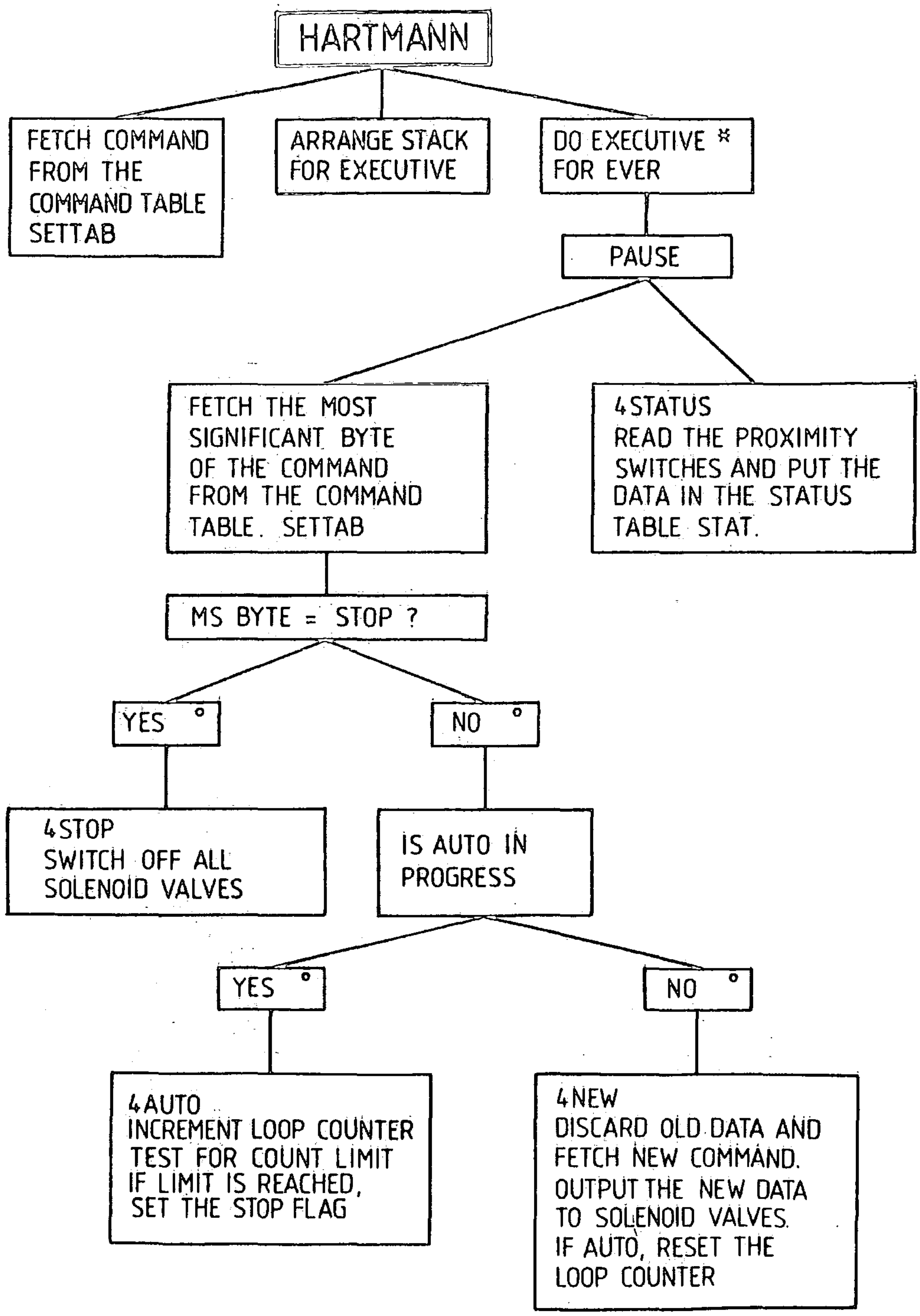


Figure 6.21

MOVE procedure. The counter's timeout is calculated to ensure the valves are open for sufficient time for the supply to rotate the actuator shafts.

4NEW - enables ENGINEERS control of the solenoid valves.

4STATUS - reads the proximity switches to determine the position of each shutter and writes the data into the Status Table. A subsequent status request command results in the transmission of a status message of the form:

)DP00a0b CR LF

P = 0	indicates the shutters are set to a STOP state.
P = 1	indicates the shutters are currently engaged in an AUTOMATIC MOVE procedure.
b (bit 0=1)	shutter A is closed.
b (bit 1=1)	shutter A is open.
b (bit 2=1)	shutter B is closed.
b (bit 3=1)	shutter B is open.
a (bit 0=0)	attempting to close shutter A
a (bit 1=0)	attempting to open shutter A
a (bit 2=0)	attempting to close shutter B
a (bit 3=0)	attempting to open shutter B

6.9.4 Engineer's Terminal Task

The local microprocessor controller's resident software includes a terminal task which, under normal operation, plays a passive role in the control of the spectrograph's mechanisms. Its function is to allow an engineer to test the system through a terminal connected to the controller's second ACIA channel. In this configuration, the engineer has access to all of the FORTH definitions. In addition, new definitions may be entered which are compiled for temporary storage in the task's dictionary space.

CHAPTER 7

FOS COMMISSIONING

7.1 Introduction

FOS was assembled and optically tested at the RGO over the winter 1983/84. It was shipped to La Palma in May 1984 and subsequently commissioned on three separate observing runs in July and December 1984 and in May 1985.

The way in which FOS was set up on the INT during the first of these commissioning periods is described briefly in this chapter. Also given is an outline of its operation, including its on-line data reduction facilities, and a summary of its instrumental performance.

7.2 Commissioning Schedule

FOS was unpacked and reassembled on its handling trolley in an instrument test room within the INT building, nine days in advance of the first night of its allocated commissioning time on the INT. During the period leading up to its installation on the telescope, the initial alignment of the optics was undertaken, following a procedure devised during laboratory testing at the RGO. This required the use of the CCD camera for obtaining test exposures, necessitating that the electronics were also set up in the test room and connected into the INT's computer data acquisition system. Besides enabling progress to be made with the optical alignment, the presence of the electronics in the test room also allowed the few remaining problems with the hardware and its control software to be sorted out prior to FOS going on the telescope.

FOS was installed on the INT during the afternoon preceding the first night allocated to observing. Most of the final optical alignment and focussing of the detector was completed during the remaining daylight hours, enabling the whole of the first night to be given over to observing. In all, five nights were allocated to observational commissioning of the instrument and assessing its performance.

7.3 Electronics and Computer Data Acquisition System

A schematic of the electronics and the computer data acquisition system is shown in Figure 7.1. The organization of the electronics can be summarized as follows:

(i) the CCD camera head electronics (preamplifier, digitization unit and temperature controller) were mounted within FOS′ open-frame structure, immediately beneath the camera body assembly, in order that their connections to the inside of the camera vessel could be of minimal length.

(ii) the CCD controller and the local microprocessor controller (connected to the camera head and focus adjustment mechanism subassemblies via 3 m cabling) were initially set up with FOS in the instrument test room in order to progress with the optical alignment. When FOS was later fitted to the telescope, they were installed in cubicles mounted off the bottom of the INT′s mirror cell support structure.

(iii) the CAMAC interface modules (the three CCD camera modules described in Chapter 3, and a commercial RS232C driver module for communication with the local microprocessor controller) were installed within a CAMAC branch crate in the CLIP (Control, Logic, Interconnection and Power) centre. This branch crate is connected to the CAMAC system crate, located in the INT′s control room together with the instrumentation computer hardware and the astronomer′s control console.

The CCD controller and the local microprocessor controller were designed to be connected to their CAMAC interface modules through the multiple twisted-pair cabling installed between the INT′s Cassegrain focus and the CLIP centre. However, this meant that in order to be able to operate the electronics in the instrument test room, it was necessary to have similar twisted-pair cabling temporarily installed in the ducting between the test room and the CLIP centre.

The instrumentation computer control system supervises the control of

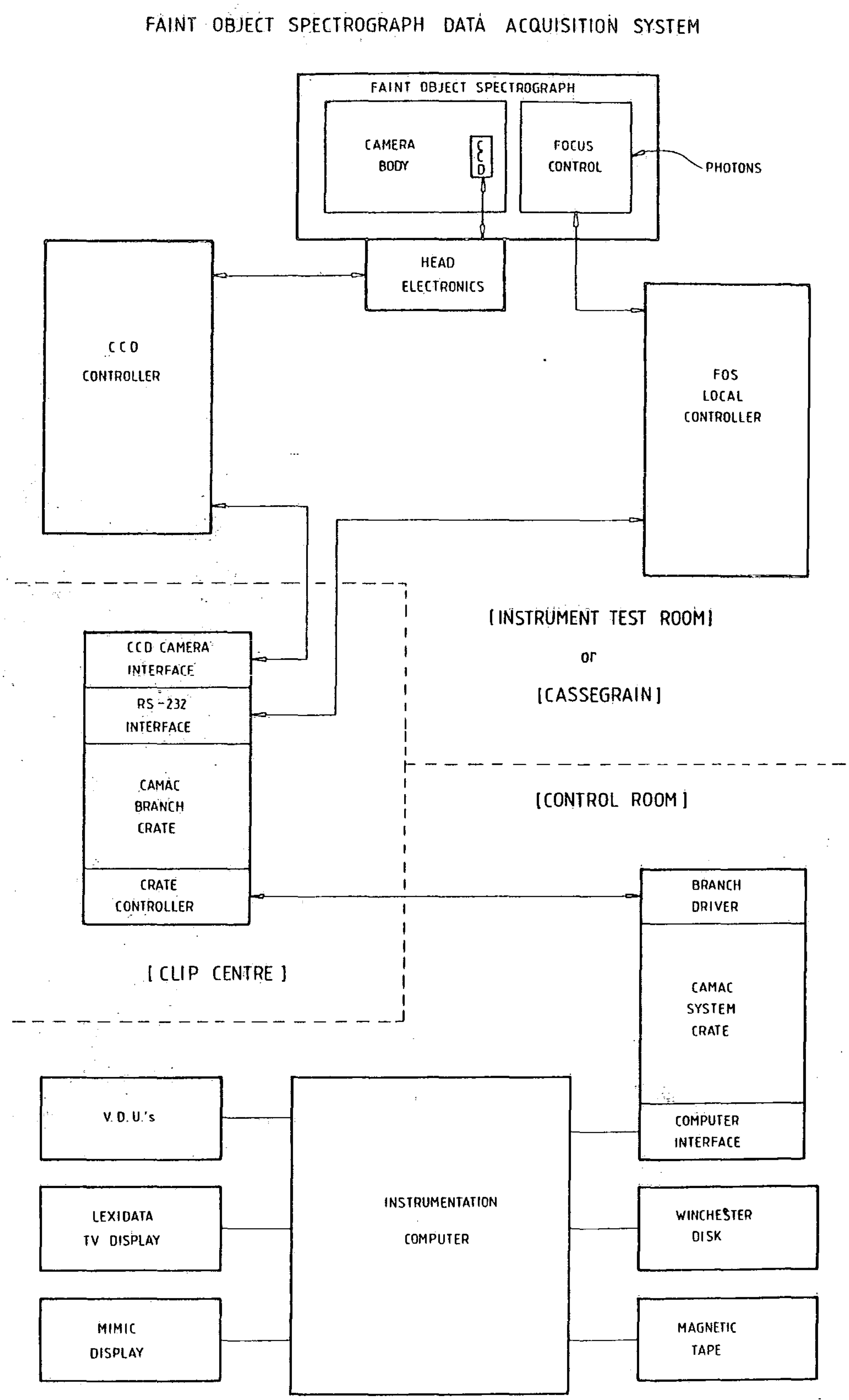

FAINT OBJECT SPECTROGRAPH DATA ACQUISITION SYSTEM
FAINT OBJECT SPECTROGRAPH
CAMERA BODY
CCD
FOCUS CONTROL
PHOTONS
HEAD ELECTRONICS
CCD CONTROLLER
FOS LOCAL CONTROLLER
[INSTRUMENT TEST ROOM]
or
[CASSEGRAIN]
CCD CAMERA INTERFACE
RS-232 INTERFACE
CAMAC BRANCH CRATE
CRATE CONTROLLER
[CLIP CENTRE]
[CONTROL ROOM]
BRANCH DRIVER
CAMAC SYSTEM CRATE
COMPUTER INTERFACE
V.D.U.'s
LEXIDATA TV DISPLAY
MIMIC DISPLAY
INSTRUMENTATION COMPUTER
WINCHESTER DISK
MAGNETIC TAPE

Figure 7.1

all of the INT's instruments and the acquisition, display, reduction and storage of data from detectors. The heart of the system is a Perkin Elmer 3220 mini-computer which is equipped with the following peripherals:

(i) a 98 Mbyte Ampex Winchester disc for the storage of data and a 10 Mbyte Drico disc (5 Mbyte fixed, 5 Mbyte removable) for the storage of system software and application programmes.

(ii) a Lexidata colour raster graphics display of 512 x 512 pixels with 12 bit planes (10 are used for the data display, the remaining 2 for graphics overlays).

(iii) two 9-track tape drives for archiving data.

(iv) a line printer with plotting capability.

(v) system and user VDU consoles.

(vi) a 'mimic' display. This is an RGO-designed facility which shows schematically on a TV display, the current state of the mechanisms within each of the instruments in use (e.g. the various shutters, mirrors, filters etc.), and the light path through the system in this configuration. Relevant information, for example, slit width, dekker mask position, filter number etc., is also given.

The computer runs Fortran software in conjunction with Perkin Elmer's OS-32 operating system. All instrument control and data acquisition are carried out using ADAM (Astronomical Data Acquisition Monitor), a software environment developed at the RGO. The approach has been to write the individual programmes which control the hardware and handle data in such a way that ADAM can tell them what they are to do, give them the data necessary to perform the required operations, and interrogate them for information. A powerful feature of ADAM is the facility for setting-up procedures to perform sequential tasks in a way not too dissimilar to the programming structure of Forth. Standard procedures, generally involving complex series of operations, are available within the basic system, but the user may also enter additional procedures to satisfy specific requirements of the observing. While it is still possible to run the individual programmes independently, under most circumstances the use of ADAM procedures simplifies the operation of the instrumentation and thereby helps the user to make the most efficient use of the available observing time and to concentrate on the astronomical programme in hand.

To integrate FOS' electronics into the instrumentation control system, it was necessary to write Fortran device handlers which would operate within the ADAM environment (Martin, 1980). Thus, the software written to control the CCD camera on the laboratory LSI-11/23 computer system had to be modified to run on the Perkin Elmer machine in conjunction with ADAM. Procedures also had to be written for communication with the local microprocessor controller. A mimic display specific to FOS was not however developed which meant that the standard display for the Acquisition and Guidance (A&G) unit and Intermediate Dispersion Spectrograph (IDS) had to be used during commissioning, bearing in mind that only some of the information was relevant.

Using FOS necessitates that the software is initialized, ADAM is started, and the option of using FOS is selected on the observer's console. Thereafter, the user has access to an extensive catalogue of commands for controlling the instrumentation, obtaining status information from it, and examining previously acquired data. These have been described in detail in the FOS user manual (Breare et al., 1985); but briefly, they include commands for:

(i) controlling the mechanisms within the A&G unit and IDS (e.g. mirrors, filter slides, slit width, dekker mask position, calibration lamps).

(ii) controlling FOS' Motor Mike focus adjustment mechanisms and Hartmann shutters, and monitoring their status.

(iii) taking a CCD exposure of the required duration. When the exposure is finished, the CCD is automatically read out, the data displayed on the Lexidata, and during routine observing stored in a disc file.

(iv) changing the display options on the Lexidata (e.g. changing look-up tables to display the data in such a way as to highlight either the most significant or least significant details of the data), zoom and pan control.

(v) drawing a plot through an image and calculating the FWHM of a feature.

(vi) arithmetic operations on an image and between a pair of image files.

(vii) simple photometry functions such as calculating the mean and standard deviation of data within a pixel matrix, selected with the aid of a cursor.

(viii) on-line data reduction of FOS data (to be described later).

7.4 Optical Alignment and Focussing

Having assembled FOS in the instrument test room, connected the CCD camera electronics into the INT's computer data acquisition system, and established that the camera was working satisfactorily, the initial alignment of the optics was undertaken following a procedure devised during laboratory testing at the RGO (Lowne, 1984). The procedure and the ways in which the necessary tests were performed are described below:

(i) folding-flat mirror adjustment

In order to ease the overall manufacturing tolerances, FOS' folding-flat mirror was designed to allow a small manual adjustment of its tilt so as to ensure that the beam from the slit could be made to fall centrally upon the camera grating. Setting the mirror to the correct position was necessary before any further progress could be made with alignment of the camera optics.

The alignment was established with the aid of a purpose-built 'dummy' slit assembly (illustrated in Figure 7.2) comprising a tube with an

OPTICAL ALIGNMENT - FOS ON ITS HANDLING TROLLEY

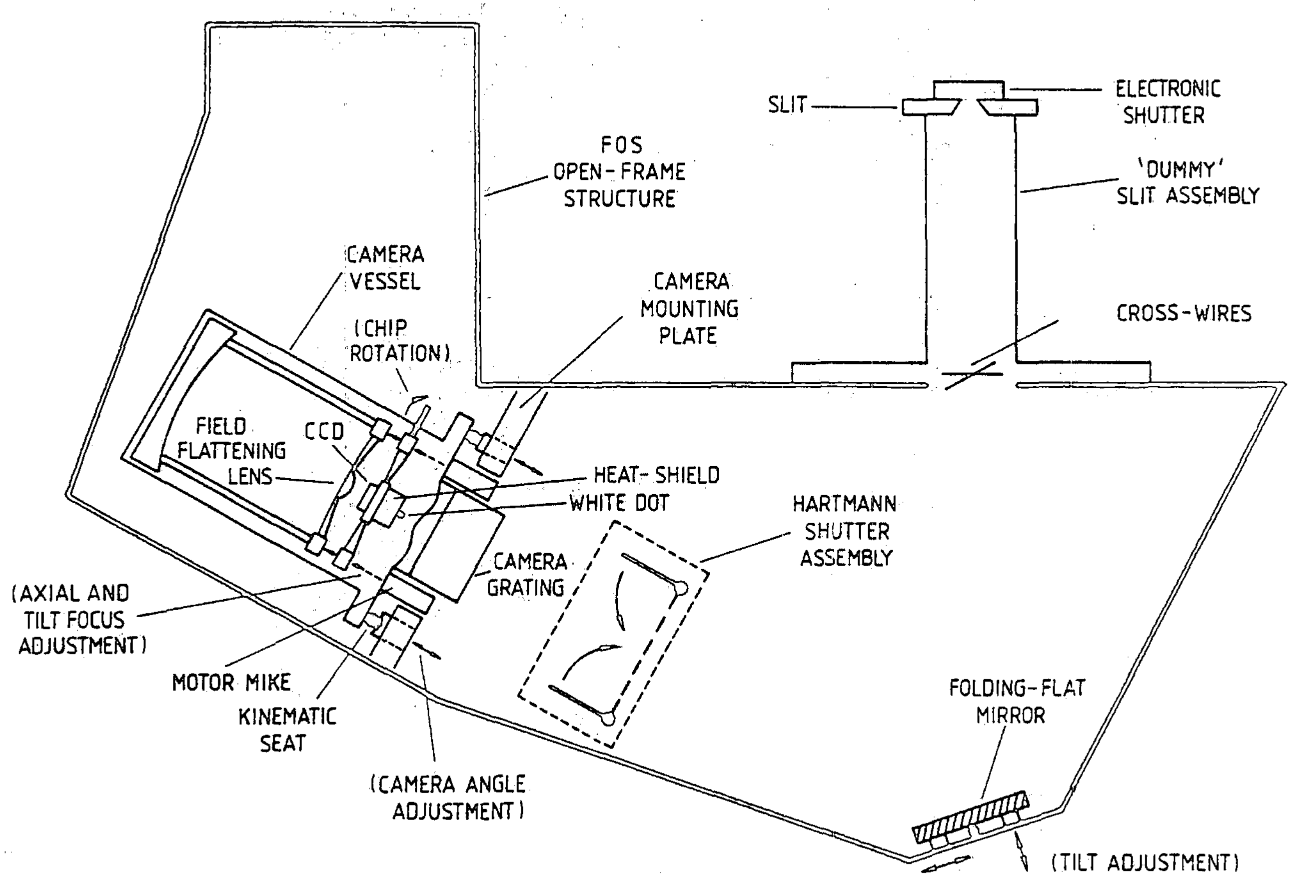


Figure 7.2

adjustable slit mechanism and an electronic shutter fitted at the top, and centrally positioned cross-wires at the bottom. This was designed so that when bolted onto the FOS structure, the slit would be located in the same position as that of the IDS slit when FOS was later installed on the telescope.

The Hartmann shutter assembly was temporarily removed and the front of the camera strongly illuminated with a 60 W bulb. A white dot had been painted in the centre of the heat-shield assembly, located behind the CCD chip's support block (see Chapter 6, Figure 6.5), and this was used to trace the optical axis back to the slit. The brightest image of the dot as seen through the aperture at the slit is its first order image as dispersed by the grating. The folding-flat was then adjusted until the red end of the dot's image was seen through the slit to intersect the cross-wires, in which position the mirror is correctly aligned.

The Hartmann shutter assembly was then refitted. All subsequent alignment required that CCD test exposures were taken.

(ii) camera angle adjustment

Having set the folding-flat to the position specified by the optical design, the next task was to ensure that the camera was set at the correct angle to the beam by observing the position of a spectrum on the CCD. FOS was designed so that a line at 800 nm would image in first order in row 160, column 289 of the CCD as illustrated in Figure 7.3.

The camera vessel was designed with screw-adjustable kinematic seats spacing it off a mounting plate fixed within FOS' open-frame structure (Figure 7.2), enabling its angle with respect to the beam to be altered by rotating the screws within these kinematic seats. To set the angle, a portable copper-argon (CuAr) source was placed above the slit assembly, and a short CCD exposure was taken. Using the cursor facility on the Lexidata, the position of the 801 nm line within the CuAr spectrum was identified, this being sufficiently close to the specified 800 nm wavelength that it can be used to establish the alignment in pixel (160, 289) without making any significant difference to the image quality. The camera angle was then adjusted until the line was

POSITION OF THE CCD IN RELATION TO THE MOTOR MIKE / LVDT FOCUS ADJUSTMENT MECHANISMS (NOT TO SCALE)

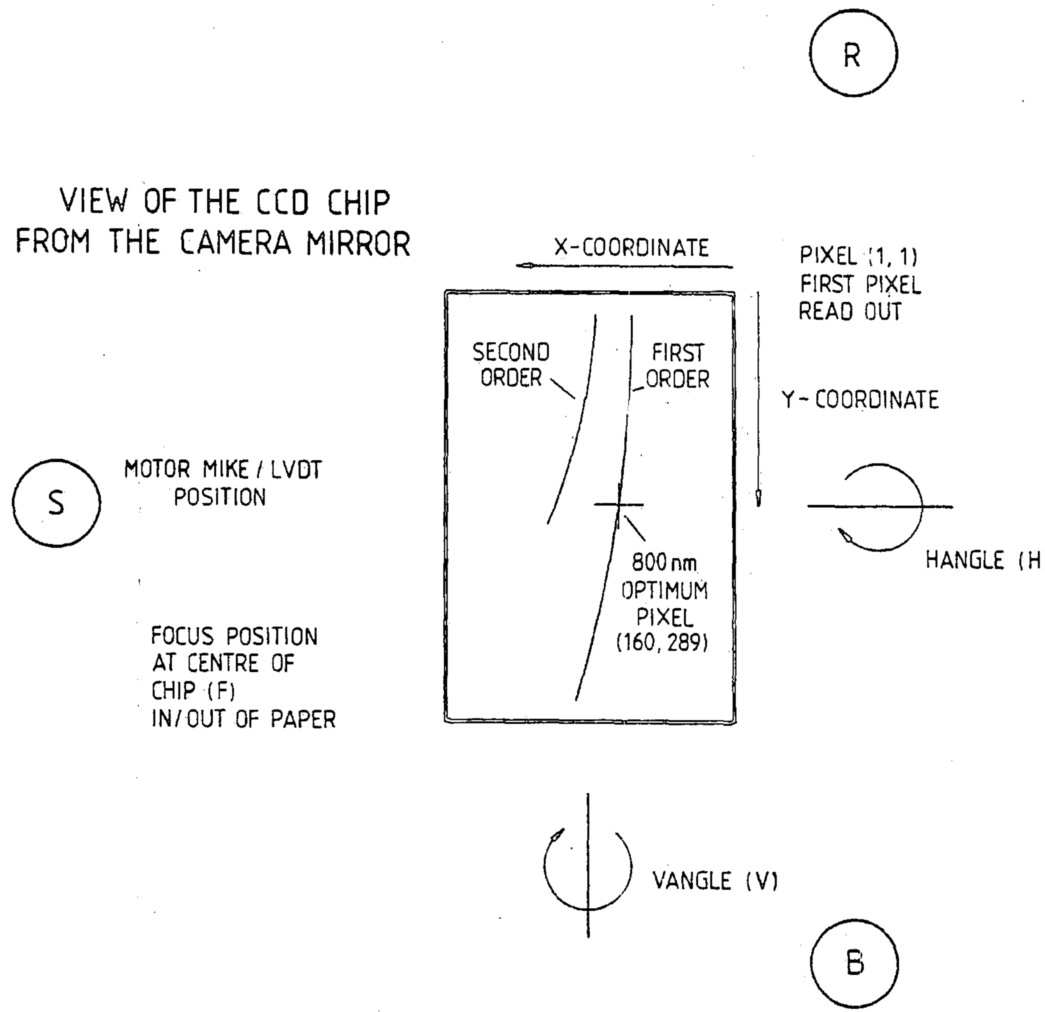


Figure 7.3

eventually made to image in pixel (154, 301), this being the nearest that could be achieved due to the rather coarse adjustment on the kinematic seats, but still within the tolerances specified by the optical design.

(iii) detector rotation adjustment

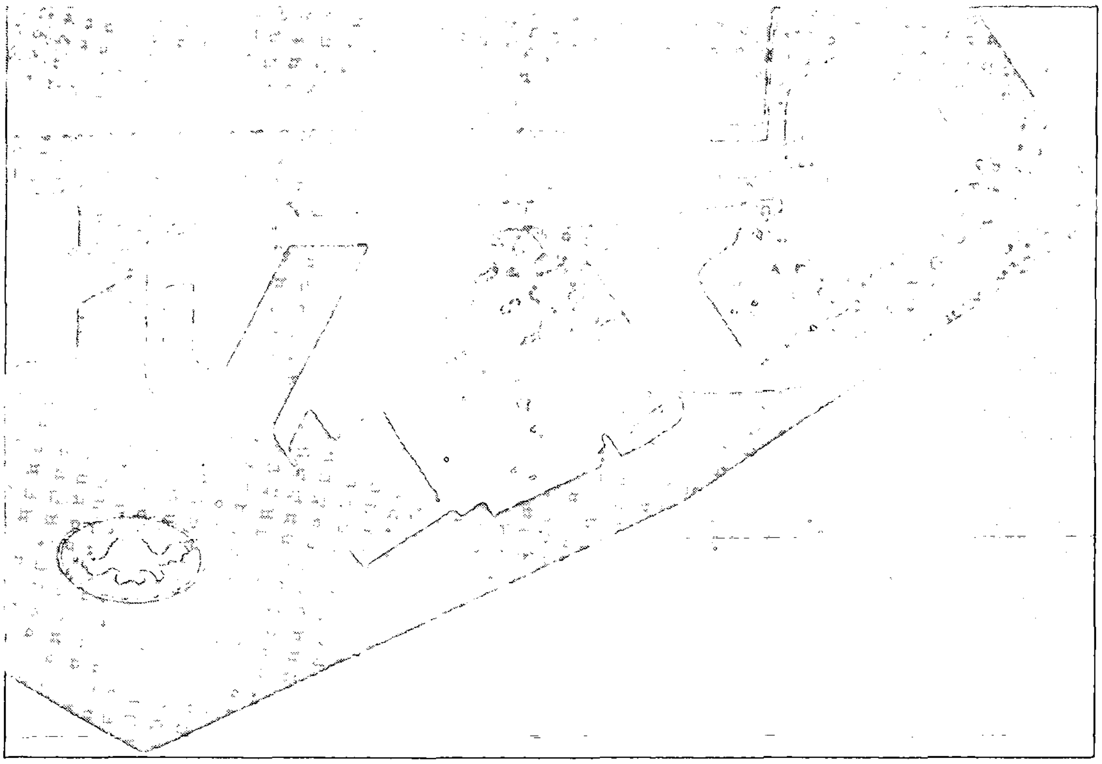
Here the objective was to align the CCD chip with the camera grating by rotating the CCD so as to align the columns of the chip to be parallel with the grating dispersion. To achieve this, the camera was designed so that the innermost part of the annular ring supporting the chip in the centre of the beam could be rotated through small angles by a linkage passing through the camera vessel's wall to an external manual micrometer. The CuAr source was exchanged for a mercury (Hg) source and the position of the 546 nm line within the Hg spectrum, appearing in first and second orders at opposing ends of the chip, was examined. The chip's rotation was then adjusted until the 546 nm line was observed to fall in the same CCD column (column 184).

FOS was now fitted to the telescope. Photographs showing FOS mounted beneath the IDS and the A&G unit are reproduced in Figure 7.4. Having also installed the electronics on the telescope and checked that the system was still working as expected, the remaining optical alignment and focussing of the CCD detector was carried out. The procedure was as follows:

(i) realignment of the folding-flat mirror

With FOS mounted beneath the IDS, the first task was to readjust the folding-flat mirror so as to correct for the small difference between the positions of the dummy slit and the IDS' slit, and thus ensure that the beam from the IDS' slit was projected centrally upon the camera grating. The alignment was examined by taking 10 second test exposures of the CuAr source within the A&G unit, with a narrow (50 μm) slit, a short dekker, and a neutral density filter above the slit. The folding-flat was then adjusted until the 801 nm line was made to image in pixel (165, 286), the nearest that could be achieved owing to the coarse tilt adjustment on the mirror, but again within the tolerances specified by

FOS ON THE INT



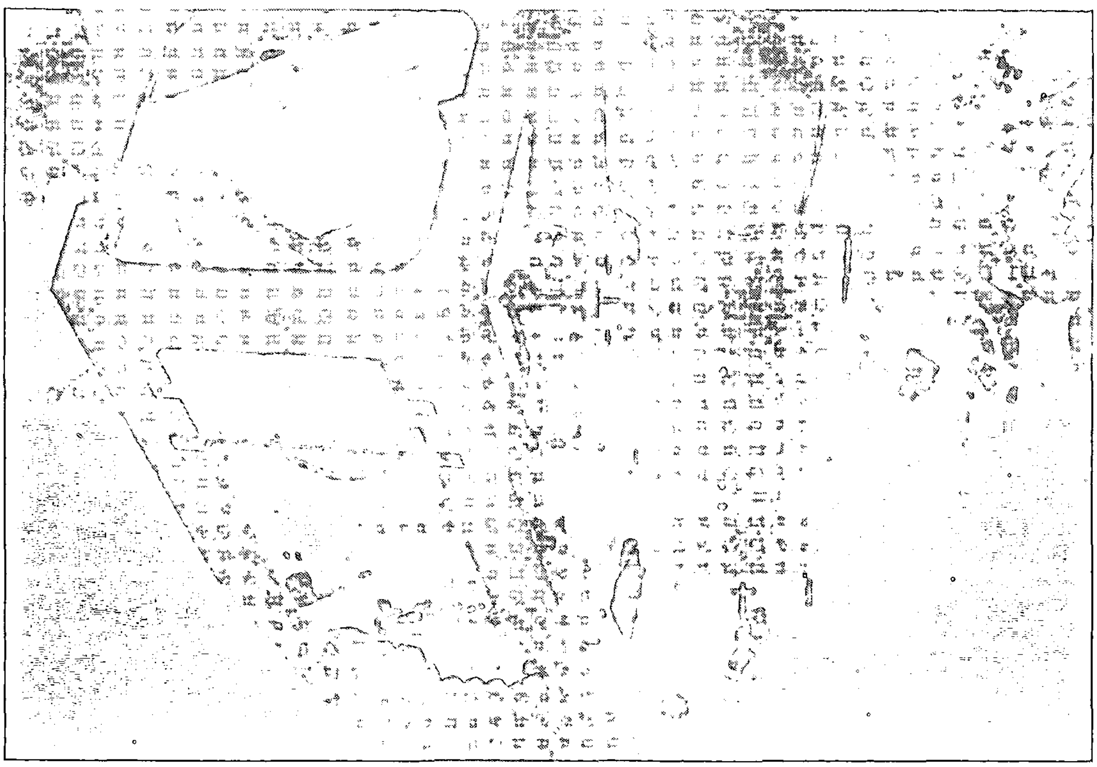


Figure 7.4

the optical design.

(ii) camera rotation

Here the objective was to align the camera grating with the slit by rotating the camera body in its mounting plate so as to align the image of the slit to be parallel with the CCD rows. This was done by taking an exposure of the CuAr source, with a long slit and a short dekker inserted, and examining the position on the CCD of the 826 nm line at either end of the slit image. To obtain a precise measure of its position, a programme called SLICE was used to obtain a profile through the line in the direction of dispersion, and to calculate the centroid of the line position by two methods:

(i) by obtaining a gaussian fit

(ii) by producing a weighted mean position of the centre of the line

In practice, the two methods were found to yield slightly different results, by as much as 0.1 pixels in some cases, but with similar variations overall. The weighted mean method was arbitrarily chosen for obtaining the measurements reported below. After some adjustment of the camera orientation, centroids for the position of the 826 line at either end of the slit of 263.126 and 263.083 were obtained, the alignment thus differing by only 0.043 pixels along the length of the slit.

(iii) axial focus adjustment

Figure 7.3 illustrates the position of the three Motor Mikes with respect to the CCD chip. For convenience, these were labelled as S (slit), R (red) and B (blue). The status information provided by the LVDT encoders is given as a number in the range 0-511 where 1 unit is equivalent to 4 μm. These numbers on their own are not particularly useful and consequently three other parameters were defined to facilitate axial and tilt focus adjustment of the CCD:

F (focus)

- the position at the centre of the CCD of a plane passing through S, R and B, in LVDT units.

H (hangle)

- the tilt in LVDT units in the direction of main dispersion.

V (vangle)

- the tilt in LVDT units in cross-dispersion.

The necessary algorithms to convert the S, R and B numbers into F, H and V values, and vice versa, were written as subroutines within the Perkin Elmer software for communicating with the local microprocessor controller.

Axial focus was optimized with the aid of the CuAr source, a narrow slit, the short dekker and the Hartmann shutters. In order to calculate the focus error, the centroid of the 826 nm line was measured from each half-aperture given by the Hartmann vanes in turn. The Hartmann shift, defined as the difference between the centroids, in pixels (in the sense vane A open - vane B open), enables the focus error (in LVDT units of focus travel) to be determined from:

Focus error = Hartmann shift x Hartmann ratio

The Hartmann ratio had been previously measured during laboratory testing at the RGO and found to have a value of -15 (Lowne et al., 1984).

Having found a Hartmann shift of 0.4 pixels, and thus a focus error of -6, the Motor Mikes were given commands to move by equal amounts so as to increase the F value by 6 LVDT units. In this new position, with focus position parameters of F = 293, H = 24 and V = 0, the difference in the centroids was found to be -0.003 pixels, giving a focus error of only 0.045 LVDT units.

(iv) tilt adjustment of the CCD in cross-dispersion

In order to optimize the tilt of the CCD in cross-dispersion, the long slit was installed, and the Hartmann shift of the 826 nm line was measured at either end of the slit image. In the optimum position, the Hartmann shift should be the same along the length of the line.

The procedure of measuring the Hartmann shifts and making appropriate adjustments to the tilt of the chip was repeated iteratively until shifts of -0.091 and 0.332 pixels were obtained with a tilt setting of V = 10. Although not equal in value, this position was found to give the minimum difference in Hartmann shift between the two ends of the line and was therefore taken as the best focus position likely to be achieved.

(v) tilt adjustment in main dispersion

The final focus adjustment was to find the optimal tilt position of the CCD in the direction of main dispersion. This was done using the Hg source within the A&G unit and by measuring the Hartmann shifts of the 546 nm line in the two orders. An incorrect setting of the tilt should yield Hartmann shifts which are equal in magnitude but of opposite polarity. However, with the chip initially set with a tilt value of V = 24, the shifts were found to be 0.163 and 0.088 pixels, both therefore positive in value. In order to explain this, it was calculated that the surface of the chip was bowed to the extent of ± 10 μm. Several attempts were made to improve the focus, but it was eventually concluded that the original tilt setting with V = 24 was the best position likely to be achieved.

(vi) final checks

Having established a satisfactory focus of the detector, for which the focus position parameters were S = 273, R = 328, B = 280, F = 293, H = 24 and V = 10, a final assessment of the focus was made by measuring FWHMs for several lines within the CuAr spectrum, both on and off axis. The results were in the range 1.2-1.6 pixels, largely depending upon whether a line fell centrally on a pixel or across two pixels, and in accord with the results obtained during laboratory testing at the RGO.

The completion of the optical alignment preceded the first night of FOS' week of allocated observing time by a matter of only a few hours. During the course of the first night, it was discovered that when operating in one of the beam-switching modes (with two slots, each of 25 arcsec width, and separated by 85 arcsec), the image from one aperture fell on a dead column chip defect. Since it was felt that beam-switching would prove to be a useful technique for simplifying sky subtraction, it was decided to readjust the folding-flat mirror so as to move the spectrum laterally across the chip in cross-dispersion to a position away from the defect. This was done the following morning, when it was found necessary to move the spectrum towards second order by 60 pixels, with the 801 nm line of the CuAr spectrum now appearing in pixel (220, 287) compared to the optimum position of (160, 289). In this position, chip defects were avoided in all but the long slit mode. The displacement was found to have introduced a small amount of vignetting at the ends of long slit images, but not to have had any serious effect on the focus or image resolution.

No further adjustments to the optical alignment proved to be necessary during the remaining week of commissioning. Over this period, for which there was no significant change in the ambient temperature inside the observing dome, the focus position defined by the LVDTs was found to be stable to ± 1 units. It is important to note, however, that the LVDTs were never intended to be treated as absolute position encoders and that their readings may be expected to vary with the ambient temperature of the camera body by approximately 0.6 LVDT units/^{o}C, owing to the thermal expansion of the nylon screws supporting the LVDT cores within their coil windings. This of course does not indicate a change of focus and in fact over the 6 months following the commissioning run, during which FOS was removed and refitted to the IDS several times, the focus was reproduced to within measurement errors without any re-focussing being necessary. The fact that the LVDTs cannot be relied upon as long-term indicators of the focus, means that the only way to be sure that the camera is aligned correctly is to measure FWHMs for several lines from an arc source and compare the results with previously obtained values, summarized for reference in the FOS user manual (Breare et al., 1985).

7.5 Operation

Setting up FOS for an observing run necessitates:

(i) configuring the IDS and FOS for FOS operation which involves:
- removing the folding prism within the IDS through an access

port so that the beam is allowed to enter FOS through a hole in the bottom of the IDS.

- inserting a light-tight tube between the IDS and FOS.
- replacing the dekker and both of the below slit filter slides within the IDS with those specifically for FOS.

(ii) vacuum pumping the camera-cryostat assembly (to $\sim 10^{-5}$ torr) and cooling the CCD to 150 K. This can take up to 12 hours and so must obviously be done well in advance of observing.

(iii) making appropriate cable changes between the IDS′ CCD and the FOS CCD data acquisition system (the IDS and FOS share the same cabling between Cassegrain and the CLIP centre) and, of course, switching on the electronics.

These tasks, however, are all duties of the LPO support staff. FOS has no moving parts which the observer is required to adjust. There are, however, several checks that users can make to reassure themselves that the system is working as it should:

(i) the most exhaustive test is to initialize the FOS software and take a CCD exposure of an arc source. This tests the entire CCD electronics, A&G, IDS and FOS computer instrument control and data acquisition hardware, and of course the control software.

(ii) a second useful exercise is to check the focus of the CCD. The focus has proved to be very stable, however, since it was first set during commissioning, and so users are strongly discouraged from attempting to alter it.

Having established that the system is working as expected, the only decision to make is which mode of operation to adopt. There are four possible modes of operation, selected by setting up one of the following dekker mask and field-lens/filter configurations:

Mode A: two 5, 2 or 1.2 arcsec slots (12 arcsec centre to centre spacing) intended for beam-switching observations of point sources in both first and second orders. Each observation requires a pair of exposures (I & II) with the object positioned firstly in the left-hand aperture (L), and secondly in the right-hand aperture (R). A 2-D sky-subtracted frame can then be obtained from (L-R)I + (R-L)II.

Mode B: two 25 arcsec slots (85 arcsec centre to centre spacing) intended for beam-switching observations of extended objects in both first and second orders. A clear field-lens is required beneath the slit assembly to avoid vignetting along the slit direction.

Mode C: a 200 arcsec long slot for observing very extended or multiple objects in first order only. A GG495 field-lens is required to filter out the second order and to avoid vignetting along the slit.

Mode D: a centralized 25 arcsec slot for single object work in first and second orders.

The format of the data taken in these modes is illustrated in Figure 7.5. The choice of which mode to adopt depends, of course, on the object(s) being investigated and the user's own personal preferences.

Observing with FOS is simply a matter of setting up the required mode of operation and running the system by entering the appropriate commands at the control console. The most important is the RUN command which prompts for an object name descriptor, assigns a run number, clears the CCD, opens the IDS shutter for the required exposure period, and finally reads out the data from the CCD to a disc file. Images are automatically displayed on the Lexidata. The FOS on-line data reduction package may then be used to assess the data while a new exposure is started.

7.6 Data Reduction

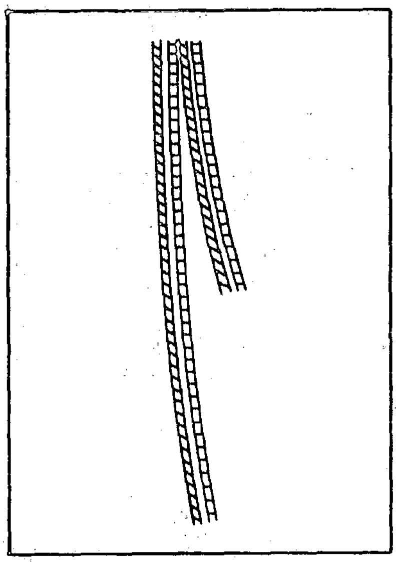
FOS' fixed-format design has allowed the development of an on-line data reduction package which aims to provide:

FOS OPERATING MODES

(FORMAT OF THE DATA AS SEEN ON THE LEXIDATA DISPLAY)

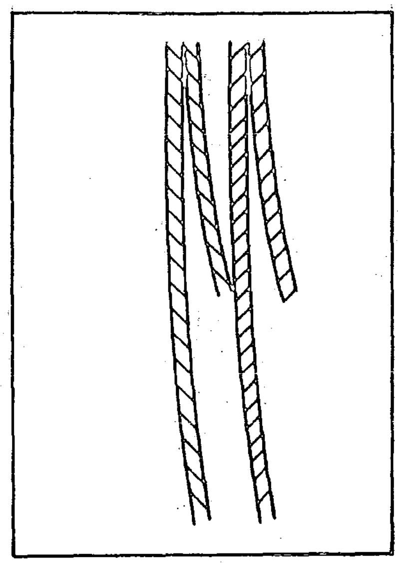
MODE A

- two 1·2," 2" or 5" slots, 12·5" apart.
- both orders



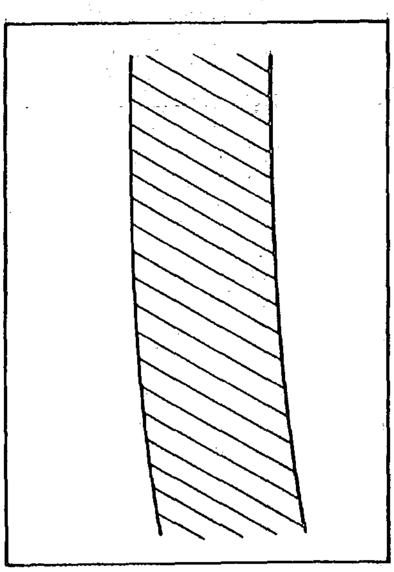
MODE B

- two 25" slots, 85" apart
- clear field lens
- both orders



MODE C

- 200" slot
- yellow field lens
- first order only



MODE D

- 25" slot
- clear field lens
- both orders

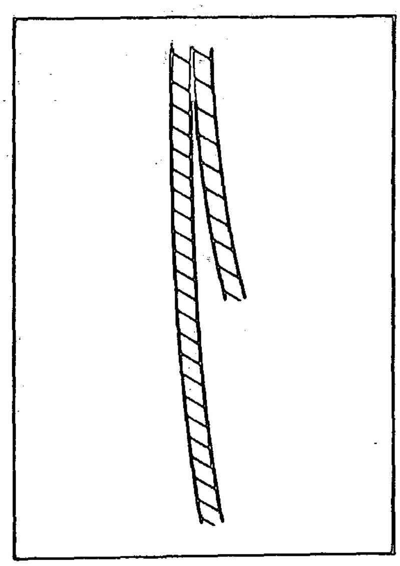


Figure 7.5

(i) fully reduced and calibrated spectra a matter of a few minutes after the data has been collected, thus enabling the astronomer to assess the data in tandem with further observing.

(ii) limited facilities for interactive classification and redshift determination for extragalactic objects.

The package has already been described in detail by Parry (1986) and in the FOS user manual (Breare et al., 1985). Here, therefore, only a very brief outline of its capabilities will be given.

Table 7.1 summarizes the various modules within the data reduction package together with an indication of their functions. Those of most importance are the spectrum extraction and sky subtraction programmes. Taking each stage of the reduction in turn:

(i) CCD column defect removal

The programme ZAPCOLS allows the user to remove CCD column defects by prompting for the first and last columns defining an area to be cleaned by interpolation. Routine defect removal is unnecessary, however, because the sky subtraction programmes reject anomalous pixels in the sky spectrum, and with the CCD chip currently installed in FOS, the object signal can only land on a column defect when operating in the long slit mode. The observer is expected to take the necessary precautions to avoid this.

(ii) cosmic ray removal

If two similar exposures are taken so that two frames of data are available for comparison, cosmic ray events may be removed from the data using a programme NITPICK. This compares the two frames, identifies deviating features above a specified significance level (usually 4 sigma) in one, and replaces these pixels with the corresponding ones in the other frame. Photon noise is automatically allowed for using known characteristics of the CCD. This routine is only necessary if the object signal is affected as the sky subtraction software automatically applies a similar procedure across sky columns.

(iii) flat-fielding

A flat-field correction can be applied using a programme DOFF which divides the raw data image by either a standard flat-field image file held on disc, or one generated by the user by taking several exposures of a tungsten source and combining them to produce a low shot noise average.

(iv) spectrum extraction and sky subtraction

Each spectral order has a curvature which results primarily from the cross-dispersion introduced by the FOS optics but also atmospheric dispersion when the slit is close to the parallactic axis. This curvature can be mapped at any zenith distance (z.d) using a programme FOSCOFFS which is used to fit a high order polynomial to an observation of a bright point source. The polynomial coefficients are stored in named reference files. A set of default files (obtained from low z.d observations of numerous stars of extreme colours) are available which suffice in most circumstances. For observations at large z.d, however, it is recommended that an observation of a bright star is obtained and FOSCOFFS is used to generate a new set of coefficients. In this case, it is necessary to use ZAPCOLS to remove a hot column defect present on the current chip as this confuses the software when searching for the spectrum.

There are two procedures available for extracting the object and sky signals: EXTRIC and TRIM + LEXEXT. Both use the curvature files to define curved object and sky windows from which a straightened sky-subtracted spectrum is obtained.

EXTRIC is a batch version designed specifically for rapid assessment of unresolved objects obtained while operating in mode D. The programme automatically scans the CCD frame along the slit direction with a 20 pixel (25 arcsec) wide curved window until it locates the position for which the integrated signal within the window is a maximum (i.e. the dekker area containing the overall sky signal and the object signal within it). A narrower window of user-defined width is then scanned through the dekker area until the object signal is located. The data are then extracted and sky-subtracted, using an interpolative sky subtraction to allow for non-uniform sky illumination along the slit.

EXTRIC has been found to be satisfactory for objects which are less than 4 arcsec across (including faint galaxies) and centred within the middle two thirds of the mode D dekker. For more demanding cases (e.g. for extended objects or when observing several objects along the slit), the programmes TRIM and LEXEXT enable the object and sky apertures to be selected interactively on the Lexidata display using the cursor. Here the user first straightens the spectrum using TRIM which prompts for the width of the spectrum (sky and object) in the slit direction and reconfigures the pixels according to the curvature coefficients. The object and sky windows are then defined using LEXEXT which prompts for appropriate cursor positions.

The resulting spectra from either TRIM and LEXEXT or EXTRIC are of a standard form: a spectrum pair containing the sky-subtracted object signal and the adopted sky spectrum. The wavelength to pixel number calibration is linear and so it is not necessary to resample the data.

(v) flux calibration, atmospheric absorption correction and redshift estimation

The remaining data reduction programmes are those for flux calibration of the data (using a standard flux calibration spectrum) and correction for atmospheric absorption using a sky-subtracted spectrum of a standard featureless star. A programme is also available which takes commonly seen features in particular types of object and redshifts them for comparison with the observer's data.

(vi) spectrum plotting

Wavelength calibrated spectra may be plotted graphically on the Lexidata display. The cursor may be used to determine the wavelength of spectral features of particular interest, and comments can be annotated on the screen. Hard copy plots from the Lexidata may also be obtained.

Table 7.1 FOS DATA REDUCTION PACKAGE

ZAPCOLS	-	CCD column defect removal
NITPICK	-	cosmic ray removal
DOFF	-	applies a flat-field correction
EXTRIC	-	spectrum extraction and sky subtraction (batch version for mode D only)
or		
TRIM + LEXEXT	-	spectrum extraction and sky subtraction (interactive in conjunction with the Lexidata display)
ATABS	-	flux calibration and atmospheric absorption correction
FOSPLOT	-	interactive spectrum plotting on the Lexidata display
LEXPLOT	-	hard copy dump of FOSPLOT
ZED	-	redshift estimation

7.7 Commissioning on the Telescope

FOS was first commissioned over 5 nights between the 18th and 22nd July 1984. The objectives of this run were principally:

(i) to determine the instrumental performance of FOS.

(ii) to refine the on-line data reduction software and determine how to make the best use of it.

(iii) to compile a catalogue of observations of different types of objects. The aim was to determine the types of faint objects most appropriate for investigation with FOS, and the S/N attainable for these objects as a function of magnitude.

7.7.1 Instrumental Performance

FOS' instrumental performance i.e. its measured efficiency and spectral resolution has already been reported (Breare et al., 1985, Breare et al., 1986a) but a brief summary will be given here for reasons of completeness.

(i) throughput

The efficiency of the FOS system (i.e. the throughput after losses in the atmosphere, telescope, FOS optics and the GEC CCD) was determined from observations of standard stars (Parry, 1986), and is shown for both orders in Figure 7.6. The peak efficiency is 12% in first order at 700 nm with the telescope at a z.d = 27 degrees. In second order, however, the peak efficiency is only 1.3% at 500 nm, due mainly to the poor blue response of the GEC CCD.

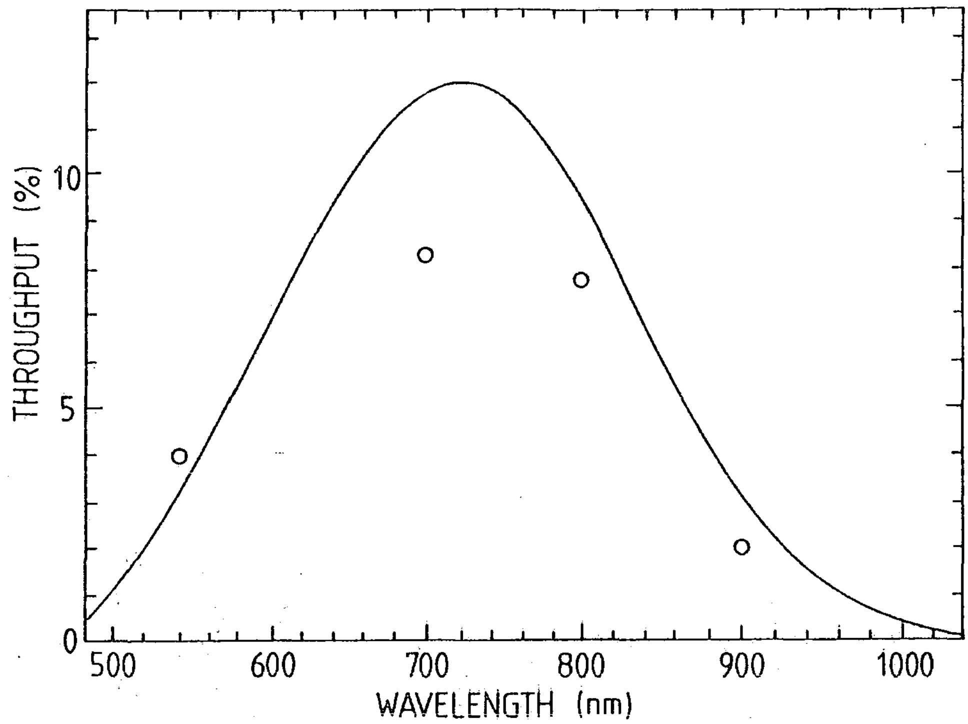
It is interesting to compare these figures with the original estimates made in 1980 (see Chapter 2, Table 2.1). For comparison, the predicted figures are also included in Figure 7.6. Although the relative variation of throughput with wavelength is in reasonable agreement, the peak efficiency is somewhat better than expected, 12% at 700 nm in first order compared to the original estimate of 8.2%. There are two main reasons for this discrepancy.

(i) the FOS optics are in fact more efficient than expected. The original estimates did not fully account for the reflectivity and transmission obtainable from the various optical surfaces with the use of coatings (Powell, 1986). The efficiency of the grating was measured in the laboratory at RGO, and from this, the peak throughput of the optics (with revised estimates for the efficiency of the optical surfaces) has been determined to be 70% at 700 nm (Lowne, 1983) compared to an anticipated efficiency of 45%.

(ii) the peak QE of the GEC P8603 has proved to be better than expected (~ 40% at 700 nm rather than the expected 31%).

FOS THROUGHPUT IN FIRST ORDER

(FOS + INT + ATMOSPHERE, ZD = 27·6)



FOS THROUGHPUT IN SECOND ORDER

(FOS + INT + ATMOSPHERE, ZD = 3)

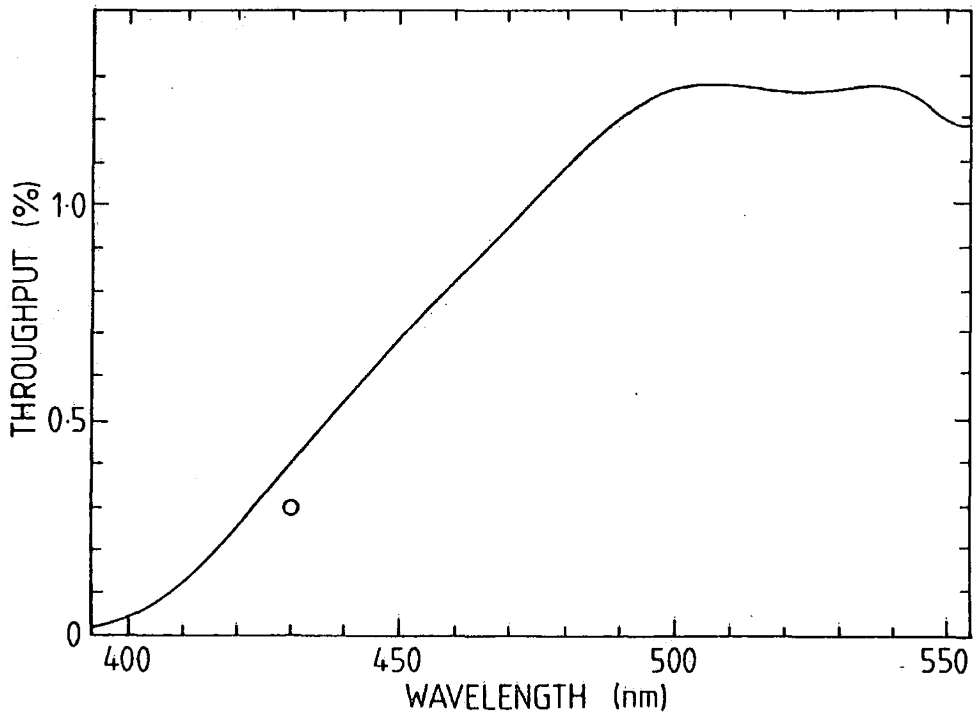


Figure 7.6

Taking these figures with the original estimates of the throughput of the atmosphere and the telescope, one can derive a new estimate for the efficiency of 16% (at 700 nm) which is now greater than that actually measured. This can be attributed to the fact that the original estimate for the efficiency of the telescope was rather optimistic with regard to the reflectivities of the primary and secondary mirrors. A more realistic estimate for the INT's throughput is ~ 0.57 rather than the original figure of 0.67 (Powell, 1986). Substituting the revised estimate for the INT's efficiency yields a new estimate for the efficiency of the FOS system of 13.5% (at 700 nm), which, given the cumulative uncertainties in each part of the system, is now in good agreement with the measured figure.

(ii) spectral resolution

The optical resolution seen with a narrow (~ 0.25 arcsec) slit is 1.2 pixels FWHM (12.8 Å in first order), independent of wavelength, and does not degrade significantly across a 4 arcmin slit. Under normal operating conditions (1 to 2 arcsec slit), however, the resolution is 15-20 Å FWHM in first order and 8-10 Å FWHM in second order, depending on how features are sampled by the pixels. FOS is slightly undersampled for its resolution at 10.7 Å/pixel in first order. These results need to be compared with what one would expect of the system.

FOS' spectral resolution is dependent upon:

(i) the slit width as projected onto the detector (a 1 arcsec slit is equivalent to 17.6 μm on the CCD).

(ii) the image spread at the detector arising from aberrations in the optics. The design was optimized such that for a point source in the centre of the slit, the image spread at the detector should be less than 20 μm in the direction of dispersion at all wavelengths. This was confirmed experimentally during laboratory tests at the RGO when the image spread was found to be between 10 and 20 μm depending on wavelength.

(iii) the sampling by the GEC CCD's 22 μm wide pixels.

The cumulative effect of these factors (i.e. a positional uncertainty interpreted as a cumulative image spread) may be estimated by their addition in quadrature (Worswick, 1986). Three cases are considered.

(i) 0.25 arcsec slit

With a narrow slit (0.25 arcsec is equivalent to 4.4 μm on the detector) the resolution is dominated by the optics and the sampling by the pixels. Assuming that the image spread due to aberrations is in the range 10–20 μm, an estimate for the cumulative image spread is 1.1 to 1.3 pixels (11.8–13.9 Å).

(ii) 1 arcsec slit

The image spread due to the slit is closely matched to the size of a CCD pixel. Assuming again that the image spread due to aberrations is in the range 10–20 μm, then the estimate for the cumulative image spread is 1.4 to 1.6 pixels (15.0–17.1 Å).

(iii) 2 arcsec slit

The resolution is now dominated by the slit width (2 arcsec is equivalent to 35.2 μm on the detector). The estimate for the cumulative image spread is 1.9 to 2.0 pixels (20.3–21.4 Å).

Relating the figures for the estimated image spreads to ones of FWHMs is not straightforward because of the way in which images are sampled by the CCD pixels. The pixels are not discrete sampling points and so the results can be expected to differ from what one might first expect from Nyquist sampling (i.e. FWHM = 2 pixels). A comparison between the estimated image spreads and the measured FWHMs does however allow the following points to be made.

(i) the optical resolution (i.e. that with a narrow slit) is in good agreement with that expected.

(ii) the overall variation of resolution with slit width, and the actual resolution for a given slit width, is consistent with that expected of the system.

7.7.2 Data Reduction Software Development

The data reduction software was initially developed on the Durham Starlink VAX 11/750 (Parry, 1986). Converting the code to run on a Perkin Elmer computer required much effort for the following reasons:

(i) the VAX and Perkin Elmer machines handle bulk data (in this case CCD image files) in different ways.

(ii) the Durham VAX is equipped with an ARGS display system whereas the LPO Perkin Elmer uses a Lexidata which requires different driver software.

(iii) the Perkin Elmer does not provide any general purpose mathematical subroutine libraries (as available on the VAX) which meant that the curve fitting routines to extract the spectra had to be written specially for the Perkin Elmer machine.

Some of this work was undertaken during several visits to the RGO while FOS was still being constructed. However, the bulk of the work had to be done during commissioning on La Palma because a Lexidata was not available on the Perkin Elmer at the RGO. This work was the responsibility of I R Parry, A Purvis and R S Ellis.

Experience gained through observing and obtaining real astronomical data proved useful in highlighting those areas of the reduction package to benefit from some development and refinement of the software. For example, the facilities for wavelength calibrating a spectrum plotted on the Lexidata, and identifying the wavelength of features of interest with the cursor, were developed in this way as their importance for speeding up the on-line analysis of the data became apparent. It was found that the ability to do immediate wavelength calibrations of features seen in faint object spectra facilitated line identification and thereby helped in determining their redshift.

The software was developed further and debugged during commissioning runs in December 1984 and May 1985, after which the package was released to the La Palma software team for common-user support.

7.7.3 Observations

FOS' first commissioning run on the INT was used extensively to investigate its instrumental performance and the nature of spectra obtained from a wide diversity of objects, rather than to embark on any one individual programme of research. To this end, the commissioning period was used:

(i) to observe standards from which the throughput could be determined.

(ii) to compile a catalogue of spectra, both stellar and extragalactic, for classification purposes and comparison with future observations.

Bright objects yielding high S/N were attempted first in order to investigate the nature of features sampled at low resolution, and the ease of line identification. Fainter objects, more demanding of good sky subtraction, were then attempted, the aim being to determine the S/N, and hence the integration time for a given magnitude, necessary to enable classification and/or redshift determination for different types of objects. During the course of commissioning, observations were made in each of FOS' different operating modes (i.e. slit type) in order to assess how to make best use of the instrument.

In an attempt to catagorize the types of objects investigated during commissioning, a few examples from the observing log are given below.

(i) calibration standards

Several standard stars were observed in order that FOS' throughput could be determined. Amongst these were:

VMa 2
Wolf 1346
LDS 749B
GD 140
GD 190

(ii) classification work

FOS' wide spectral coverage makes it ideally suited for classification work, both stellar and extragalactic.

(i) stellar

(a) spectral classification

Faint stars can be classified from studies of their continuum (i.e. colour), and their atomic and molecular absorption features. A catalogue covering spectral classification type was compiled to provide a basis for comparison with future observations. Examples of those objects studied are listed below together with their spectral type.

NGC 6664 F	B3 IV
NGC 6664 M	B9 V
NGC 6664 A	A0 IV
NGC 6791 15	F2 IV
NGC 6791 20	G0 V
NGC 6791 1	K5 III
Wolf 1040	M5 V

(b) planetary nebulae

The planetary NGC 7027 was observed, its well defined emission line features being a useful check of FOS' wavelength calibration.

(ii) extragalactic

FOS' primary function is to obtain spectra of faint extragalactic sources, both for classification purposes and redshift determination. Normal galaxies and active galactic nuclei (e.g. radio-sources, QSOs, Seyferts) were observed. Examples are given below.

(a) normal galaxies

NGC 5813
Abell 655
0658+49
J1836.10RC

(b) active galactic nuclei (radio-sources, QSOs and Seyferts)

3C390.3
PKS2128-12
4C16.49
3C345
3C380
OQ172
3C454
4C14.27
4C53.24
1012+008

(iii) unidentified objects

FOS is well suited to the investigation of unusual, faint, previously unidentified objects, providing an efficient means of classification and thus allowing the observer to assess whether to pursue follow-up observations. During the course of commissioning, three objects selected by N Reid (RGO) and designated ´funny faint red things´ were observed.

FFRT 16h #21
FFRT 22h #30
FFRT 22h #29

Detailed results from a few selected examples will be presented in Chapter 8.

CHAPTER 8

RESULTS

8.1 Introduction

With the aid of selected examples from the commissioning period, this chapter aims to show the nature of spectra obtained with FOS from a variety of objects. The main objectives are:

(i) to illustrate how FOS' wide wavelength coverage can be used for classification work.

(ii) to show the types of faint extragalactic objects for which a redshift can most easily be obtained.

(iii) to show the limiting magnitudes for which a redshift can be determined for different types of objects in a given exposure time.

(iv) to highlight the problems of reducing and assessing the data from the instrument.

Some new redshift measurements are included, these in particular illustrating the difficulties which can be encountered in reducing and assessing the data from an object whose signal is comparable to that from the sky background.

Finally, spectra of Comet Halley obtained in December 1984 are presented.

8.2 The Observations

Details of the relevant observations are listed in Table 8.1.

Table 8.1 OBSERVATIONS

FIGURE	DATE	OBJECT	VISUAL MAGNITUDE	SEEING (arcsec)	EXPOSURE (seconds)
8.2	5 5 85	GD 140	12.50 (a)	1.2	20
8.3	18 7 84	BL Lac	14.50 (b)	1.1	300
8.4	20 7 84	NGC 6664 F	10.97 (c)	0.8	10
8.5	20 7 84	NGC 6664 A	10.61 (c)	0.8	3
8.6	20 7 84	NGC 6791 15	15.95 (d)	0.8	400
8.7	20 7 84	NGC 6791 20	15.02 (d)	0.8	160
8.8	20 7 84	NGC 6791 1	13.35 (d)	0.8	20
8.9	18 7 84	Wolf 1040	14.5 (e)	1.1	60
8.10	21 7 84	FFRT 22h #29	-	1.1	500
8.11	20 7 84	VB 10	18.9 (f)	0.8	400
8.12	19 7 84	NGC 5813	12.0 (g)	1.2	300
8.13	16 5 85	J1836.10RCa	21 (h)	1.5	3 x 1000
8.14	18 7 84	PKS2128-12	15.98 (i)	1.1	800
8.15	19 7 84	3C380	16.8 (j)	1.1	600
8.16	5 5 85	4C53.24	17.90 (k)	1.2	1000
8.17	22 7 84	3C454	18.47 (j)	0.9	2 x 1000
8.18	27 12 84	4C14.27	19.5 (j)	1.0	2 x 1000
8.19	19 7 84	4C16.49	18.47 (l)	1.2	2 x 1000
8.20	27 12 84	Comet Halley	20 (m)	2.4	5 x 1000

(a) - Oke (1974)
(b) - Hewitt and Burbridge (1980)
(c) - Arp (1958)
(d) - Kinman (1965)
(e) - Woolley et al. (1970)
(f) - Liebert et al. (1978)
(g) - Sulentic and Tifft (1973)
(h) - estimated visual magnitude (INT Cassegrain TV acquisition system)
(i) - Craine (1977)
(j) - Laing et al. (1983)
(k) - Walsh and Carswell (1982)
(l) - Mitton et al. (1977)
(m) - estimated visual magnitude (INT Cassegrain TV acquisition system)

Note - Exposure times shown as n x 1000 seconds indicate that n consecutive exposures of 1000 seconds were taken.

8.3 Data Reduction

Most of the data presented in this chapter were partially reduced on-line at La Palma during observing. At that time, however, the software was still being developed and the practice of fully reducing the data to give hard-copy, wavelength calibrated plots had not become routine. All these data were therefore subsequently reduced on the Durham Starlink VAX 750.

The programmes to reduce the data on the VAX are similar to those used at the telescope but are written to work within the Starlink VAX VMS environment and with the VAX's ARGS display (Parry, 1986).

The procedure used to reduce the data, similar to that described in Chapter 7, is outlined below.

(i) extraction and sky subtraction

The first steps of the reduction procedure are to extract the curved object+sky and sky spectra from the raw 2-D CCD image, and straighten the data by mapping the curvature with a high order polynomial derived from pre-determined coefficients stored in a set of standard curvature files. The sky spectrum is then subtracted from the object+sky data. Two methods were used:

(a) using a programme called EXTRICATE (the VAX equivalent of the programme EXTRIC described in Chapter 7) which automatically searches for the object and sky signals and extracts them. The data are then straightened and sky-subtracted to yield the object spectrum.

(b) using the programmes TRIM and ARGSEXT. This method requires that the user defines the object+sky and sky windows from the ARGS display after which the data are extracted and sky-subtracted.

A typical spectrum of the La Palma night sky (obtained in a 1000 seconds exposure during 'grey time' in May 1985) is shown in Figure 8.1. The spectrum is highly structured, comprising in addition to the continuum, a number of emission lines, and bands of OH emission in the near infrared (Broadfoot and Kendall, 1968).

As will be seen later, it is the degree to which these emission features can be removed from the data that determines the limiting magnitude for faint object spectroscopy with FOS.

(ii) flux calibration and atmospheric absorption correction.

The programme ATABS was used to remove the effect of atmospheric absorption bands from the data and to apply a flux calibration.

The most significant atmospheric absorption features are seen in first order in the wavelength region 6800 to 10000 A; there is no significant atmospheric absorption in second order. The correction for atmospheric absorption is therefore applicable only to first order spectra.

The absorption bands are removed using the (non-fluxed) first order, sky-subtracted spectrum of an otherwise featureless object. The object needs to be featureless only in the wavelength region where the atmospheric absorption features are seen; features found outside this region are ignored. ATABS automatically accounts for the colour dependence of the featureless object's spectrum so that this does not affect the final result (Parry, 1986).

Observations of bright, intrinsically featureless objects, usually white dwarfs, were therefore made at regular intervals during commissioning. Two examples of these (non-fluxed) spectra (GD140, a white dwarf, and BL Lac) in which the various atmospheric absorption lines are identified (Allen, 1973) are shown in Figures 8.2 and 8.3. BL Lac (the prototype of the BL Lacertae class of objects) is an elliptical galaxy with a bright nucleus, known for its featureless continuum.

Flux calibration uses a default calibration file held on the VAX, derived from an observation of a standard star (VMa 2) of known flux distribution.

(iii) spectrum plotting and wavelength calibration.

Wavelength calibrated plots of the spectra were produced using the programme SPECPLOT. This enables the user to select the wavelength range over which the spectrum is to be plotted and to add an object descriptor. A hard-copy plot of the data may then be obtained using a PRINT command.

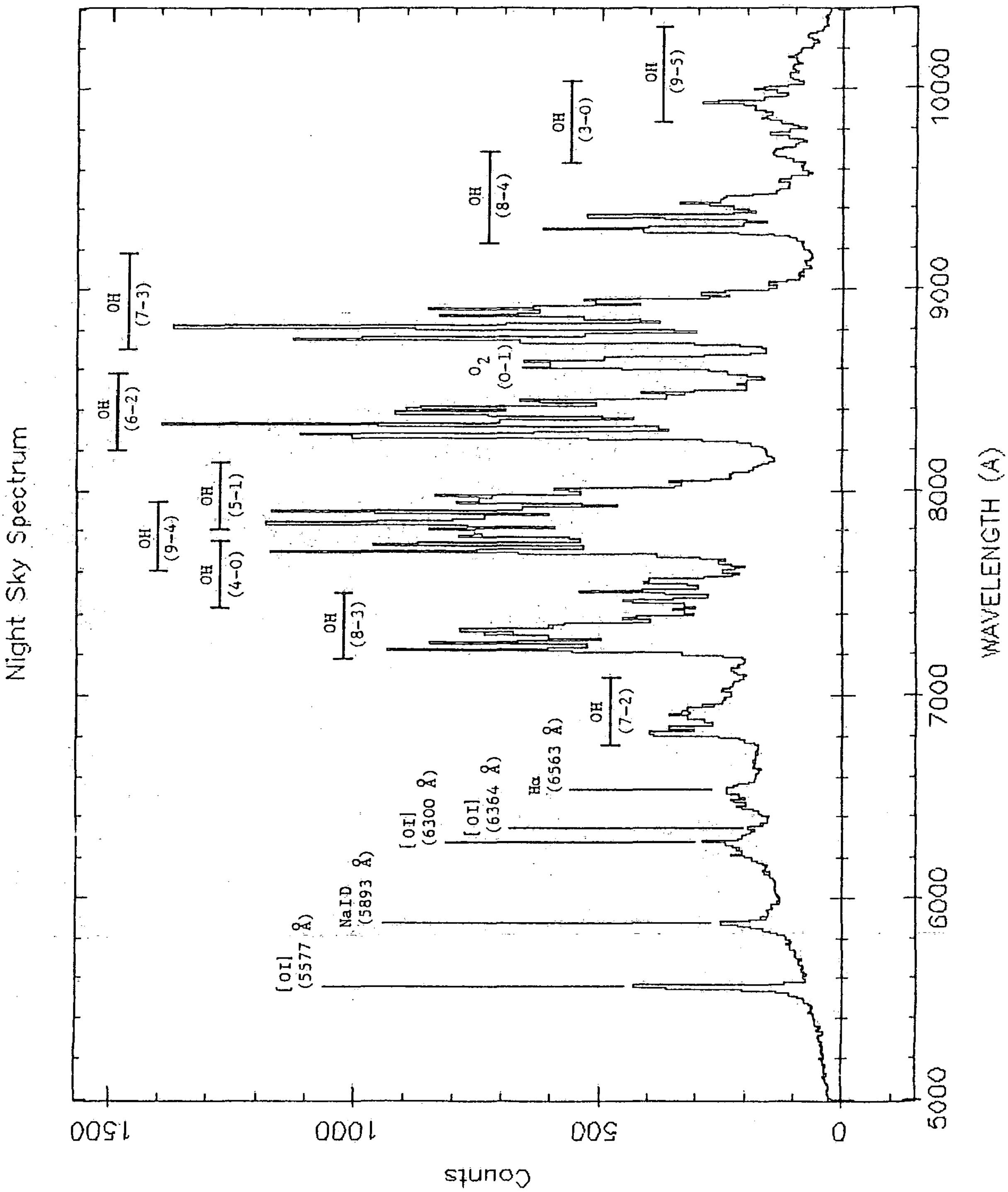

Night Sky Spectrum
Counts
WAVELENGTH (A)
[OI] (5577 Å)
NaI D (5893 Å)
[OI] (6300 Å)
[OI] (6364 Å)
Hα (6563 Å)
OH (7-2)
OH (8-3)
OH (4-0)
OH (9-4)
OH (5-1)
OH (6-2)
OH (7-3)
O_2 (0-1)
OH (8-4)
OH (3-0)
OH (9-5)
0
500
1000
1500
5000
6000
7000
8000
9000
10000

Figure 8.1

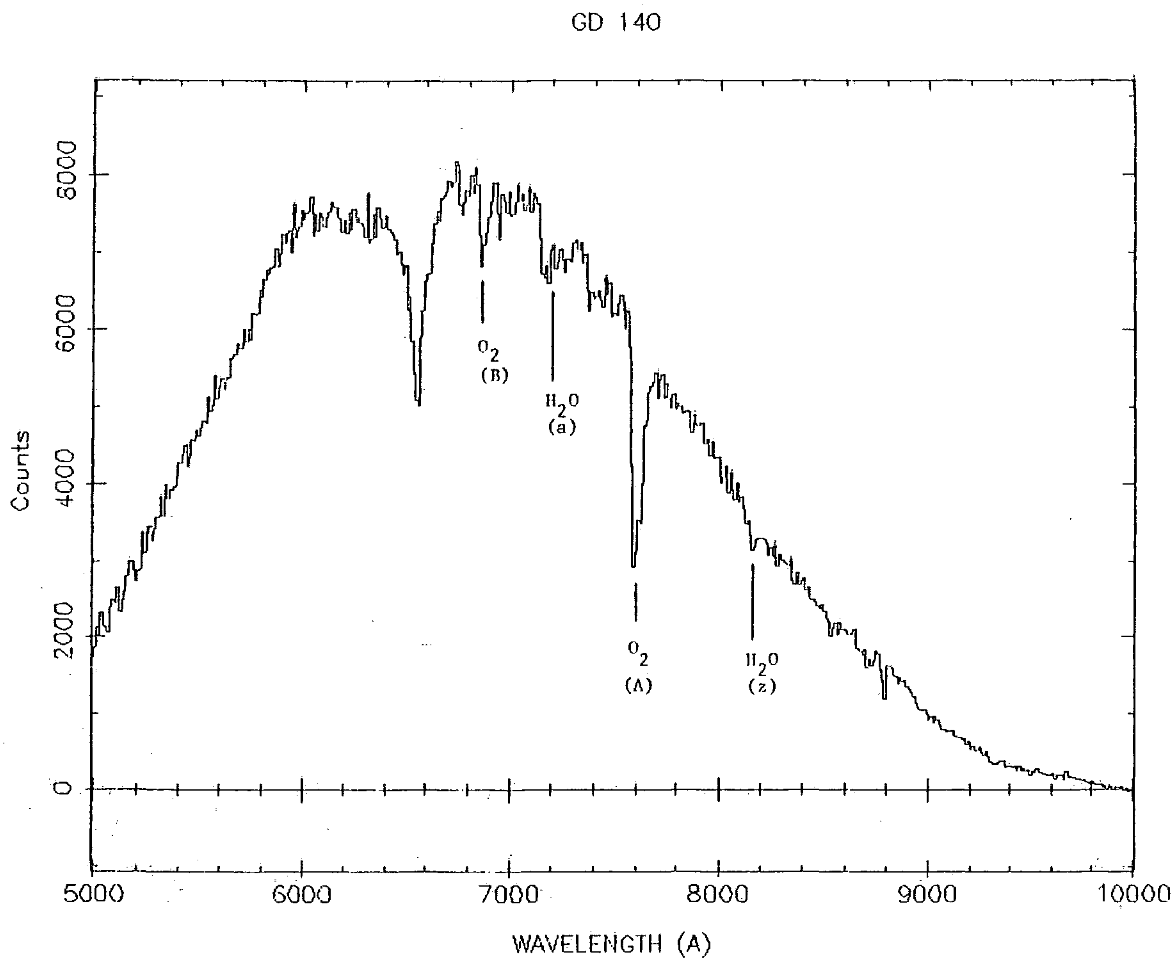


Figure 8.2

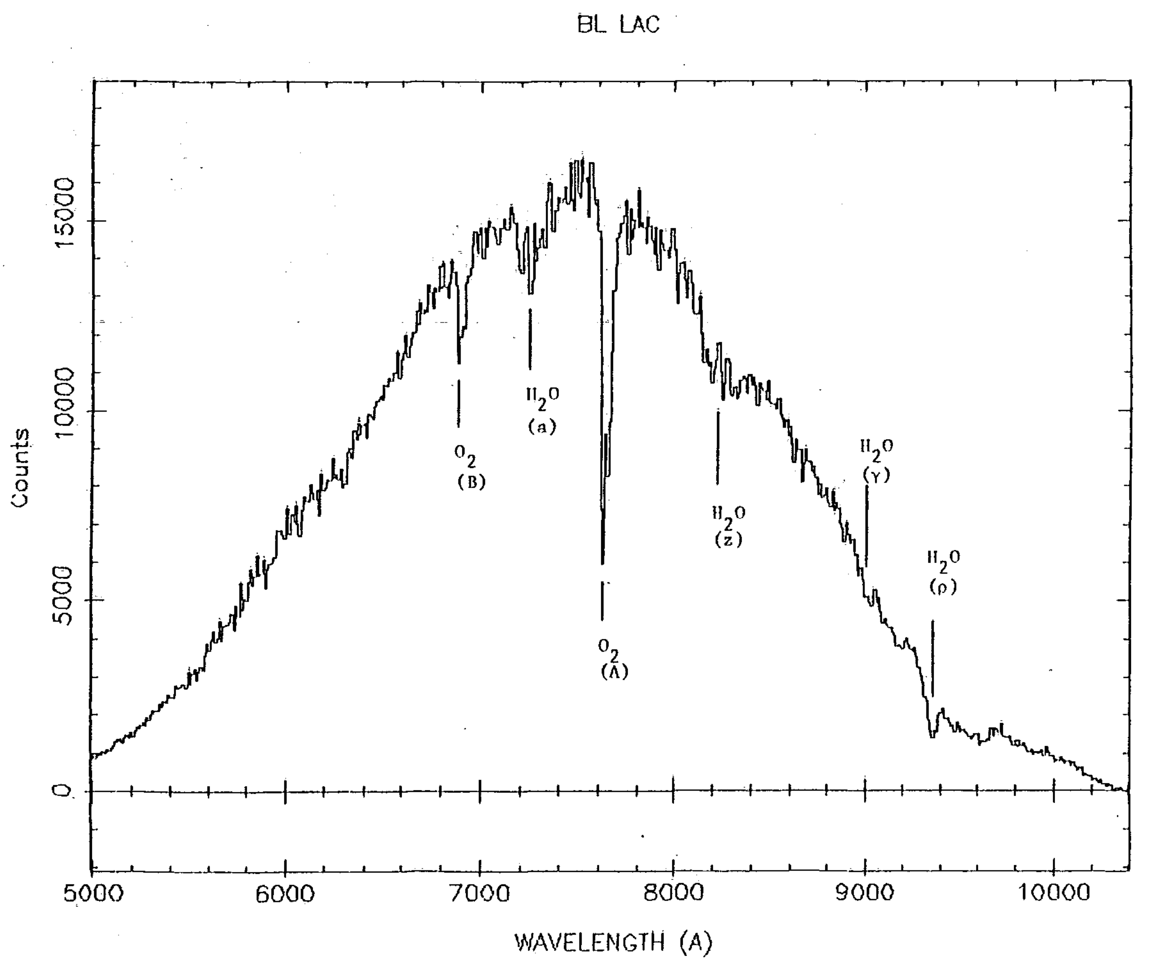


Figure 8.3

8.4 Stellar Spectra and Stellar Classification

Stars can be classified from studies of their continuum (i.e. colour), and their atomic and molecular absorption features. Stars covering a wide spectral classification were observed in order to compile a series of spectra for comparison with future observations.

Figures 8.4 to 8.9 show a sequence of 6 stellar spectra. The object names and their spectral type are listed in Table 8.2:

Table 8.2 FOS STELLAR SPECTRA - STELLAR CLASSIFICATION

Figure 8.4	NGC 6664 F	B3 IV
Figure 8.5	NGC 6664 A	A0 IV
Figure 8.6	NGC 6791 15	F2 IV
Figure 8.7	NGC 6791 20	G0 V
Figure 8.8	NGC 6791 1	K5 III
Figure 8.9	Wolf 1040	M5 V

The following points can be made.

(i) FOS' wide spectral coverage allows one to see the change in continuum slope from early to late-type stars particularly well. Note the change from the blue continuum of the B star through to the red continuum of the M star.

(ii) The characteristically increasing strength of the Hydrogen-alpha line (6563 Å) from the early-type B star, to its maximum strength in the A0 star, and its decreasing strength in the later-type F and G stars is clearly evident.

(iii) Molecular bands, characteristic of late-type stars, are clearly evident from the wide absorption features seen in the spectra of the K and M stars.

Note that in most of the spectra, the atmospheric absorption O_2 A-band has not been fully removed by the data reduction. This is because the data were reduced using the spectrum of a featureless object which was observed on a different night to that of the stars. The lesson to be learnt is that it is important to observe a featureless object for the purposes of removing these bands which is as close as possible, both in terms of its position on the sky and at the time at which it is observed, to the main object of interest.

These stellar spectra proved to be useful in later observations aimed at determining the nature of faint, previously unidentified extragalactic candidates. Figure 8.10 shows the spectrum of an object selected for observation, and designated a 'Funny Faint Red Thing' (FFRT 22h #29), by N Reid (RGO). The exposure time was 500 seconds.

The object is clearly very red but its spectrum contains molecular absorption bands similar to those seen in the two late-type stars, and thus appears to be from a low-luminosity late M dwarf. For comparison, the spectrum of VB 10 (a typical low-luminosity star), obtained with a 400 seconds exposure, is shown in Figure 8.11. Many features seen in FFRT 22h #29's spectrum are also clearly evident in that of VB 10, and are also seen in the spectra of other similar low-luminosity M stars (see for example: Liebert et al., 1978; Liebert et al., 1984).

No further time was spent observing FFRT 22h #29 when it was found to be an M star. During the course of commissioning, several other previously unidentified objects, including objects thought to be members of faint galaxy clusters, were also found to be faint M stars.

FOS' wide wavelength coverage makes it a useful instrument for classification work, and on-line data reduction enabling a spectrum to be produced immediately after an observation has been made can prevent valuable telescope time from being wasted.

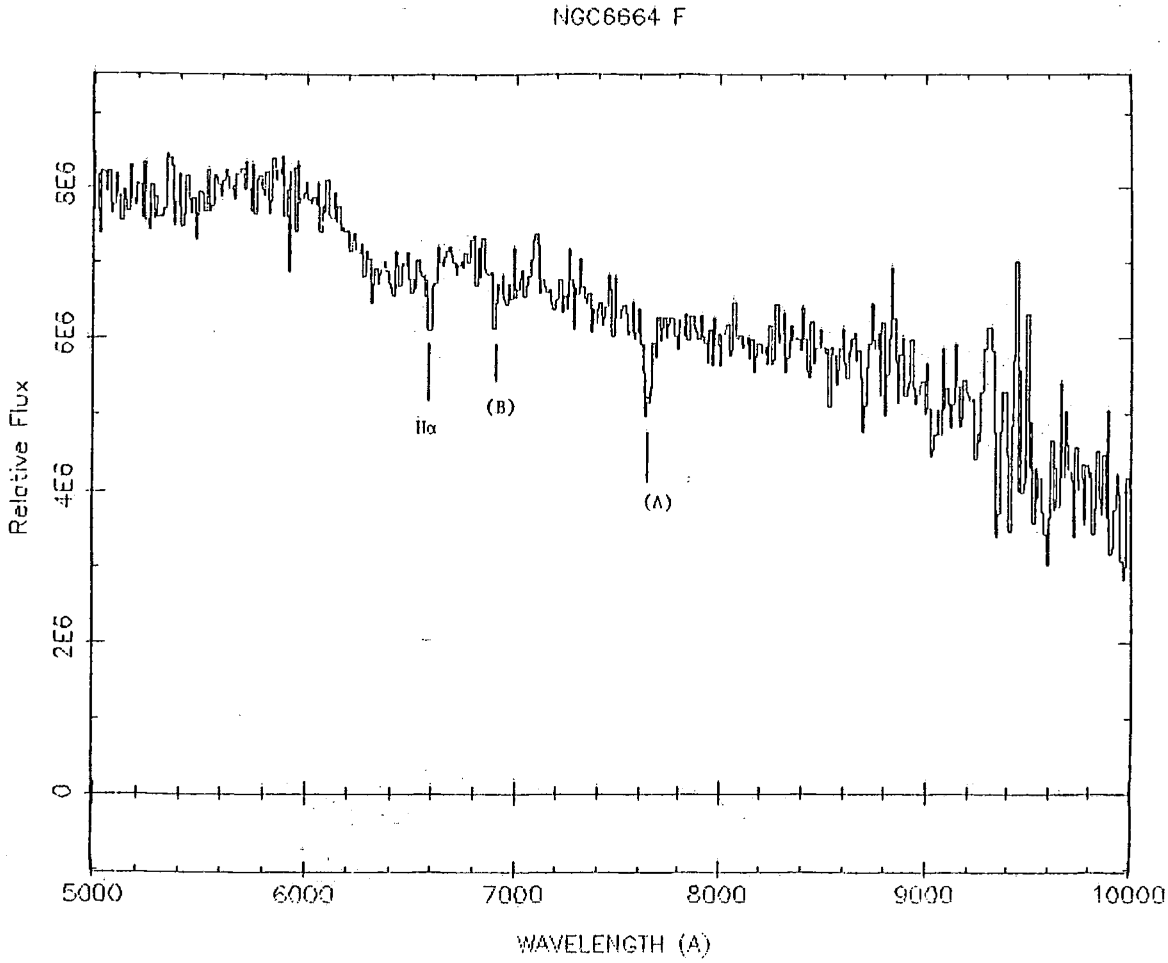


Figure 8.4

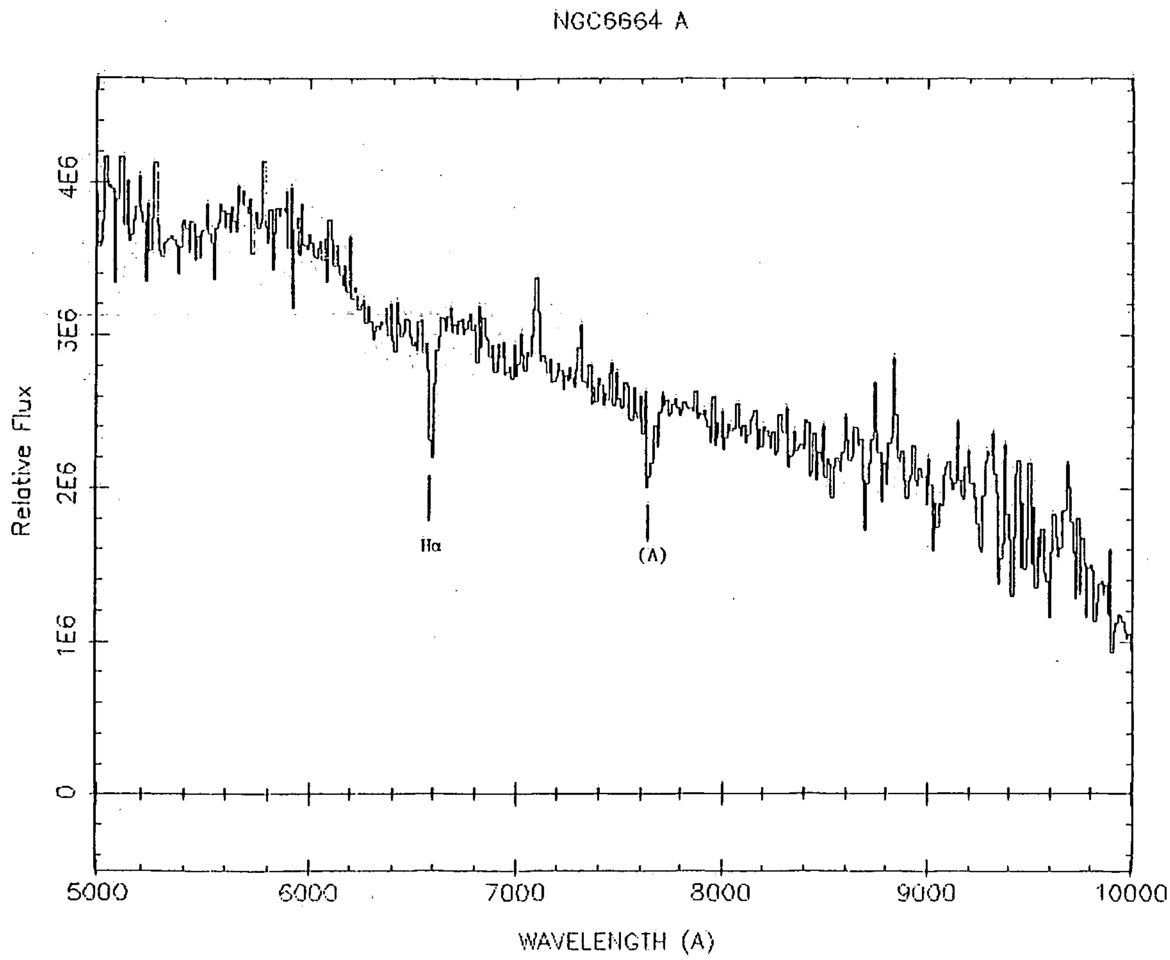


Figure 8.5

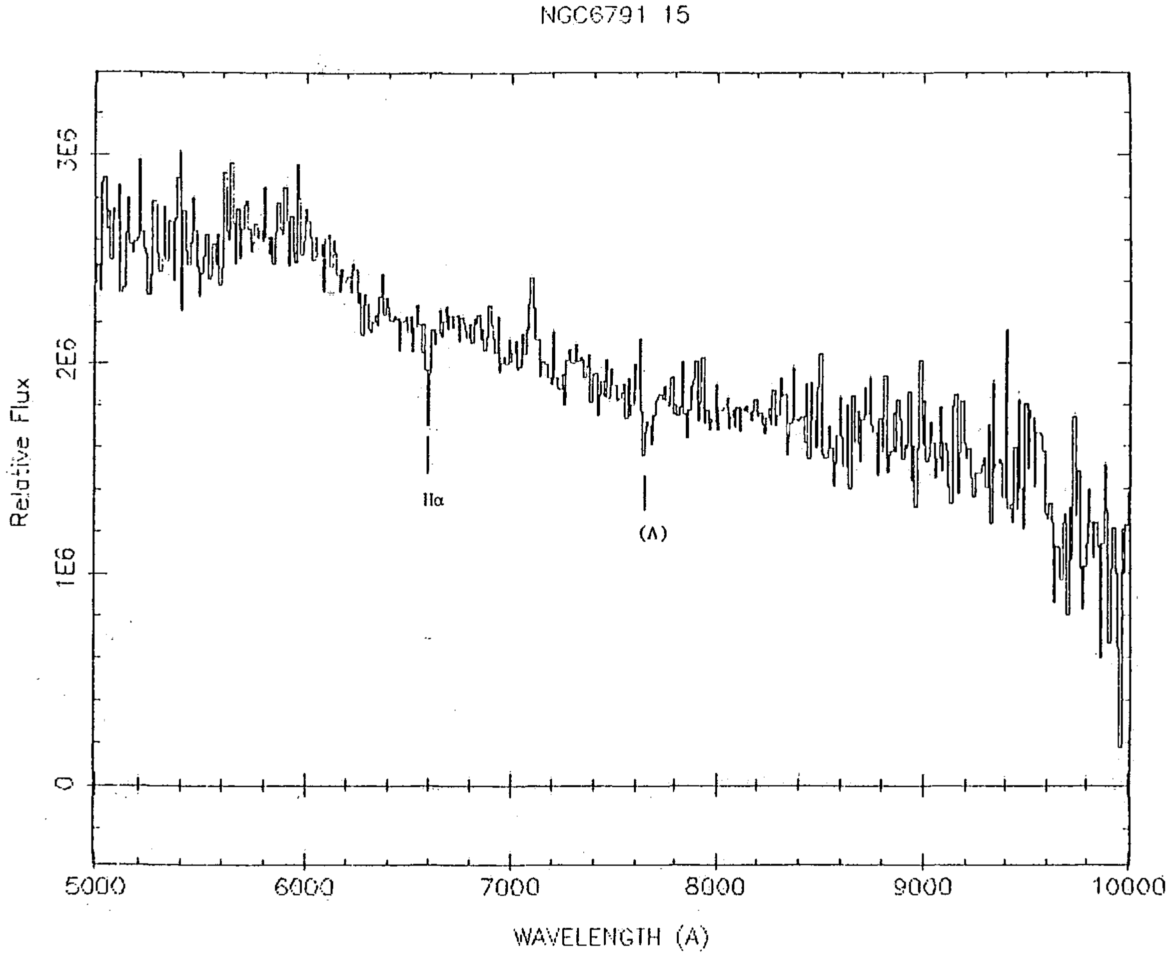


Figure 8.6

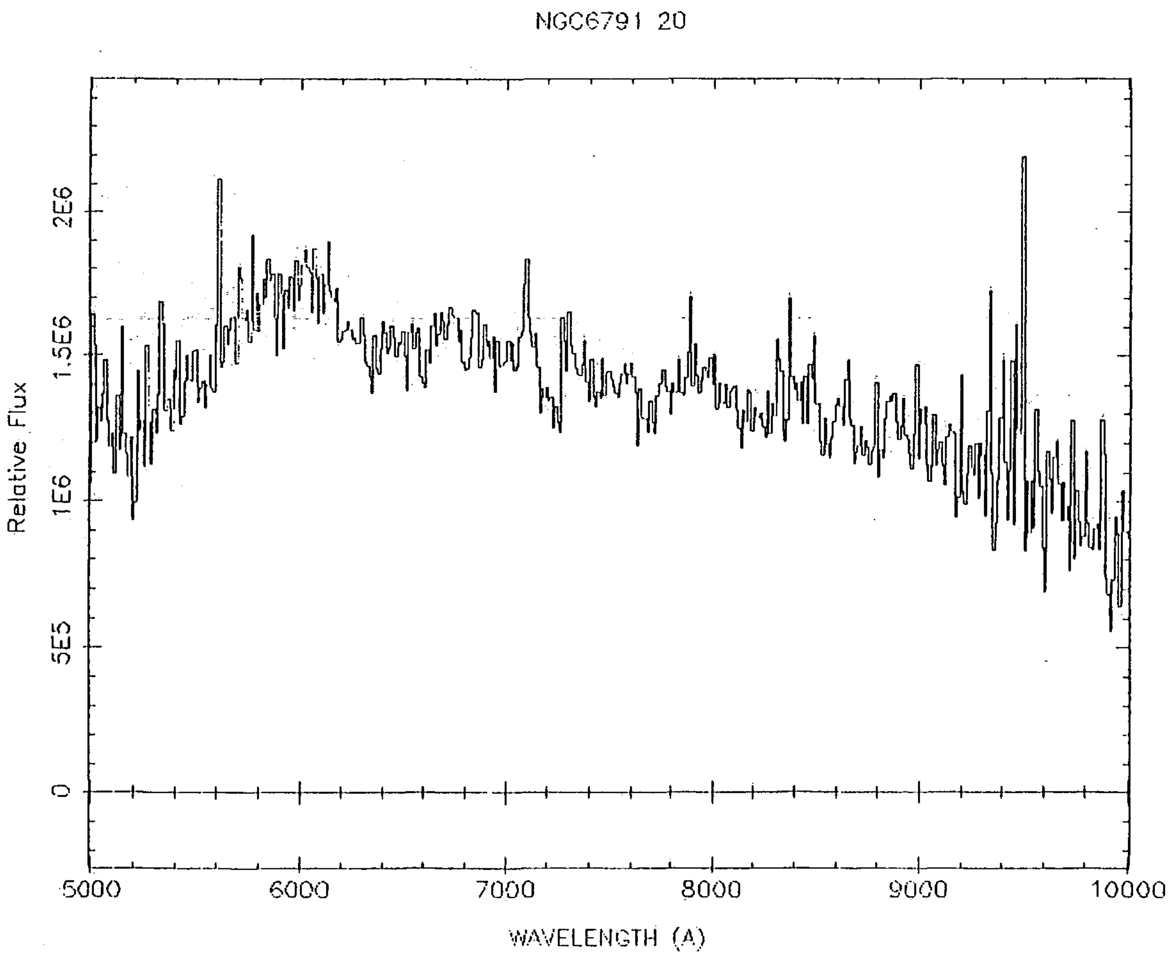


Figure 8.7

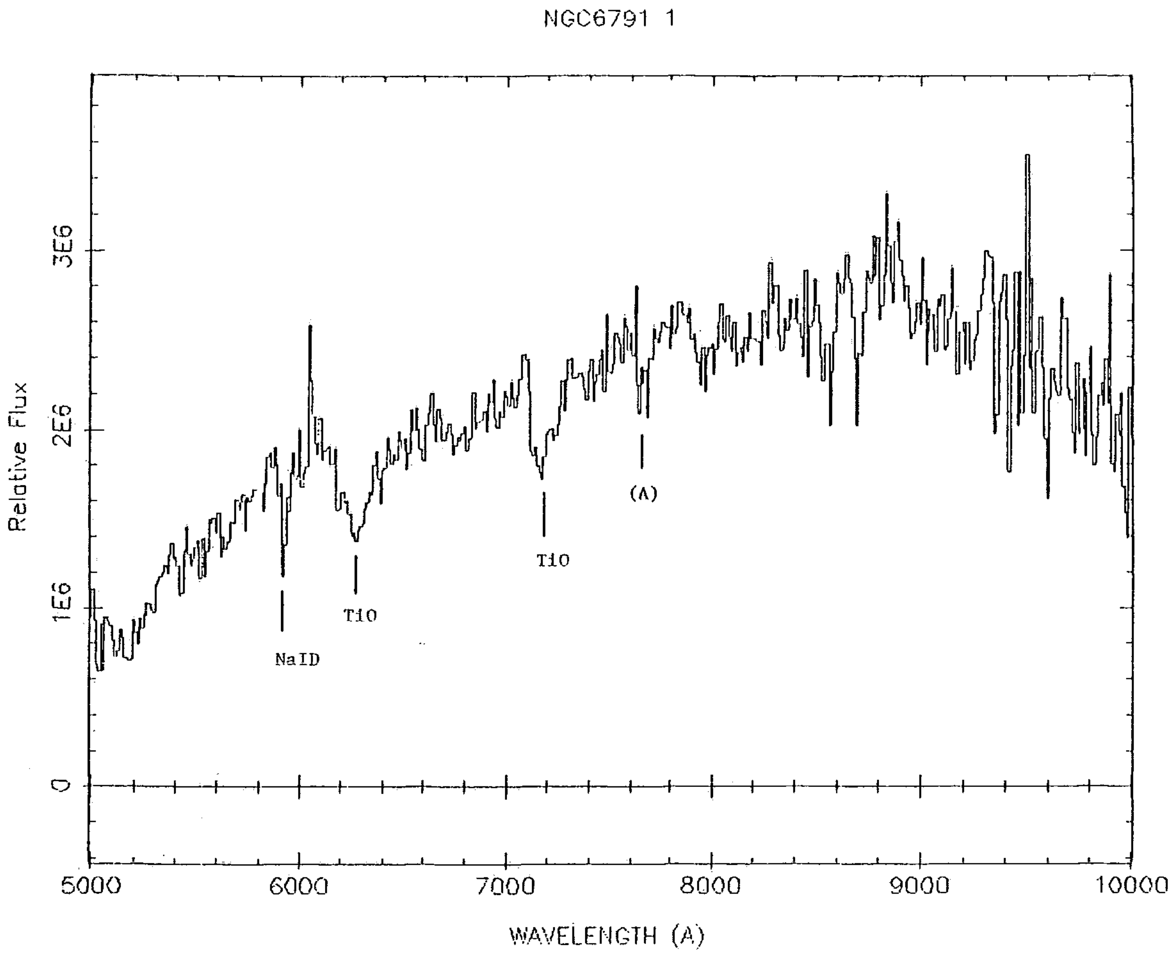


Figure 8.8

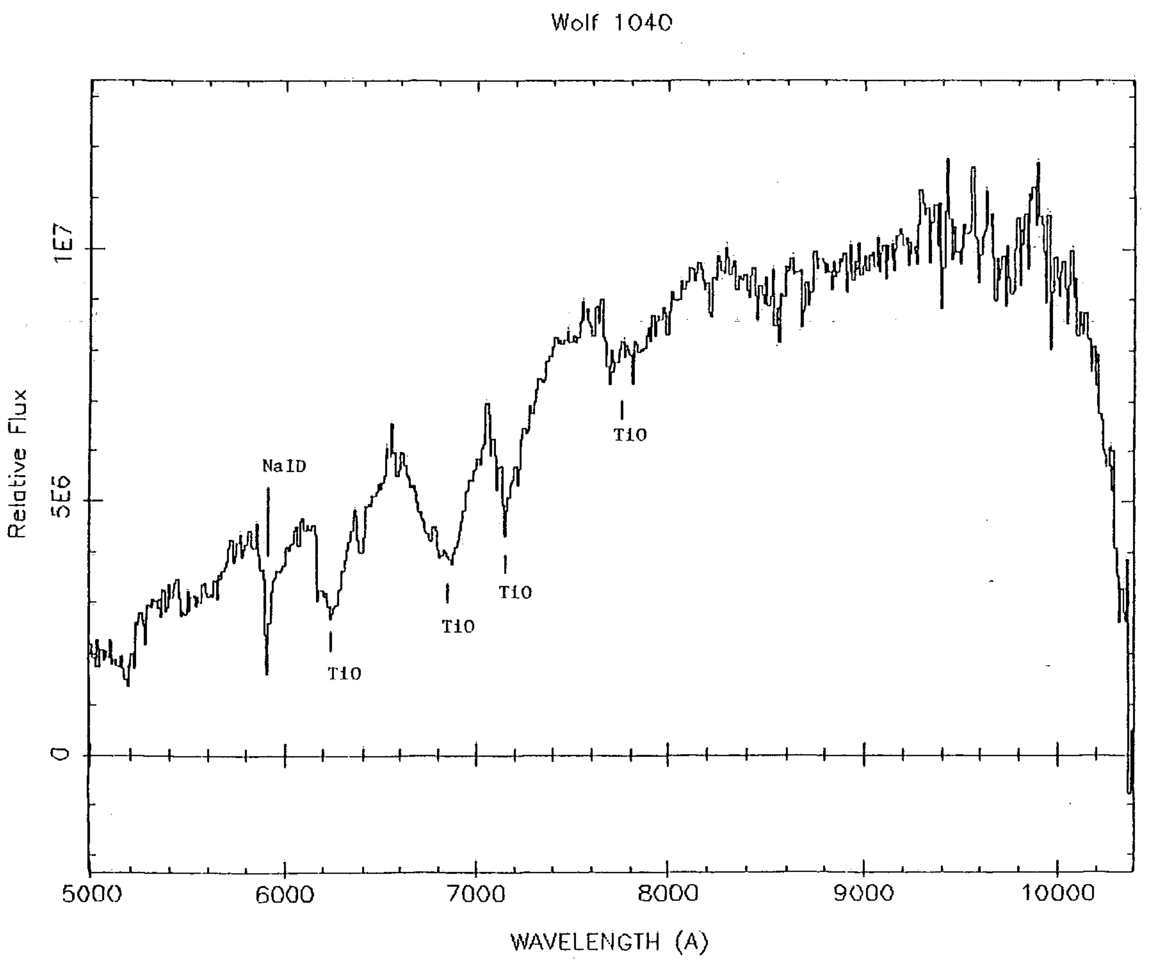


Figure 8.9

FFRT 22h #29

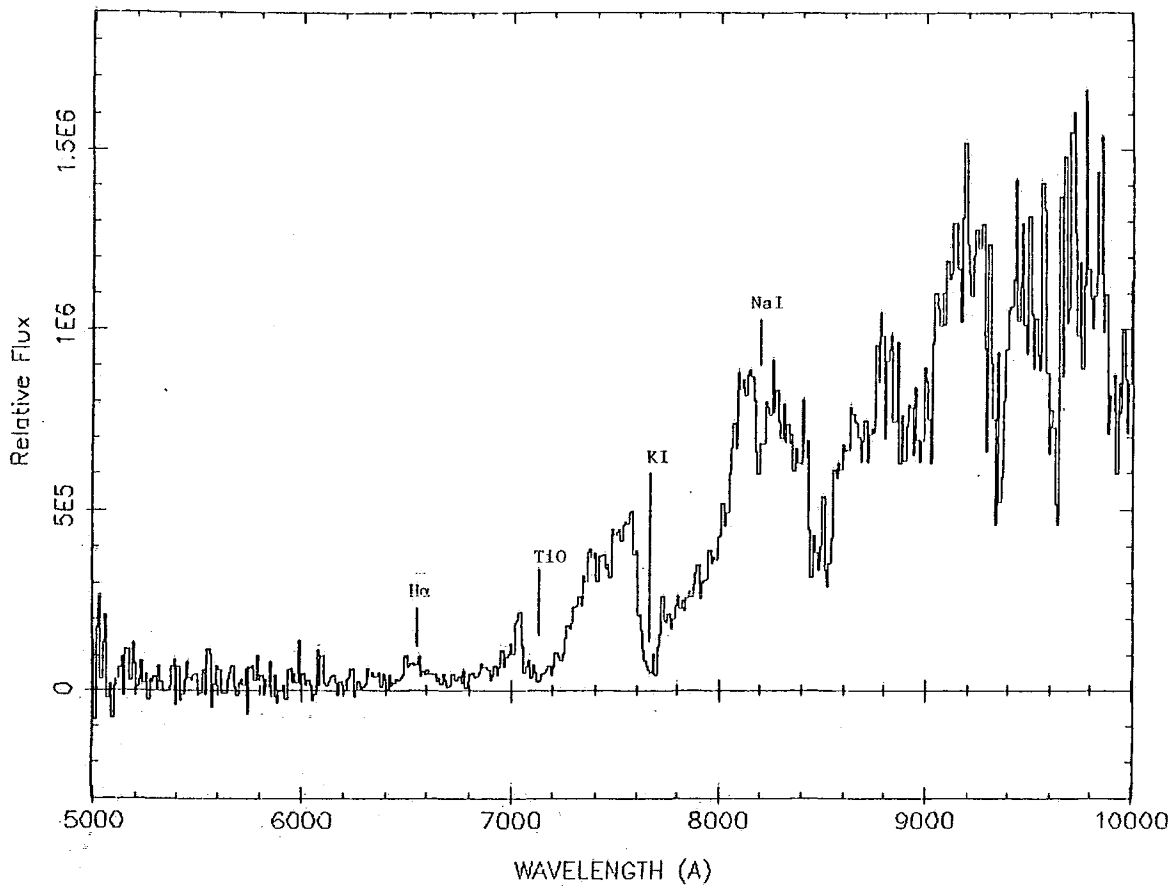


Figure 8.10

VB 10

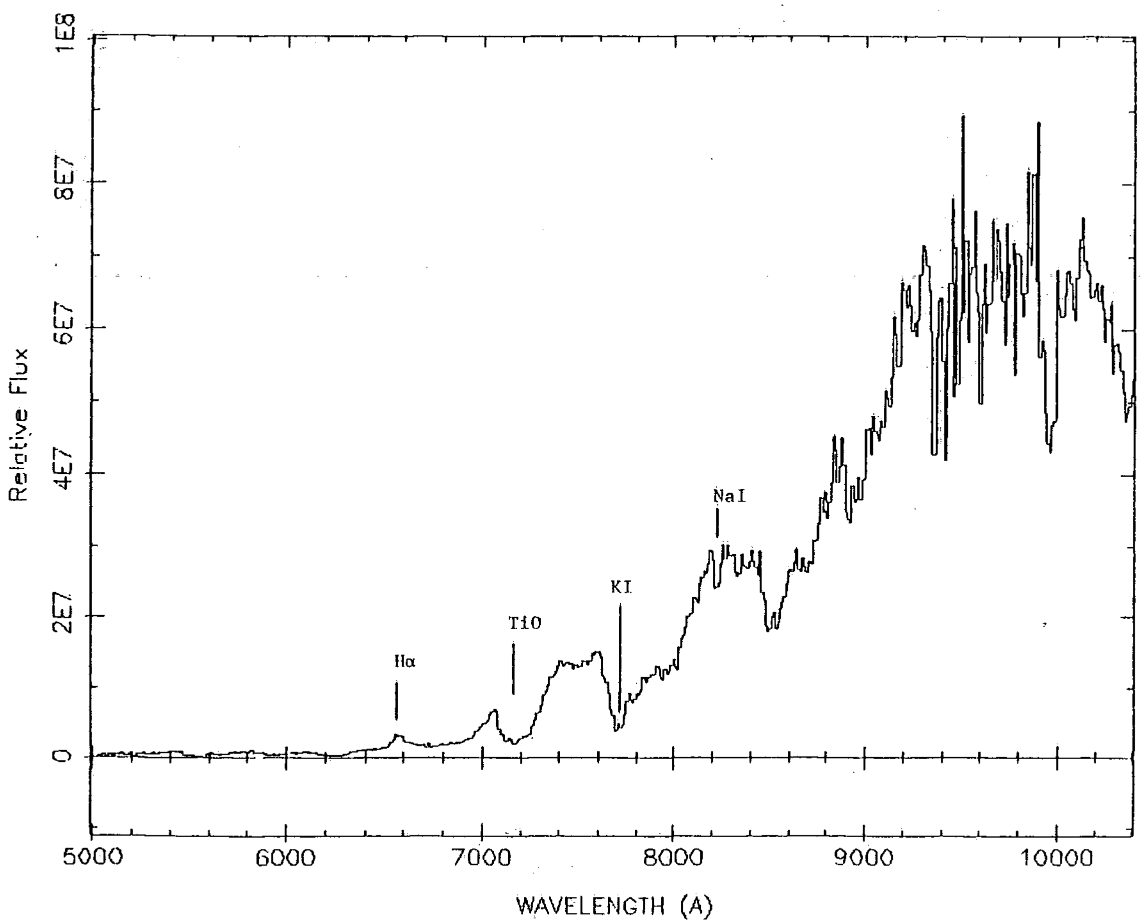


Figure 8.11

8.5 Extragalactic Spectra

FOS is primarily intended for obtaining the spectra of faint extragalactic sources, both for classification purposes and redshift determination.

Spectra of normal galaxies and active galactic nuclei (AGN) are presented in the following sections.

8.5.1 Normal Galaxies

Figure 8.12 shows first and second order spectra of NGC 5813 (m_V = 12.0), obtained with a 300 seconds exposure. NaID (5893 Å) and MgIb (5174 Å) absorption lines, and TiO molecular bands that are attributable to late-type stars, can be identified.

The second order spectrum is plotted in analogue-to-digital conversion (ADU) counts (after sky subtraction), i.e. it has not been fluxed. 1 ADU corresponds to 1 detected photo-electron.

NGC 5813 is a relatively bright object for FOS, but it is already clear that weak absorption features will be difficult to identify until the (sky-subtracted) continuum S/N is good. Data obtained from J1836.10RCa, a faint (m_V ~ 21) galaxy cluster member, illustrates this point particularly well.

Three consecutive 1000 seconds exposures were taken during ´dark time´ in May 1985. Figure 8.13 shows the data at successive stages of reduction.

Figures 8.13a and 8.13b show the object+sky and sky spectra from the first of these exposures. It is immediately clear that the signal counts from J1836.10RCa´s continuum are comparable in number to those from the sky continuum. Identifying features which are attributable to the object will depend on how successfully the sky, and in particular the sky OH emission bands, can be removed from the data.

The resultant data after sky subtraction, and then after flux calibration, are shown in Figures 8.13c and 8.13d. Although the general form of the object's continuum is fairly clear, and there is at least some suggestion of a G-band, the S/N is not really adequate to identify other absorption features with any certainty.

It is also clear that the object's sky-subtracted continuum is contaminated with 'spikes', particularly at wavelengths greater than 7000 Å. These are residuals arising from the subtraction of the night sky OH emission bands, but in general they are too large to be attributable to the shot noise alone. Careful examination of the data reveals that they mostly occur at the transitions between the night sky continuum and the sky emission lines. This is illustrated in Figures 8.13e and 8.13f. Figure 8.13e shows the object+sky and sky spectrum counts (recorded in one pixel wide windows) over the wavelength range 8500–9000 Å. Figure 8.13f shows the result of subtracting these data. Note the features marked A,B,C and D which are all coincident with continuum-line transitions in the night sky spectrum.

The effect is attributable to poor low-level charge transfer efficiency in this particular CCD, arising because of a threshold at the interface between the chip's imaging area and its output register (see Chapter 5). The charge stealing at the threshold, and the resultant charge smearing, results in the precise wavelengths at which the sky lines appear in the object+sky and sky data being slightly different. This misalignment gives rise to the observed residuals when these data are subsequently sky-subtracted. An extreme case of this is seen in Figures 8.13e and 8.13f at the leading edge of the sky line at 8630 Å. Note that the red end of the spectrum is read out first so that the smearing is towards the blue.

Returning to J1836.10RCa, Figures 8.13g and 8.13h show the improvement in S/N gained by adding the data from a further two 1000 seconds exposures. The spectra were added together after each individual spectrum had been sky-subtracted, but before flux calibration. G-band (4304 Å), MgIb (5174 Å) and H-beta (4861 Å) identifications are proposed, giving a redshift for J1836.10RCa of 0.275.

It is clear from this example that weak absorption features only become recognizable when their widths distinguish them from the general pixel to pixel noise. It is also clear that the identification of weak absorption features will be difficult until the (sky-subtracted) continuum S/N is good.

Redshift determinations for faint galaxy cluster members without strong emission lines will therefore rely primarily on the identification of strong absorption features such as G-band and CaII K and H (laboratory wavelengths 4304 Å, 3933 Å and 3968 Å respectively) when these are redshifted sufficiently so as to appear in FOS' first order (CaII K will appear in first order at 5000 Å when $z = 0.27$).

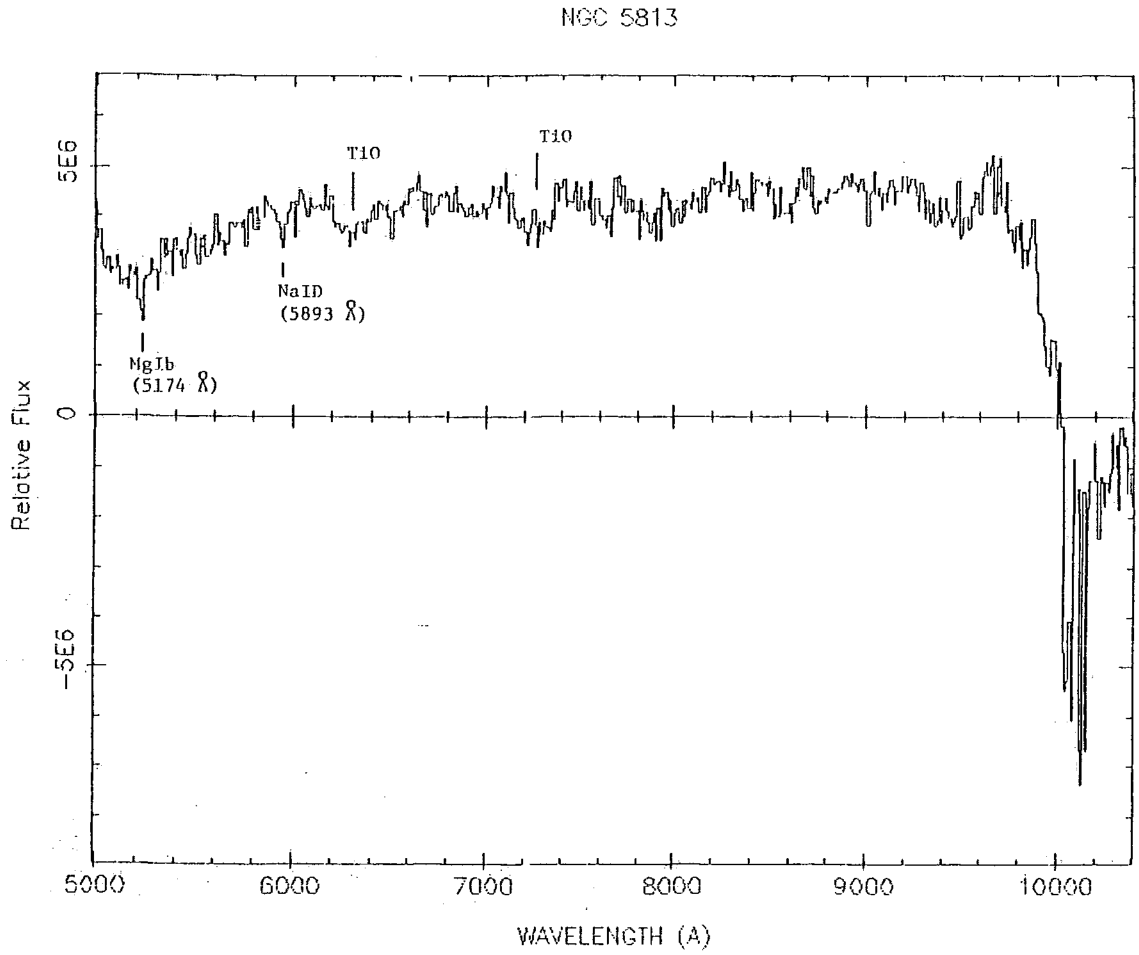


Figure 8.12a

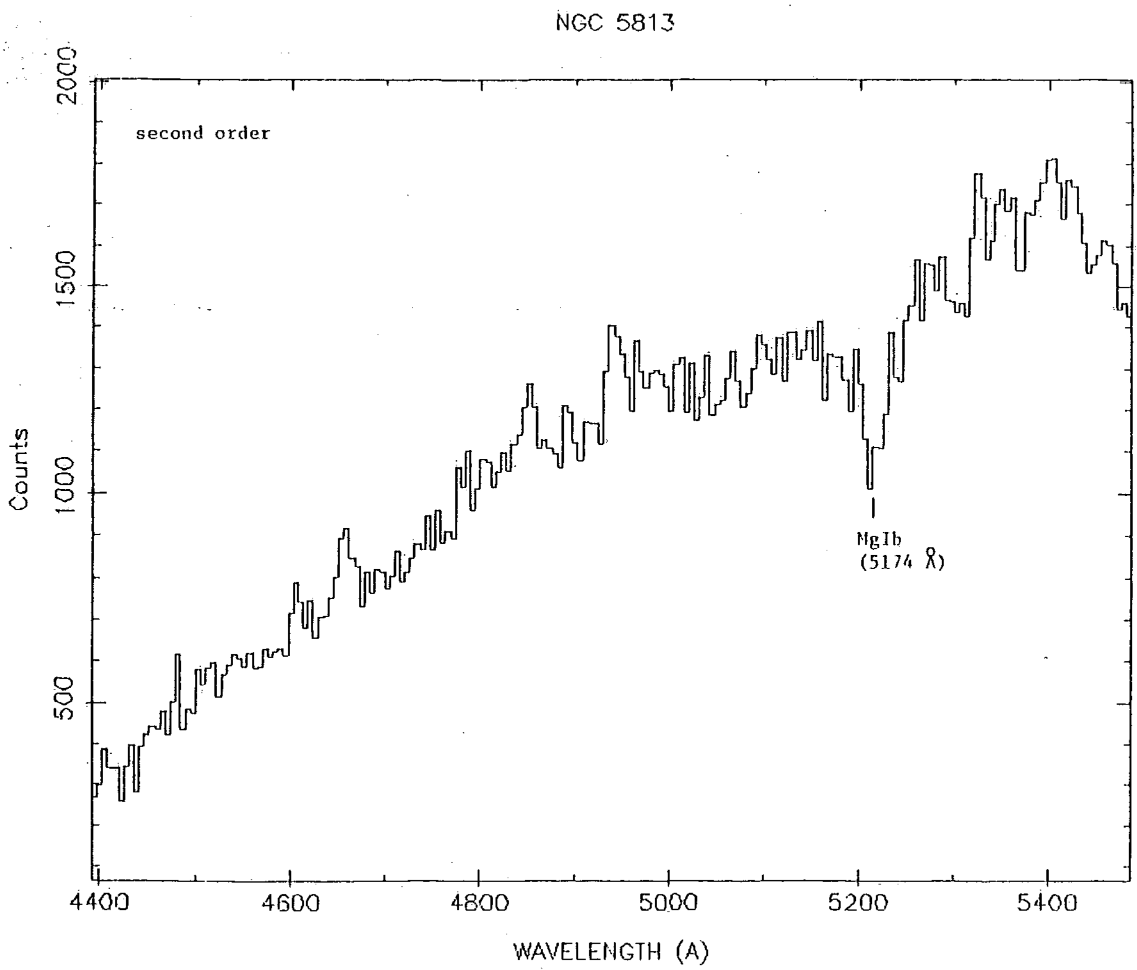


Figure 8.12b

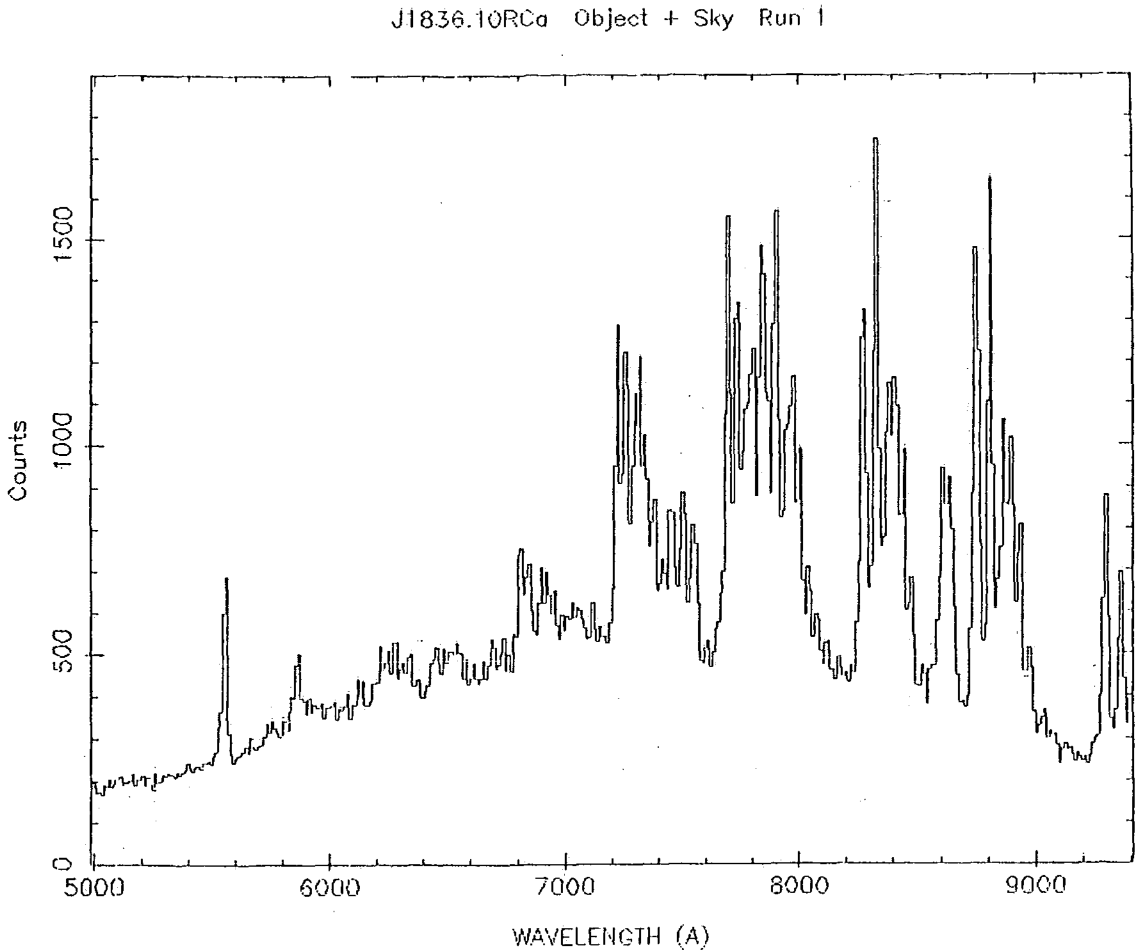


Figure 8.13a

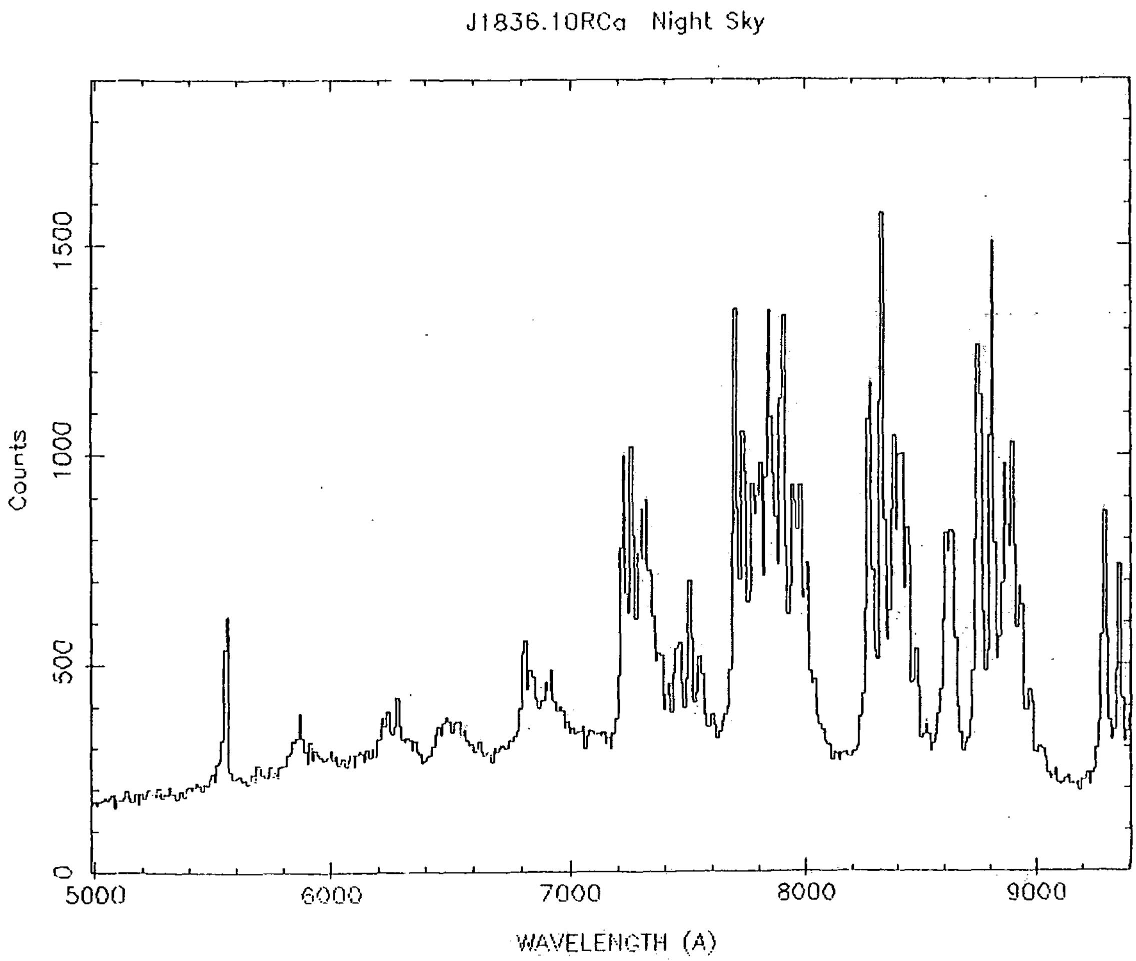


Figure 8.13b

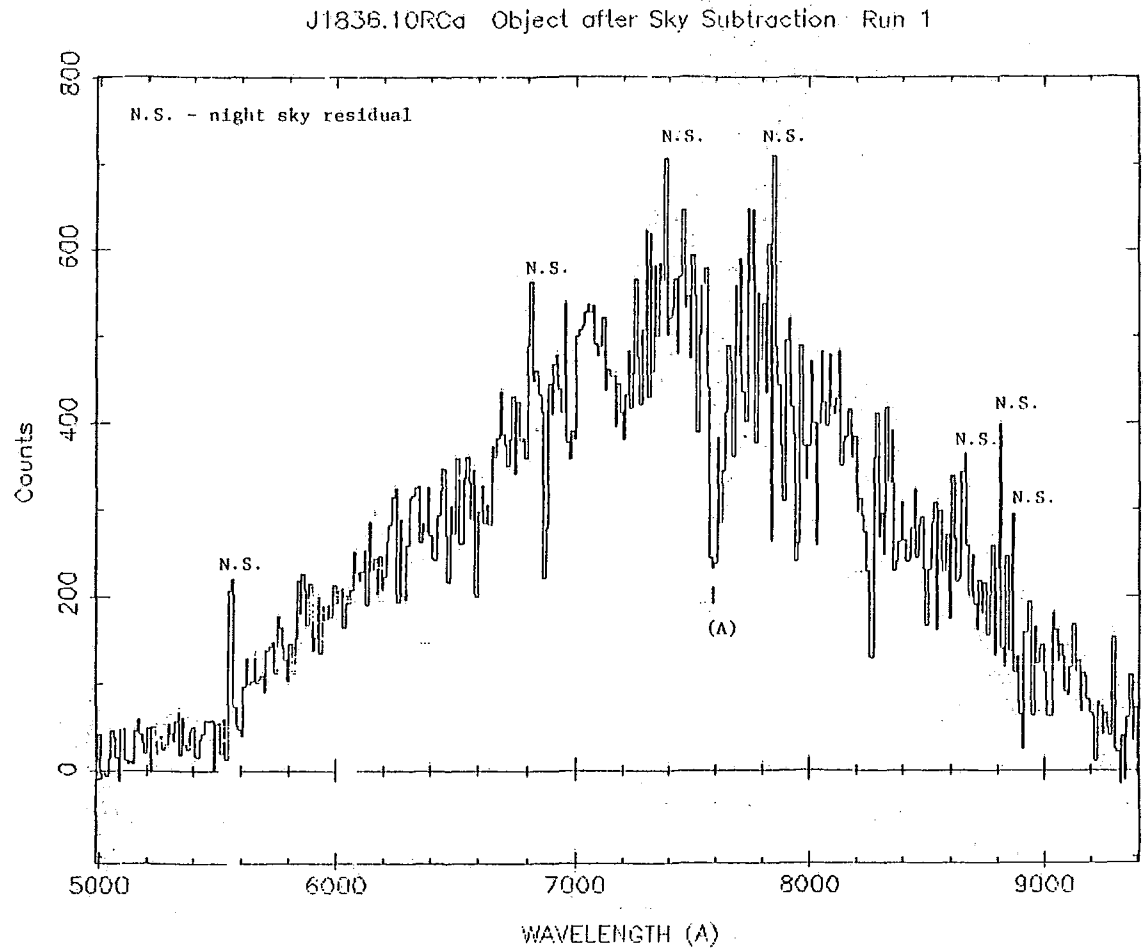


Figure 8.13c

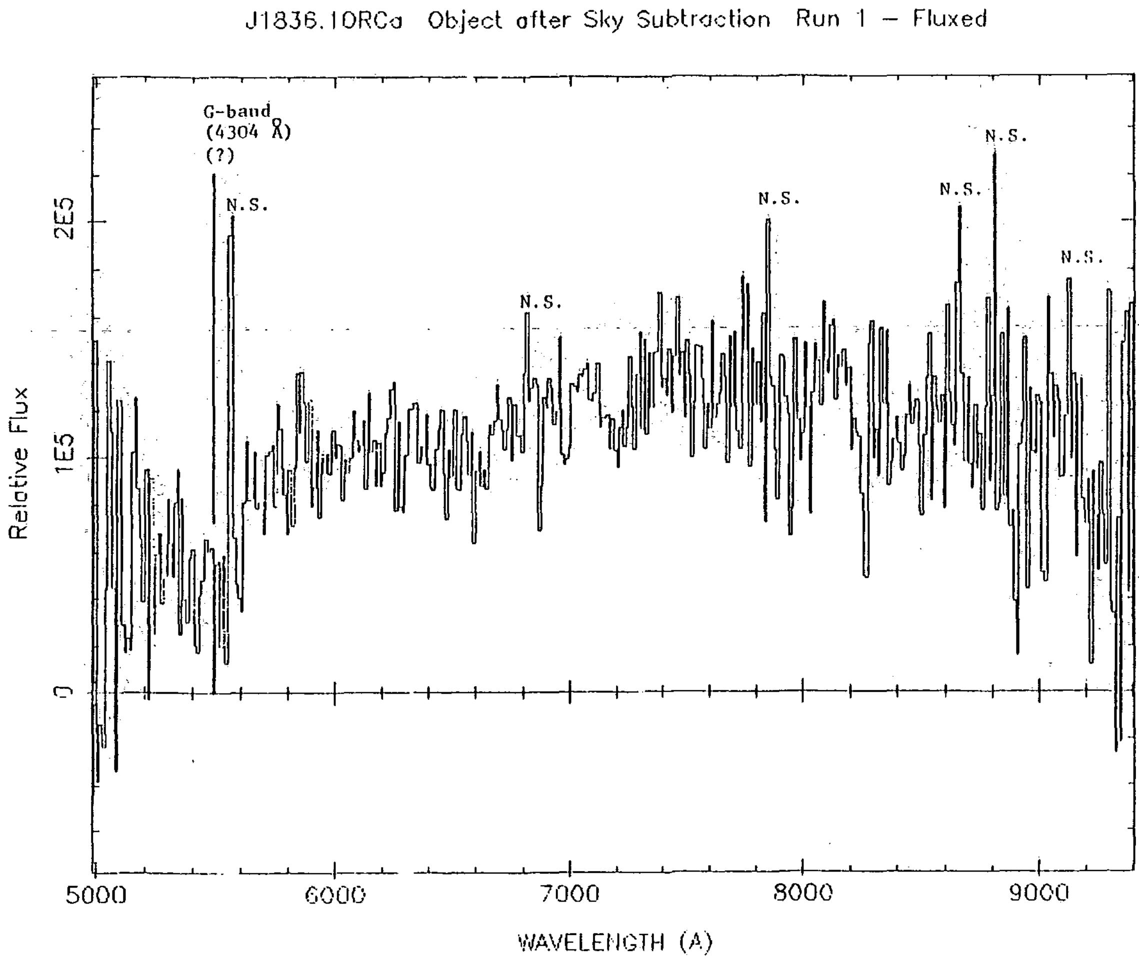


Figure 8.13d

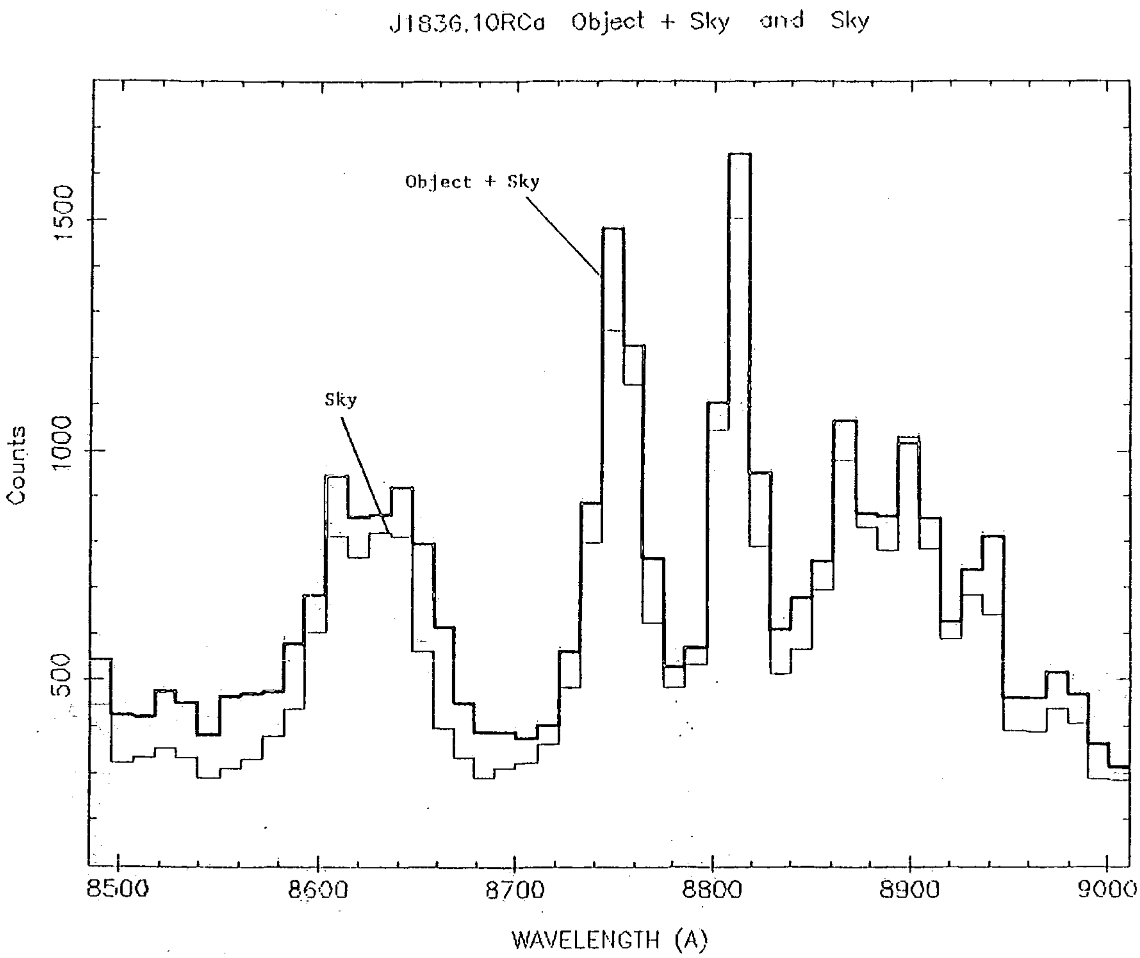


Figure 8.13e

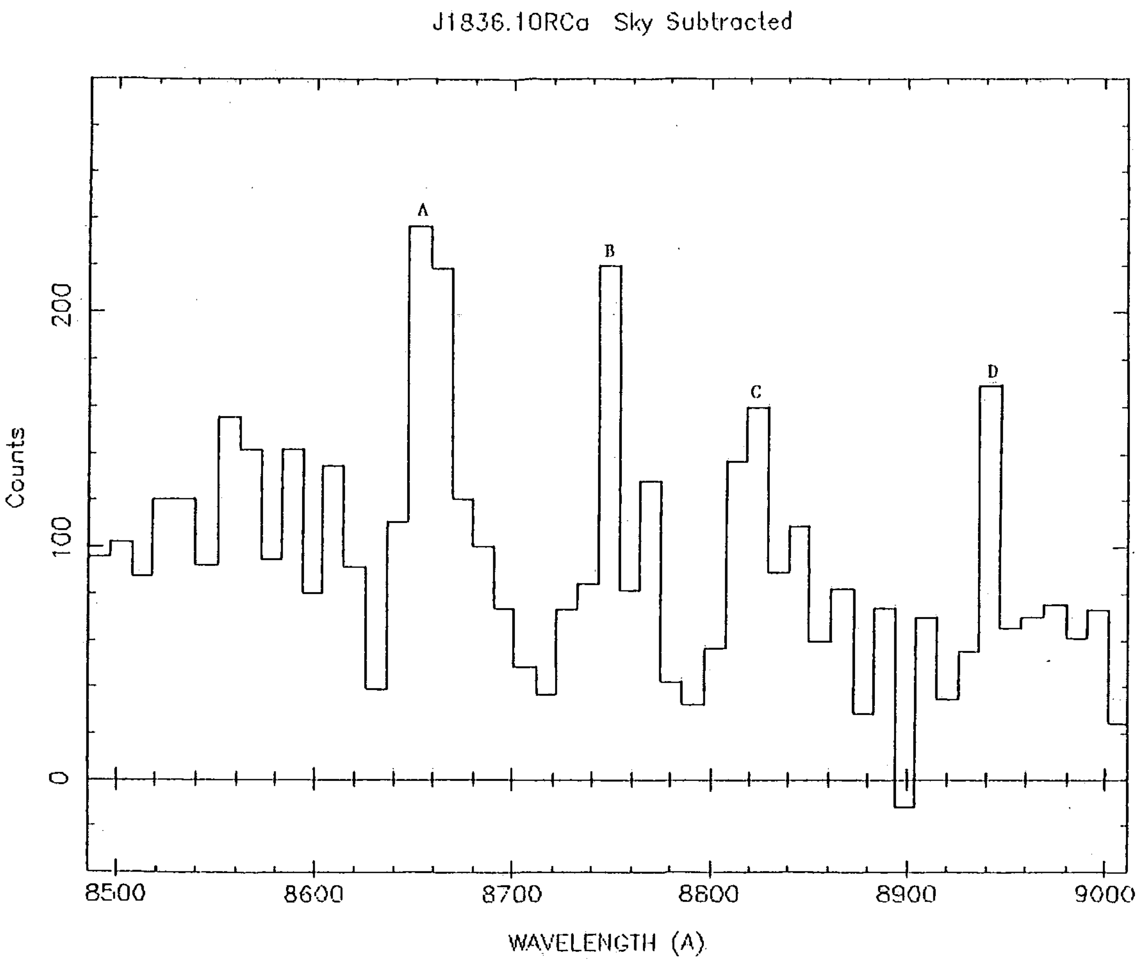


Figure 8.13f

J1836.10RCa Object after Sky Subtraction – Sum of 3 Runs

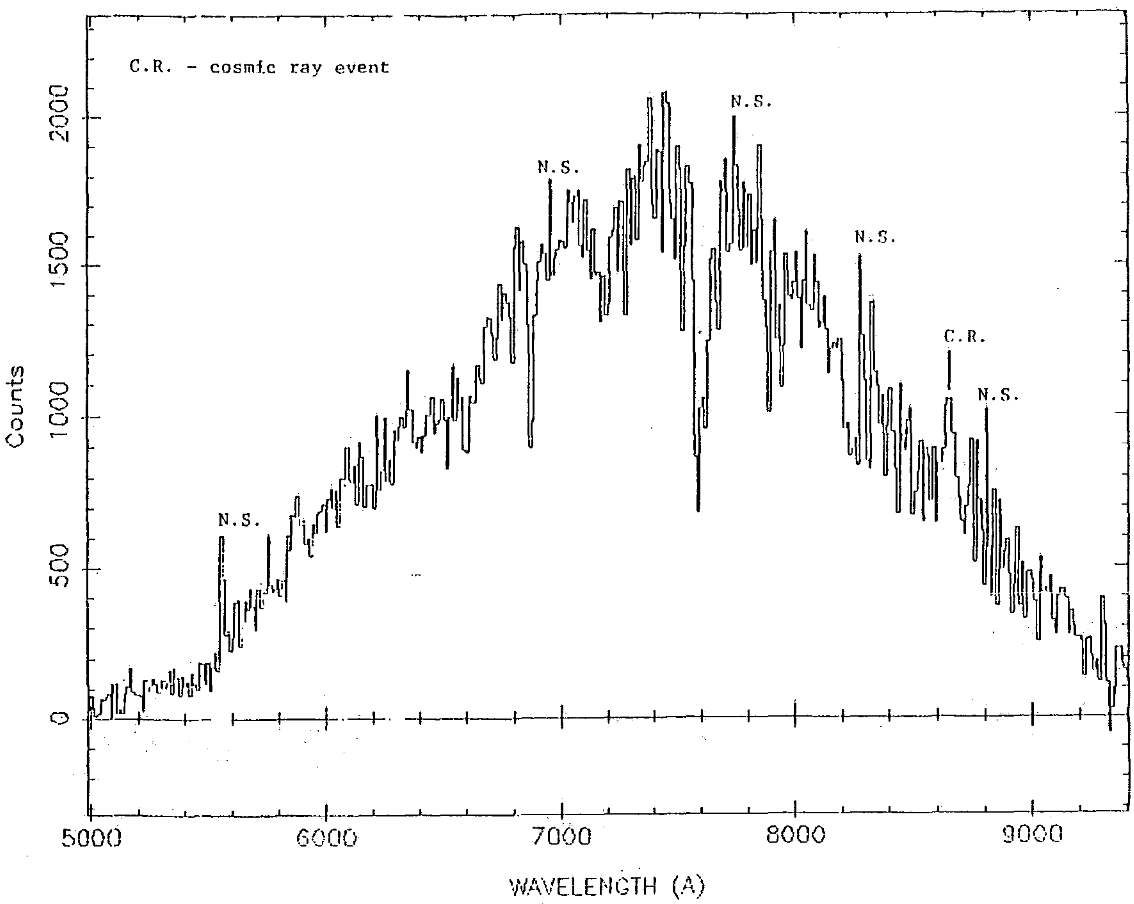


Figure 8.13g

J1836.10RCa Object after Sky Subtraction – Sum of 3 Runs – Fluxed

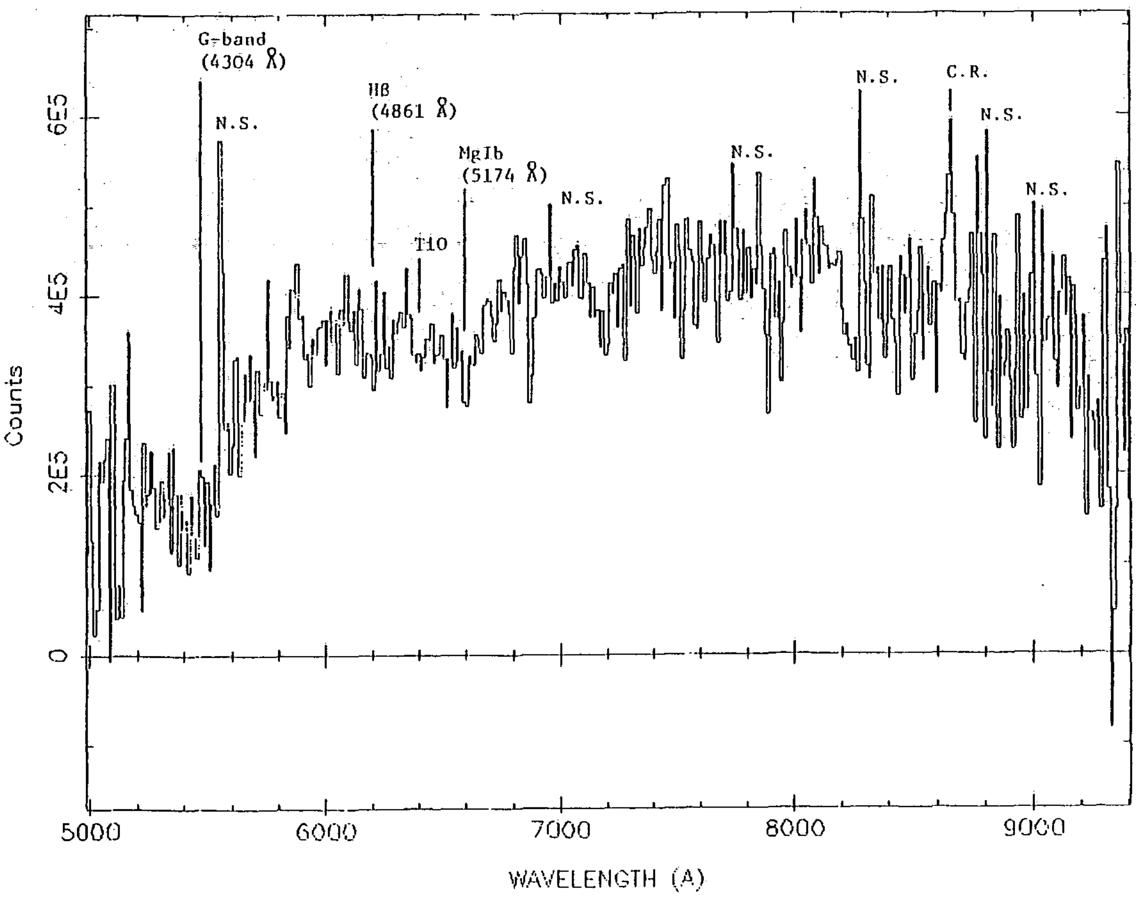


Figure 8.13h

8.5.2 Active Galactic Nuclei

The spectra of active galactic nuclei are generally characterized by the presence of strong emission line features upon a background continuum. One would therefore expect the classification of this family of objects to be easier than for absorption line objects since, even for faint objects with a low S/N (sky-subtracted) continuum, the emission features should stand out above the continuum.

The first two examples to be presented are relatively bright objects for FOS. Both were obtained early in the first commissioning run and given long exposures in order to obtain a high S/N.

Figure 8.14 shows the spectrum of PKS2128-12, a Seyfert I object (m_V = 15.98, z = 0.501, Craine, 1977), obtained with an 800 seconds exposure on the first night of commissioning.

A Seyfert galaxy is classed as a spiral galaxy which has a bright compact nucleus and an emission line spectrum. Seyferts are grouped into two categories:

(i) Type I - broad wings on the permitted lines and narrow forbidden lines.

(ii) Type II - narrow excitation and forbidden lines.

PKS2128-12's spectrum clearly shows H-alpha (6563 Å), H-beta (4861 Å), H-gamma (4340 Å) and [OIII] (4959 and 5007 Å) emission. The broad wings on the permitted hydrogen lines are consistent with the object's Seyfert I classification. H-delta (4102 Å), [OII] (3727 Å), [NeIII] (3869 Å) and [NeV] (3426 Å) identifications are also proposed, these being consistent with a redshift z = 0.501. The absorption features at 7600 and 9370 Å are residuals of the atmospheric absorption.

Figure 8.15 shows the spectrum of 3C380 (1828+487) obtained with a

600 seconds exposure. 3C380 (m_V = 16.81, z = 0.691) is classed as a QSO (Laing et al., 1983). H-beta (4861 Å), H-gamma (4340 Å), H-delta (4102 Å), [OIII] (4959 and 5007 Å), [OII] (3727 Å), [NeIII] (3869 Å) and [NeV] (3426 Å) emission are identified at wavelengths consistent with the object's previously measured redshift. Note that H-alpha is redshifted beyond FOS' wavelength coverage.

Relatively bright (i.e. m_V < 17) objects with strong emission line features are thus easily classified with FOS. In these cases, the counts from the object are relatively large in number compared to those from the sky. As fainter objects are observed, the counts from the sky become comparable, and eventually greater, in number to those from the object and so good sky subtraction again becomes important.

Figure 8.16 shows the spectrum of 4C53.24 (1213+538), a m_V = 17.9 QSO (Hewitt and Burbridge, 1980), obtained with a 1000 seconds exposure during 'bright time' in May 1985.

Walsh and Carswell (1982) have reported a redshift z = 1.065 for 4C53.24 based on identifications of [CIII] (1909 Å) seen at 3938 Å and MgII (2798 Å) seen at 5793 Å. The FOS spectrum confirms this, with MgII clearly visible at 5790 Å, and H-gamma (4340 Å) seen at 8970 Å. H-delta (4102 Å), [OII] (3727 Å), [NeIII] (3869 and 3968 Å) and [NeV] (3346 and 3426 Å) identifications are also proposed, these appearing at wavelengths consistent with z = 1.065.

Note that the continuum S/N is obviously less than in the two previous AGN spectra, and residuals from the subtraction of the night sky are beginning to appear. This becomes even more evident in the next example.

Figure 8.17 shows the spectrum of the fainter (m_V = 18.47) QSO 3C454 (2249+185) with redshift z = 1.757 (Laing et al., 1983). This spectrum was obtained by adding the data from two 1000 seconds exposures. MgII (2798 Å) and [CIII] (1909 Å) emission are identified (these being consistent with the object's previously measured redshift), but the lower continuum S/N is now making it difficult to identify weaker features with any certainty.

The objects discussed so far all have previously measured redshifts. It is obviously fairly straightforward to identify features when one has a good idea of what features to look for, and where. A more useful test of FOS, therefore, is to attempt to interpret the spectra from faint objects with unknown or unconfirmed redshifts.

The remaining AGN spectra to be presented are of faint, identified radio sources, selected for observation from a compilation of optical identifications of bright radio sources at 178 MHz (Laing et al., 1983). The first object, the candidate for the central core of the radio source 4C14.27, does not have a previously measured redshift. In the case of the second object, the candidate for the central core of 4C16.49, a provisional redshift has been reported by Mitton et al. (1977), but FOS data contradicts their result.

The radio source 4C14.27 (0832+143) is thought to be associated with a m_V = 19.5 galaxy (Laing et al., 1983). From its apparent magnitude, Laing et al. have estimated the galaxy's redshift to be ~ 0.31. FOS spectra of this object were obtained with two 1000 seconds exposures. The data, as outlined below, are shown at successive stages of reduction in Figure 8.18.

Figure 8.18a	non-fluxed sky-subtracted spectrum obtained from the first exposure.
Figure 8.18b	sky spectrum from the first exposure.
Figure 8.18c	non-fluxed sky-subtracted spectrum obtained from the second exposure.
Figure 8.18d	sky spectrum from the second exposure.
Figure 8.18e	fluxed sky-subtracted spectrum from the first exposure.
Figure 8.18f	fluxed sky-subtracted spectrum from the second exposure.
Figure 8.18g	non-fluxed sky-subtracted spectrum obtained by adding the data from the first and second exposures, after sky subtraction, but before flux calibration.
Figure 8.18h	fluxed spectrum of Figure 8.18g.

Examination of the non-fluxed sky-subtracted spectrum and its corresponding sky spectrum obtained from each exposure reveals that the signal counts from the object's continuum are comparable in number to those from the sky continuum. Residuals of the night sky OH emission bands are also evident.

Moving on to the fully reduced spectrum (Figure 8.18h); although the redshift of this object is not known, note the three emission features seen at 9140 Å, 6970 Å and 6770 Å. These could well be H-alpha (6563 Å), [OIII] (5007 Å) and H-beta (4861 Å), which will all appear at these wavelengths in the spectrum of an object having a redshift $z \sim 0.4$. The presence of several other emission lines seen at 6900 Å, 6040 Å and 5190 Å and their association with [OIII] (4959 Å), H-gamma (4340 Å) and [OII] (3727 Å) confirms this hypothesis, and together these identifications yield a precise redshift $z = 0.392$.

Note that the same recognizable pattern of H-alpha, [OIII] and H-beta lines also occurs in the spectrum of PKS2128-12 (Figure 8.14), but at a slightly greater redshift $z = 0.501$.

It is now interesting to examine the fluxed sky-subtracted spectra obtained from the individual 1000 seconds exposures (Figures 8.18e and 8.18f). The spectrum from the first exposure clearly reveals the H-alpha, [OIII] (5007 Å) and H-beta features, the suggestion being that a redshift could have been obtained from this spectrum alone. Note how H-alpha is still seen clearly amongst the continuum noise which becomes increasingly significant at wavelengths greater than 8400 Å due to the residuals from the sky OH emission bands. The H-alpha emission feature is also seen in the spectrum from the second exposure, and although [OIII] can also be seen, H-beta is not obvious. H-beta actually appears (at this redshift) close to the atmospheric O_2 B-band and is to a certain extent obscured by this.

The presence of several easily recognizable emission features within this object's spectrum therefore makes the redshift interpretation quite straightforward. H-alpha, the two [OIII] lines and H-beta will appear together in FOS' first order for redshifts up to $z \sim 0.5$. As will be seen in the next example, it is much more difficult to determine a redshift when there are only one or two features within a spectrum which can be associated with known emission lines.

The second example, the candidate for the central core of the radio source 4C16.49 (1732+160), is thought to be associated with an 18th magnitude stellar-like object (Laing et al., 1983). This is virtually confirmed as a QSO because of its strong ultraviolet continuum (Wills and Wills, 1976). From its apparent magnitude Laing et al. (1983) have estimated the redshift to be ~ 1.0. Mitton et al. (1977) have obtained a spectrum of the object and report the marginal detection of two emission lines at 4500 Å and 5480 Å. They identify these features with CIV (1549 Å) and [CIII] (1909 Å) from which they deduce a redshift $z = 1.88$, but conclude further observations to be essential.

FOS spectra of the object were obtained with two 1000 seconds exposures. The object was found to be fainter than $m_V = 18.4$ as reported by Mitton et al. (1977), its visual magnitude being estimated at $m_V \sim 19.5$ from the Cassegrain TV acquisition system. The data, as outlined below, are shown in Figure 8.19.

Figure 8.19a	non-fluxed sky-subtracted spectrum obtained from the first exposure.
Figure 8.19b	fluxed spectrum of Figure 8.19a.
Figure 8.19c	non-fluxed sky-subtracted spectrum obtained from the second exposure.
Figure 8.19d	fluxed spectrum of Figure 8.19c.
Figure 8.19e	non-fluxed sky-subtracted spectrum obtained by adding the data from the two exposures, after sky subtraction, but before flux calibration.
Figure 8.19f	fluxed spectrum of Figure 8.19e.

Examination of the final spectrum (Figure 8.19e) shows a broad emission feature centred around 6450 Å. The tentative association of this feature with MgII (2798 Å) yields a redshift $z = 1.31$.

Ideally, one would like to be able to identify other features within the spectrum to support the proposed redshift. The only other feature of any significance is that seen at 8600 Å which could be [OII] (3727 Å), this being consistent with the proposed redshift z = 1.31.

The emission line reported by Mitton et al. (1977) at 5480 Å is not evident, and their redshift of 1.88 would not result in any well known emission features appearing around 6450 Å. Their non-detection of the feature is somewhat surprising and may point to an unusual variability in the spectrum of this object.

More observations are essential to establish the redshift of this object with more certainty. In particular, a longer exposure to obtain a higher S/N is necessary if the proposed identification of [OII] is to be confirmed. Identifications of weaker emission features are also desirable, i.e. possibly [NeV] (3346 Å, 3426 Å), [NeIII] (3968 Å).

The ease with which a redshift can be determined from a low S/N spectrum therefore depends on how many features are visible.

Spectra similar to that of 4C14.27 are obviously easier to interpret than those like 4C16.49's with only one broad feature.

From the examples of active galactic nuclei spectra presented above, it is clear that FOS is well suited to the classification of objects with strong emission line features. In particular, FOS' wide wavelength coverage provides good probability for finding characteristic lines for these objects over a wide redshift spectrum.

PKS 2128−12

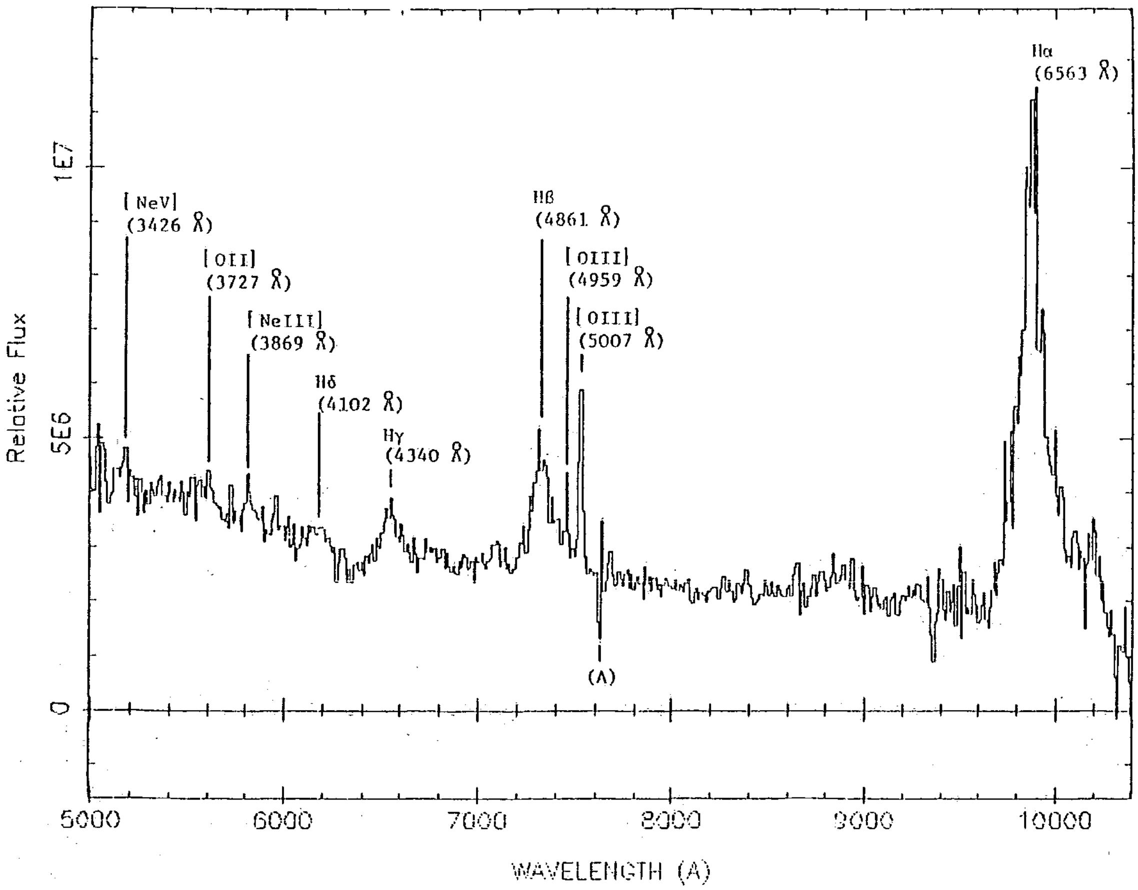


Figure 8.14

3C 380

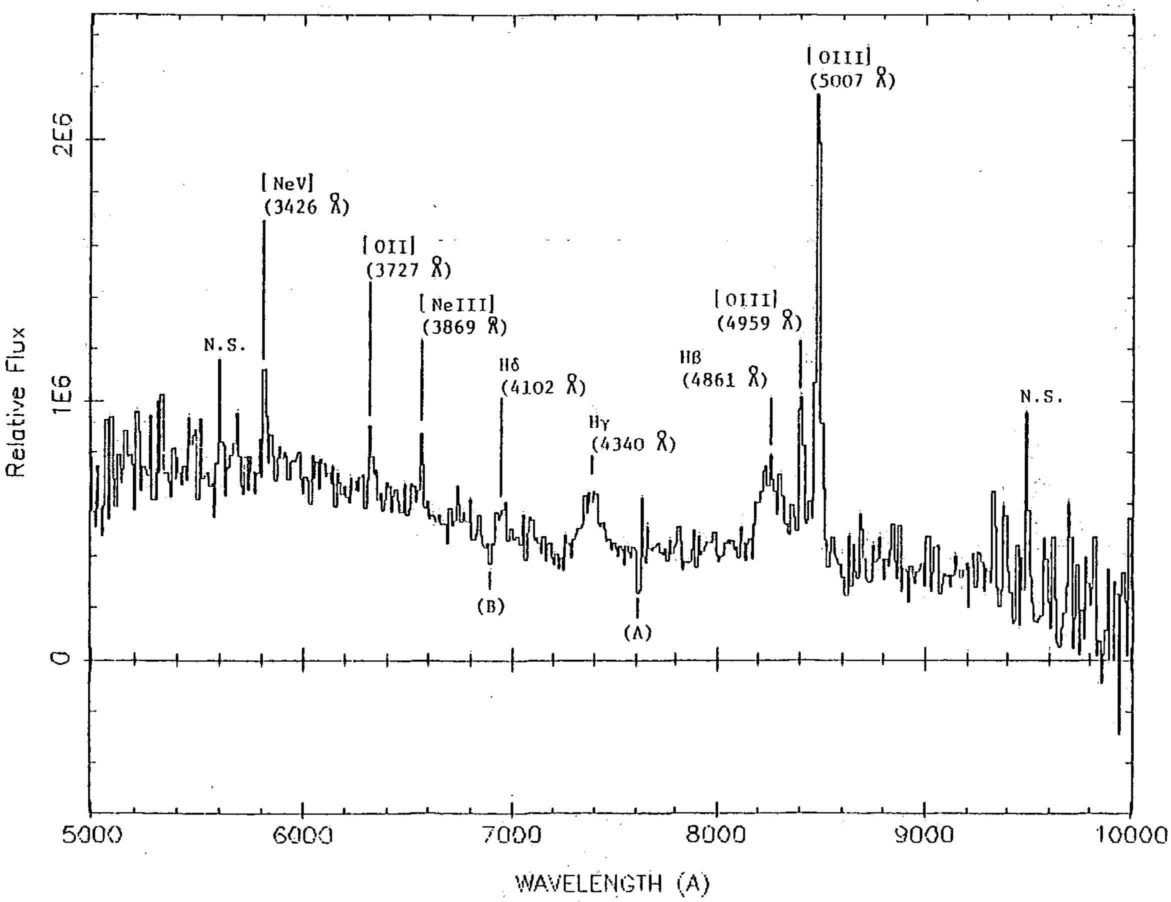


Figure 8.15

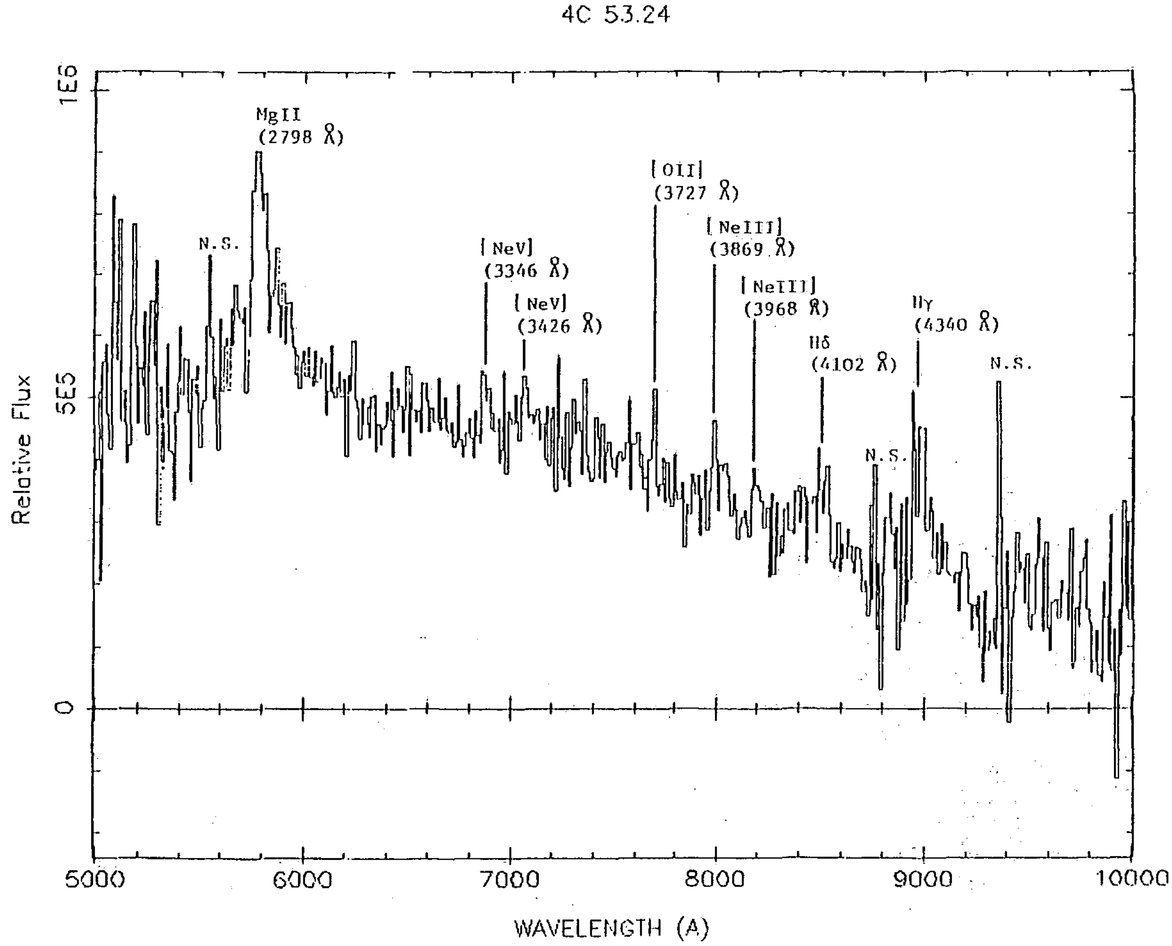


Figure 8.16

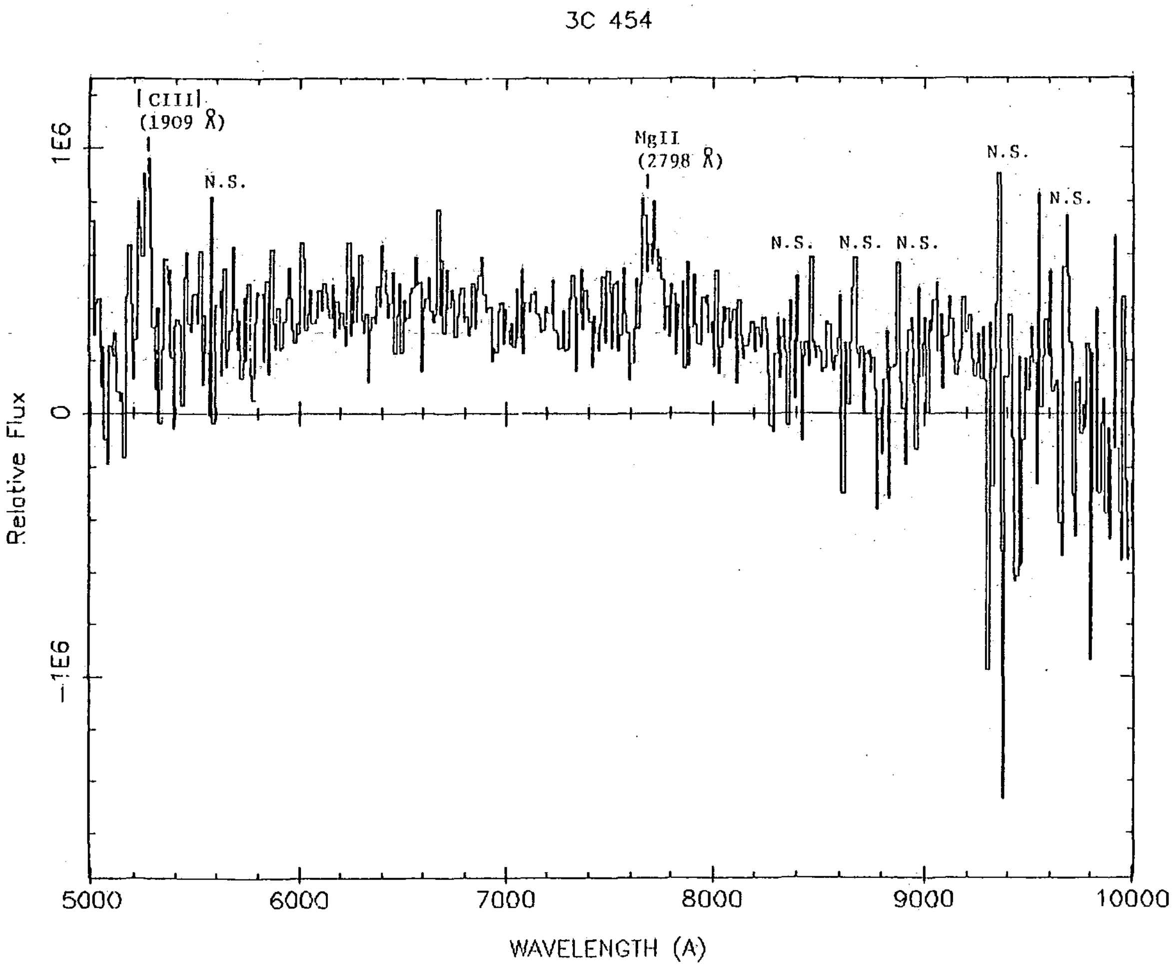


Figure 8.17

4C 14.27

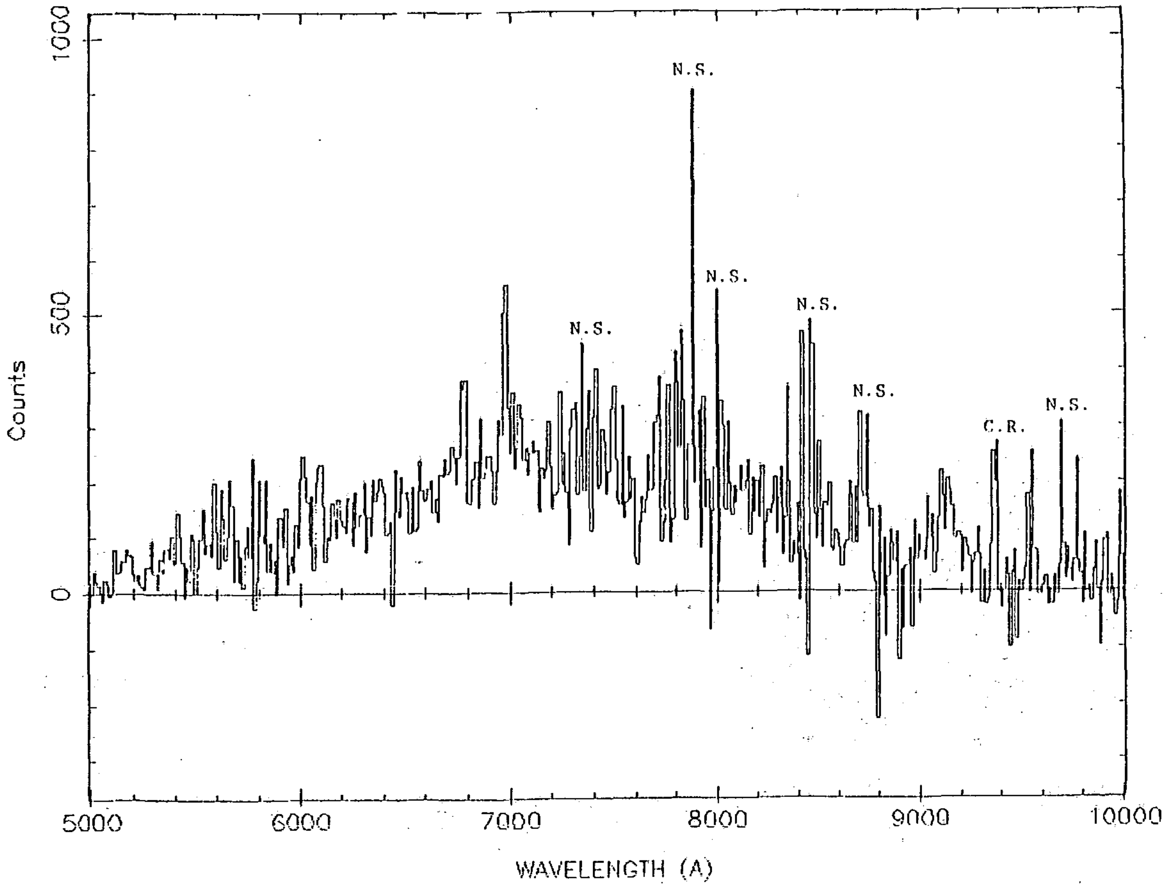


Figure 8.18a

4C 14.27 Sky

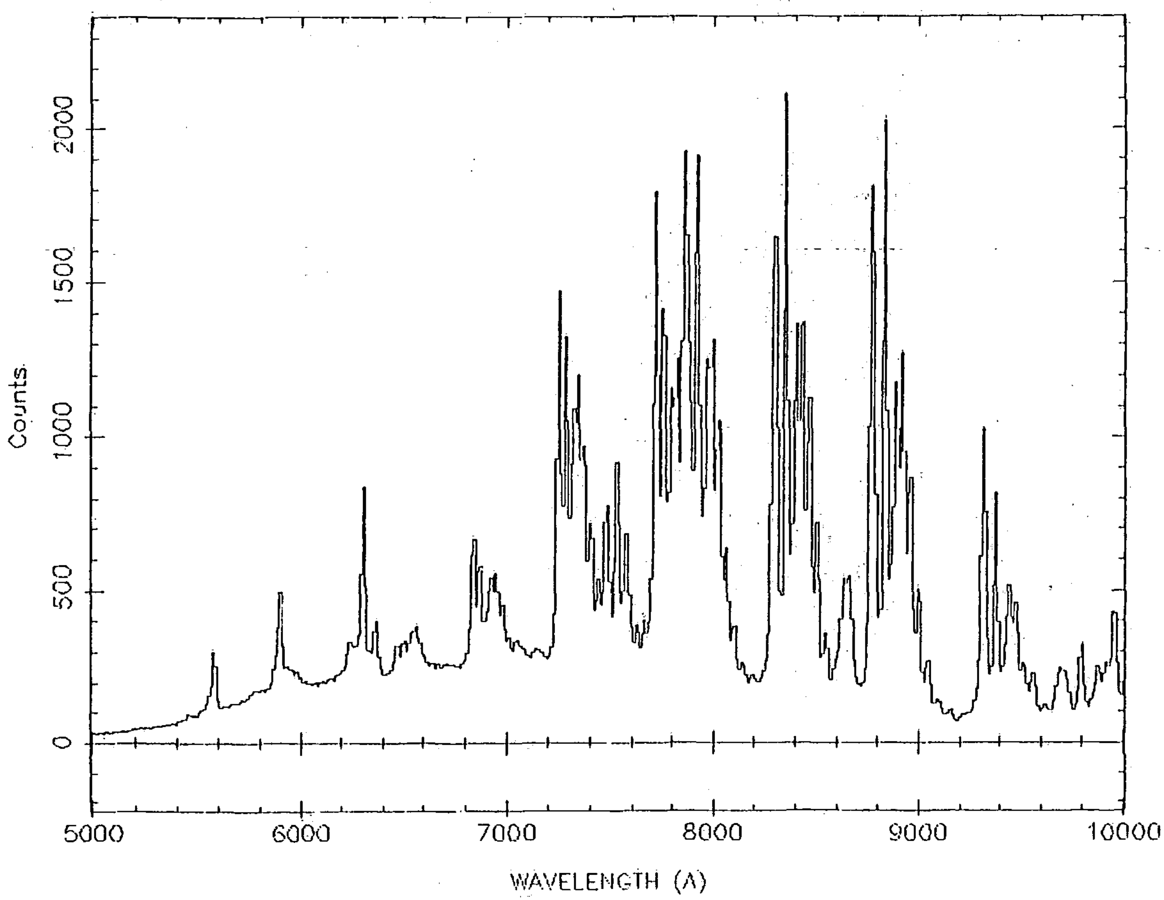


Figure 8.18b

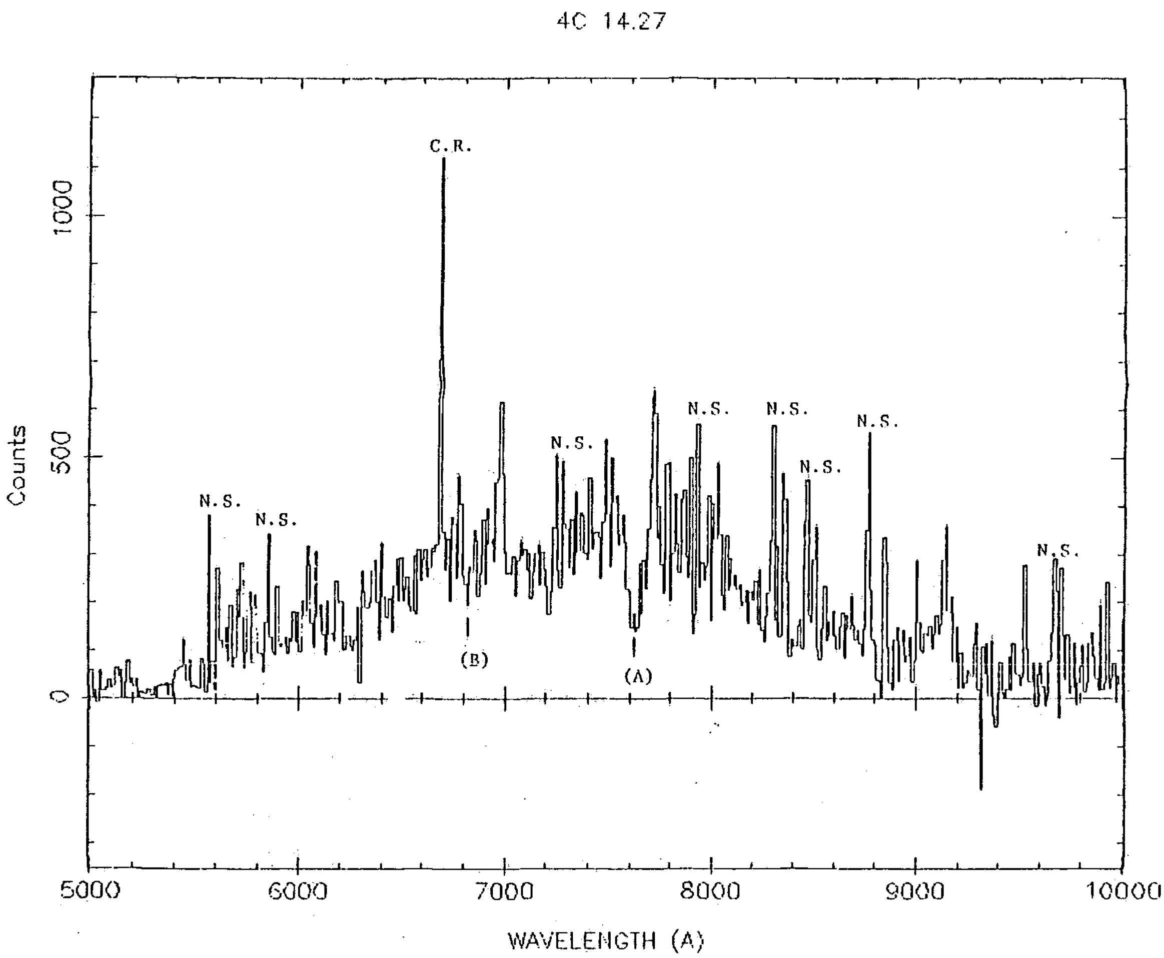


Figure 8.18c

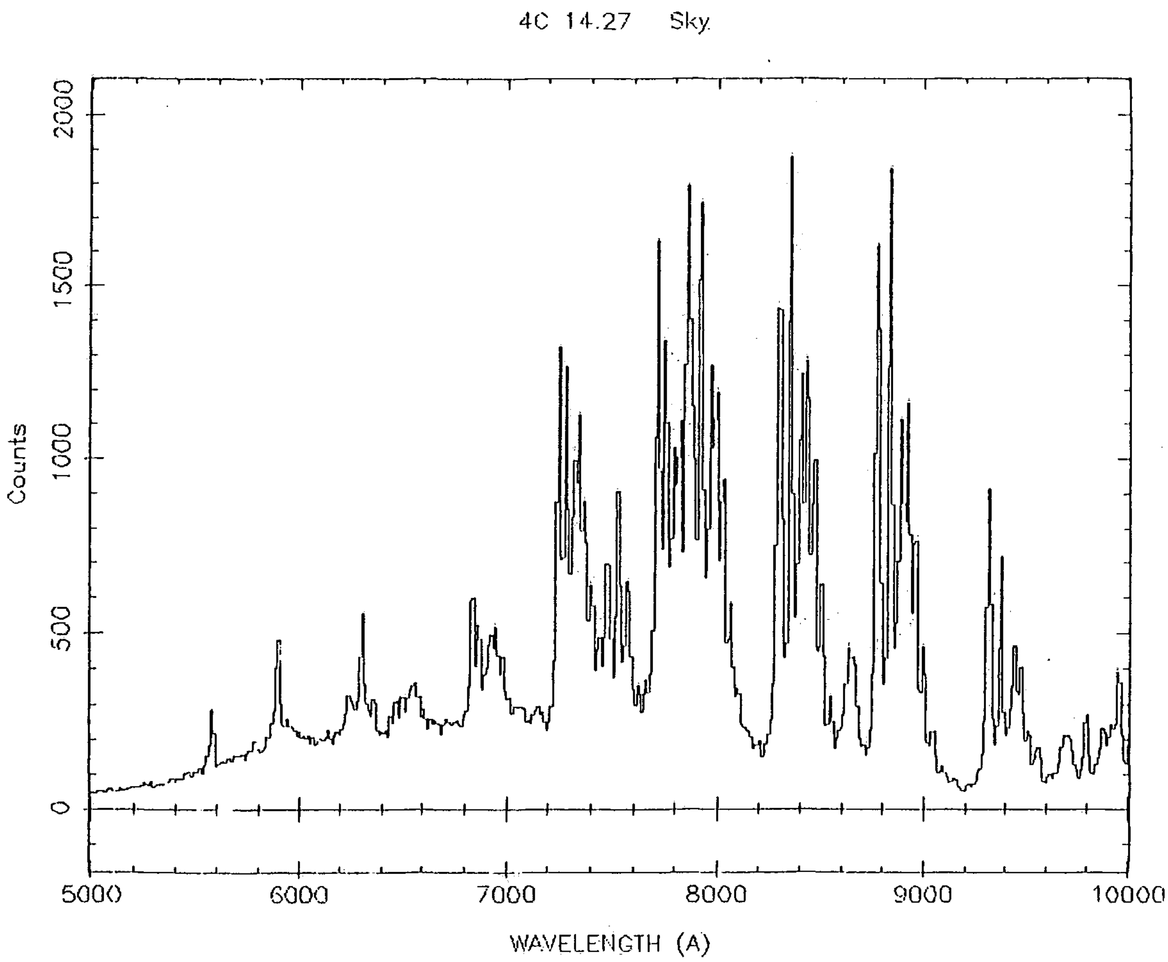


Figure 8.18d

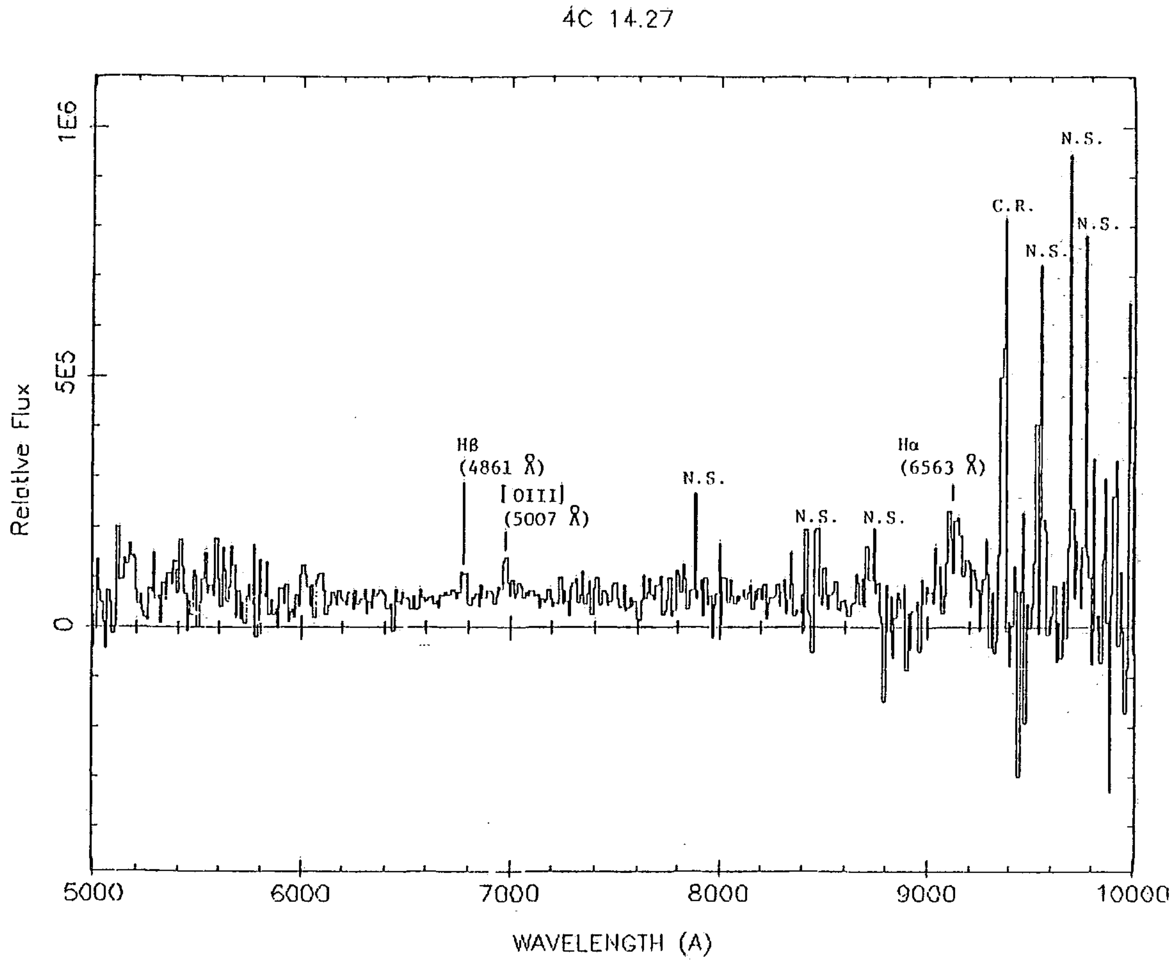


Figure 8.18e

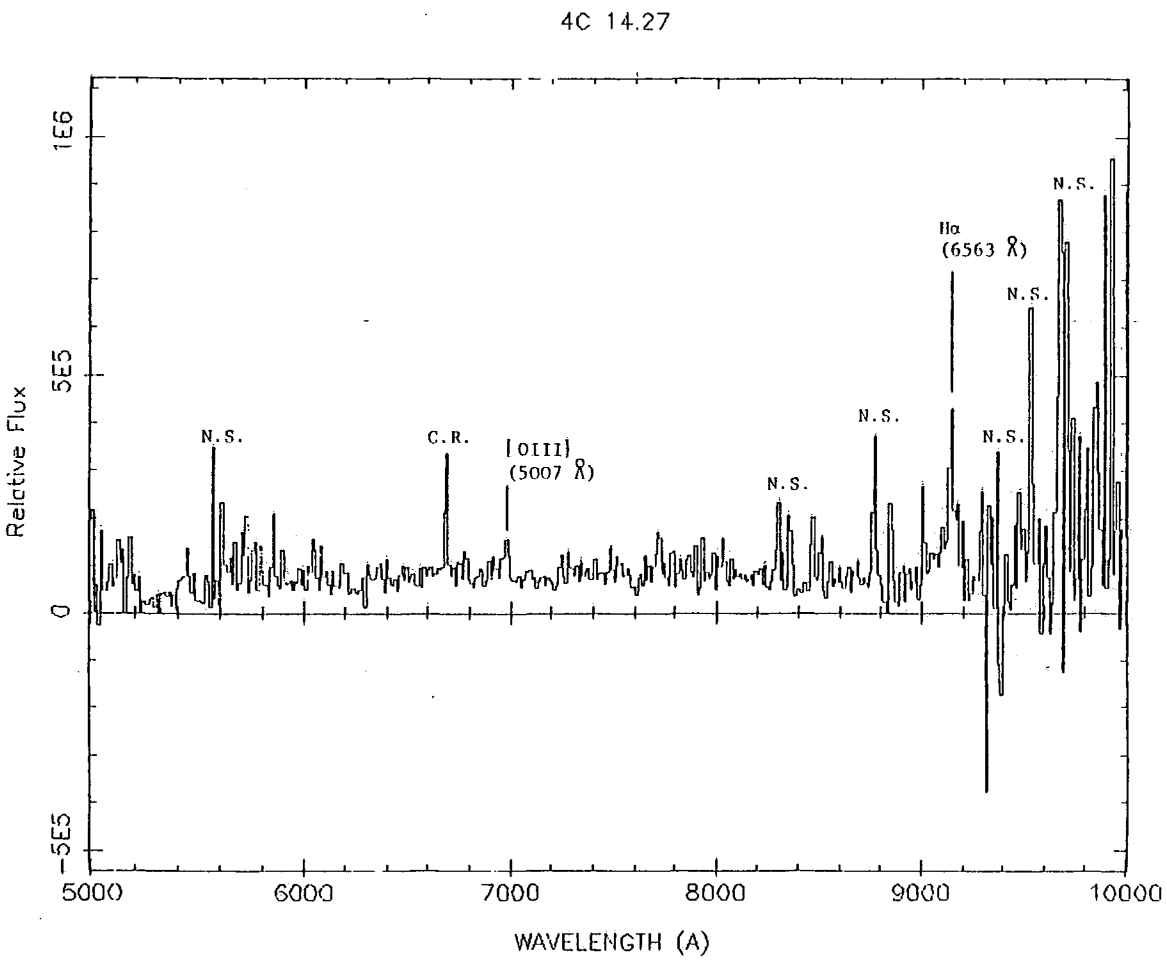


Figure 8.18f

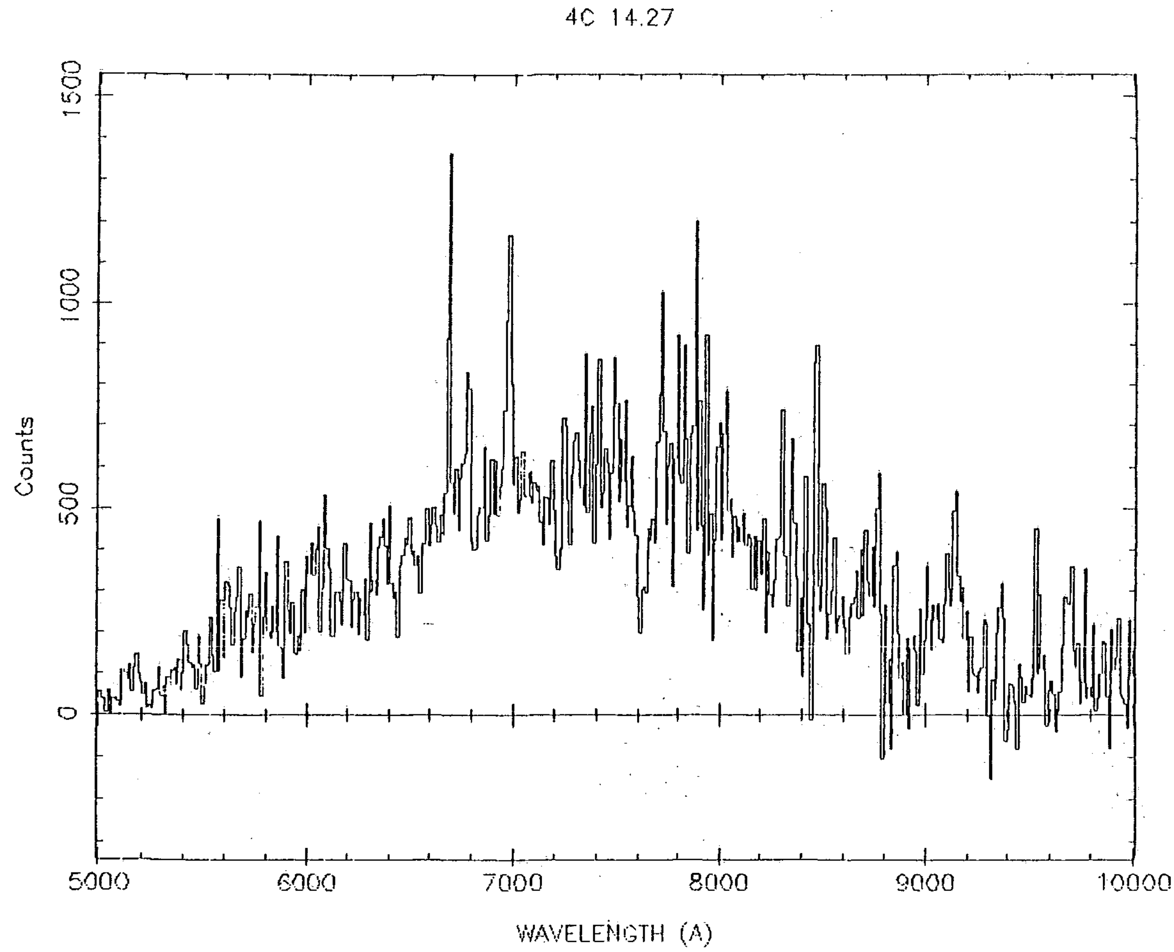


Figure 8.18g

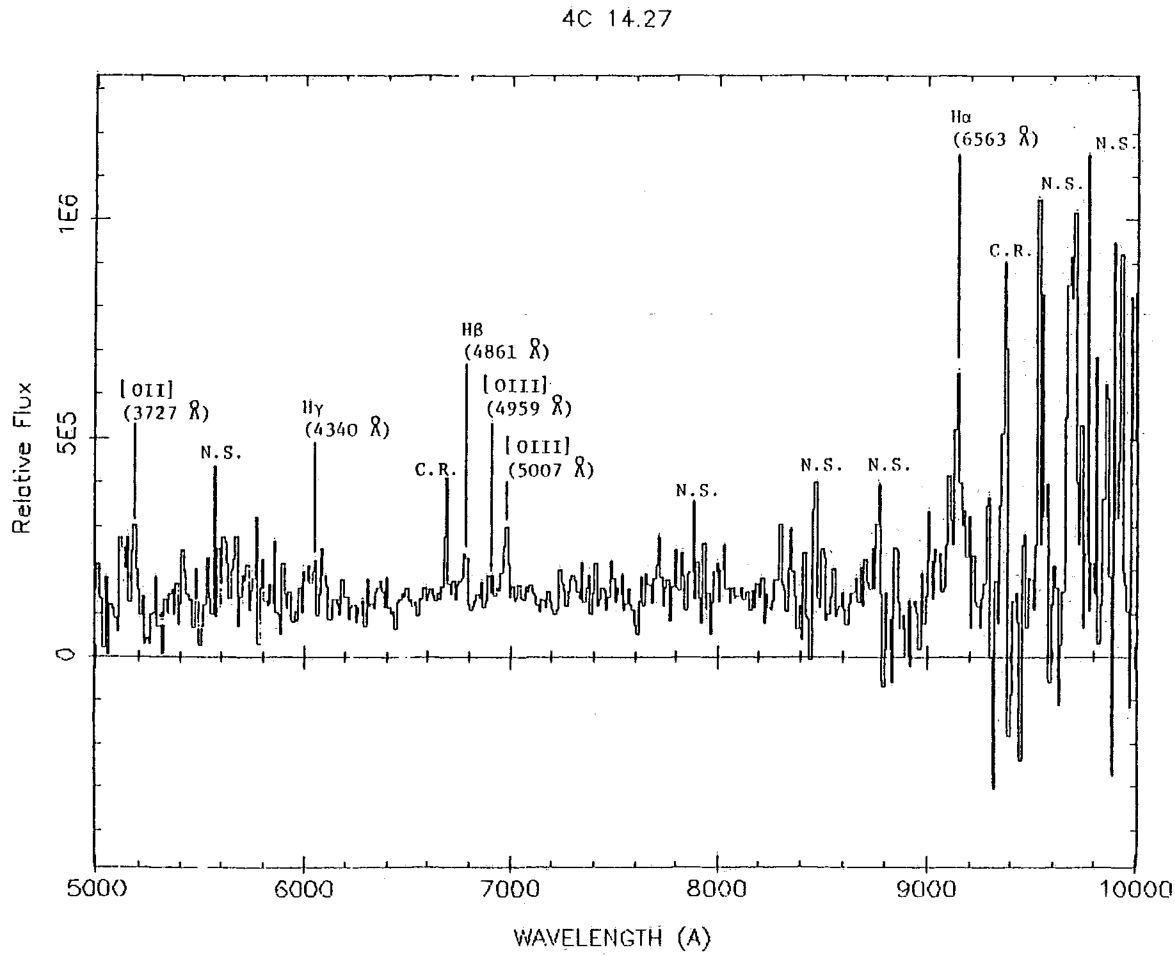


Figure 8.18h

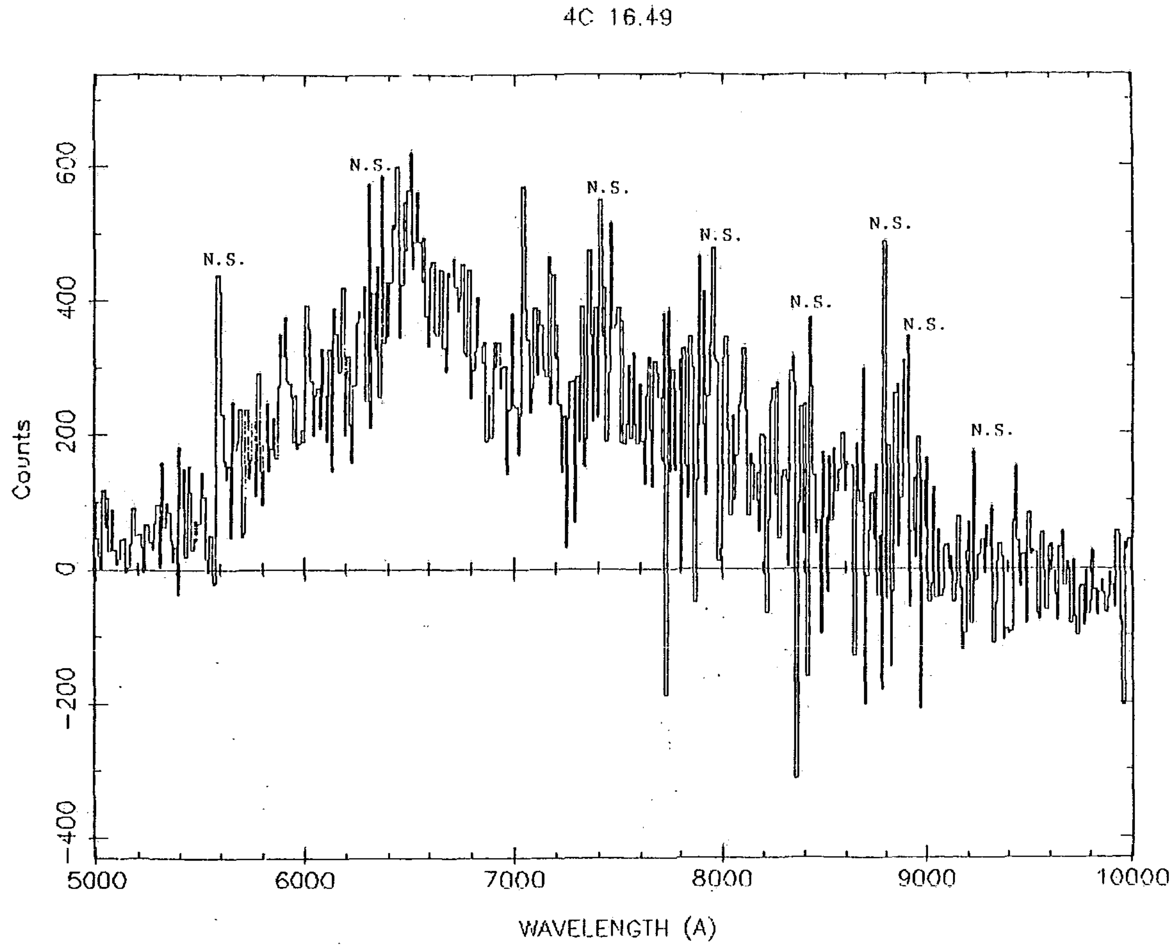


Figure 8.19a

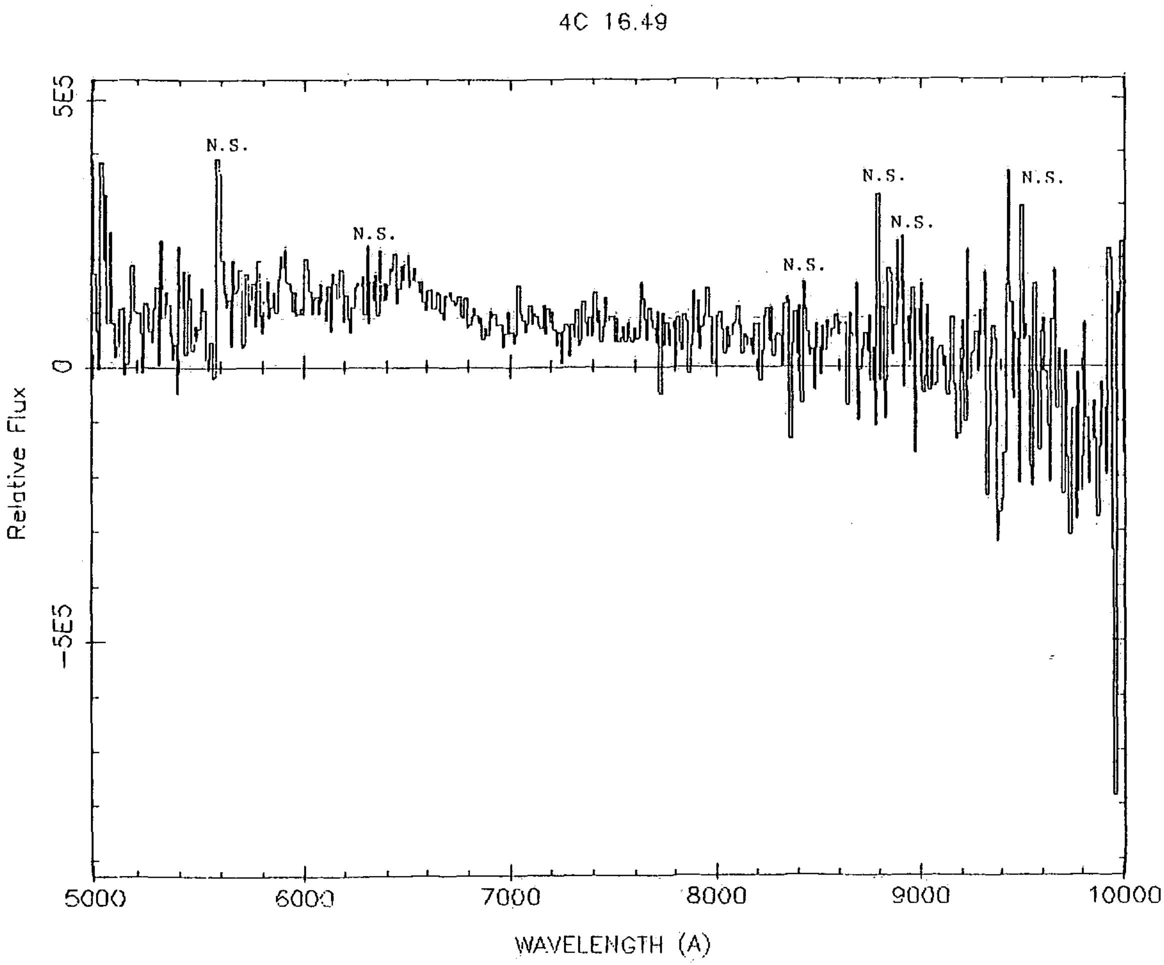


Figure 8.19b

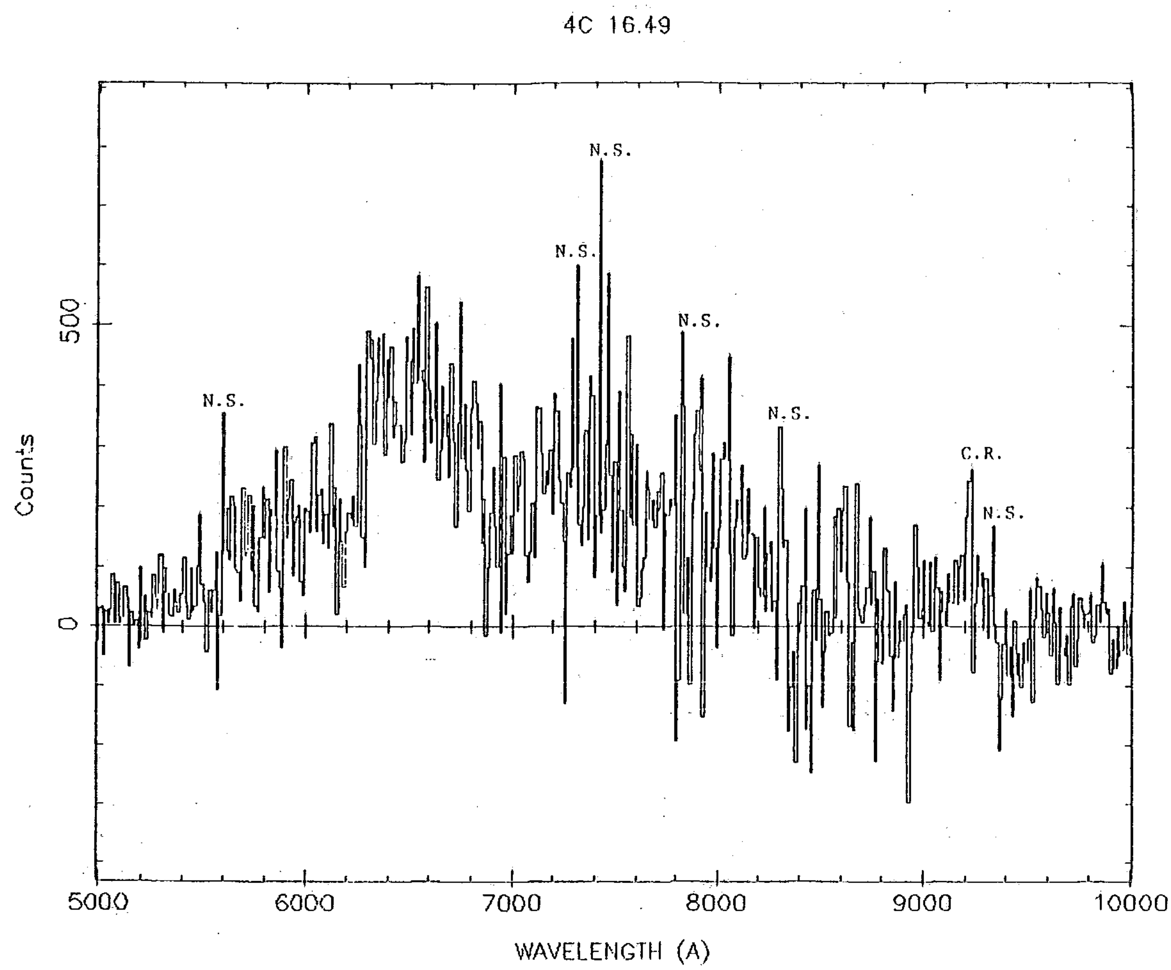


Figure 8.19c

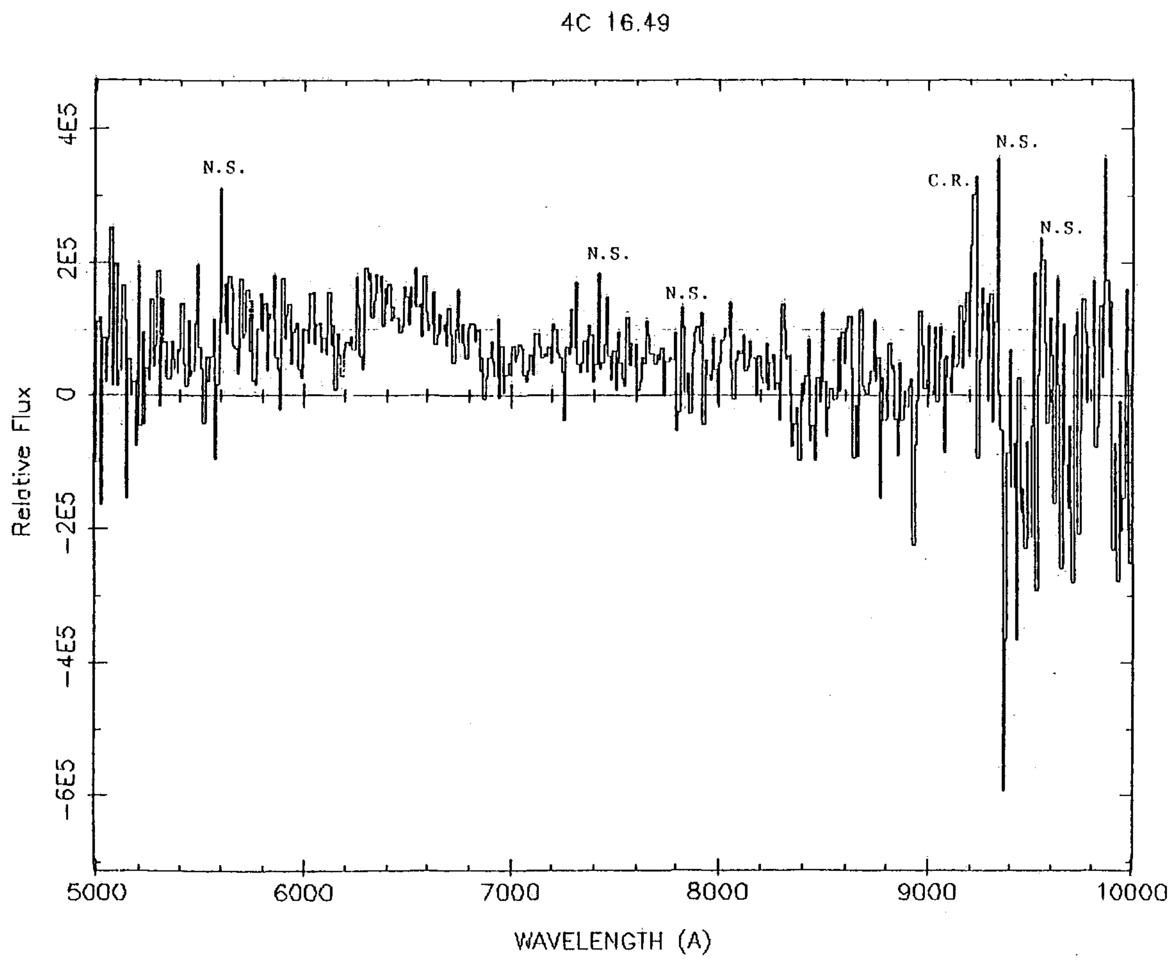


Figure 8.19d

4C 16.49

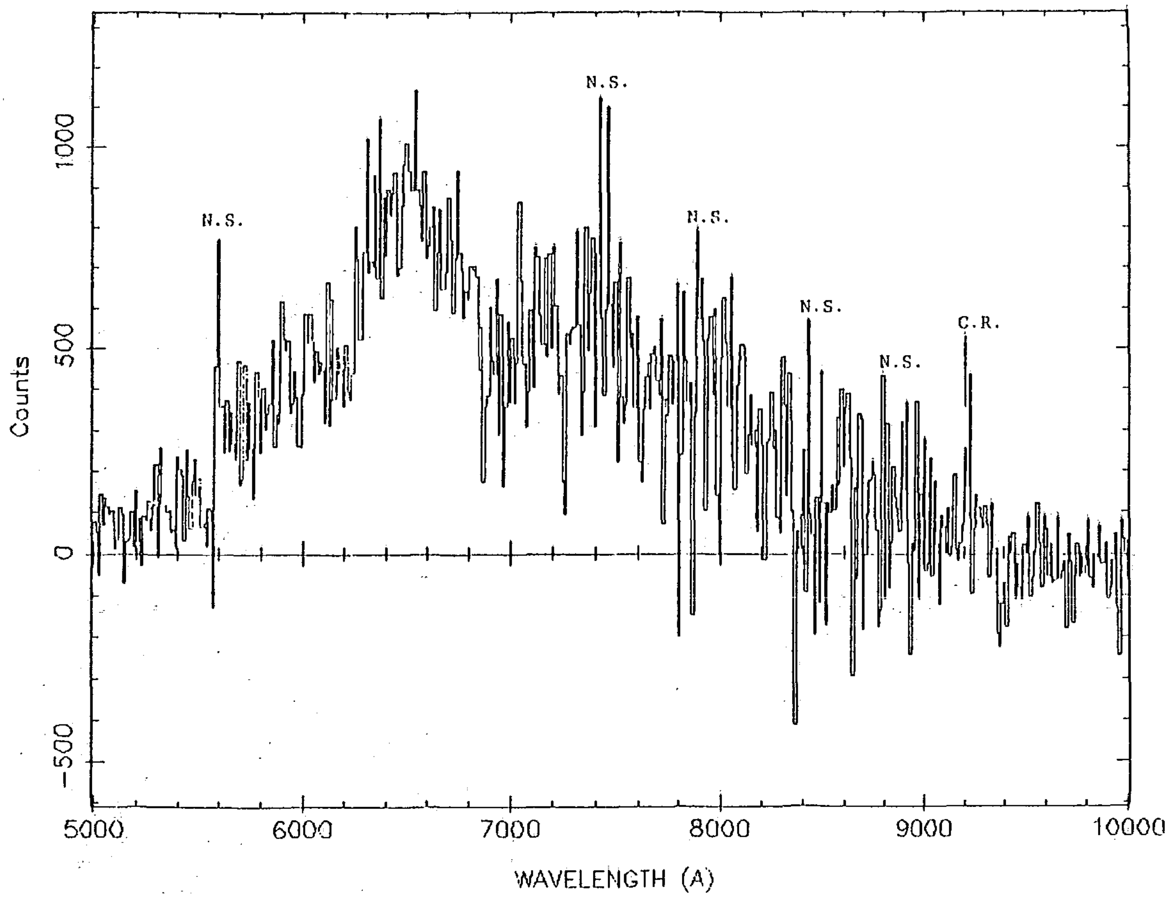


Figure 8.19e

4C 16.49

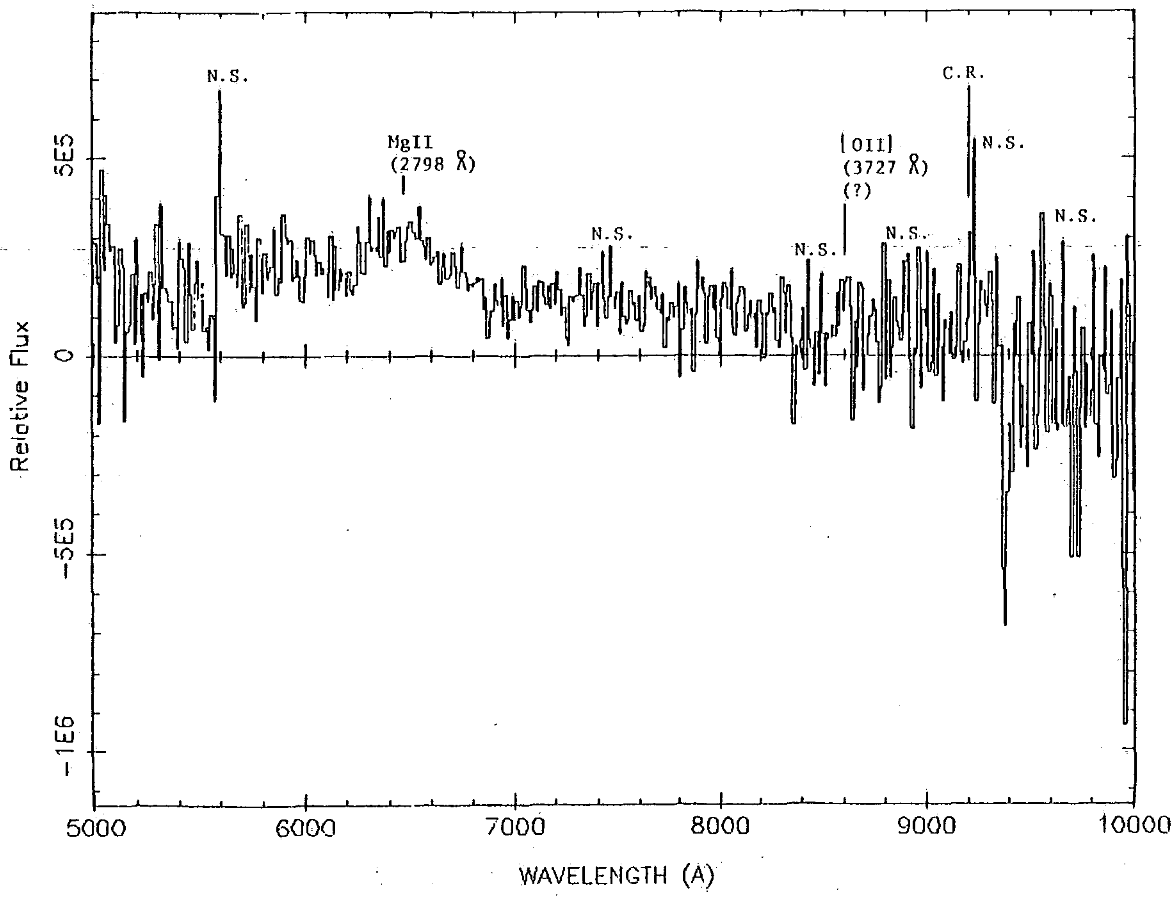


Figure 8.19f

8.6 Comet Halley

Comet Halley, during its recent apparition, was first detected on the 16th October 1982 by D C Jewitt and G E Danielson using a Texas Instruments 800 x 800 pixel CCD on the 200 inch Hale Telescope at Palomar. At that time, and at a distance of 1600 million Kms (10.7 AU) from the Earth, P/Halley (1982i) was estimated to have a visual magnitude $m_V = 24$.

During FOS' second commissioning period in December 1984, 13 months before P/Halley's perihelion passage, an attempt was made to obtain a spectrum from which it was hoped that any activity from the comet might be identified, in particular molecular emission lines, attributable to the development of a gas coma. At this time the comet had a heliocentric distance r = 5.3 AU, and from its appearance on the INT's TV acquisition system, was estimated to have a visual magnitude fainter than $m_V = 20$.

Five 1000 seconds exposures were taken on the night of 27/28th December 1984 for which the weather conditions were poor, the seeing being estimated from the TV system at 2.4 arcsec.

The resultant non-fluxed sky-subtracted spectra and their corresponding sky spectra obtained from the five exposures are shown in Figures 8.20a to 8.20e. It is immediately clear that the spectra are of low S/N and polluted with sky-subtraction residuals.

In order to improve the S/N, the data from the five exposures were added together. The resulting non-fluxed sky-subtracted spectrum is shown in Figure 8.20f. The presence of residuals from the sky subtraction are now even more apparent.

Figure 8.20g shows the spectrum after flux calibration. It shows a reflected solar continuum. On first examination, it was thought that the emission line seen at 6300 Å could be attributed to [OI], thus providing some evidence for the presence of a gas coma. However, more careful inspection of the raw data revealed this to be the result of a cosmic ray event detected during the fourth exposure (Figure 8.20d). In fact, no emission features (lines or bands) arising from the comet have been positively identified.

The FOS data confirms the results of others who also attempted to obtain an early spectrum of Comet Halley.

Spectra obtained on the F L Whipple Observatory 4.5m Multiple-Mirror Telescope (MMT), the Kitt Peak National Observatory (KPNO) 4m telescope and the McDonald Observatory 2.7m telescope between September 1984 and April 1985 have been reported in the International Halley Watch (IHW) Newsletter No. 7 (Wyckoff and Wehinger, 1985). Spectra obtained before 1985 are all reported to show only a reflected solar continuum. The first evidence of a gas coma was found by Wyckoff et al. (1985) on the 17th February 1985 when CN (3883 Å) emission was observed using a photon-counting intensified reticon detector on the 4.5m MMT. H Spinrad is reported to have detected [OI] (6300 Å) emission at the same time using the KPNO 4m telescope.

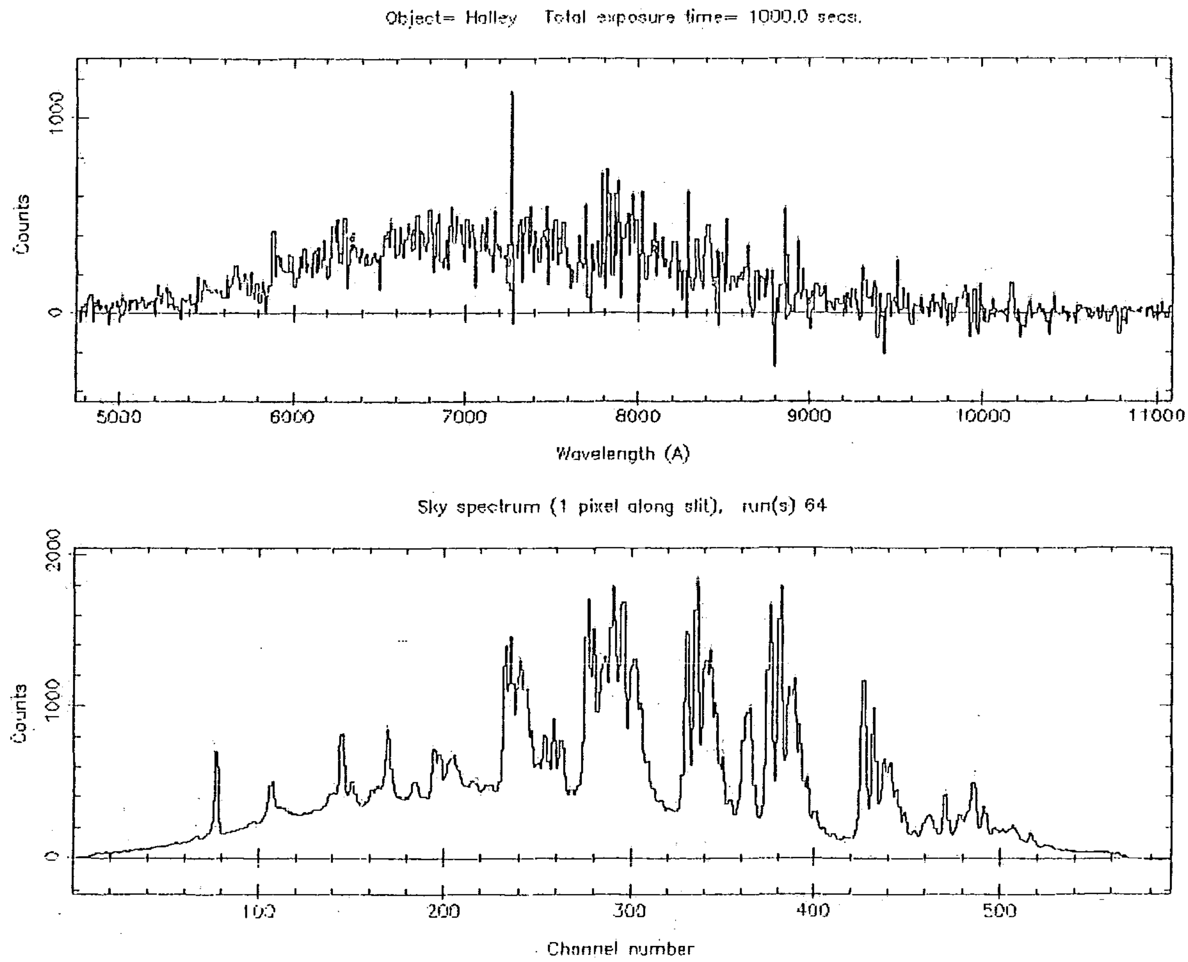


Figure 8.20a

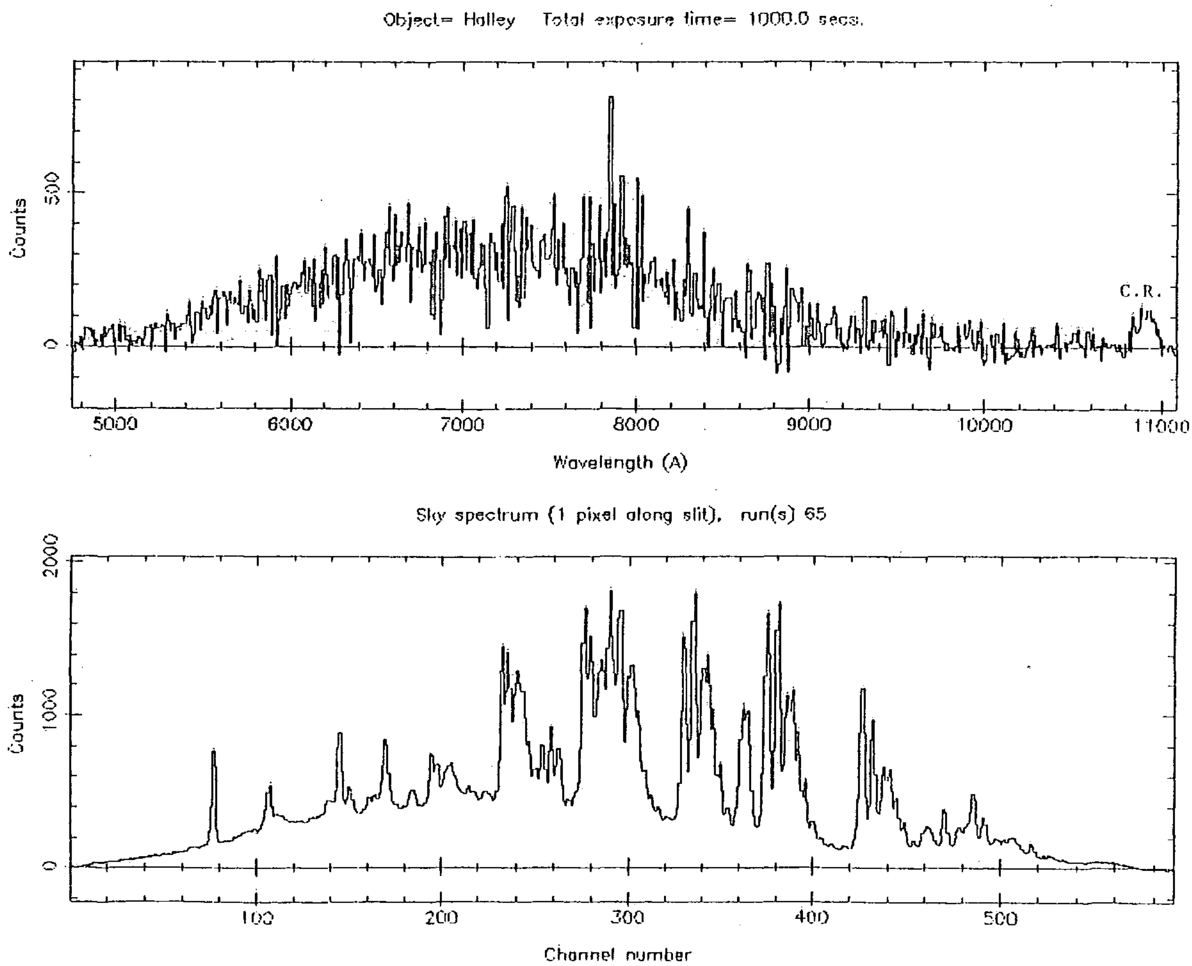


Figure 8.20b

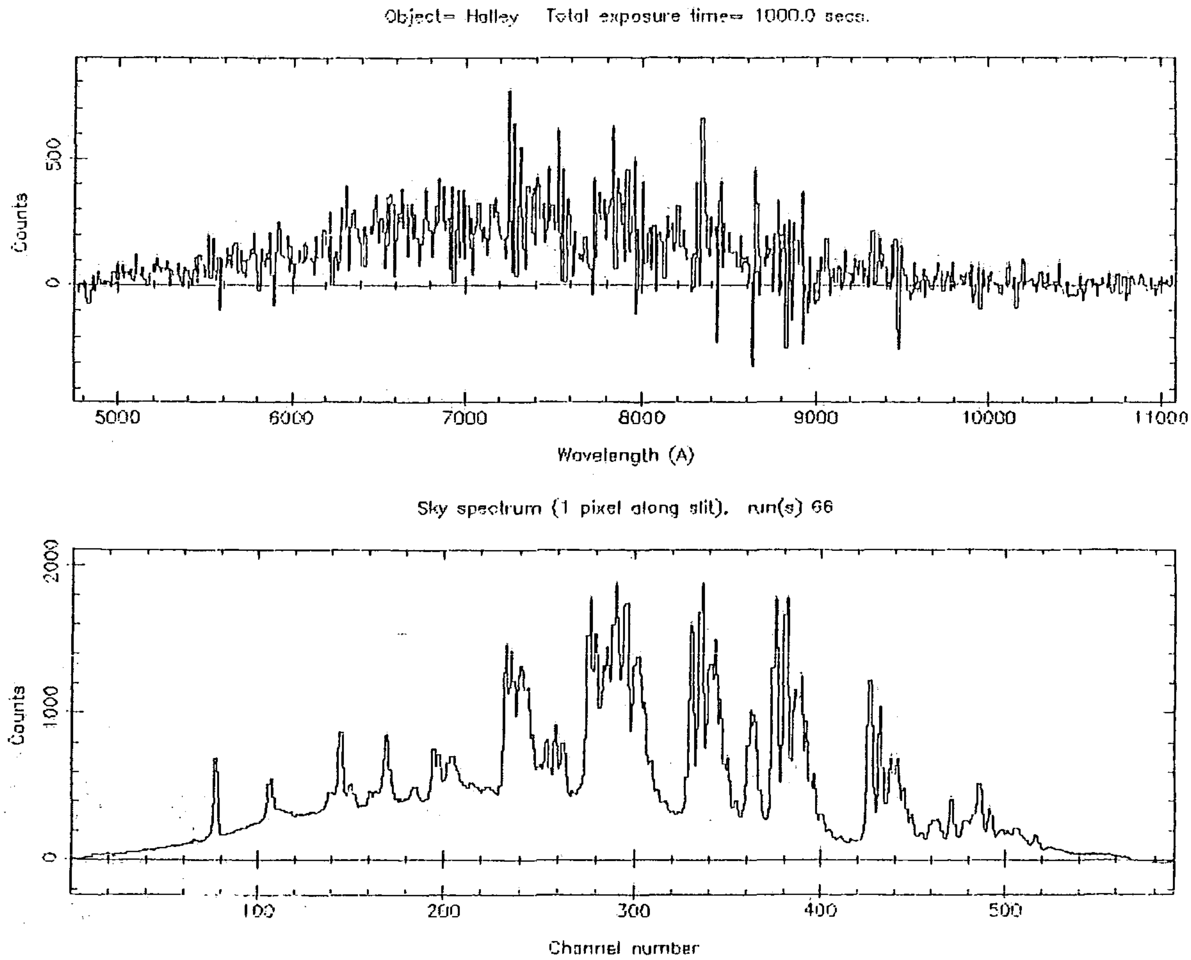


Figure 8.20c

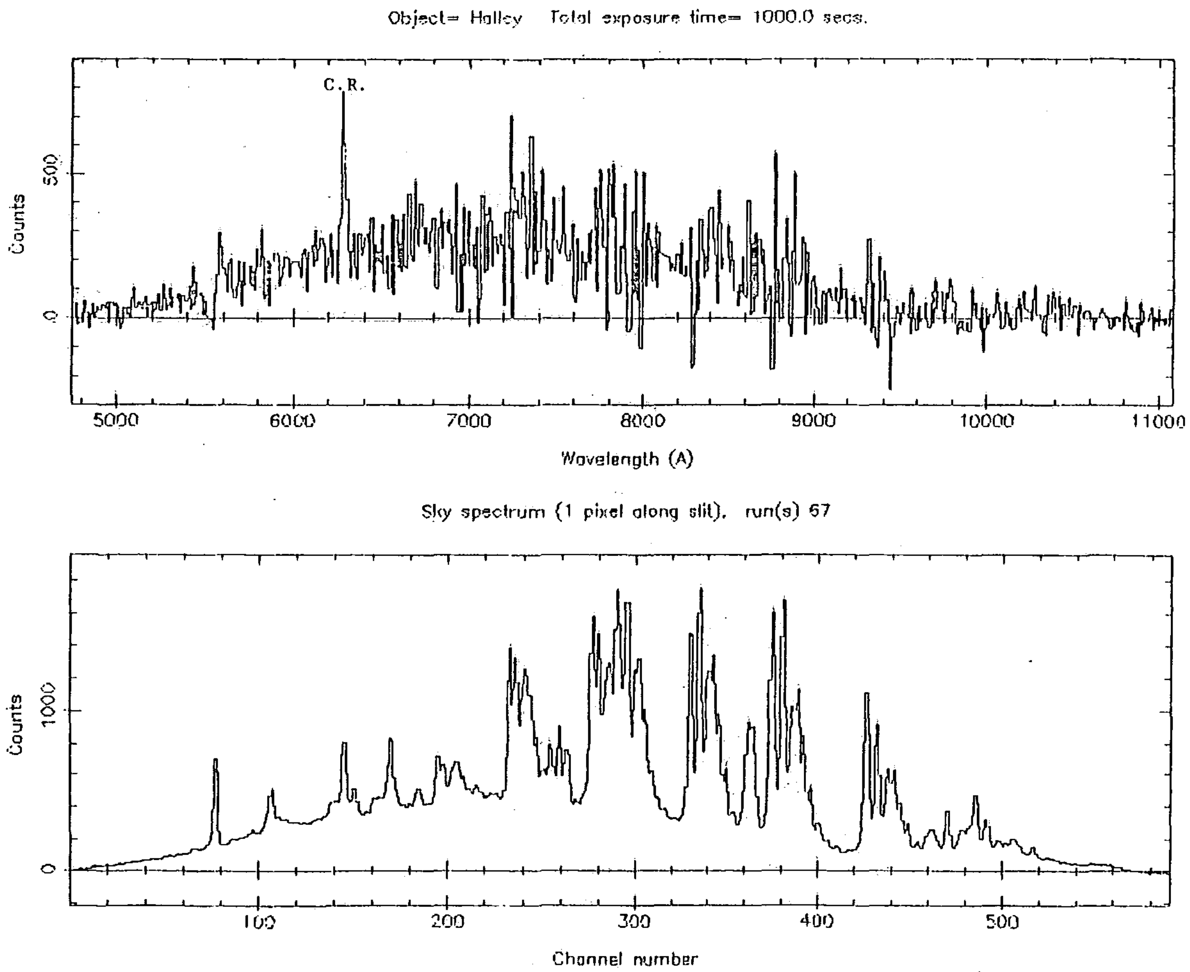


Figure 8.20d

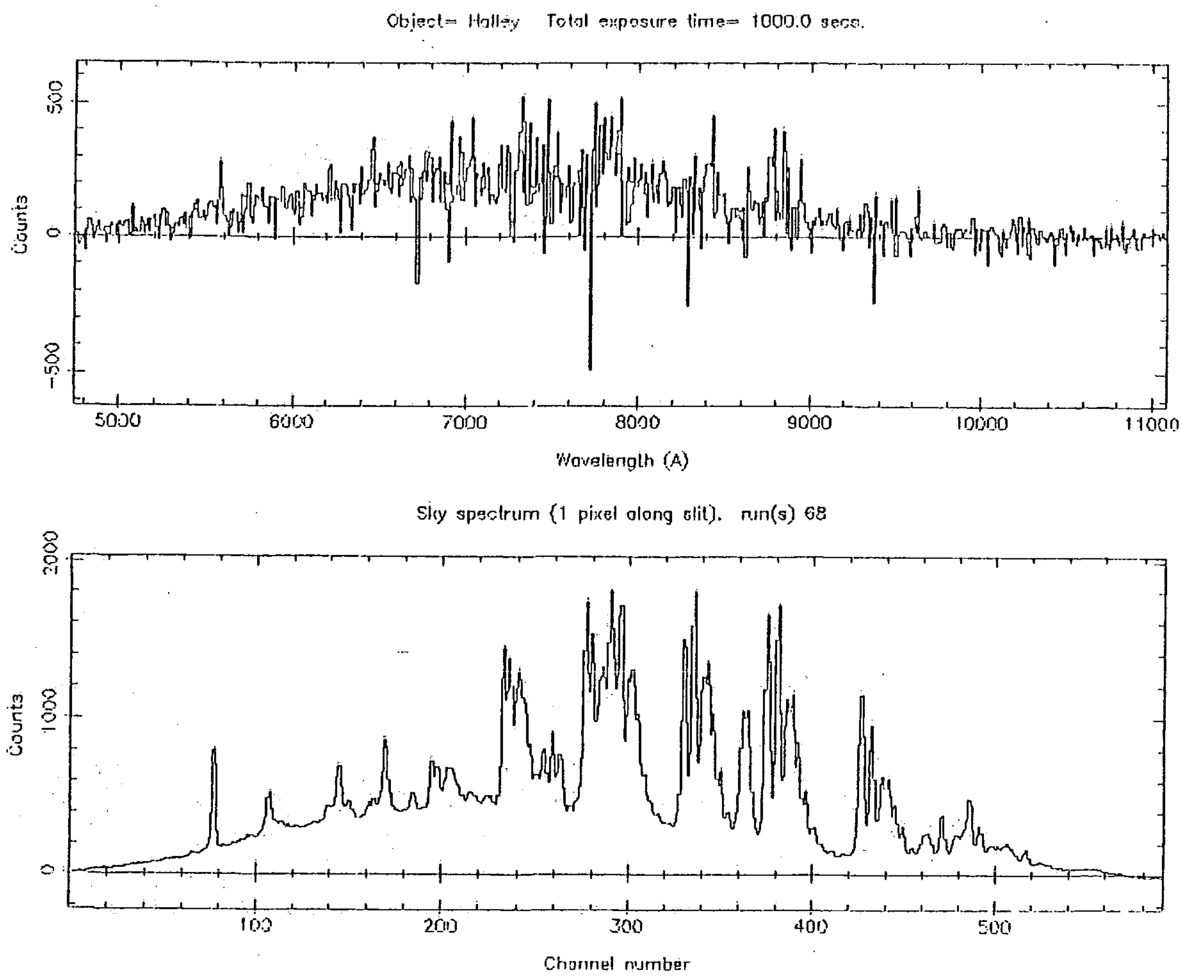


Figure 8.20e

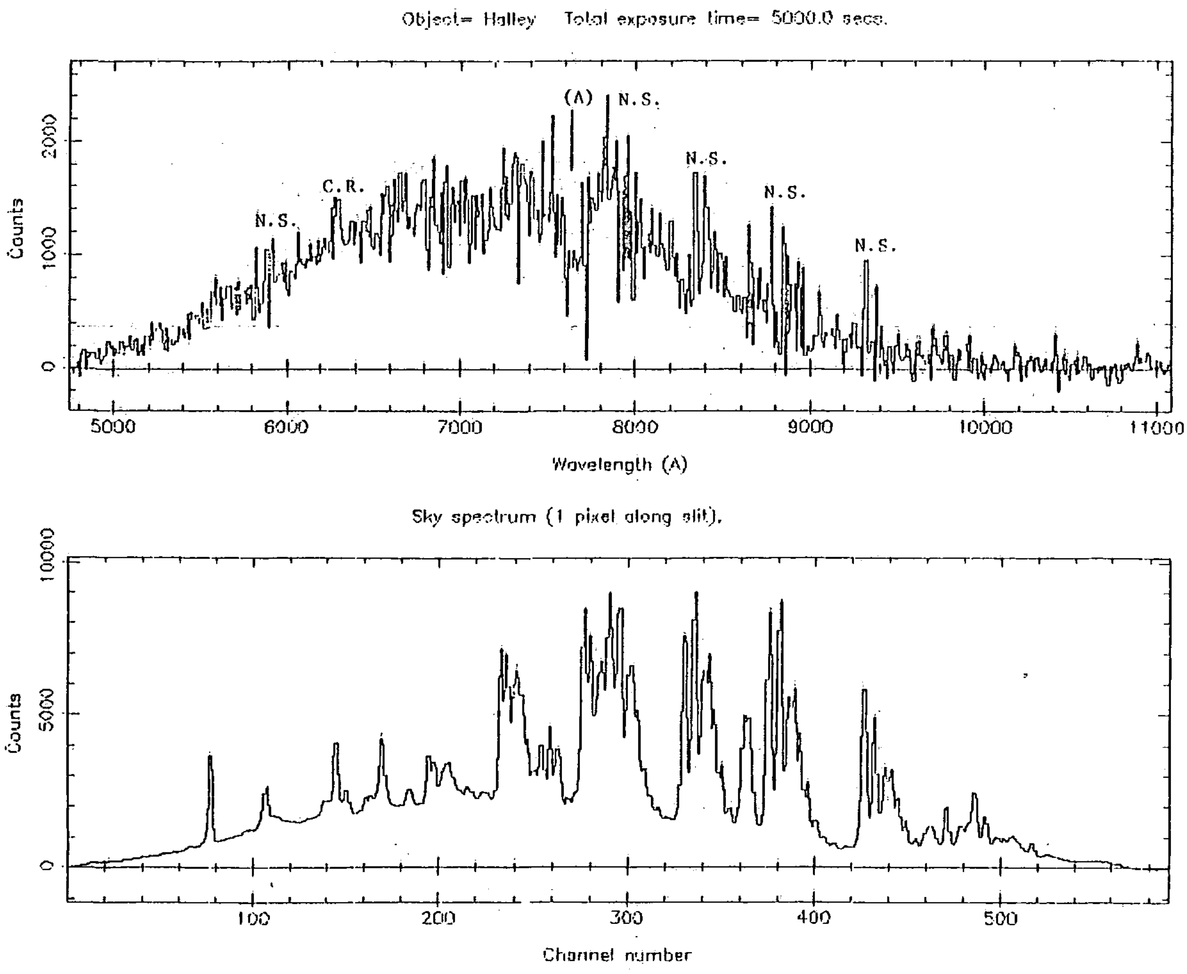
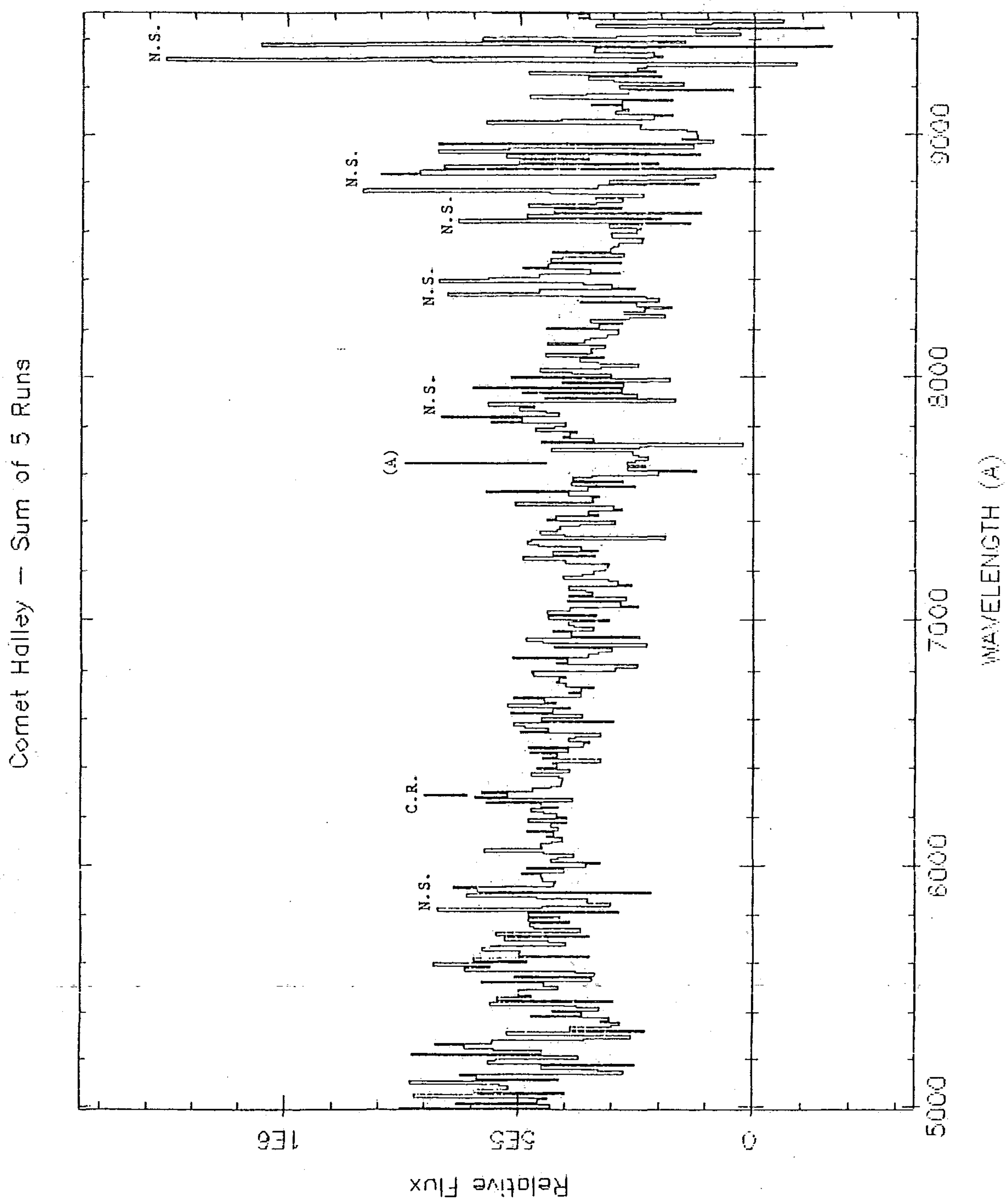


Figure 8.20f



Comet Halley — Sum of 5 Runs
Relative Flux
0
5E5
1E6
WAVELENGTH (A)
5000
6000
7000
8000
9000
N.S.
C.R.
(A)

Figure 8.20g

8.7 Discussion and Conclusions

FOS' wide wavelength coverage and its high throughput clearly make it a useful instrument for classification work and for determining the redshifts of faint extragalactic objects. It is worthwhile summarizing the types of objects which are most suited for investigation, and making some estimate of the limiting magnitudes for these objects for a given exposure time.

FOS' low dispersion makes it most applicable to objects with strong features. Weak features with widths less than 10-15 Å will not be seen easily until the continuum S/N (after sky subtraction) is good because of the difficulty of distinguishing real features from pixel to pixel noise. Broad emission line active galactic nuclei (radio galaxies, QSOs, for example), and galaxies with strong absorption features (e.g. G-band, CaII K and H), are thus appropriate targets.

Absorption line objects will generally require a higher continuum S/N to determine a redshift compared to emission line objects. Emission features, because they stand out above a noisy, sky-subtracted continuum, are easier to see than absorption features which, unless they are strong, tend to be hidden amongst the continuum noise.

Results obtained during commissioning suggest that sufficient S/N to determine a redshift can be obtained in a 1000 seconds exposure for:

(i) most objects with strong emission features (e.g. H-alpha, [OIII] and H-beta, MgII) which are brighter than $m_V = 19.5$.

(ii) objects with strong absorption features (e.g. G-band, CaII K and H) which are brighter than $m_V = 19$.

Exposures longer than 1000 seconds will generally be necessary to obtain a redshift from objects fainter than $m_V = 19.5$, although the limiting magnitude obviously depends on the number of visible features and their strengths.

FOS' limiting magnitude is in fact largely dictated by sky subtraction problems. Spectra from objects fainter than m_V = 18 become increasingly polluted with residuals of the night sky emission lines and in particular the OH emission bands present at wavelengths greater than 6800 Å. The problem arises because of poor charge transfer efficiency at low signal levels in this particular CCD, causing the sky emission lines within the object+sky and sky spectra to be smeared by slightly different amounts. Subsequent sky subtraction leaves ´spikes´ within the data which mask weak features and therefore hinder the interpretation.

So far little has been said about FOS´ second order; indeed only one second order spectrum has been presented, that being from a bright (m_V = 12) galaxy. FOS´ second order responsivity is low compared to that of its first order (see Chapter 7, Figure 7.6), and so for the fainter objects observed during commissioning, there was insufficient signal to make the reduction of the data worthwhile. It should be noted, however, that there are features which could be seen in second order which would prove useful identifications for redshift determination (e.g. CaII K and H for low ($z < 0.25$) redshift galaxies). FOS would therefore benefit from having a blue sensitive CCD, particularly since there are fewer problems with sky subtraction at wavelengths less than 6800 Å.

CHAPTER 9

CONCLUSIONS

9.1 Introduction

The last chapter of this thesis summarizes the achievements of the 2.5m Faint Object Spectrograph, examines the limitations of the instrument, and assesses where progress is likely to be made in the future with regard to instrumentation for faint object spectroscopy.

9.2 The 2.5m Faint Object Spectrograph

The development of the 2.5m FOS has provided the LPO with a more efficient means of classifying and determining the redshifts of faint extragalactic objects. In terms of its throughput, FOS is approximately 2 to 3 times faster than the INT's Intermediate Dispersion Spectrograph working at its lowest resolution and with a similar GEC P8603 CCD detector.

The spectrograph is most suited to the investigation of broad emission line objects such as active galactic nuclei and absorption line objects with strong features (e.g. galaxies with G-band, CaII K and H absorption). Objects with only weak absorption features will generally require a higher continuum S/N to identify features hidden amongst the sky-subtracted continuum pixel to pixel noise.

In good conditions (~ 1 arcsec seeing), an exposure of 1000 seconds will usually be sufficient to obtain an adequate S/N for determining a redshift to $m_V = 19.5$ for emission line objects and $m_V = 19$ for absorption line objects.

In order to illustrate the types and diversity of research programmes to which FOS has been applied since it became a common-user instrument, Table 9.1 lists the PATT (Panel for the Allocation of Telescope Time) allocations over the period May 1985 to January 1987 for which the use of FOS has been requested.

Table 9.1 REQUESTS FOR FOS - MAY 1985 TO JANUARY 1987 PATT ALLOCATIONS

- Space distribution of radio quasars over large ranges of log Prad and redshift (Katgert, Leiden - 4 separate observing runs).
- Low resolution spectroscopy of a complete sample of IRAS galaxies (Rowan-Robinson, Lawrence, QMC - 3 separate observing runs).
- Composition of large planetary nebulae (Mampaso, IAC).
- Filaments in the large scale structure of the universe (Smith, Sussex).
- Spectra of globular clusters and other galaxies (Martinez, IAC).
- Physical studies of the interstellar medium (Alvarez, IAC).
- Search for hidden energy in quasar spectra (Beckman, IAC).
- Probing Seyfert I nuclei over a large wavelength region (Prieto, Vilspa).
- Optical identification content of the Eridanus Deep X-ray Survey (Murdin, RGO).
- Redshifts of '1 Jansky' radio sources (Allington-Smith, UCL).
- A new search for primaeval galaxies (Ellis, Durham).
- Faint active-galaxy populations from the IRAS deep fields (Keel, Leiden).
- Horizontal branch stars in globular clusters (Mocoroa, IAC).
- Supergiants towards the galactic centre (Prieto, IAC).
- Detection of dust discs round Vega type stars (Lazaro, IAC).
- Further studies of cooling flows in nearby and distant galaxies (Fabian, Cambridge).
- Velocity structure of supernova ejecta in Cassiopeia A (Winkler, Cambridge).
- Spectroscopic study of quasars (Kidger, IAC).
- Simultaneous optical and infrared emission line observations of bright low redshift quasars (Yates, Edinburgh).

9.3 Limitations of the System

The main limitation of FOS is currently its particular CCD. There are two reasons for this:

(i) it has a threshold problem which gives rise to poor charge transfer efficiency at low signal levels. This results in severe smearing of emission line features (including night sky lines) which, in cases where the object signal is small in comparison to the sky background, leaves sky residuals in a sky-subtracted spectrum.

(ii) the (thick) GEC CCD has poor blue response which means that in many cases, FOS′ second order is largely wasted.

Solutions to each of these problems warrant discussion.

(i) A temporary solution to the threshold problem would be to install a preflash facility within the spectrograph camera to provide a background bias charge as discussed in Chapter 5. However, besides the fact that this would increase the readout noise, it would also present some practical problems. This is due to the difficulty of installing a system within the spectrograph camera to provide uniform illumination at the CCD. The best solution would be to have a diffuse source of illumination at the centre of the camera mirror. Some modifications to the camera would clearly be necessary. The longer term solution to the threshold problem is to find a better chip.

(ii) There are two ways in which the blue response of the CCD could be improved:

(a) fluorescent coating of the GEC CCD. This would improve the blue response of the system, increasing the CCD′s RQE to ~ 12% between 400 and 500 nm, but would not significantly affect its responsivity at wavelengths greater than 500 nm (see Chapter 5, Figure 5.1).

(b) installing a different, thinned, type of CCD. RCA's achievements with their thinned CCDs (see for example: Thorne et al., 1986a) demonstrate how a suitable device could increase the blue responsivity to 3-5 times that attainable from a coated GEC chip. Installing a different chip would of course necessitate remaking the CCD support block and modifying the electrical connections to the chip.

The argument in favour of using a better GEC chip is that it would require no hardware modifications to FOS, although re-focussing would be necessary. Against this is the lower improvement to the blue responsivity of the system compared to that expected from a thinned CCD, and the not insignificant problem of finding a suitable chip. The most variable aspects of GEC CCDs are their low level charge transfer efficiency and their cosmetic quality. What is required, therefore, is a chip which, assuming it to be typical with regard to its quantum efficiency and readout noise characteristics, satisfies the additional requirements that it:

(i) does not have a threshold.

(ii) is cosmetically acceptable.

However, experience suggests that such chips are a rarity and that the only way to find a suitable device is to have a large sample (perhaps as many as 10 to 20 chips) to choose from.

In an attempt to find a solution to the problem, the RGO, in October 1986, initiated an exercise designed to find several high quality astronomical-grade GEC CCDs for the LPO. Briefly, a contract was placed with EEV, the distributor of GEC CCDs, for 10 devices. EEV agreed to supply chips in batches of 10 from which the RGO would be allowed to make a final selection and return those devices deemed unsuitable, this process being repeated until 10 acceptable devices were found. A statistical assessment of the exercise is somewhat difficult, however, since of the first 18 chips to be tested, 3 were produced on EEV's new P8603 CCD production line at Chelmsford, while the remaining chips were among the last to be produced at GEC's Hirst Research Centre. Bearing this in mind:

(i) of the 3 EEV produced chips:
- all were found to have good low-level charge transfer efficiency.
- 2 chips were found to be cosmetically excellent, each chip having only 2 small trap defects.
- the third chip was found to possess 6 traps and a number of partial column defects in the lower half of the array.

(ii) of the 15 GEC produced chips:
- 7 were found to be good with respect to CTE, the others exhibiting some smearing of cosmic ray events.
- only 4 chips could be deemed to be cosmetically acceptable, but still inferior overall to the EEV produced chips.

Although this exercise is still to be completed, the initial conclusions are that there is a high probability that good quality GEC CCDs will be available in the future from EEV.

The alternative of using a different type of CCD has two main drawbacks:

(i) the hardware modifications required inside the spectrograph camera.

(ii) a thinned, low readout noise CCD is not currently available, although it is hoped that Tektronix and GEC will become new sources of supply in the future.

The announcement by Tektronix of their intention to make thinned, state-of-the-art CCDs (Blouke et al., 1985) has generated much interest within the astronomical community. However, like other manufacturers in the past, Tektronix have experienced production difficulties and as yet only a few chips have become available. Few details are known of the performance of these chips. Furthermore, one can expect that there will be some initial variation in the characteristics of the Tektronix CCD as the processing of the chips is refined.

GEC's programme to develop a thinned, back-illuminated version of their standard P8600 series CCD is a result of a contract placed in 1984 at the joint instigation of the RGO and the AAO. The project has been funded to cover an investigation of thinning techniques and the production of 12 working devices. Although some work is still to be done, it is hoped that the first prototype chips will be available for testing in late 1987.

Thus, although the availability of high quality, astronomical-grade CCDs is still far from satisfactory, efforts are underway to overcome the situation, and there is already some encouragement in the fact that the first GEC chips to be produced at EEV appear to be very good.

9.4 Future Developments

It is worth assessing where progress is likely to be made in the future in the development of instrumentation to increase the efficiency of faint object spectroscopy.

(i) optical efficiency of spectrograph systems

It would appear that there is little that can be done to increase the optical efficiency of spectrograph systems. FOS' design, as discussed in Chapter 1, has a minimum of optical surfaces which is the important factor in achieving high throughput over a wide spectral range.

(ii) CCD detectors

There is clearly still some room for improvement in the performance of CCD detectors. In terms of increasing observing efficiency, the important parameter of a CCD is its RQE. Increases of the order of 1 to 2 times (in the wavelength range 350-1100 nm) are being predicted for the future through advances in CCD thinning technologies (see for example: Janesick et al., 1984, Janesick et al., 1985, Janesick et al., 1986).

(iii) multi-object spectroscopy

The most significant gains in observing efficiency are undoubtedly those to be made by the development of multi-object spectroscopy techniques. The ability to record the spectra of many objects simultaneously has the potential for increasing observing efficiency by many times that which could ever be achieved by the development of better CCDs, perhaps by 2 to 3 orders of magnitude.

Techniques for obtaining spectral information from more than one object in a single exposure have been in existence for some time (Parry, 1986):

(i) slitless spectroscopy

(ii) narrow-band imaging

(iii) long-slit spectroscopy

However, current interest is focussed upon the development of multislit devices and fibre optic feeds to provide conventional spectrographs with a multi-object capability. These can yield tens of spectra at a time, thus offering considerable gains in observing efficiency, and hence equivalent savings in telescope time.

Multislit devices make use of an aperture plate, placed at the focal plane of the telescope, with precisely engineered slits that allow the light from the objects to enter the spectrograph (see for example: Butcher, 1982).

The use of fibre optic feeds for multi-object spectroscopy is now well established (Hill et al., 1980; Tubbs et al., 1982; Gray, 1983; Lund and Enard, 1983; Powell, 1983). Optical fibres positioned in the focal plane of the telescope, usually via a pre-drilled aperture plate, are fed to the entrance aperture of a spectrograph where they are arranged adjacent to each other in a line so as to form a pseudo slit.

The relative merits of multislit and fibre optic multi-object spectroscopy have been discussed in detail by Parry (1986). Examples of systems presently in use or under development are given below:

(i) the AAT's fibre optic coupled aperture plate (FOCAP) system (Gray, 1986) which consists of 50 fibres feeding from the Cassegrain focus to the slit of the RGO-AAT spectrograph.

(ii) AUTOFIB (Parry and Gray, 1986), an automated fibre optic coupler for the AAT to position 64 fibres in the field.

(iii) the Steward Observatory's MX spectrograph, an automated fibre optic coupler for positioning 32 fibres. (Hill et al., 1982; Hill and Lesser, 1986).

(iv) LDSS, the Low Dispersion Survey Spectrograph, a multislit aperture plate spectrograph designed specifically for multi-object, low-resolution spectroscopy, initially on the AAT and later on the LPO 4.2m telescope (Taylor, 1983).

(v) a fibre optic coupler (40 fibres) for the 1.2m UK Schmidt telescope (Watson, 1986).

9.4.1 Multi-Object Spectroscopy with FOS

One of the main objectives in developing FOS was to provide a means of obtaining redshifts of faint objects in large numbers so that survey-type work could be pursued more efficiently. The next step to achieving this goal was clearly to provide FOS with a multi-object capability.

FOS has a usable field of 3 by 4 arcmin which is well suited to multi-object work in small clustered fields. Following initial discussions in 1983 between R A E Fosbury (RGO), R S Ellis (Durham) and D W Gellatly (RGO), a multislit unit was designed to replace the conventional slit assembly within the IDS.

The unit was designed in detail by D W Gellatly and constructed at the RGO during 1984-1985 (Ellis et al., 1986). It consists of 10 slit slides which move adjacent to each other in a direction normal to the slits themselves. Each slit is 16 arcsec long and has a fixed width of 1.5 arcsec. The centre to centre spacing between the slit slides is 23 arcsec i.e. there is a dead space of 7 arcsec between each slit. The slits need to be manually set to pre-determined positions using an XY coradograph before the unit is installed within the IDS. A GG495 field-lens is required to filter out the second order and to prevent vignetting across the field.

The unit was commissioned on the INT in November 1985 and successfully used to observe faint clusters in February 1986.

An automated version of the multislit unit is currently being developed in Durham which will allow the slitlets to be configured remotely from the observer's console, thereby obviating the necessity for the unit to be removed from the IDS and reconfigured for each observation (Breare et al., 1986b).

9.5 4.2m WHT Faint Object Spectrograph

The success of the INT FOS has encouraged the construction of a similar instrument for the f/11 Cassegrain focus of the LPO 4.2m William Herschel Telescope (WHT); the project again being a collaboration between the University of Durham and the RGO, and involving the author in its development.

The 4.2m FOS is scheduled for commissioning in the latter half of 1987. Its function will be basically the same as that of the 2.5m FOS, i.e. for classification and redshift determination of the faintest of astronomical targets. However, the greater collecting area of the 4.2m mirror will in principle allow observations to approximately one magnitude deeper than those achievable with the 2.5m FOS for a given S/N.

The overall optical design is similar to that of the 2.5m FOS, producing two cross-dispersed orders covering the wavelength range 350 to 1050 nm, and with a first order dispersion of 400 Å/mm.

The original intention was to install a thinned Tektronix CCD of 512 by 512 pixels which, with its anticipated blue responsivity, should enable the second order spectrum to be used to better effect than in the 2.5m FOS. However, because of the uncertainty in the availability of the Tektronix CCD, it is now planned to install a coated GEC CCD until such time that it can be replaced with a Tektronix chip.

The camera assembly is designed to fit beneath the WHT's intermediate dispersion spectrograph, ISIS, in order that it can use ISIS' slit and calibration facilities in the same way as the 2.5m FOS uses those in the IDS. A folding-flat mirror is not necessary, however, since there is sufficient room at Cassegrain for the instrument to work in a 'straight-through' position.

The WHT's Cassegrain spectrographs have been designed with multi-object work in mind. ISIS' slit assembly is to be modular, enabling the insertion of a conventional slit and dekker slide, a manually-preset multislit unit, or a fibre optic feed.

The CCD camera is to be one of the new generation of CCD controllers currently being developed for the WHT as a collaboration between the RGO and Dwingeloo in the Netherlands (Bregman and Waltham, 1986). A local microprocessor controller to allow remote focussing of the CCD is also being developed which will be very similar to the one designed for the 2.5m FOS.

9.6 Summary

The Faint Object Spectrograph is an important addition to the Isaac Newton Telescope's instrumentation. Its high throughput and wide spectral coverage promise to serve the community well in those fields which depend upon the classification of the spectra from the faintest of astronomical objects.

The central problems in cosmology concerning the large scale structure of the universe, its age and its evolution are among those areas in which FOS can undoubtedly play an important role. Looking through the PATT allocations outlined earlier in this chapter, it is interesting to see that the instrument is already being used to tackle these and related problems.

FOS can also be regarded as a success in terms of its development as a collaboration between the University of Durham and the RGO. The project has involved many people, both at Durham and the RGO, with specialist interests in astronomy, optics, mechanical design, electronics and software. Further vindication of the project's success comes from the fact that a similar instrument is being constructed for the LPO 4.2m telescope, and that it is again being organized as a collaboration between the University of Durham and the RGO.

APPENDIX A CCD CAMERA ELECTRONICS CIRCUIT DIAGRAMS

Circuit diagrams of the Preamplifier and 16 bit Digitization unit are given in Chapter 4.

CCD CAMERA

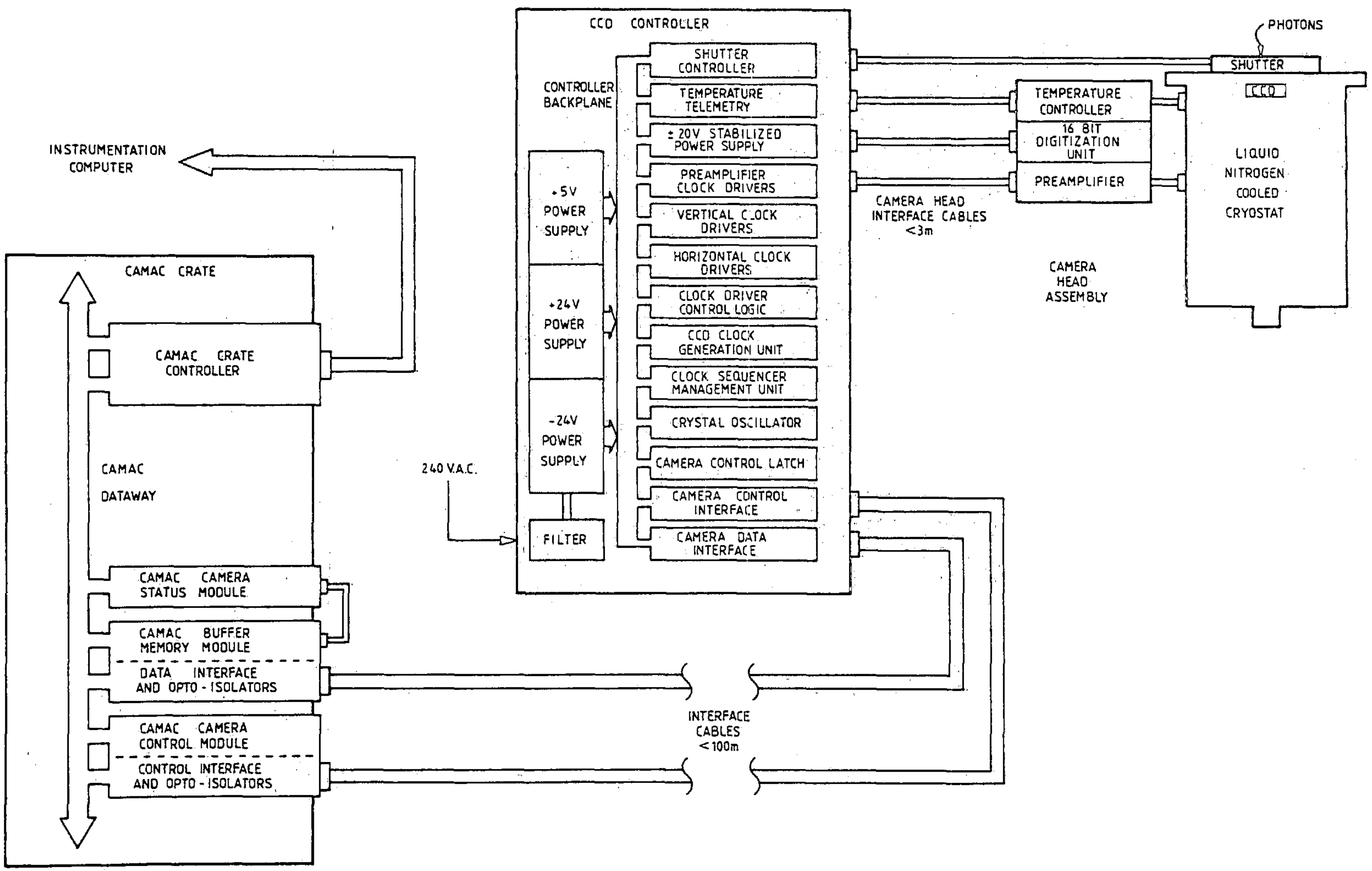
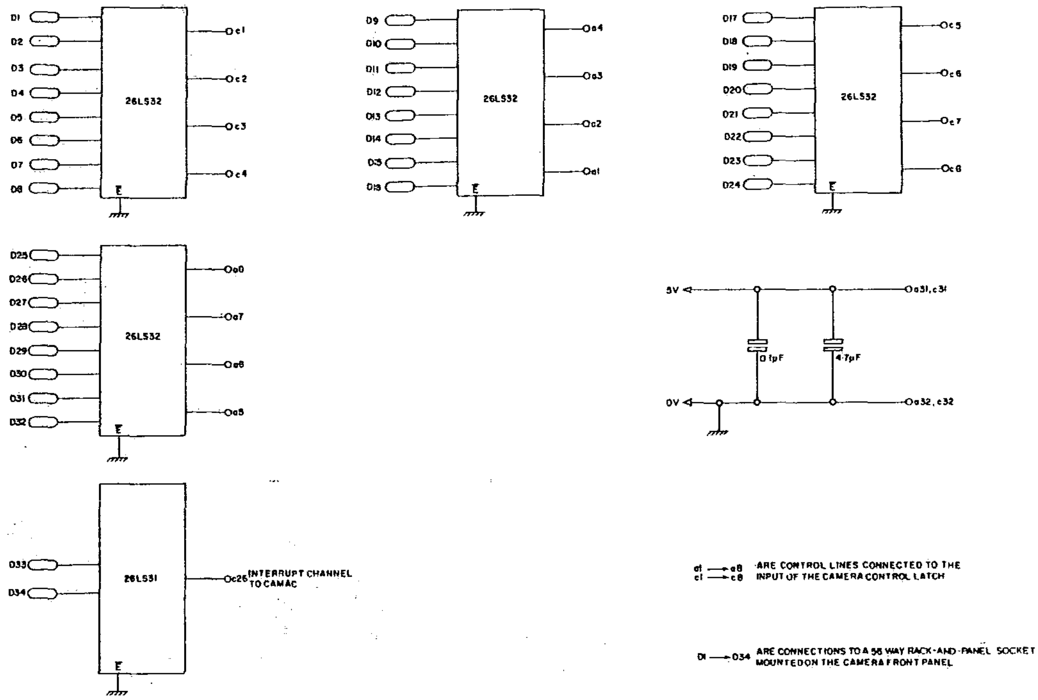


Figure A1

CAMERA CONTROL INTERFACE UNIT



CAMERA DATA INTERFACE UNIT

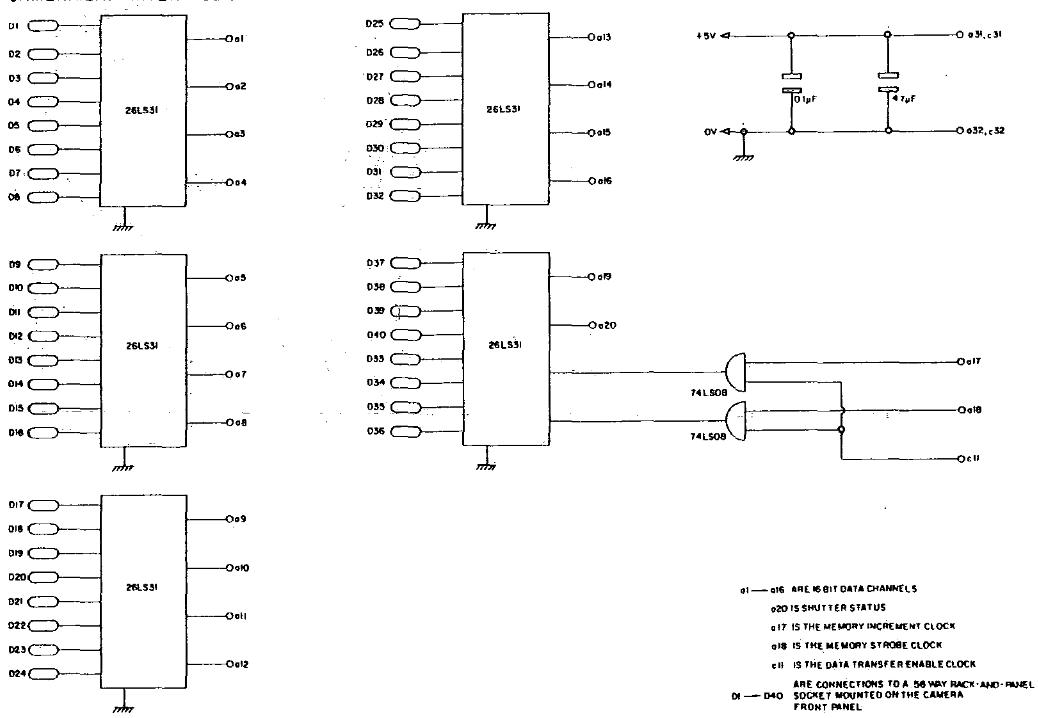


Figure A2

CAMERA CONTROL LATCH

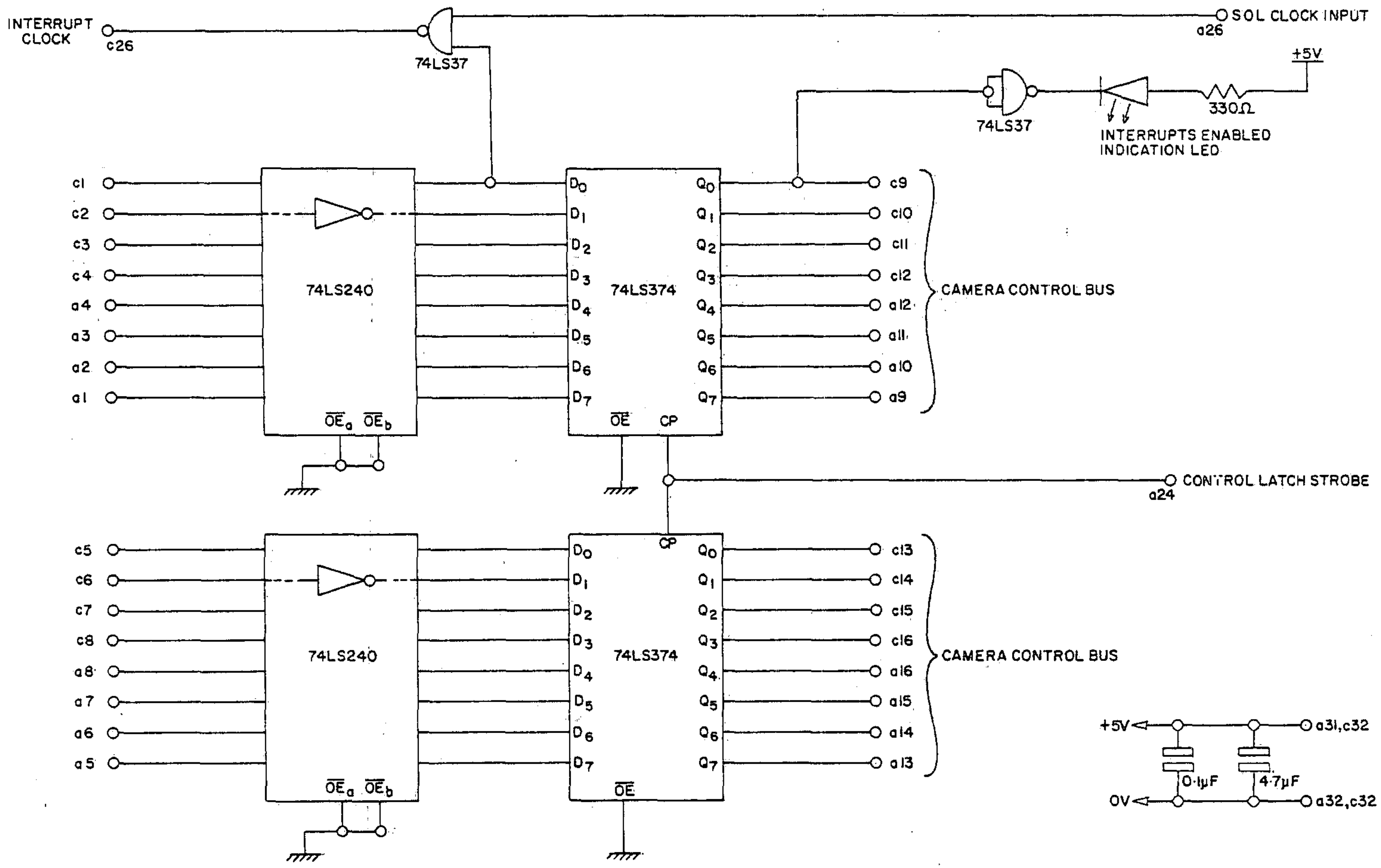


Figure A3

CCD CLOCK SEQUENCER MANAGEMENT UNIT

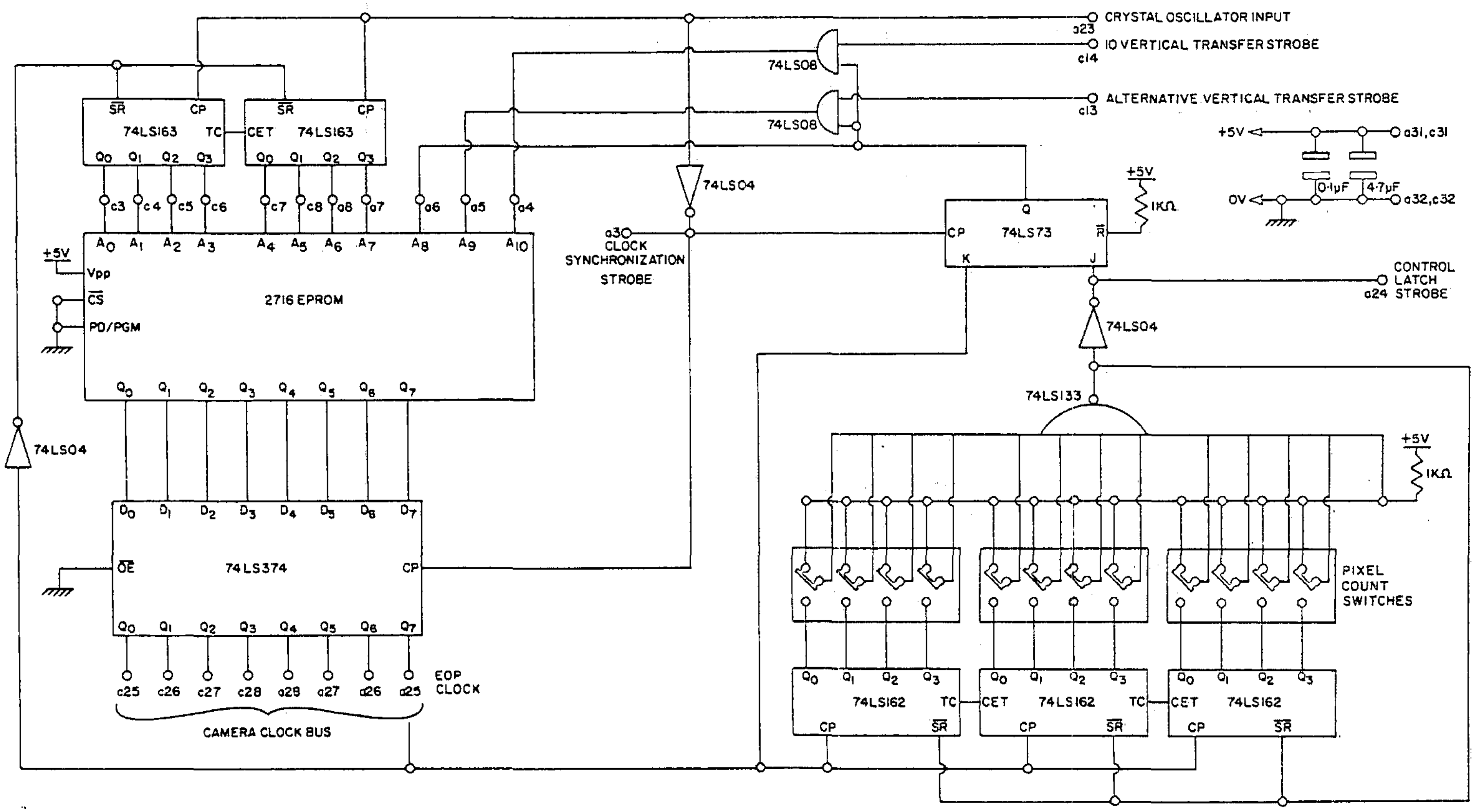
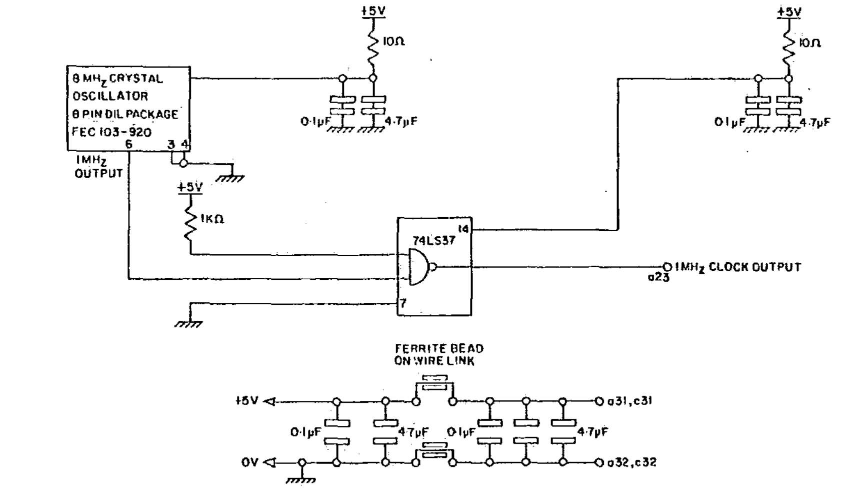


Figure A4

CRYSTAL OSCILLATOR – MASTER CLOCK



CCD CLOCK GENERATION UNIT

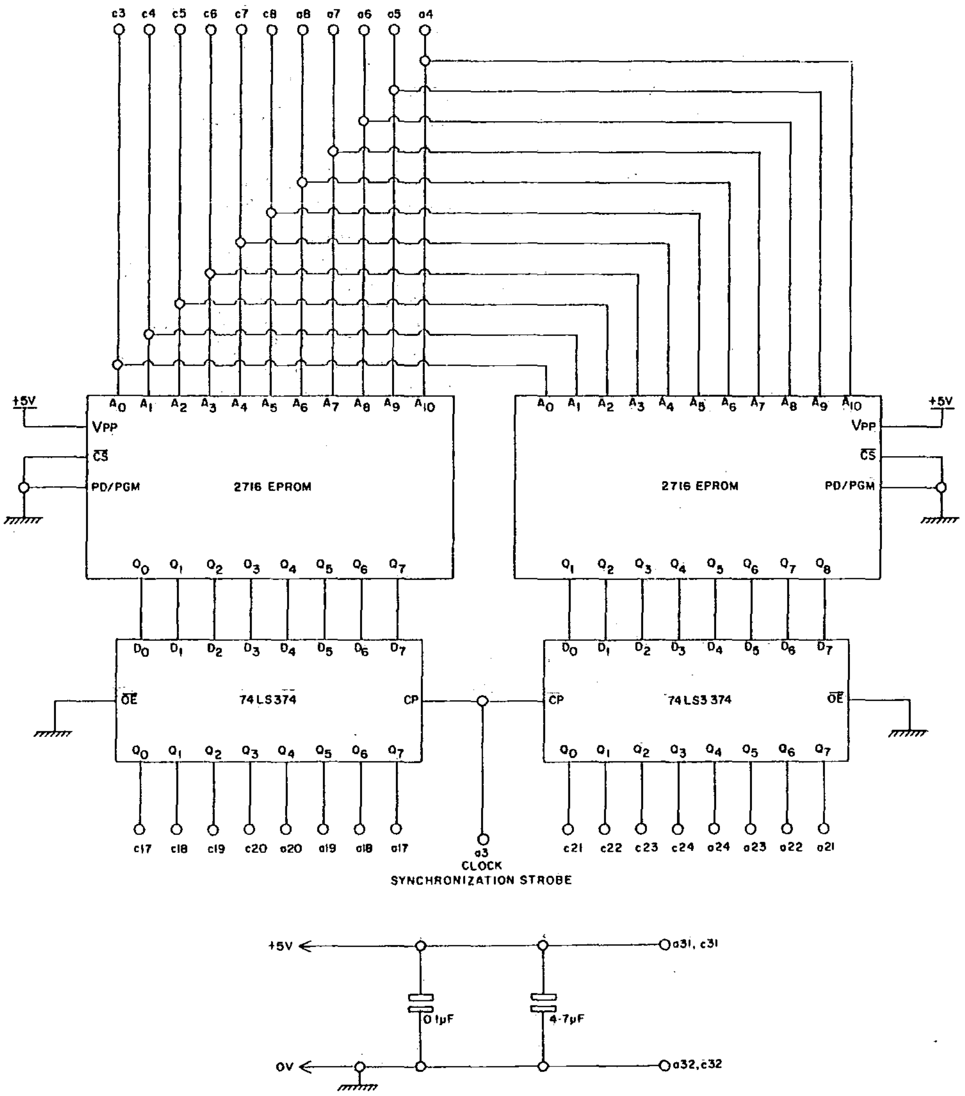


Figure A5

CLOCK DRIVER CONTROL LOGIC

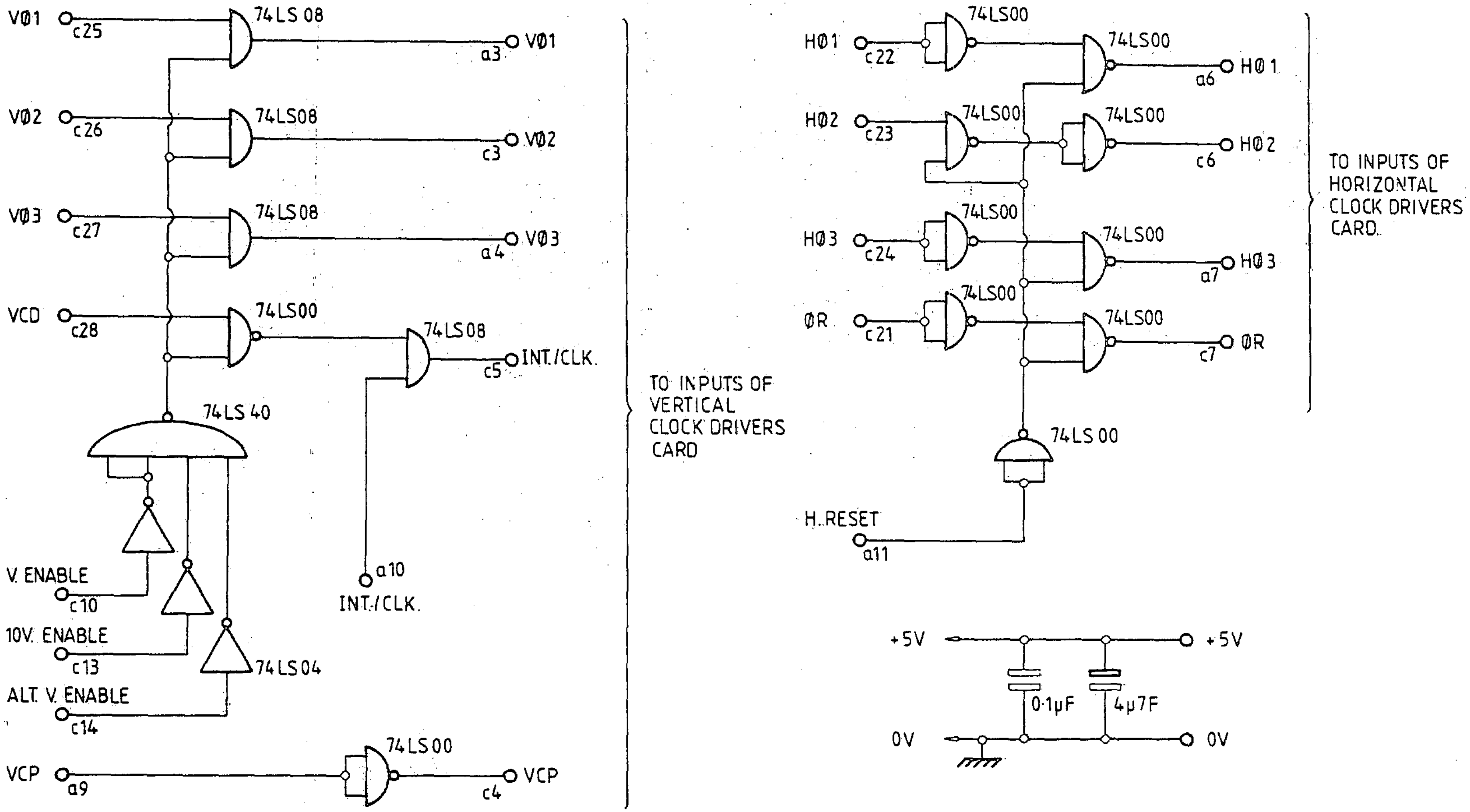


Figure A6

HORIZONTAL AND RESET CLOCK DRIVERS

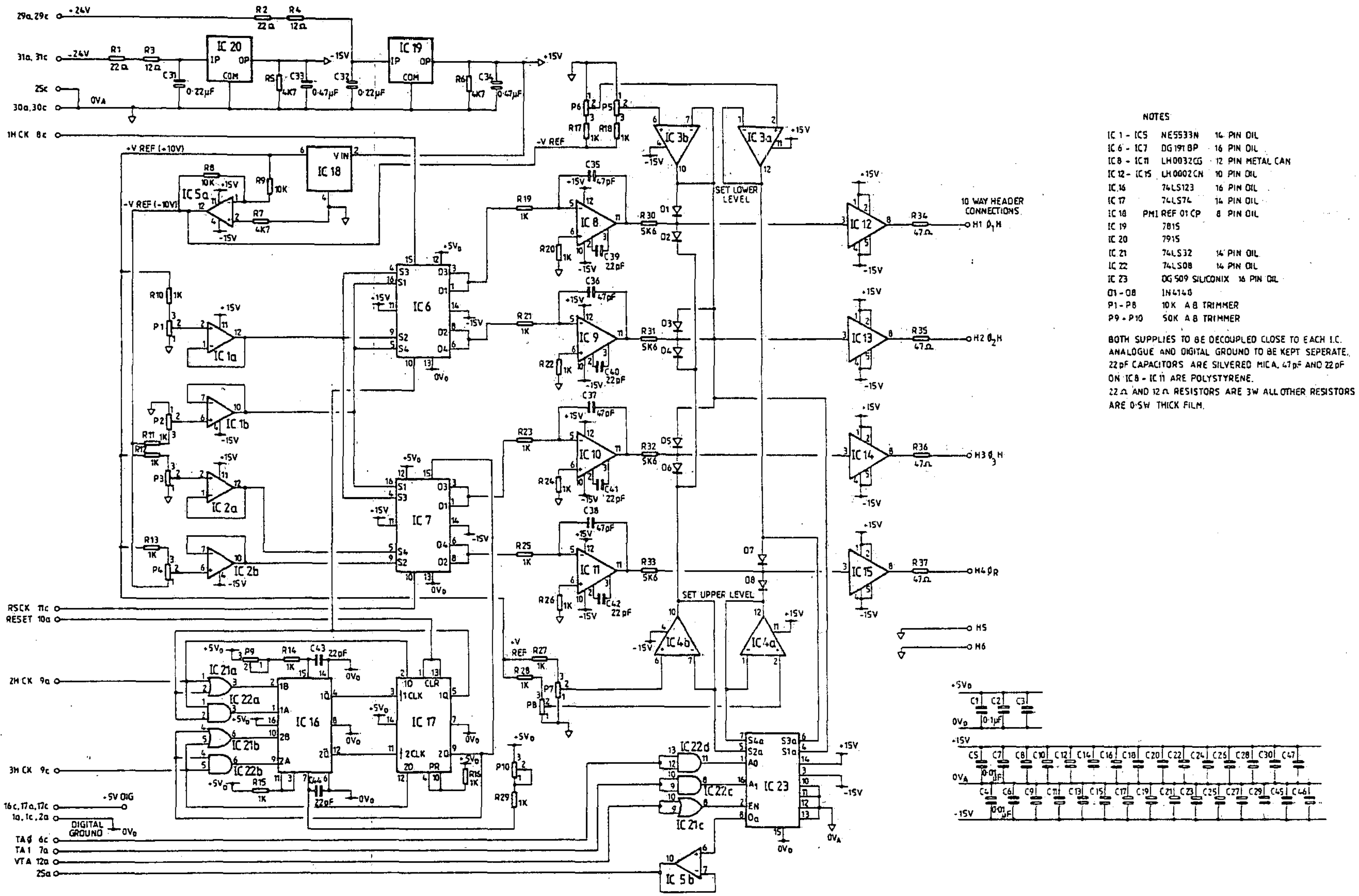
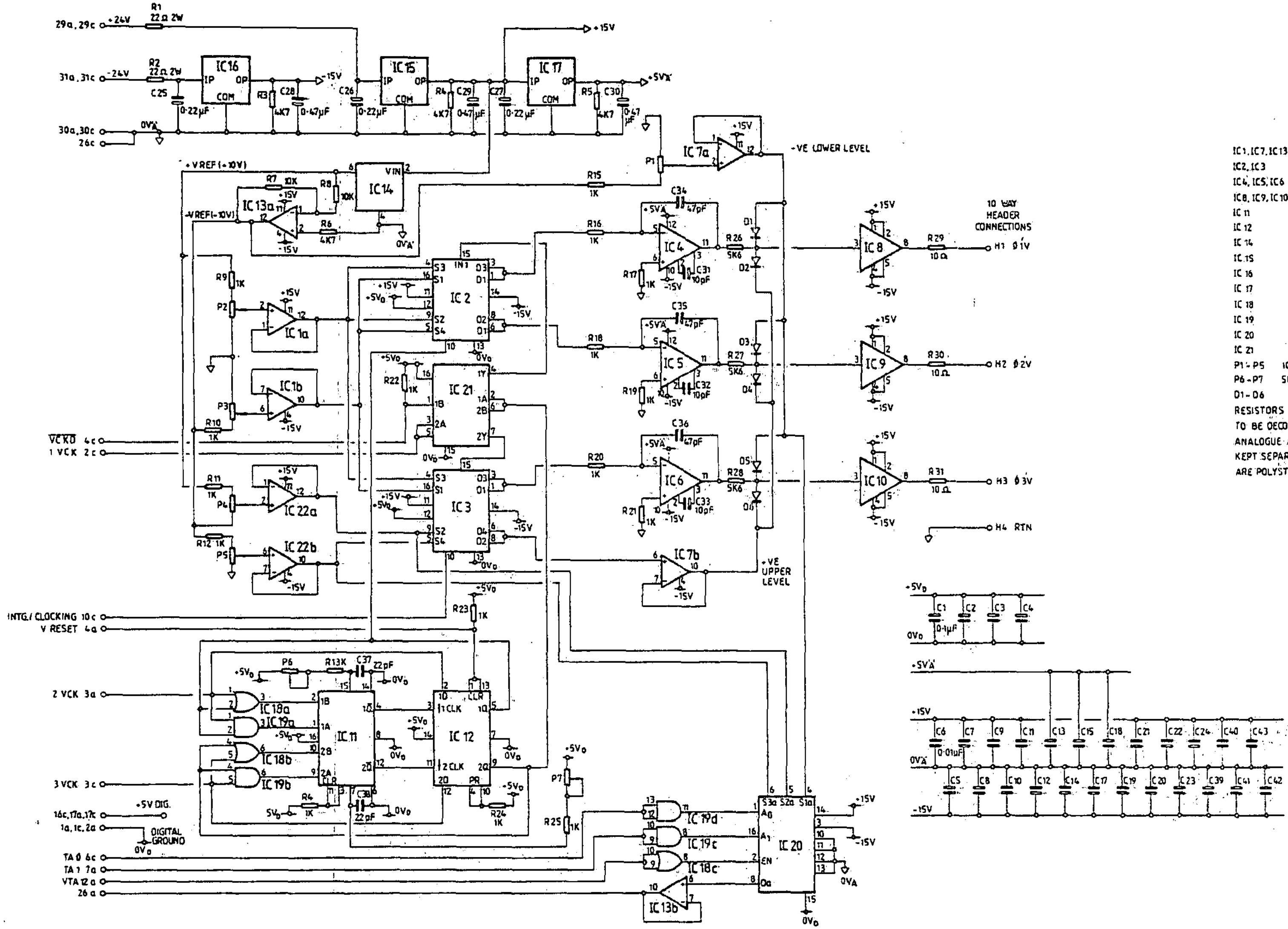


Figure A7

VERTICAL CLOCK DRIVERS



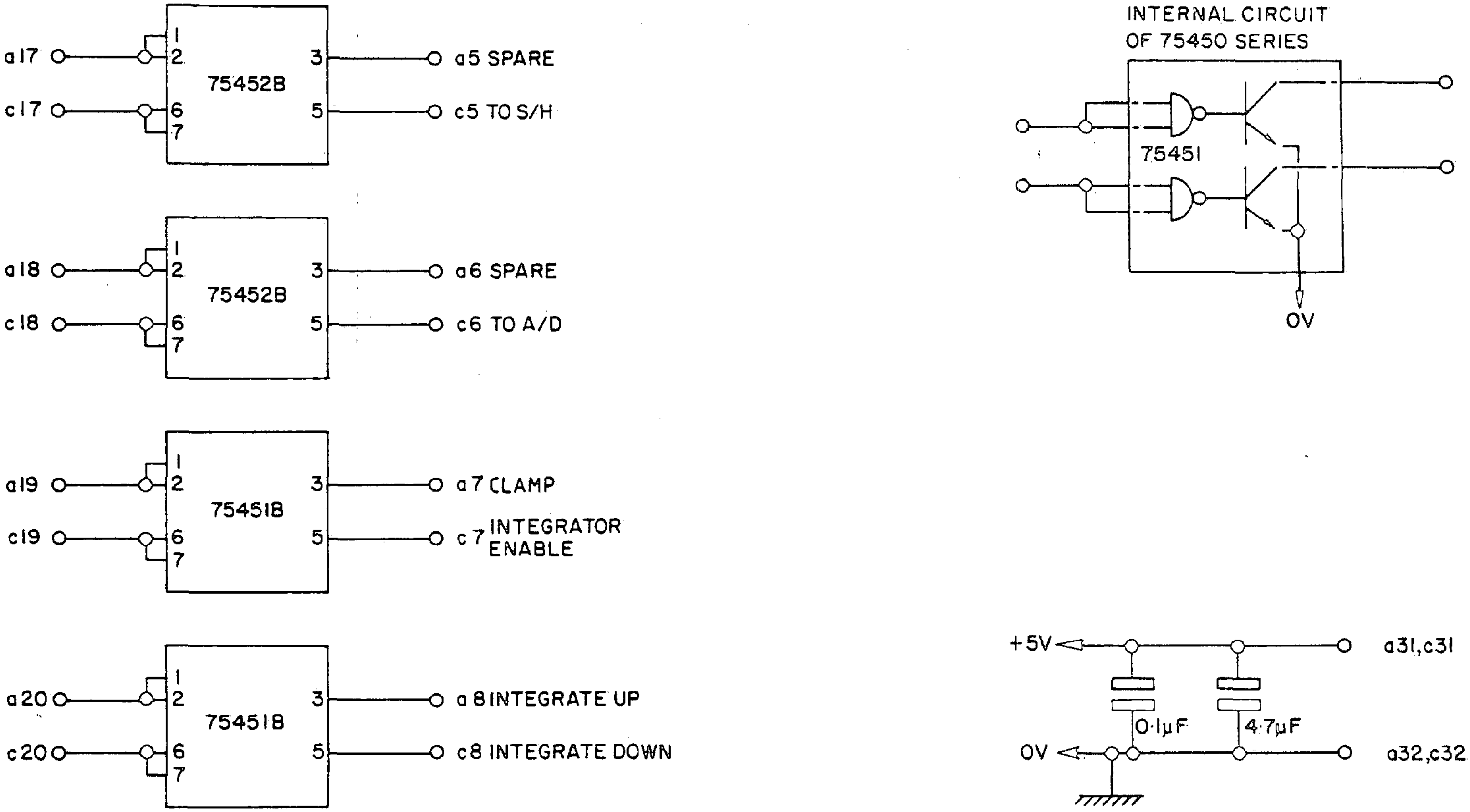
IC1, IC7, IC13, IC22	NE5533N 14 PIN DIL
IC2, IC3	DG 191BP 16 PIN DIL
IC4, IC5, IC6	LH0032CG 12 PIN METAL CAN
IC8, IC9, IC10	LH0002CN 10 PIN DIL
IC 11	74LS123 16 PIN
IC 12	74LS74 14 PIN
IC 14	PMI REF-01 CP 8 PIN
IC 15	7815
IC 16	7915
IC 17	7805
IC 18	74LS32 14 PIN
IC 19	74LS08 14 PIN
IC 20	DG509 16 PIN
IC 21	74LS157 16 PIN
P1 - P5	10K AB TRIMMER
P6 - P7	50K AB TRIMMER
D1 - D6	1N4148

RESISTORS ½ W THICK FILM SUPPLIES TO BE DECOUPLED CLOSE TO EACH IC. ANALOGUE AND DIGITAL GROUNDS TO BE KEPT SEPARATE. 10 pF AND 47 pF CAPACITORS ARE POLYSTYRENE 22 pF CAPS ARE SILVERED MICA.

Figure A8

Figure A9

PREAMPLIFIER CLOCK INTERFACE



± 20V REGULATED SUPPLY

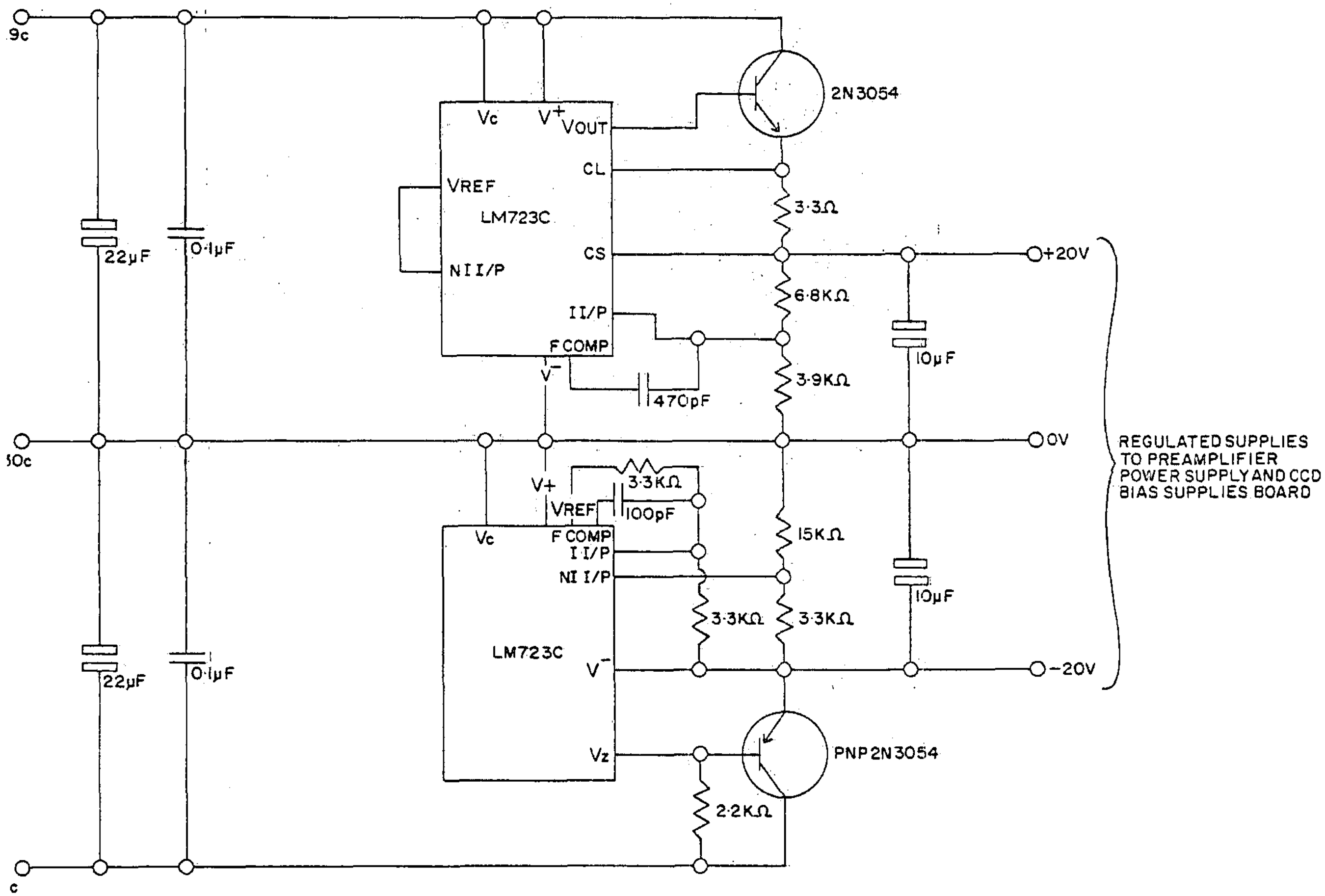
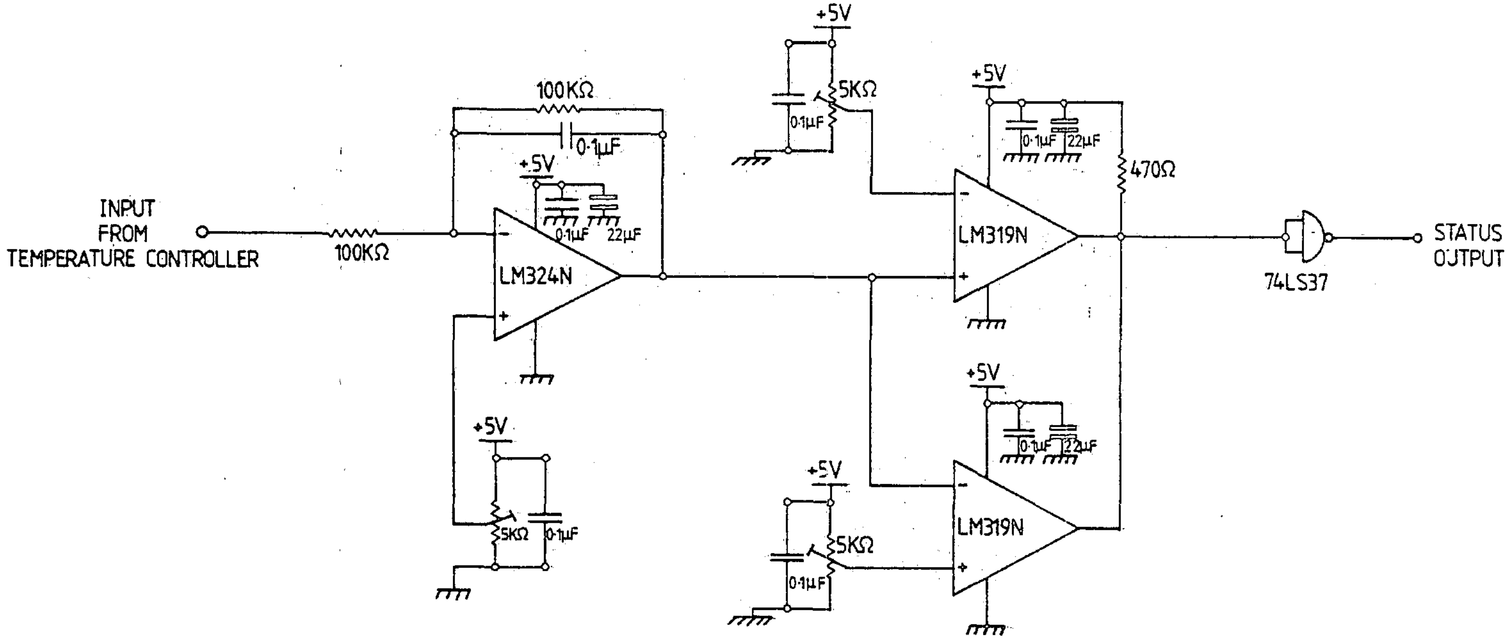
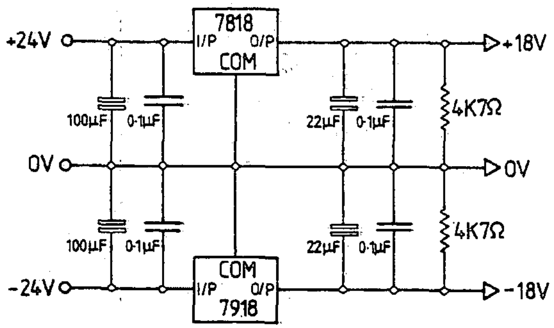


Figure A10

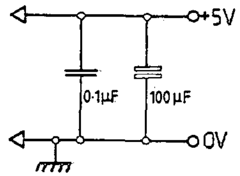
Figure A11

TEMPERATURE CONTROLLER INTERFACE





POWER SUPPLY
TO
TEMPERATURE
CONTROLLER



SHUTTER CONTROLLER

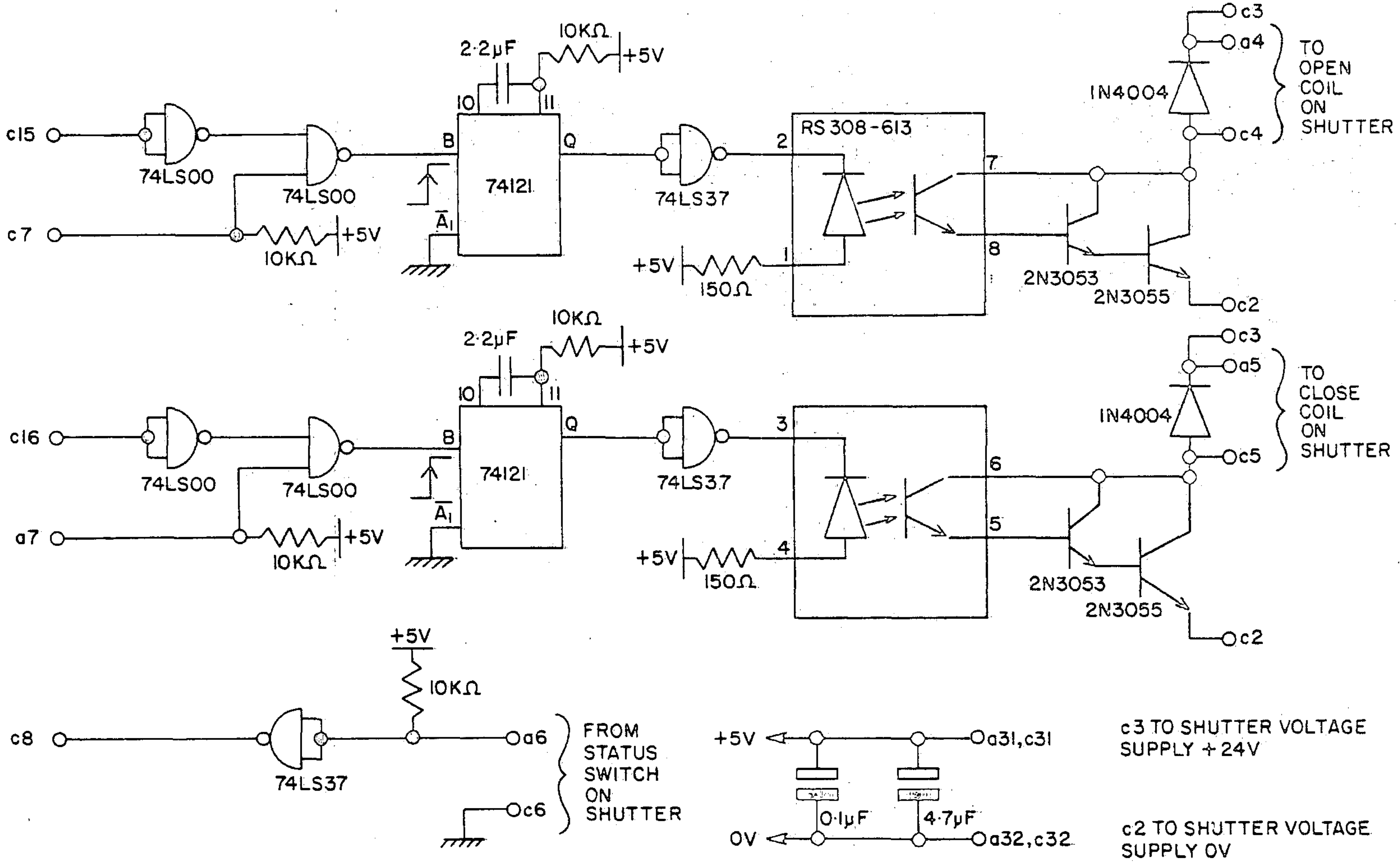


Figure A12

CAMAC CAMERA CONTROL MODULE

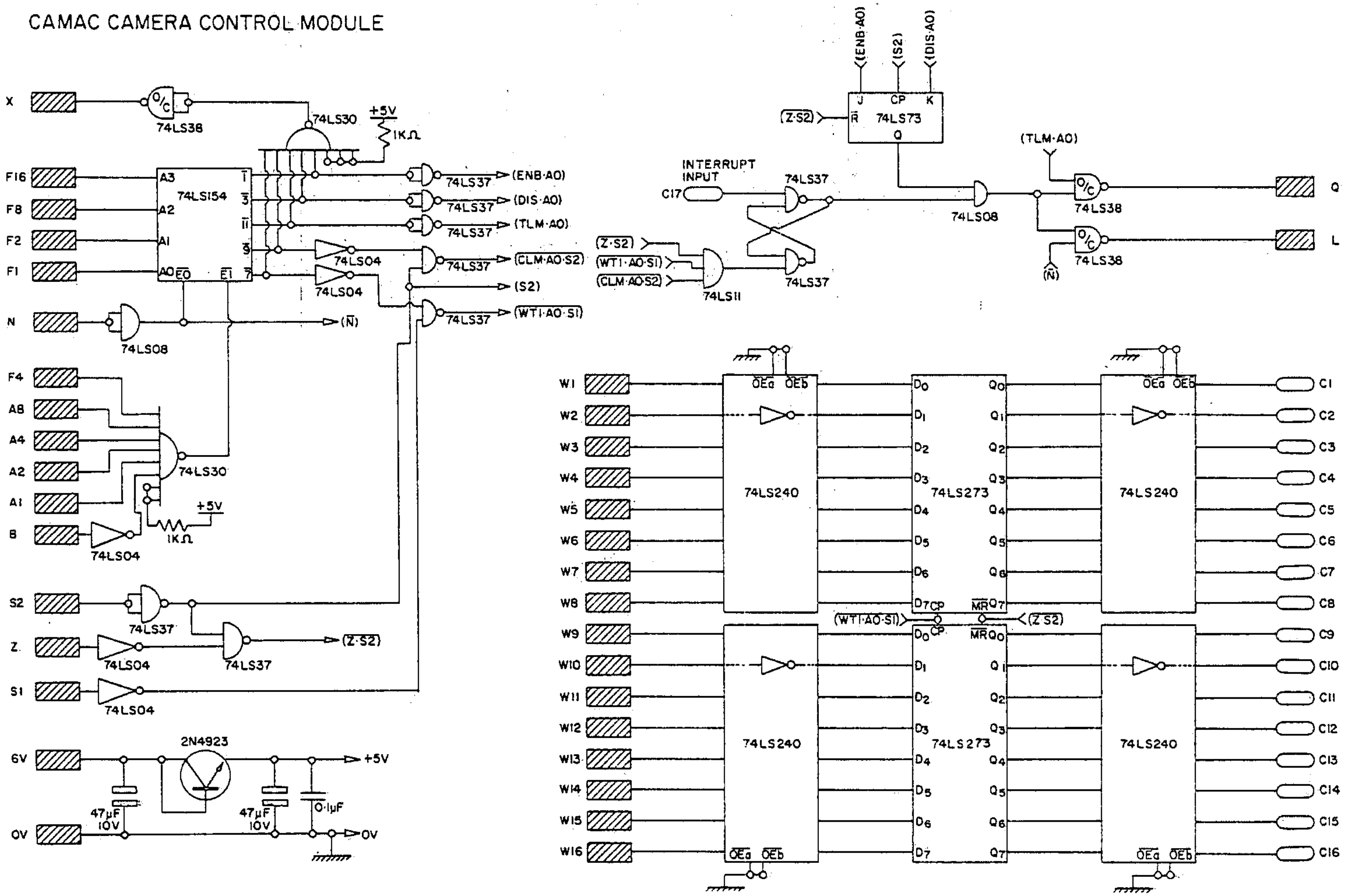


Figure A13

INTERFACE UNIT FOR THE CAMAC CONTROL MODULE

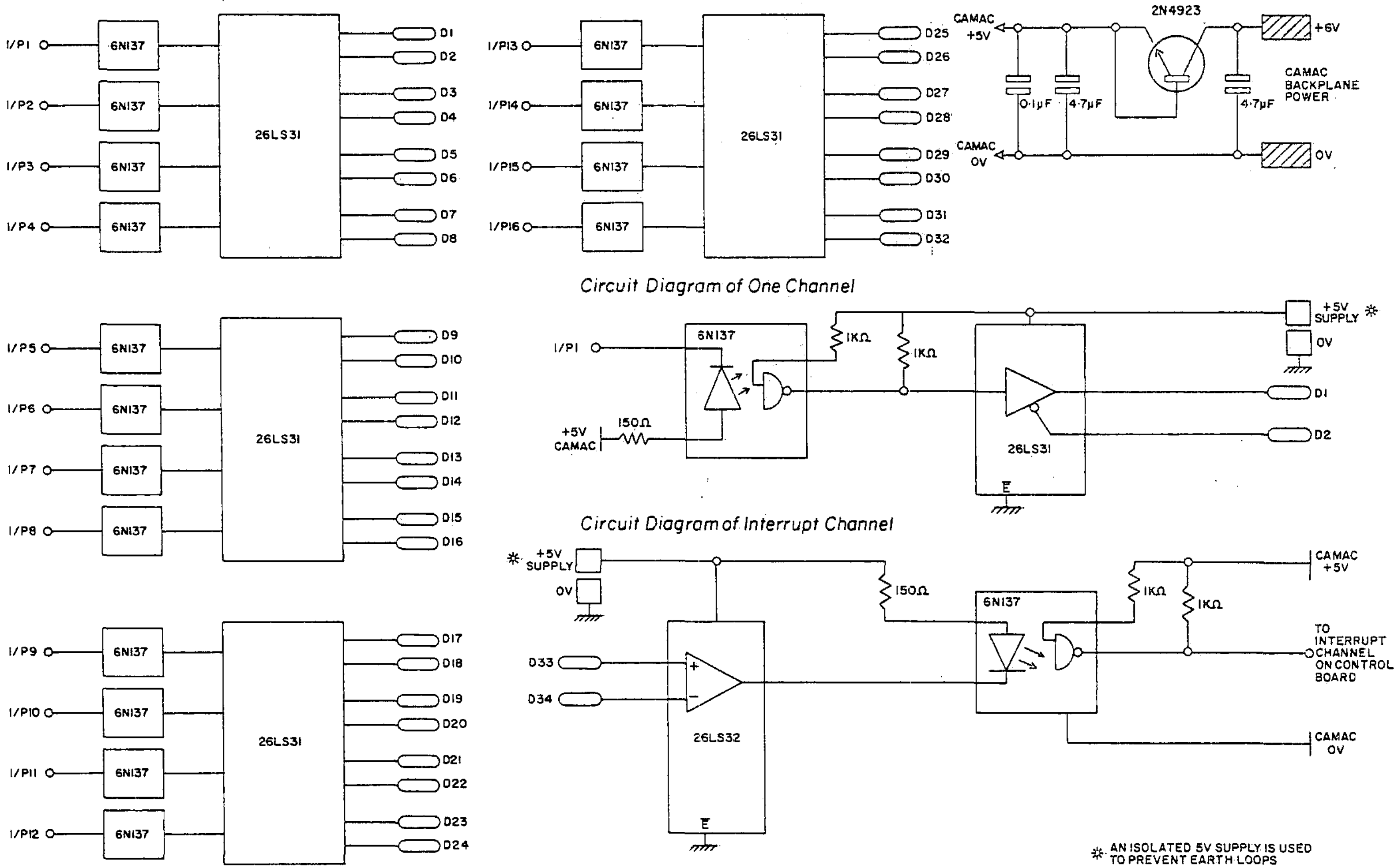


Figure A14

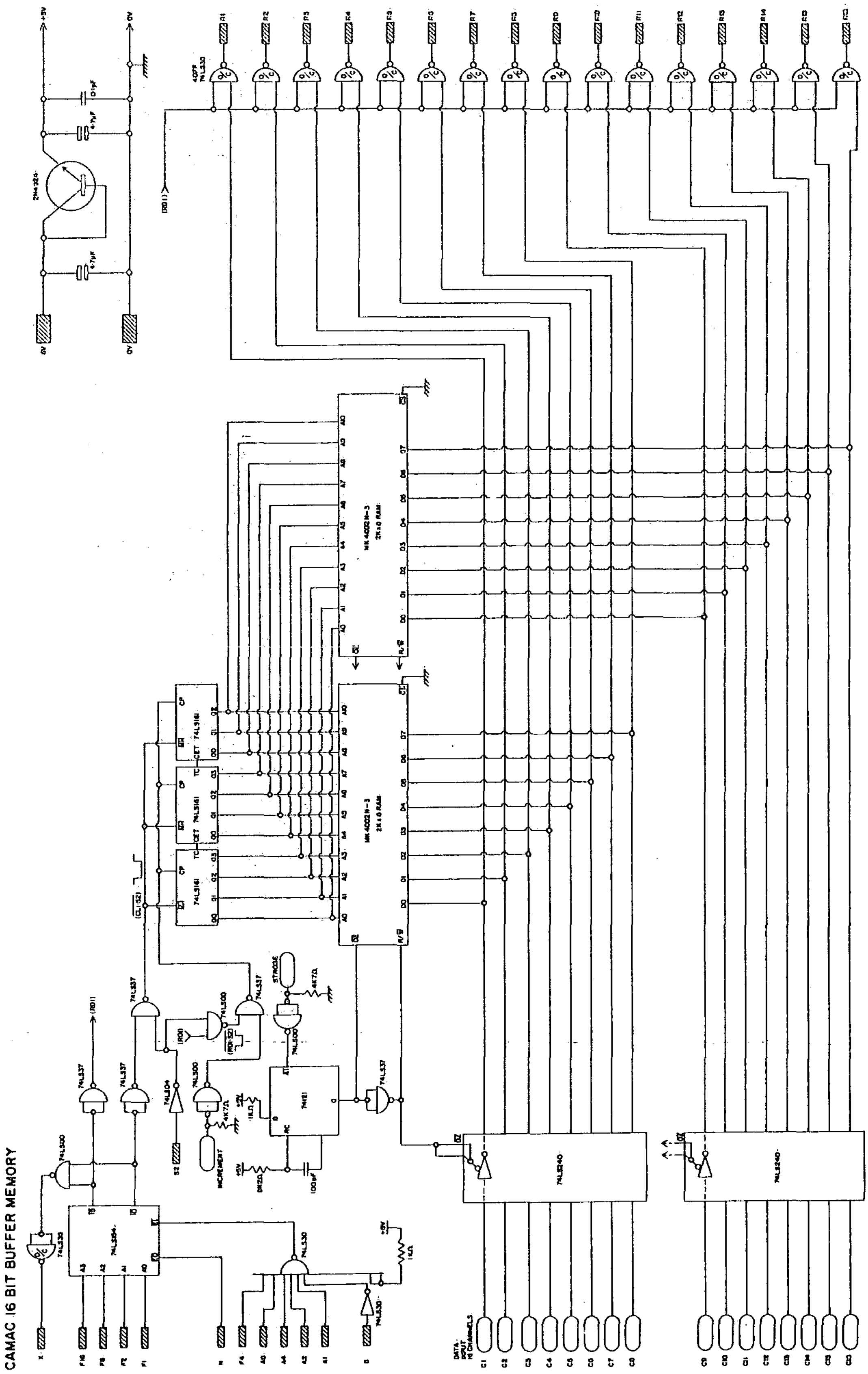


Figure A15

INTERFACE UNIT FOR CAMERA DATA

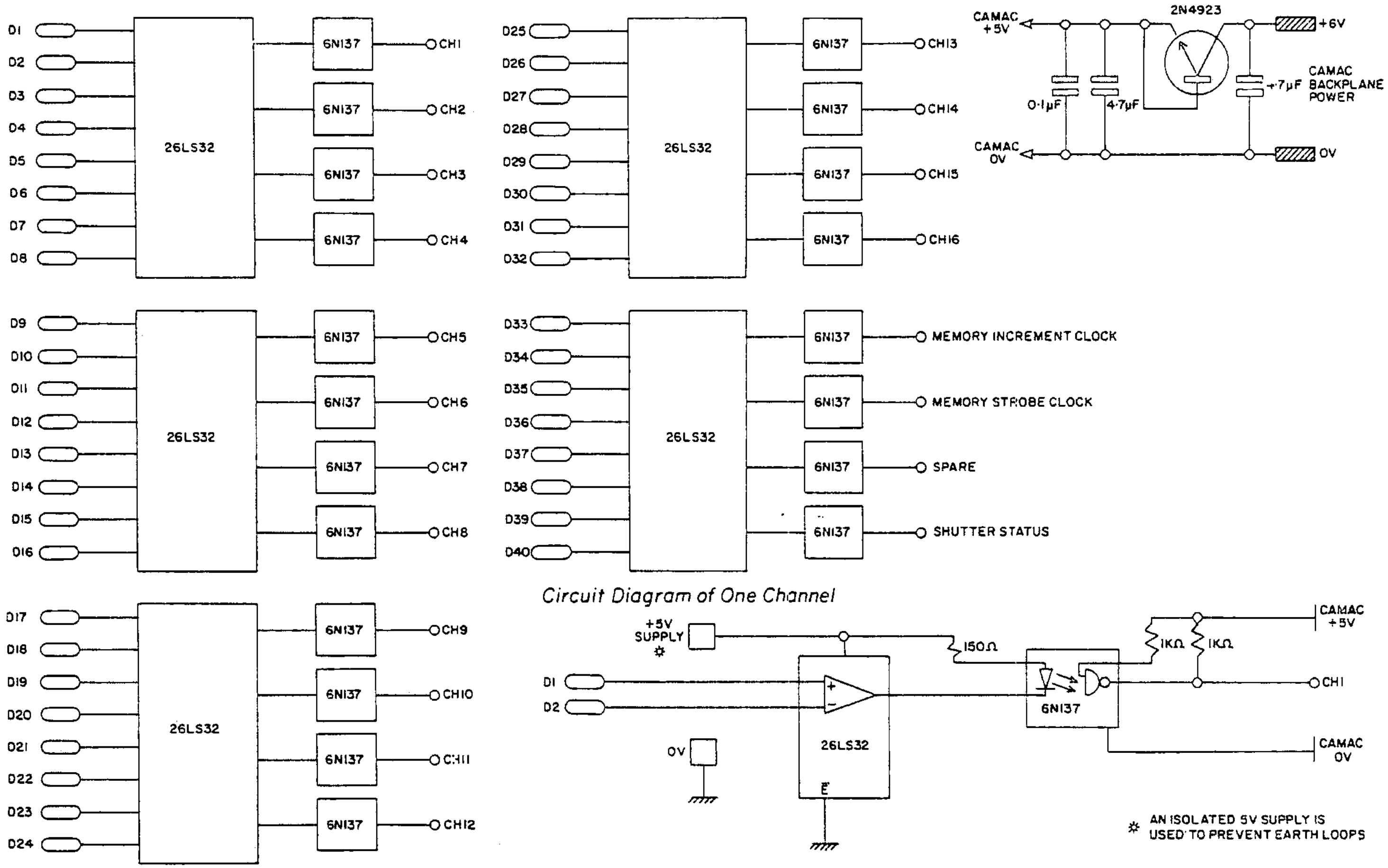
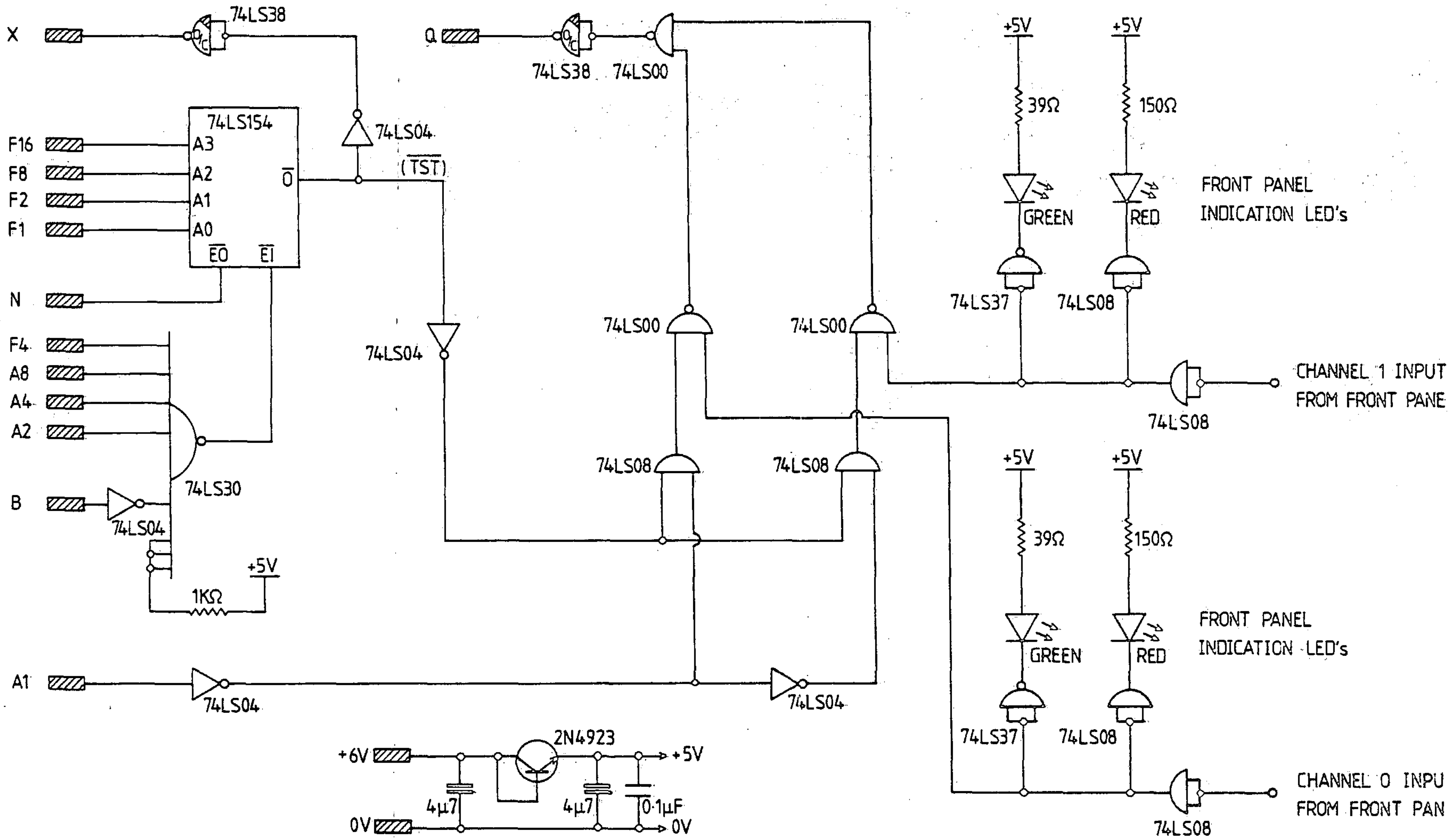


Figure A16

Figure A17

CAMAC CAMERA STATUS UNIT



TEMPERATURE CONTROLLER

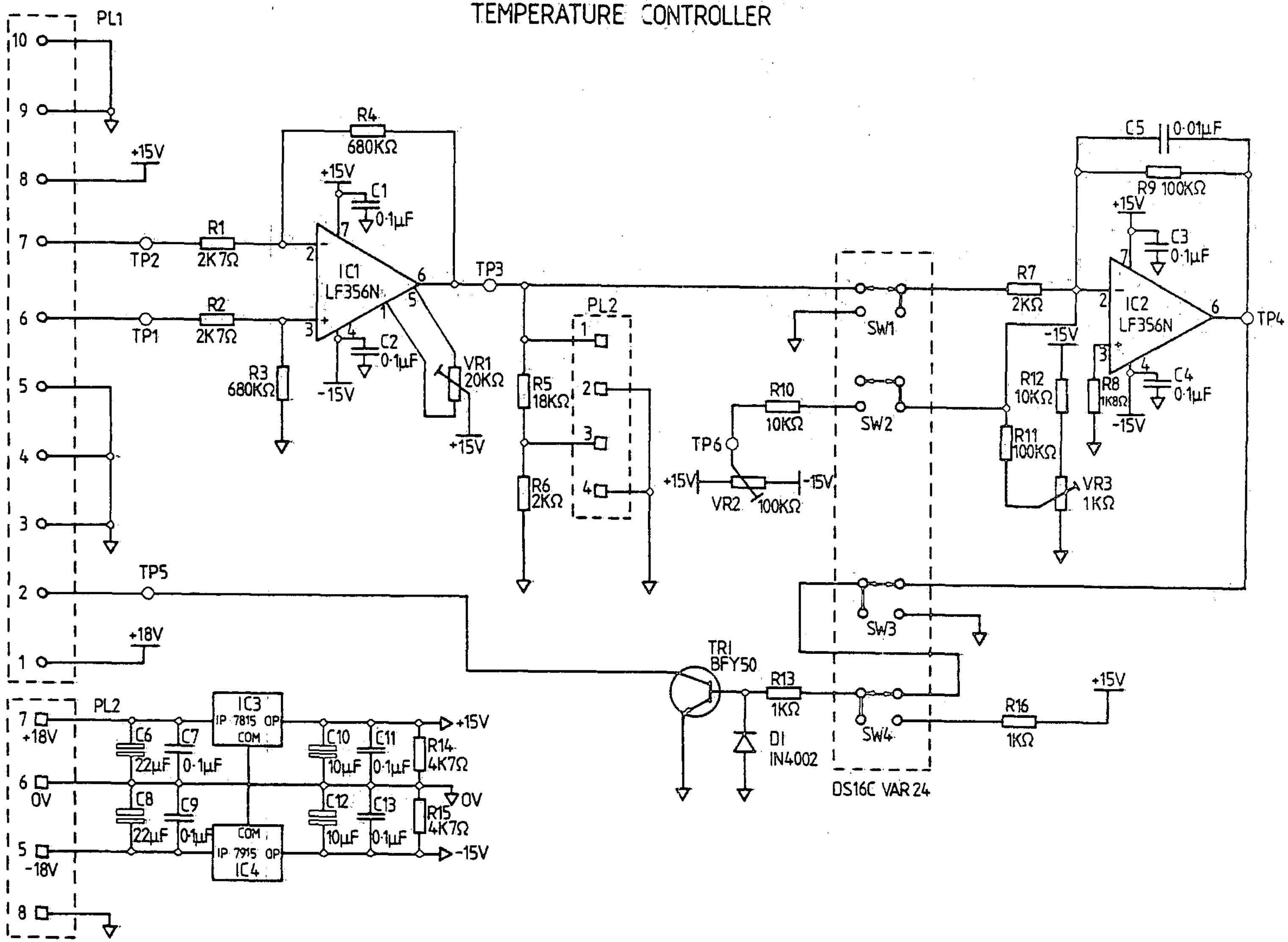


Figure A18

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