CDS-CU(_x)S single crystal and thin film solar cells

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CdS-Cu_xS SINGLE CRYSTAL AND THIN FILM SOLAR CELLS

by

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Presented in candidature for the degree of

Doctor of Philosophy

in the

University of Durham

February 1988

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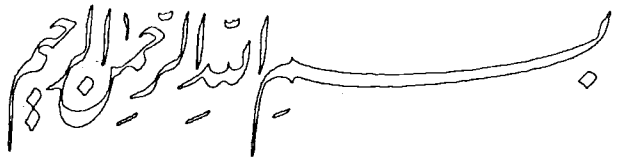


36. Glory to God, Who created
In pairs all things that
The earth produces, as well as
Their own (human) kind
And (other) things of which
They have no knowledge.

٣٦- سُبْحٰنَ الَّذِيْ خَلَقَ الْاَزْوَاجَ كُلَّهَا
مِمَّا تُنْۢبِتُ الْاَرْضُ وَمِنْ اَنْفُسِهِمْ
وَمِمَّا لَا يَعْلَمُوْنَ ۝

37. And a Sign for them
Is the Night: We withdraw
Therefrom the Day, and behold
They are plunged in darkness;

٣٧- وَاٰيَةٌ لَّهُمُ الَّيْلُ ۖ نَسْلَخُ مِنْهُ النَّهَارَ
فَاِذَا هُمْ مُّظْلِمُوْنَ ۝

38. And the Sun
Runs his course
For a period determined
For him: that is
The decree of (Him),
The Exalted in Might,
The All-Knowing.

٣٨- وَالشَّمْسُ تَجْرِيْ
لِمُسْتَقَرٍّ لَّهَا ۭ
ذٰلِكَ تَقْدِيْرُ
الْعَزِيْزِ الْعَلِيْمِ ۝

39. And the Moon,—
We have measured for her
Mansions (to traverse)
Till she returns
Like the old (and withered)
Lower part of a date-stalk.

٣٩- وَالْقَمَرَ قَدَّرْنٰهُ مَنَازِلَ
حَتّٰى عَادَ
كَالْعُرْجُوْنِ الْقَدِيْمِ ۝

40. It is not permitted
To the Sun to catch up
The Moon, nor can
The Night outstrip the Day:
Each (just) swims along
In (its own) orbit
(According to Law).

٤٠- لَا الشَّمْسُ يَنْۢبَغِيْ لَهَآ اَنْ تُدْرِكَ
الْقَمَرَ وَلَا الَّيْلُ سَابِقُ النَّهَارِ ۭ
وَكُلٌّ فِيْ فَلَكٍ يَّسْبَحُوْنَ ۝

To my parents

and

my wife

ACKNOWLEDGEMENTS

I must express my sincere gratitude to ALLAH without whose help this study would never have been possible. I would like to thank my supervisors Prof. J. Woods and Dr. G.J.Russell for their guidance, assistance and valuable discussion during the course of this research project.

I would also like to thank Prof. G.G.Roberts for allowing me to use the facilities of the department and I am grateful to workshop staff, headed by Mr. F. Spence for their technical help and advice. I wish to extend my thanks to Mr N.F. Thompson for technical assistance in the laboratory and in the crystal growth.

I am particularly indebted to Mr T. Harcourt for cutting and polishing the single crystal. I also wish to thank Dr. S. Oktik for the valuable discussion and Dr. A.W. Brinkman and other members of the group who rendered me their help during the course of this work in one way or another.

I am also grateful to Miss K. Cummins for drawing the diagrams included in this thesis and to Mrs S. Little for typing the thesis. In addition, special thanks are due to Mr T. Furlong for proof-reading. The financial support by King Saud University is gratefully acknowledged.

Finally I would like to express my gratitude to my parents for their many sacrifices, my brother, Ahmed for his constant encouragement over the years and to my wife for her understanding, support and contributions to a happy home and enjoyable family life.

ABSTRACT

The work presented in this thesis is concerned with photovoltaic cells formed by plating CdS single crystals and thin films, and $Cd_yZn_{1-y}S$ single crystals, with copper sulphide. An electroplating technique has been used to control the phase of copper sulphide by changing the electric field during its formation. Different phases of Cu_xS have been identified directly using Reflection High Energy Diffraction (RHEED), and indirectly from spectral response measurements. A dramatic change in the spectral response accompanying the reduction in the covellite response associated with an increase in that from chalcocite following argon heat treatment has been achieved. The change from the djurleite phase to that of chalcocite has also been obtained by using argon heat treatment for 5 minutes at 200°C. This effect was found to be reversible in that layers of chalcocite were converted to djurleite when air was used as the ambient for the heat treatment. C-V measurements have demonstrated that with increasing plating bias the donor concentration decreases at first before it assumes a constant value. This led to the effect of decreasing the junction capacitance as the width of the depletion region changed.

The problem of the stability of the CdS-Cu_2S photovoltaic devices formed by "wet plating" is addressed by studying the combined effects of the substrate onto which the CdS is deposited and the ambient used during annealing. Thin film cells have been prepared on both Ag/Cr and SnO_x substrates, and the device characteristics for each have been investigated as a function of annealing ambient. The results have shown that devices formed on Ag/Cr substrates were more stable following annealing in air than in argon, while the converse was true for cells fabricated on SnO_x substrates.

The degradation effects of CdS-Cu_2S photovoltaic cells have been investigated. While devices stored in the dark showed little or no degradation, those maintained under illumination exhibited a significant deterioration in all operational parameters over a four week period. As far as the combined effect of temperature and ambient on the stability of cells are concerned, it was found that the ageing of devices in argon at room temperature in the dark was negligible, and moreover the fill factor was observed to improve marginally. When the devices were stored in the same ambient conditions at 50°C, they showed a significant improvement in the fill factor, but simultaneously exhibited a considerable reduction in the short circuit current. This process was reversible, since the sensitivity of degraded devices could be restored by annealing them in a hydrogen/nitrogen mixture. By comparing Electron Spectroscopy for Chemical Analysis (ESCA) studies with solar cell device characteristics, it has been shown that the formation of copper oxide on the Cu_2S surface plays a significant role in the degradation of CdS-Cu_2S devices.

The extent of the cross-over between the dark and light J-V characteristics is a function of the period of etching used prior to junction formation. The variation of current and diode factor has been established as a function of the bias value. The dependence of forward current on the temperature at fixed forward voltage has also been investigated.

Finally this work has shown that an increase in V_{oc} can be achieved when $Cd_{0.8}Zn_{0.2}S$ is used as a base material for solar cells instead of CdS. Different traps were identified through a photocapacitance investigation. An important trap was found at 0.78eV below the conduction band. It has been demonstrated that the effect of this level was found to be diminished much more slowly when the annealing was carried out in argon rather than in air. This level may play an important role in the $Cd_{0.8}Zn_{0.2}S$-Cu_2S solar cell properties.

CHAPTER ONE

Introduction

1.1 Introduction

It is estimated that less than 20% of the population of the developing countries are supplied with electricity. In Africa, for example, more than 400 million people out of a total population of 470 million are not connected to an electricity distribution grid. Also in the developing countries, 75% of the population are in danger of becoming marginalized in the long term [1]. In addition, since the world has been using an exhaustible energy supply, it is necessary to investigate renewable energy sources. In this connection, solar energy is regarded as one of the most promising alternative sources especially for the electrification of rural areas in Third World countries. Solar cells are particularly attractive in this respect as the incident solar energy is converted directly into electricity without movement of any mechanical parts or associated problems of pollution.

In a photovoltaic device, light photons are absorbed by the semiconductor which forms the absorber limb and thereby creates equal numbers of electric charge carriers called electrons and holes. These diffuse to a junction which is formed between either a p- and an n-type semiconductor or between a metal and a semiconductor (Schottky barrier). In both types of device a strong internal electric field exists. Electrons and holes are separated by this field which leads to the development of a voltage and the flow of a current, so allowing power to be delivered to an external load such as a light bulb or a motor. A schematic diagram of a solar cell structure is shown in Figure 1.1. To appreciate the quantity of solar energy available, it is

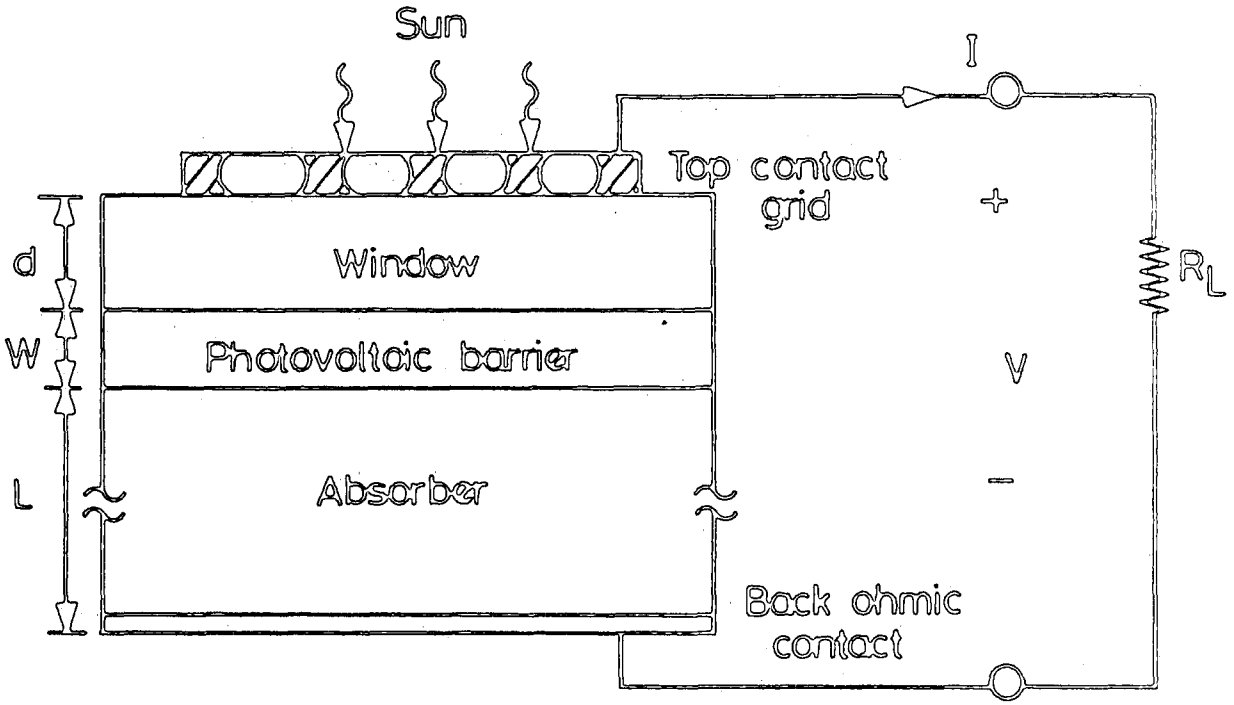


Fig 1.1 : Schematic diagram of a general solar cell structure (Ref 3)

found that on a bright summers day at noon the solar energy falling on the earth's surface is about 1000 watts per square metre. If this amount of solar energy falling on a single square metre could be converted completely into electricity, then this could power ten 100 watt bulbs, or two furnace motors, or several 25 inch television sets [2].

Photovoltaic systems have many advantages; in addition to being very reliable, they are clean power sources utilising renewable energy. Operating and maintenance costs are expected to be low because of the simplicity of photovoltaic system designs. Photovoltaic energy conversion is used today for both space and terrestrial solar energy conversion. The success in space applications is well known (communication satellites, manned space laboratories) and the use of solar cells in terrestrial applications becomes clearer with their use in radios, calculators, watches, water pumping, the lighting industry ... etc [4,6]. Table 1.1 lists examples of present terrestrial applications of photovoltaic systems and devices.

1.2 Background

Solar cells depend upon the photovoltaic effect for their operation. This effect has been known for about 150 years. It was reported initially in 1839 by Becquerel [7] who observed a light-dependent voltage between two metal electrodes placed in an electrolyte solution. Willoughby-Smith [8] discovered photoconductivity in selenium in 1873 and Adams and Day [9] observed it in solid selenium three years later. Many of the subsequent solid state workers including Hallwachs [10], Lange [11], Grondahl [12], and Schottky [13] prepared photovoltaic cells on selemium and cuprous oxide. However, the photovoltaic effect is essentially different from the Dember [14] effect which is the production of a potential difference across a photoconductor by non-uniform

APPLICATION	COMMENTS
I Large land installations	
Building power systems	Provide power to single-family homes, apartment, public, or commercial buildings. Often installed on rooftops. [1 to 100s of kW].
Central power station	Feeds ac power to utility grid for transmission and distribution. [MW to multi-MW].
Forest Service lookout	Supplies lights, communications, refrigeration; energy storage desirable.
Military installations	For remote site; solar and wind power complementarity useful to provide more continuous supply. Grid connection, ac or dc output possibly useful. Storage likely necessary.
Village power system	Water pumping, refrigeration, lighting, communications. [0.1 to 100s of kW].
Water pumping systems	Mobile systems with no storage, to multi-kW fixed systems that may be grid-connected or independent, operate on ac or dc. [power to multi-kW]
Water purification	[multi-kW].
II Communications equipment	
Emergency or remote telephone	Energy storage desirable or necessary.
Emergency or portable radio	Storage desirable or necessary. [power to 50 W useful].
Microwave telephone repeater station	Storage necessary; dc output usable.
Military radar installation	Storage necessary. [multi-kW].
Radio broadcast station	Storage or grid connection as back-up necessary; dc output usable. DOE demonstration project as described in text. [multi-kW].
Railroad telephone system	For communications between caboose and engineer on train.
Television receiver in village	[50 W usable].
III Remotely sited equipment of all kinds	
Alarms	Intrusion, smoke, and fire alarms. Energy storage necessary. [watts].
Cathodic protection system	To prevent corrosion of pipelines, bridges, and structures. Energy storage desirable; usually no grid connection.
Desalinization system	Electricity used for pumping: may be tolerant to fluctuating supply of energy.
Electric cattle fence	Dc output usable; energy storage necessary; usually no grid connection.
Highway dust storm and other warning signs	Energy storage necessary. [watts]
Naviagation aids for boats, ships, aircraft	Energy storage necessary. [10s of watts].
Offshore or remotely sited landbased equipment.	Lighting, refrigeration, communications equipment; storage desirable.
Scientific instrumentation for field use	Remote recording or telemetry; storage desirable.
IV Miscellaneous	
Airplane	Ultra-light "Gossamer Penguin" in 1980 flew powered directly by solar cells without battery storage.
Electronic calculator	Powered by room lights. Energy storage not necessary. Low efficiency cells may be used.
Electronic watch	Solar cells used to recharge battery.

TABLE 1.1 : Examples of terrestrial application of solar cells, typical power levels for some application are given in braces (Ref 5).

illumination. In this effect electrons having the higher mobility diffuse away from the surface more quickly than holes. So the differential diffusion will tend to make the surface more positive than the bulk, in the absence of any other effect. The direction of the resulting electric field is such as to accelerate the lower mobility carriers and to slow down more mobile ones resulting in no net current.

There after a variety of materials and devices were investigated, but it was not until 1954 that work directed towards the fabrication of devices utilizing the photovoltaic effect was reported in the literature. In that year Reynolds et al [15] obtained about 6% conversion efficiency with a Cu_2S-CdS p-n heterojunction. In the same year Chapin et al [16] reported a high efficiency solar cell (6%) using a diffused silicon p-n homojunction. A couple of years later Jenny et al [17] obtained a 4% solar conversion efficiency from a GaAs based solar cell. With these pioneer studies, the foundation was laid for the further development of a photovoltaic device technology. The first assessments of device requirement [18,19] suggested that the optimum band gap energy for a p-n junction solar cell should be $\sim$1.5eV. It was Wolf [20] who first suggested the use of a heterojunction cell with a wide bandgap surface layer as one of the ways of improving the conversion efficiency. Many materials were investigated for use in thin film solar cells and these included amorphous silicon, II-VI (CdS), III-V (InP), ternary ($Cd_yZn_{1-y}S$)and II-III-VI_2 compounds ($CdInSe_2$) [21].

Following the work of Reynolds [15] in 1954, CdS solar cells were made by low cost techniques and became highly promising for commercial production. Williams and Bube [22] (1960) compared electroplated junctions of several metals on CdS. Then Shirland et al [23] (1965) and Shiozawa et al [24] improved the technology of CdS-Cu_2S heterojunctions which were developed into thin film devices with efficiencies in excess

of 9.1% [25] in terrestrial sunlight.

More recently, problems with the stability of CdS-Cu_2S cells have led to the development of cells based on other materials. These, together with their efficiencies include single crystal GaAs [26] (26%), Silicon [27] (22%), CdTe [28] (12.8%) and $Cd_yZn_{1-y}S$ [29] (10.2%).

1.3 Solar Cell Materials

As stated above, a wide range of materials is employed in solar cell configurations. The two most important elements of a solar cell are the 'absorber', in which light-induced transitions produce mobile charge carriers, and the 'window' material which forms the other limb of the junction. The choice of these two elements is influenced by their energy gaps, their absorption coefficients at wavelengths corresponding to the solar spectrum and the diffusion lengths of minority carriers in the two materials. For the absorber, small band gap materials produce more photocurrent while, in order to obtain a large value of open circuit voltage, a window material with a large band gap is required. The dependence of the maximum conversion efficiency on the band gap for different absorber materials is shown in Figure 1.2. The physical location where photon absorption takes place in the solar cell is governed by the absorption coefficient (α) of the absorber material, so this part of the solar cell should have a high value of absorption coefficient to ensure the optimum conversion of the incident photon flux to electrical energy. The magnitude of α depends on the physical structure of the material, on the densities of states in the conduction and valence bands, on the direct or indirect nature of the band gap transitions and on the photon wavelength. Consequently, to achieve 90% of the maximum possible output from a solar cell, the energy gap of the absorber should be between 1.0 and 1.7eV

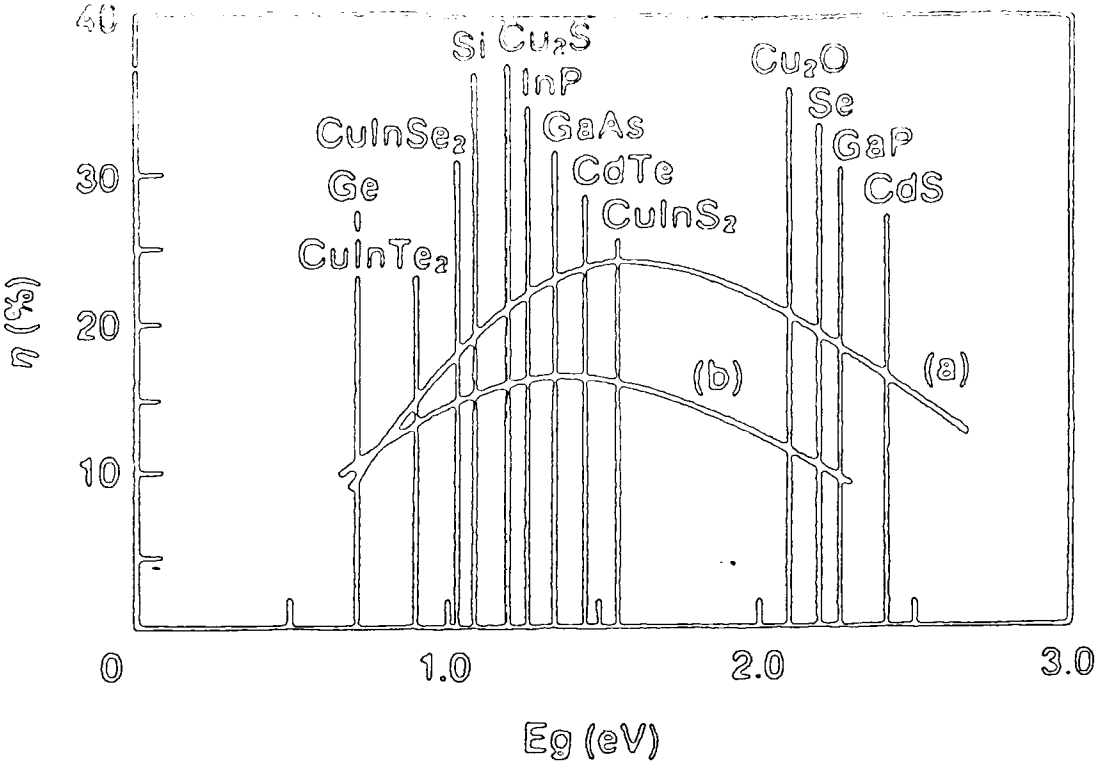


Fig 1.2 : Dependence of maximum conversion efficiency on semiconductor band gap a) for A = 1 for injection dominated current regime and
b) for A = 2 for the regime dominated by the recombination in the depletion layer (Ref 19)

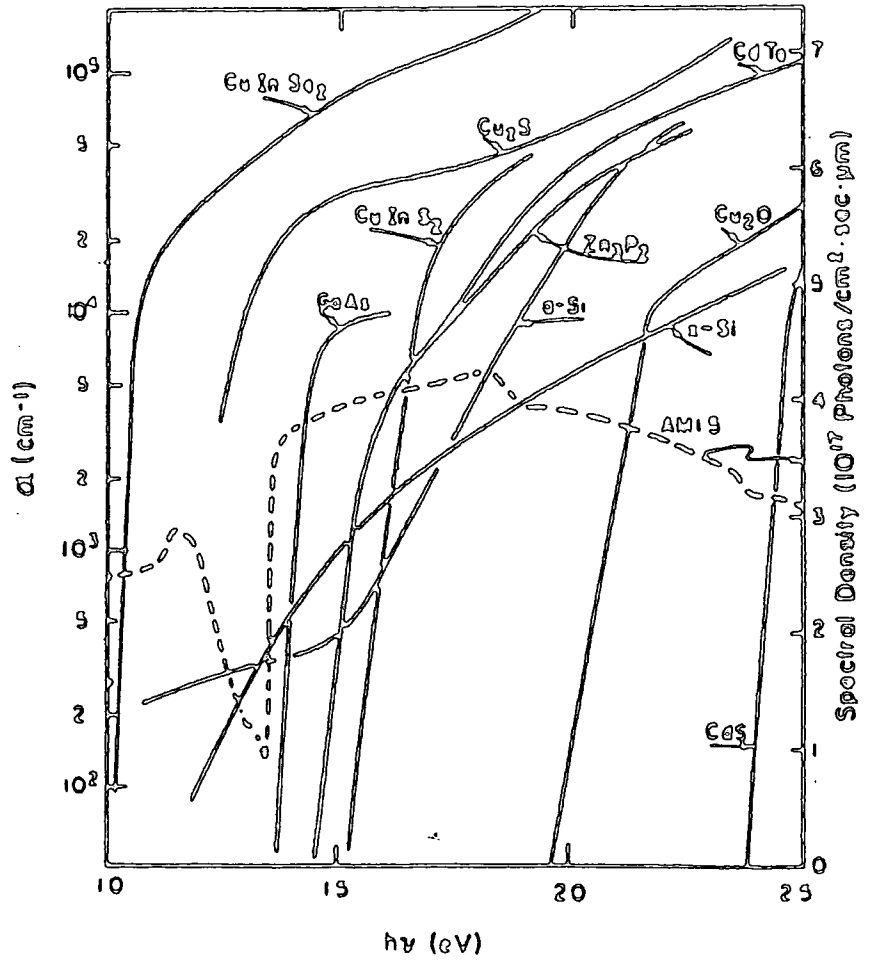
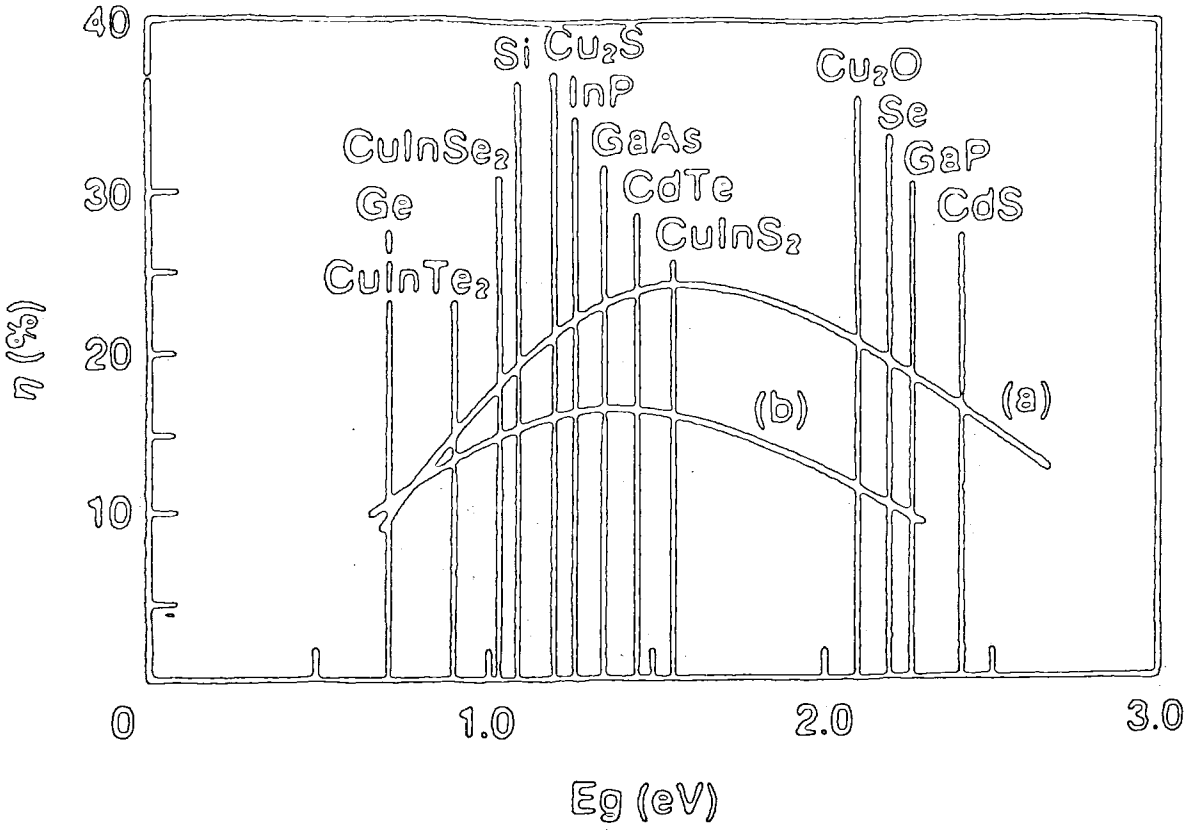


Fig 1.3 : Optical absorption coefficient vs. photon energy for various semiconductors (Ref 30)



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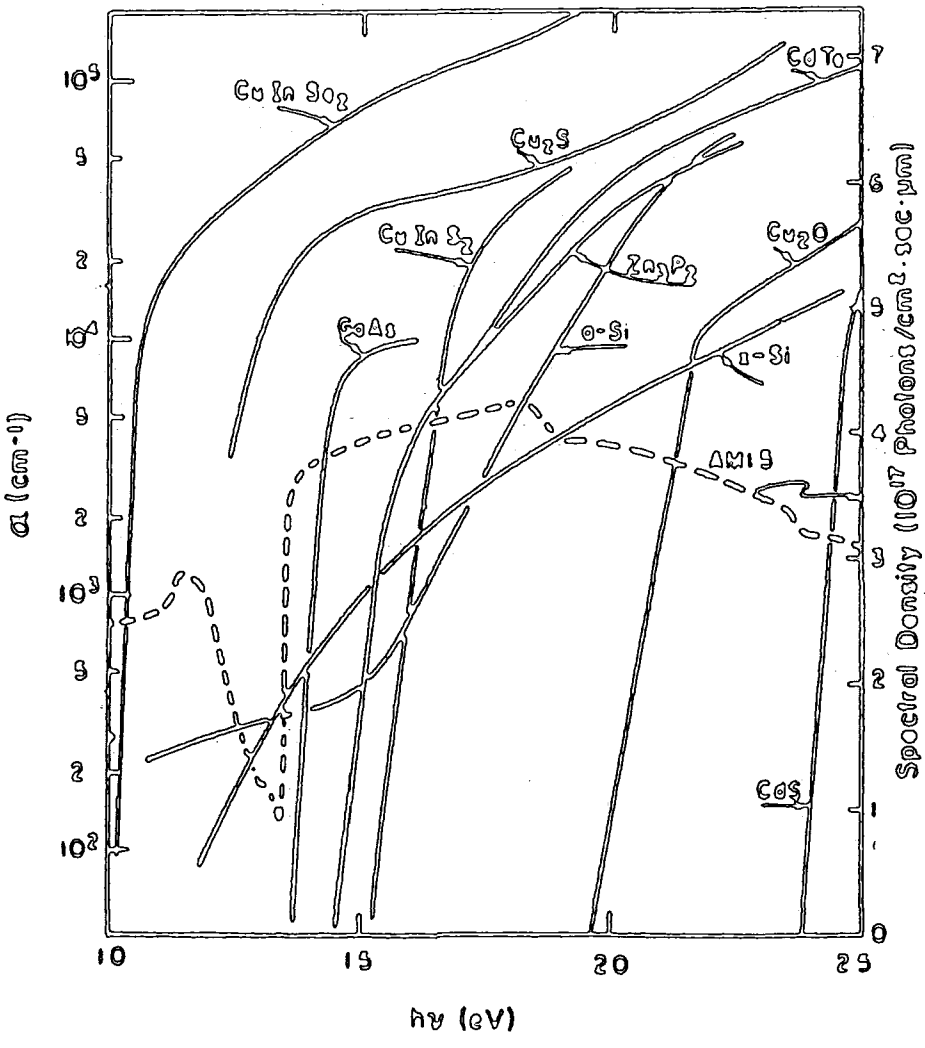

Fig 1.3 : Optical absorption coefficient vs. photon energy for various semiconductors (Ref 30)

and the carrier diffusion length should be at least twice the thickness required to absorb 90% of the incident photon energy [30]. Figure 1.3 shows the optical absorption coefficients plotted against photon energy for various semiconductors. The diffusion length can be defined as the mean distance a charge carrier (free electron or hole) moves before recombining with another hole or electron. These distances are short, typically ranging from several to a few hundred μm. Cell efficiency improves with increasing carrier diffusion length. The most important part of a solar cell is the junction between the window and absorber materials where the generated minority carriers are collected and converted into majority carriers. The presence of a potential barrier at this junction inhibits the back flow of carriers. One major factor which influences the efficiency of the device is recombination of carriers i.e. not all the electron-hole pairs created actually reach the junction field, because some of the carriers recombine with others of opposite sign, thereby eliminating both. This usually happens at a defect or impurity called a recombination centre. The recombination lifetime therefore depends on the density of defects and on their capture cross sections for carriers.

For heterojunction solar cells, a good electron affinity and lattice match between the two semiconductors, and a high carrier mobility in the region of the junction are preferable. These parameters play an important role in determining the device performance and efficiency. Any mismatch between the lattices of the two semiconductors leads to a high density of interface states which causes the generated carriers to recombine at the interface before they can be collected.

1.4 Junctions Used In Solar Cells And Cell Types

All solar cells require a junction which is capable of separating

the electrons and holes that are produced by light incident on the absorber. The types of interface structure that are used can be designated as

i) p-n homojunctions

ii) p-n heterojunctions; and

iii) metal semiconductor junctions.

A p-n homojunction essentially consists of one semiconducting material which is fabricated such that it has two regions of different conductivity type, i.e.n and p. The junction is formed at the position where the conductivity changes from one type to another. In a homojunction, the light is incident through a contact grid on a thin layer of one conductivity type (usually n- type). The obvious advantage of using a homojunction is that it is free from the problems of lattice and electron affinity matching. However, such junctions are limited to just a few materials which are amphoteric, i.e. which can be made both n and p type. The most widely studied homojunctions for photovoltaic applications include single crystal silicon, amorphous and polycrystalline silicon, gallium arsenide and cadmium telluride.

A heterojunction is a junction formed between two semiconductors having different band gaps and where usually one is p- type and the other is n- type. Heterojunction p-n solar cells can be formed from two absorbers so that electron-hole pairs are created in both semiconductors or, more commonly they can be of the form of window and absorber where electron-hole pairs are created in just one of the semiconductors. The light is incident on the heterojunction in two possible configurations, either through a grid on the larger band gap material, in which case the device is designated as a backwall cell, or alternatively through a grid on a thin layer of the smaller band gap material, thereby forming a frontwall cell. Heterojunction devices provide

a wide scope for materials, and a great deal of design flexibility. If the top material has a wide band gap it serves as a window to let the light penetrate to the absorber layer beneath. With a judicious choice of materials, a device can be formed with a large built-in potential, and hence a higher open circuit voltage than with a homojunction made from the narrow band gap semiconductor. To form a good quality heterojunction, the following requirement should be satisfied. These are:

i) the lattice constants of the two materials should be nearly equal

ii) the electron affinities should be compatible; and

iii) the thermal expansion coefficient of the two semiconductors should be similar.

The mismatch of lattice constants and a difference in thermal expansion coefficients can lead to interfacial strain at the heterojunction interface, giving rise to interface states which act as trapping centres. A difference in the electron affinity of the two semiconductors can cause an energy discontinuity in the form of a spike in one or both of the energy bands in an abrupt heterojunction [31].

Fonash and Rothwarf [32] listed the advantageous features of heterojunction cells to show how they are so useful and why they are particularly promising for economic reasons. The more important of these advantages are:

i) heterojunction structures allow the use of semiconductors that can only be effectively doped either n- or p-type, but yet have attractive properties of cost considerations;

ii) heterojunction structures enable devices to be fabricated using wide band gap materials that can serve as barrier-formers as well as reducing recombination losses at surfaces, interfaces and ohmic contacts;

iii) heterojunction structures have effective force fields [33] in addition to the electrostatic field and these may be used to assist in the collection of photocarriers, and

iv) the presence of these effective force fields can give rise to additional photovoltage [33].

In fact, the most promising combination of semiconductors for heterojunctions from the view point of the lattice match, electron affinity and predicted efficiency are $Ga_{1-x}Al_xAs$ - GaAs, ZnSe - GaAs, GaP-Si and ZnS-Si [34]. The thin film CdS-Cu_2S solar cell has also been considered to be very promising [35] and is expected to be $\sim$15% efficient under optimised conditions of fabrication. The lattice mismatch and the difference in electron affinity can both be minimized by alloying the CdS with ZnS. The efficiencies and other operational parameters for a range of different cells are shown in Table 1.2.

Finally, in metal-semiconductor or Schottky barrier, a potential drop occurs in the interfacial region between the metal and semiconductor as a result of the difference in work functions. The barrier height is the energy difference between the work function of the metal and the top of the valence band (for a p-type semiconductor) or the bottom of the conduction band (for n-type). In the Schottky barrier it is possible to have the light incident either through the semitransparent metal forming the barrier (frontwall) or through the semiconductor (backwall). The problem is that the resultant efficiency is usually limited to low values.

There are a number of other semiconductor junctions that have been considered for the use in solar cells. Two promising devices are the metal-insulator-semiconductor (MIS) and semiconductor-insulator-semiconductor (SIS) junctions where a thin insulating layer is formed between a semiconductor and a metal or between two semiconductors.

Material	V_{oc} V	J_{sc} mA/cm^2	FF	η %	Area, cm^2	Remarks
Silicon	0.622	34.3	0.796	16.8	2	p^+-n-n^+
Silicon	0.621	36.5	0.806	18.3	2.8	MIS, active area
Silicon	0.540	32.7	0.76	13.3	2.8	semicrystalline, MIS
Silicon	0.572	24.2	0.76	10.5	5	silicon-on-ceramic
Silicon	0.522	28.1	0.79	11.5	11.4	ITO/semicrystalline
Amorphous-Si	0.84	17.8	0.676	10.1	1.1	a-SiC/a-Sip-i-n
Amorphous-Si	0.880	13.1	0.57	6.6	0.73	MIS
Amorphous-Si	0.878	11.1	0.66	6.4	1.2	p-i-n
GaAs	0.93	28	0.81	18.2	1.5	AlGaAs/GaAs
GaAs	1.05	270	0.85	23	1.5	AlGaAs/GaAs,10X
GaAs	–	–	–	21	–	AlGaAs/GaAs, 1000X
GaAs	0.95	23	0.78	17	0.5	CLEFT
GaAs	0.76	24.4	0.63	12	0.1	on Ge-coated Si
AlGaAs/GaAs	2.05	10.8	0.74	16.5	4.0	tandem cell
GaAs	0.56	22.7	0.67	8.5	9	CVD thin film, MIS
Cu_2S/CdS	0.52	24.8	0.71	9.2	1	solution ion-exchange
Cu_2S/ZnCdS	0.6	22.8	0.75	10.2	1	16% Cd, 84% Zn
$CuInSe_2$/CdS	0.4	38	0.63	9.4	1	evaporation
$CuInSe_2$/CdZnS	0.431	39	0.631	10.6	–	20% Cd, 80% Zn
CdS/CdTe	–	–	–	10.5	–	thin film
CdS/CdTe	0.79	–	–	8	–	electrodeposition
CdS/InP	0.63	15	0.71	12.5	0.23	single crystal InP
InP	0.66	24.8	0.64	11.5	–	PEC
WSe_2	0.72	22.6	0.57	10.2	–	PEC
$MoSe_2$	0.65	25	0.56	9.4	–	PEC
CdTe	0.723	18.7	0.64	8.6	0.02	electrodeposition, Au/CdTe
CdSe	0.57	23.8	0.48	6.5	1	electrodeposition
CdSe/ZnSe/Au	0.6	20	0.45	5.0	0.01	
CuTe/CdTe	0.59	13	0.63	4.8	6	
Zn_3P_2	0.48	18	0.55	4.3	1	Mg/Zn_3P_2 thin film
$CuInS_2$/$CuInS_2$	0.41	19	0.43	3.3	0.12	
Merocyanine/Al	1.2	1.8	0.25	0.7	1	

TABLE 1.2 : Operational parameters for a range of different solar cells (Ref 5).

An efficiency of 7% using an MIS device has been achieved with CdSe [36]. When describing types of cell it is usual to consider each material and its degree of crystallinity as illustrated in Figure 1.4. Thus there are

i) single crystal cells which are free from grain boundaries where the structure approximates to an ideal lattice. However, such cells are expensive to produce, though their superior efficiencies warrant their use in space applications.

ii) cells fabricated from polycrystalline material containing individual grains with diameters ranging from a fraction of a micron to millimetres. The grain size of such materials depends not only on the material itself but also on the processing technique used to fabricate it into a solar cell;

iii) cells formed from amorphous material in which there is only short-range order, that extends over a few atomic distances. These are promising because of their low cost. In particular, amorphous silicon cells already form a major part of the photovoltaic industrial activity and they are likely to continue to be important for some years to come.

1.5 Recent Developments In Photovoltaics And Economic Views

Photovoltaic technology has developed extensively over the past fifteen years or so. Solar cells have been used for several years in terrestrial applications where they are economically competitive with alternative electrical energy sources particularly in remote locations. It is expected that the market for solar cells will expand rapidly as the cost of the power from conventional and non-renewable sources rises, while that of solar cells should fall in real terms because of technological improvements and the economies of large scale

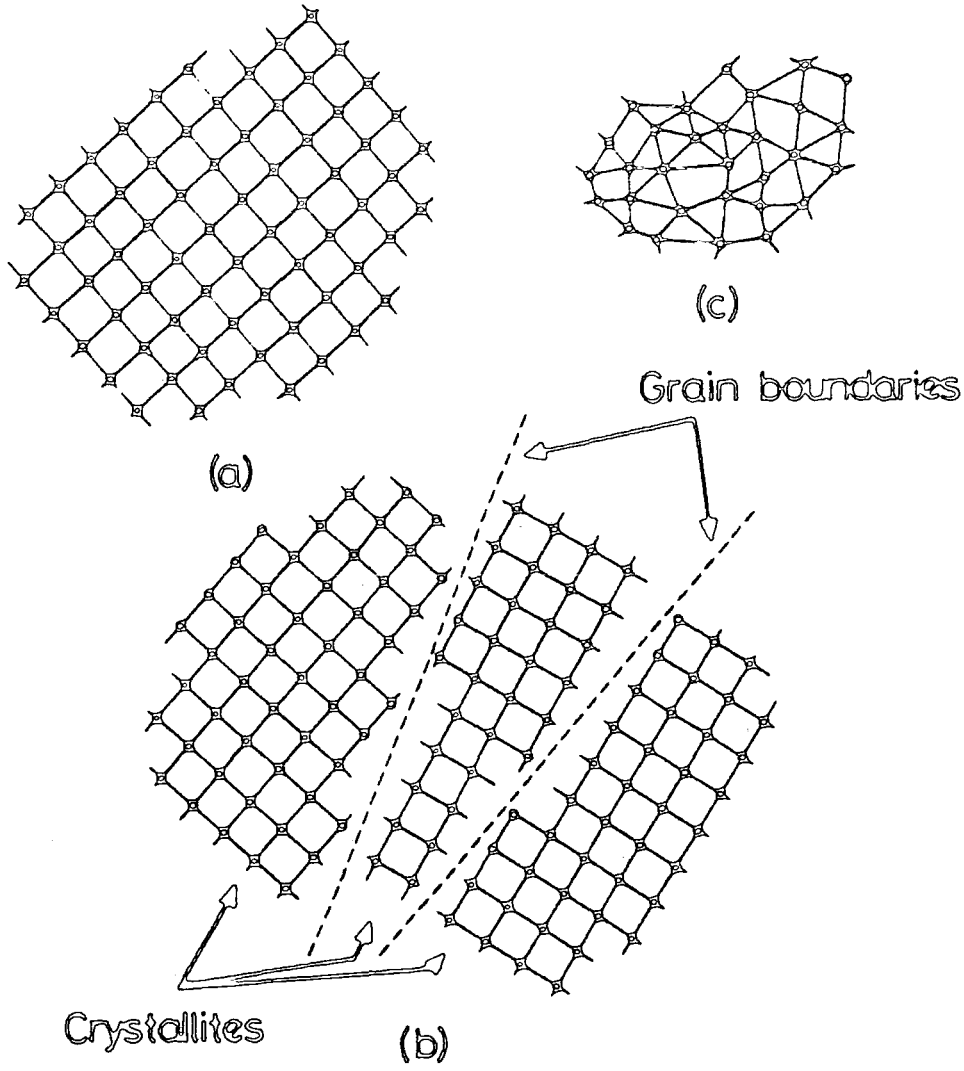

Fig 1.4 : Portions of (a) single crystal (b) polycrystalline (c) amorphous solids (Ref 5)

manufacture. The largest photovoltaic generator plant (1MWDC) has been installed by Arco Solar Inc. in Hesperia in Southern California [37]. More recently (1986) Overstraeten and Mertens [38], have compiled a list of pilot projects co-funded by the CEC and built under their auspices. The location, application, total rated power and its conditioning system are summarised in Table 1.3.

The price of photovoltaic energy continues to decline. For example in 1956 silicon single crystal homojunction cells cost 350$ per peak watt. By 1966 the cost had dropped to 100$ per peak watt through improved processing and technology [39] and by 1977 it was below 15$ per peak watt for arrays. The production of polycrystalline silicon cells in the USA increased by one third from 1984 to 1985 (from 1.8 to 2.4 MW), while production of single crystal photovoltaic cells dropped by 19% (from 6.6 to 3.35 MW). On the other hand, work on amorphous silicon photovoltaics is expanding at a fast rate [40]. In the USA the production of amorphous Si increased six-fold from 1984 to 1985 (from 0.1 to 0.6 MS) [40]. Present investigations suggest that the cost of photovoltaic plants in the Megawatt range would be of the order of 10.0 ECU per kW, with a conversion efficiency well about 10% [41]. It is generally agreed that photovoltaic systems in favourable locations would be economically competitive with other generating technologies, if the capital cost of the photovoltaic plant were in the $2.0-4.0/W range [42]. By the year 2000, the USA photovoltaic program aims to reduce the price of photovoltaic energy to 0.1 to 0.3$ per peak watt at 10^{10} per watts per year [43]. Over the expected lifetime of an installation, this level should provide electricity at a cost equivalent to 0.04 to 0.06$ per kWhr for projections 20 years hence [43]. Hay et al [44] compared the energy consumption in the fabrication of four types of cell, namely these based on single crystal silicon, ribbon

TABLE 1.3: List of pilot projects co-funded by the CEC and built under their auspics (Ref 38)

Site	Total rated power (KWp)	Application	Power conditioning system
Pellworm Island, Germany	300	The plant covers the electrical needs of the Pellworm recreation centre. The power surplus is fed into the grid. The appliances include heat pumps and water pumps for the swimming pool, TV sets, radios, stores, lighting, etc.	Two self-commutated invertors of 75 kVA to feed the load. One line-commutated invertor, 400 kVA, to feed surplus energy into the grid.
Kythnos Island, Greece	100	Supplies energy to the 15 kV network, in parallel with diesel power station and wind generators It saves costly diesel fuel.. It also tests the combination of wind generators and photovoltaic convertors.	Four DC/DC convertors each 25 KW with integrated MPPT to charge the batteries, three self-commutated invertors, each 50 kVA to feed into the grid.
Chevetogne, Belgium	63	The plant is installed on a 500 ha Provincial Domain with camping grounds and sports centre. An outdoor swimming pool is heated by solar thermal collectors. The photovoltaic system provides energy for the pumps of the solar thermal plant (40 kW) and for lighting (23 kW) at night.	Two self-commutated invertors, each 20 kVA to supply the pumps One self-commutated invertor 20 kVA for lighting. Surplus energy is fed into the grid.
Aghia Roumeli, Greece	50	The plant meets the electrical needs of a small Cretan village located 15 km from the nearest grid. The electricity is used for the electrification of homes shops and hotels (lighting, water pumps, cold stores, refrigerators and other appliances).	One self-commutated invertor 40 kVA to feed the grid in a stand-alone mode.
Mont Bouquet, France	50	The aim is to partially power an emitter station of Telediffusion de France with three radio and three TV emitters. In the future, similar stations with lower consumption equipment could be powered by photovoltaic energy only.	One self-commutated invertor 30 kVA.
Nice Airport France	50	The energy is used to power the electronic equipment of the control tower and ground signalling. These applications require an electricity supply free of distortion and microcuts.	One self-commutated invertor 5 kVA, monophase 220 V output. One battery charge 7 kVA, working in parallel with the photovoltaic array during sunless periods.
Fota Island	50	Electricity is supplied to a dairy farm with, as a load, milking machine motors, cooling motors and washing machines. The power needs of the dairy industry correspond to the seasonal variation of the available sunlight.	Three self-commutated invertors, 10 kVA each, to feed the loads. One line-commutated invertor 50 kVA to deliver surplus energy to the grid.
Terschelling, Holland	50	The photovoltaic plant is used in combination with a wind generator of 40 kW. The system supplies 95% of the power needed by a school for maritime studies. It is also connected to the grid.	29 MPPT, one without MPPT, one load-commutated invertor (60 kVA) for grid connection, one synchronous motor (50kVA) for stand-alone operation and for power factor correction.
Kaw, French Guiana	35	The electrification of a small village (70 inhabitants) remote from the grid. Diesel generators are too expensive. The energy is used for lighting streets, a school, a church, private homes and for refrigerators and cold stores. The scheme aims to stop the rural exodus by improving the living conditions.	One self-commutated invertor (40kVA) to feed the grid in a stand-alone mode.

TABLE 1.3 contd....

Site	Total rated power (kWp)	Application	Power conditioning system
Hoboken, Belgium	30	The photovoltaic power is used for the production of hydrogen by electrolysis of water. Surplus power is used for pumping water. The loads are coupled directly to the photovoltaic array, without convertors, invertors or batteries.	Three DC/DC convertors, 750 W each for powering the monitoring and control equipment.
Marchwood, United Kingdom	30	The plant is constructed on a power station site. The power output is integrated into the local distribution system either to supplement the power taken from the national grid or to support individual, isolated, selected loads. The plant's scheme facilitates four modes of operation: grid connected with or without battery storage connected and stand-alone mode with or without battery storage connected.	One self-commutated invertor with integral MPPT.
Tremiti Island, Italy	65	The system provides drinkable water by sea water desalinataion, using the reverse osmosis process. It is a stand-alone plant. The main loads are pumps with voltage and frequency controlled AC motors.	Three DC/DC convertors, each 25 kW with MPPT. Several variable frequency and voltage invertors, approx 5KVA each.
Giglio Island, Italy	45	The power is used for a water disinfection system and for a food cold store. A commercial ozoniser is used for the disinfection.	DC/DC convertors with MPPT, one invertor 12 kVA for the cold store unit and one invertor 3.5 kVA, for the ozoniser unit.
Vulcano Island, Italy	80	The plant can either supply power into the grid in parallel with an existing diesel station or feed a group of 30 isolated homes.	One line-commutated invertor 80 kVA with MPPT, one rectifier to charge the battery from the grid, one self-commutated invertor, 40 kVA, to power isolated consumers.
Rondolinu (Corsica), France	30	It is a stand-alone plant to power a remote village. The power is used for electrification of the homes, public lighting and for a submersible water pump to supply potable water. It brings the possibility of developing a cottage industry and starting some touristic activities.	One self-commutated invertor, 50 kVA, to feed the village grid in a stand-alone mode.

silicon, amorphous silicon and CdS-Cu_2S. They found that the CdS-Cu_2S cell requires less energy for its preparation than any of the other. The prime advantage of CdS-Cu_2S cells is due to the low cost of processing and the use of relatively low cost materials. Thin film CdS-Cu_2S heterojunction material is one of the few commercially available alternatives to silicon cells at the present time. The total estimated production cost for CdS-Cu_2S thin film cells is \$0.18/peak W of which 32% is material cost and 25% is labour cost [5]. One proposal for minimizing the interface and electron affinity problems is to introduce some zinc into the CdS as was first suggested by Palz et al [45]. However, this modification has not led to significant improvements in device performance.

1.6 Scope Of The Present Work

The work reported in this thesis is primarily concerned with the application of the electroplating technique to the formation of Cu_2S on thin film and single crystal CdS, and on $Cd_yZn_{1-y}S$ single crystal substrate to produce heterojunctions. The effects of the plating bias, the ambient in which the annealing was carried out, and the period of annealing on the phase of copper sulphide and on the electrical properties for these devices have been investigated. Chapters 5,6 and 8 are concerned with CdS-Cu_2S single crystal, thin film and $Cd_yZn_{1-y}S$-Cu_2S devices respectively. The combined effects of the substrate and annealing ambient on the characteristics of CdS-Cu_2S thin film heterojunction have been studied. Chapter 7 described the degradation behaviour of CdS-Cu_2S single crystal cells as a function of illumination and ambient. Also in Chapter 7, the mechanism of dark current conduction is reported as a function of the value of electroplating bias. Chapter 8 records a study of cells based on $Cd_{0.8}Zn_{0.2}S$ substrates.

This includes the influence of the plating and heat treatment on the properties of the copper sulphide phase, and on the characteristics of the heterojunction devices formed. Steady state photocapacitance studies were carried out on these devices as a function of the ambient and the period of annealing.

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CHAPTER TWO

Material Aspects Of CdS Based Solar Cells

2.1 Introduction

The CdS-Cu_xS cell has a history of development going back to 1954 when Reynolds et al [1] first discovered a photovoltaic response in heat treated Cu contacts on CdS. Since then there have been several attempts to produce a commercial solar cell based on this material. Until a few years ago the CdS-Cu_xS solar cell was the most widely studied heterojunction, and this system has been the subject of many experimental studies and theoretical models. However in 1960, Williams and Bube [2] were the first to point out the importance in the photoresponse of the cell of copper, to which they attributed the long wavelength response, i.e. at a photon energy less than the CdS bandgap. Woods and Champion [3] investigated the operation of the Cu-CdS device and this work was followed by that of Fabricius [4] and Grimmeiss and Memming [5] who reported that the magnitude of the response of the cell in the infra-red region was increased two fold by the simultaneous illumination with green light. They attributed the long wavelength response to the excitation of electrons from the valence band to impurity states in the CdS.

The first heterojunction model for the CdS-Cu_xS cell was proposed by Cusano [6] (1963) who also suggested that the Cu_xS could be responsible for some of the long wavelength response. Hill and Keramidas [7] subsequently confirmed this suggestion, and Selle et al [8] demonstrated the importance of the Cu_xS in evaporated CdS-Cu_xS cells. The early work on the CdS-Cu_2S heterojunction was carried out by research groups at Harshaw , Clevite, ARL, RCA and Stanford University in the

U.S.A., S.A.T. in France, AEG-Telefunken in West Germany and IRD Ltd in the U.K. In 1968 the Clevite Corporation concluded a major investigation involving over two years study of the chemical, electrical and optical properties of CdS-Cu_xS solar cells, fabricated by dipping CdS polycrystalline films in a CuCl solution. An extensive review of the work on these cells has been given by Stanley [10]. The three fundamental parts of the device are

i) the Cu_xS absorber,

ii) the CdS window material, and

iii) the interface region.

This chapter provides a general review of the preparation and properties of cadmium sulphide, cadmium-zinc sulphide and copper sulphide for solar cell applications.

2.2 Preparation of CdS Single Crystals

Of the several methods of preparation of CdS single crystals, growth from the vapour phase is the most frequently used technique. In this method the compound sublimes at a relatively low temperature (700°C) under reduced pressure. This sublimation process was applied to the growth of single crystals by Piper and Polich [11], who used an open ended growth ampoule placed in a temperature gradient. Thus the material at the hotter end of the capsule sublimed to the cooler end where it condensed to nucleate a crystal which grew as the growth ampoule was moved through the furnace. A similar technique was subsequently used by Clark and Woods [12] who reported a relationship between the colouration and resistivity of CdS. This was such that material of dark colouration was of low resistivity and this was attributed to the presence of excess Cd. In an alternative method, Clark and Woods [13] employed a vertical growth system using sealed silica ampoules.

In this technique the ampoules were connected to a tail tube which contained a reservoir of cadmium or sulphur and which was held at a fixed temperature throughout the growth cycle. This allowed the partial pressure over the growing crystal to be adjusted, thereby providing a degree of control over its stoichiometry. It has been demonstrated that, unless the free silica particles (arising from glass blowing) are removed from the inside walls of the growth capsule, then a large density of voids result in the crystal. However, this problem may be overcome by an appropriate modification to the glass blowing procedure [14].

2.3 Preparation of CdS Thin Films

Thin films of cadmium sulphide can be deposited in many different ways, which strongly influence their physical properties. The perfection of the structure of the crystallites, their size and the degree of their preferred orientation depend on the experimental conditions of preparation [15]. The method chosen for deposition depends on a number of factors which are primarily concerned with optimising efficiency and reducing costs. Reviews of various growth techniques are given in books and papers such as those by Chopra and Das [16], Hill [17], Stanley [10] and Shirland and Rai-choudhury [18].

Since each technique can give rise to different grain size, impurities, dislocation densities, stoichiometry and composition of phases, it is not unexpected that the performance of the heterojunction depends strongly on its method of preparation.

Thermal evaporation is most frequently used for depositing films of CdS, and has been used in the present research. There have been many other methods developed for laboratory deposition of CdS and $Cd_yZn_{1-y}S$ films including spray pyrolysis [19-22], electrophoresis

[23], sputtering [24,25] or reactive sputtering [26] and sintering of screen printed layers [27]. Of these, only thermal evaporation has been used in this work and it is consequently discussed in some detail.

2.3.1 Thermal Evaporation Method

Thermal evaporation of CdS films has been the most popular technique of thin film production. This process involves the sublimation of cadmium sulphide powder from a heated source at about 1000°C, followed by condensation of the vapour onto a substrate held at 200°C. The dissociation of the CdS into its components occurs as follows:

$$CdS\ (solid) \longrightarrow Cd(g) + \tfrac{1}{2}S_2\ (g)$$

Rocheteau et al [28] have discussed in detail the thermal evaporation of CdS for large area solar cell applications. CdS usually grows preferentially with the hexagonal C-axis [0001] oriented perpendicular to the substrate. Its orientation depends on the position of the substrate. Further, it has been shown that the thicker the layer, the stronger is the preferred orientation [29]. When the CdS is deposited onto a heated substrate placed vertically above the source, the layer that results exhibits the hexagonal wurtzite structure with the fibre axis of the crystallites lying preferentially normal to the substrate. In general the C-axes of the crystallites tend to align themselves along the direction parallel to that of the incident vapour beam [17]. The properties of the film are influenced by many parameters, including the construction and design of the source, its temperature, the substrate temperature, evaporation rate, film thickness, the composition of the residual gas in the vacuum chamber and the surface finish and

properties of substrate. The effects of these parameters have been described by Stanley [10] and more recently by Bhandari and Karekar [30], and Szot and Haneman [31]. The design of the source is one of the most important factors which determines the deposition of uniform films reproducibly. Several different source designs have been described by Stanley [10]. The rate of evaporation, and therefore the deposition rate, changes exponentially with the absolute temperature. It is important therefore to ensure that there are no temperature gradients within the source. The size of the crystallites in the layer is a function of both film thickness and deposition rate [32,33]. The substrate temperature plays an important role in the properties of the film, particularly the degree of preferred orientation [33]. However, the optimum substrate temperature depends to some extent on the evaporation system used, and on the other deposition parameters. However, work in this laboratory has shown that the films grown at 200°C exhibit the best hexagonal structure with columnar grains extending from the top to the bottom of a layer [33]. In contrast, films grown at 150 and 240°C showed the presence of a cubic phase as well as a poor degree of preferred orientation. The resistivity of films generally decreases with increasing evaporation rate, but increases with increasing substrate temperature. Wilson and Woods [34] and Buckley and Woods [35] have reported the variation in the dark resistivity as a function of film thickness. They [34] found that the cells with the best values of efficiency were obtained using films 10-30μm thick with a resistivity of 10-100 Ωcm. The Hall mobility is usually dependent on the deposition conditions, and its values for good quality films vary from $40 cm^2 v^{-1} sec^{-1}$ to over $100 cm^2 v^{-1} sec^{-1}$.

Thermally evaporated filmshave been studied extensively for photovoltaic applications. Their main advantage is that layers can be produced for large area solar cells, and the method is a low cost one.

Even so, one disadvantage of this method is that only a few percent of the material used is deposited on the substrate.

2.3.2 Other Methods of Thin Film Deposition

Cadmium sulphide thin films can be prepared by many methods, and each has a strong influence on the materials properties. The choice of a specific technique is determined by the device requirements.

In sputter deposition a vapour species is created by gaseous ion bombardment of a target, comprised of the material to be deposited. The kinetic energy of the incident ions is sufficient to cause ejection of surface atoms, which subsequently condense on a substrate to form a film. In stead of using a high voltage to generate the bombarding ions, magnetron and r.f. sputtering can be used. The main advantages of sputtering are that up to 80% of material can be deposited over large areas; and this can be done at room temperature which often minimises diffusion problems. The electrical properties of films are essentially dependent on their thickness and the substrate temperature. However, the disadvantage is that it is difficult to produce a low resistivity layer and the structure of a film can be affected in the presence of a high electric field.

The method of silk screen printing has frequently been applied in the preparation of CdS layers for photovoltaic applications [27,39,40]. In this technique, the CdS is first ballmilled to a fine powder and suspended in a slurry, using either water or an organic solvent, to which a binding agent is added. Cadmium chloride is usually added to the slurry and acts as a flux for the crystallisation of the cadmium sulphide. This slurry is applied to a substrate through a screen of fine mesh [41]. It is then dried and fired at about 500-600^{o}C to produce the final layer.

CdS thin films can also be fabricated by spraying a solution of

a cadmium salt and a sulpha-organic compound onto a heated substrate using the pressure provided by a compressed gas [42,43]. The subsequent reaction on the hot substrate leads to the formation of a cadmium sulphide film and volatile products. The resultant film is usually very compact.

Electrophoresis has been employed for the deposition of CdS for photovoltaic applications as reported by Williams et al [23]. In this technique an electric field is applied to suspension of colloidal particles (sol) of CdS, which are deposited onto a conductive substrate that acts as an electrode. The 'sol' is made by the precipitation of CdS from the reaction between a cadmium compound such as cadmium acetate and H_2S. As the precipitated CdS particles are as small as a few hundred Å, recrystallization is a major problem with this method.

2.4 Properties of Cadmium Sulphide

Cadmium sulphide forms one limb of the CdS-Cu_2S photovoltaic cell, and its structural, optical and electrical properties must be known, since they can influence the conversion yield of this cell considerably. CdS is a II-VI semi-conducting compound which has a direct bandgap of 2.4eV and generally crystallizes in the hexagonal wurtzite configuration. As stated above, evaporated films of CdS exhibit a high degree of preferred orientation with the C-axis perpendicular to the substrate, although, under non-ideal deposition conditions, the zinc blende cubic configuration is adopted as well. The wurtzite structure is composed of two interpenetrating hexagonal close packed lattices displaced with respect to each other by a distance 3c/8 along the C-axis (Fig 2.1b) The zinc blende configuration is composed of two interpenetrating face centred cubic lattices translated with respect to each other by one quarter of a body diagonal (Fig 2.1a). The wurtzite and zinc blende configurations are both characterised by tetrahedral sites and in consequence, their nearest neighbour environment is identical, but positional

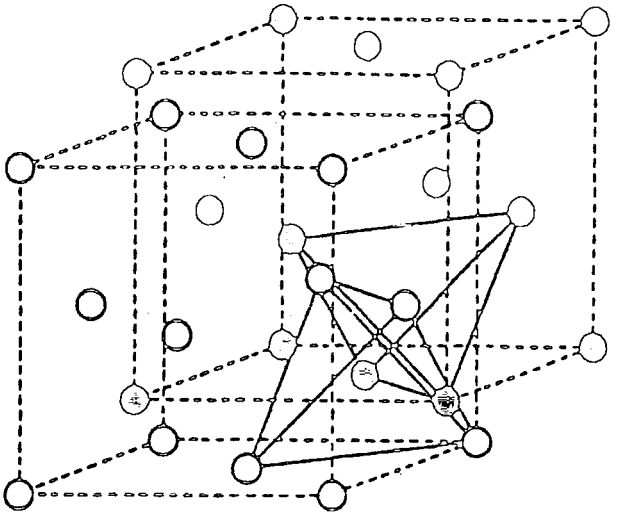

FIGURE 2.1a : The zinc blende structure

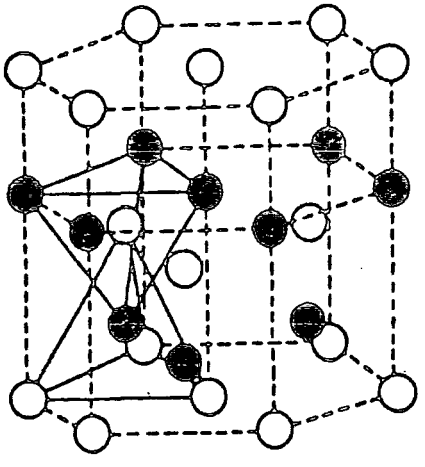

FIGURE 2.1b : The wurzite structure

and directional differences exist beyond the next nearest neighbours.

CdS can only be made n-type. It begins to sublime at about 700°C, and melts at about 1750°C under a pressure of many atmospheres. It can be grown from melt using a high pressure autoclave [44], but it is much easier to grow crystals from the vapour phase [12] as is done in this laboratory.

As the energy gap is direct with high densities of states in the conduction and valence bands, the absorption coefficient varies as the square of the incident photon energy and rises to very high values of $10^5 cm^{-1}$ for photon energies even slightly higher than the band gap. The mobility in single crystals is limited by ionized impurity scattering at low temperature and polar optical mode scattering at high temperature. In thin films there may be additional geometrical effects as well as intergranular boundaries which will limit the values of mobility. The electron mobility for CdS ranges from 100 to 400 $cm^2 v^{-1} sec^{-1}$ at 300K for single crystals whereas the hole mobility is about 20 $cm^2 v^{-1} sec^{-1}$. In thin films the mobility is commonly dominated by grain boundary potential barriers, and mobilities from well below 1 up to above 100 $cm^2 v^{-1} sec^{-1}$ can occur, depending strongly on the carrier density. CdS prepared for solar cell applications usually has a resistivity in the range of 1 to 10 Ω cm, with a carrier concentration between 10^{16} to $10^{18} cm^{-3}$ and a minority carrier diffusion length in the range of 0.1 to 0.3 μm. In addition to anion and cation vacancies and interstitials, as-grown CdS contains complexes associated with these defects. Generally, it has a low density of intrinsic carriers and its conductivity is completely controlled by the presence of native defects and impurities. Pyari [45] concluded that there are a large number of deep trapping levels in CdS which are filled or emptied by impact ionization or by thermal stimulation. With a knowledge of these trapping levels a better correlation between experimental and theoretical

results for tunnel-induced impact ionization is possible.

The conductivity of CdS is dominated by sulphur vacancies, i.e. excess which represents a deviation from stoichiometry. Romeo et al [46] found that the best CdS properties, as far as solar cells are concerned, were obtained for a Cd:S ratio of 1.5. CdS is easily doped with In,Sn,Al,Cl or Br, all of which form shallow donors. Sulphur vacancies act as donors and resistivites below 0.1 Ωcm can be obtained. Deep acceptor states are formed by Cu, Ag and Au impurities, and these readily compensate the native donors. The density of trapping states is related to the doping density [47]. The effect of doping on orientation is such that indium, copper, silver and gallium have little effect but chlorine destroys the preferred orientation of the C-axis [48]. For In doped material [49], the electrical conductivity is found to be temperature independent and the carrier concentration typically has a value of $n = 1.5 \times 10^{19} cm^{-3}$.

Several techniques have been used to characterise the localised levels introduced into the forbidden gap of pure or intentionally doped samples. These techniques include thermally stimulated conductivity (TSC), photo-decay, space charge limited currents (SCLC) [50,51], etc. More recently, methods such as admittance spectroscopy [52], transient capacitance measurement [53], photocapacitance [54], deep level transient spectroscopy (DLTS) [55,56] and Optical DLTS [57] have been applied to study the location and nature of the carrier trapping in CdS.

In summary, CdS has been thoroughly investigated over the last 30 years and it has been shown to exhibit many interesting phenomena such as high photoconductivity, acoustoelectric amplification, a large piezo-electric effect, laser emission and luminescence (thermo-,photo-tribo-,cathodo-, and electroluminescence) etc.

2.5 Deposition of Copper Sulphide

Copper sulphide can be deposited in various ways, but the two most successful techniques in the production of efficient solar cells are the so-called 'wet process' developed by the Clevite Corporation and the 'dry process' first used at the Philips Laboratory. Both of these methods depend on the ion exchange process.

In the wet process, the exchange reaction is produced by dipping the CdS into a cuprous chloride solution at a temperature of about 95°C. The reaction can be described as $CdS + 2CuCl \rightarrow Cu_2S + CdCl_2$. Many parameters must be controlled in this chemical displacement reaction, such as the pH, the concentration of the solution, the dipping time and the solution temperature [58,59].

The application of voltage to the CdS during the formation of the Cu_xS has been investigated by Nakayoma [60]. It was found that the structural, optical and electrical properties of Cu_xS are strongly affected by the value of the applied potential [61,62,63]. The technique has the advantage that the growth of Cu_xS at the CdS grain boundaries in the thin film solar cell can be inhibited [64], and the rate of Cu_xS growth can be controlled [65,66].

The second commonly used technique for the formation of Cu_xS is the dry barrier method, which was first used in 1975 by Te Velde [67]. Here, the CuCl is vacuum evaporated onto the CdS, then the chemical displacement reaction takes place by heating in an inert atmosphere at ~ 200°C for a few minutes, and finally the reaction product $CdCl_2$ is removed by washing the surface with absolute alcohol. The advantage of this method is that the reaction proceeds much more slowly than in the wet process, and penetration down grain boundaries is limited [17].

Copper sulphide layers can also be deposited by other methods.

For instance they can be formed by sputtering using a $Cu_{1.98}S$ target and an ambient H_2S and Ar [67]. Thornton and Anderson [67] have reported on all sputter deposited CdS-Cu_2S device. Copper sulphide can alternatively be grown by flash evaporation in a vacuum. This technique offers the advantage of allowing the properties of the Cu_xS layer to be studied separately. Using this technique, solar cells with 6% efficiency have been prepared. Also employing this method, Selle and Megge [68] have studied the effect of the depositional parameters on the stoichiometry of the Cu_xS, and they succeeded in producing layers of good stoichiometry.

Finally spray pyrolysis, in which copper and sulphur containing solutions are sprayed onto a heated CdS layer, has also been employed for cell preparation [19,69].

2.6 Properties of Copper Sulphide

The role of copper sulphide is very important, since this is responsible for nearly all of the light absorption and charge carrier generation which occurs in the CdS-Cu_2S cell. The layer is very thin, being of the order of 0.1-0.3μm, but the Cu_2S can penetrate several micrometers along grain boundaries into the CdS. The minority carriers generated in the Cu_2S diffuse to the junction, where they come under the influence of the electric field there, and are swept across the junction. The structural, optical and electrical properties of copper sulphide are discussed in the following sections.

2.6.1 Chemical and Structural Properties

It is well established that copper sulphide exists in a range of different phases such as Cu_2S, $Cu_{1.96}S$, $Cu_{1.8}S$ and CuS [60]. It is for this reason that the material is often referred to as Cu_xS.

The performance of the CdS-Cu_2S solar cell is very dependent on the stoichiometry of the copper sulphide formed during the fabrication of the device. The phase that is of most interest for photovoltaic applications is chalcocite (Cu_2S), and several workers have shown that the most efficient cells are fabricated with this phase [70,71]. It has been demonstrated that the efficiency of a photovoltaic device with chalcocite is about an order of magnitude higher than that of device with djurleite.

The phase diagram of the Cu-S system shown in Figure 2.2 demonstrates that at room temperature several phases are possible [72]. These include:

i) Chalcocite (Cu_2S) which has an orthorhombic structure at room temperature with lattice constants [73] of a = 11.84Å, b= 27.330Å and c= 13.497Å. At 104°C this phase transforms to hexagonal with a = 3.961Å and c= 6.722Å.

ii) Djurleite (Cu_xS, $1.93 \leq x \leq 1.96$), which is also orthorhombic at room temperature with lattice parameters of a = 15.71Å, b = 13.56Å and c = 26.95Å. It transforms to tetragonal at 86-93°C and to cubic at 100°C.

iii) Digenite, Cu_xS (x = 1.8) with a pseudo-cubic structure at room temperature with a = 5.56Å transforming to cubic at 78°C .

iv) Covellite (CuS) which has a hexagonal structure [74] with lattice parameters a = 3.66Å and c = 15.70Å.

Cook et al [73] found a mixture of phases of chalcocite and djurleite in the compositional range $1.960 < x < 1.998$, but the structure appeared to be hexagonal in the compositional range $1.8 < x < 1.96$. As the copper content of the Cu_xS phase decreases, the mismatch between the lattice parameters of the CdS and the Cu_xS increases, thus introducing a larger density of interfacial states at the junction [75].

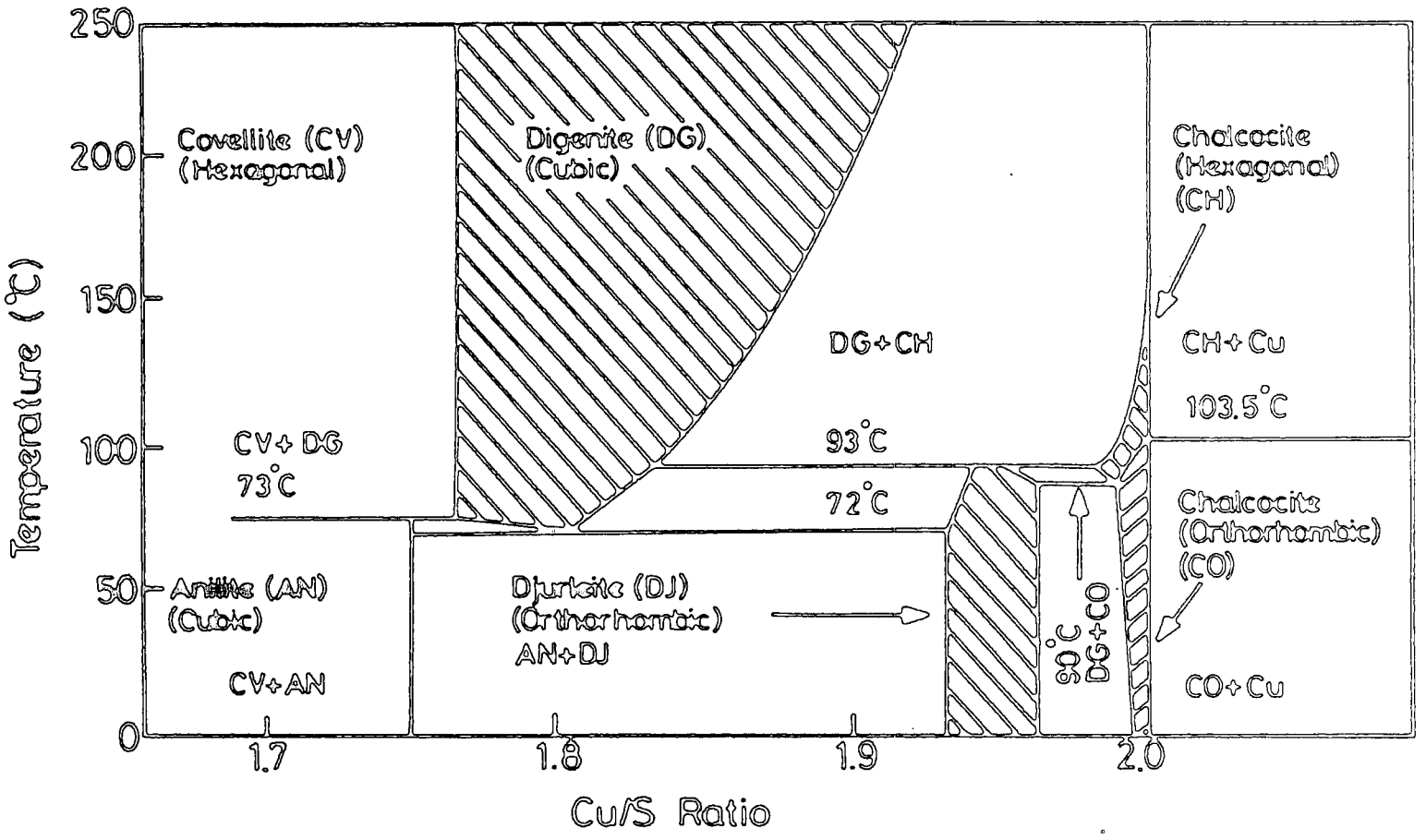

FIGURE 2.2 : The phase diagram of copper sulphide

The effect of heat treatment on the Cu_xS phases has been studied since 1941, and it has been found that the chalcocite degenerates to digenite when it was heated in air [76]. Recently it was reported that chalcocite can degenerate to djurleite on exposure to air for several months or after heating in air for a short period. These effects are attributed to the oxidation of the copper sulphide [77,78].

2.6.2 Optical Properties

Copper sulphide has a high optical absorption with an absorption coefficient between 10^4 and 10^5 in the visible region of the spectrum, and a high transmission in the infra-red. The value of the absorption coefficient strongly depends on the phase of copper sulphide, and as can be seen from Figure 2.3, the chalcocite phase has by far the best optical absorption properties for solar cell requirements.

In fact the absorption coefficients of the Cu_xS phases decrease as the x value decreases [75]. The region of the absorption spectrum that is the subject of much discussion is the absorption edge from which one can derive the width of the bandgap and determine whether it is direct or indirect.

The first attempt to specify the bandgap for chalcocite was made by Marshall and Mitra [79] in 1965 who found an indirect gap of 1.21eV at 300K, which increased to 1.26eV at 80K. However, while a lot of work has been done to investigate the optical properties (see for instance Mulder [80],) Eisenmann [81] showed that chalcocite was strongly absorbing with an indirect gap at about 1.2eV, and a direct gap at higher energy.

More recently [82], the optical and absorption constants for different phases of copper sulphide have been obtained. Also the effects on the diffusion lengths and lifetime of minority carriers of both heterojunction components in $CdS-Cu_2S$ of the surface recombination behaviour

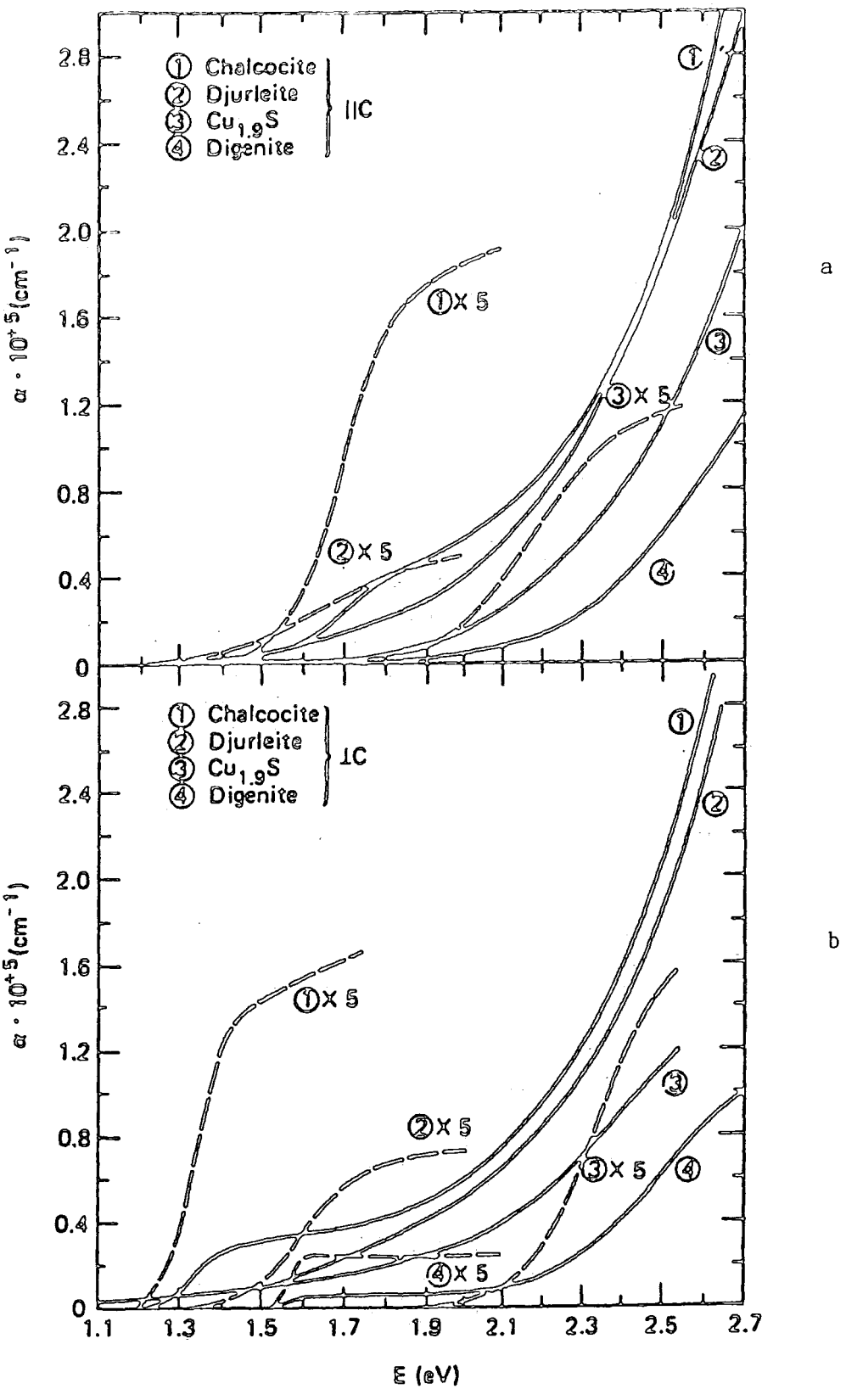

FIGURE 2.3 : The absorption coefficient as a function of copper sulphide phases (Ref 103).
The light coming a) parallel b) perpendicular to C-axis
——— sum of the direct and indirect bands
– – – indirect band only

are reported [82].

2.63 Electrical Properties

Copper sulphide is a p-type semiconductor in which copper vacancies act as acceptor centres. The electrical properties of Cu_xS have been studied by several workers who are listed in review articles such as those by Stanley [10], Hill [17] and Hill and Meakin [83].

Carrier densities observed commonly range from 10^{18} cm^{-3} to greater than $10^{21} cm^{-3}$. Hall mobilities reported are usually low; 3-30 $cm^2 v^{-1} sec^{-1}$ for single crystals and 2-7$cm^2 v^{-1} sec^{-1}$ for thin films. Thus resistivities usually range from 10^{-3} to $6 \times 10^{-1} \Omega cm$ for undoped material, and to more than $10^3 \Omega$ cm for Cd componsated material. Soriano et al [84] and Wagner and Wiemhöfer [85] found a strong dependence of the resistivity of Cu_xS on its stoichiometry with values of $3.5 \times 10^{-2} \Omega cm$ for x = 1.998 and less than $10^{-2} \Omega cm$ for other phases with less copper. The diffusion length of minority carriers (L_n) in chalcocite varied from less than 0.1 μm to 0.6μm in thin films, which compares with less than 50Å for djurleite. However, at least 80% of the photocurrent is generated in the Cu_xS layer, and the interface between the Cu_2S and the CdS is altered by a large interfacial state density (10^{13}-10^{14} cm^{-2}) as a consequence of the mismatch of lattice and expansion coefficients [86]. The conductivity is found to be of the order of $10^5 \Omega^{-1} cm^{-1}$ for stoichiometric material. The electrical conductivity of copper sulphide increases almost linearly with copper deficiency [87]. A slight increase occurs in the effective mass of holes in copper sulphide from about $1.5 m_o$ for chalcocite to about 2 m_o for diginite, as the copper deficiency increases. The electrical properties of Cu_xS, namely resistivity, hole density and Hall coefficient are quite temperature dependent [87].

Since the reduction in the free carrier density and the improvement in the Cu_xS stoichiometry towards Cu_2S combine to improve the device

efficiency, doping can be very effective. Okomoto and Kawai [88] have used indium as a dopant and they demonstrated that it plays the same role as Cu in Cu_xS. Other workers [89,90] found that Cd and Zn compensate copper vacancies and also displace copper atoms to the surface.

Pakeva and Germanova [91] summarized the electric and photoelectric properties of polycrystalline copper sulphide as follows:

i) At room temperature the samples have an extremely low dark conductivity $\delta = 10^{-2}\Omega^{-1}cm^{-1}$

ii) the shape of the photoconductivity spectra indicates that appreciable surface recombination occurs,

iii) the minority carrier diffusion lengths were found to be $L = 3.3x10^{-5}$ $L = 2.5 \times 10^{-5}$ cm for the composition Cu_2S and $Cu_{1.96}S$ respectively.

2.7 Cadmium Zinc Sulphide Solar Cells

The major problems which limit the conversion efficiency of the CdS-Cu_2S photovoltaic cell are the differences in electron affinities of about 0.2eV, and in lattice constants of about 4-5%. The lattice mismatch and electron affinity difference between Cu_2S and CdS can be improved by substituting the CdS layer with the ternary compound $Cd_yZn_{1-y}S$ [92]. The bandgaps of the CdS and ZnS are 2.4eV and 3.6eV, the lattice constants are 4.137Å and 3.814Å and the electron affinities are 4.5eV and 3.9eV respectively.

Davis and Lind [93] demonstrated that the growth of CdZnS by iodine vapour transport yields highly uniform and relatively strain free single crystals of $Cd_yZn_{1-y}S$ with hexagonal structure. Similar mixed (CdZnS) crystals have been grown from the vapour phase in this laboratory using a modification of the method described by Clark and Woods [13]. It is reported [94] that in the growth of mixed crystals, the initial growth is richer in CdS and the later growth is richer in ZnS. Also there

is a variation in colour from orange-yellow to white as the concentration of zinc gradually increases, and reaches a maximum and has been demonstrated by Rgje-Bhosale and Pawar [95]. The orientation of $Cd_yZn_{1-y}S$ alloys is greatly influenced by an increase in the zinc content [96].

CdS and ZnS in the wurtzite modification have unit cells with volumes in the ratio ~ 1.26, and cation radii in the ratio $Cd^{++}/Zn^{++} \sim 1.3$. They are both n-type photoconductors and their reflectivity spectra show similar structure.

The lattice parameters of CdZnS alloys have been studied by Ballentyne and Ray [97] who found that the C-axis dimension of the alloy decreases sublinearly with the zinc content. In addition, native or intrinsic defects play a critical role in determining the electrical and luminescence properties of alloy materials [98,99]. The carrier densities initially increase with increasing Zn concentration, but decrease monotonically when the Zn concentration is high. The film mobilities, however, decrease continuously with increasing Zn concentration. The optical energy gap is also found to increase with increasing Zn concentration [100]. The variation in the energy gap as a function of composition has been reported, and it was found that the conductivity depends strongly on the growth parameters [101]. The values of resistivity are found to increase with increase in Zn content [95]. The photoconductivity also increased as the Zn content increased. The incorporation of about 15% Zinc into CdS reduced the dark conductivity by a little more than one order of magnitude, but with the next 5-10% Zn content, the dark conductivity decreased by about 7-8 orders of magnitude. With a Zn content in the range 25-60%, the dark conductivity was about $10^{-10}\Omega^{-1}cm^{-1}$, and a further decrease of about three orders of magnitude was detected when 60-100% zinc was added.

Since Palz et al [92] reported that $Cd_yZn_{1-y}S$ solar cells give a significant increase in V_{oc} compared with that from $CdS-Cu_2S$ devices,

a great deal of interest was taken in $Cd_yZn_{1-y}S$ alloys as a window material for both thin film and single crystal devices. Bragagnolo et al [102] reported a higher open circuit voltage of about 0.85V. It was claimed that, for low Zn concentration i.e. $y \leq 0.1$, the performance of the $Cd_yZn_{1-y}S$ - Cu_2S solar cell could be improved by reducing grain boundary recombination [103]. The influence of the Zn content in the $Cd_yZn_{1-y}S$ layer on the performance of $Cd_yZn_{1-y}S$-Cu_2S solar cells has been discussed by Gordillo [104]. An efficiency in excess of 10% has been obtained by Hall et al [105] in thin film devices of $Cd_yZn_{1-y}S$-Cu_2S.

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CHAPTER THREE

Theoretical Aspects of the CdS-Cu_2S Solar Cell

3.1 Introduction

In this chapter, the theoretical background required for understanding various types of heterojunction and their application as solar cells is described. In the first section, the various possible conduction mechanisms in CdS-Cu_2S and (Cd, Zn) S-Cu_2S photovoltaic cells are discussed. First the current-voltage characteristics, spectral response and other parameters affecting the junction performance are considered. Capacitance-voltage and photocapacitance methods, which are applied to identify and characterize the defect traps in the space charge region of the heterojunction, are then outlined.

3.2 Photovoltaic Mechanisms in the CdS-Cu_2S and $Cd_yZn_{1-y}S$ - Cu_2S Junctions

Since the photovoltaic effect in CdS was discovered in 1954 [1], this device has been studied extensively from both the experimental and theoretical standpoints. The way in which light affects this cell and the role of interface states began from the work of Shiozawa et al [2] at the Clevite Corporation and Professor R.H. Bube's group at Stanford University [3,4,5]. The properties of these devices depend critically on the post fabrication heat treatment [6,7]. In particular, copper diffuses into the CdS across the interface producing a cross-over effect between the current-voltage characteristics measured in the dark and in the light. This leads to photo effects associated with Cu-doped CdS [7], and compensation of the n-type CdS layer causing the space-charge region on the CdS side of the junction to widen [8]. Since the electrical properties of Cu_2S are controlled by copper

vacancies, oxidation can increase the conductivity of the material making it a degenerate semiconductor, as well as converting it to different crystallographic phases. Hence the band diagram changes significantly with carrier density changes of many orders of magnitude. However, under illumination, the compensating centres can be emptied either through direct excitation by the light, or by the trapping of holes created by band to band transitions in the CdS. This leads to large changes in the capacitance values due to the shrinkage of the space-charge region [9,10]. This shrinkage leads to an increase in tunnel conduction mechanisms [11].

The CdS-Cu_2S junction is very complex as a result of interfacing two materials with different electron affinities, bandgaps and crystal structures. Not surprisingly, many models have been put forward to explain the conduction mechanism in this device. In the Clevite model [2], the devices were essentially considered to be of the p-i-n variety. The Clevite group considered the structure of copper-doped, high resistivity CdS in great detail and indicated that photoconductivity is to be expected in the i-CdS region, resulting in the observed reduction in the cell series resistance when illuminated with light of the appropriate wavelength. In 1971 Van Aershodt et al [12] disputed the presence of an i-layer because of the sharp rise in current at high forward bias. A conduction band spike model was suggested by Gill and Bube [3], and this idea was later developed by Lindquist and Bube [5]. This spike in the conduction band was attributed to the mismatch in the electron affinity at the CdS-Cu_2S interface. This model proposed that electron tunnelling through the spike, and recombination via interface states were the dominant factors in determining the means of current transport. The thickness of the spike was considered to be controlled by the trapping of charge near the interface, and its height

was estimated to be between 13 and 60 meV. The tunnelling probability is controlled by the occupancy of deep levels in the CdS depletion region, at 0.3 eV and 1.1 eV above the valence band. Te Velde [13] proposed a model which invoked a change of the conduction band discontinuity (ΔE_c), and the CdS band bending, and the conduction band discontinuity changes from a notch to a spike due to the absorption of oxygen at the interface, where it forms electron traps. He explained the current-voltage characteristics in terms of the height of this discontinuity, and he did not consider the existence of copper in the depletion region, and hence the associated effects which depend on the wavelength of the incident illumination could not be explained. It was found that the electron current injected into the copper sulphide was small compared to the recombination current at the junction, but the transport of the photogenerated carriers across the junction into the cadmium sulphide was very efficient if the interface recombination velocity was small [14]. In the interfacial tunnelling-recombination model, Fahrenbruch and Bube [15,16], showed that the electric field at the CdS-Cu_2S junction interface affects the loss of photogenerated carriers there, due to a tunnelling-recombination pathway through interface states. Haines and Bube [17] concluded that a deep donor level with an ionization energy of 0.45 eV acts as a tunnelling-recombination site and is responsible for the increasing tunnelling currents and interfacial recombination which in turn affected the operational device parameters. Recently work done by Rezig et al [18] demonstrated that a deep centre located at 1.38 eV above the valence band is responsible for recombination effects and for the quenching behaviour. Boer [19] proposed a high field domain model and he attributed the control of photogenerated carrier transport partly to the formation of the high field domains in the CdS:Cu layer, and these strongly affected V_{oc},

but had little influence on J_{sc}. Martinuzzi et al [20,21] investigated the dark conduction mechanisms in cells fabricated on both single crystals and thin films. They proposed a multistep tunnelling mechanism as the dominant process in the transport across the junction. Moorthly et al [22] suggested that the control of the forward bias current in both dark and light is dominated by space-charge limited flow. Similarly Partain et al [23] have proposed a space-charge limited current theory to explain the CdS-Cu_2S junction behaviour. Finally, following a series of experiments at the Institute of Energy Conversion, Delaware, Rothwarf [24] put forward an interface recombination model to explain the behaviour of the CdS-Cu_2S heterojunction. This model is well accepted. It is illustrated in Figure 3.1. Transport is described in terms of electric field control of interfacial recombination. In this model, the depletion layer is divided into two parts; a photoactive layer of about 0.3 μm thickness adjacent to the interface and another significantly wider section extending as much as 3 μm into the CdS bulk. The model has taken into account most of the well documented phenomena such as:

i) the large photocapacitance

ii) the cross-over between dark and light J-V characteristics

iii) the stoichiometry of the Cu_xS which controls the carrier density and relative band bending in the two materials [25]

iv) the presence of shallow donors (arising from excess Cd or intentional dopants) and deep levels (which may be native or created by annealing),

v) the lattice mismatch between CdS and Cu_2S (4%) which leads to a large density of interface states of about $10^{13}cm^{-2}$ at the junction,

and vi) the mismatch in the electron affinity of CdS and that of the

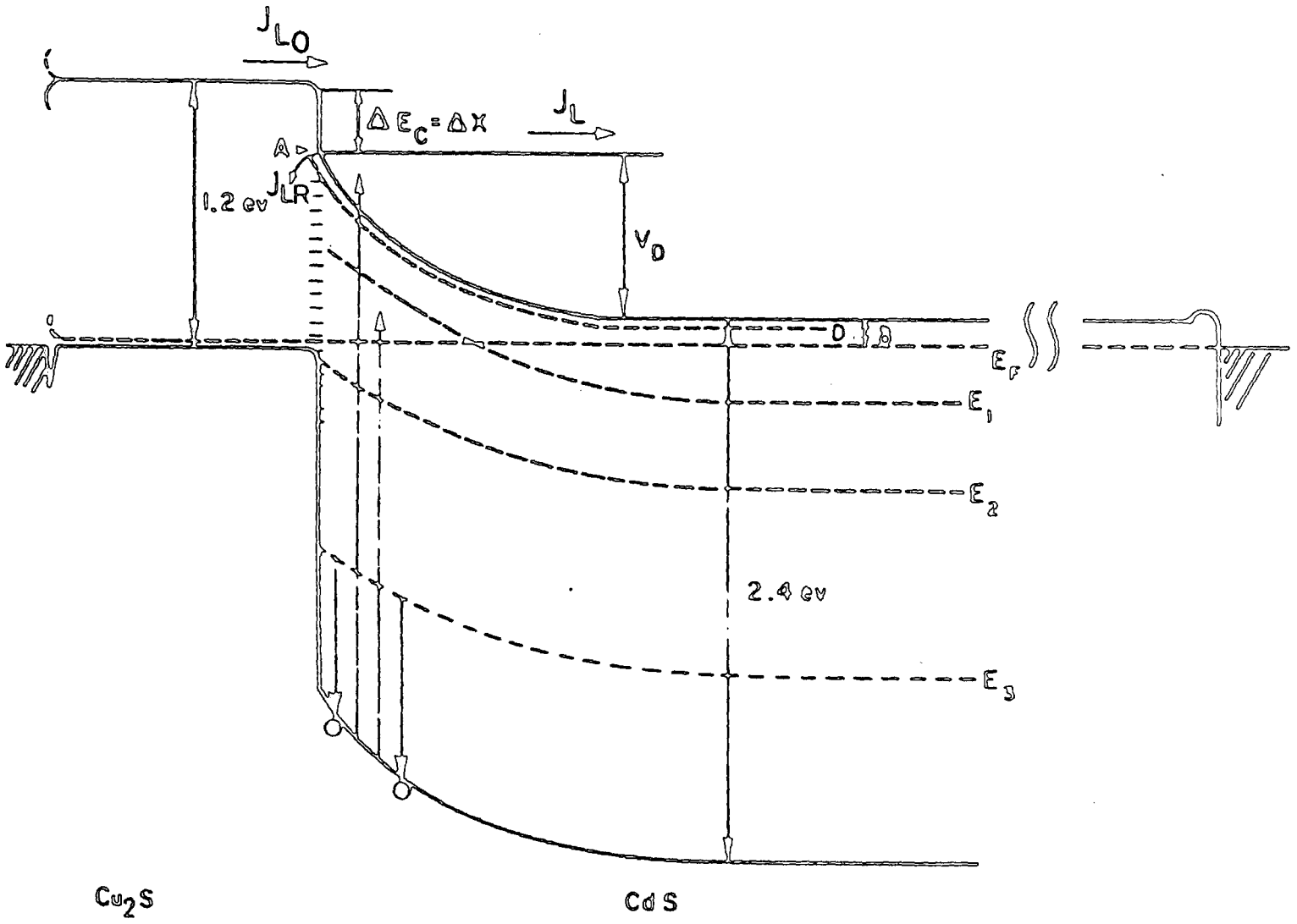


FIGURE 3.1 : Schematic band diagram proposed by Rothwarf (Ref 7).

Cu_2S. Using this model most of the observed behaviour can be explained [7]. In addition, Fabrenbruch and Bube [16] have listed in their book the generally accepted features of the CdS-Cu_2S cell. Recently a p-n junction model has been proposed which shows that the recombination that occurs is mainly due to the tunnelling of the generated electrons from the conduction band to the recombination centres in the depletion region. These electrons subsequently fall back to the valence band completing the recombination process [26]. Vandendriessche et al [27] showed theoretically and experimentally that deep levels which lie at about 0.5 eV below the conduction band play an important role in the properties of the space charge region. These levels have a spread in energy of about 0.2 eV. They are found both in the dark and under illumination, and are responsible for the frequency dependence of the capacitance. However, their role in the compensation mechanism of diffused Cu acceptors is different in the two situations.

For $Cd_yZn_{1-y}S$-Cu_2S solar cells the importance of interface recombination effects [28] and of thermally activated tunnelling [29] has been discussed in detail. Basically the junction model for this device is the same as that for the CdS-Cu_2S junction, but it is obviously modified to allow for the change in the $Cd_yZn_{1-y}S$ band parameters. Razykov and Kadirov [30] have drawn band diagrams of the $Cd_yZn_{1-y}S$-Cu_2S heterojunctions for compositions y = 0, y = 0.8, and y = 1 and they have shown that the band diagram at y = 1 is characterized by the presence of a negative conduction band edge discontinuity (ΔE_c = -0.2 eV) at the heterojunction interface. At y = 0.8, there is no discontinuity of the conduction band edge in the energy band diagram for the heterojunction. However at $y > 0.3$ a positive conduction band edge discontinuity is formed.

3.3 Basic Theory of Solar Cells

A model for an ideal abrupt interface heterojunction without interfacial defect states was proposed by Anderson [31] as an extension of Schottky diode theory. He also presented a fairly detailed model for the energy band profiles of various heterojunctions [32]. This model can adequately explain most transport processes, and only a small modification is needed to account for nonideal cases such as interface traps. The Anderson model is shown in Figures 3.2a and 3.2b, which give the band diagram of two different semiconductors before and after joining materials with energy gaps E_{g_1} and E_{g_2}, electron affinities χ_1 and χ_2, dielectric constants ε_1 and ε_2 and work functions ϕ_1 and ϕ_2. The electron affinity is the energy needed to excite an electron from the bottom of the conduction band to the vacuum level, while the work function is the energy required to excite an electron from the Fermi level to vacuum level. The quantities δ_n and δ_p indicate the separation of the Fermi level from the respective band edges in the p and n-type semiconductor materials. The difference in energy of the conduction band edges in the two materials is represented by ΔE_c, and that in the valence band edges by ΔE_v. In Figure 3.2a, the Fermi level E_{F_2} is higher than E_{F_1}. This difference cannot continue to exist if the two materials are brought together to form the junction. The discontinuity step is a natural consequence of the abrupt interface where the Fermi level, in equilibrium with no applied bias, must be the same in the two materials. Several different transport models have been proposed for the heterojunction and they are discussed in detail by many workers such as, Milnes and Feucht [33], Sharma and Purohit [34], Fonash [35] and more recently by Fonash and Rothwarf [36]. Figure 3.2b shows one of these models which has a negative discontinuity step occuring in the conduction edges at the interface and corresponds

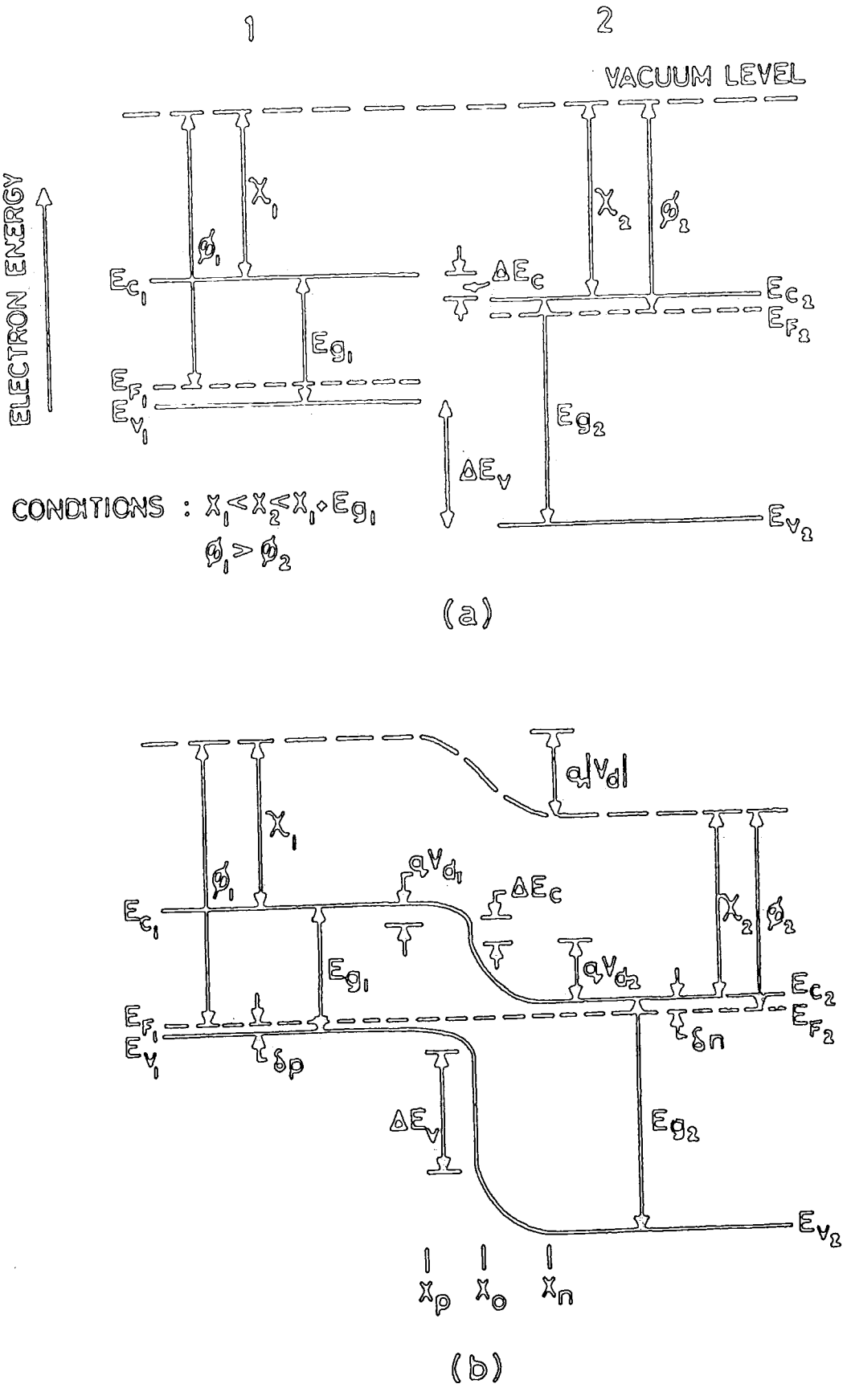


FIGURE 3.2 a: Energy band profile for two isolated semiconductors in which space chargeneutrality is assumed to be present in every region.
b: Energy band diagram for Anderson heterojunction model at equilibrium without external voltage applied.

to the case in which $\phi_1 > \phi_2$ and $\chi_1 < \chi_2 < \chi_1 + E_{g1}$.

Band bending is observed as a result of electrons moving from the n-region and leaving behind an uncompensated positive space charge of ionized donors in the layer of width X_n, while simultaneously, holes moving from the p-region leave behind an uncompensated space charge of ionized acceptor atoms in the layer of width X_p. The amount of band bending after the materials are joined is qV_D, where V_D is the built-in potential of the heterojunction. The total built-in voltage qV_D is equal to the sum of the built-in voltages on both sides $V_D = V_{d_1} + V_{d_2}$ and given by:

$$qV_D = \phi_1 - \phi_2 = (E_{g1} + \chi_1 - \delta_p) - (\chi_2 + \delta_n) = E_{g1} + \Delta\chi - \delta_p - \delta_n \qquad 3.1$$

Equation 3.1 comes from the fact that V_D, the total electrostatic potential energy developed across the junction, is established to equate the electrochemical potential (Fermi level) of semiconductor 1 to that of semiconductor 2. The conduction band energy spike, ΔE_c, is determined by the electron affinity difference

$$\Delta E_c = \chi_2 - \chi_1 = \Delta\chi \qquad 3.2$$

The valence band step is

$$\Delta E_v = (\chi_2 + E_{g2}) - (\chi_1 + E_{g1}) = \Delta E_g - \Delta\chi \qquad 3.3$$

Hence

$$\Delta E_c + \Delta E_v = \Delta E_g \qquad 3.4$$

The width of the depletion regions X_1, X_2 in the two materials, as a function of the applied voltage V is given by:

$$X_1 = X_o - X_p = \left[\frac{2\varepsilon_1 \varepsilon_2 N_D \varepsilon_o}{qN_A (\varepsilon_1 N_A + \varepsilon_2 N_D)} \right]^{\frac{1}{2}} (V_D - V)^{\frac{1}{2}} \qquad 3.5$$

$$X_2 = X_n - X_o = \left[\frac{2 \varepsilon_1 \varepsilon N_A \varepsilon_o}{qN_D (\varepsilon_1 N_A + \varepsilon_2 N_D)} \right]^{\frac{1}{2}} (V_D - V)^{\frac{1}{2}} \qquad 3.6$$

The total width of the depletion region is thus:

$$\omega = (X_n - X_o) + (X_o + X_p) = \left[\frac{2\varepsilon_1 \varepsilon_2 (N_A + N_D)\varepsilon_o}{qN_A N_D (\varepsilon_1 N_A + \varepsilon_2 N_D)} \right]^{\frac{1}{2}} (V_D - V)^{\frac{1}{2}} \qquad 3.7$$

The relative voltages supported in each semiconductor are:

$$\frac{V_{d2}}{V_{d1}} = \frac{V_2}{V_1} = \frac{V_{d2} - V_2}{V_{d1} - V_1}$$

where V_{d1} and V_{d2} are the voltage drops across the space charge region on either side of the junction and V_1 and V_2 are the voltage drops across the semiconductor.

$$= \frac{\varepsilon_1 \omega_{d1}}{\varepsilon_2 \omega_{d2}} = \frac{\varepsilon_1 N_{A1}}{\varepsilon_2 N_{D2}} \qquad 3.8$$

The capacitance-voltage relationship is:

$$C(v) = \left[\frac{qN_A N_D \varepsilon_1 \varepsilon_2 \varepsilon_0}{2(\varepsilon_1 N_A + \varepsilon_2 N_D)} \right]^{\frac{1}{2}} \left(\frac{1}{V_D - V} \right)^{\frac{1}{2}} \qquad 3.9$$

where it is assumed that the N_A acceptors and N_D donors in the uncompensated n-type and p-type regions, are ionized : $N_A = P$ and $N_D = N$. However, in principle, equation 3.9 allows a determination of V_D from a capacitance-voltage plot (C^{-2} vs. V). Therefore using equation 3.1, a value of $\Delta\chi$ can be deduced if the bandgap energy E_{g_1} and other parameters (needed to determine the Fermi level position with respect to the band edges) are known. Then from equation 3.2, ΔE_c can be calculated, while equation 3.4 yields ΔE_v if ΔE_g is known.

In Figure 3.2a and b, the condition $E_{g_2} > E_{g_1}$ should be satisfied to maximize the bandgap window, so that in most cases the transport of one of the carrier types across the junction dominates. In the case shown, hole transport across the interface is negligible compared with the electron current because of the large barrier for holes. In addition the photogeneration in the wide band gap material is usually neglected. With this assumption, Anderson derived an expression for the J-V relationship and it is very similar to that for a homojunction:

$$J = q \times N_d \left\{ \frac{D_n}{\tau_n} \right\}^{\frac{1}{2}} \exp\left[\frac{q\left(\Delta E_c + V_D\right)}{kT} \right] \left[\exp\left(\frac{qV}{kT}\right) - 1 \right] \qquad 3.10$$

where V is the applied voltage, k Boltzmann's constant, T the absolute temperature, D_n and τ_n are the electron diffusion coefficient and lifetime in the p-region and χ is the transmission coefficient which represents the fraction of the carriers with sufficient energy to cross the barrier.

The Anderson model is very helpful in assessing the merits of using a particular materials system in a heterojunction configuration, and is somewhat successful in predicting the structure of the bands at the junction. However, in most cases the measured J-V characteristics

are much different, both in quality and magnitude from those predicted. The values of ΔE_c and ΔE_v as-measured by capacitance and other techniques are not always as predicted by published χ values. For these and other reasons the Anderson model has been modified.

Experimentally, J-V characteristics can be described by the equation [16] :

$$J = J_{oo} \exp\left\{\frac{-\Delta E}{kT}\right\}\left[\exp\left(\frac{qV}{AkT}\right) - 1\right] \qquad 3.11$$

where J_{oo} and A may be slowly varying functions of T, and ΔE is a measured activation energy for the zero bias exptrapolation of $\ln J$ versus V curves. This may also be written in another general form:

$$J = J'_{oo}\left[\exp\left\{\frac{-q(\phi_b - V)}{AkT}\right\} - 1\right] \qquad 3.12$$

where $\phi_b = V_d + \frac{\delta_n}{q}$. In these cases where the relationship between $\ln J$ and V is relatively temperature independent, many junction characteristics appear to fit the relation:

$$J = J''_{oo} \exp(\beta T) \exp(-\alpha\phi_b) \exp(\alpha V) \qquad 3.13$$

where β and α are constant and are relatively temperature independent. The barrier height or activation energy to electron flow between the n and p regions of the junction (Fig 3.3) is given by the relationship:

$$\phi = E_{g_1} - \delta_1 - qV_{DP} - \Delta\chi \qquad 3.14$$

where $\Delta\chi$ is the difference in the electron affinities of CdS and Cu_2S,

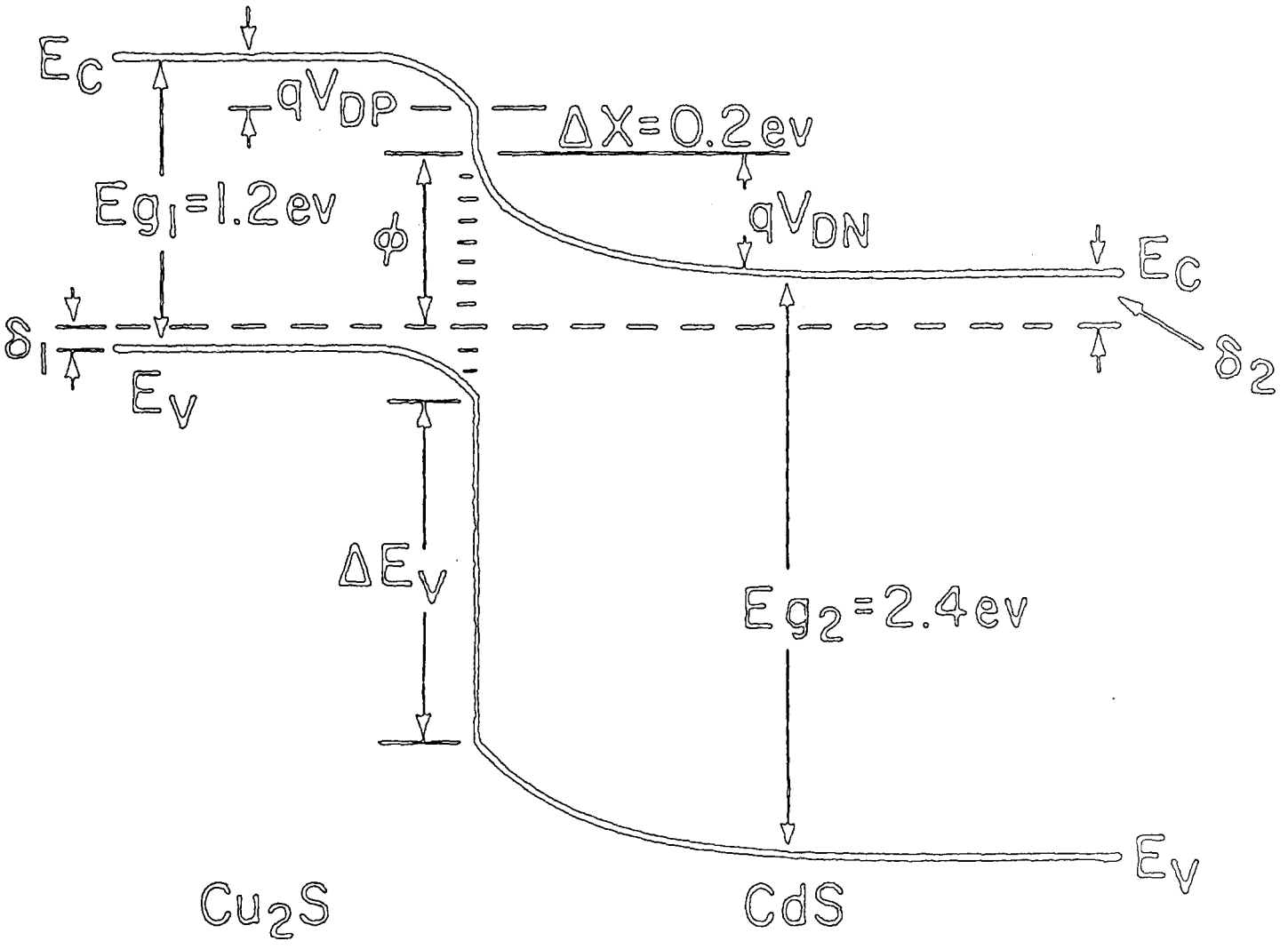


FIGURE 3.3 : Energy band diagram of CdS-Cu_2S heterojunction (Ref 7)

V_{DP} is the diffusion voltage in Cu_2S which is related to the diffusion voltage in CdS by:

$$V_{DP} = V_D \frac{N_D}{N_A + N_D}$$

where N_D and N_A are the uncompensated donor and acceptor densities in CdS and Cu_2S.

At this point it should be emphasised that the Anderson model is the idealized situation where two semiconductors form an abrupt heterojunction free from interface states, interface dipoles, cross diffusion and intermediate layers. However, in practice semiconductor heterojunction structures have band diagrams that deviate from the Anderson model [36,37]. The presence of lattice mismatch, cross diffusion and deviation from stoichiometry give rise to localized band gap states at the interface. However, not all the interface states need to be electrically active and many are compensated. Therefore only a small fraction remains active to account for the observed electrical phenomena [38]. These electrically active states act either as recombination centres causing a deterioration in the heterojunction current-voltage characteristics, or as charge traps, in which case a modified band profile results. An interface centre which acts as a charge trap is considered a donor if it can become neutral or positive by donating an electron to the conduction band. On the other hand, an acceptor interface trap can become neutral or negative by accepting an electron from the valence band. When ionised, the interface states below the Fermi level, contain negative charge, while those above Fermi level have been assumed to be acceptors. In fact, the electrical properties of interface states are characterised by their density, their position in the band gap and their capture cross-section. A minimum

interface state density is realized when the semiconductor or pair of materials comprising the heterojunction have the same crystal structure and similar lattice parameters. The importance of misfit dislocations on the behaviour of heterojunctions was first pointed out by Oldham and Milnes [39]. The difference in lattice constants of the separate materials of the heterojunction produces a periodic array of misfit dislocations with their associated dangling bonds. These edge dislocations ideally form a regular net at the interface.

Electric dipole effects which arise, for example, from interface or dislocation states being dipolar and distributed in space on either side of the junction were postulated by Van Ruyven [40]. He [41] assumed that the existence of a large number of surface states on the surface of the semiconductor is equivalent to a metallic layer which pins the Fermi level. Such dipoles could arise from charges on opposite sides of a thin insulating layer at the interface, or from a spatial distribution of oppositely charged defects on either side of the junction in the bulk of the semiconductor [16].

There may be an intermediate layer formed either deliberately or inadvertently when a heterojunction is fabricated. In such a layer, the material properties grade from those of material 1 to those of material 2 (see Fig 3.2). Grading spreads out the region where the effective forces F_e and F_h act and, consequently where ΔE_c and ΔE_v are developed [36].

Native layers frequently occur in non-ideal semiconductor devices in which case they strongly affect the characteristics [42].

3.4 Solar Cell Equivalent Circuit

The operation of a solar cell can be modelled by a current source and a diode in parallel (Fig. 3.4). By connecting a load across the

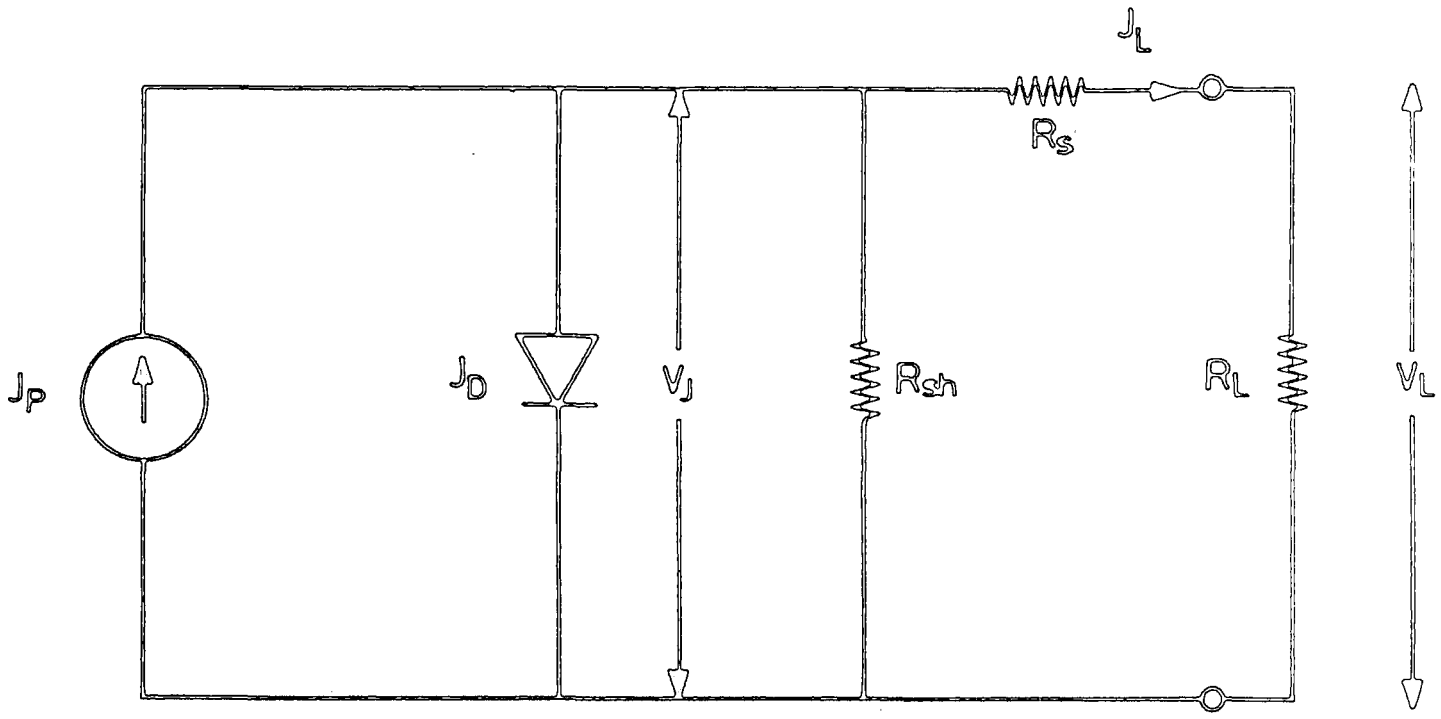


FIGURE 3.4 : Equivalent circuit of solar cell.

terminals of a solar cell, a current J_L can flow through the load and develop a voltage across it. As well as depending on the nature of the load, the values of V_L and J_L will be related to the photogenerated current J_P and the properties of the diode. These relationships are incorporated in Figure 3.4 where imperfections in the diode that lead to current leakage are represented by a shunt resistance R_{sh} and parasitic series resistance effects are represented by R_s.

When the junction is illuminated, the light generated current is normally assumed to be added linearly to the dark diode current, so that the characteristic shifts downwards, and intersections of the curve with the current and voltage axes are called the short circuit current (J_{sc}) and open circuit voltage (V_{oc}) respectively. The current through a photovoltaic cell generally can be described by the following equation which is a super-position of the dark and light generated currents [43]:

$$J - \frac{V - JR_s}{R_{sh}} = \sum_i J_{oi} \left[\exp \left\{ \frac{q}{A_i kT} \left(V - R_s J \right) \right\} - 1 \right] - J_L \qquad 3.15$$

where A_i is the diode factor which usually varies between 1 and 2 and where J_{oi} represents the reverse saturation current. If the series and shunt resistance effects are negligible, then J_L is equal to the short circuit current. This is the current that flows through the junction under illumination and zero applied bias. Because of the various contributions to the diode current which may arise, a summation of all these is necessary. These include, the ideal diffusion or emission currents, recombination generation currents which are characteristic of the depletion or space charge region on either side of the junction, tunnelling from band states to localized defect states in the gap across the interface, recombination via interface states at the

junction and band to band tunnelling.

For homojunctions $A_i = 1$, and when the current mechanism is ideal diffusion, the reverse saturation current is given by:

$$J_o = \frac{qD_p P_{no}}{L_p} + \frac{qD_n n_{po}}{L_n} \qquad 3.16$$

where P_{no} is the thermal equilibrium density of holes on the n-side of the junction, n_{po} is the corresponding density of electrons on the p-side, D_p and D_n respectively are the hole and electron diffusion constants, and L_p and L_n are the minority carrier diffusion lengths on the n and p-sides of the junction respectively. The minority carrier diffusion constants D_p and D_n are given by:

$$D_p = \frac{kT}{q}\mu_p \quad \text{and} \quad D_n = \frac{kT}{q}\mu_n \qquad 3.17$$

where μ_n and μ_p are electron and hole mobilities, and

$$P_{no} = \frac{n_i^2}{N_d}, \qquad n_{po} = \frac{n_i^2}{N_a} \qquad 3.18$$

N_d and N_a are the n and p-region effective impurity concentrations and n_i is the intrinsic carrier concentration. Also the diffusion lengths are related to the basic material properties by the following equations:

$$L_p = \sqrt{\tau_p D_p}, \qquad L_n = \sqrt{\tau_n D_n} \qquad 3.19$$

where τ_p and τ_n are hole and electron lifetimes as minority carriers.

In a Schottky diode the various mechanisms operative in forward bias (in the case of an n-type semiconductor for example) include

i) thermionic emission of electrons from the semiconductor over the top of the barrier into the metal;

ii) recombination in the depletion region;

iii) quantum mechanical tunnelling through the barrier; and

iv) hole (minority carrier) injection and diffusion.

If the space charge region is narrower than the diffusion length, according to thermionic-emission theory the total current density is given by [44,45] :

$$J = \overset{*}{A}\, T^2 \exp\left\{ \frac{-q\phi_b}{kT} \right\} \left[\exp\left(\frac{qV}{kT}\right) - 1 \right] \qquad 3.20$$

where $\overset{*}{A}$ is the modified Richardson constant for thermionic emmission, ϕ_b is the barrier height and the other terms have their usual meanings. In this expression, $\overset{*}{A} = 4\pi q\, m^* k^2 h^{-3} = 120 \frac{m^*}{m_o}$ Amp.cm^{-2} k^{-2}

Alternatively, if the space charge region is wider than the diffusion length, the dark current-voltage characteristics will be determined by the following equation:

$$J = qN_c\, \mu_e F_{max} \exp\left(- \frac{q\phi_b}{kT} \right) \left[\exp\left(\frac{qV}{kT}\right) - 1 \right] \qquad 3.21$$

where N_c is the effective density of states in the conduction band, μ_e the electron mobility, F_{max} the maximum electric field at the junction and where

$$N_c = 2 \left[\frac{2\pi m^* kT}{h^2} \right]^{3/2}$$

In the third situation, where the space charge is comparable in thickness to diffusion length, the equation for the current flow becomes

$$J = \frac{qN_c\nu_R}{1+\nu_{R/\nu_D}} \exp\left(-\frac{q\phi_b}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \qquad 3.22$$

Here $\nu_R = \frac{A^* T^2}{qN_c}$ is the effective recombination velocity and ν_D is an effective diffusion velocity.

For an MIS photovoltaic cell, the current density is similar to that for a Schottky barrier with an additional tunnelling term and can be written as [16]:

$$J = A^* T^2 \exp\left(-\phi_T^{\frac{1}{2}} d\right) \exp\left(-\frac{q\phi_b}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \qquad 3.23$$

$\exp\left(-\phi_T^{\frac{1}{2}} d\right)$ is the tunnelling probability, $q\phi_T$ is the average barrier height presented by the insulating layer and d is the thickness of the insulator.

3.5 Light Generated Current

Since the incident light of the cell is primarily absorbed by the Cu_2S layer, the generation of current takes place almost exclusively in the Cu_2S. The current generated can be determined as in Figure 3.1 from the relation:

$$J_{Lo} = J_{LR} + J_L \qquad 3.24$$

where J_{Lo} is the light generated current which crosses the junction, J_{LR} is the current which returns to the Cu_2S via interface state path and, J_L is the current which flows through the CdS to the electrodes.

The magnitude of the light generated current depends on many parameters of the Cu_2S layer [46] such as, its thickness, the electron diffusion length, the surface recombination velocity at the front surface, the drift field in the Cu_2S, the grain size of the Cu_2S, the absorption coefficient as a function of wavelength, incident light intensity and wavelength, the topology of the Cu_2S surface and the refractive index of the covering material.

At the junction

$$J_{LR} = qS_1n_1 \quad \text{and} \quad J_L = qn_1\mu_2F_2 \tag{3.25}$$

where n_1 is the density of electrons at the junction, μ_2 is the mobility of electrons in the CdS and F_2 is the field at the interface.

The relation between the J_L and J_{Lo} can be written:

$$J_L = J_{Lo} \quad \frac{\mu_2F_2}{S_I + \mu_2F_2} \tag{3.26}$$

where F_2 is the field in the CdS at the junction in the light, S_I is the interfacial recombination velocity, and μ_2 is the electron mobility. The factor $\frac{\mu_2F_2}{S_I + \mu_2 F_2}$ is the interfacial collection factor (ICF). When $S_I = \mu_2F_2$, the ICF = 0.5. The junction field F_2 is given by the following equations [5] at the zero bias and the short circuit conditions respectively:

$$F_2(o) = \frac{2V_D}{\omega} = \frac{2N_D^*\omega}{\varepsilon\varepsilon_0} = \left\{\frac{2V_DqN_D^*}{\varepsilon\varepsilon_0}\right\}^{\frac{1}{2}} \tag{3.27}$$

$$F_2(v) = \left[\frac{2qN_D^*\,(V_D - V)}{\varepsilon\varepsilon_0}\right]^{\frac{1}{2}} \tag{3.28}$$

where V_D is the diffusion voltage, ω is the width of the space charge region, ε is the dielectric constant of CdS and ε_0 is the permeability of free space. Thus the field is directly related to the total positive charge in the CdS space charge region and depends on the bias voltage.

3.6 Junction Capacitance

Observing the depletion region in a p-n junction and measuring its width can be a very simple matter. In the depletion approximation, a change in applied voltage will cause a change in stored charge at the edges of the regions. The depletion region capacitance, C, is given by:

$$C = \frac{\varepsilon A}{w} \qquad 3.29$$

where ω is the width of the depletion region and A is the area of the junction capacitor.

Under reverse bias, the depletion region capacitance dominates the total diode capacitance. Hence, a measure of C as a function of reverse bias for a diode or solar cell and a plot of $\frac{1}{C^2}$ versus V will allow N, the donor concentration to be found.

Hall and Singh [47] made a comprehensive study of the capacitance-voltage characteristic of the space charge distribution in CdS-Cu_2 S cells. They assumed that the space charge is wholly in the CdS and is comprised of three regions: a surface of high space charge density, a compensated layer and a conducting bulk. The change in the width of the space charge as a function of the reverse applied voltage is determined using the assumption that the applied voltage does not affect the space-charge density in any part of space charge region.

Donelly and Milnes [48] showed, however, that in the limit where the interface charge is independent of applied voltage, the capacitance

voltage relation takes the form

$$C^{-2} = \left[\frac{2\,(\varepsilon_1 N_{A_1} + \varepsilon_2 N_{D_2})}{q\,\varepsilon_0 \varepsilon_1 \varepsilon_2 N_{A_1} N_{D_1}} \right] \left[V_{di} - V \right] \qquad 3.30$$

Here V_{di}, the diffusion voltage is modified by the charge stored at the interface, Q_{ss}, and the dipole voltage, ϕ_d, and is given by:

$$V_{di} = V_d + \frac{Q_{ss}}{2q\,(\varepsilon_1 N_{A_1} + \varepsilon_2 N_{D_2})} + \phi_d \qquad 3.31$$

The capacitance of the CdS-Cu_2S heterojunction has been investigated by Rothwarf [7] for various space charge profiles. A more recent study of the effect of interface states on the C-V measurements has been made by Nagami[49].

3.7 Spectral Response

The spectral response (SR) is defined as the short circuit current collected from a given number of photons per second of energy $h\nu$ incident on a solar cell.

Measurements of the spectral response can provide detailed information about the operative mechanisms in a particular solar cell. The quantity SR is also known as the collection efficiency at each wave length, or as the quantum efficiency. Thus the photocurrent collected at each wavelength relative to the number of photons of that wavelength incident on the surface determines the spectral response of the device.

Monochromatic light causes electron-hole pairs to be generated in the semiconductor with a spatial distribution, given by [50]:

$$G(x) = (1 - R)\ \alpha F \exp - \alpha x \qquad 3.32$$

where the carrier generation rate (G) depends on the distance travelled by the photon (x) in the semiconductor before being absorbed, and where R is the fraction reflected, F is the flux density of photons, and α is the absorption coefficient.

For short wavelength (U.V.), α is large, and light is obsorbed within a short distance of the surface of the semiconductor. If the quantum collection efficiency γ_Q is defined as the number of electrons flowing in the external short-circuiting lead per incident photon in the monochromatic light, it will be very low for such U.V. light. At intermediate wavelengths, α is smaller in value and a large proportion of the carriers are generated in regions where the collection probability is high. γ_Q consequently increases in this case. At long wavelengths, light is absorbed very weakly and only a small proportion of it is absorbed in the active region of the cell. γ_Q therefore decreases dropping to zero once the photons have insufficient energy to create electron-hole pairs.

Certainly the qualitative behavioural trends of measured devices having different values of carrier lifetime, diffusion length, electric field, etc are predicted very well by the analytical expressions, and it is common practice to compare measured spectral responses of devices with those predicted by theory.

Spectral response measurements for the CdS-Cu_2S cell have been extensively applied to investigate several features of the phase of copper sulphide [51,52,53].

3.8 Solar Cell Operational Parameters

3.8.1 Solar Cell Efficiency

The efficiency of a solar cell is defined as the ratio of its maximum power (P_{max}) to the incident light power (P_{inp}) where both are measured in $W.cm^{-2}$

$$\gamma = \frac{P_{max}}{P_{inp}} \qquad 3.33$$

The maximum power point can be found from current-voltage (J-V) characteristics in the dark and under illumination as shown in Fig 3.5. Thus, the maximum power output of the photovoltaic cell can be represented by the area of the small rectangle, and it is obtained when the product JxV is maximum. The ratio of the maximum power ($J_{max}.V_{max}$) to the product of V_{oc} and J_{sc} is called the fill factor (FF). It represents the ratio of the area of the largest rectangle that can be inscribed in the fourth quadrant of the J-V curve obtained under illumination, to the area of the rectangle bounded by $J = J_{sc}$, $V = V_{oc}$ as shown in Fig 3.5. Thus

$$FF = \frac{J_{max} \times V_{max}}{J_{sc} \times V_{oc}} \qquad 3.34$$

These three parameters namely V_{oc}, J_{sc} and FF essentially define the solar cell performance. Then equation 3.33 can be written:

$$\gamma = \frac{(J_{sc} V_{oc})\ (FF)}{P_{inp}} \qquad 3.35$$

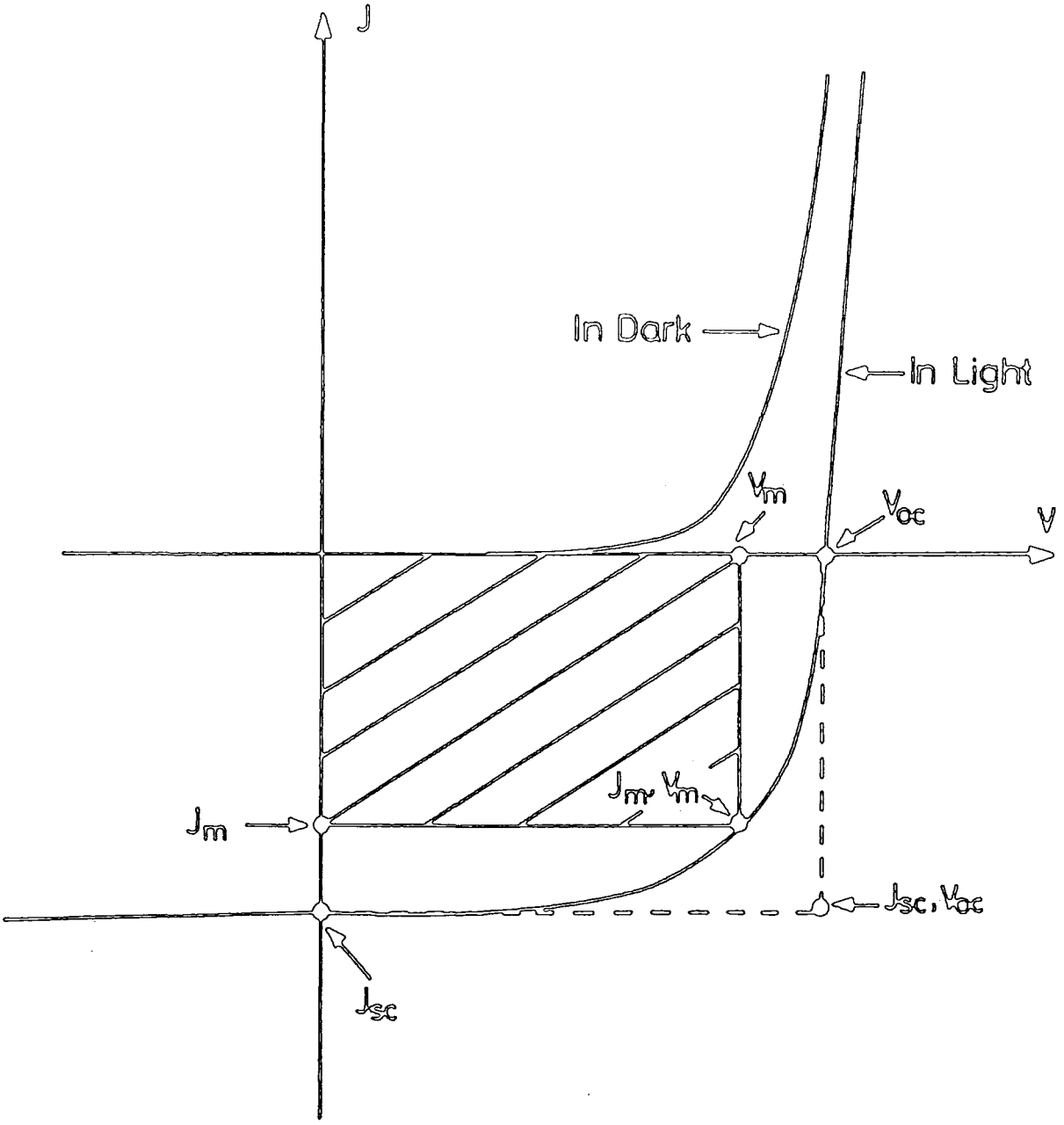


FIGURE 3.5 : The J-V characteristics of a solar cell measured in the dark and in the light.
J_{sc} is the short circuit current.
V_{oc} is the open circuit voltage.
$J_m.V_m = P_m$, is the maximum power point.

There are two primary sources of fundamental inefficiency in the operation of a solar cell. The first concerns the mismatch of the semiconductor energy gap with the solar spectrum. Low energy photons, with $h\nu < E_g$, are not absorbed in the semiconductor where electron-hole pairs are created. Photons with energy greater than E_g create electron-hole pairs, but the excess energy $h\nu - E_g$ is lost in heating up the semiconductor. The second basic inefficiency mechanism relates to recombination of electron-hole pairs before the minority carriers cross the junction. Recently Rothwarf [55] summarized the important solar cell parameters, the factors leading to enhanced performance and the critical processing steps.

3.8.2 Solar Radiation

The basis for photovoltaic energy conversion is the absorption of photons by a semiconductor. Only photons of the appropriate energy can be absorbed by the material. It is, therefore, important to be aware of the spectral distribution of sunlight. In particular this is affected by the atmosphere, altitude and geographical location. The intensity of solar radiation in free space at the average distance of earth from the sun is used as a reference and is defined as the solar constant with value of 1.353 $kW.m^{-2}$. Since the absorption by the atmosphere is different for different wavelengths, the solar spectrum on earth is different from that emitted by the sun. The absorption in the ultraviolet is due to electronic transitions in molecular and atomic oxygen, nitrogen and ozone in the upper atmospheric layers, while water vapour and carbon dioxide molecules are responsible for the absorption bands in the infra-red.

The secant of the angle between the sun and the zenith is called the air mass (AM). It is the ratio of the actual pathlength of the

solar radiation through the atmosphere to its minimum value. In Fig 3.6 the upper curve represents the solar spectrum outside the earth's atmosphere and this is air mass zero (AM0) condition. This spectrum is the relevant one for satellite and space vehicle applications. When the sun is at its zenith i.e. the sun is directly overhead, the air mass is one (AM1) and the incident power of about 1000 $W.m^{-2}$. On the other hand, when the sun is 60^{o} above the horizon, the radiation is AM2 and has an incident power of about 690 $W.m^{-2}$. At the laboratory level, it is usual to simulate terrestrial sunlight by the simple expedient of filtering the light from a 3200 ^{o}K colour temperature tungsten-halogen lamp through water, and adjusting the intensity until a reference solar cell detector indicates a power density of 1000 $W.m^{-2}$.

3.8.3 Short Circuit Current

It is not surprising that as the band gap decreases, the short circuit current density increases. More photons have the energy required to create electron-hole pairs as the band gap becomes smaller.

In the CdS-Cu_2S heterojunction, the minority carriers photogenerated in the Cu_2S diffuse to the junction, where some recombination can be expected to occur via the large density of interface states ($\sim 10^{14}$ dangling bonds per cm^2). The photocurrent limitations in these devices have been attributed to different mechanisms. Boer [19,56] suggested that high field domains can form near the CdS-Cu_2S interface, leading to field quenching conditions similar to those observed in photoconducting cadmium sulphide. The field quenching causes a transition from high to low carrier lifetime states and thus leads to a diode saturation current. This is the short circuit photocurrent and it is of lower value than that which would otherwise be supported by minority carrier extraction from the Cu_2S layer. In

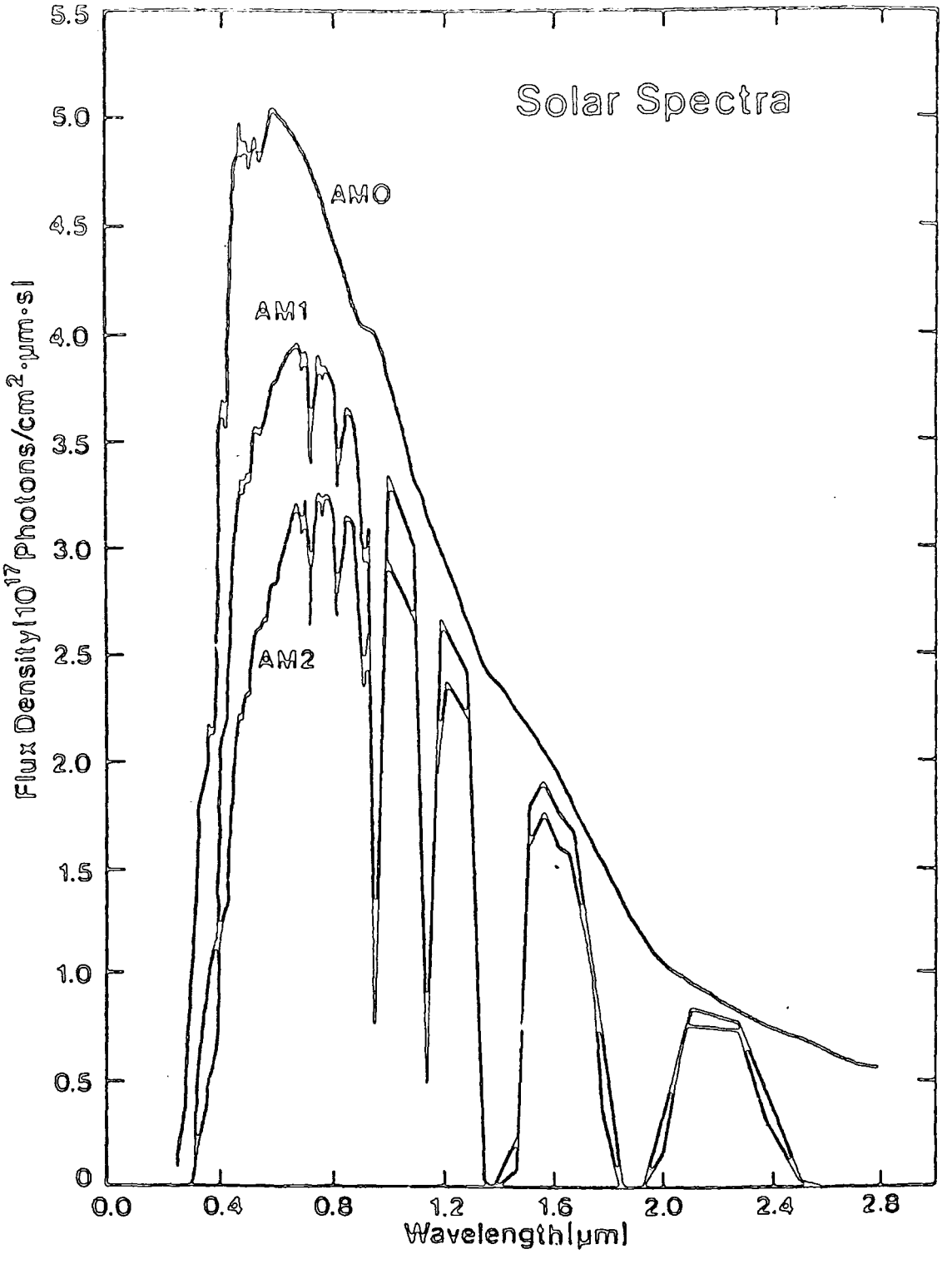


FIGURE 3.6 : Spectral distribution of sunlight. Shown are the case of AM0, AM1 and AM2 radiation (Ref 54).

another model [57], photocurrent limitations have been attributed to more conventional mechanisms, such as photon reflection losses and photocarrier recombination at the interface, at the grain boundaries, at the surface and in the bulk regions of the cell.

3.8.4 Open Circuit Voltage

The open circuit voltage (V_{oc}) is determined by the properties of the semiconductor by virtue of its dependence on J_o. The V_{oc} is given by:

$$V_{oc} = \frac{kT}{q} \ln \left(\frac{J_L}{J_o} + 1 \right) \qquad 3.36$$

where J_L is the light generated current and J_o is the diode saturation current. For maximum V_{oc}, the J_o needs to be as small as possible. The value of J_o depends on the band gap of the semiconductor, and on the densities of states in the conduction and valence bands and can be expressed as follows:

$$J_o = AN_cN_v \exp \left(- \frac{E_g}{kT} \right) \qquad 3.37$$

where A is a constant of proportionality. N_c and N_v are densities of states in the conduction and valence bands respectively.

The value of V_{oc} is limited by factors such as interfacial recombination velocity, crystallite size, etc. Rothwarf [58] attributed a loss in V_{oc} (ΔV_{oc}) of as much as 0.06 V to the effective junction area and this was given by

$$\Delta V_{oc} = kT \ln \frac{A_I}{A_J} \qquad 3.38$$

where A_I and A_J are the planar and actual junction area respectively. It has been shown that V_{oc} as high as 0.85 V can be achieved for the $Cd_yZn_{1-y}S$-Cu_2S photovoltaic cell [59] and this can be attributed to the reduction in the difference in electron affinities. The relationship between the J_{sc}, V_{oc}, J_{max} and V_{max} can be written in one equation [60] :

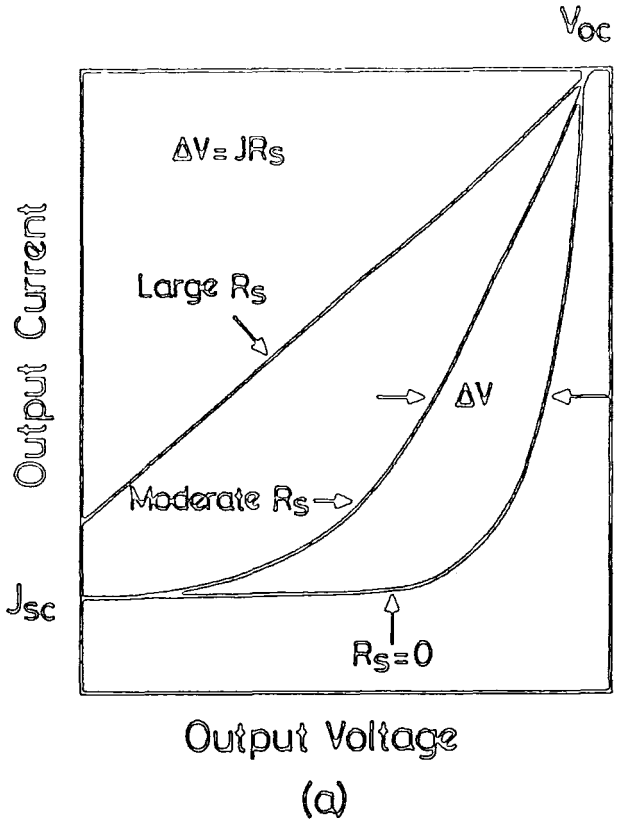
$$\frac{J_{max}}{J_{sc}} = 1 - \exp\left[\frac{(V_{max} - V_{oc})q}{kT}\right] \qquad 3.39$$

In CdS-Cu_2S cells, V_{oc} values are limited by the electron affinity difference between the two semiconductors.

3.8.5 The Fill Factor

It is known that the efficiency of a solar cell is strongly affected by the value of the fill factor. The effect of series and shunt resistance on J-V characteristics is shown in Fig 3.7. The ideal FF can be attained as R_{Sh} and R_s reach their maximum and minimum values respectively.

There are several physical mechanisms responsible for the device resistance. The major contributions come from the series resistance (R_s) and the resistance of the metallic contacts and interconnections to the semiconductors. In addition, there is the shunt resistance (R_{sh}) which is caused by leakage across the p-n junction around the edge of the cell and in nonperipheral regions in the presence of crystal defects and precipitates of foreign impurities. Figure 3.8 shows that very high values of R_s and very low values of R_{sh} can also reduce J_{sc} and V_{oc} respectively. The magnitude of the influence of R_s and R_{sh} on the fill factor can be found by comparing their values with



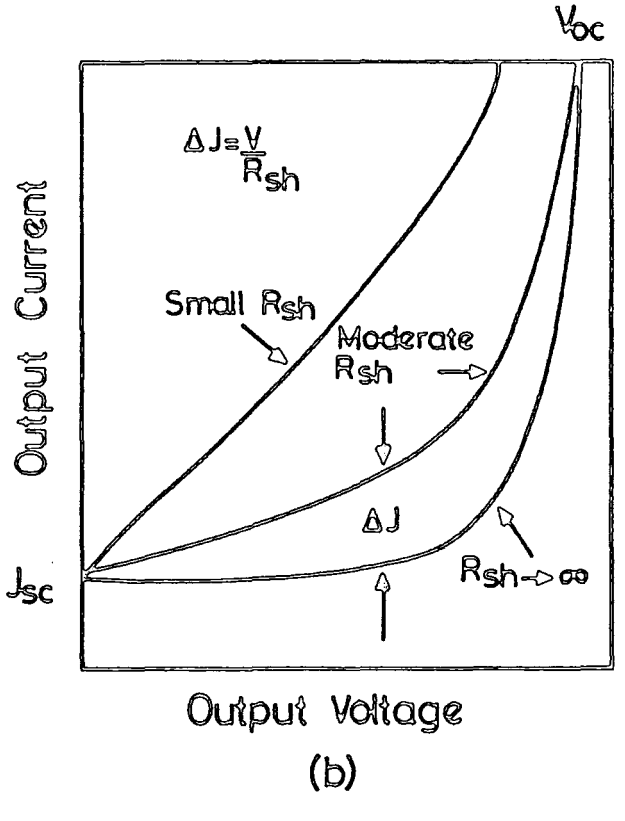


FIGURE 3.7 : Effect of parasitic resistances on the output characteristics of cells (Ref 61).
a : Effect of series resistance, R_s
b : Effect of shunt resistance, R_{sh}

the characteristic resistance of solar cell defined as

$$R_{ch} = \frac{V_{oc}}{J_{sc}} \qquad 3.40$$

Defining a normalized resistance, r_s as $\frac{R_s}{R_{ch}}$, an approximate expression for the real fill factor in the presence of series resistance is:

$$FF = FF_o (1 - r_s) \qquad 3.41$$

where FF_o represents the ideal fill factor in the absence of parasitic resistance. In the same way the effect of shunt resistance on the actual fill factor can be written as:

$$FF = FF_o (1 - r_{sh}) \qquad 3.42$$

Generally, Rothwarf [7] has summarized the parameters affecting the fill factor in the CdS-Cu_2S solar cell.

3.9 Defect and Impurity Centres

When native defects or impurity atoms are introduced into a perfect crystal, the periodicity of the crystal potential is affected and new energy levels are created. These levels normally lie within the forbidden gap of the semiconductor and they have a strong influence on crystal properties. Defect states in semiconductors have many labels such as electron or hole traps, recombination centres, optical absorption centres, donor or acceptor centres, etc and the one chosen often depends on the experimental technqiue used to observe them.

These names do not correspond to different physical species but reflect the behaviour of the energy level. In order to provide a complete description for an energy level, several parameters have to be determined such as ionisation energy, the density of levels, their thermal and optical capture and emission constants for electrons and holes. The main parameter which establishes these defects as either shallow or deep levels is the ionisation energy. It is known that, if the impurity levels lie close to one of the energy band edges, such centres are called shallow impurity levels, while the deep levels are localised further into the band gap.

3.9.1 Shallow Levels

The traps are considered as shallow levels if the ionisation energy is comparable with 0.026 eV ($\sim$kT). These centres can be classified as either donor or acceptor. Since these levels are normally ionised at room temperature, they play the dominant role in the determination of the semiconductor conductivity (n or p). The distinction between deep and shallow levels is somewhat arbitrary, often corresponding to the experimental method used for analysis.

3.9.2 Deep Levels

Deep levels have binding energies which are much larger than those of shallow ones. One of the characteristics of deep energy levels is their ability to control carrier lifetime [62,63]. The performance of many semiconductor devices is determined by the lifetime of the excess free charge carriers and a better insight in the electronic properties of deep energy levels is therefore important. Deep levels may be introduced into semiconductors in several different ways, such as by the incorporation of transition metal impurities

like copper and iron, or by the formation of vacancies and vacancy complexes.

For solar cell applications, deep level impurities will influence current collection in the following three ways:

i) by reducing the minority carrier lifetime [63]

ii) by recombination losses in the depletion region [63,64]; and

iii) by modification of the junction electric field under illumination [65]. Generally all these effects will apply simultaneously with the consequence that deep levels reduce the device efficiency. If the probability for an electron being thermally freed from a centre to the conduction band is greater than that of recombining with a hole, the centre is considered to be an electron trap. Conversely, if the recombination probability is greater than that of the electron being thermally freed, the levels are recombination centres. Similar definitions apply for hole traps. The ability to capture a free carrier is determined by the capture cross section of a centre and the values for both types of carrier indicate the electron or hole trapping nature of the centre.

It is worth noting that the opposite process of capture is ionization. It can be defined as the probability of a centre emitting an electron or hole, and it can be achieved by thermal or optical processes.

3.9.3 Photocapacitance For The Detection Of Defect Levels

The capacitance of a cell is determined by the distribution of the charge density ρ in the space charge region of the barrier. Charge density depends however, on the occupancy of the deep centres. Photocapacitance is the change in the charge state and the subsequent effect of this change on the capacitance of the depletion region brought

about by exposure to light. The steady state photocapacitance entails the recording of the variation in the junction capacitance with changing wavelength. Photocapacitance has been used for many years for the investigation of the presence of carrier trapping centres in semiconductors [66]. In particular, it has been used in Si [67], GaP [68], GaAs [69,70], CdTe [71], CdSe [72,73], ZnSe [74,75,76], CdS [77], $Cd_yZn_{1-y}Se$ [78], and many other materials. Grimmeiss and Overn [79] have described the fundamental principles of the method and their application to II-VI compounds is given by Grimmeiss [80].

The measurement of photocapacitance not only provides information on deep levels, whether radiative or not, but also permits high sensitivity with quantitative information on trap concentration as well as energy level structure. The threshold and the sign of the capacitance change identify the process with either emptying or filling of the impurity level.

Although this method has been successfully applied to the study of many shallow levels, it is not generally suitable for the investigation of deep centres, primarily because of the large associated time constants of such centres. Nevertheless this problem can be overcome by scanning the wavelength with a very slow speed and by allowing sufficient time for the steady state condition to be established. Also the presence of several energy levels in the band gap of a semiconductor can complicate the analysis.

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CHAPTER FOUR

Experimental Technique

4.1 Introduction

In this chapter the experimental techniques and the equipment used in the present work is described in detail. This includes a brief summary of crystal growth, the fundamentals of Scanning Electron Microscopy (SEM) and Reflection High Energy Electron Diffraction (RHEED) and the equipment required for the measurement of current-voltage characteristics, spectral response and capacitance.

4.2 Crystal Growth

The technique employed for growth of single crystal CdS and $Cd_yZn_{1-y}S$ was developed by Clark and Woods [1,2]. It is based on the sublimation method designed by Piper and Polich [3], and utilises a self-sealing technique to ensure that congruent evaporation is achieved (some of the important features of CdS crystal growth have been discussed in Chapter Two). For CdS, the charge was initially prepared by passing a continuous stream of argon over heated polycrystalline CdS, this gave platelets of CdS which were used for the growth of the large single crystals. The ZnS used as charge material for the growth of $Cd_yZn_{1-y}S$ was supplied by Cerac and was used in the as-received form. CdS platelets (for CdS crystal growth), or CdS platelets mixed with polycrystalline ZnS (for $Cd_yZn_{1-y}S$ crystal growth), were loaded in the growth ampoules which were evacuated and sealed using an oxy-gas flame.

The experimental arrangement used for growth with this system is shown in Fig 4.1. The charge was maintained at $1150^{o}C$ in the growth ampoule, which was connected via a narrow orifice to a long tail tube containing a reservoir of cadmium or sulphur. The temperature of this

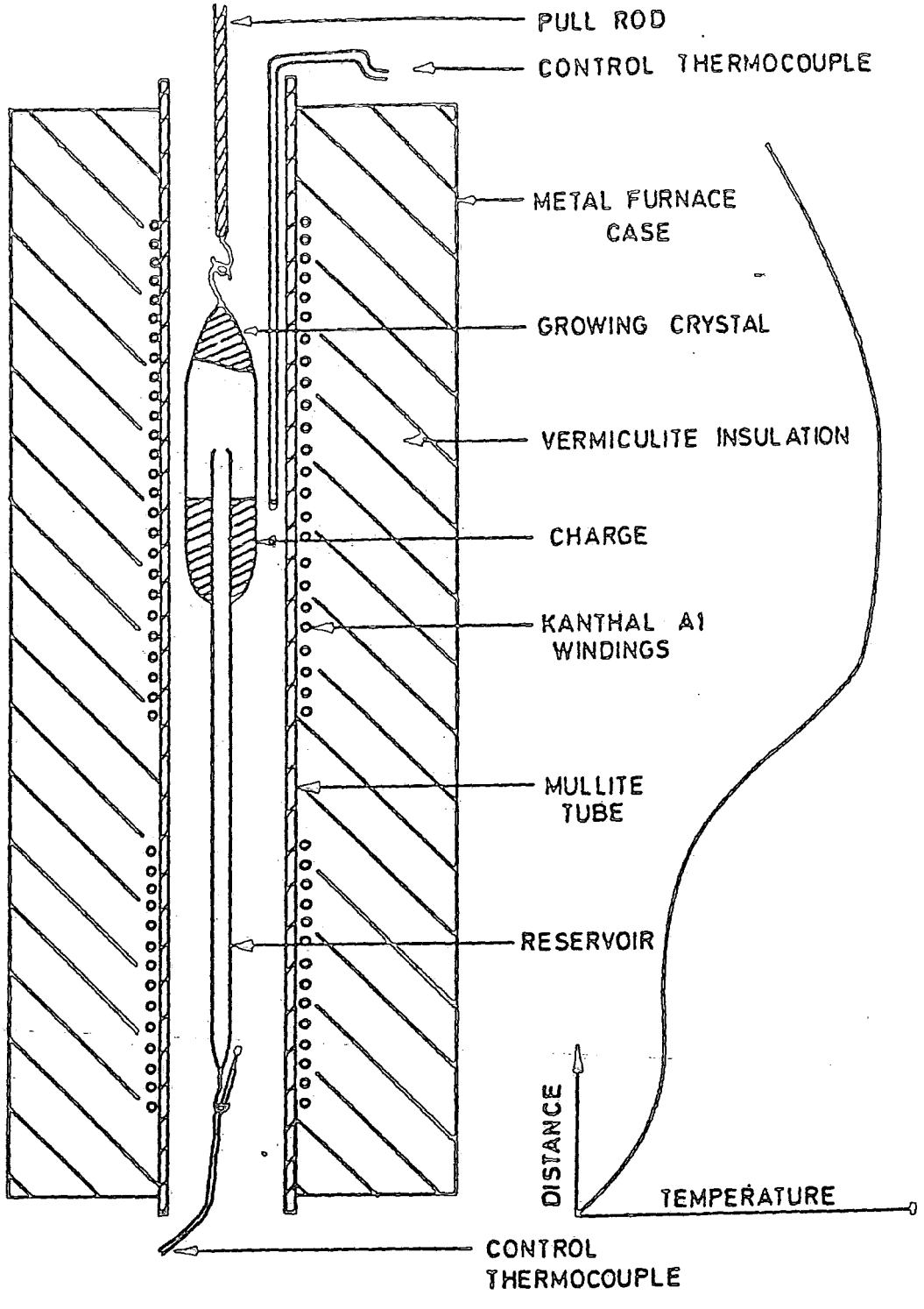

FIGURE 4.1 : Experimental arrangement for the growth of CdS and $Cd_yZn_{1-y}S$ single crystal from the vapour phase.

tail tube was adjusted to provide an appropriate vapour pressure over the evaporating charge. Normally with mixed crystals, before growth, the charge was first converted to a solid solution of $Cd_yZn_{1-y}S$ in a reverse temperature gradient. Then as the capsule was pulled through the furnace and a temperature gradient for growth was established, the various vapour species diffused to the cooler regions resulting in supersaturation of the vapour and growth of the crystal. For CdS, a boule 3 cm long and 1 cm in diameter took about two weeks to grow, allowing three days to cool the grown crystal to room temperature. As the growth axis of a single crystal boule did not usually coincide with the C-axis, and to eliminate any effects in measurments which might be due to devices being made on different crystallographic planes, all the boules were oriented along the C-axis by the X-ray back reflection technique. In all cases this was done so that the boules could be cut parallel to the basal $(000\bar{1})$ planes.

4.3 Scanning Electron Microscopy

A Cambridge Stereoscan S600 scanning electron microscope (SEM) has been used to investigate the surface topographies of both single crystals and films of CdS and $Cd_yZn_{1-y}S$.. The cross-sections of some of the polycrystalline films were imaged to assess film thickness and degree of grain growth. A schematic diagram of the instrument used is illustrated in Fig. 4.2. The SEM may be used in several different modes, where the signals are derived from the different interactions between the electron beam and the specimen [4]. Some of these are illustrated in Fig. 4.3. In most of the work reported here, the secondary emmission (SE) mode was employed. The principle of operation is that an electron beam is scanned across the sample in a raster, and the secondary electrons that are emitted from the sample surface are

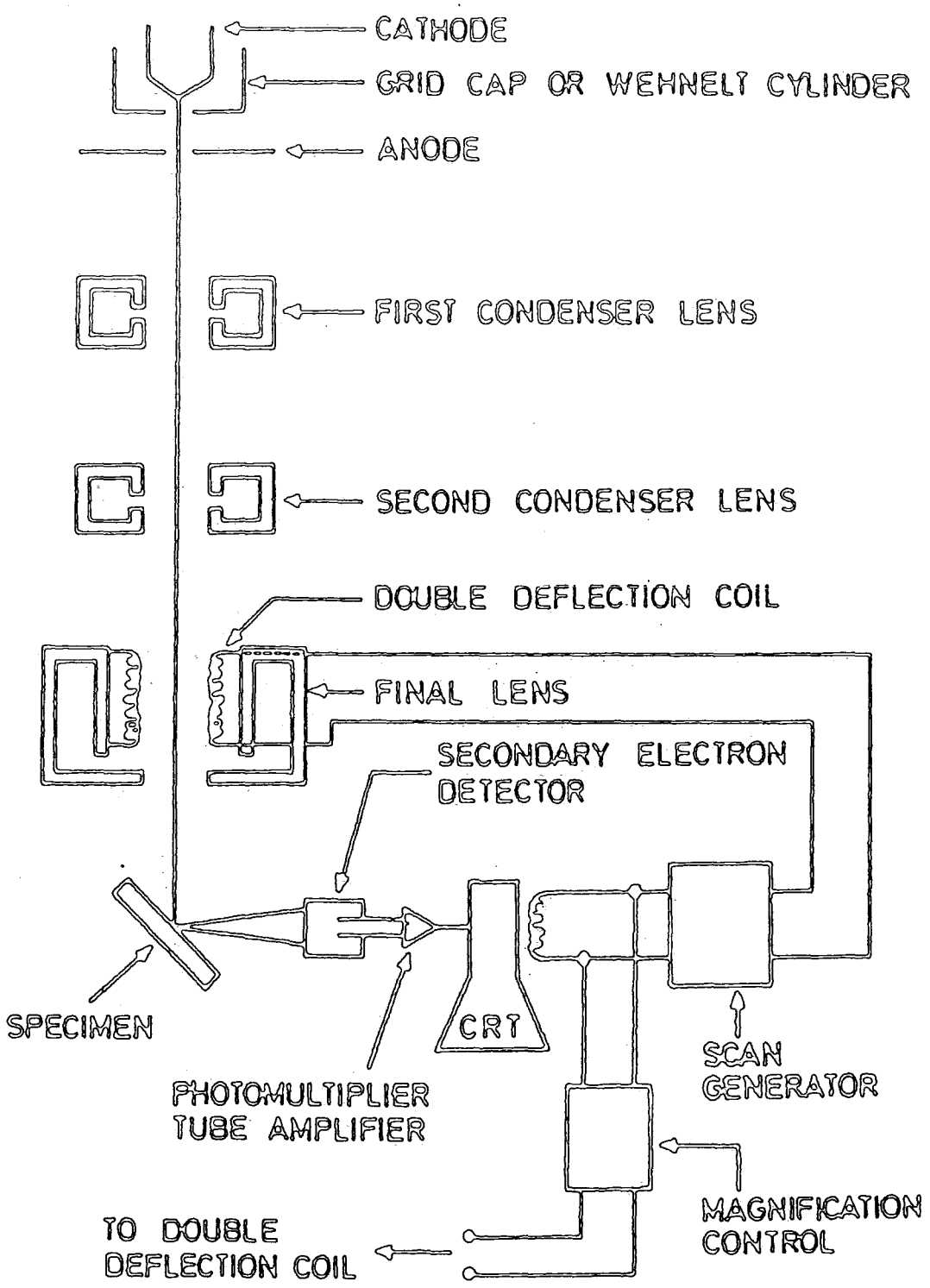

FIGURE 4.2 : Schematic diagram of the Scanning Electron Microscope

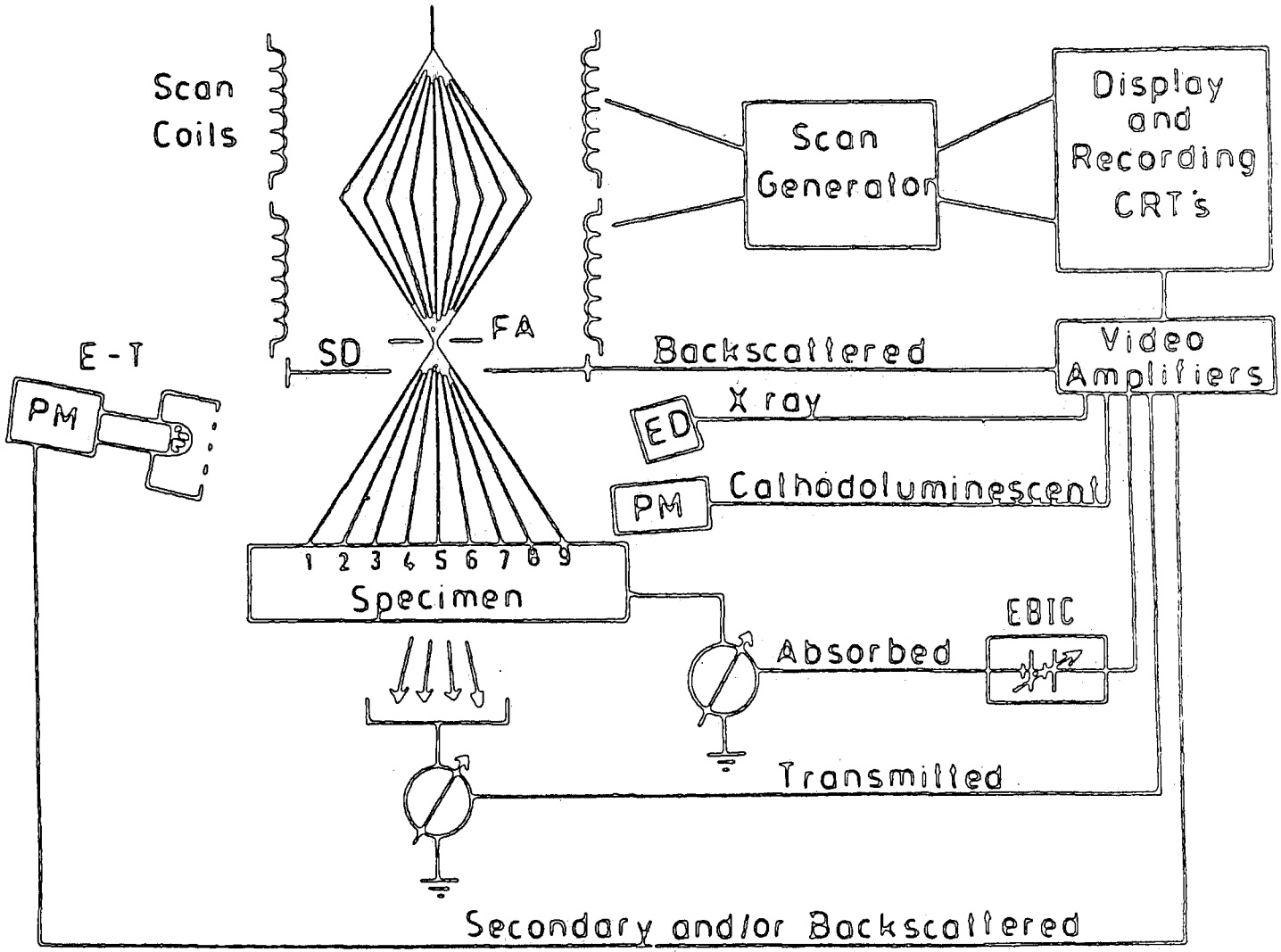

FIGURE 4.3 : Schematic diagram showing some of the various modes of operation of the SEM.

collected by an Everhart-Thornley detector consisting of a scintillator and photomultiplier (PM). The output from the PM is taken through a head amplifier and fed into the input of a cathode ray tube monitor, which is scanned with the same generator as that used to scan the electron beam across the sample. In this way a micrograph of the secondary emitted electrons from the specimen surface is generated.

For the SEM investigation of material evaporated onto glass substrates, samples were sputter coated with gold to provide a conducting path to avoid charge build-up.

4.4 Reflection High Energy Electron Diffraction

RHEED studies were carred out in a JEM 120 transmission electron microscope (TEM). The main advantages of this technique are that it is non-destructive, easy to apply and has a short turn around time. These features make the technique particularly suitable for following changes occurring as a result of different treatments at various stages of device fabrication. The technique was used to identify the phases of Cu_xS produced on both single crystal [5] and thin film CdS [6], the phase of the evaporated CdS films and the degree of preferred orientation of the crystallites in these films.

In RHEED, an electron beam with energy in the range of 10 to 100keV produces diffraction from atomic planes at the surface of crystalline specimens. If the Bragg diffraction requirement is fulfilled

$$\lambda = 2d_{hk\ell} \sin \theta \qquad 4.1$$

where the wavelength (λ) is dependent upon the accelerating voltage (and varies from 0.12 to 0.04 Å in the energy range from 10 to 100keV), $d_{hk\ell}$ is the interplanar spacing, and θ is the Bragg angle between the

the incident beam and the atomic planes. The interplanar spacing is of the order of Angstroms ($\mathring{A}$), therefore to obtain a diffraction pattern the Bragg angle must have a value between 1.5^{o} and 0.5^{o} for electrons in the energy range mentioned. Thus, in this technique, only those crystal planes that are tilted at less than a few degrees to the surface of a specimen will diffract an electron beam incident at a grazing angle. Fig. 4.4 illustrate the necessary conditions to produce an electron diffraction pattern. Each real space plane (hkℓ) gives rise to a reciprocal lattice point which has the same set of Miller indices, and each reciprocal lattice point lies on a line which passes through the origin of reciprocal space and which is perpendicular to its corresponding plane in real space. When the incident beam strikes the crystal plane (hkℓ) at the Bragg angle θ, then it is diffracted to form a diffraction spot at P on the fluorescent screen, placed at a distance L from the sample. In three dimensions the Bragg reflection condition can be determined using a geometrical model known as the Ewald sphere construction and this is illustrated in Fig. 4.5. In this graphical representation of Bragg's law of diffraction, constructive interference occurs only when the reflection sphere intersects points in the reciprocal lattice. As the radius of this sphere is $1/\lambda$, it is very large compared with the reciprocal lattice distances of $1/d_{hk\ell}$ for the diffraction of a beam of high energy electrons. Generally at high energies, such as 100 keV, the reflection sphere can be approximated to a plane section through the reciprocal lattice, and consequently the RHEED pattern observed corresponds to this plane section, lying perpendicular to the direction of the incident beam. With small valves of Bragg angle the relationship

$$\lambda L = R_{hk\ell}\, d_{hk\ell} \qquad 4.2$$

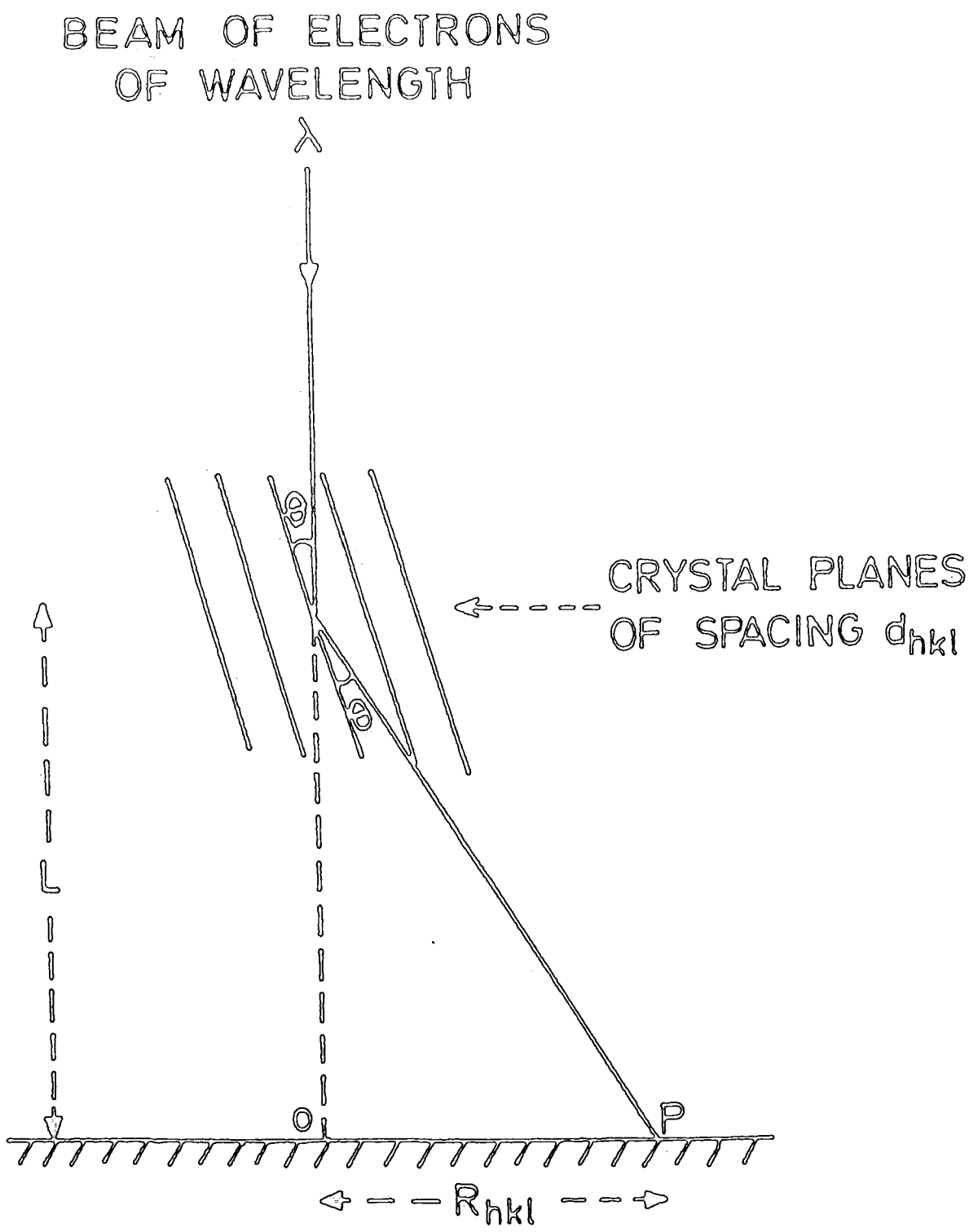

FIGURE 4.4 : Schematic diagram illustrating the RHEED technique.

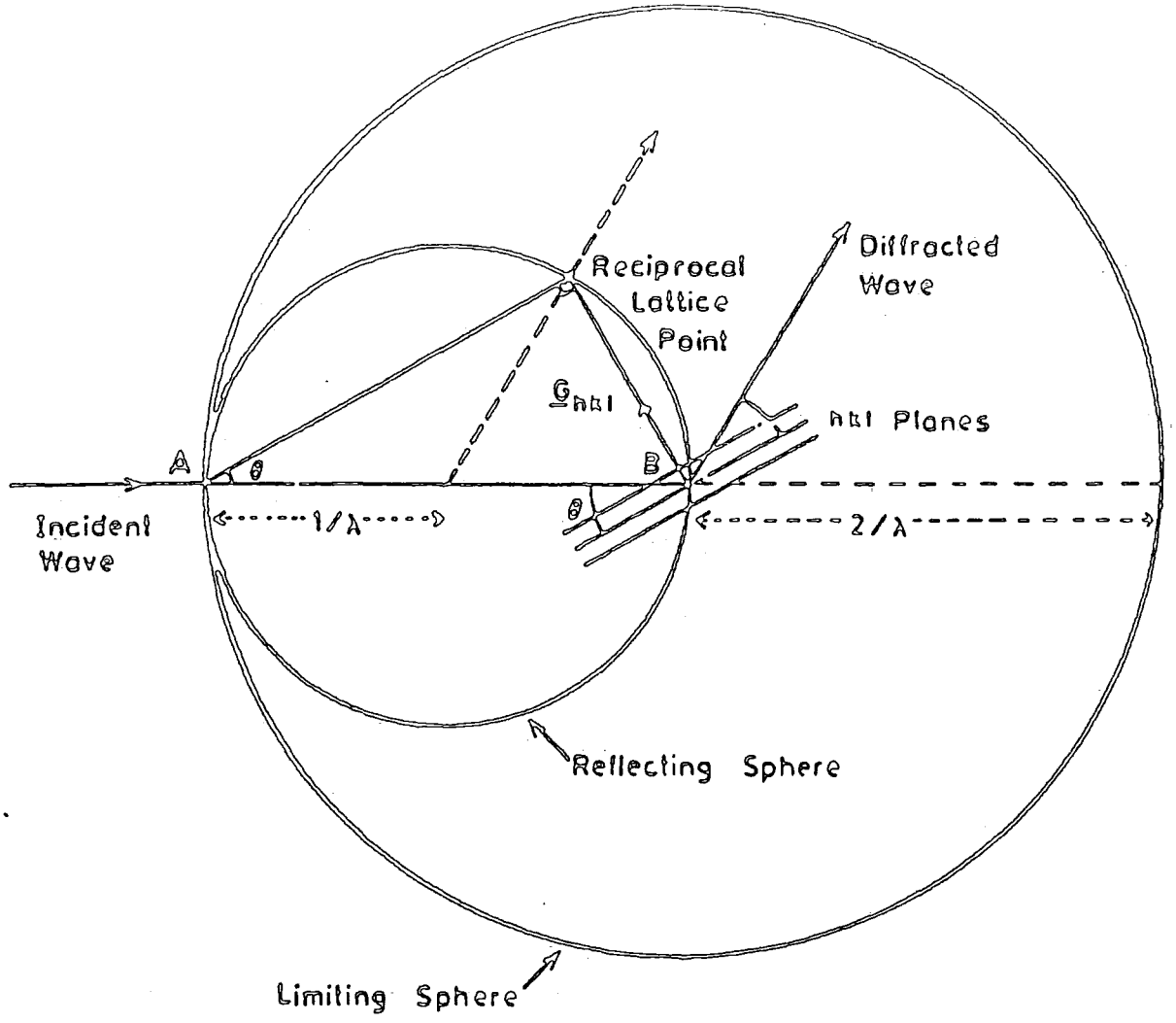

FIGURE 4.5 : The Ewald sphere construction.

can be derived from the Bragg condition for constructive interference (see Fig. 4.4). This is the camera equation for the electron microscope and is used to obtain the interplanar spacings $d_{hk\ell}$ from the observed diffraction pattern. Russell [7] gave a detailed account of the practical applications of the RHEED technique in the study of a wide range of materials.

In the present work, the RHEED technique was used extensively to identify both the crystal structure and the phase of the copper sulphide layer formed on single crystal and thin film CdS and on $Cd_yZn_{1-y}S$ single crystals.

4.5 Measurement of Spectral Response

The spectral response of devices was measured using light from the exit slit of a Barr and Stroud double prism monochromator, type VL2, fitted with Spectrosil 'A' silica prisms. A 250 watt quartz halogen lamp, driven by a d.c. stabilised power supply, was used as the light source. The energy distribution of the source at the exit slit, which includes the varying dispersion of the prism monochromator, was measured using a Hilger and Watts Schwartz compensated linear vacuum thermopile type FT 16301/60297. The light source was chopped at 10 Hz and the resulting thermopile output signal was recovered using a Brookdeal lock-in amplifier type 9401 and a Brookdeal nanovolt preamplifier type 431. In addition, an accurate calibration of the spectral distribution of energy at the exit slit over the wavelengths $0.45>\lambda>0.95\mu m$ was made using a silicon PIN diode (type 10DF). In order to avoid the effects of wavelength drift in the monochromator, the calibration procedure was repeated using a sodium source. Almost all of the spectral measurements were taken over the range from 0.4 to 2.0 μm. The

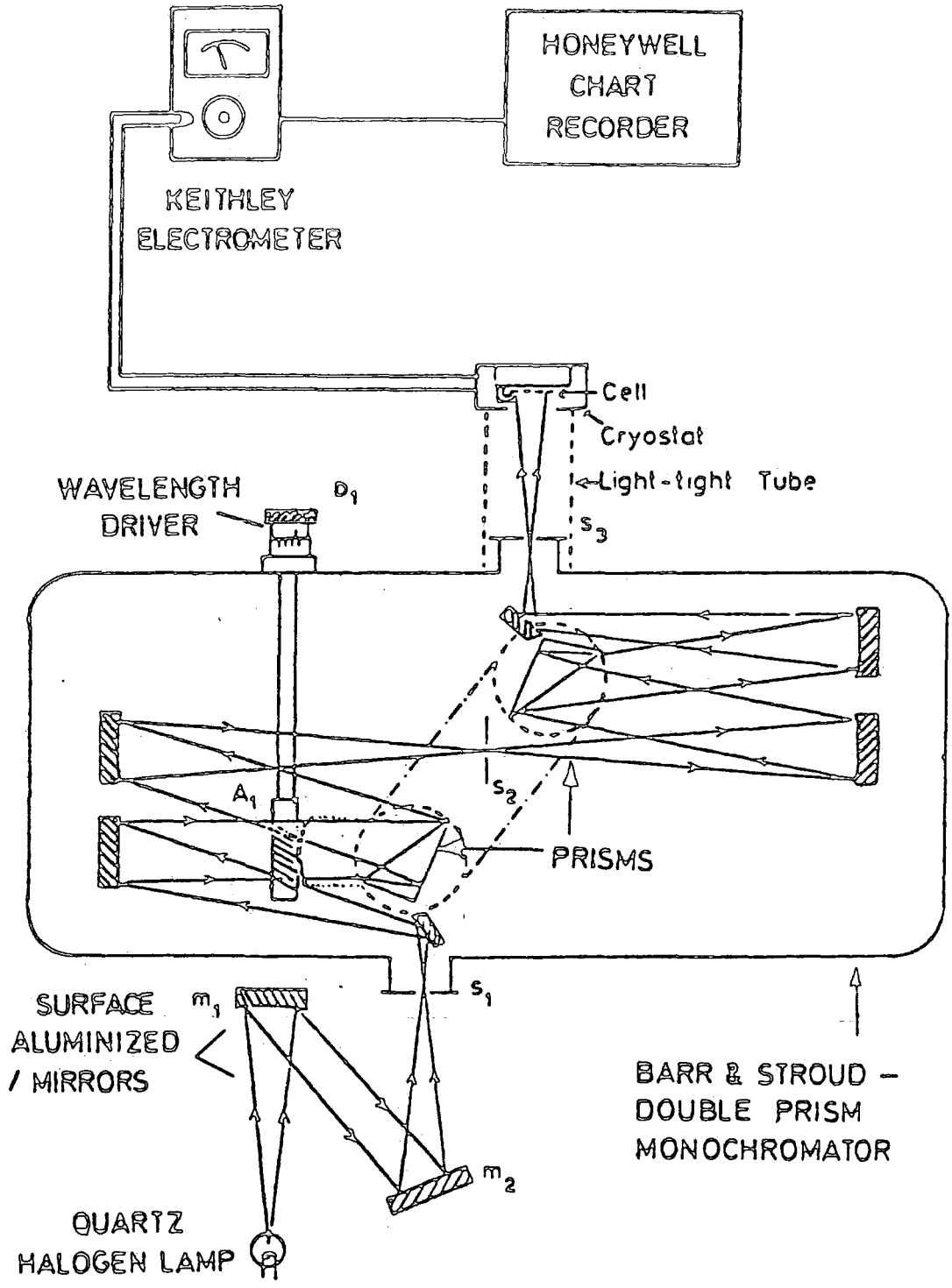

FIGURE 4.6 : Schematic diagram of the spectral response measurement system.

schematic diagram for the system used for the measurement of spectral response is shown in Fig 4.6. The device under test was mounted in a cryostat where its temperature was monitored using a copper constantan thermocouple. The device was illuminated from the front on the Cu_xS face in the front wall mode. The cryostat also has a second window for bias illumination when required. The photovoltaic current and voltage were measured using a Keithley Electrometer model 602, which has a high impedance for voltage measurements, and very low input impedance for current measurements. Thus, the recorded open circuit voltage and short ciruit current spectra were adequate approximations of V_{oc} and J_{sc}. The output of the electrometer was recorded by a Bryans Model BS 312 high impedance chart recorder.

4.6 Measurement of Current-Voltage Characteristics

Current-Voltage (J-V) characteristics were recorded in the dark and under AM1 illumination at room temperature. Simulation of AM1 illumination was accomplished using a 1.5 kW quartz halogen strip lamp with a parabolic reflector housing, and with a tray of flowing water (2 cm deep) placed between the source and the sample to reduce the infra-red content (Fig 4.7). The source was calibrated using a standard silicon PIN diode (type 10DF, United Detector Technology), and adjusting the distance between the source and the sample to provide 100 mW/cm^2 constant illumination. Point by point current-voltage measurements were carried out using a high impedance Bradley voltometer (type 173B), and a low impedance Hewlett Packard ammeter (type 3465B). The bias voltage was provided by DC voltage calibrator type 2003 (Time Electron Ltd). An automatic system consisting of a power supply and a Bryans model 21001 X-Y recorder was also used in the initial tests to monitor the changes in the characteristics with different treatments. The

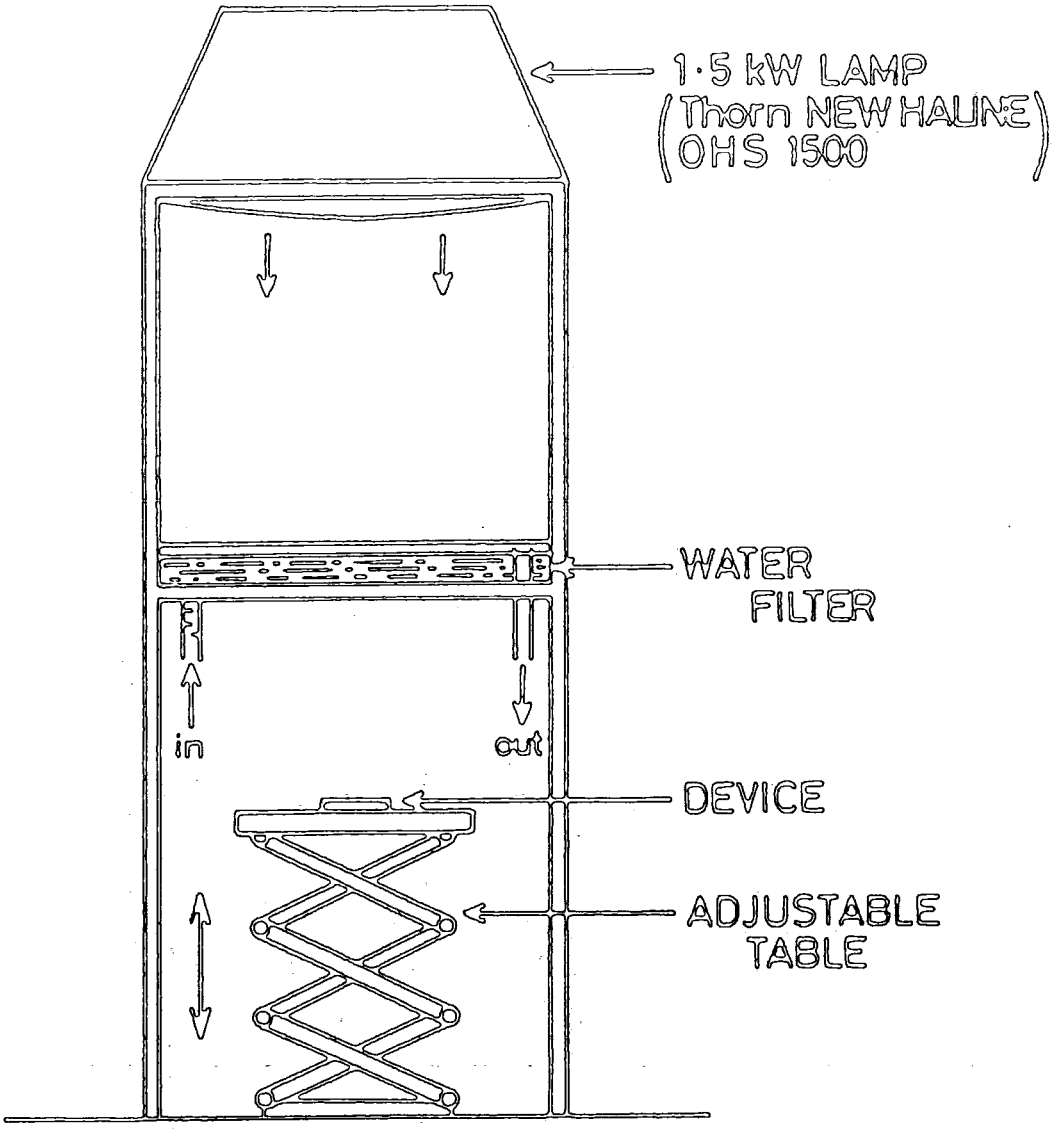

FIGURE 4.7 : Solar Simulator for AM1 illumination.

measurement of temperature dependence of current-voltage characteristics was studied using a cryostat. The system was designed around a 2 cm i.d. gas exchange vessel. This was connected to a copper specimen block fitted with a heater at one end and to the liquid nitrogen container of about 1 litre capacity at the other. An Edwards 11cc oil diffusion pump was used to maintain the pressure in the cryostat below 10^{-3} torr.

4.7 Capacitance Measurement

The C-V measurements on the cells were determined using a Boonton 72B capacitance meter which operates at 1 MHz. These characteristics were measured point by point by applying the bias voltage through a DC calibrator type 2003. Some C-V measurements were carried out using an integrated circuit voltage ramp which allowed the scan rate to be adjusted from 1 volt/sec to 1000 volt/sec. The output was recorded with a Hewlett Packard X-Y-T recorder model 7041 A.

Measurement of steady state photocapacitance was made using the same monochromator which was used for spectral response measurements. A schematic diagram of the arrangement used for photocapacitance measurements is shown in Fig 4.8. The output of the capacitance meter was connected to a Bryan chart recorder. The device capacitance was normally compensated with an external capacitance to allow small changes induced by the monochromatic radiation to be recorded. Measurements were made at both room and liquid nitrogen temperature. In all experiments sufficient time was left to allow steady state conditions to be achieved before the scan was made very slowly from long to short wavelength. For infra-red quenching of photocapacitance, a second quartz halogen lamp powered by a 24 d.c. supply was used in addition to the light from the monochromator. The light from the quartz halogen

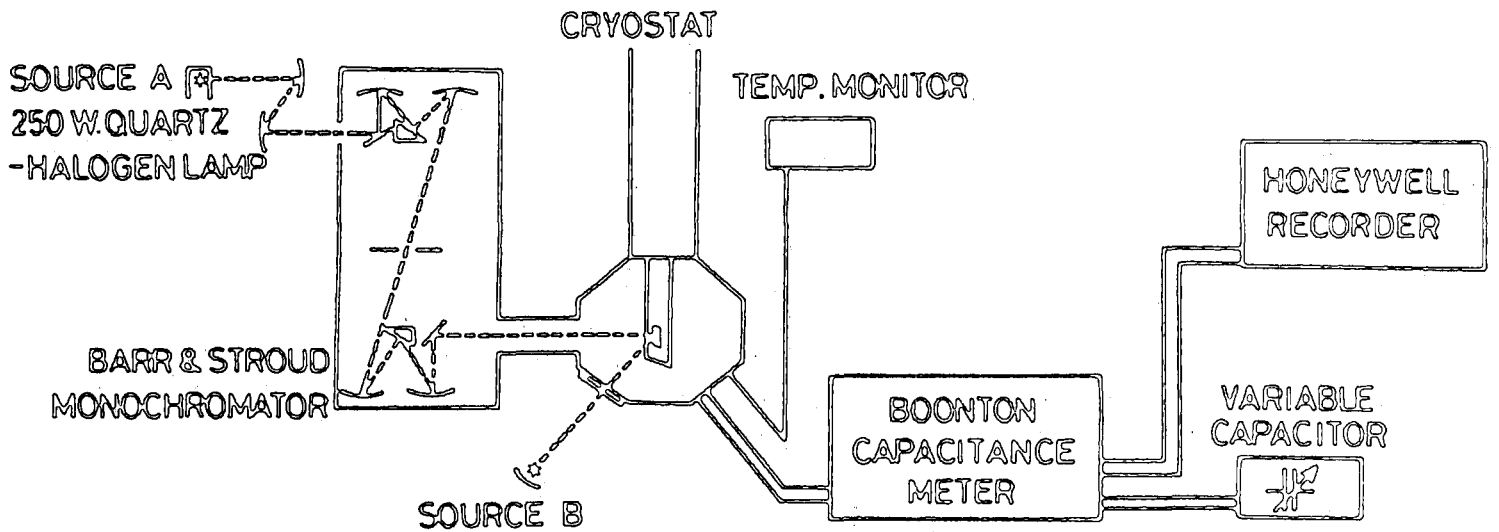

FIGURE 4.8 : Experimental arrangement used for photocapacitance measurements.

source was filtered by Oriel 5200 Å band pass and infra-red absorption filters.

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CHAPTER FIVE

$CdS-Cu_xS$ Single Crystal Solar Cells Formed By The Electroplating Technique

5.1 Introduction

The wet chemiplating process is one method used in the fabrication of $CdS-Cu_xS$ solar cells. Unfortunately this method does not always yield the preferred stoichiometry and the formation of the different phases of copper sulphide cannot easily be controlled. Consequently, an electroplating technique for the formation of Cu_xS has been investigated in an attempt to overcome these problems. A wide range of voltages from +3.0V to -1.0V has been applied to the CdS sample being plated to control the phase of copper sulphide. Firstly the phase of the copper sulphide has been examined by reflection high energy electron diffraction (RHEED). The surface topography of fabricated devices was studied by scanning electron microscopy (SEM). Their current-voltage (I-V) characteristics were measured in the dark and under AM1 illumination. The spectral response of the open circuit voltage (V_{oc}) and short circuit current (I_{sc}) were measured at room temperature and at liquid nitrogen temperature for all devices. In addition capacitance-voltage (C-V) measurements were recorded for all of the heterojunctions fabricated. All of these measurements were made as a function of electroplating bias. Further, the effects of heat treatment in argon and in air on different phases of copper sulphide were compared.

5.2 Studies Of Mechanically Polished And Of Chemically Etched $(000\bar{1})$ CdS Surfaces

Slices 2mm thick were cut from large single crystal boules of

CdS grown from the vapour phase in this laboratory using the technique described in Chapter Two Section (2.2). The single crystal boules were oriented using the Laue X-ray back-reflection technique before they were cut into slices with the large area faces perpendicular to the C-axis. The use of a diamond saw causes damage to the surface, so in order to remove this damage and simultaneously to produce a flat surface, some of the slices were polished by hand on a polishing pad and others were polished on a lapping machine successively using different particle sizes of alumina powder starting with 3 μm and finishing with 1 μm. The slices were then cut into dice of dimension 4 x 4 x 2 mm^3 which were washed successively with acetone, methanol and water to remove grease or oil arising from the cutting process from the surface. They were then etched in concentrated HCl for 20 sec. The etching treatment of the single crystal dice provided a means for the determination of surface polarity [1]. The sulphur face appeared optically matte while the cadmium face was highly reflective. Etching also removed the polycrystalline layer formed at the surface during the mechanical polishing process [2]. The surfaces of the etched devices were examined by SEM. This showed that facetted hillocks exhibiting 6-fold symmetry and having few ledges and kink sites were obtained when the mechanical polishing was carried out using alumina of particle size 1 μm (see Fig 5.1). On the other hand, polishing with alumina of particle size 3 μm gave rise to smaller hillocks with kink sites and many ledges (see Fig 5.2). Polishing with a suede pad and cerium oxide has also been investigated. The effect of etching this polished surface in HCl is illustrated in Fig 5.3. A RHEED pattern obtained from the same surface is shown in Fig 5.4 in which the set of diffraction rings can be attributed to a disordered hexagonal polycrystalline structure of CdS [3].

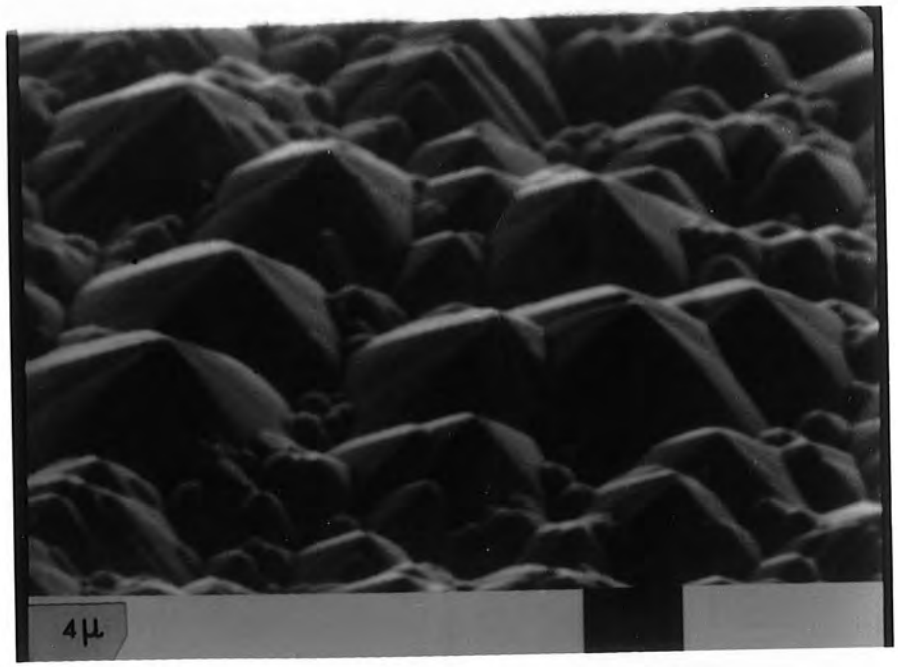

Fig 5.1 Secondary Emission Micrograph of CdS Polished With Alumina of 1 μm Particle Size and Etched In Concentrated HCl for 30 sec.

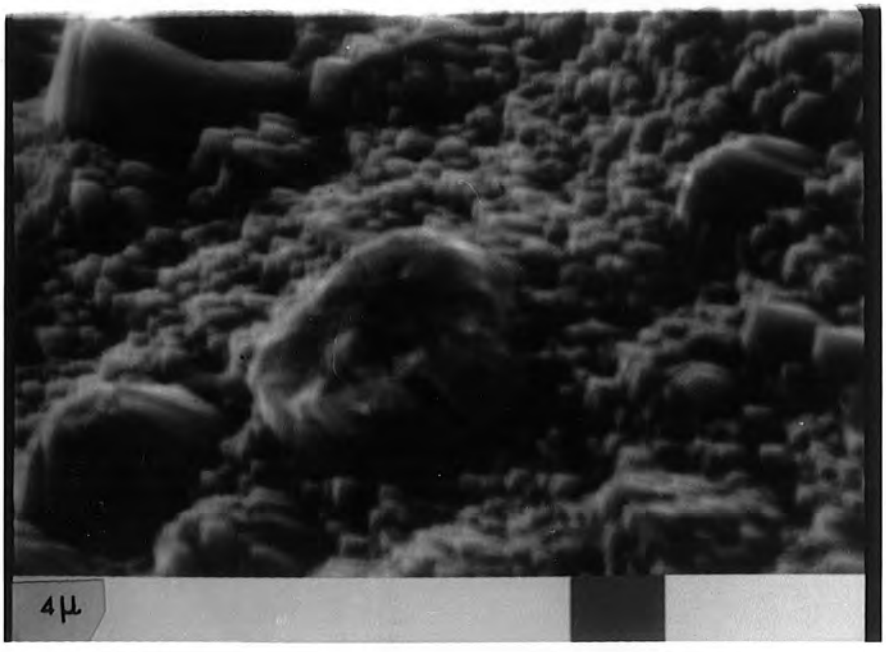

Fig 5.2 Secondary Emission Micrograph of CdS Polished With Alumina of 3 μm Particle Size and Etched In Concentrated HCl for 30 sec.

Fig 5.3 Secondary Emission Micrograph of CdS Polished With A Suede Pad and Cerium Oxide and Etched in Concentrated HCl for 30 sec.

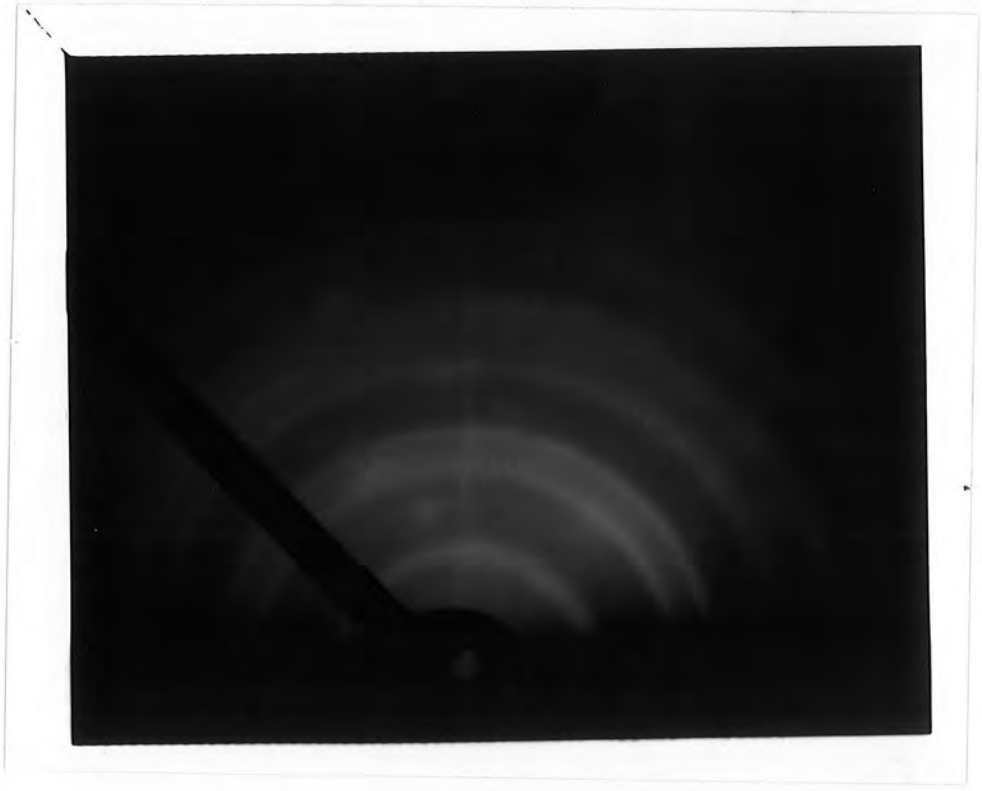

Fig 5.4 100 kV RHEED Pattern From CdS Surface After Polishing With a Suede Pad and Cerium Oxide and Etching In Concentrated HCl for 30 sec.

5.3 The Copper Sulphide Layer

Copper sulphide is the absorber "limb" of the CdS-Cu_xS heterojunction and as such it is an important part of the current generator [4]. Consequently much work has been carried out into an investigation of its properties. It has been established that a strong correlation exists between the efficiency of CdS-Cu_2S solar cells and the composition and the structure of the copper sulphide layer. Chalcocite (Cu_2S) has been found to be the phase producing the most efficient cells [5-8]. Other phases of copper sulphide which have been identified include djurleite ($Cu_{1.96-1.94}S$), digenite ($Cu_{1.765-1.790}S$), anilite ($Cu_{1.75}S$) and covellite (CuS) [8,9].

The chemiplating process used in the formation of Cu_xS does not always yield the desired phase. As it is based on an ion exchange reaction it depends substantially on many parameters which affect the formation of the Cu_xS phase. The aim of the work described in this chapter, therefore, was to investigate and to establish control over the formation of Cu_xS on CdS substrate by the electroplating technique using a wide range of bias.

5.3.1 Heterojunction Formation

After etching the polished dice in concentrated HCl for 20 sec. the devices were subsequently fabricated in the following way:

Indium ohmic contacts were made to the cadmium faces of the dice by pressing a pellet of this element in metallic wire form with diameter of about 0.5 mm and subsequently heating the dice in an argon atmosphere at 200°C for 10 minutes to melt the indium. This method was very reproducible and reliable for obtaining good ohmic contacts [10]. All the faces of the CdS dice except the sulphur ones were coated with an acid resistant lacquer so that the copper sulphide was grown only

on the sulphur face. Immediately before the CdS-Cu_xS heterojunction was formed, the dice were etched in concentrated HCl for 10 sec. in order to remove any oxide layer that might have formed either during or following the ohmic contact process. The wet barrier method was used to form the p-type Cu_xS layer on the sulphur face. The Cu_xS was prepared in a similar way to that described by Caswell et al [11] with the modification made by Oktik et al [12] as follows:

i) First of all, the CuCl powder was treated by washing it in 10% HCl to remove any cupric ions. It was then rinsed with acetone and dried in a vacuum before being used to prepare the plating solution.

ii) 75 ml of deionized water was heated in a closed reaction vessel and oxygen free nitrogen was continuously bubbled through the liquid to remove any dissolved oxygen.

iii) 12 ml of concentrated HCl acid was added to the water and the heating and nitrogen gas flow was continued.

iv) 7 ml of hydrazine hydrate was added to produce a solution with a pH of 2.5 as measured by pH paper.

v) 1 gm of freshly prepared CuCl (see i above) was added.

vi) The dice were pre-heated in deionized water at 95°C before being immersed in the chemiplating solution.

vii) After heating the solution up to 95°C, the pH was measured again and re-adjusted to the value of 2.5 by using a small amount of hydrazine hydrate or hydrochloric acid.

In the electroplating method an external D.C. potential was applied to the CdS through the indium contact. A section of platinum sheet acted as the counter electrode. For the formation of Cu_xS, this fixed electrode and the die were immersed with the required potential applied to the die for the 10 sec. plating period. The result of the chemical

displacement between the cuprous and cadmium ions is given by the following reaction:

$$CdS + 2CuCl \rightleftharpoons Cu_2S + CdCl_2$$

The topotaxial Cu_2S layer is produced at the CdS surface while the cadmium chloride goes into the solution by exchanging 1 Cd^{++} ion with $2Cu^{+}$ ions.

5.3.2 Examination of Copper Sulphide Phases on CdS

Cu_xS phases have been investigated non-destructively by (RHEED). This technique is described in Chapter Four Section (4.4). It has been used to study the phases of copper sulphide for several years [13-19]. In this work, all RHEED patterns were taken with the electron beam incident either parallel to a $<10\bar{1}0>$ direction (a-axis of the CdS) or parallel to a $<11\bar{2}0>$ direction which was obtained after a 30^{o} rotation of the sample about the C-axis. By applying a wide range of electroplating voltages between +3.0V to -1.0V various phases have been produced and identified. The electron diffraction patterns obtained from a layer which had been deposited while applying a bias of +0.01V to the CdS are shown in Figs 5.5a and b. These can be indexed as arising from the [100] and [010] zone axes respectively of the orthorhombic chalcocite phase [14]. There is a close crystallographic relationship between the hexagonal structure of cadmium sulphide and orthorhombic Cu_2S [17]. Since the a-axes of CdS and chalcocite are coincident, there are three possible orienations of the orthorhombic unit cell of chalcocite based on the sulphur lattice of the hexagonal CdS. These three possible unit cell orientations are shown as M, L and R in Fig 5.6. When the beam is incident along the a-axis, [100], of the unit cell M, it is simultaneously incident along a <430> direction in each of the unit cells designated L and R. Similarly, when the electron

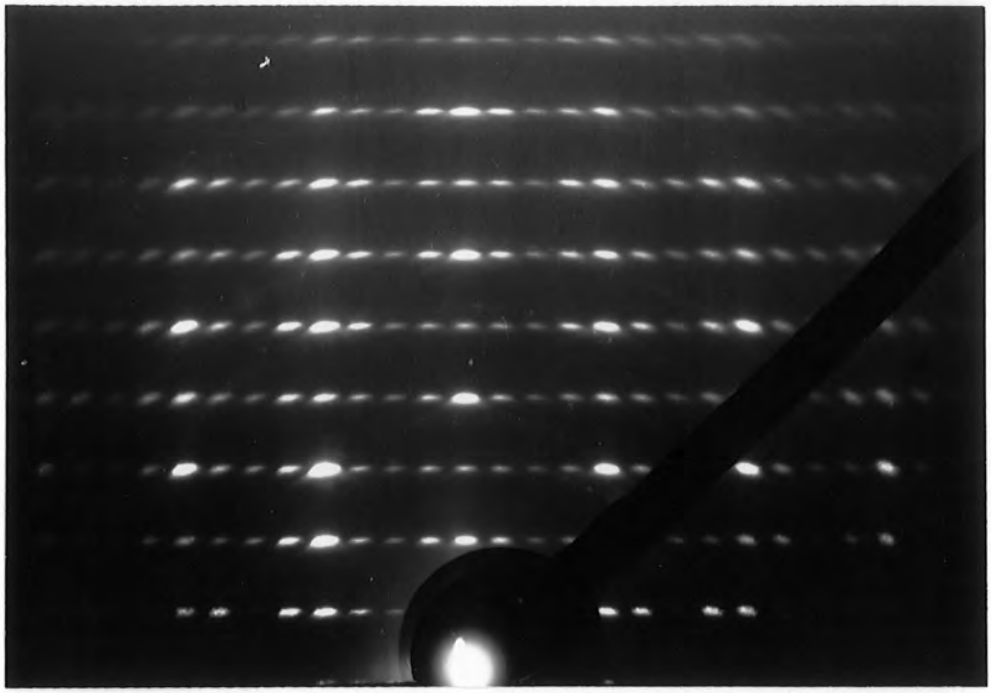

Fig 5.5a RHEED Pattern of Chalcocite Phase Along [100] Direction of CdS

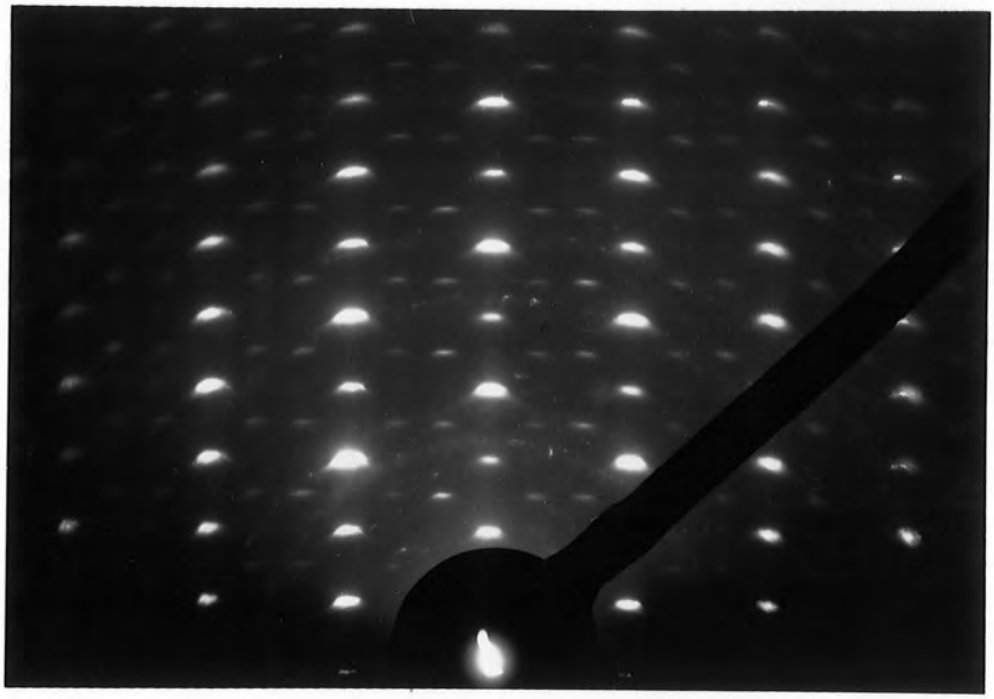

Fig 5.5b RHEED Pattern of Chalcocite Phase Along [120] Direction of CdS

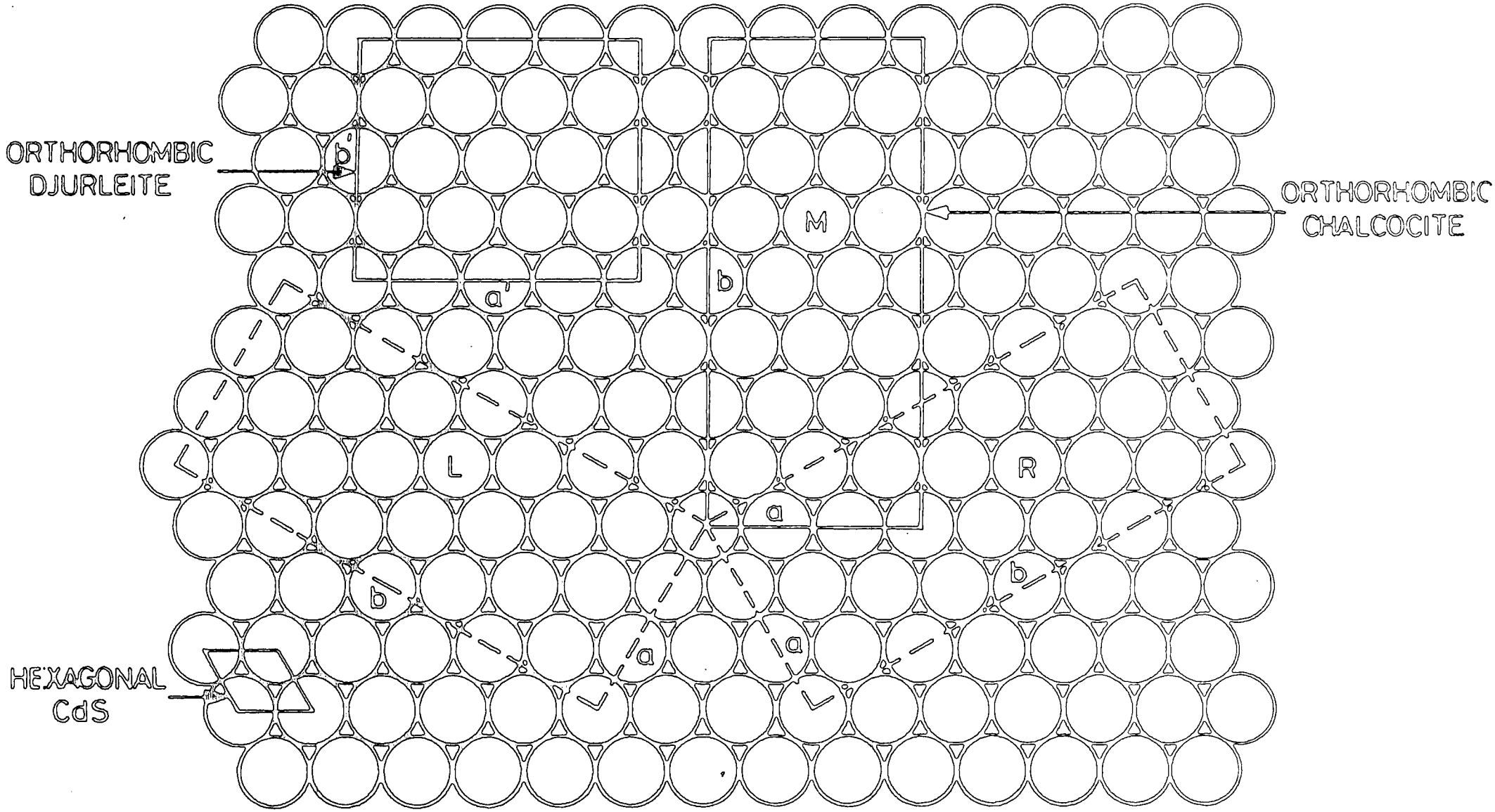

FIGURE 5.6 : Unit cell geometries of chalcocite (in three orientations) and djurleite in the basal plane of CdS.

beam is incident along the b-axis, <010> of the unit cell M, it is simultaneously incident along <410> directions in the unit cells L and R. In both cases the reflections from the two different zone axes are coincident within the limits of experimental measurement [15]. Thus, although the patterns in Fig 5.5 show single arrays of reflections which implies a single crystal structure, there are in fact sets of grains in each of the three orientations corresponding to the unit cells M, L and R. This was indeed confirmed by the recurrence of the same pattern after every 60^{o} of rotation about the C-axis. The RHEED patterns in Fig 5.7 were obtained from Cu_xS prepared by applying a bias of +1.0V during the electroplating process. The reflections in these patterns can be attributed to those arising from [100] and [010] axes respectively of the orthorhombic unit cell of the djurleite phase of copper slphide. As with the chalcocite unit cell, the djurleite one can similarly take up any one of three orientations and the patterns in Fig 5.7 are also composite ones formed from grains in three different orientations. The patterns from djurleite are characterised by the rows of closely spaced spots lying in the direction perpendicular to the shadow edge of the sample and arising from the much larger inter-planar spacing in the c direction ($c \simeq 27^{o}A$) for djurleite.

By applying a bias of +0.1V to the CdS during plating, a mixture of the phases of chalcocite and djurleite has been produced. RHEED patterns from such a mixture are illustrated in Fig 5.8. The phase obtained by using a plating bias of +3.0V yields the RHEED patterns shown in Fig 5.9a and b. By analysing these patterns it was established that they could be attributed to the presence of covellite having a hexagonal structure [15]. From the work in the last reference, the RHEED patterns in Figs 5.9a and b correspond to $[2\bar{2}0\bar{1}]$ and $[\bar{2}\bar{1}31]$ zone axes respectively. The RHEED pattern in Fig 5.9a shows that the arced

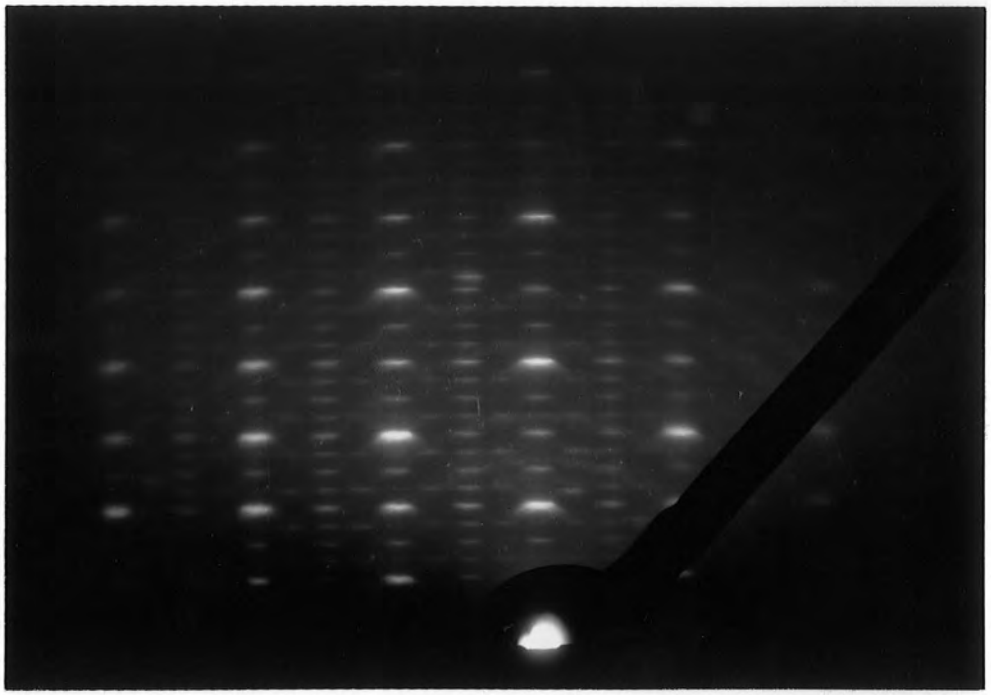

Fig 5.7a RHEED Pattern of a Pure Djurleite Along [100] Direction of CdS

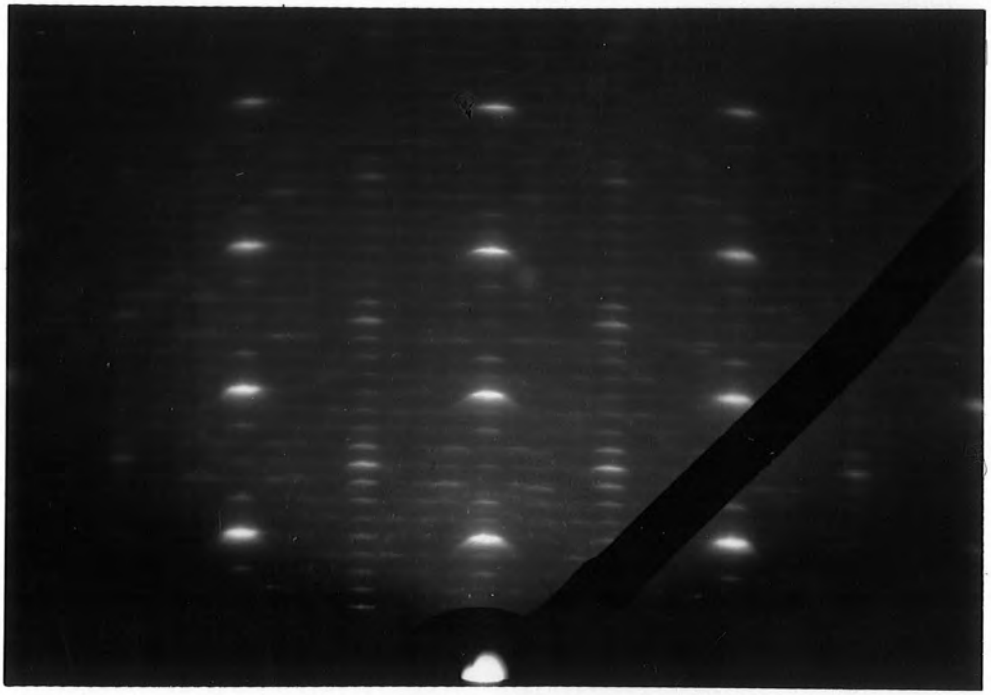

Fig 5.7b RHEED Pattern of a Pure Djurleite Along [010] Direction of CdS

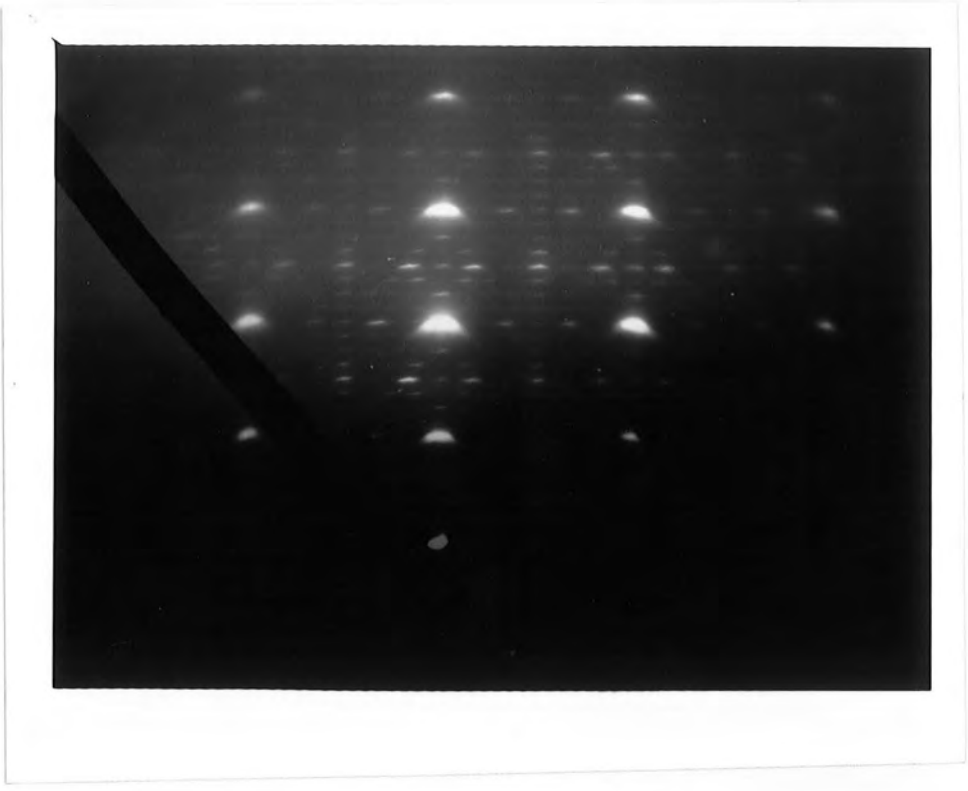

Fig 5.8 RHEED Patterns of a mixture phase of chalcocite and djurleite

Fig 5.9a RHEED Patterns of a covellite phase with the beam along [100] axis of CdS

spots arise from two different grains in twinned orientation which yield sets of reflections in positions that are mirror image related across the fibre axis. Consequently the arced spots in Fig 5.9a do not form a single continuous array. In the other orientation shown in Fig 5.9b these grains in twin related positions give rise to reflections that are symmetrical about the fibre axis and are consequently coincident.

An unidentified phase was obtained for a device fabricated using a bias of -1.0V during topotaxial Cu_xS layer formation.

The effect of the electroplating bias on the phase of copper sulphide during the growth of the Cu_xS on the sulphur face of CdS can be summarised as shown in Table 5.1.

bias (V)	Phase of copper sulphide
+3.0	Covellite
+1.0	Pure djurleite
+0.1	Mixture of djurleite and chalcocite
+0.01	Chalcocite
-0.1	Djurleite

Table 5.1 The effect of electroplating bias on the phase of copper sulphide.

5.4 Properties Of As-made CdS-Cu_xS Solar Cell as a Function Of Electroplating Bias.

5.4.1 Current-Voltage Characteristics

After studying the phase of copper sulphide, ohmic contacts were made by evaporating gold dots of 1 mm diameter onto the copper sulphide layers to complete the device fabrication. The current-voltage characteristics of these devices with topotaxial Cu_xS layers prepared at different bias potentials were measured in the dark and under AM1 illumination and are shown in Fig 5.10. No rectification was observed for heterojunctions prepared using biases of +3.0V or -1.0V during electro-

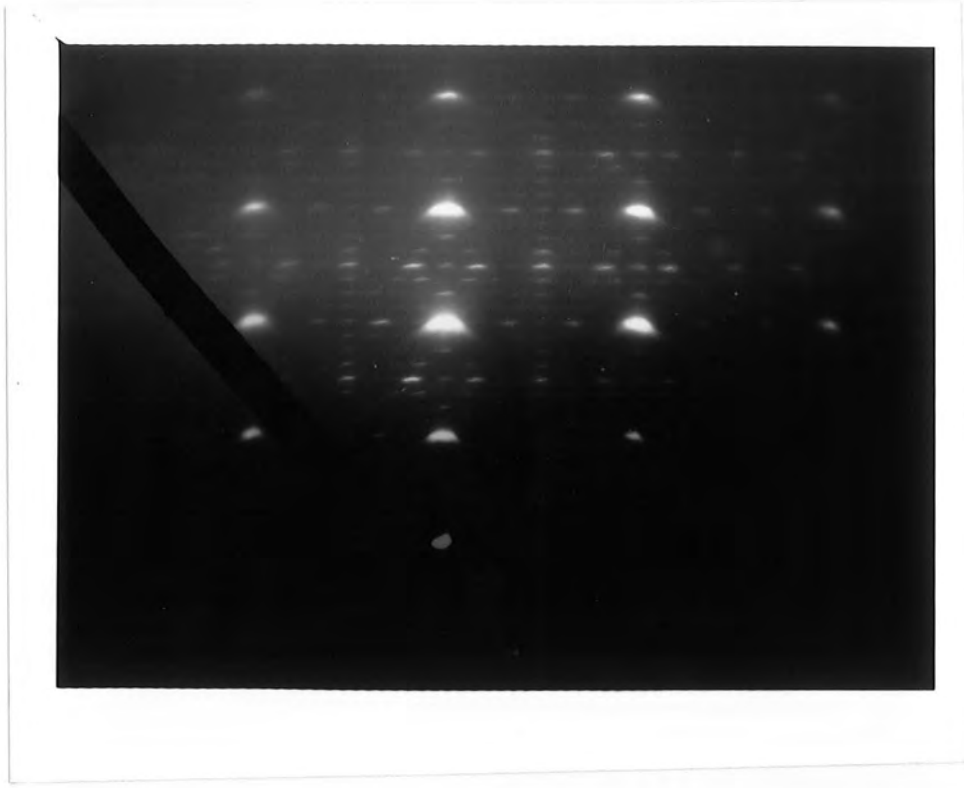

Fig 5.8 RHEED Patterns of a mixture phase of chalcocite and djurleite

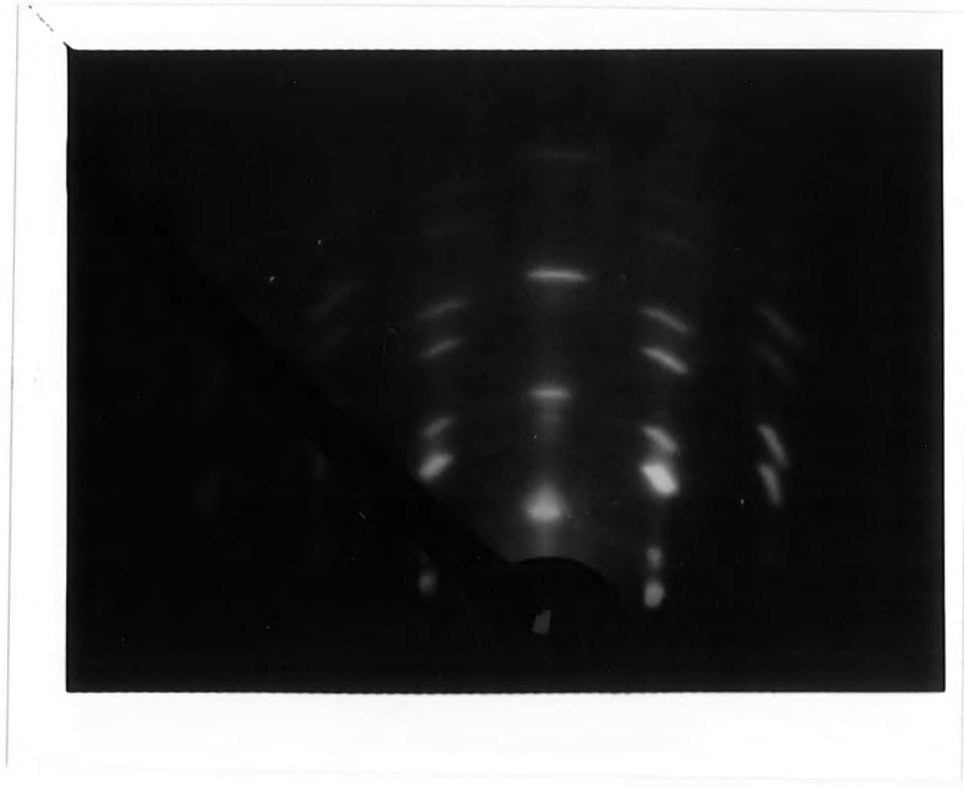

Fig 5.9a RHEED Patterns of a covellite phase with the beam along [100] axis of CdS

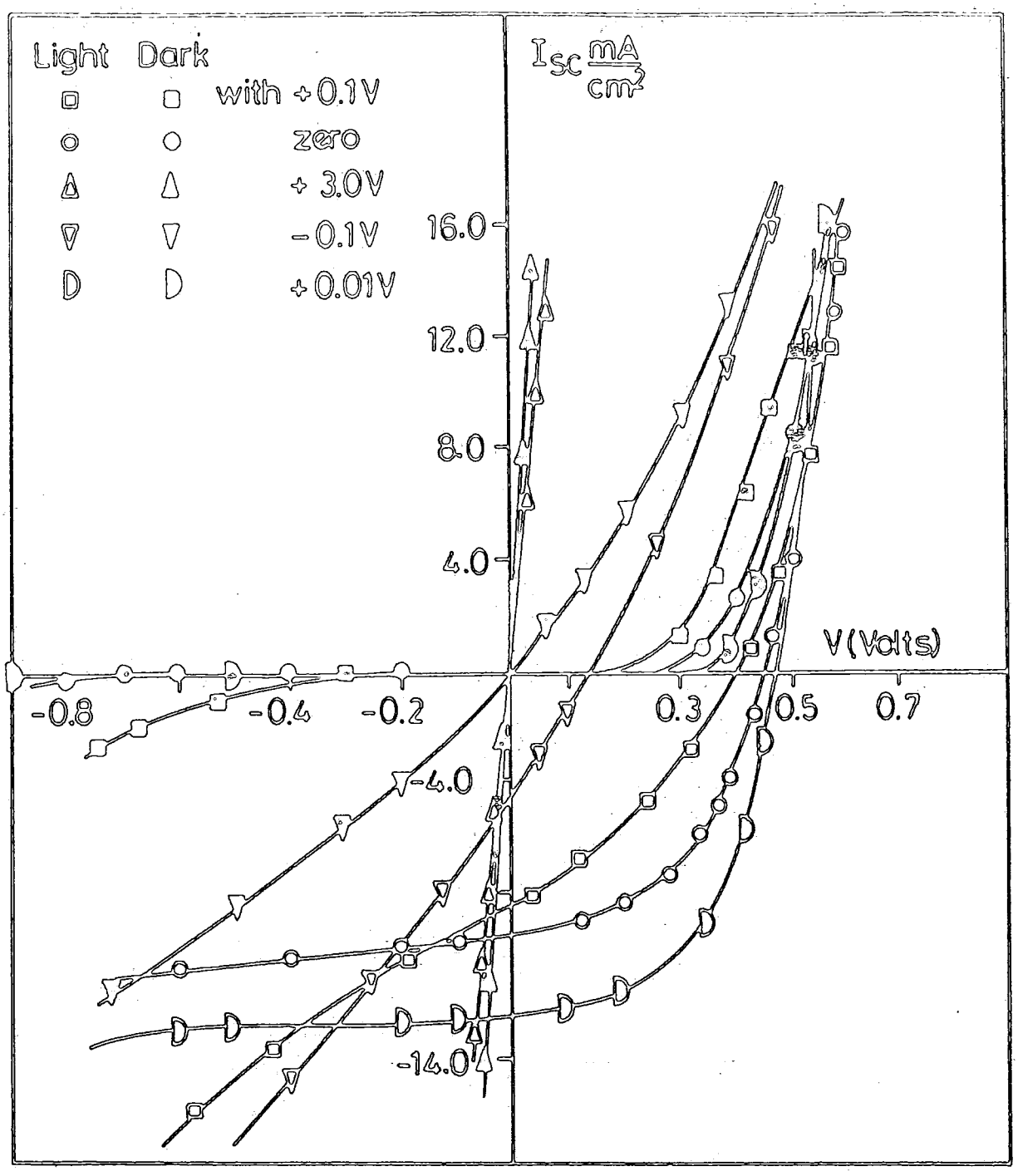

Fig 5.10

Current-voltage characteristics for as-made devices as a function of bias potential during plating, in the dark and under AM1 illumination.

plating. When the bias potential used for plating was -0.1V the photovoltaic behaviour was also very poor with a high leakage current and a small value of V_{oc}. If the heterojunction was formed with zero plating bias, the characteristic was improved but the value of I_{sc} was still small. The I_{sc}, V_{oc} and fill factor (FF) approached their best values in this particular study when a bias of +0.01V was used during the preparation of the Cu_xS layer. Under AM1 illumination devices fabricated on such layers typically gave rise to a V_{oc} of 0.475V. an I_{sc} of 12.3 $mA.cm^{-2}$ a fill factor (FF) of 0.545 and an efficiency of 3.15%. The current-voltage characteristics of such an as-made device are shown separately in Fig 5.11. All of these device parameters were significantly worse when using a bias potential +0.1V for plating. The parameters of as-made devices fabricated on Cu_xS layers formed at different values of bias potential are summarised in Table 5.2.

bias (V)	OCV (V)	SCC ($mA.cm^{-2}$)	FF	γ %
+3.0	0	0	0	0
+1.0	0.05	1.4	0.25	0.02
+0.1	0.41	8.4	0.31	1.08
+0.01	0.475	12.3	0.545	3.15
-0.1	0.15	4.6	0.23	0.16

Table 5.2 The dependence of the parameters of as-made devices on the electroplating voltage.

The variation of effective parameters OCV, SCC, FF and γ with the bias potential is presented graphically in Fig 5.12. Reasonable devices were only obtained for plating potentials in the range from +0.1V to -0.1V. The optimum value for each of these parameters is achieved by using a plating bias of +0.01V $\sim$0.02V. From Fig 5.12 it can be seen that the values of all cell parameters decrease more rapidly with small changes to negative values of plating potential than they

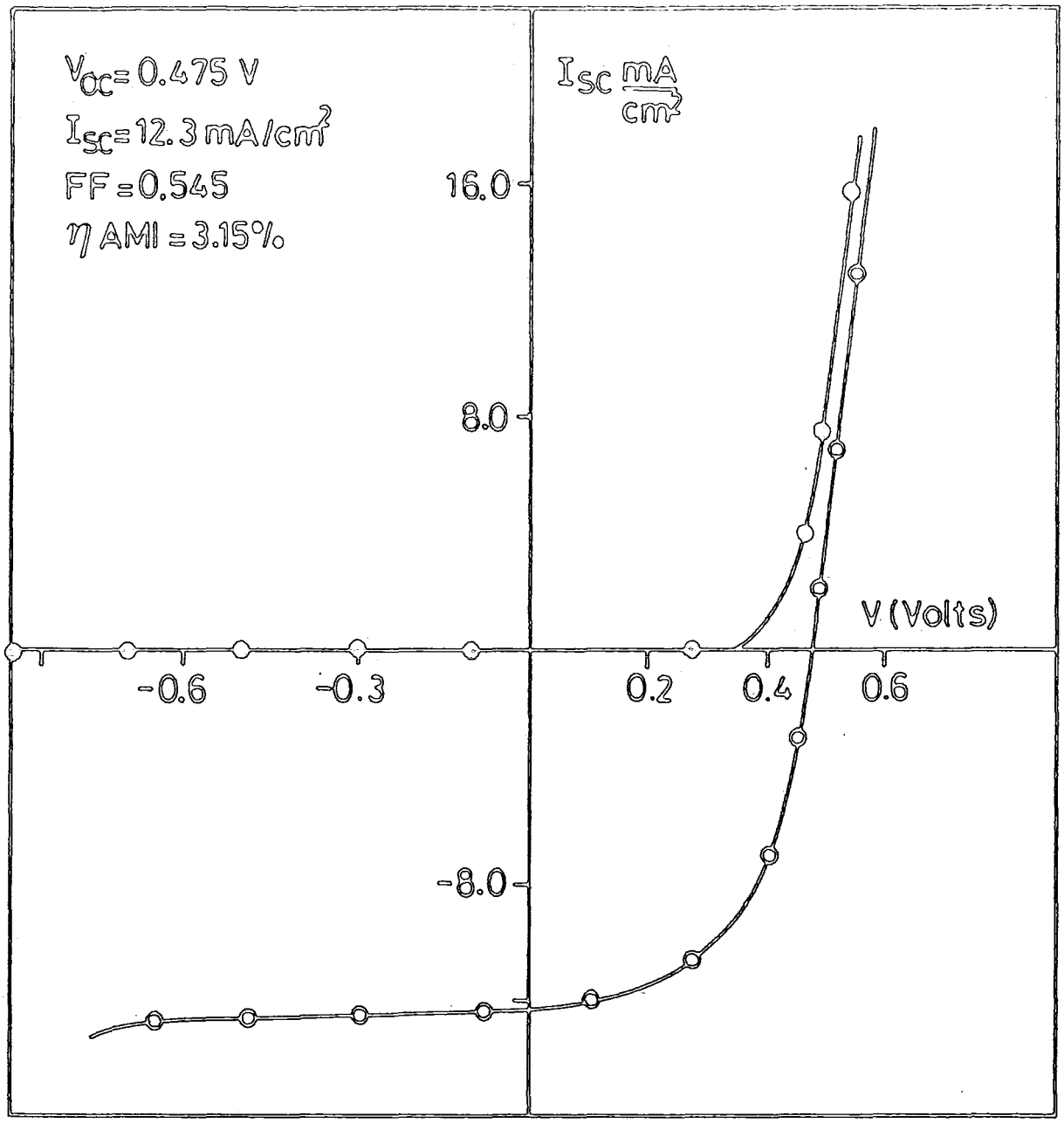

Fig 5.11

Current-voltage characteristics measured in the dark and under AM1 illumination for as-made device prepared by the electroplating technique under the optimum bias.

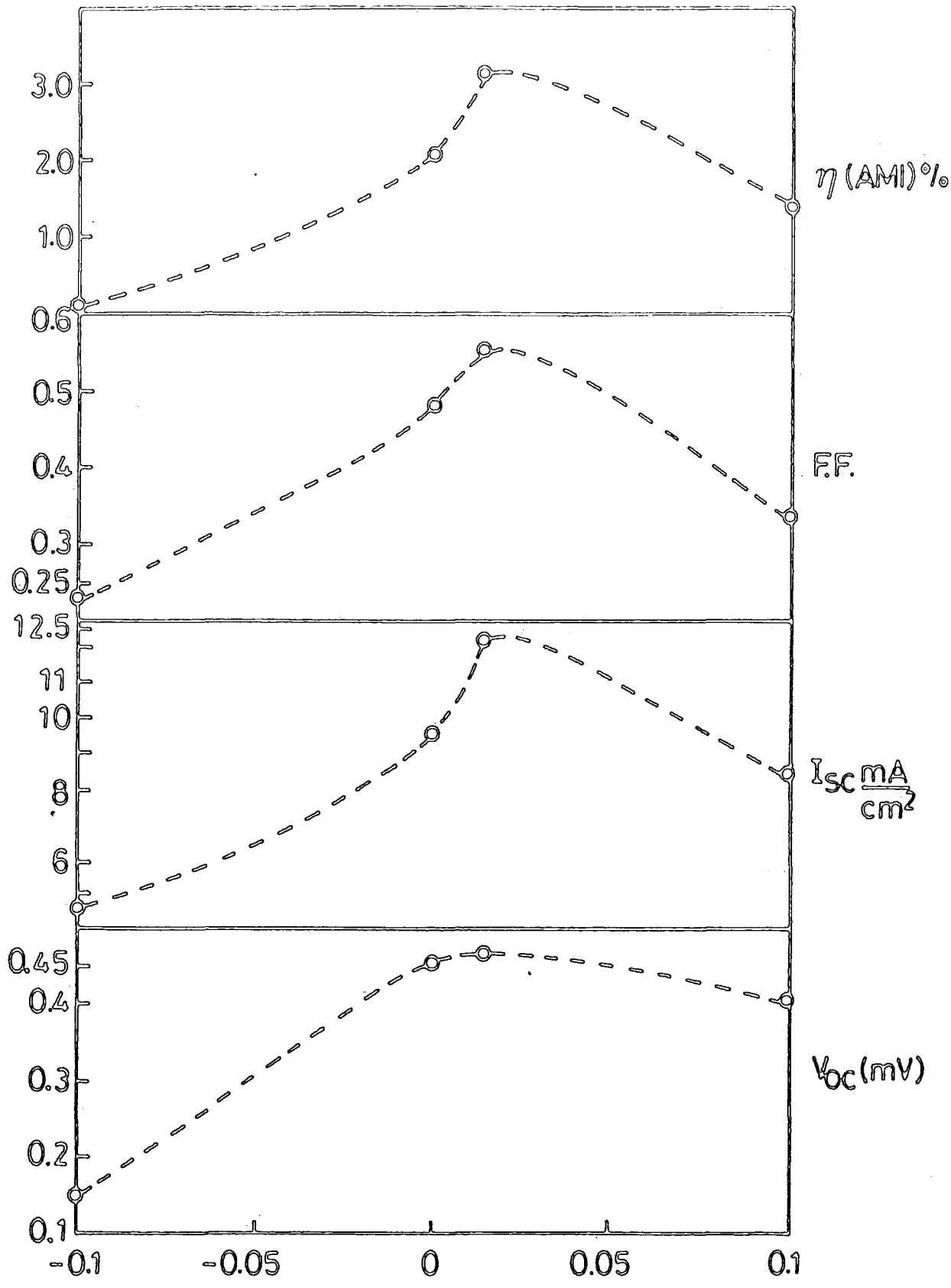

Fig 5.12

Variation of cell parameters with applied voltage during electroplating for as-made devices.

do for corresponding changes to positive bias.

5.4.2 Spectral Response

The spectral response of a photovoltaic cell provides a great deal of information about its operation. A correlation between the spectral response of both V_{oc} and I_{sc} and the phase of copper sulphide has been established [8,18,19]. Consequently the spectral responses of all devices have been measured to investigate the effect of the applied voltage during heterojunction growth on the phase of Cu_xS present. In addition to corroborating the RHEED evaluation of the phase of Cu_xS present at the top surface of the device, these measurements provide information regarding the heterojunction interface such as the presence of Cu levels in the CdS [38-42] caused by cross-diffusion. The shape of V_{oc} and I_{sc} spectral responses for devices made using the optimum electroplating bias voltage are shown in Fig 5.13 and 5.14 respectively. RHEED examination of this device indicated the presence of the chalcocite phase alone. While the spectral distribution of V_{oc} and I_{sc} at both temperatures show a dominant peak at a wavelength of $\sim$0.96 μm corresponding to the absorption of light across the indirect bandgap of chalcocite [20], the responses also exhibit a small shoulder lying at about 0.75 μm which can be attributed to a transition across the direct bandgap of djurleite [21]. For both V_{oc} and I_{sc} there was no change in the shape of the response when the temperature was reduced to liquid nitrogen temperature (85K) but generally the magnitude of the overall response was increased. Fig 5.15 and 5.16 show the spectral distribution at 295K and 85K respectively of the V_{oc} of cells for these different plating voltages used in the formation of the Cu_xS layer. Only the responses of these cells which gave reasonable diode behaviour in the as-prepared condition are shown in these figures. The responses

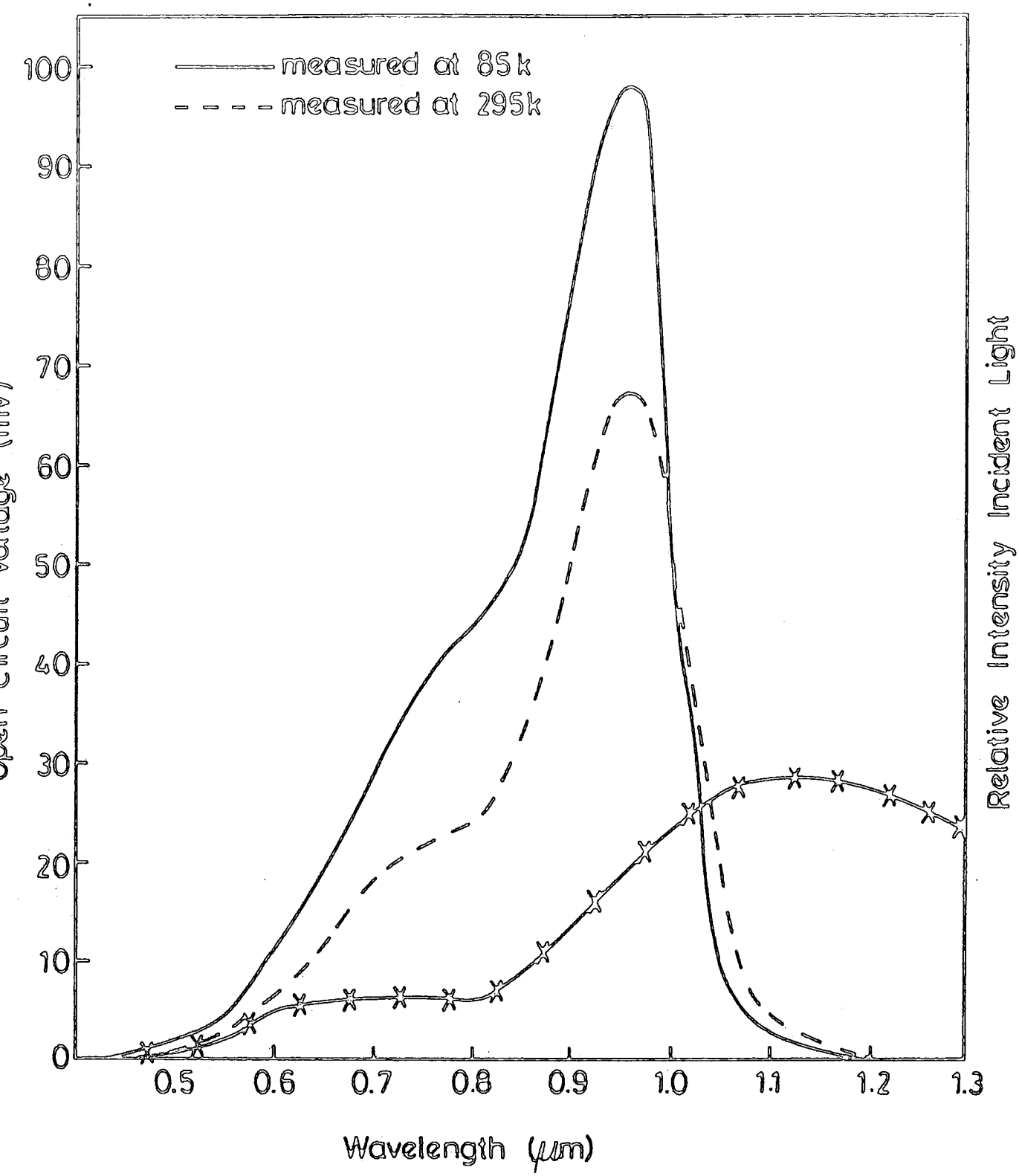

Fig 5.13

V_{oc} spectral response of as-made CdS-Cu_2S heterojunction formed at optimum electroplating bias.

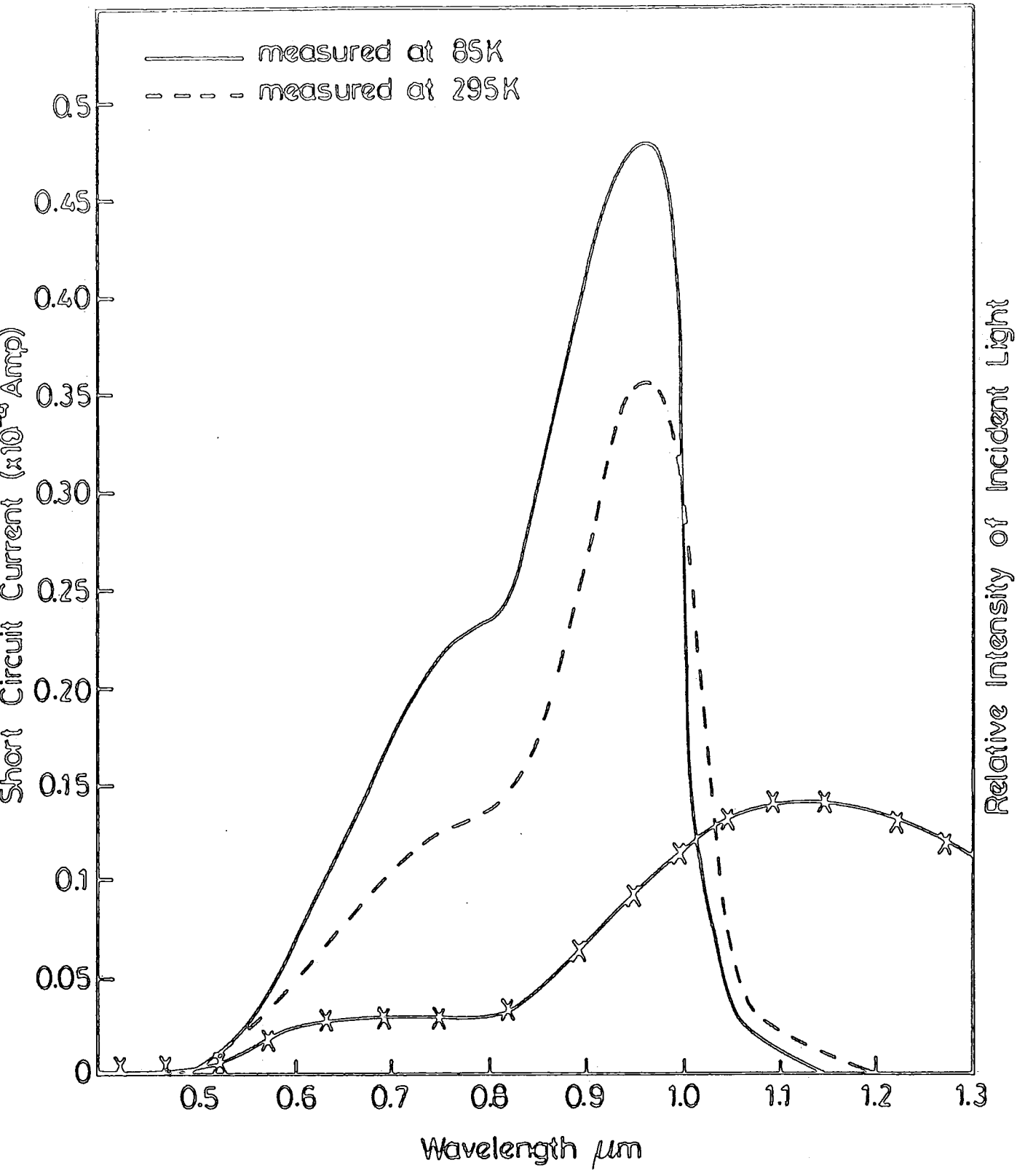

Fig 5.14

I_{sc} spectral response of as-made CdS-Cu_2S heterojunction formed at optimum electroplating bias.

show that for both temperatures of measurement the chalcocite phase is dominant for devices formed at all three values of bias, while there is an additional response due to djurleite, and the relative magnitude of this progressively increases as the plating bias used for device formation is changed from 0.01 to 0 to 0.1V. This trend became more obvious when the temperature of measurement was reduced to 85K. At both temperatures it is clear that the response of the device made at +0.01V has a maximum peak at a wavelength of 0.96 μm and small shoulder at 0.75 μm. Earlier work in this laboratory [11,12] has demonstrated that peaks at 0.96 and 0.75 μm correspond to the chalcocite and djurleite phases of Cu_xS respectively.

5.5 RHEED Study After Heat Treatment In A Different Ambient

In the study of the effect of post fabrication heat treatment on cells prepared at different values of plating bias, RHEED has been employed to investigate the phase of Cu_xS at the outermost surface of devices. In most cases and particularly when the treatment was conducted in air, these investigations were not particularly conclusive largely because, for reasons unknown, the diffraction patterns were invariably less clear after heat treatment than they were before. However, one interesting observation was made after heating in an argon ambient and that concerned a device with the djurleite phase in the as-made condition (see Fig 5.7). When this was heated for 5 minutes in argon, the phase was observed to change to chalcocite (see Fig 5.17).

5.6 Properties of CdS-Cu_xS Solar Cells After Heat Treatment In Air Or In Argon

5.6.1 Current Voltage - Characteristics

While only those Cu_xS layers produced at a plating bias of +0.01,

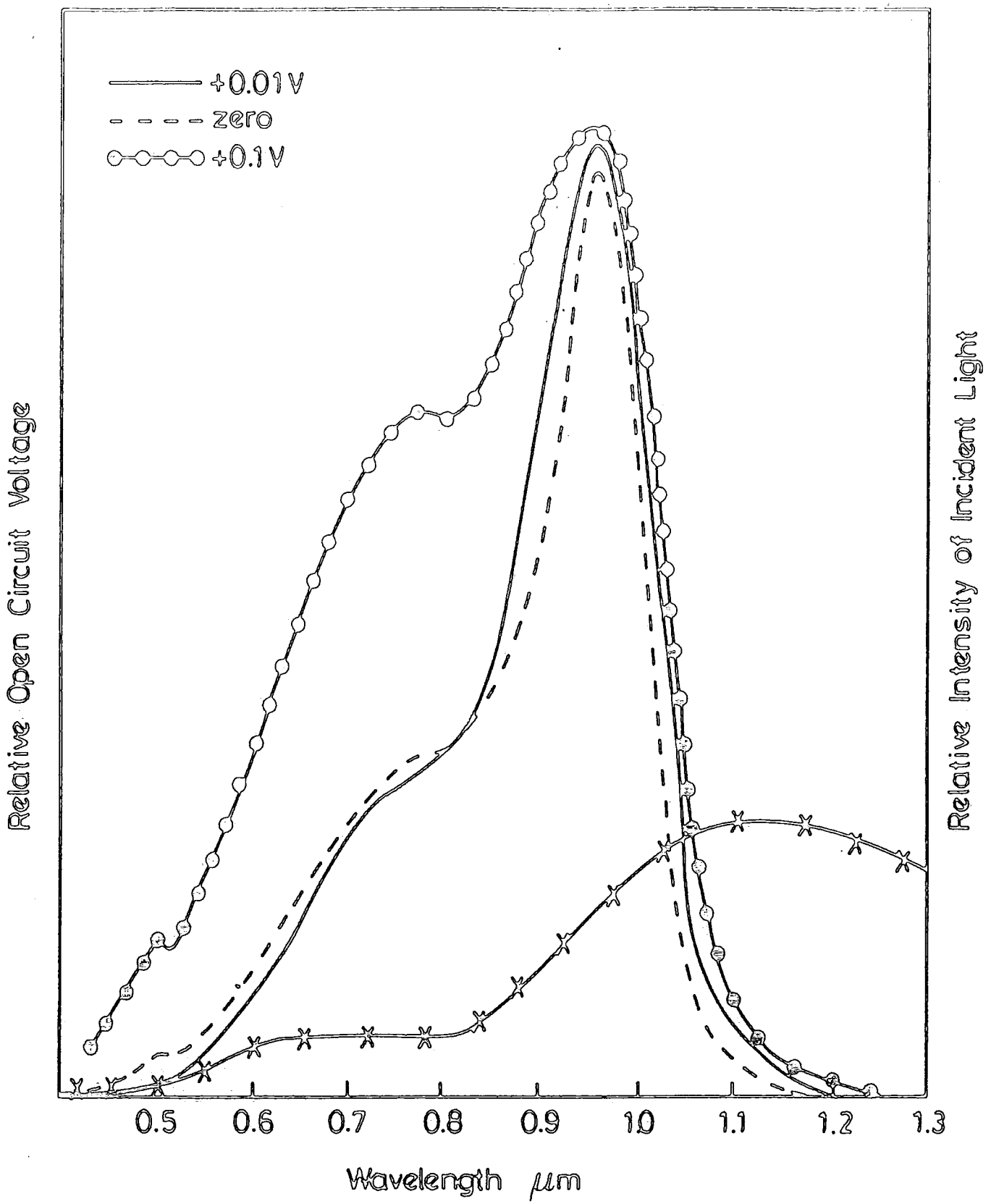

Fig 5.15

Spectral response of V_{oc} at 295 K for as-prepared devices as a function of electroplating bias.

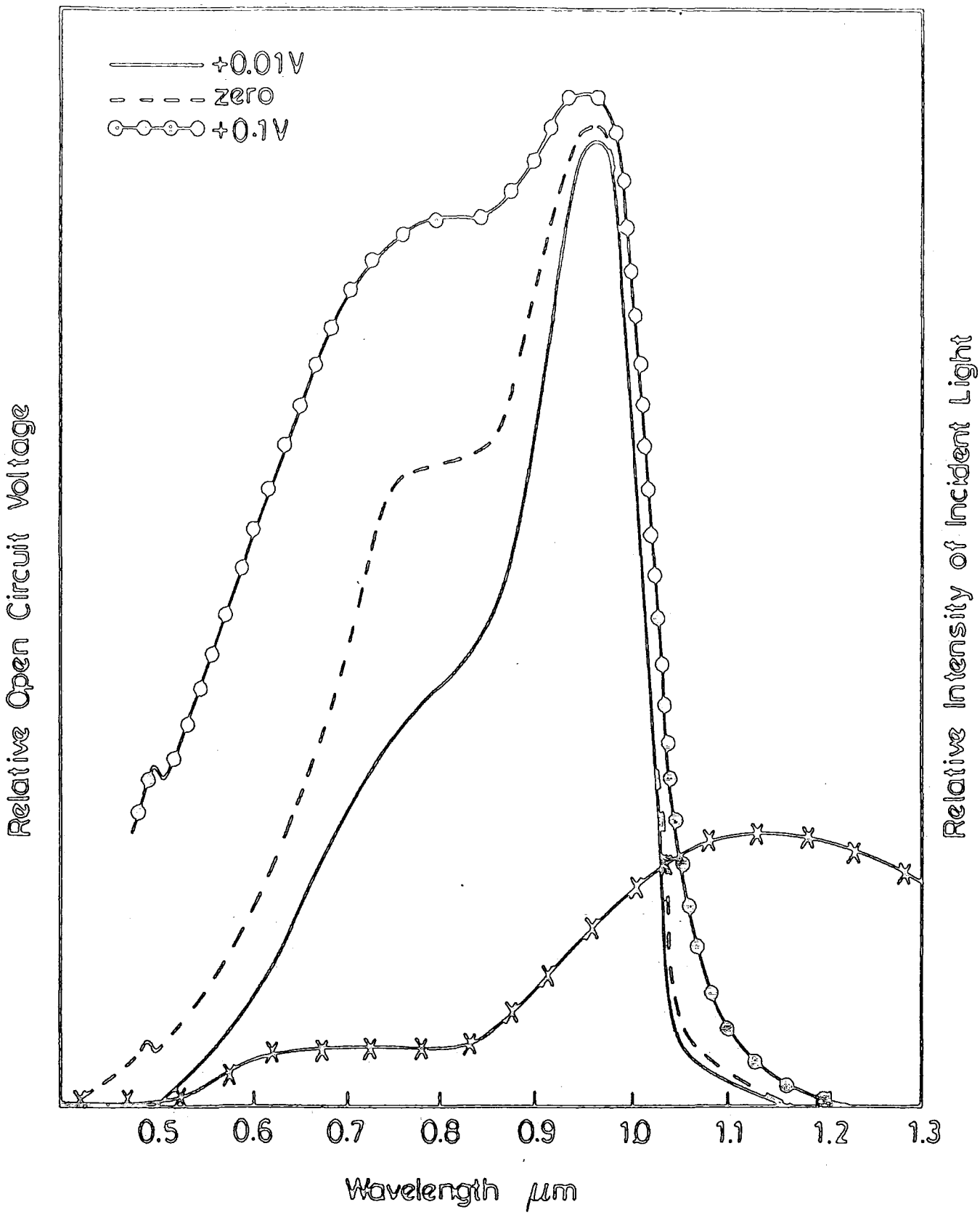

Fig 5.16

Spectral response of V_{oc} at 85 K for as-prepared devices as a function of electroplating bias.

Fig 5.17 RHEED patterns of a djurleite phase after 5 minutes heated in argon at 200°C.

zero and +0.1V gave rise to devices which showed rectifying behaviour in the as-made condition, layers produced at other values of plating bias led to the formation of some sort of photovoltaic cell following a post-fabrication heat treatment. For instance, the covellite phase which was formed by using a bias of +3.0V during heterojunction formation gave rise to a straight line I-V characteristic in the as-prepared condition. However, a post-fabrication heat treatment led to rectifying behaviour. The effects of heat treatments carried out for different periods of time in argon and in air are shown in Figs 5.18 and 5.19 respectively. After 10 minutes of heating in argon at 200°C a hard characteristic was obtained yielding device parameters of V_{oc} = 0.24V, I_{sc} of 2.3 $mA.cm^{-2}$, FF of 0.49 and efficiency of 0.27%. In contrast, devices heated in the same conditions but in air instead of argon exhibited inferior parameters with a V_{oc} of 0.14V, an I_{sc} of 1.4 $mA.cm^{-2}$ a FF of 0.245 and an efficiency of 0.05%. These parameters are listed in table 5.3 a and b.

length of heating min	OCV (V)	SCC $\frac{mA}{cm^2}$	FF	γ%
0	0	0	0	0
5 min	0.16	1.4	0.27	0.06
10 min	0.24	2.3	0.49	0.27
15 min	0.21	1.8	0.48	0.182

Table 5.3a Variation of cell parameters of a CdS-CuS device with duration of heat treatment at 200°C in argon

length of heating	OCV (V)	SCC $\frac{mA}{cm^2}$	FF	γ%
0	0	0	0	0
5 min	0.10	0.95	0.315	0.03
10 min	0.14	1.40	0.245	0.05
15 min	0.14	1.30	0.35	0.064

Table 5.3b Variation of cell parameters of a CdS-CuS device with duration of heat treatment at 200°C in air.

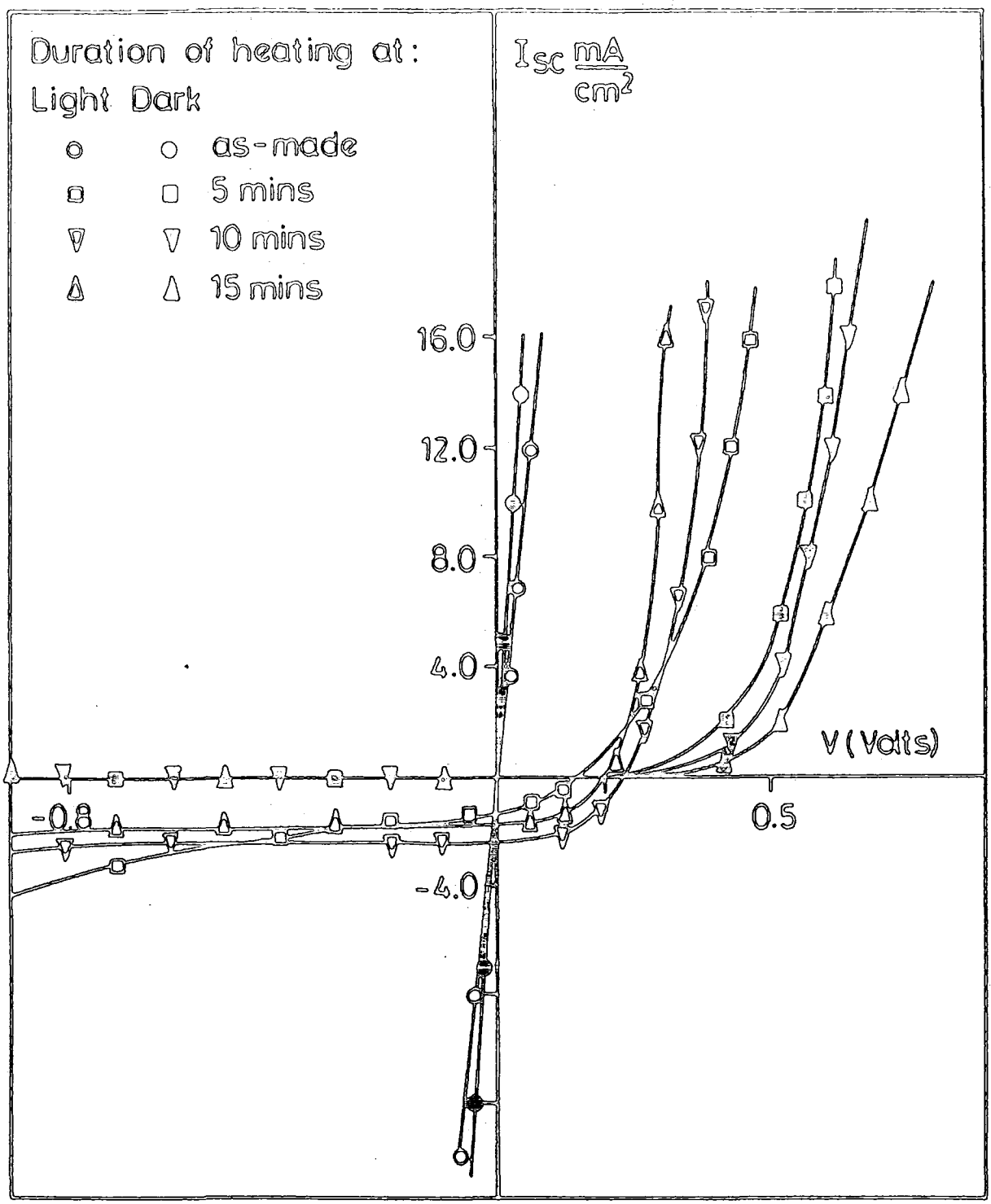

Fig 5.18

Current-Voltage characteristics measured at dark and under AM1 illumination for CuS-CdS (covellite) as a function of Argon heat treatment.

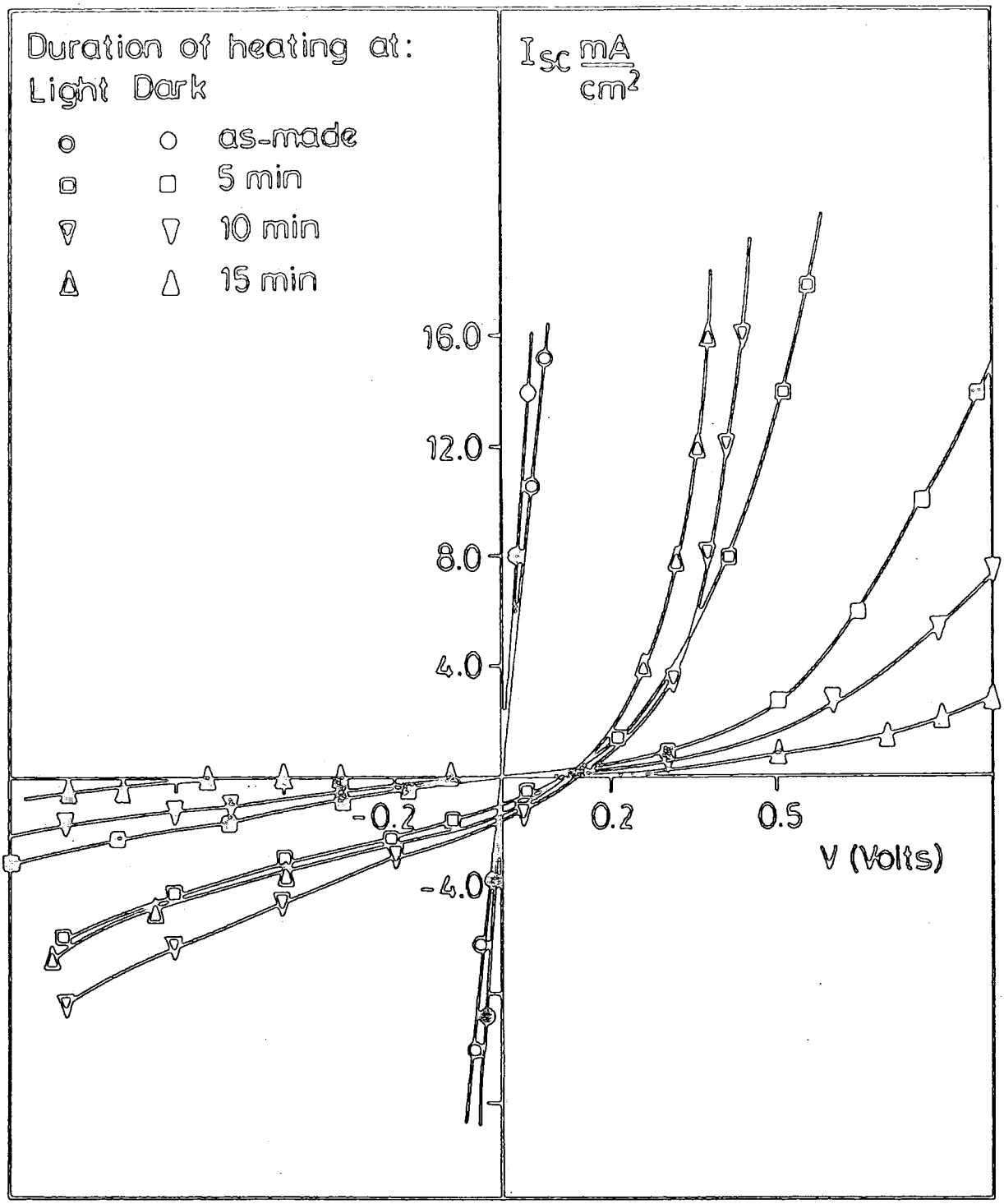

Fig 5.19

Current-Voltage characteristic measured in the dark and under AM1 illumination for CuS-CdS (covellite) as a function of Air Heat treatment at 200°C.

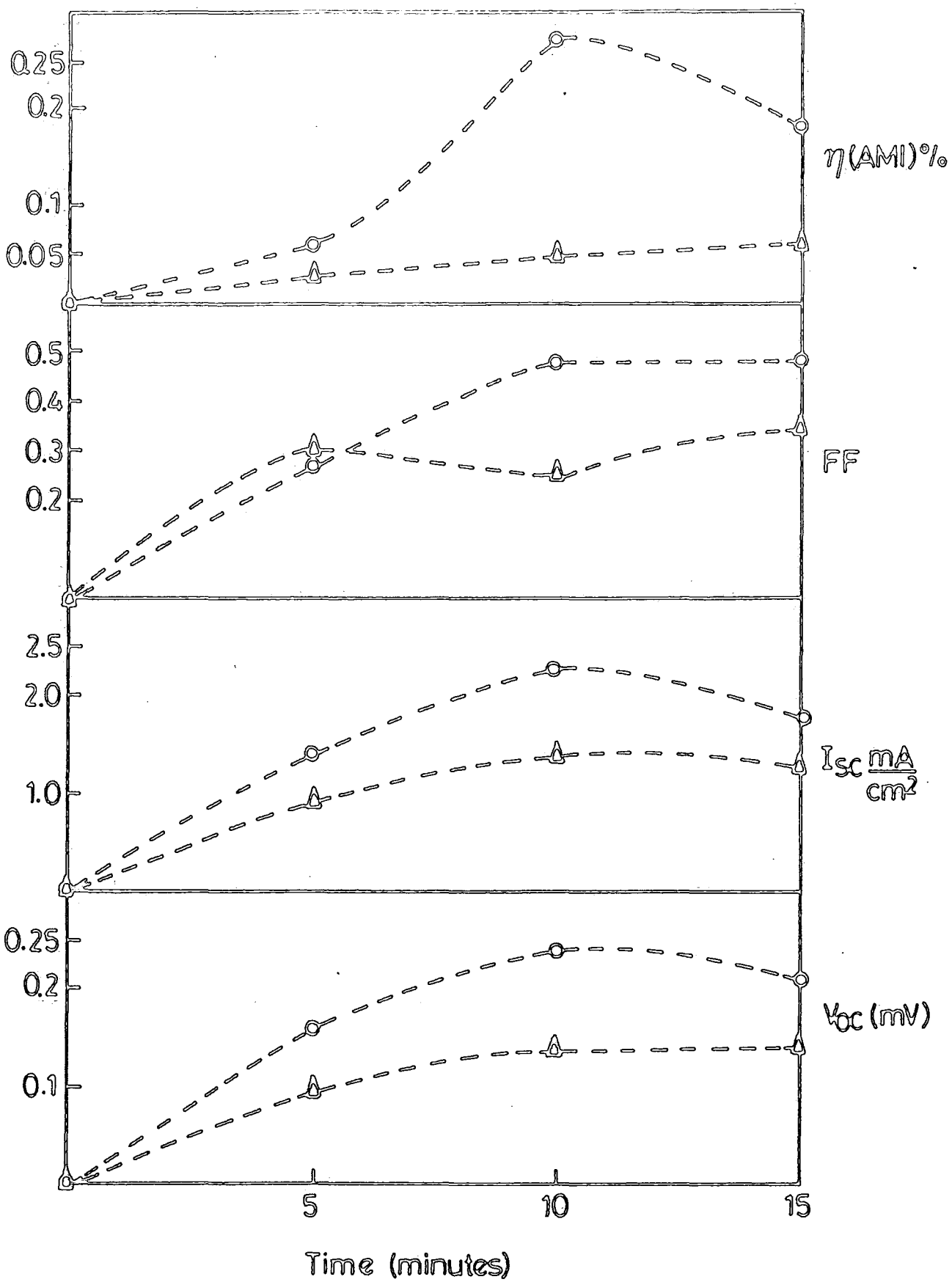

Fig 5.20

Variation of effective parameters for CdS-CuS (covellite) with heat treatment in O Argon and Δ Air.

Fig 5.20 compares the influence of a post fabrication heat treatment in argon with that in air for different periods of time on CdS-CuS cell parameters. Inspection shows that 10 minutes is the optimum period for heating in argon, while 15 minutes is the optimum for heating in air. There was a progressive increase in FF as the duration of heating was increased. Also Fig 5.20 shows that the improvement of the parameters associated with argon heat treatment was much greater than that associated with air heating.

The effects of a 5 minute heat treatment conducted separately in argon and in air at 200°C for devices prepared at -0.1V, +0.1V, zero and +0.01V are shown in Figs 5.21, 5.22, 5.23 and 5.24 respectively. Fig 5.21 which corresponds to a device carrying the djurleite phase of Cu_xS shows that a poor characteristic was obtained with as-made cells which gave values for V_{oc} of 0.15V and I_{sc} of 4.6 $mA.cm^{-2}$ and a FF of 0.23. These parameters were improved by a heat treatment for a few minutes. Heating in air at 200°C for 5 minutes gave rise to a hard characteristic with the value of V_{oc} increasing to 0.37V, I_{sc} to 7.4 $mA.cm^{-2}$ and the FF to 0.51. In contrast, heating a cell in the same conditions but in argon rather than in air, led to less improvement with V_{oc}, I_{sc} and FF only increasing to 0.38V, 5.8$mA.cm^{-2}$ and 0.39 respectively.

Some typical I-V characteristics of cells prepared with +0.1V bias and measured in the as-made condition and after heat treatment for 5 minutes at 200°C in air and in argon, are shown in Fig 5.22. For these cells the V_{oc} was improved from 0.41V to 0.45V and to 0.46V by using air and argon respectively. Simultaneously I_{sc} increased from 8.4 $mA.cm^{-2}$ to 9.6 $mA.cm^{-2}$ by employing air, but it remained unchanged after the argon heat treatment.

When a good device fabricated with zero bias Fig 5.23, was heated either in argon or in air for 5 minutes, the V_{oc} showed only a very small

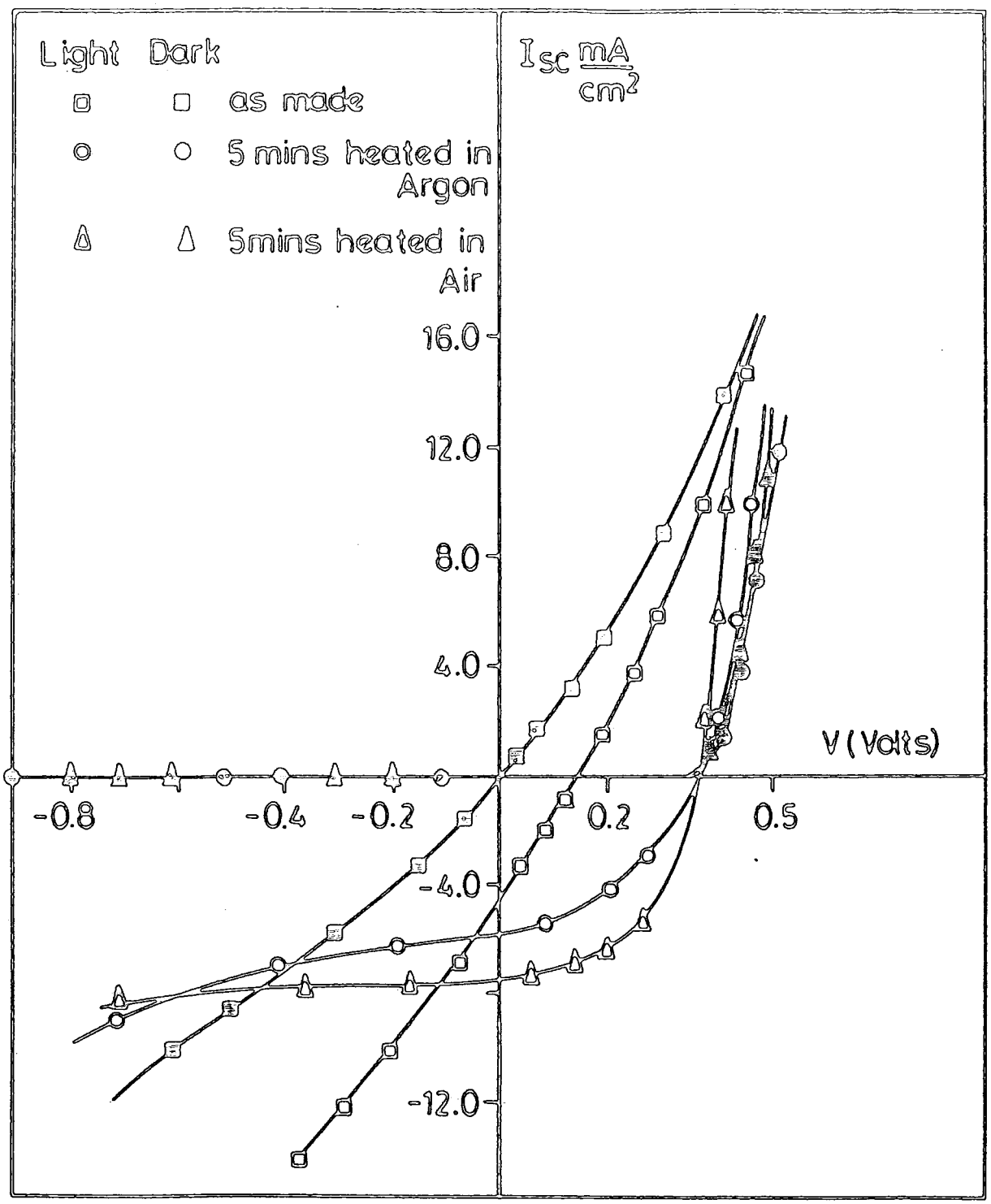

Fig 5.21

Current-Voltage characteristics measured in the dark and under AM1 illumination for a device prepared at -0.1V after heated in Air and in Argon at 200°C.

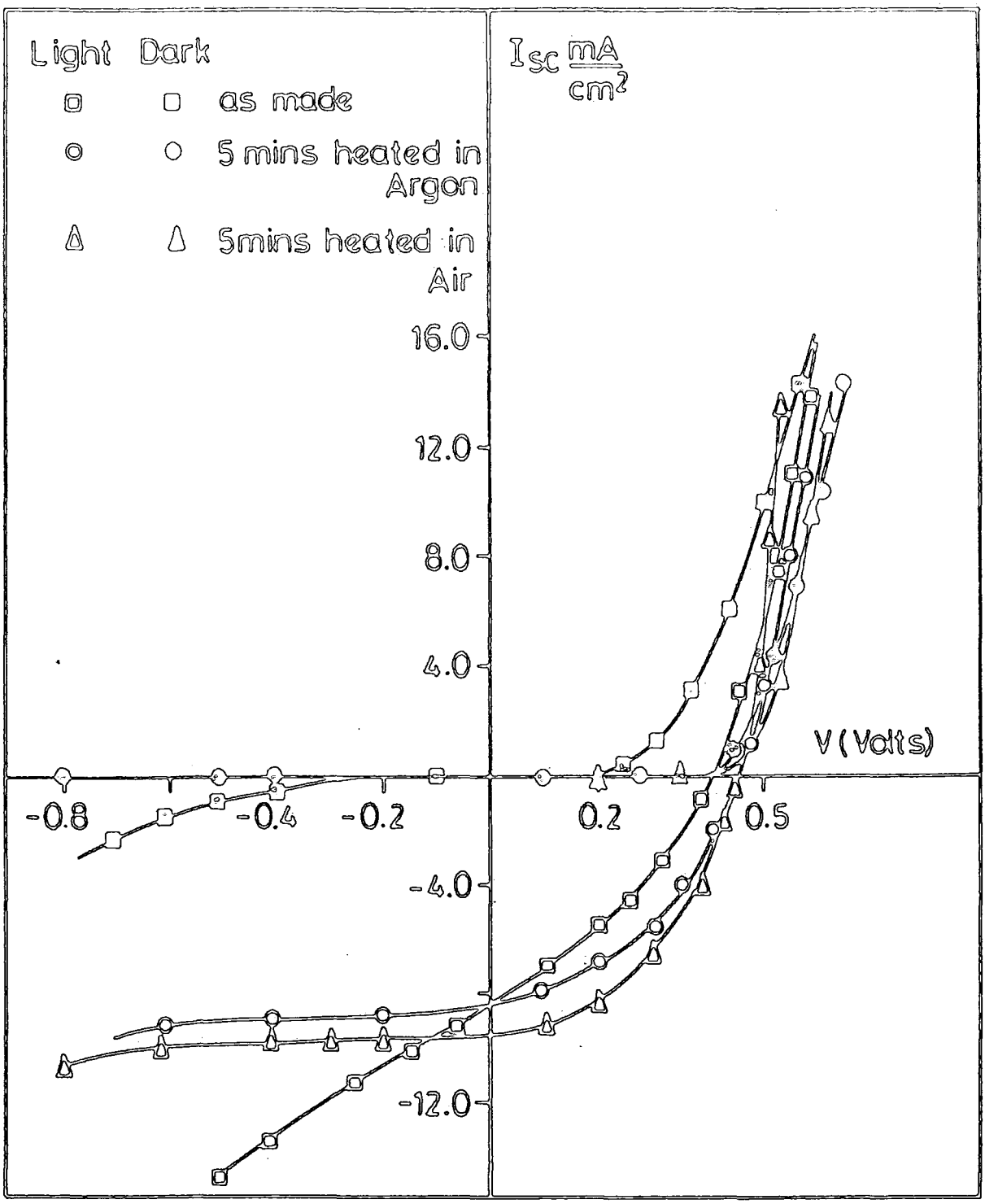

Fig 5.22

Current-Voltage characteristics measured in the dark and under AM1 illumination for a device prepared at +0.1V after 5 minutes heated in Air and in Argon at 200°C.

increase but a considerable reduction in I_{sc}. Further, the heating of a device with a hard characteristic, which indicates the presence of the chalcocite phase (Fig 5.24), whether in argon or in air, leads to a reduction in the efficiency. These results are summarized in Table 5.4.

bias (V)	OCV (V)	SCC $mA.cm^{-2}$	FF	γ%
+0.1	0.46	8.4	0.42	1.62
+0.01	0.49	3.0	0.55	0.80
zero	0.49	6.3	0.39	1.2
-0.1	0.38	5.8	0.39	0.86

5.4a

bias (V)	OCV (V)	SCC $mA.cm^{-2}$	FF	γ%
+0.1	0.45	9.6	0.445	1.92
+0.01	0.47	4.3	0.50	1.01
zero	0.46	7.9	0.405	1.47
-0.1	0.37	7.4	0.51	1.32

5.4b

TABLE 5.4 : Comparison of the effects on device parameters of heat treatments at 200°C for 5 minutes in a: argon b: air.

5.6.2 Spectral Response

While the spectral response of heterojunctions formed using a plating potential of +3.0V could clearly not be measured in their as-made state due to the absence of a barrier, after a heat treatment these devices gave rise to rectification (see Fig 5.18 and 5.19) so it was then possible to measure their spectral response. Figs 5.25 and 5.26 show the spectral response of V_{oc} at room temperature for CdS-CuS cells heated for 5, 10 and 15 minutes at 200°C in argon and in air respectively. Heating in air produces (i) a dominant narrow

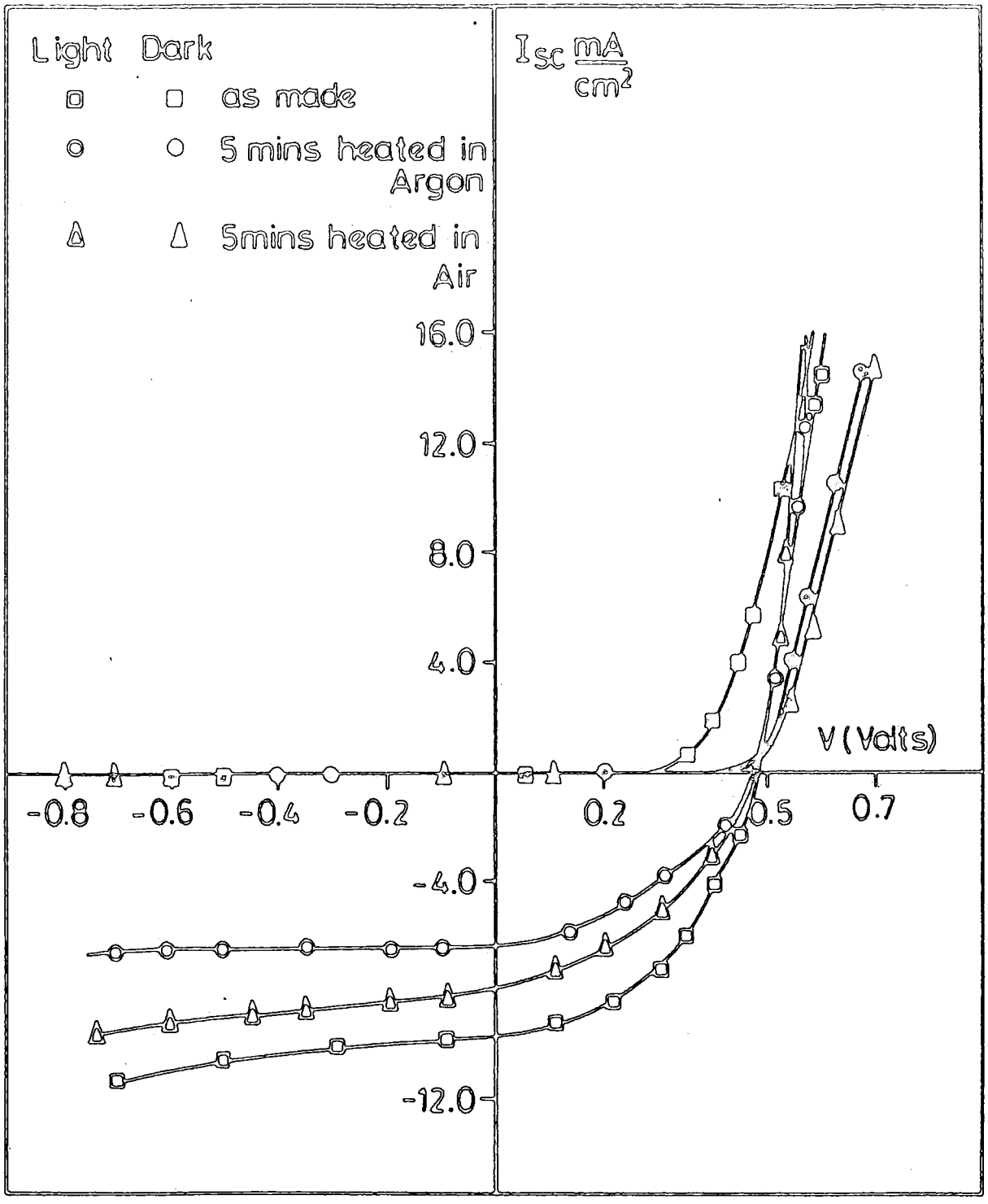

Fig 5.23

Current-Voltage characteristics measured in the dark and under AM1 illumination for a device prepared at zero bias after 5 minutes heated in Air and in Argon at 200°C.

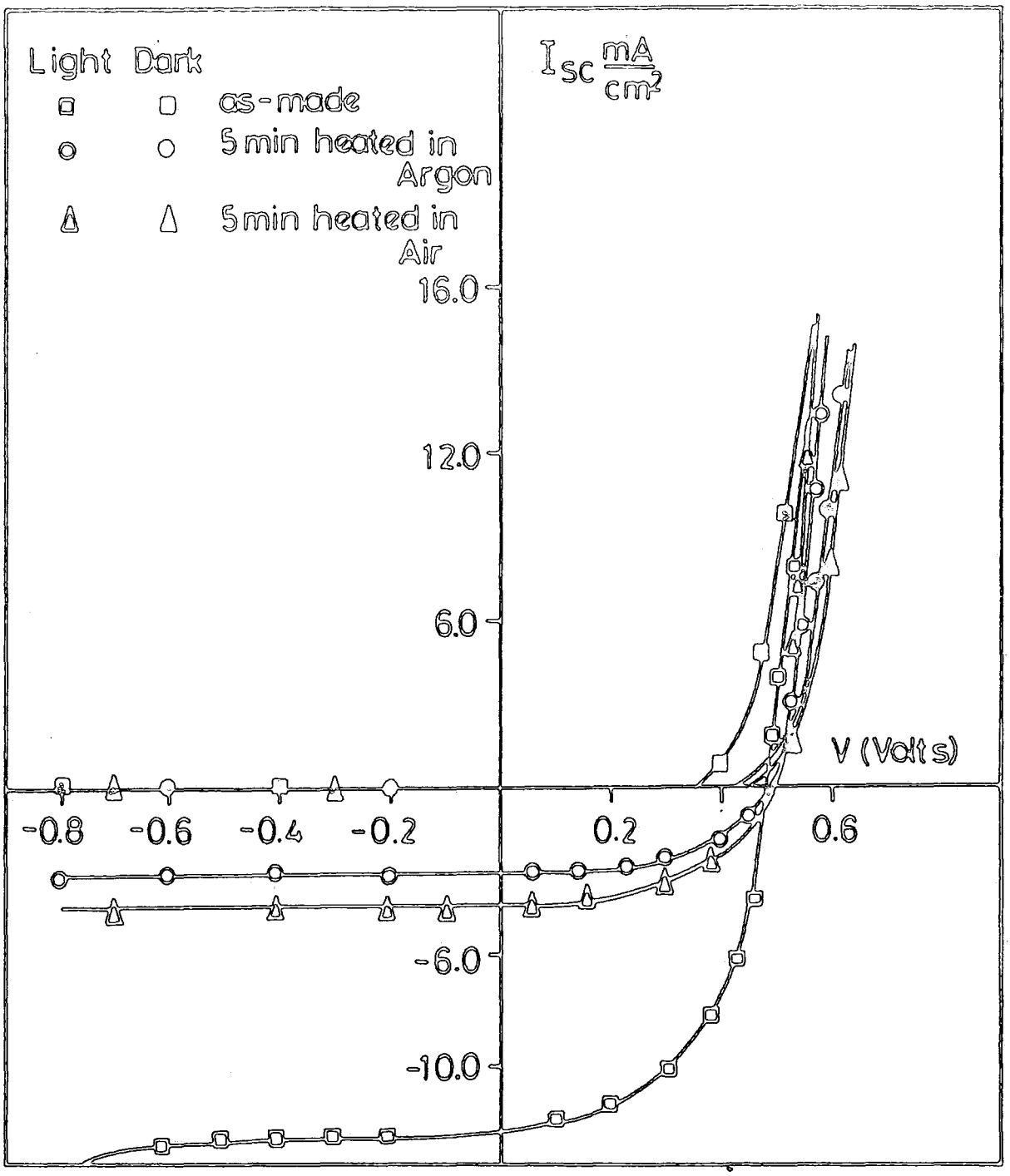

Fig 5.24

Current-Voltage characteristics measured in the dark and under AM1 illumination for a device prepared at +0.01V after 5 minutes heated in Argon and in the air at 200°C.

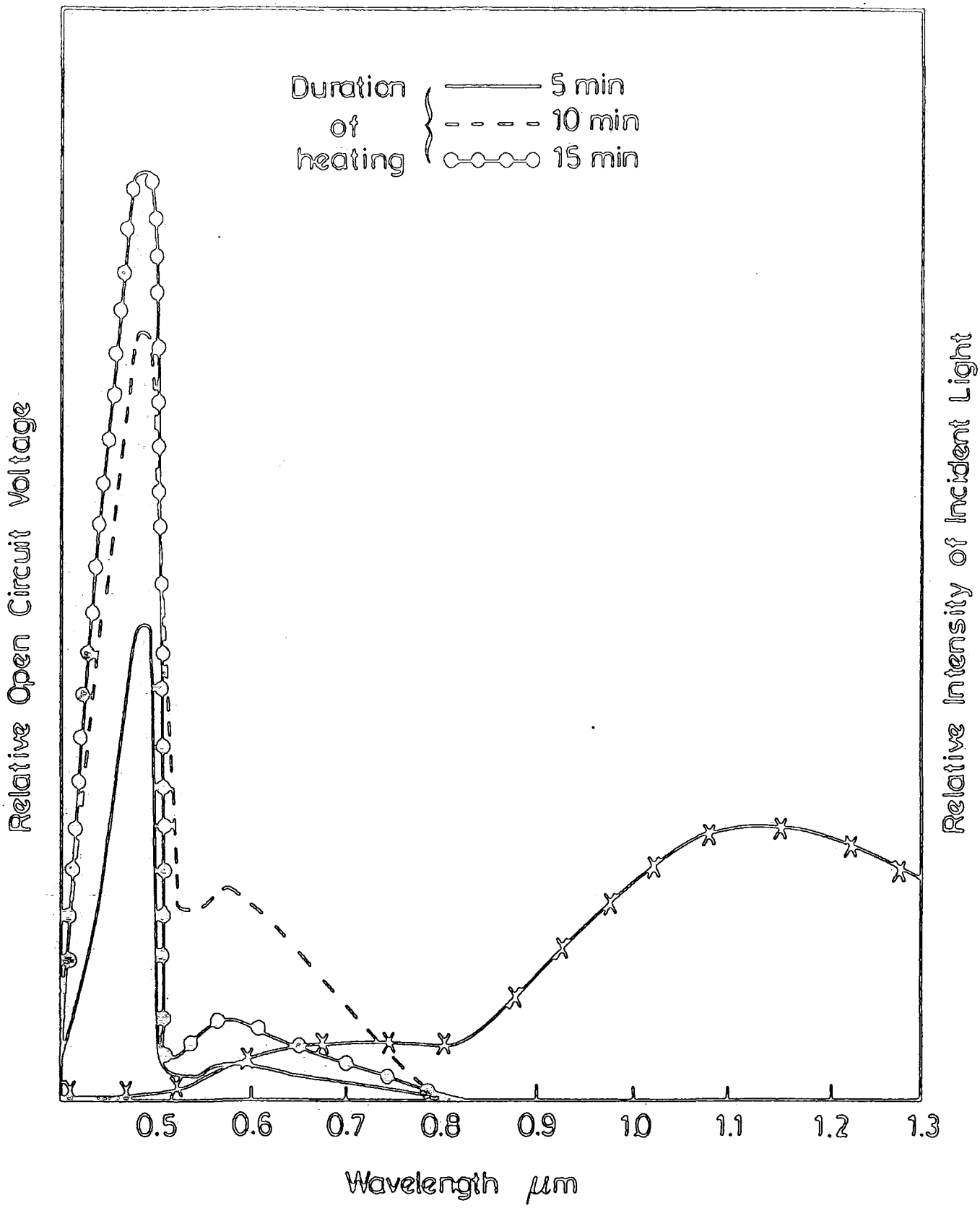

Fig 5.25

The effect of Argon heat treatment on the spectral response of CdS-CuS heterojunction measured at 295 K.

peak at a wavelength of 0.49 μm which is attributable to the response from the bandgap of CdS and (ii) a relatively small peak at a wavelength of about 0.60 μm which is due to a transition in CuS [5]. Also this response might be enhanced by the response of copper level formed by the diffusion of copper into the CdS after heat treatment [11,23]. RHEED inspection demonstrates that the covellite phase was obtained in this device which was made with a bias of 3.0V during the growth of Cu_xS. Heat treatment in argon leads to a similar result but the response in the band at 0.60 μm is shifted to the shorter wavelength of 0.58 μm. By increasing the time of heating, the relative magnitudes of these two peaks were increased until the heating period exceeded 10 minutes (in argon) beyond which it was observed to decrease.

The spectral distribution of V_{oc} of these devices was also measured at 85 K and the results are shown in Figs 5.27 and 5.28 for devices treated in argon and air respectively. The interesting effects concern the differences between the spectral distribution measured at room temperature and at 85 °K, and also between the heat treatment in argon and in air for measurements at 85 K. Fig 5.27 shows three curves indicating how the spectral response changed as a function of duration of argon heat treatment. After 5 minutes heating there are three peaks lying at wavelengths of 0.96 μm, 0.58 μm and a dominant response at 0.49 μm. When the heating period was increased to 10 minutes, the peak which is located at 0.96 μm increased dramatically by factor of three times while the peak at 0.58 μm increased by factor of only two times and the peak at 0.49 μm decreased. Particularly interesting effects were obtained when the heating was extended to 15 minutes . This led to a dominant peak at a wavelength of 0.96 μm and the response became smaller in the bands at 0.70 μm and 0.49 μm. Also there was evidence of a small peak at about 0.6 μm. The appearance of the peak at 0.70μm

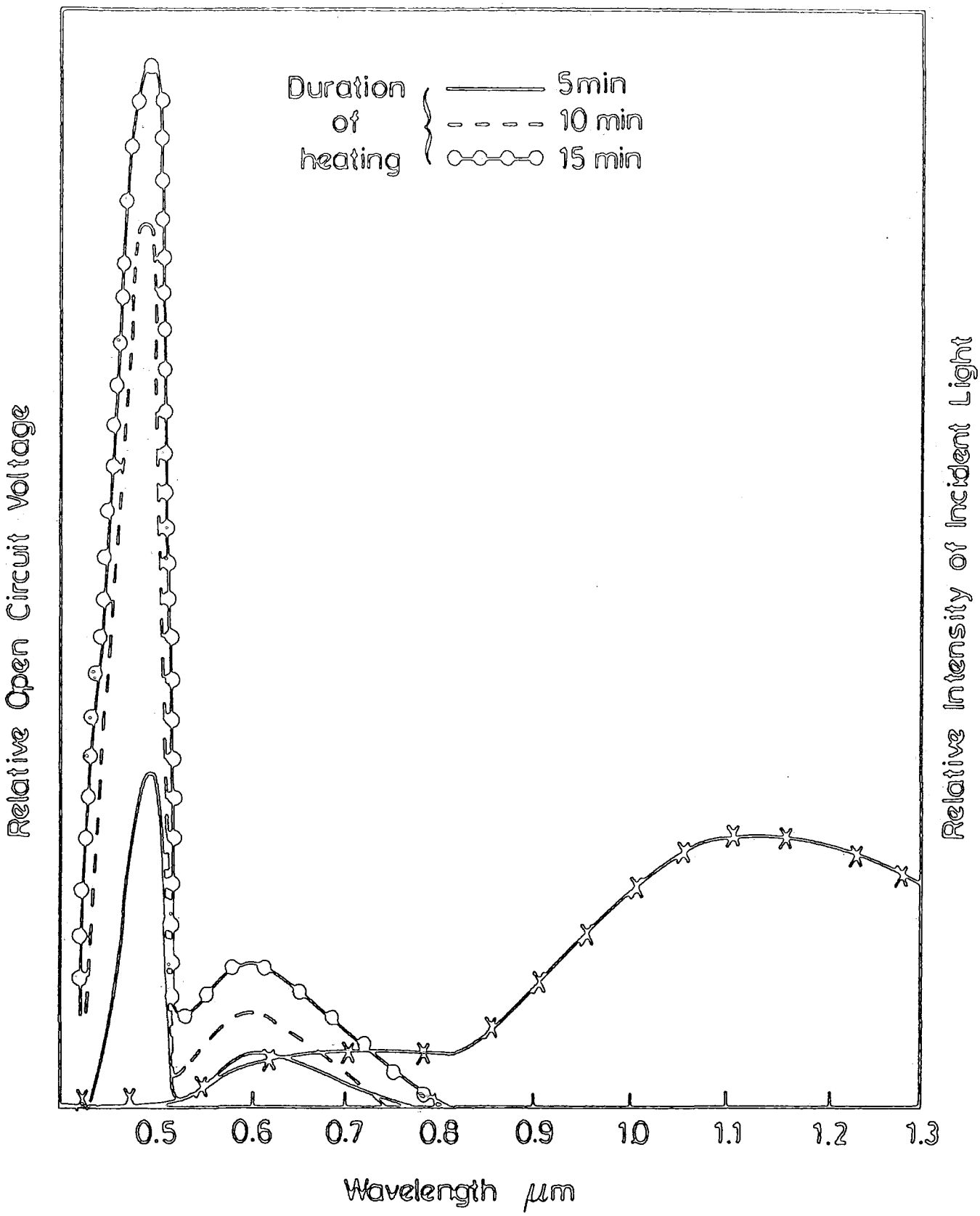

Fig 5.26

The effect of Air heat treatment on the spectral response of CuS-CdS heterojunction measured at 295 K.

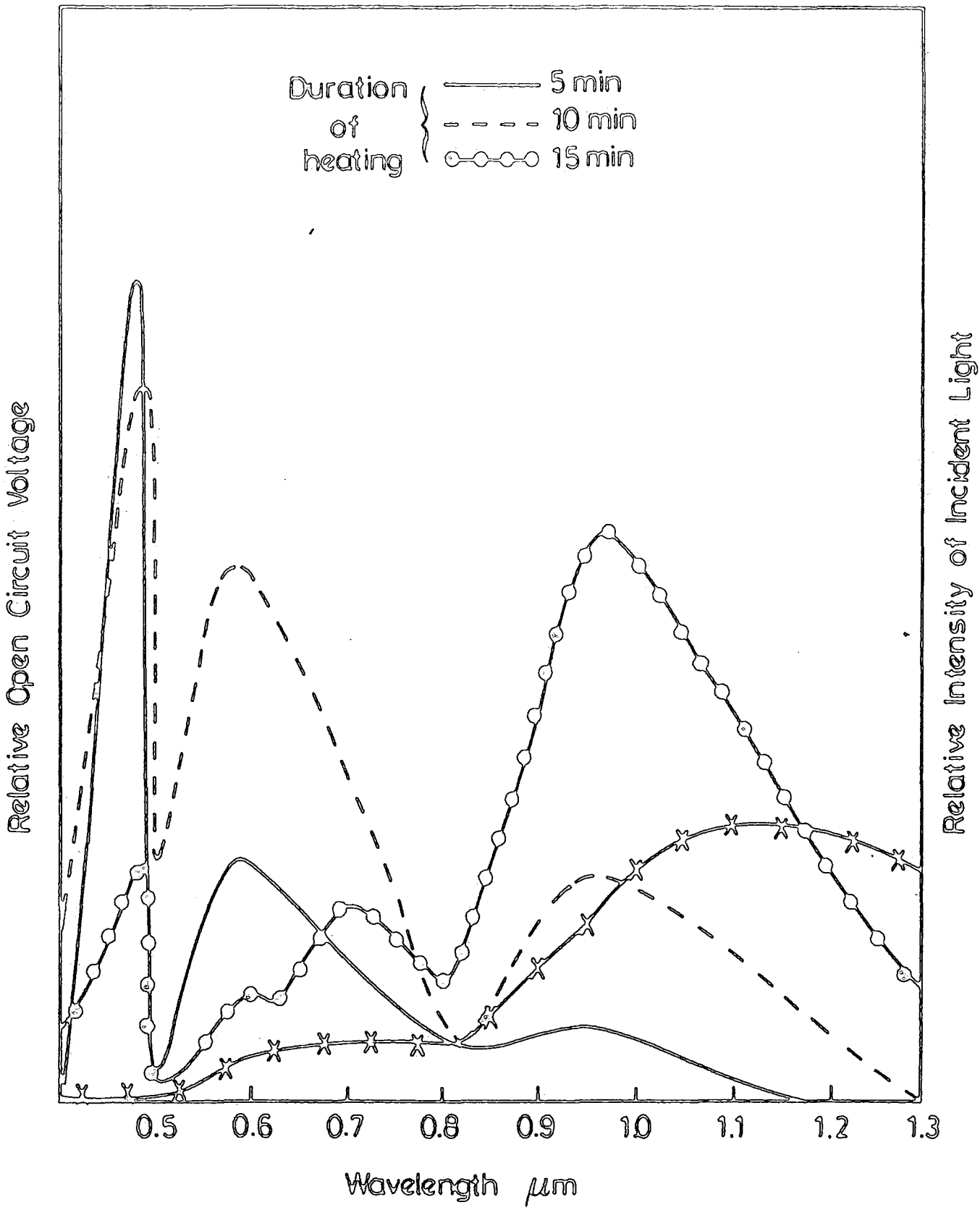

Fig 5.27

The effect of Argon heat treatment on the spectral response of CuS-CdS heterojunction measured at 85 K.

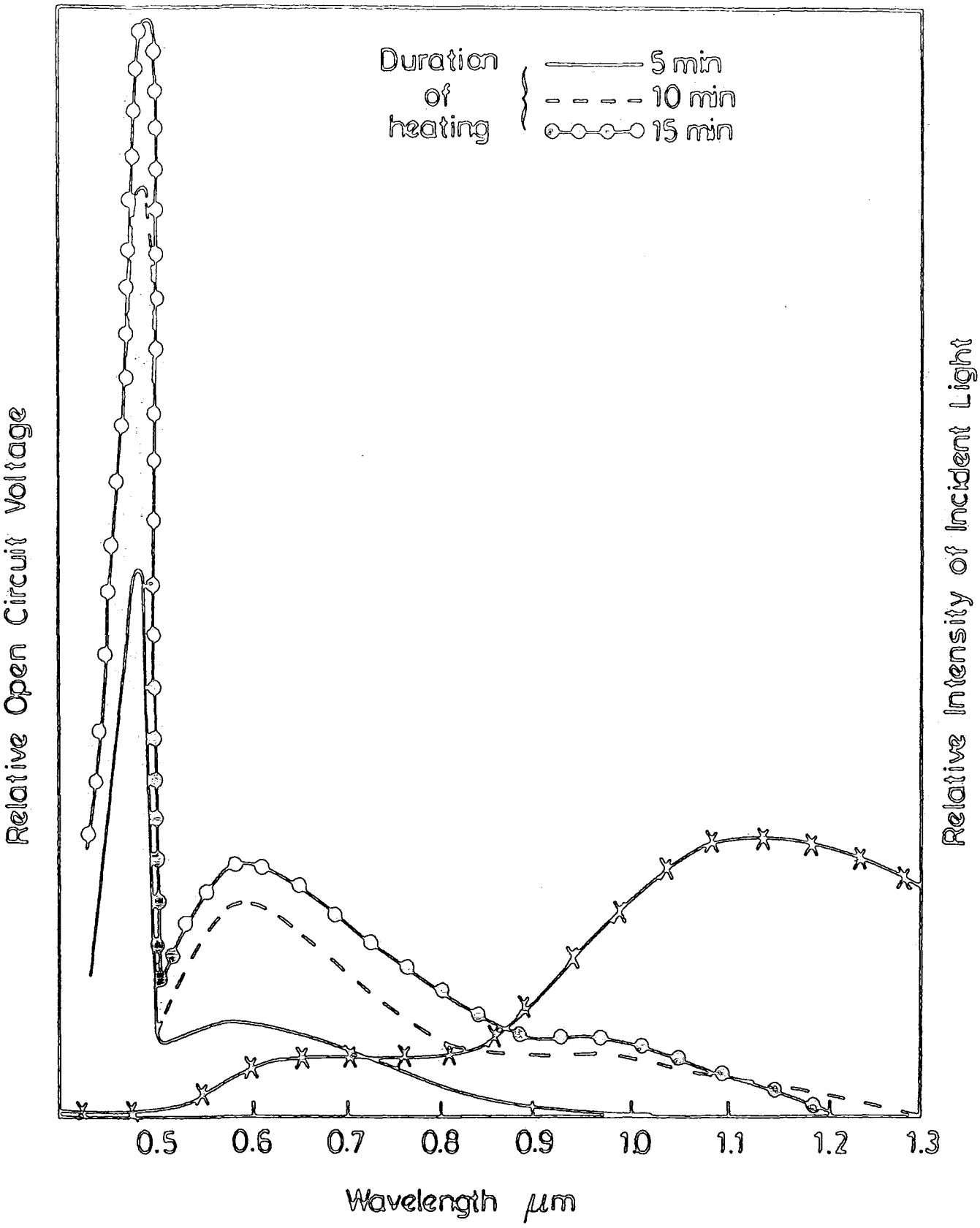

Fig 5.28

The effect of Air heat treatment on the spectral response of CuS-CdS device measured at 85 K.

is due to the formation of djurleite (so the response may come from this phase of copper sulphide) [21,22]. For the device heated under the same conditions but in air, the spectral response (measured at 85 K) as a function of the duration of heat treatment is shown in Fig 5.28. The curve for 5 minutes heating shows two bands at 0.60 μm and at 0.49 μm without a significant response beyond 0.8 μm. With heat treatment for 10 minutes and 15 minutes, the response of these two bands was increased and a very small peak appeared around 0.96 μm which indicated some response at this wavelength at least. RHEED examination after 15 minutes heating in argon and in air showed that there was no change in the structure and the phase was still covellite. However, the pattern was not as clear as that from an as-prepared device. Under these circumstances it is possible that the top surface is covellite as identified by RHEED, while the phase at the interface is chalcocite, especially considering that the information provided by the RHEED technique is confined to thin surface layers, because of the limited penetration of the electron beam (typically a few 100 Å).

In order to determine the effect of a heat treatment in argon relative to that in air on a mixture of chalcocite and djurleite phases, samples carrying such layers (as identified by RHEED) were heated for 2 and 5 minutes separately in argon and in air at 200°C. A spectral response of V_{oc}, typical of these devices, measured at room temperature before and after heat treatment in argon and in air is shown in Fig 5.29. For the as-made sample there are two peaks located at wavelengths of about 0.96 μm and 0.78 μm which indicate the presence of the chalcocite and djurleite phases. Also there is a small response in the region of the bandgap of CdS. While heating in argon leads to a relative decrease in the response of the band at about 0.78 μm (which causes this peak to be resolved more accurately at about 0.72 μm), the response

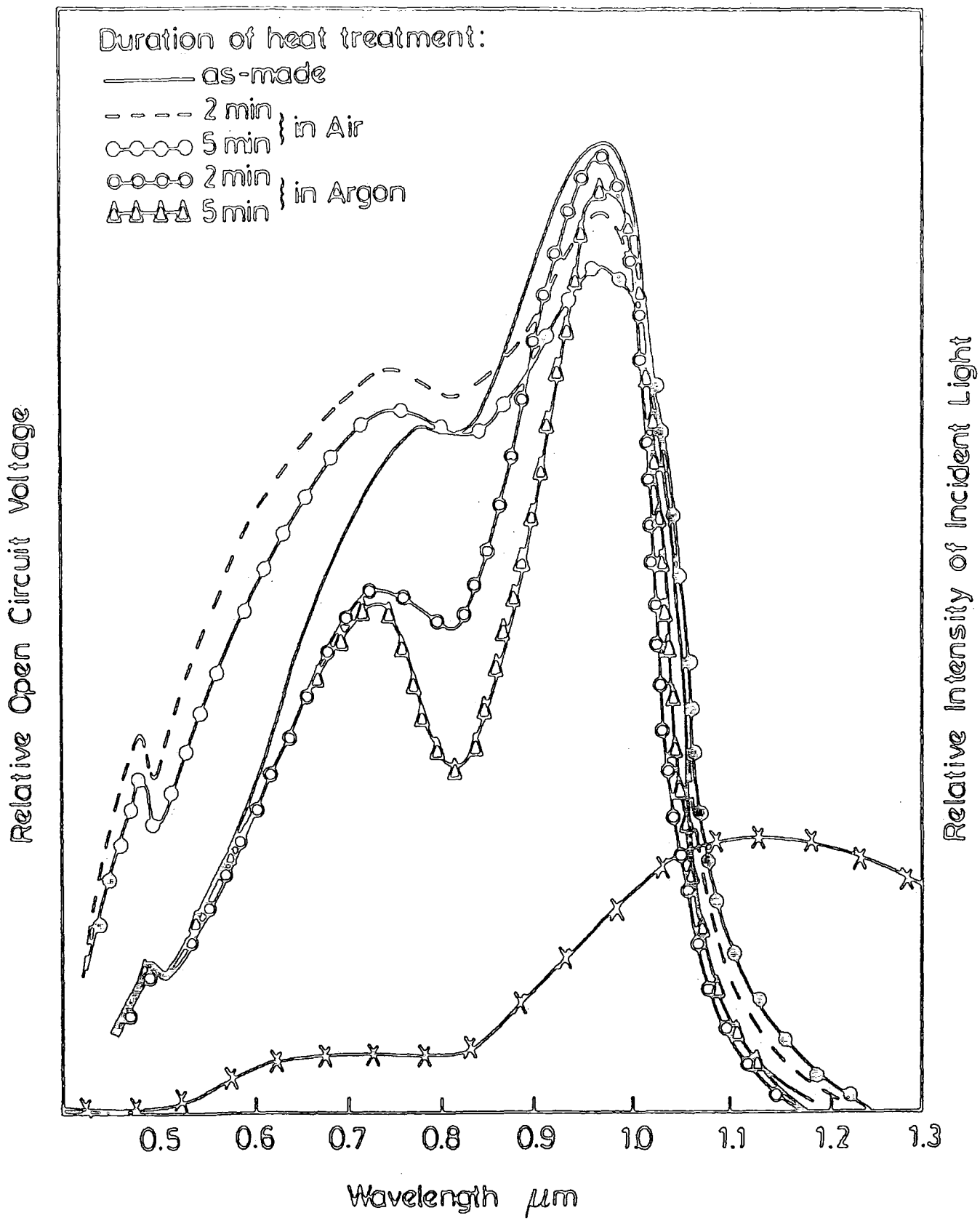

Fig 5.29

Spectral response of the open circuit voltage measured at 295 K of a device heated at 200°C in different ambients.

of the band at 0.49 μm is almost unchanged. In contrast, heating in air causes the peak at 0.78 μm to increase in magnitude relative to that at 0.96 μm. However, the former peak again exhibited an apparent shift to a slightly shorter wavelength. The magnitude of the response of the peak at 0.49 μm, due to the bandgap of CdS, also increased slightly with air heat treatment. In order to determine whether the response of the band in the range of 0.70 - 0.80 μm was due to the absorption of the light across the direct bandgap of djurleite [21] or to the optical absorption of the copper acceptor centres in an i-layer of CdS [11,23], the spectral responses of these cells were measured at 85 K (see Fig 5.30). At this temperature it is known that the effects associated with the copper centres are diminished [24]. This shows that when the device was heated for 5 minutes in air, the peak at wavelength of 0.72 μm was pronounced. On the other hand these two spectral peaks had almost the same magnitude. For the sample heated under the same condition but in argon, the spectral response shows that the response of the band at 0.96 μm increased while the response at wavelength of 0.75 μm decreased, i.e. the response in the range (0.70 - 0.80 μm) diminished. This suggests that the response at room temperature (Fig 5.29) in the range of (0.70 - 0.80 μm) after 5 minutes heating in argon is due to an i-layer which formed in CdS, while the same response in the same range after 5 minutes heated in air, is due to the djurleite phase. To summarise, the composition of the mixture phase of chalcocite and djurleite is shifted towards the chalcocite phase by heating at 200^{o}C in argon for 5 minutes. This finding agrees with RHEED, where the chalcocite phase was observed. However, heating under the same conditions, but in air, led to an increase in the contribution from the djurleite phase.

A CdS-Cu_2S heterojunction carrying the chalcocite phase was heated

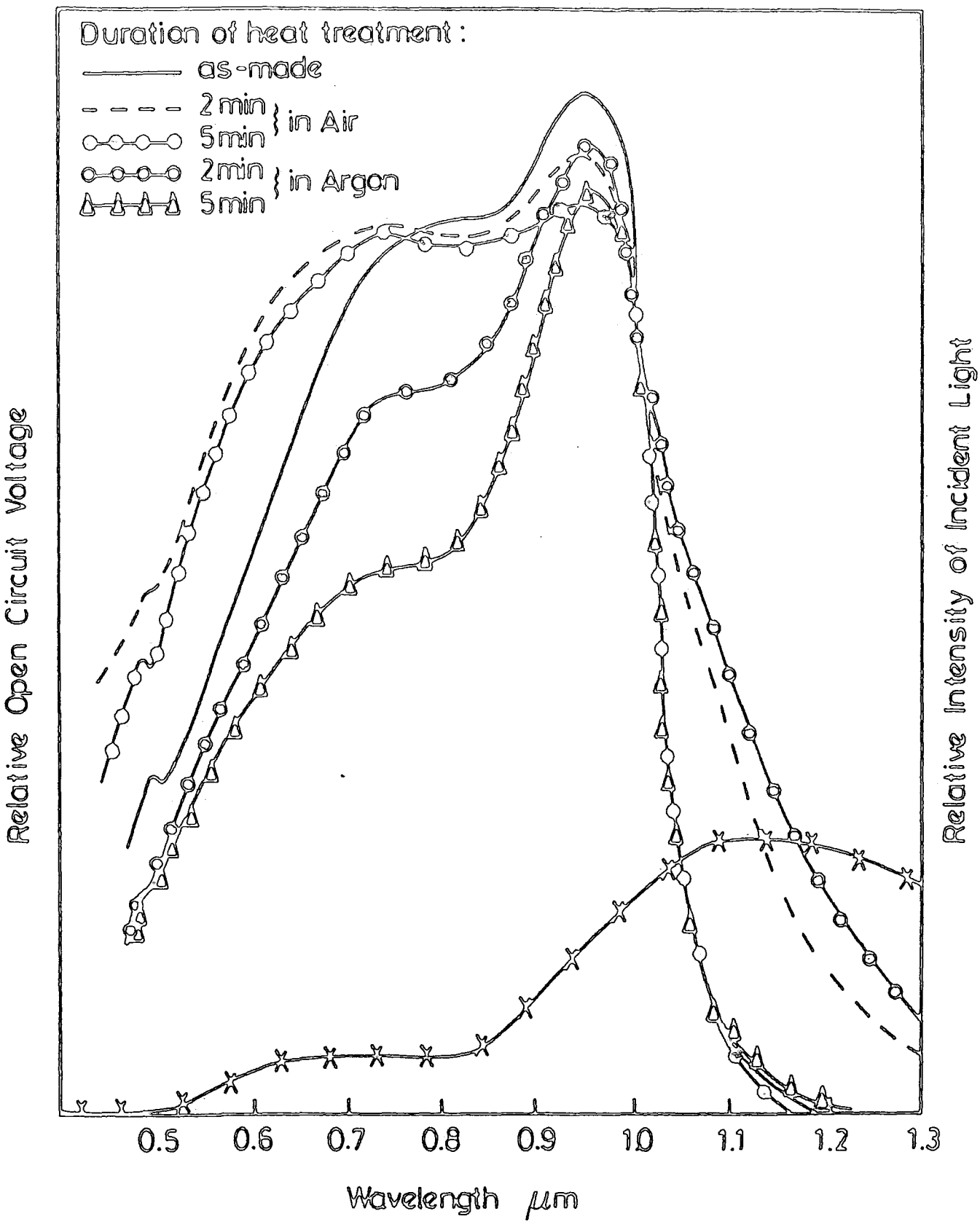

Fig 5.30

Spectral response of the open circuit voltage measured at 85 K of a device heated at 200°C in different ambients.

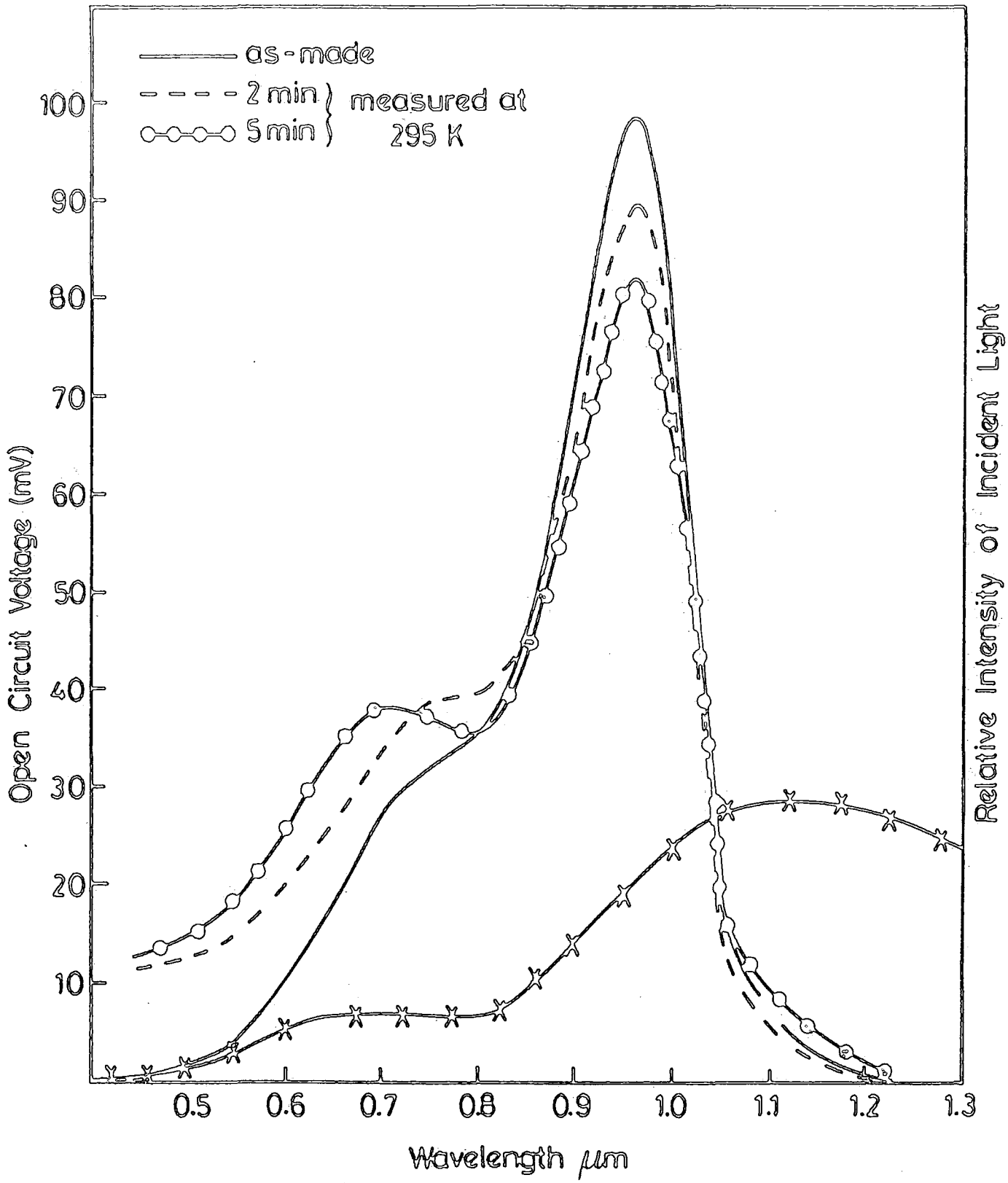

Fig 5.31

Spectral response of open circuit voltage for a Cu_2S-CdS heterojunction heated in Argon at 200°C.

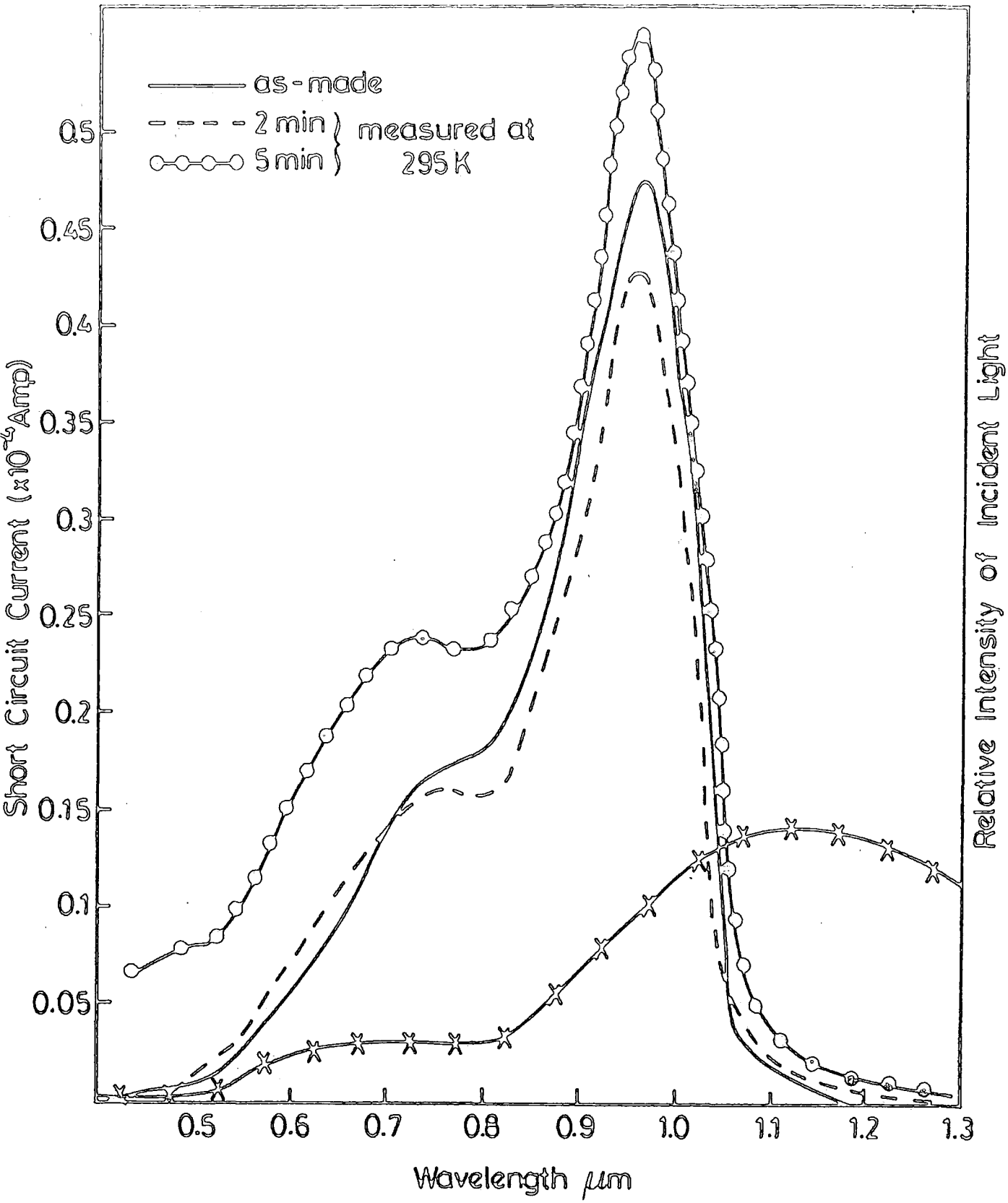

Fig 5.32

Spectral response of short circuit current for a Cu_2S-CdS heterojunction heated in Argon at 200°C

in argon at 200°C for 2 minutes and 5 minutes. The curves in Fig 5.31 and 5.32 illustrate the spectral distribution of V_{oc} and I_{sc} respectively measured at room temperature. In the as-prepared condition both V_{oc} and I_{sc} exhibited a dominant peak at a wavelength of 0.96 μm with a small shoulder at a wavelength of 0.78 μm. After the cell had been heated for 5 minutes, the response in the band at 0.78 μm became large and shifted to 0.70 μm. When the temperature of measurement was reduced to 85K (Figs 5.33 and 5.34) the increase in the response produced by heat treatment, which was noted at room temperature (Figs 5.31 and 5.32) in the band 0.78 μm, was diminished and appeared as a small shoulder lying at a wavelength of 0.75 μm on both the V_{oc} and I_{sc} curves.

5.7 Capacitance-Voltage Measurement

In order to obtain information about the junction of CdS-Cu_xS solar cells and how it depends on the electroplating voltage during the formation process, the device capacitance has been studied as a function of applied bias. By plotting C^{-2} against applied voltage, straight lines should be obtained (see Chapter 3 Section 3.6). The results of such plots for devices formed with different potential bias are shown in Fig 5.35. The devices fabricated with an electroplating bias of +0.25V showed a lower junction capacitance at zero bias than did those formed at smaller electroplating bias. From the slope of the straight lines, and by using the formula (see Chapter 3 Section 3.6), the impurity concentration was calculated and from the intercept of C^{-2} curves with V axis, the diffusion voltage (V_d) was determined. The width of the depletion region of the heterojunction could be obtained by using the formula $w = \frac{\varepsilon_s A}{C(V=0)}$ where A is the area of the sample (see Section 3).

Fig 5.35 shows that when the electroplating bias was

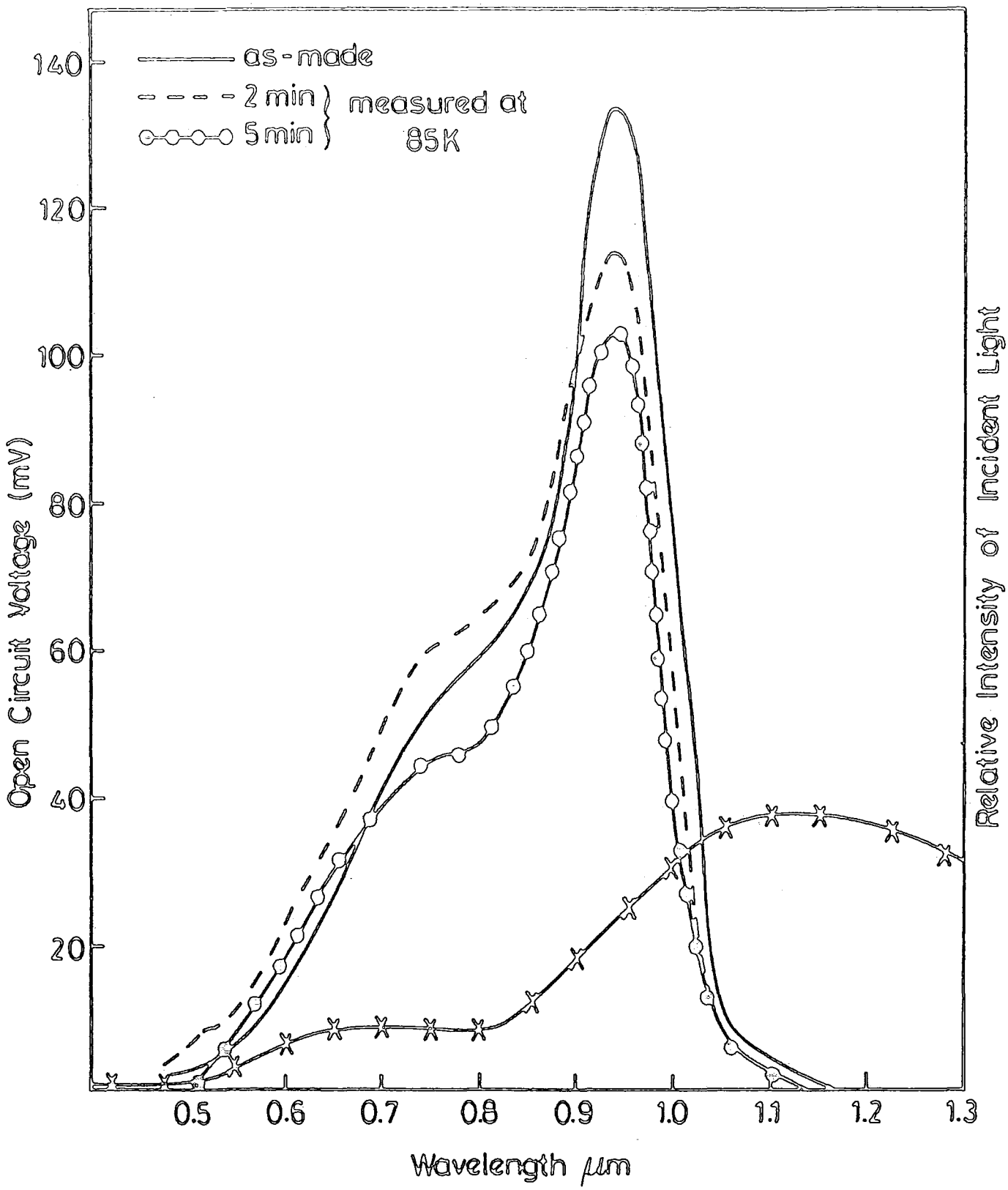

Fig 5.33

Open circuit voltage spectral response of Cu_2S-CdS heterojunction after heated in Argon at 200 C

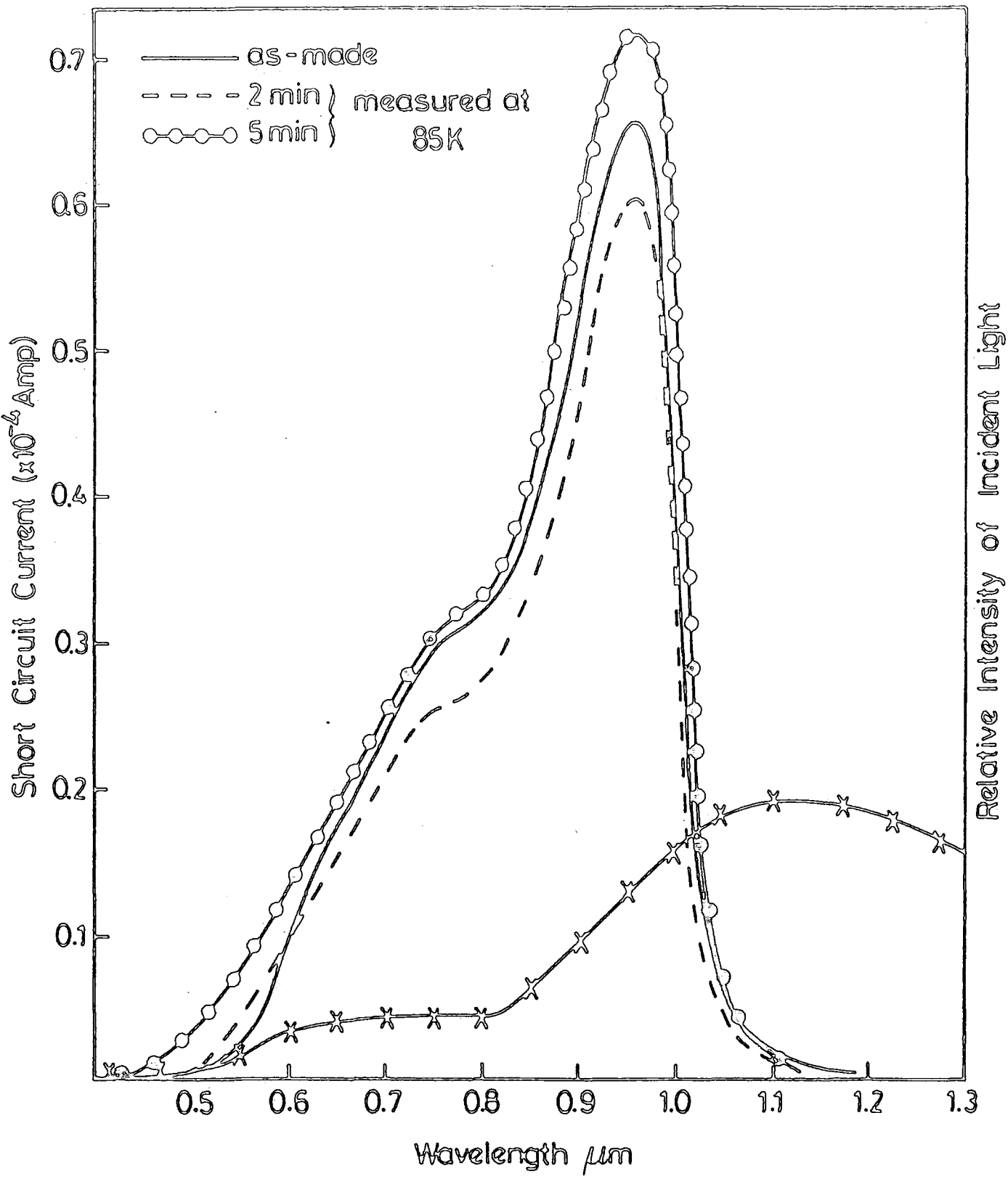

Fig 5.34

Spectral response of short circuit current for a Cu_2S-CdS heterojunction heated in Argon at 200°C.

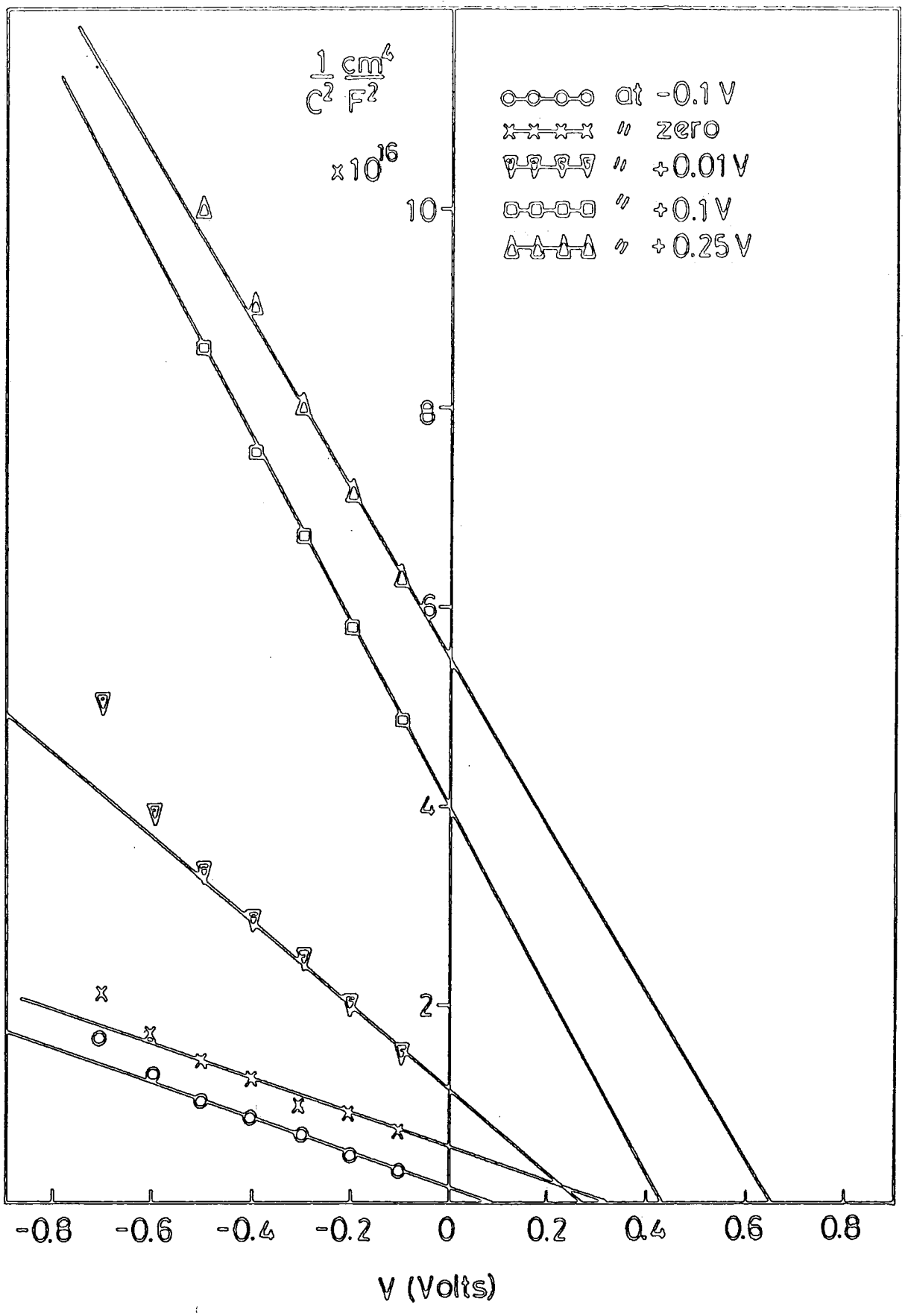

Fig 5.35

C^{-2} - V for an as-prepared device as a function of electroplating bias during preparation.

decreased, the capacitance at zero voltage increased and consequently the diffusion voltage decreased. While the donor concentration increased from 2.24 x 10^{14} to 16.68 x 10^{14} cm^{-3}, the diffusion voltage and the depletion width decreased from 0.65 V to 0.09 V and from 1.21μm to 0.213 μm respectively on reducing the electroplating bias from +0.25V to -0.1V. Fig 5.36 and 5.37 show that the result of plotting V_d and w versus electroplating bias is a straight line. A parabolic relationship was obtained between donor concentration and the plating bias, (see Fig 5.38). Table 5.5 lists the change of donor concentration, diffusion voltage and width of the depletion region as a function of plating voltage.

bias (V)	N_D-N_A	V_d (V)	w (μm)
+0.25	2.24 x 10^{14}	0.65	1.121
+0.1	2.80 x 10^{14}	0.42	0.95
+0.01	6.27 x 10^{14}	0.27	0.512
0.0	15.68 x 10^{14}	0.34	0.364
-0.1	16.68 x 10^{14}	0.09	0.213

TABLE 5.5 : The value of N_D-N_A, V_D and w as a function of electroplating bias.

5.8 Discussion

5.8.1 The Effect Of Using Electroplating Bias

The results reported in this chapter show the way in which the electroplating technique affects the electrical and optical characteristics of CdS-Cu_xS solar cells. The electroplating method has been used to improve the control over the formation of copper sulphide. In this way it has been possible for the phases of copper sulphide to be prepared in a reproducible manner simply by changing the value

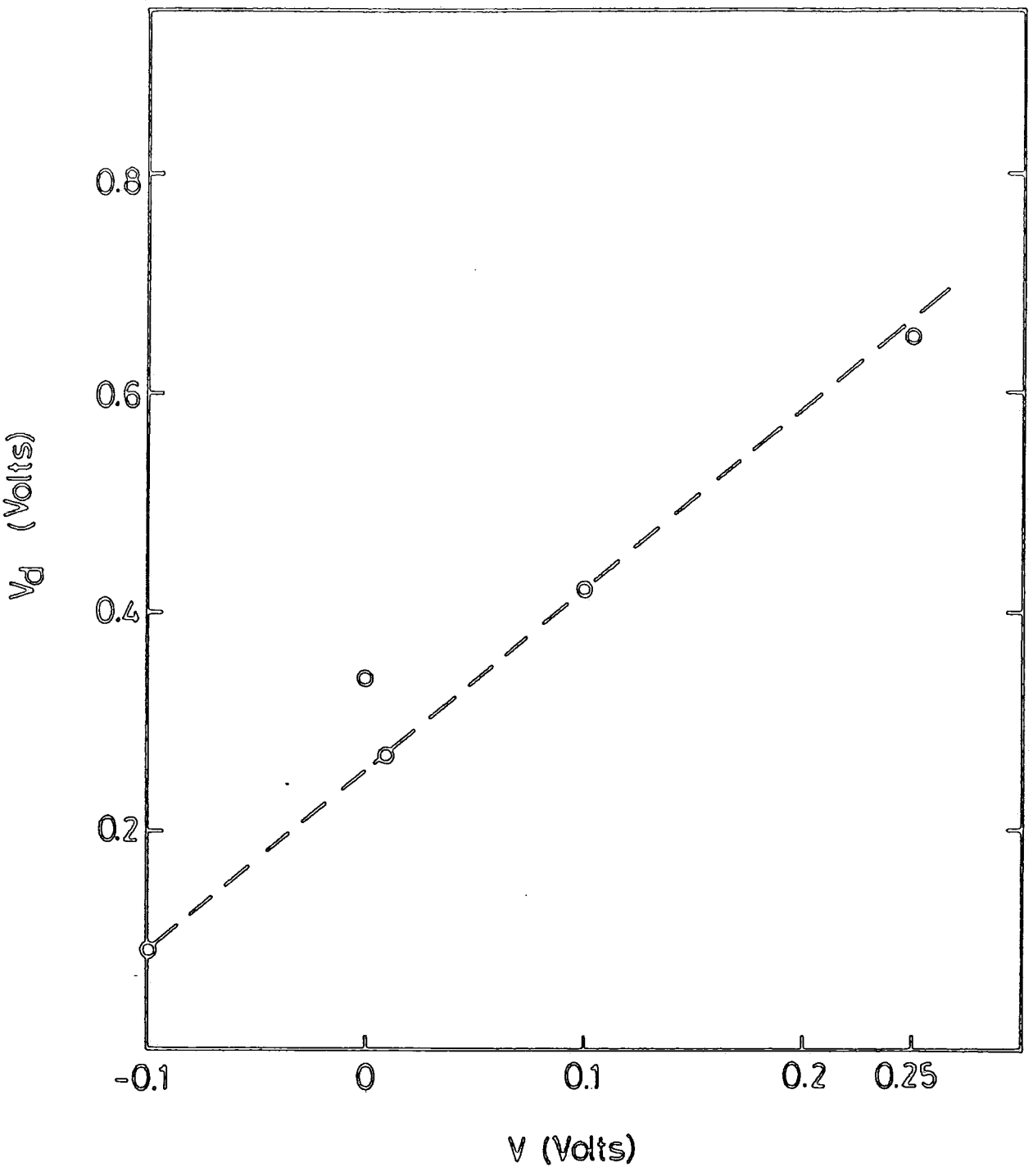

Fig 5.36

The variation of diffusion voltage vs. applied voltage during process.

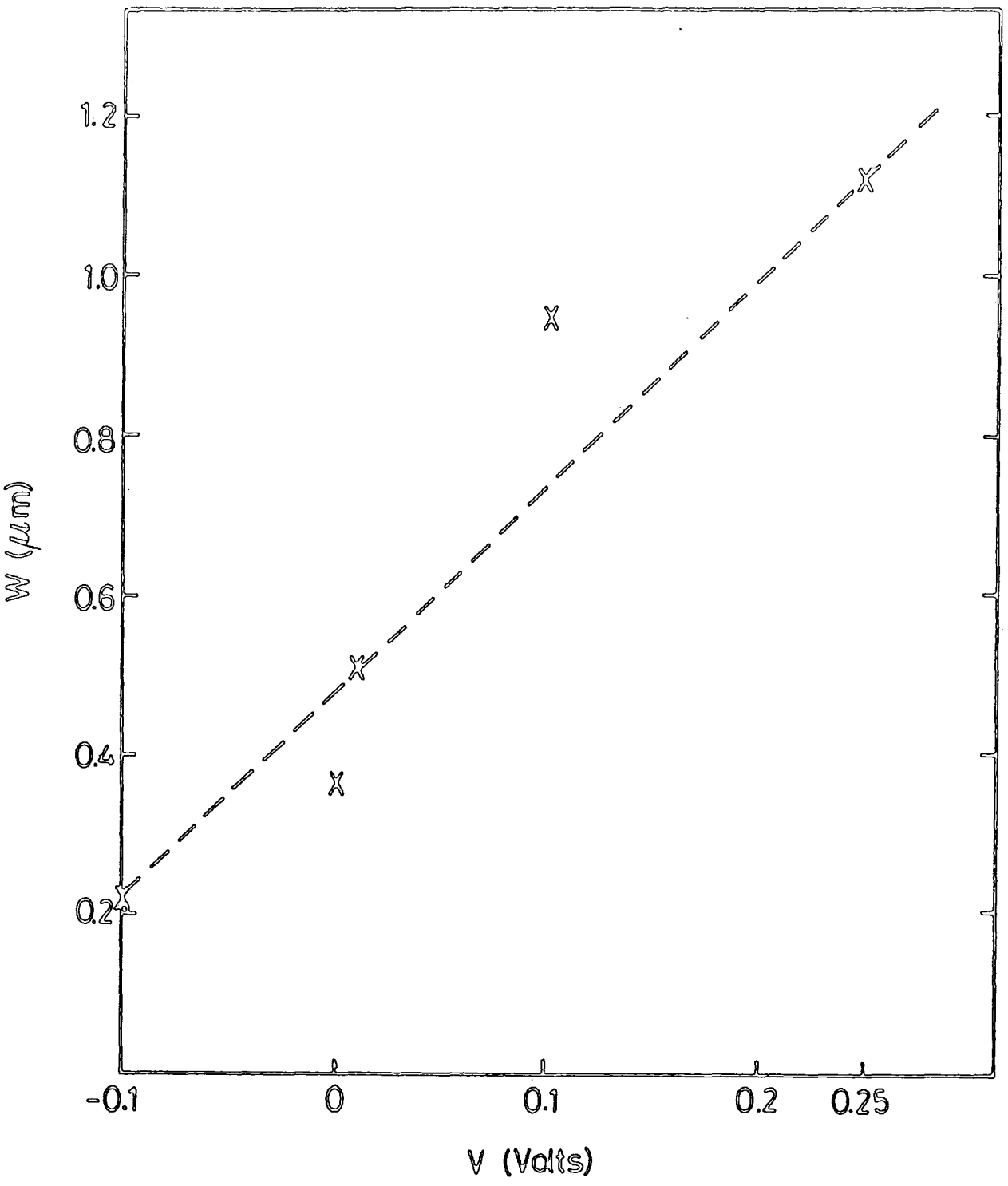

Fig 5.37

The variation of deplation width *vs.* electroplating bias during plating.

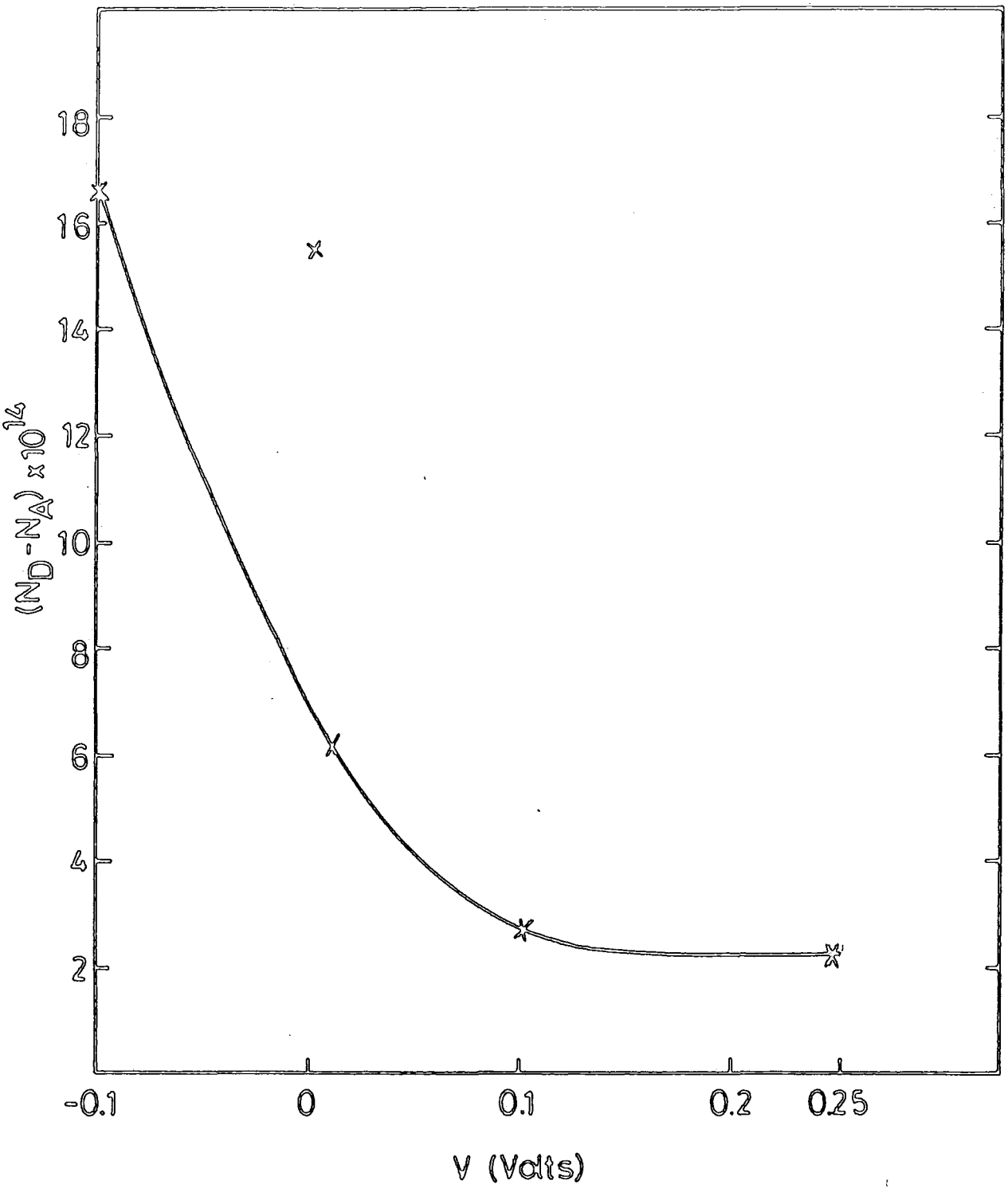

Fig 5.38

The change of donor concentration (N_D-N_A) vs. electroplating bias during preparation.

of the potential bias. Chalcocite, chalcocite with a small proportion of djurleite, a mixture of more or less similar amounts of chalcocite and djurleite, pure djurleite and covellite were obtained by applying electroplating voltages of +0.01V, 0.0, +0.1, +1.0, and +3.0V respectively. It is well established that the chalcocite phase is the one most suitable for solar cells applications [5-8].

Rickert and Mathieu [25] have carried out a theoretical investigation of the parameters controlling the stoichiometry of Cu_xS. They found that it is possible to change the stoichiometric composition by changing the value of electroplating bias during CdS-Cu_xS heterojunction formation. Buckley [26] used Electron Spectroscopy for Chemical Analysis (E.S.C.A.) to find whether the stoichometry was affected by electroplating. The problem encountered was that the E.S.C.A. method was very sensitive to the presence of carbon. So the corresponding signal associated with carbon flooded the relatively small signals arising from the copper and sulphur present. Also it was found that at a bias -0.1V, copper nodules began to appear on the surface of the crystal [26]. Such nodules lead to poor diodes. The consequence of using a bias while plating is that the d.c. field affects the kinetics of Cd^{++} and Cu^{+} ions involved in the formation of Cu_xS on CdS substrates [27]. Without an applied potential the reaction takes place by exchanging one Cd^{++} atom with two Cu^{+} atoms, and the cadmium chloride goes into the plating bath solution. Rastogi and Salkalachen [28] explained the mechanism behind the use of electroplating for CdS-Cu_xS thin film heterojunctions. These workers pointed out that because of the attractive affect of the d.c. field within the CdS for specific values of voltage, the displaced Cd^{++} ions are no longer able to migrate out into the solution of copper chloride, and consequently they accumulate at the junction of the growing Cu_xS interface with CdS. This

accumulation provides a barrier against a deeper penetration of Cu^+ ions and hence more and more Cu^+ ions are incorporated in the bulk of the grown Cu_xS layer [29]. Also the build up of a Cd rich layer adjacent to the interface results in a high junction field which consequently helps to improve the current collection [30]. An additional contributing factor, namely ionic dissociation of the aqueous solution, may become important, if the d.c. potential is increased further, with the result that an evolution of H^+ in the vicinity of the n-CdS surface will reduce the few unavoidable oxidized Cu ions (Cu^{++}) in the CuCl solution to Cu^+. Since it now requires two Cu^+ ions to replace one Cd^{++}, this will also help to improve the Cu_xS stoichiometry [28]. At relatively higher d.c. potentials, two additional mechanisms may reduce the Cu_xS stoichiometry (i) Of the two competing processes, namely acceleration of Cu^+ from the solution into the CdS and accumulation of Cd^{++} at the interface, a higher field may shift the balance in favour of the former. This would cause breaches in the Cd^{++} barrier and develop Cu_xS at greater depth which, by nature being inhomogeneous and irregular, would diminish the overall Cu_xS stoichiometry. (ii) Excessive evolution of H^+ at CdS will reduce the Cu^+ ions to metallic copper which will not participate in the ion-exchange reactions and instead will coat over the CdS surface, consequently reducing the Cu_xS composition. These metallic Cu deposits are clearly observed when the d.c. potential exceeds 2.5V [28]. One proposed model is that by increasing the applied d.c. bias the cadmium barrier may cause a breach or hole. High voltage (+3.0V) would diminish the overall Cu_xS stoichiometry. With a negative one the explanation is different. The use of negative bias is expected to reduce the velocity of the ion exchanging process. Consequently a little Cu^+ is deposited on the surface. However, the use of electroplating leads to results comparable with those obtained

by conventional plating without the application of bias [31,32,33].

Fig 5.10 shows the effect of plating voltage on the device I-V characteristics, while Fig 5.12 illustrates the variation of the device parameters as a function of electroplating bias. The optimum bias of +0.01V produced maximum values of V_{oc}, I_{sc}, FF, γ simultaneously. The change in these parameters can primarily be associated with the variation in Cu_xS stoichiometry with applied bias. The fact that Buckley [26] reported a different value for the plating potential can probably be attributed to the modification introduced in the preparation of the plating solution [12]. At larger values of positive bias devices became short circuited and this can be ascribed to increased Cu^+ diffusion into the Cu_xS layer grown.

The variation in the value of x for Cu_xS between $1 \leq x \leq 2$ has been shown to be strongly dependent on the value of electroplating bias. This has been demonstrated directly by RHEED and indirectly using the established relationship between the phase of copper sulphide and the spectral response [18,19]. Thus it is clear from the measurements of spectral response that the chalcocite peak was most dominant in cells produced using the optimum voltage of +0.01V (see Fig 5.13 and 5.14). The dependence of spectral distribution on bias is illustrated in Fig 5.15 and 5.16. These figures demonstrate a clear relationship between the electroplating bias and the spectral response on the one hand, and between the phase of copper sulphide and the spectral response on the other. A small amount of djurleite always exists with the chalcocite in the converted layer. Fig 5.13, 5.14, show that the large response at the chalcocite bandgap is always accompanied by a shoulder at 0.78 μm due to djurleite, even though RHEED patterns showed no evidence of djurleite [19]. The fact that the response at the CdS bandgap (at 0.49 μm) appeared for devices other than those prepared at the

optimum bias is indicative of reduced absorption in the Cu_xS topotaxial layer and this can be attributed to the presence of less absorbing phases of Cu_xS [34,35].

5.8.2 The Effect Of Heat Treatment

In general during the heat treatment of the CdS-Cu_xS solar cells, many processes take place and these include:

(i) Copper diffusion from the Cu_xS into the CdS to form a compensation i-layer in the CdS [36-40].

(ii) Some cadmium diffusion into the Cu_xS [37,40-43]. Even without heating it has been found that the Cd atoms move rapidly to both the Cu_xS free surface and the CdS-Cu_xS interface on exposure to air at room temperature [44].

(iii) A thin insulating layer may form between the CdS and the copper sulphide [45].

(iv) An oxide layer may be established on the free surface of the copper sulphide [44,45,46]. This leads to changes in the sheet resistance of the copper sulphide layer [4,47] and the shunt resistance [48].

The present work shows that even the covellite phase of Cu_xS can give rise to a reasonable I-V characteristic after heat treatment. Inspection of Figures 5.18 and 5.19 shows that heating in argon for 10 minutes at 200°C was more beneficial than heating in air. However, the difference between heating in argon and in air is that with the argon heated samples, the compensation at the interface takes place solely due to the diffusion of the copper from Cu_xS to the CdS. But with air heat treatment the compensation is due to the combined effects of copper diffusion and the diffusion of oxygen which must have been absorbed at the CdS-Cu_xS interface. This oxygen plays the role of

an electron acceptor [38,49]. This might explain the higher I_{sc} value achieved using air rather than argon. The shift along the voltage axis between the dark and the light current-voltage characteristic curves was considerably larger for heat treatment in air than it was for argon. This may be attributed to the different increase in the series resistance arising from heating in different ambients. Another contributing factor could be the formation of an oxide layer when air is used. It was established in this work using RHEED that the djurleite phase was converted to the chalcocite phase by heating in argon at 200°C for 5 minutes (see Fig 5.17). In contrast there was no change of phase when air was used as an ambient. This could be explained by the loss of sulphur from the Cu_xS layer due to the presence of argon. On the other hand RHEED investigation of the covellite phase indicated that there was no change of phase for heat treatments in either air or argon. This implies that the covellite phase of Cu_xS is more stable than djurleite for the conditions of heat treatment employed. However, RHEED is only able to examine the top layer to a depth of few hundreds of angstroms. So it is possible that the effects ocurring at the junction interface might be different from those at the surface.

The soft I-V characteristics of a device prepared using a bias of -0.1V improved by heating in either argon or air (see Figs 5.21 and 5.22). The effective parameters V_{oc}, I_{sc}, FF and γ all improved with heat treatment. The diffusion of copper from the Cu_xS into the CdS, as well as the other diffusion processes mentioned above, led to the formation of a barrier to both the tunneling of electrons from the CdS to the empty interface states, and the tunneling of holes from the Cu_xS into occupied states in the CdS. Thus the diffusion of copper increases the tunneling distance and the absorption of the oxygen at the interface makes the barrier height greater and the interface

recombination velocity smaller, so that the probability of the light generated electrons being collected is higher than by recombination through the interface.

It is well established that the increase in the barrier height is a function of heat treatment [49]. When the barrier height reaches the optimum value ($\Delta E = 0$) i.e. when the barrier in the CdS reaches the conduction band of the Cu_xS, the device parameters also reach their optimum values. In addition the diffusion of copper into the CdS results in a widening of the junction [50]. The effect of a widened junction is an increase in the recombination losses. These two effects of increase in barrier height and widening of the junction are illustrated schematically in Fig 5.39. So, for these reasons the diode properties improve with heat treatment for the appropriate period in a given ambient. Independent of the bias voltage used during plating, the effect of heating devices with good photovoltaic properties in the as-made condition was not beneficial either in an argon or in an air ambient, and gave rise to a significant reduction in I_{sc} (see Fig 5.23 and 5.24). This result is consistent with the work of Oktik et al [12] for devices prepared by chemiplating. The effect can be attributed to the decrease the sheet resistance [20] and absorption coefficient [7,51].

That there was no response for the as-made CdS-CuS junction is not particularly surprising, but heating the same device in air at 200°C for 5, 10, 15 minutes produced junctions which gave rise to the spectral responses shown in Fig 5.26. The spectral distribution of these shows two peaks, one located at 0.6 μm which might be attributed to a combination of the response from the CuS phase [5] and a copper acceptor level formed by the diffusion of copper into the CdS after heat treatment [11,23]. The other peak, located at 0.49 μm was due to the response from the CdS bandgap. In contrast, heating in argon led to the same

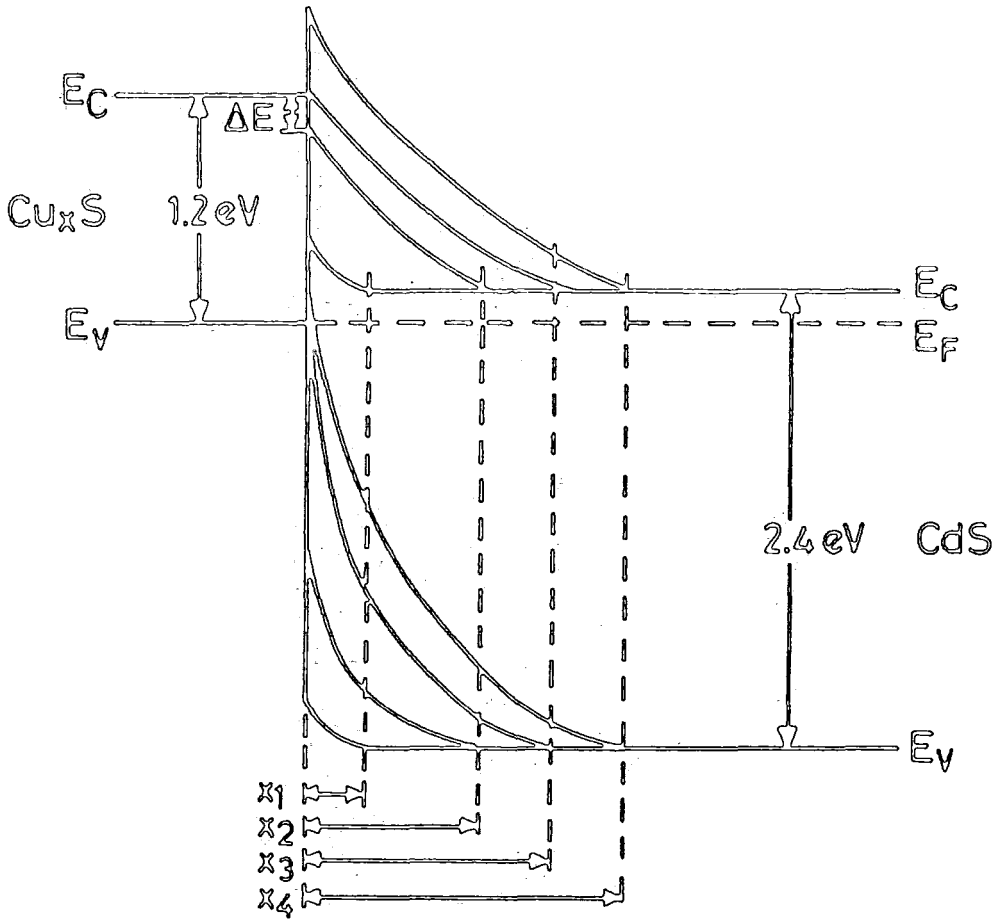

Fig 5.39

Schematic band diagram prepared for a CdS-Cu_2S heterojunction showing how the barrier height of CdS becomes greater and the junction widens as a result of heat treatment.

x_1 , x_2, x_3 and x_4 shows the increase of junction widens with the increasing of time of heating

result except that the peak at 0.60μm shifted to 0.58μm (see Fig 5.25). It was recognised that prolonged heating causes the response at 0.49μm to increase and this is due to the reduction in the absorption of the Cu_xS, with the result that the response of the CdS bandgap is increased [34,35]. The same measurement of these devices (CdS-Cu_xS) at 85 K (Fig 5.28) shows the appearance of a small peak at ∿0.96μm after heating in air which could not be seen at 295 K. This might be attributed to the improvement in collection factor. In contrast, heating in argon (Fig 5.27) for 15 minutes shows a dominant peak at 0.96 μm and small peaks at 0.70 μm, 0.60μm and 0.49μm attributed to chalcocite, djurleite, covellite and the bandgap of CdS. The dramatic change from low phase Cu_xS to high phase Cu_2S is associated with the use of argon as the ambient during heat treatment. This effect is enhanced by changing the djurleite phase to chalcocite as described previously (see Section 5.5 and 5.6.2). This transformation can be attributed to the loss of sulphur from the Cu_xS surface in the presence of argon. The response in the band at 0.70 μm (Fig 5.27) was due to djurleite alone without the copper acceptor layer response in the CdS. This was established because the response in the region of 0.60 to 0.70 μm, which is due to copper levels in the CdS, is diminished at low temperature, whereas that due to the phases of Cu_xS is enhanced [24].

When a device carrying a mixture of phases of chalcocite and djurleite was heated in argon this led to a relative decrease in the response due to djurleite. In contrast when the heating was carried out in air an increase in the djurleite peak was obtained (Fig 5.29). In order to establish whether the peak in the range of 0.70 to 0.80μm was due to the copper acceptor level or to the djurleite phase, the response was measured at 85 K (Fig 5.30). These curves confirm that with heat treatment in air, the peak could be attributed to the direct

bandgap of djurleite. It was clear that the peak at 0.49 μm increased, indicating a decline in the copper sulphide stoichiometry. On the other hand the response in the same range when using argon as an ambient was reduced, and the response at ∿0.96 μm was increased. Thus two different processes have taken place using argon. These are

(i) the loss of sulphur in the presence of argon i.e. an increase in the relative proportion of copper present

(ii) the diffusion of copper into CdS. Here curve 5.30 indicates that the first process was faster than the second, so the stoichiometry was consequently improved. Also it can be seen that the response from the bandgap of CdS has decreased.

This is a further indication for the improvement of the stoichiometry of the Cu_xS. The variation in stoichiometry has two distinct effects on the spectral response [52]. First it decreases the quantum efficiency, owing to a decrease in the absorption coefficient. Secondly, due to the increase in the density, there is a consequential decrease in the photogenerated current. The effect of heat treatment on the chalcocite phase has also been studied. The spectral distributions of V_{oc} and I_{sc} measured at room temperature and at 85 K are shown in Figs 5.31, 5.32, 5.33 and 5.34. These curves have confirmed that the effect of using argon as an ambient during heat treatment is to produce the peak associated with the copper acceptor level in the wavelength range 0.50 to 0.80 μm, rather than a response from direct bandgap of djurleite. This is confirmed by the reduction in the response in this range when the measurements were made at 85 K.

5.8.3 The Effect Of Electroplating Method on C-V Measurements

The C^{-2}-V measurements in Fig 5.35 shows that the voltage axis intercept and the slope of these curves increases with the value of

the electroplating bias used during heterojunction formation, while the capacitance decreases with increasing bias. The reduction in the capacitance arises from an increase in the thickness of the space charge layer. The change in the intercept on the C^{-2} axis indicates that different amounts of copper have diffused during the different platings. That is consistent with the explanation presented for a different phase of copper sulphide, that the use of a high electroplating bias results in the diffusion of the copper to greater depths in the CdS, so the capacitance was consequently decreased. It was found that chalcocite (Cu_2S) has a low value capacitance at zero voltage [53]. On the basis of the results reported here (see Section 5.3.2 and 5.8.1), that when a negative bias is used the ion exchange between Cu^+ and Cd^{++} was controlled (see Section 5.8.1), a small quantity of Cu^+ was deposited on the CdS. Fig 5.37 shows the increase in the depletion width with plating bias which was expected because of the differing extent of copper diffusion. The increase in the depletion width leads to a shift of the curve along the voltage axis resulting in a smaller value of the intercept with the decrease in the bias (Fig 5.35). The net donor concentration is shown to establish a relationship between the value of electroplating bias during the growth of Cu_xS on CdS and the magnitude of the donor concentration (see Fig 5.38).

5.9 Conclusion

An electroplating method has been used in this work to control the phase of copper sulphide by changing the electric field during the formation of CdS-Cu_xS heterojunctions. Different phases have been produced by using a wide range of electroplating bias and these have been identified directly using RHEED, and indirectly from spectral response measurements, except in the case of cells carrying a layer

of covellite, where the spectral response has not previously been reported. The change from the djurleite phase to chalcocite has also been achieved by using argon heat treatment for 5 minutes at 200°C. This effect was found to be reversible in that layers of chalcocite were converted to djurleite when air was used. Generally the transformation from covellite to djurleite and from this to chalcocite can be accomplished by argon heat treatment for 15 minutes at 200°C where an i-layer is formed. Thus for affecting the stoichiometry of Cu_xS, argon is found to be a beneficial ambient. Hard and soft current-voltage (I-V) characteristics have been obtained by changing the value of the electroplating bias. From non-rectifying devices for cells carrying a covellite phase, heat treatment either in air or argon led to a reasonable device. Soft I-V characteristics improved by this heat treatment as well. The effect of heating devices with good photovoltaic properties in the as-made condition was not beneficial either with argon or air as the ambient. A significant reduction in the value of SCC after heat treatment was observed. A dramatic change in the spectral response accompanying the reduction in the covellite response associated with the increasing in the chalcocite response as a function of argon heat treatment has been achieved. A reduction of the response due to copper levels in the CdS was observed at low temperatures. Also C-V measurements have demonstrated that with increasing plating bias the donor concentration decreased at first and then became constant. This will effect the junction capacitance by changing the width of the depletion region.

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CHAPTER SIX

CdS-Cu_2S Thin Film Photovoltaic Cells

6.1 Introduction

Thin film solar cells have been studied and used for more than 25 years. In this chapter the structure of CdS films is investigated. In order to establish better control over the phase of Cu_xS, formed topotaxially on evaporated thin films of CdS, the effect of the application of a d.c. bias to the CdS during electroplating has been studied. The influence of the substrate material on the CdS deposited has been investigated by using tin oxide and silver/chromium coated glasses. RHEED patterns were recorded for devices prepared at different values of electroplating bias to study the relationship between the electroplating bias and the phase of Cu_xS thin film. Current-voltage characteristics of the heterojunctions were measured together with spectral response recorded at room and liquid nitrogen temperature. The effects on the I-V characteristics and on the spectral responses of annealing in different ambients for thin film devices prepared on both tin oxide and Ag/Cr substrates are also reported.

6.2 Film Deposition

6.2.1 Substrate Preparation

Two kinds of substrate have been used in this work, namely tin oxide coated glass and glass slides coated with silver and chromium. Each type requires different cleaning and handling techniques prior to deposition of the CdS film. All substrates were firstly cleaned thoroughly using 5% Decon-90 solution in an ultrasonic bath. Next they were washed with deionized water and isopropyl alcohol and finally

they were cleaned by placing them in isopropyl alcohol vapour for a few hours.

An electron beam evaporator was employed to coat glass slides with layers of silver and chromium. The experimental arrangement is shown in Fig 6.1 in which the hot molybdenum filament was optically screened from both source and substrate by the negatively biased focussing cage and washer. The electrons were focussed onto the surface of the evaporant which was contained in one of the four graphite crucibles in the water cooled hearth. Two of these contained chromium and silver respectively. Each crucible could be positioned below the electron gun by a lateral movement of the copper hearth. A 10 kV variable power supply was used to provide the accelerating potential and a stabilised maximum beam current of 150 mA was employed. For the deposition of the first layer, the substrate temperature was raised to 300°C and then about 500 Å of chromium was deposited onto the glass slides. Next the crucible which contained the silver was positioned below the electron gun and a layer of silver about 1 μm thick was deposited onto the chromium. The use of chromium ensured better adhesion to the glass than was attainable with silver alone.

6.2.2 Vacuum System

Fig 6.2 shows a schematic diagram of the vacuum system used for the deposition of CdS films. The system maintained a pressure of about 10^{-5} torr during the evaporation process. In the bell jar fixture shown in Fig 6.3, two separate NiCr/NiAl thermocouples were located at the top of the substrate. One of these was used to control the substrate temperature with a Eurotherm controller and the other measured the substrate temperature separately during the evaporation. The substrates were heated indirectly by a 1 kW infra-red lamp. The layer

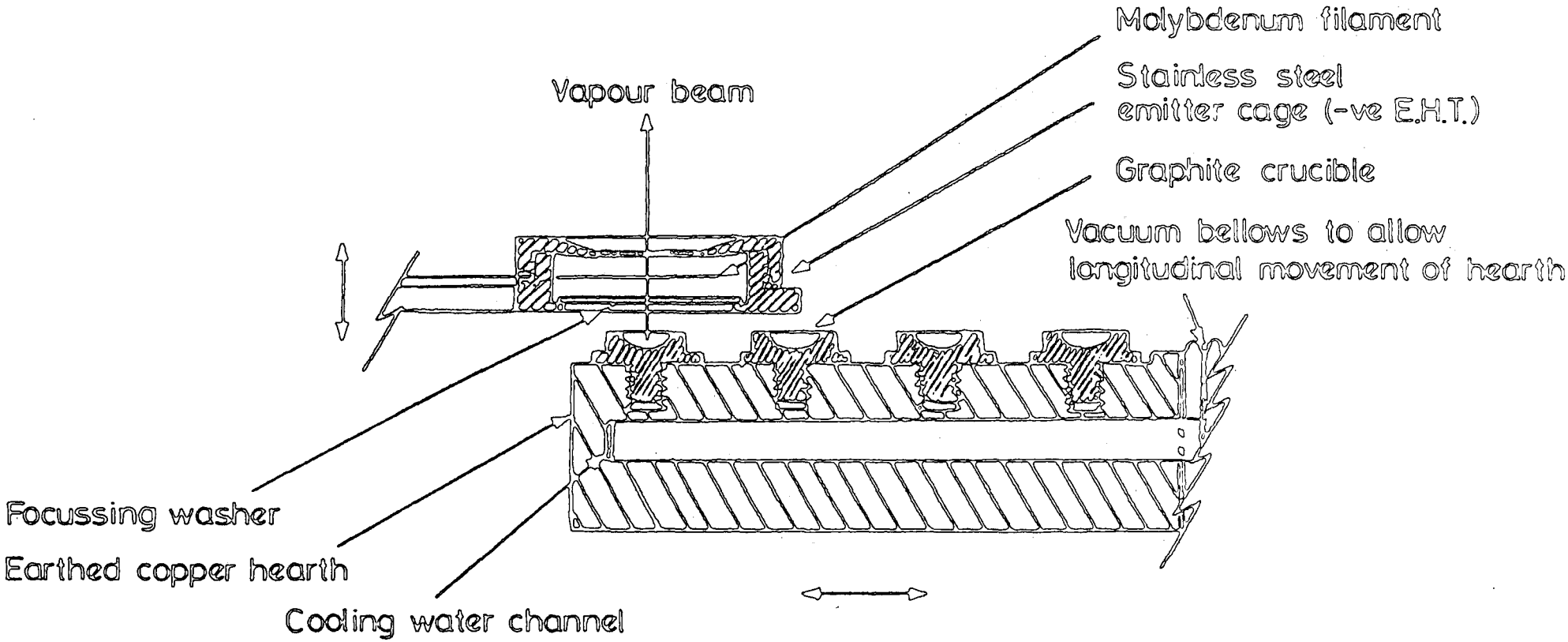

Fig 6.1 : Electron beam evaporator.

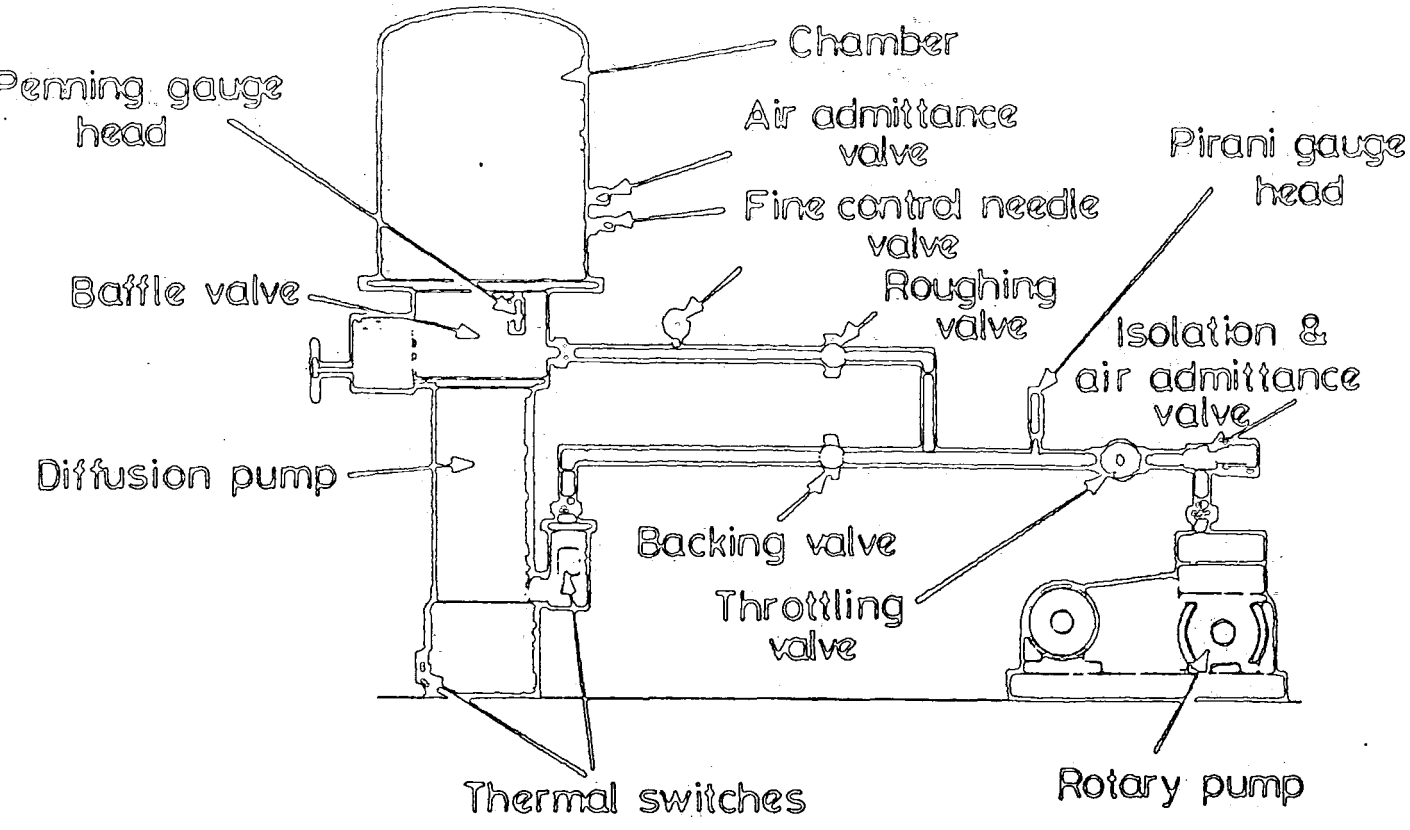

Fig 6.2 : Schematic diagram of evaporator.

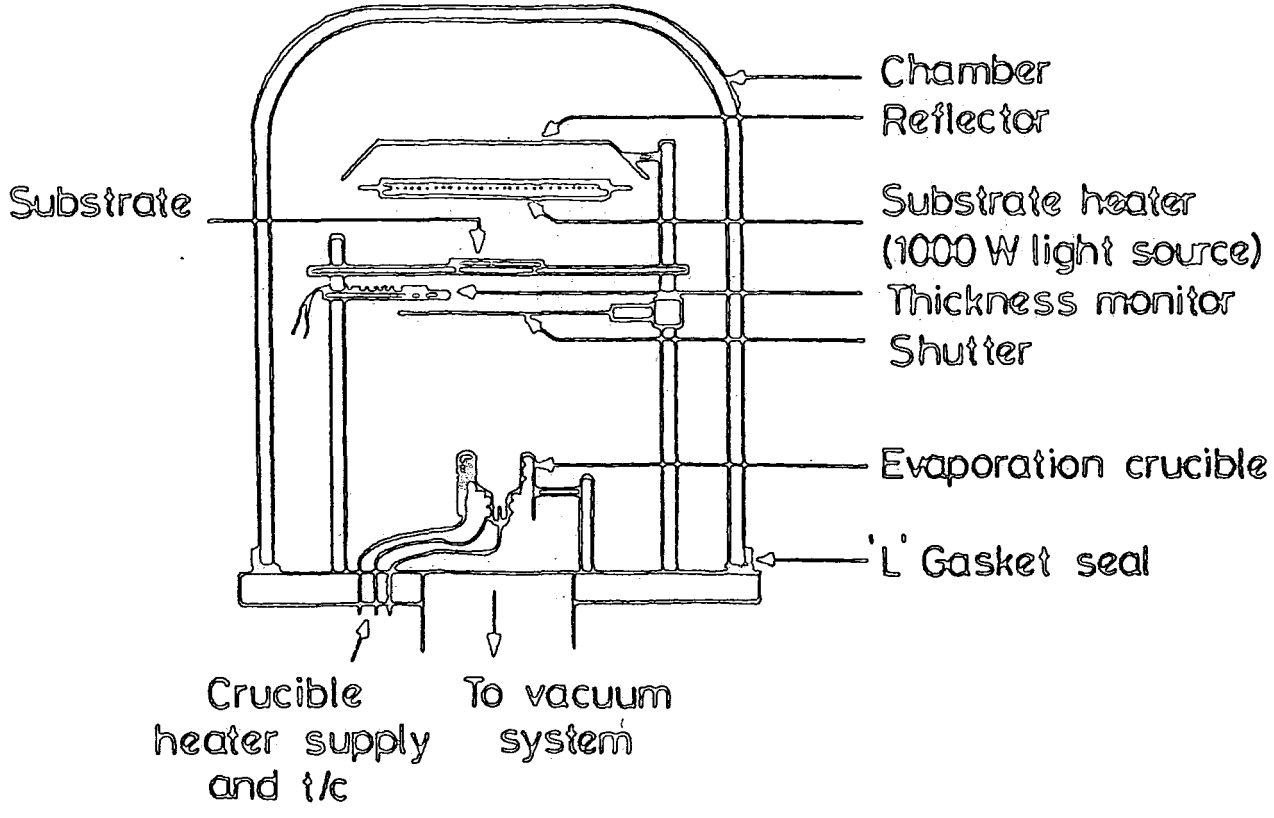

Fig 6.3 : Bell jar fixture of the evaporator.

thickness and the deposition rate were determined using a quartz thickness monitor.

A movable shutter was located above the crucible so that the source could be outgassed before the start of the deposition onto the substrate. The crystal holder was fixed onto the same rod which operated the shutter through a rotary seal, thereby allowing the thickness monitor to be moved away from the substrate after measuring the evaporation rate. A tantalum crucible was used to contain the CdS charge and the evaporation source is shown in Fig 6.4. This crucible was heated directly and the temperature was measured using a Pt (13%) Rh/Pt thermocouple.

6.2.3 Evaporation Procedure

The crucible was filled with $\sim$10 g of Optran grade CdS powder and then a layer of quartz wool was placed at the mouth of the crucible to prevent spattering. The freshly cleaned substrates were mounted on their holder (see Fig 6.3) and the vacuum system was evacuated to 10^{-5} torr. Next the substrate was heated to 200^{o}C for 30 minutes and the CdS was outgassed over the same period by increasing the filament current gradually until the temperature reached 550^{o}C. The source temperature was then increased to 100^{o}C and the evaporation rate was set to the required value. When the steady state was reached, the shutter was opened and the evaporation rate was measured using the thickness monitor. In this way a film could be grown to the desired thickness. To minimise oxidation effects, the films were allowed to cool down to room temperature before removing them from the vacuum.

6.3 Film Structure

A typical RHEED pattern of a deposited CdS film is shown in Fig 6.5. Examination of a cross section of this film in the SEM led to

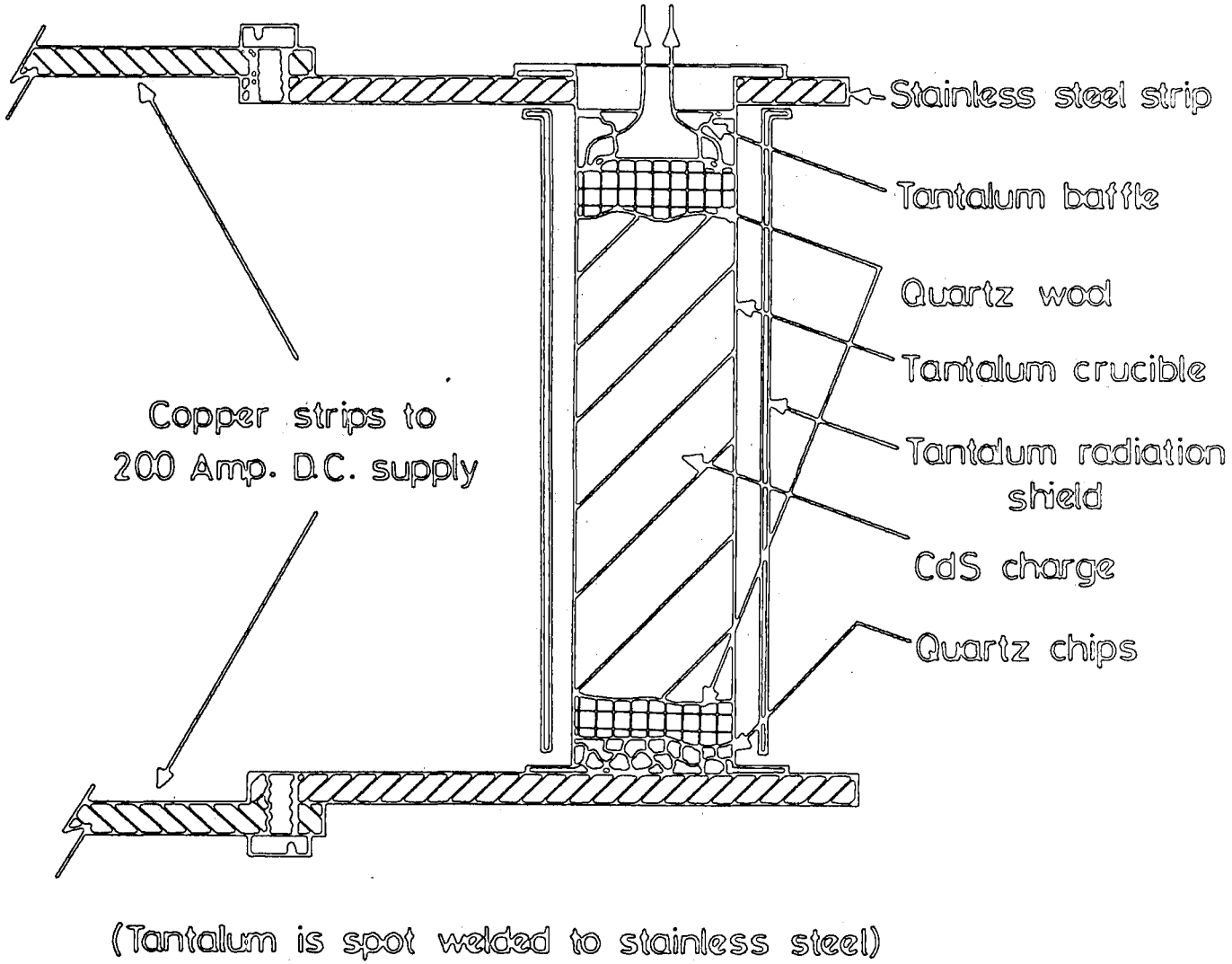

Fig 6.4 : Evaporation source

the micrograph shown in Fig 6.6. This demonstrates that the thickness of the film was about 7μm. It was found that the absorption coefficient and carrier concentration increased as the thickness of the film decreased [1]. The RHEED pattern is characteristic of a film with fibre axis. The important parameters which control the structure and the grain size are the source and substrate temperatures and the growth rate [2]. The deposited CdS should also have a low resistivity, otherwise low current devices result [3].

6.4 Heterojunction Preparation

CdS-Cu_xS heterojunctions were formed by the wet barrier method with electroplating bias. The CdS substrate was not etched for a number of reasons. Firstly, as the film thickness was only 7μm it was considered that etching in HCl would probably lead to complications associated with preferential etching at the grain boundaries. Secondly, it had been found using XPS that etching caused a reduction in the Cd to S ratio because Cd is etched out faster in the etchant, leading to reduced inclusion of Cu in the ion-exchange deposition of Cu_xS [4,5]. Thirdly the opening of the grain boundaries leads to the growth of Cu_xS along them [5]. Migration of Cu from the solution along the grain boundaries of CdS can lead to ohmic shunting [6].

For the plating process the edges of evaporated films were painted with an acid resistant lacquer to avoid the CdS being plated in these regions to avoid shorting directly to the substrate. This action also served to prevent the film from peeling at its edges when it was immersed in the aqueous plating bath. The films were dipped in deionized water just before immersing them in the plating solution. Various potential biases were applied using a platinum sheet as an electrode. The films were then immersed in the CuCl solution (see Chapter 5

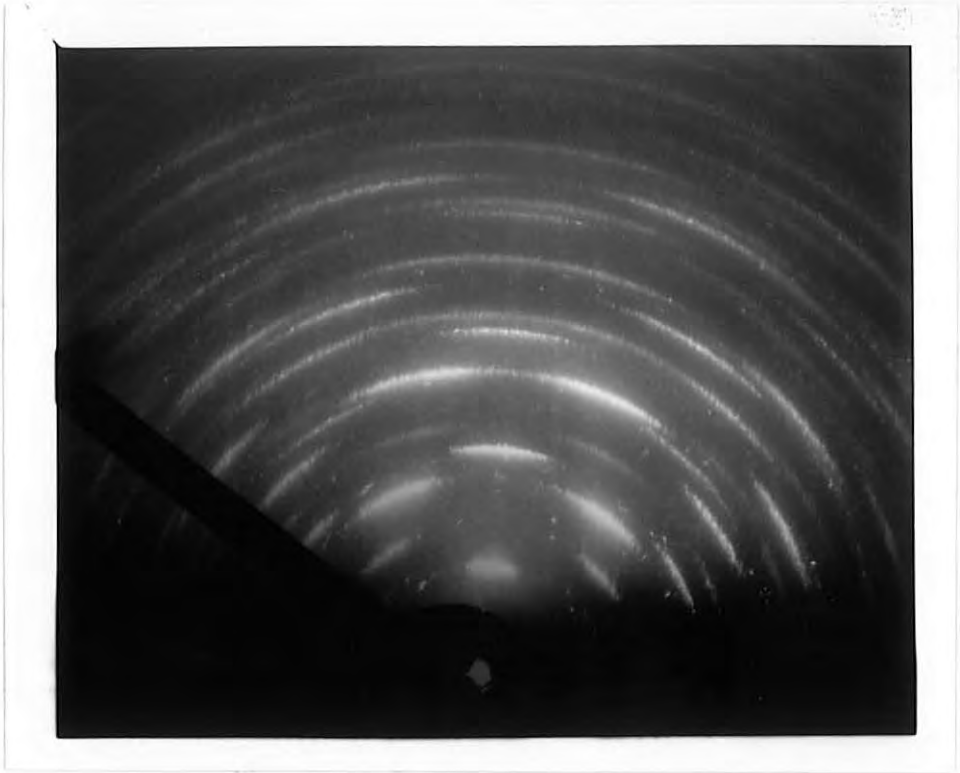

Fig 6.5 100 kV RHEED pattern from a thin film of evaporated CdS.

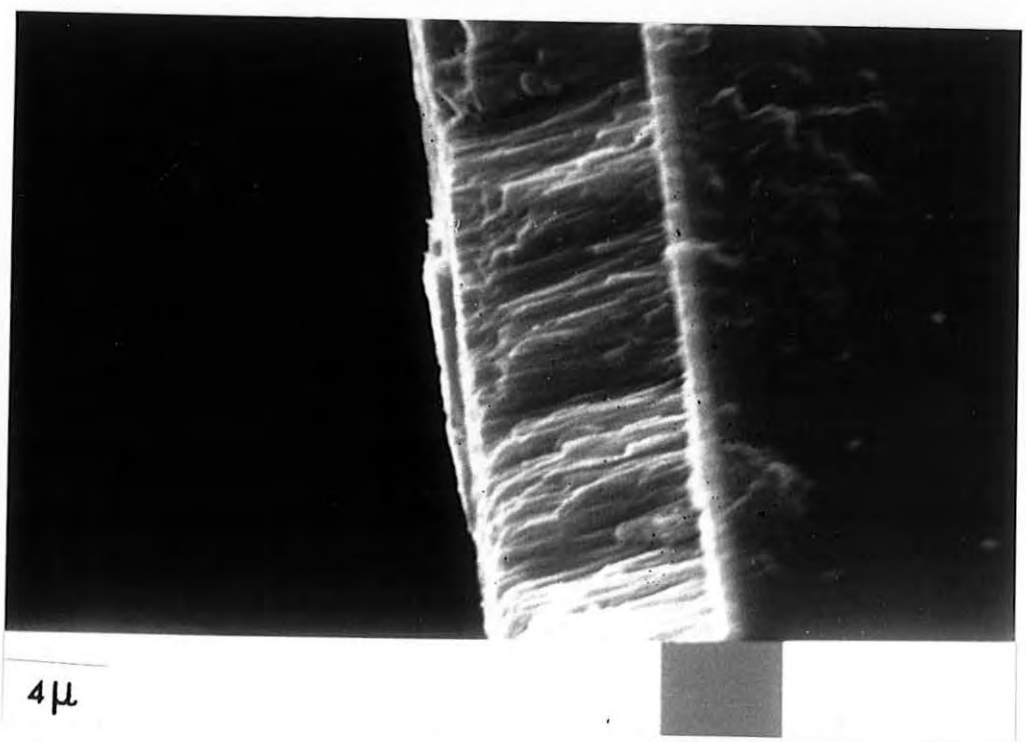

Fig 6.6 SEM of a cross section of CdS evaporated film.

Section 3.1) for 10 seconds, after which they were rinsed with deionized water and dried in a stream of nitrogen. A circular gold contact of 1 mm diameter was evaporated onto each of the copper sulphide layers.

6.5 Properties of CdS-Cu_xS Thin Films Formed By The Electroplating Technique

6.5.1 RHEED Investigation

In an attempt to identify the copper sulphide phases formed on thin film CdS, the Cu_xS layers were examined by RHEED. Layers formed using a wide range of biases were examined. Fig 6.7 shows the pattern corresponding to the cell prepared with a bias of +0.1V during plating. It can be seen that while the reflections from the CdS substrate are dominant, a clear array of additional and closely spaced reflections are present. The pattern obtained from the Cu_xS phase for a device prepared with a plating bias of - 1V is shown in Fig 6.8. The reflections from the copper sulphide appear as a series of lines, or extended arcs, lying parallel to the shadow edge of the sample. These obviously preclude the measurement of interplanar spacing in the direction parallel to the shadow edge. To identify the phase in Fig 6.7 the interplanar spacings were determined by measuring the distances between the diffraction spots and the origin. By applying the formula for the hexagonal crystal system for which

$$\frac{1}{d^2_{hk\ell}} = \frac{4}{3a_0^2}(h^2 + kh + k^2) + \frac{\ell^2}{c_0^2}$$

the d_{006} spacing of CdS was used to determine the camera constant. By measuring the distances R_1 and R_2 between two weak adjacent diffraction spots perpendicular and parallel to the shadow edge, the corresponding

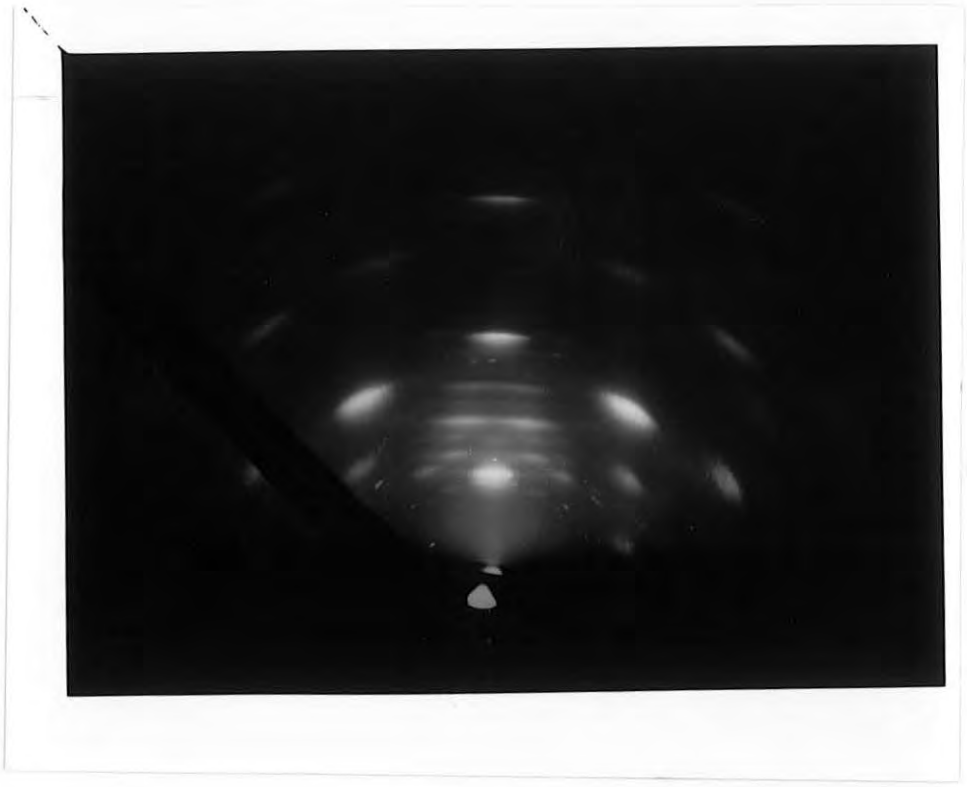

Fig 6.7 RHEED pattern of the chalcocite, Cu_2S-CdS thin film fabricated by applying +0.1V during plating.

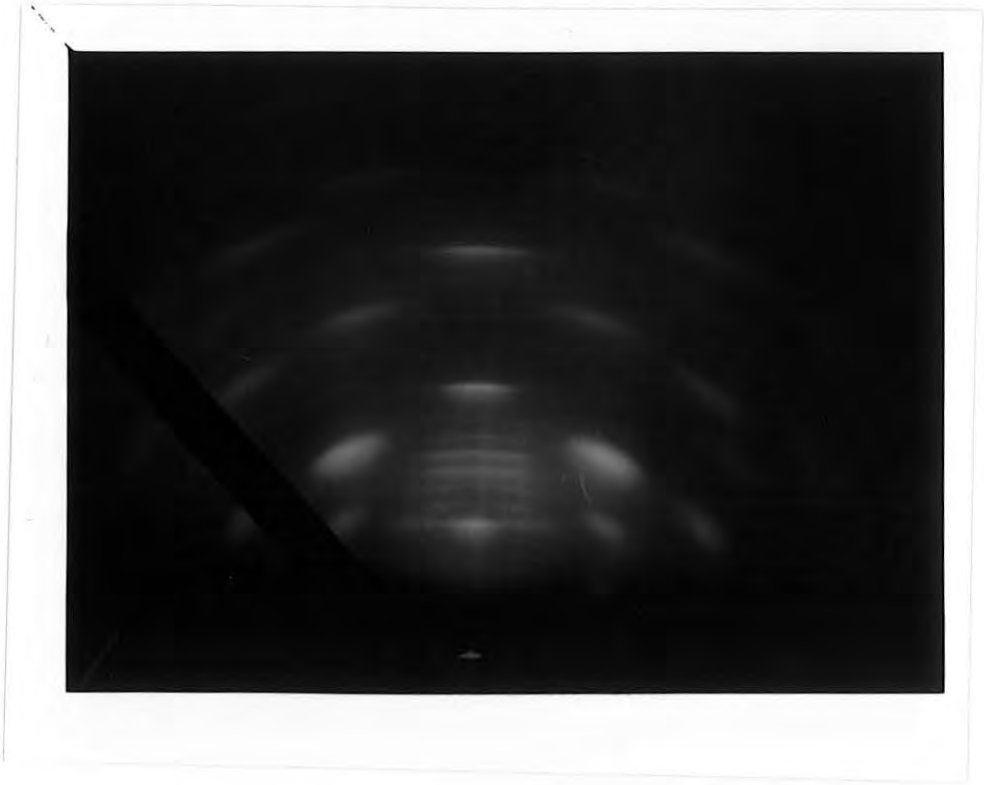

Fig 6.8 RHEED pattern of the djurleite, $Cu_{1.96}S$-CdS thin film fabricated by applying -1.0V during plating.

d-spacings were found to be

$$d_1 = 13.30\ \text{Å} \quad , \quad d_2 = 11.86\ \text{Å}$$

Comparison of these values with A.S.T.M. index data strongly suggest that the phase was orthorhombic chalcocite for which

$$d = 13.497\ \text{Å} \quad , \quad d = 11.881\ \text{Å}$$

The presence of the lines of intensity parallel to the shadow edge in the pattern in Fig 6.8, made it impossible to resolve any spots in this direction. Consequently, only the distance between the lines in a direction perpendicular to the shadow edge could be measured and this gave rise to an interplanar spacing of 26.35 Å. This is consistant with the presence of djurleite which has a c parameter of 26.84 Å. The copper sulphide for the sample prepared with +3.0V bias during copper sulphide growth is shown in Fig 6.10. Measurements from this led to d values consistant with the covellite phase. These values are in agreement with A.S.T.M. index data and are shown in Table 6.1.

d-spacing	Calculated from RHEED patterns	A.S.T.M. index
d_1	2.880	2.813
d_2	1.890	1.896
d_3	1.234	1.227

TABLE 6.1

The values of d-spacings calculated from RHEED patterns and from A.S.T.M. index for covellite.

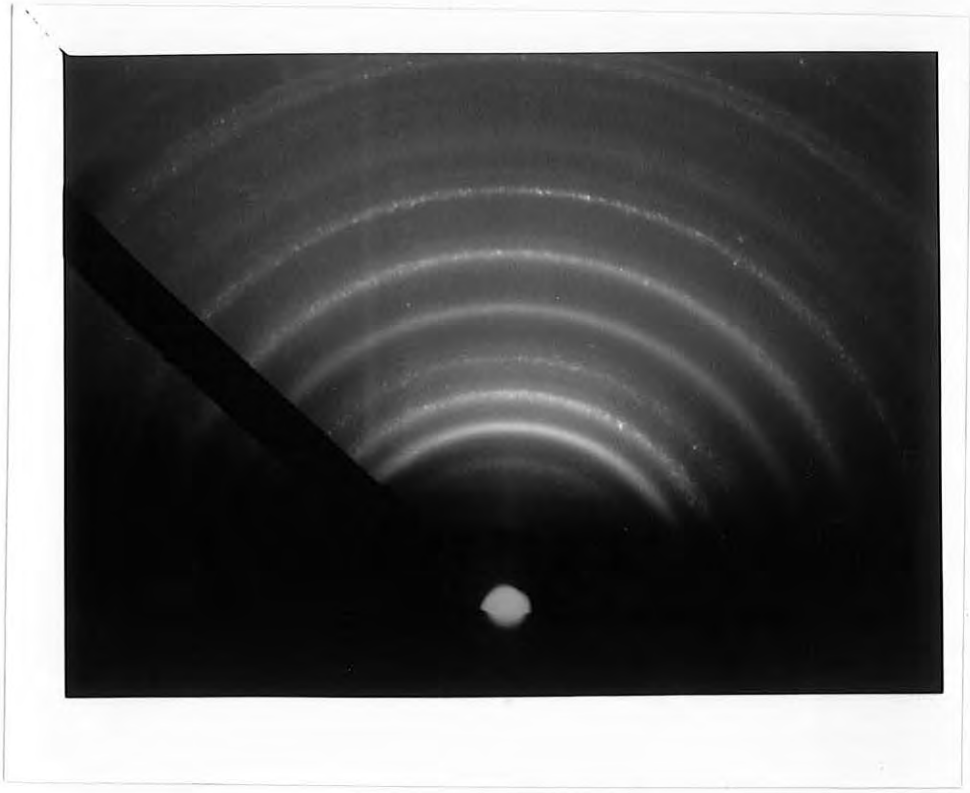

Fig 6.9 RHEED pattern of the copper sulphide phase prepared by applying -2.0V during plating.

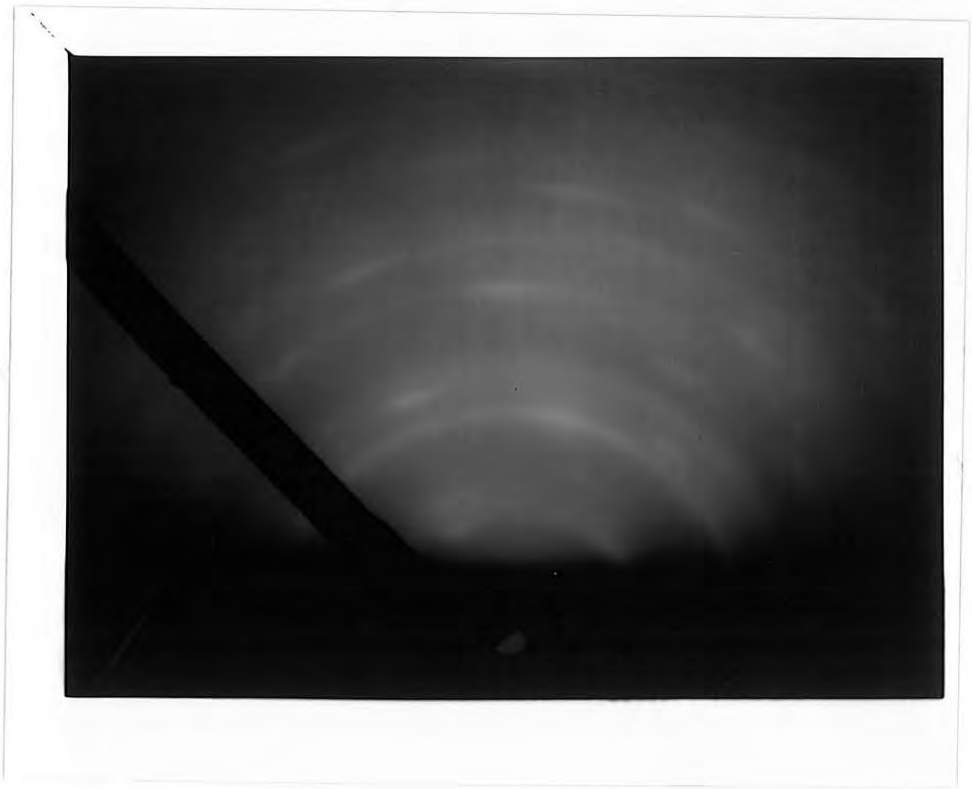

Fig 6.10 RHEED pattern of copper sulphide phase fabricated by applying +3.0V during plating.

In the electron diffraction studies of Russell and Woods [7] and Cook et al [8] on copper sulphide formed on single crystal CdS, different phases were produced.

It may be concluded therefore, that the electron differaction patterns obtained from the copper sulphide phase produced on CdS thin film substrates with plating biases of +0.1, -1.0 and +3.0V can be attributed to chalcocite, djurleite and covellite respectively.

6.5.2 Spectral Response

Measurement of the spectral responses of CdS-Cu_xS thin film devices were carried out to investigate

i) the optimum electroplating bias for thin films

ii) the effect of the substrate material upon which the CdS films were grown, and

iii) the effect of annealing in different ambients.

The room temperature spectral responses of the open circuit voltage for as-made devices formed by plating at different biases are shown in Fig 6.11. Two peaks were observed at wavelengths of 0.96 μm and 0.78 μm. These bands have been discussed in the previous chapter and are associated with the generation of electron hole pairs in the chalcocite (Cu_2S) and djurleite ($Cu_{1.96}S$) phases of copper sulphide respectively [9]. All three curves in Fig 6.11 exhibit a dominant peak at 0.96μm with small subsidiary response at 0.78μm, the smallest of these occurred when the heterojunctions were formed at 0.1V. It is concluded that this bias produced the optimum response from the chalcocite phase. To demonstrate this point more conclusively, the responses of the same devices were measured at liquid nitrogen temperature (Fig 6.12). This showed that an electroplating bias of -1.0V caused a significant increase in the peak at 0.78 μm and a reduction in that at 0.96μm, indicating

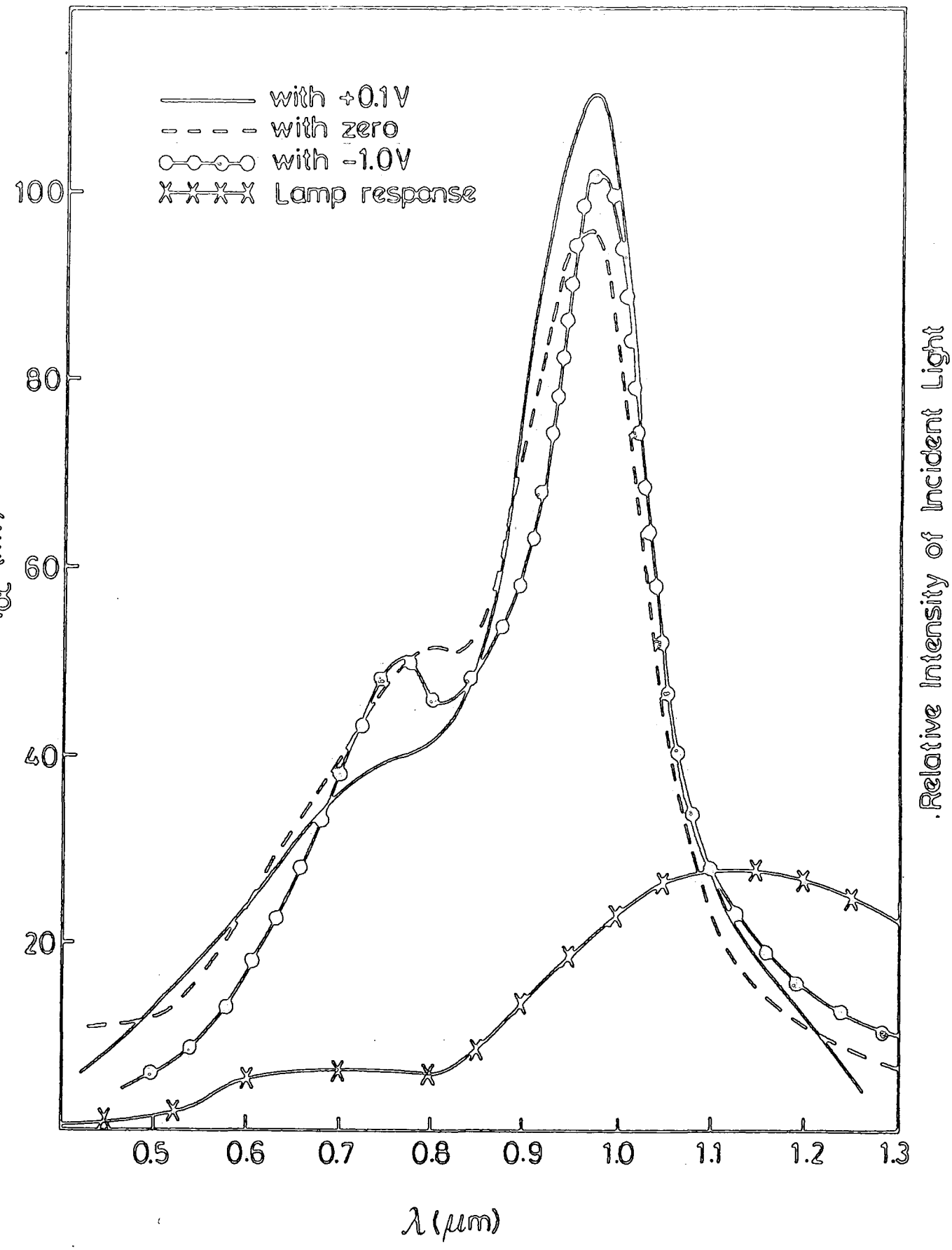

Fig 6.11 : Spectral response of V_{oc} measured at room temperature for Cu_xS-CdS formed with different electroplating bias

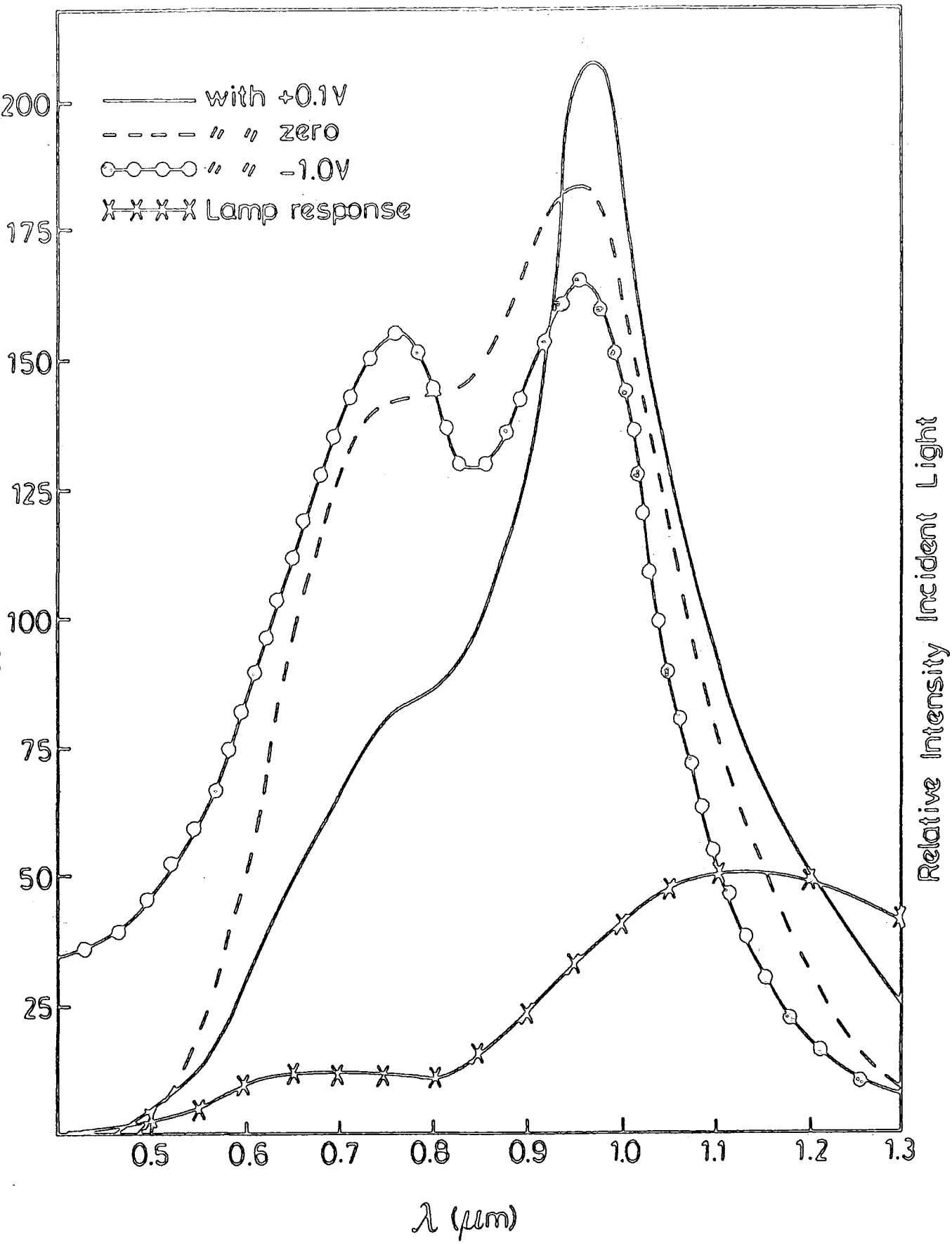

Fig 6.12 : Spectral response of V_{oc} measured at liquid nitrogen temperature of Cu_xS-CdS formed with various electroplating bias.

a relative increase in the response due to djurleite.

The effect of annealing in air on the spectral responses of CdS-Cu_xS thin film devices prepared on SnO_x and Ag/Cr coated glasses using the optimum plating bias was investigated at room temperature (Fig 6.13) and 85 K (Fig 6.14). After 2 minutes and 5 minutes annealing for a device prepared on tin oxide, a considerable reduction in the response at the wavelength of 0.96 μm and an increase in that at 0.78μm was detected thus indicating a deterioration in the optimum phase of copper sulphide. In contrast, similar annealing of a device prepared in the same conditions but on a Ag/Cr substrate showed very little difference from the as-made response with negligible increase in the djurleite response at 0.78 μm. This result shows that devices which were fabricated on Ag/Cr coated glasses were more stable with much less copper diffusion and correspondingly less degradation.

To investigate the effects of argon annealing on devices formed on these two different substrates, two such devices were heated in this ambient for 2 minutes and 5 minutes at 200°C and their spectral responses were measured at 295 K (Fig 6.15) and 85 K (Fig 6.16). For the measurement made at room temperature, other than the slight difference in the response at 0.96μm there was no other significant change after heat treatment up to 5 minutes. However, when the spectral responses were measured at liquid nitrogen temperature, a difference in the band at 0.78 μm became apparent. In particular the response in this band was larger for the device on the Ag/Cr than it was for that on the SnO_x substrate. More importantly, by comparing this response with that in Fig 6.14 (which was not discussed earlier) the increase in the 0.78 μm band is seen to be much more pronounced after annealing in argon rather than in air for a device fabricated on Ag/Cr. Conversely using argon annealing for a device on tin oxide leads to a larger 0.96μm

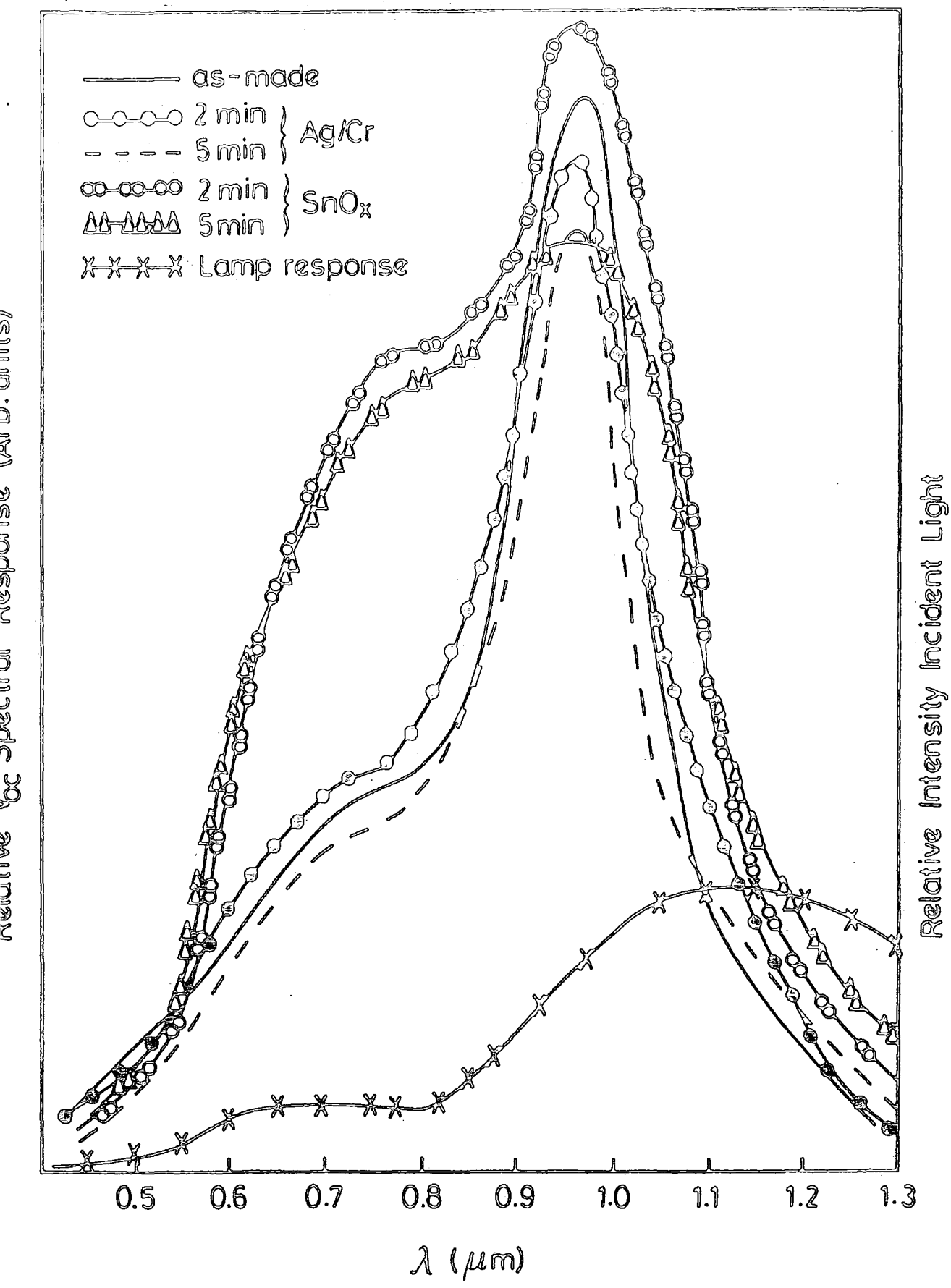

Fig 6.13 : Spectral responses (at 295 K) of heterojunctions formed on two different substrates with +0.1V electroplating bias after annealed in <u>air</u> for different periods.

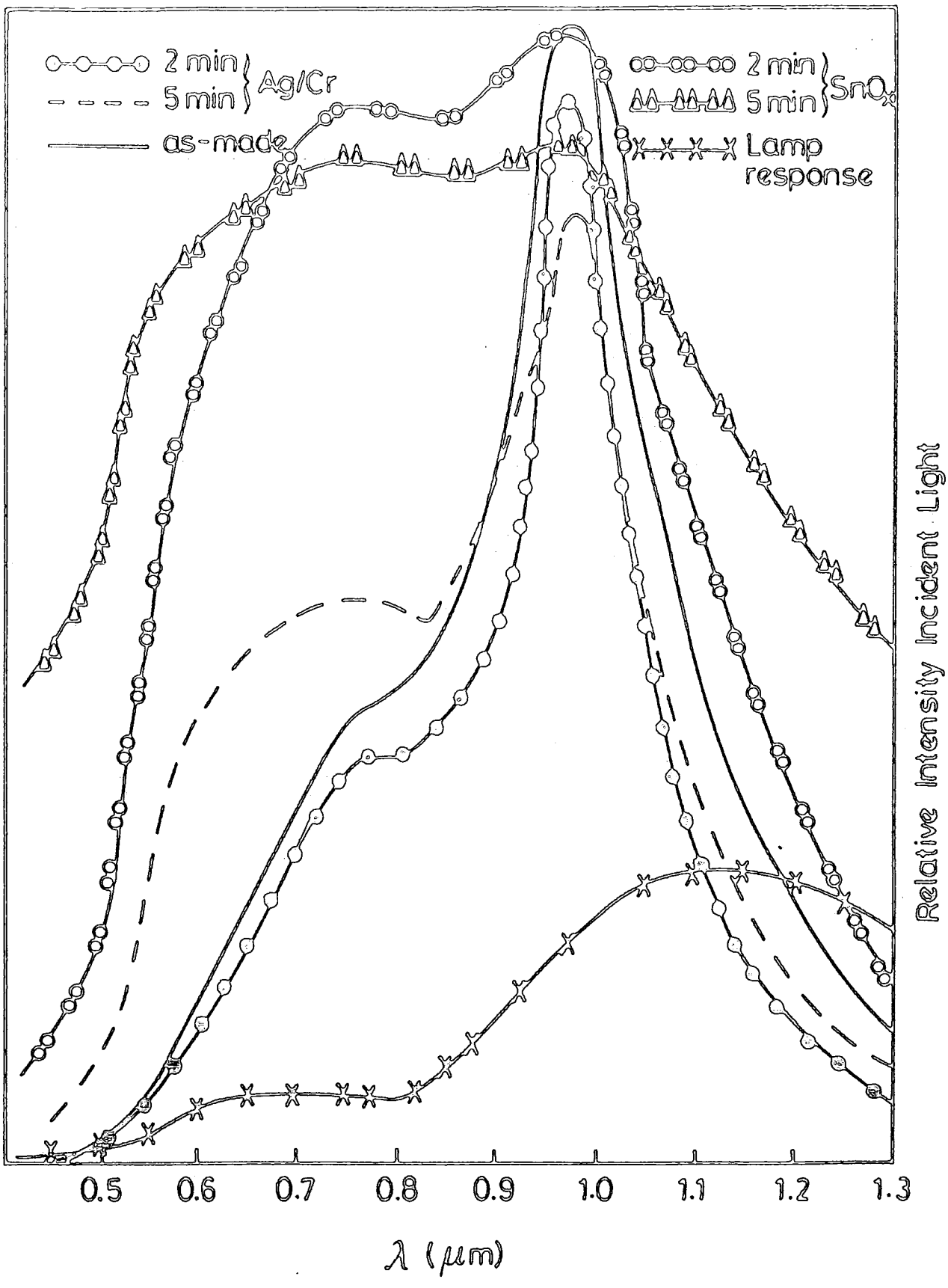

Fig 6.14 : Spectral responses at (85 K) of heterojunctions formed on two different substrates with +0.1V electroplating bias after annealing in air for different periods.

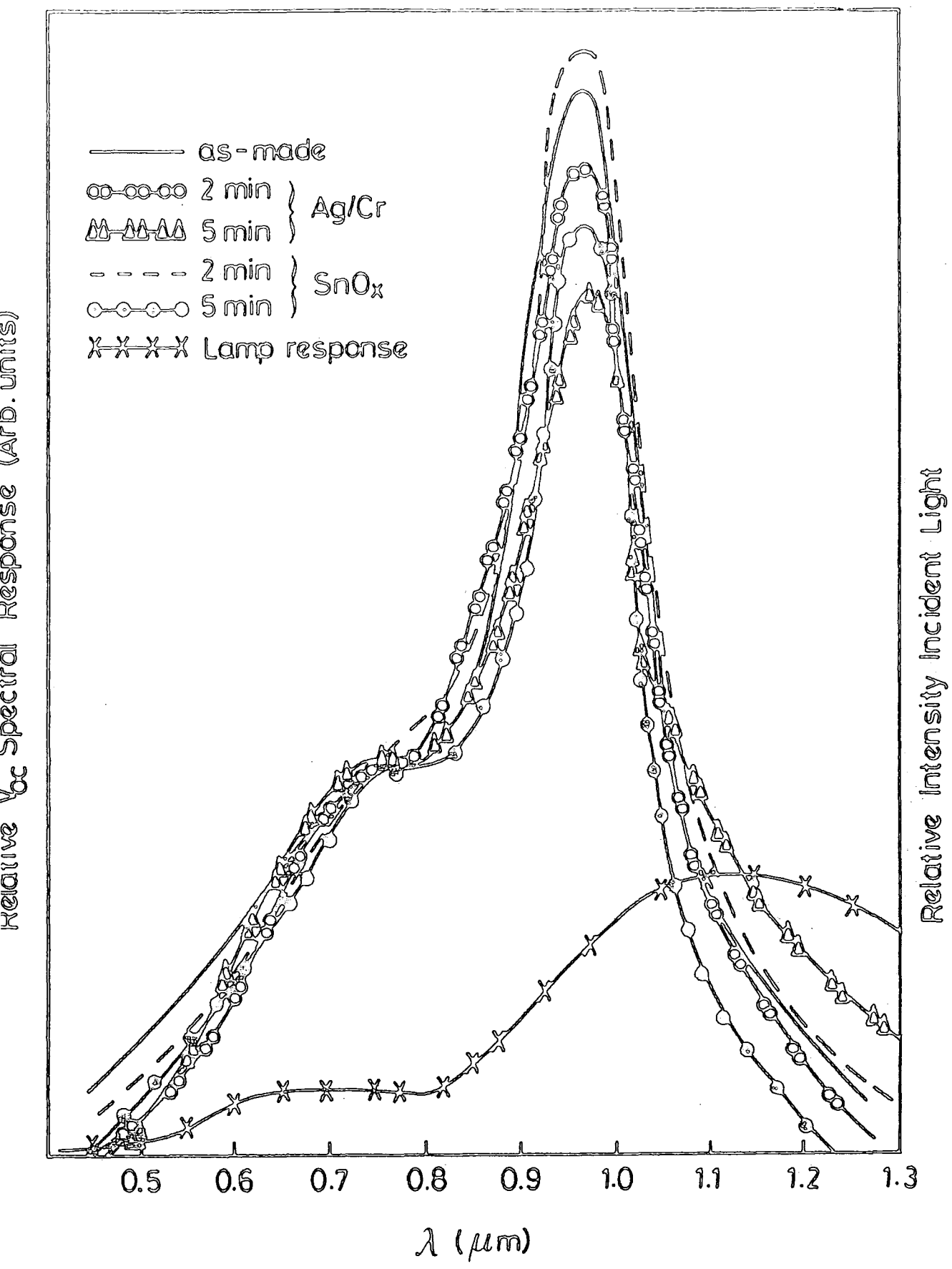

Fig 6.15 : V_{oc} spectral response (at 295 K) of two heterojunction devices fabricated on Ag/Cr and SnO_x with 0.1 V electroplating bias after annealing in Argon for different periods.

(chalcocite) response than does annealing in air.

For devices fabricated on CdS deposited on SnO_x substrates with +3.0V plating bias the spectral responses after heat treatment for 5 minutes and 10 minutes in argon and in air at 200°C are shown in Fig 6.17. Three peaks can be seen at 0.96, 0.67 and 0.49μm which correspond to a chalcocite, djurleite and the CdS bandgap response respectively. No response was observed at as-made condition. The most obvious feature in this figure is the diminished response of the chalcocite peak following 10 minutes annealing in air but not in argon. In addition, while further argon annealing only has a minimal effect on the bands at 0.67 and 0.95 μm, it reduces the CdS bandgap response by a factor of $\sim\frac{1}{3}$. On the other hand annealing in air leads to dominant peaks at 0.60 and 0.49 μm which may correspond to the absorption of light across the covellite [10] and the bandgap of CdS respectively. The effect of heating a device fabricated on Ag/Cr under the same conditions is shown in Fig 6.18. For heat treatment in both air and argon, three peaks lying at 0.96, 0.65 and 0.49 μm were observed. For devices on this substrate, the effect of the ambient was much less important. In this case it is the duration of the anneal which had most influence causing the overall response to increase irrespective of the ambient. The most significant difference between the responses from the annealed devices on SnO_x and Ag/Cr substrate concern the peak in the region of 0.6→0.7 μm. The position of this is independent of the ambient used in the heat treatment for devices on Ag/Cr substrates, whereas it occurs at 0.60 μm for air and at 0.67 μm for argon for devices on SnO_x.

6.5.3 Current-Voltage Characteristics

The I-V characteristics of the heterojunctions were measured in the as-made condition as a function of electroplating bias. These

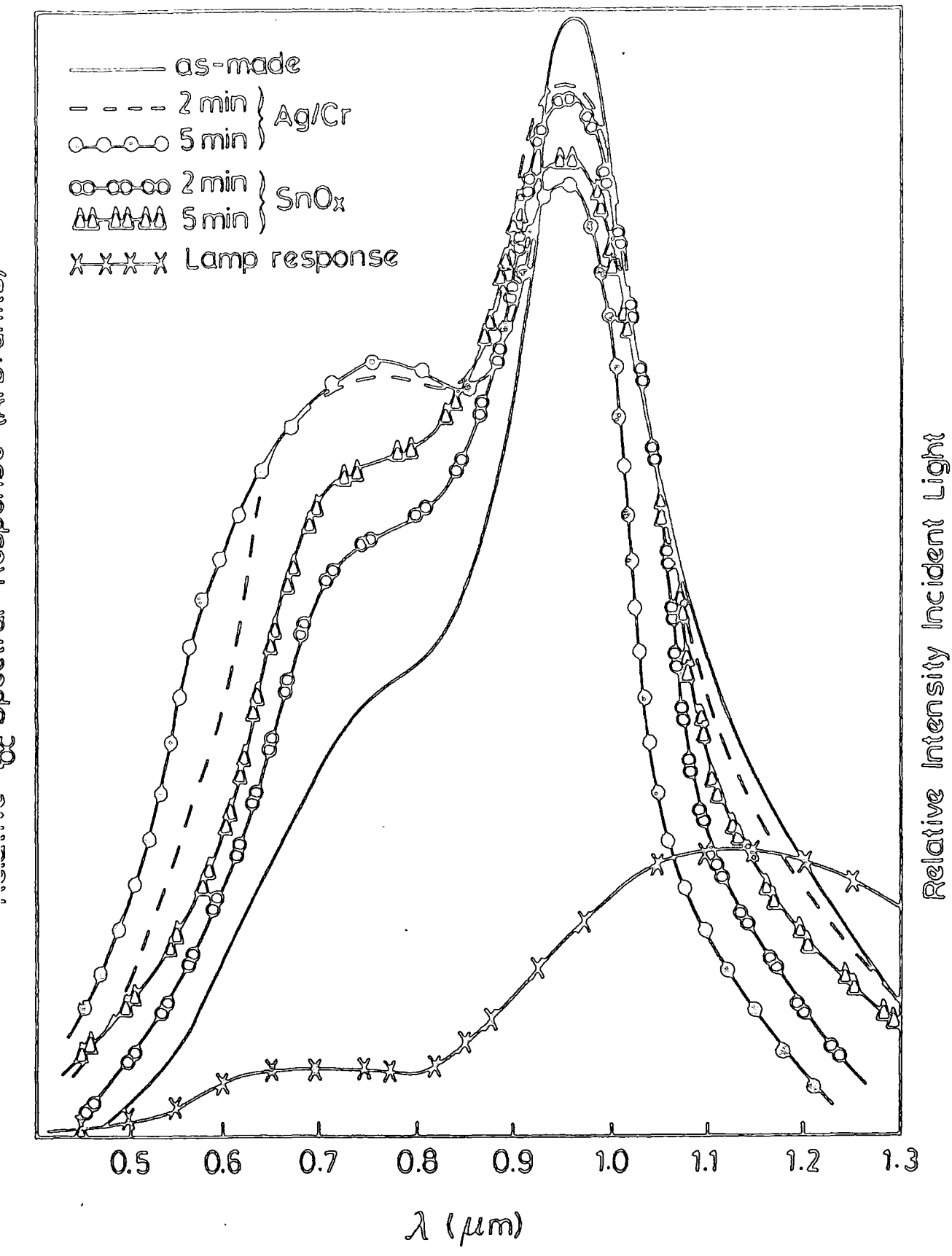

Fig 6.16 : V_{oc} spectral response (at 85K) of two heterojunction devices fabricated on Ag/Cr and SnO_x with +0.1V electroplating bias after annealing in Argon for different periods.

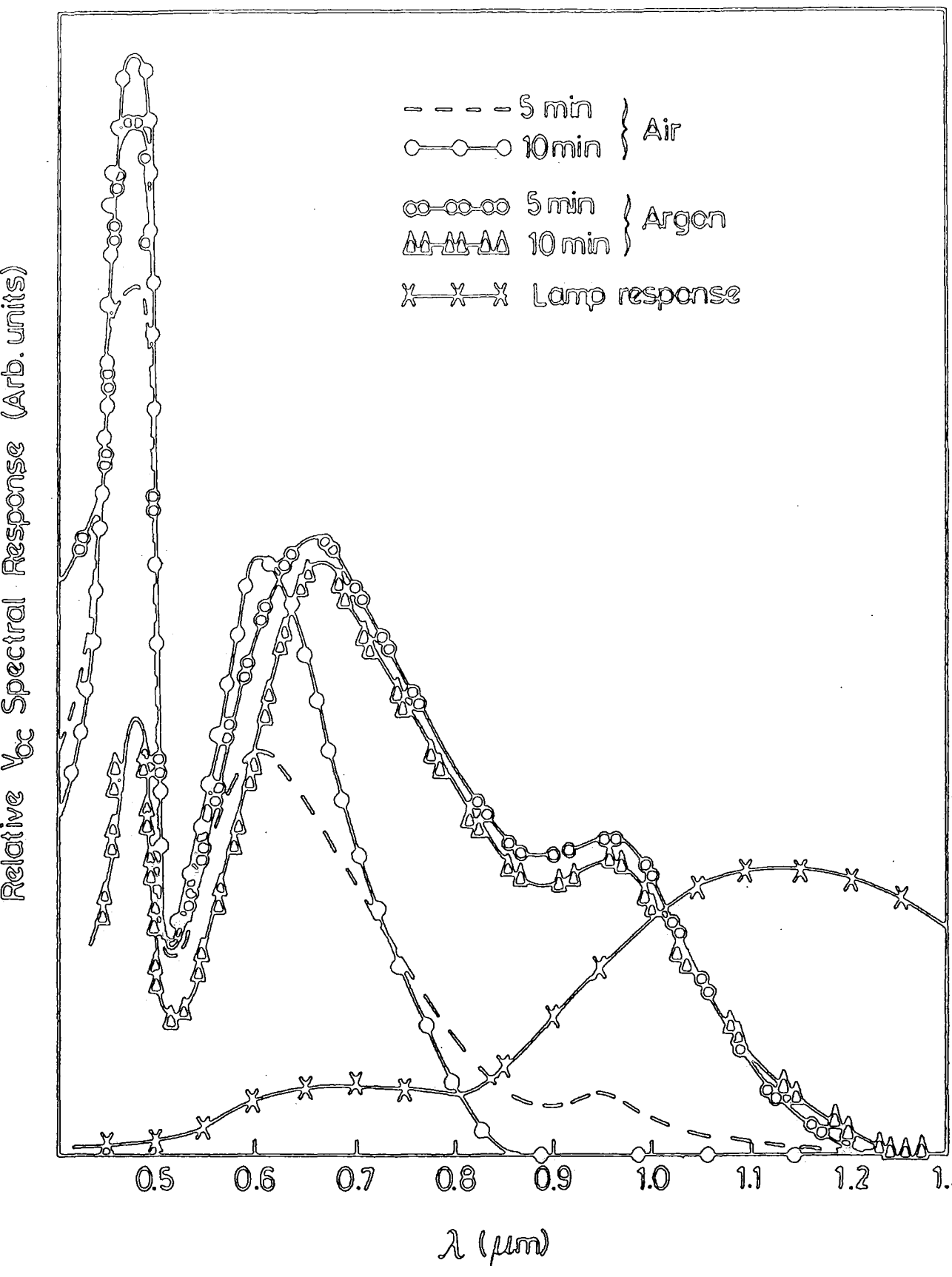

Fig 6.17 : Spectral response (at 85K) of devices fabricated on SnO_x substrate with +3.0V electroplating bias and heat treated separately in Argon and in Air.

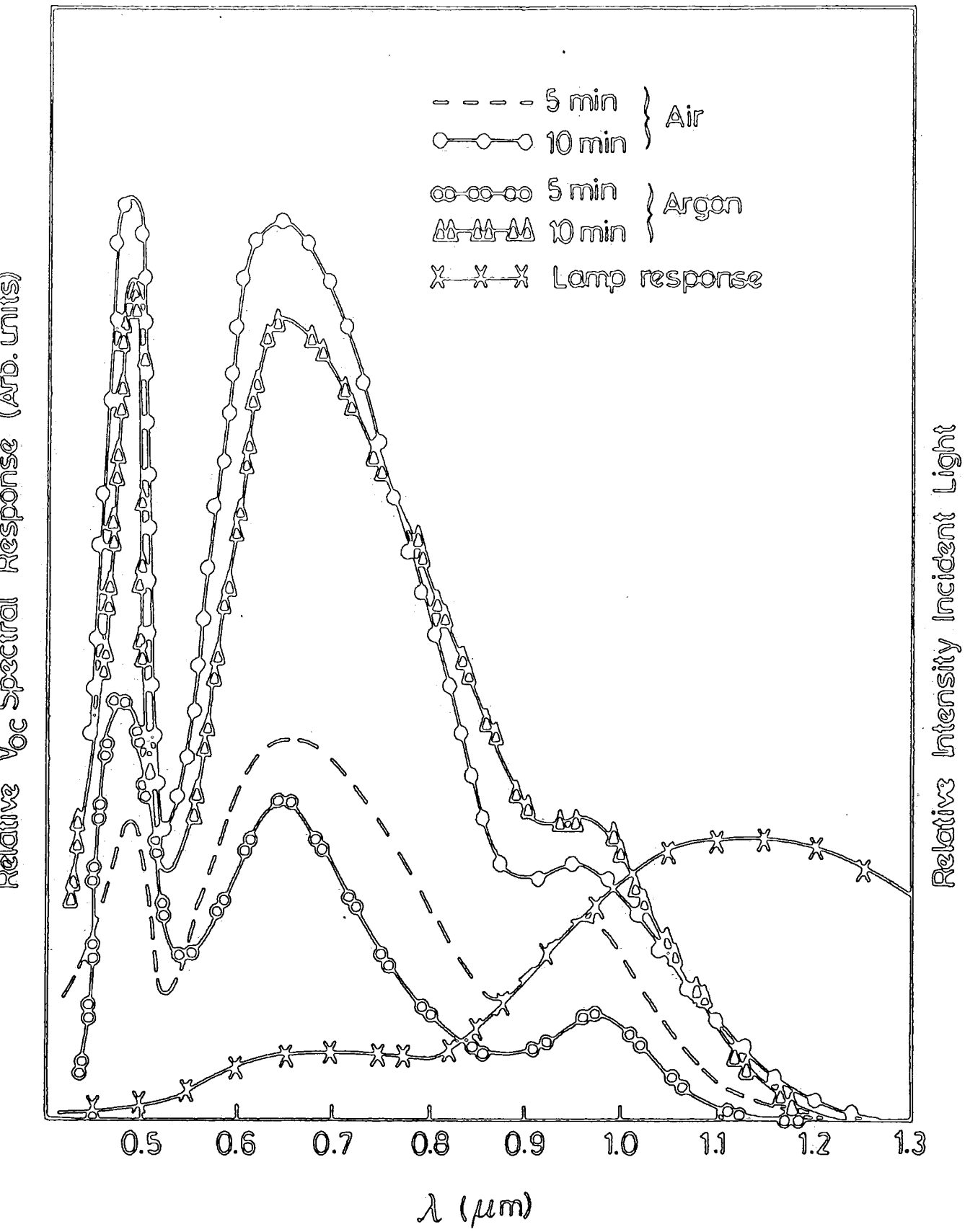

Fig 6.18 : Spectral response (at 85K) of devices fabricated on Ag/Cr substrate with +3.0V electroplating bias and heat treated separately in Air and Argon.

measurements were repeated after heat treatment in air and in argon. The typical I-V characteristics of as-made devices as a function of plating bias (Fig 6.19) show that the best diode junction parameters of V_{oc} = 0.37 V and I_{sc} = 7.3mA.cm^{-2} were using a plating bias of +0.1V. Devices prepared with all of the other plating potentials investigated exhibited poor characteristics and operational parameters. It is important to note that for as-plated device there was no difference between diodes on Ag/Cr and SnO_x substrates. Figure 6.20 shows that the I-V characteristics of devices prepared on films deposited on SnO_x substrates using the optimum plating potential became very resistive after heat treatment in air at 200^{o}C for different periods of time. In particular the forward bias cross-over between the light and dark current voltage curves became more pronounced with increased duration of annealing. This can be attributed to the formation of an i-layer at the heterojunction interface resulting from the diffusion of copper from the Cu_2S to the CdS. The curves also show a deterioration in I_{sc} and FF, with a high leakage current occuring after a 2 minute heat treatment. In contrast, annealing in argon leads to a reduction in both the extent of copper diffusion and in the resistance of these devices Fig 6.21. The effective parameters were slightly improved after a 2 minute anneal but further heating led to a reduced I_{sc} and FF. On the other hand quite different behaviour was observed for devices prepared on Ag/Cr. The I-V characteristics for these devices are shown in Fig 6.22 which demonstrates that all the parameters were slightly increased and that there was only a small amount of copper diffusion leading to a correspondingly small increase in the device resistance following annealing in air. Heat treatment for 5 minutes results in a slight decrease in I_{sc}, which shows the improved stability of devices fabricated on Ag/Cr substrates. Fig 6.23 illustrates the effect of argon annealing

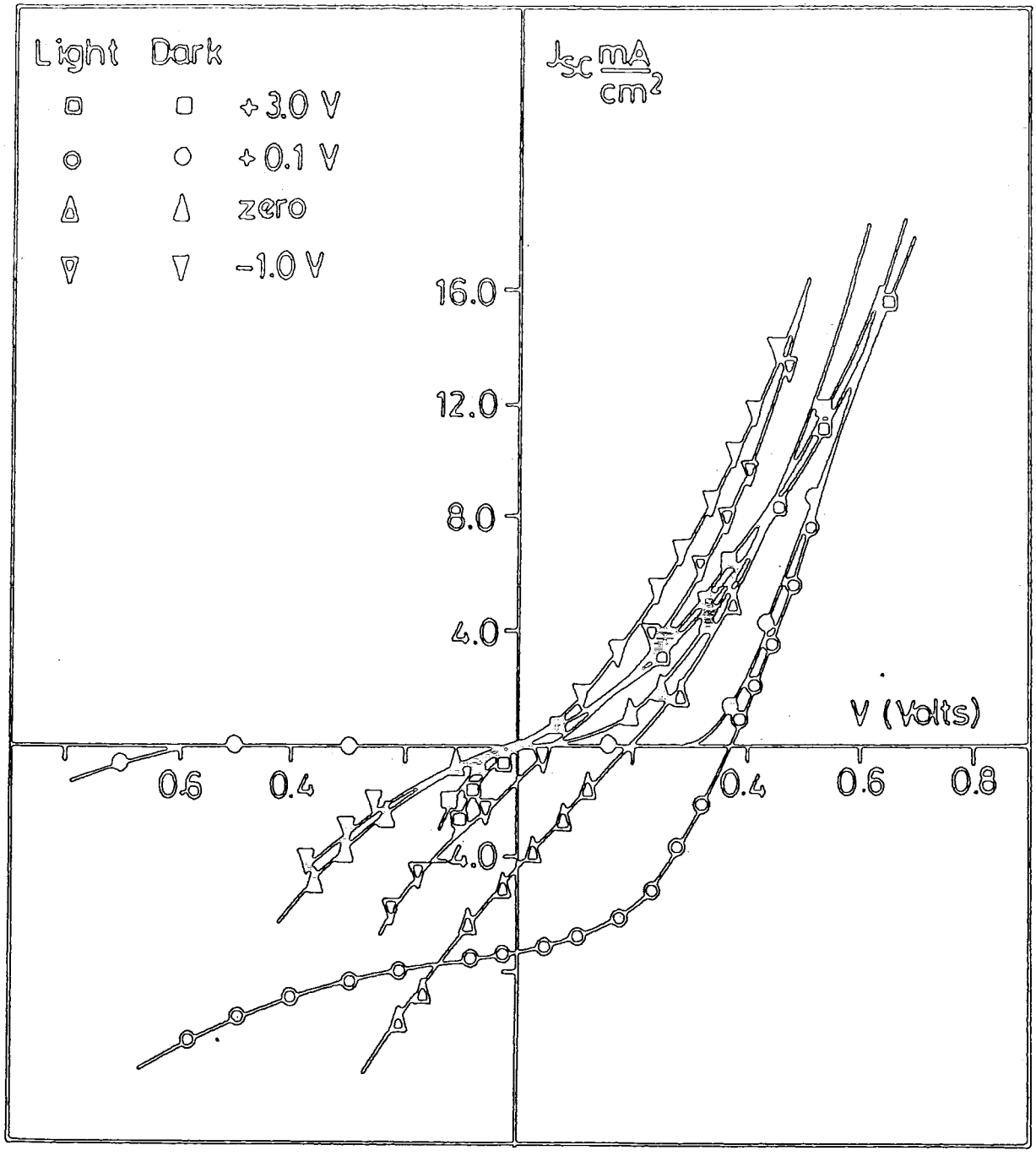

Fig 6.19 : J-V characteristics of as-made CdS-Cu_xS prepared by the electroplating technique with the biases shown.

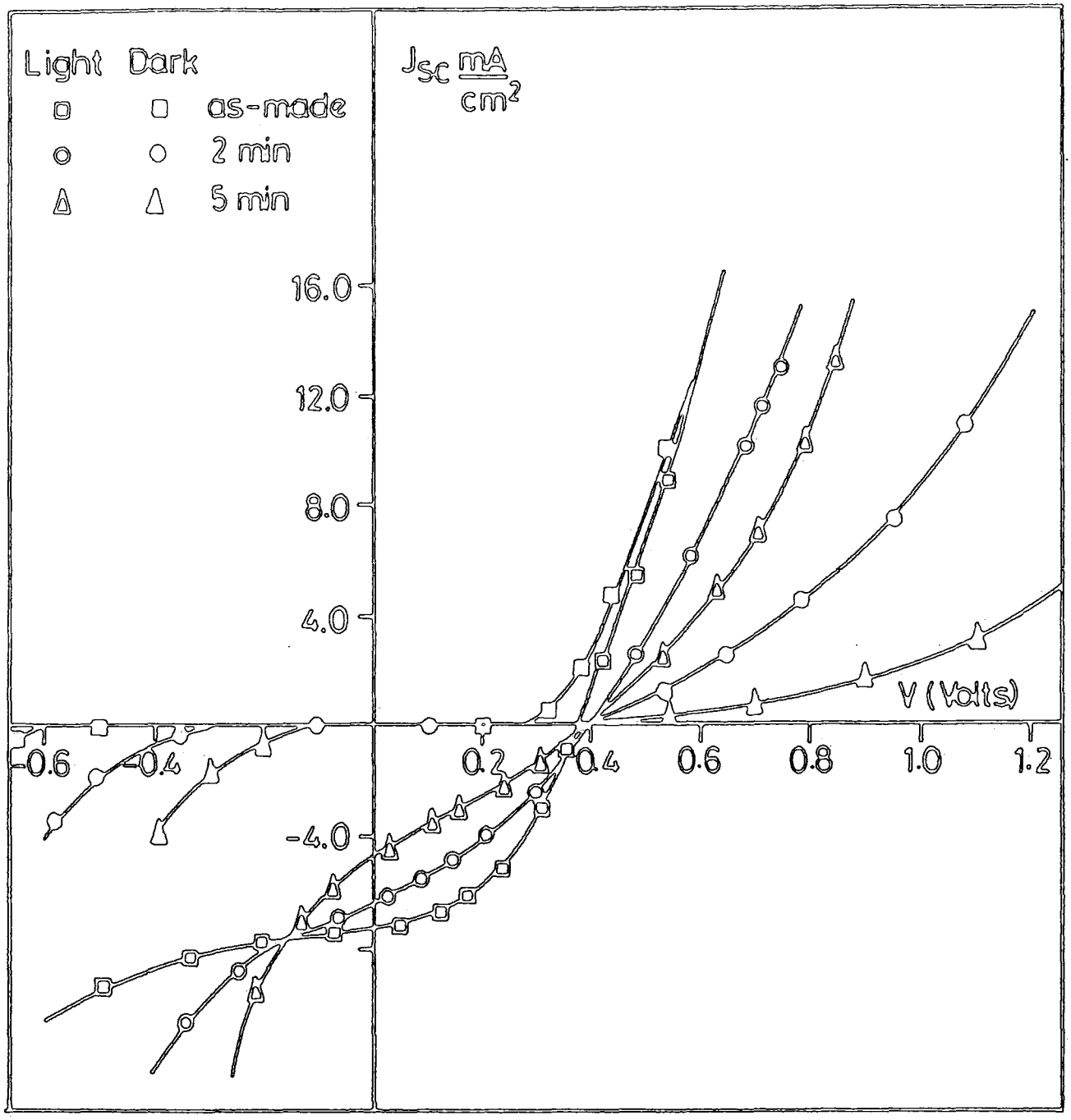

Fig 6.20 : J-V characteristics of CdS-Cu_2S prepared with +0.1V electroplating bias on SnO_x substrate as a function of Air annealing.

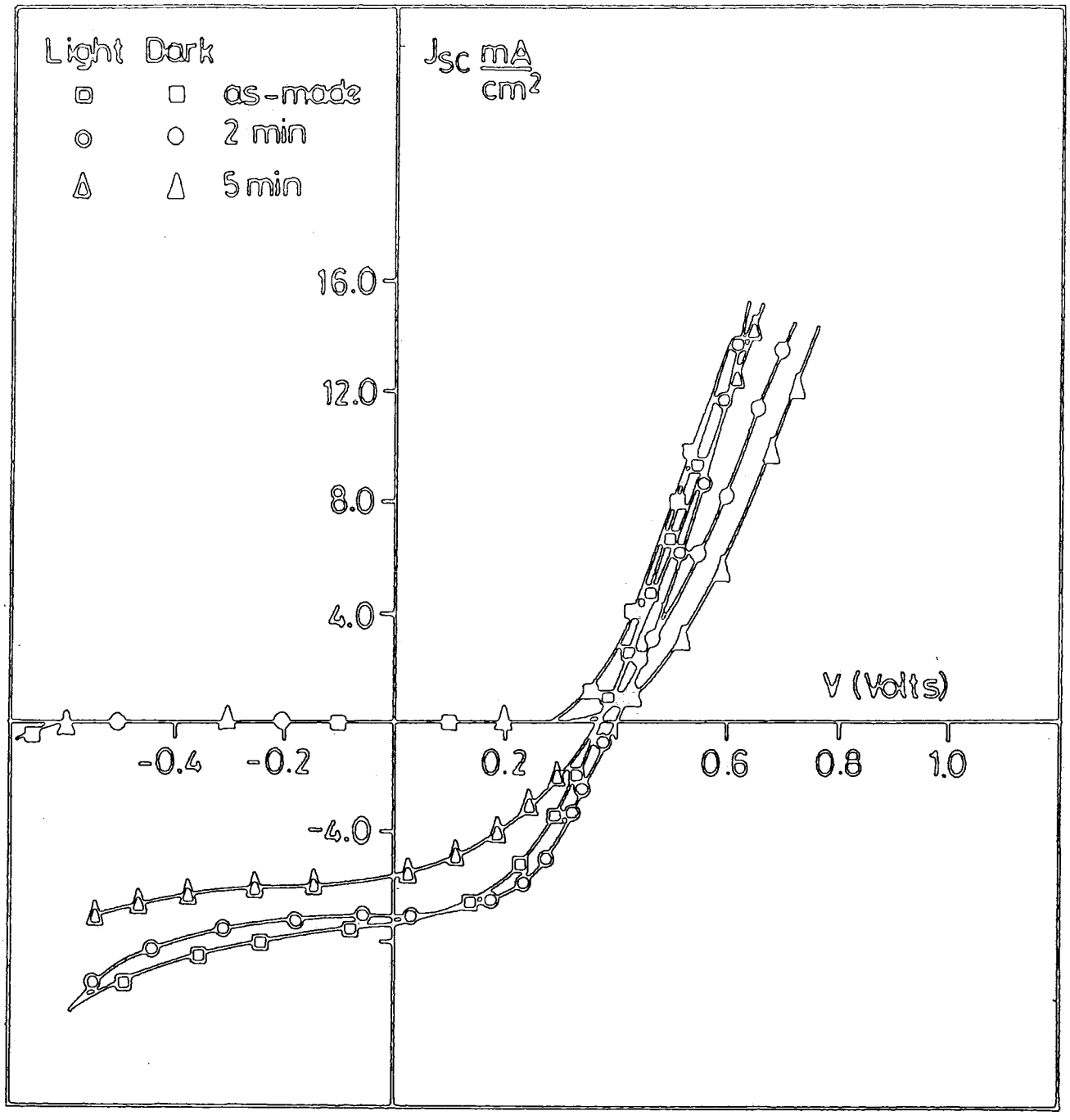

Fig 6.21 : J-V characteristics of a CdS-Cu_2S prepared with +0.1V electroplating bias on SnO_x substrate as a function of Argon annealing.

on a device made on Ag/Cr. After 2 minutes heat treatment there is a slight reduction in I_{sc} while the other parameters remained unchanged. However, further heating causes a significant reduction in I_{sc}.

For the sake of completeness annealing has been carried out on devices prepared with -1.0V plating bias which have a djurleite phase. Although very poor I_{sc} and V_{oc} values were found in the as-made condition for devices on both Ag/Cr and SnO_x substrates, these device parameters did improve after heat treatment. Figures 6.24 and 6.25 show an improvement of V_{oc} to 0.325 and 0.22V and I_{sc} to 2.8 and 1.3mA.cm^{-2} following air annealing of devices on Ag/Cr and SnO_x respectively. Further the devices fabricated on SnO_x substrates become very resistive with air heat treatment while those on Ag/Cr do not. Siu and Kowk [11] found that by using tin oxide substrates the dark resistance was increased by extending the heat treatment. It may be concluded therefore that the presence of silver may play a role in improving the stability of the Ag/Cr devices. Further using air as an ambient leads to hard characteristics and more improvement for devices on Ag/Cr than for those on SnO_x.

Figures 6.26 and 6.27 show the effect of argon annealing on devices prepared under the same conditions as those for which the result of air annealing have just been described. The resistance for Ag/Cr devices after argon annealing was very similar to that produced by air annealing. In contrast, for SnO_x substrates, the resistance values of the devices were reduced by annealing in argon. Consequently the use of argon was more beneficial for SnO_x devices and led to harder characteristics, unlike the soft ones obtained by argon annealing Ag/Cr devices. For the same argon annealing V_{oc} was increased to 0.23 and 0.335V and I_{sc} to 0.27 and 0.23 mA.cm^{-2} for devices on the Ag/Cr and SnO_x substrate respectively.

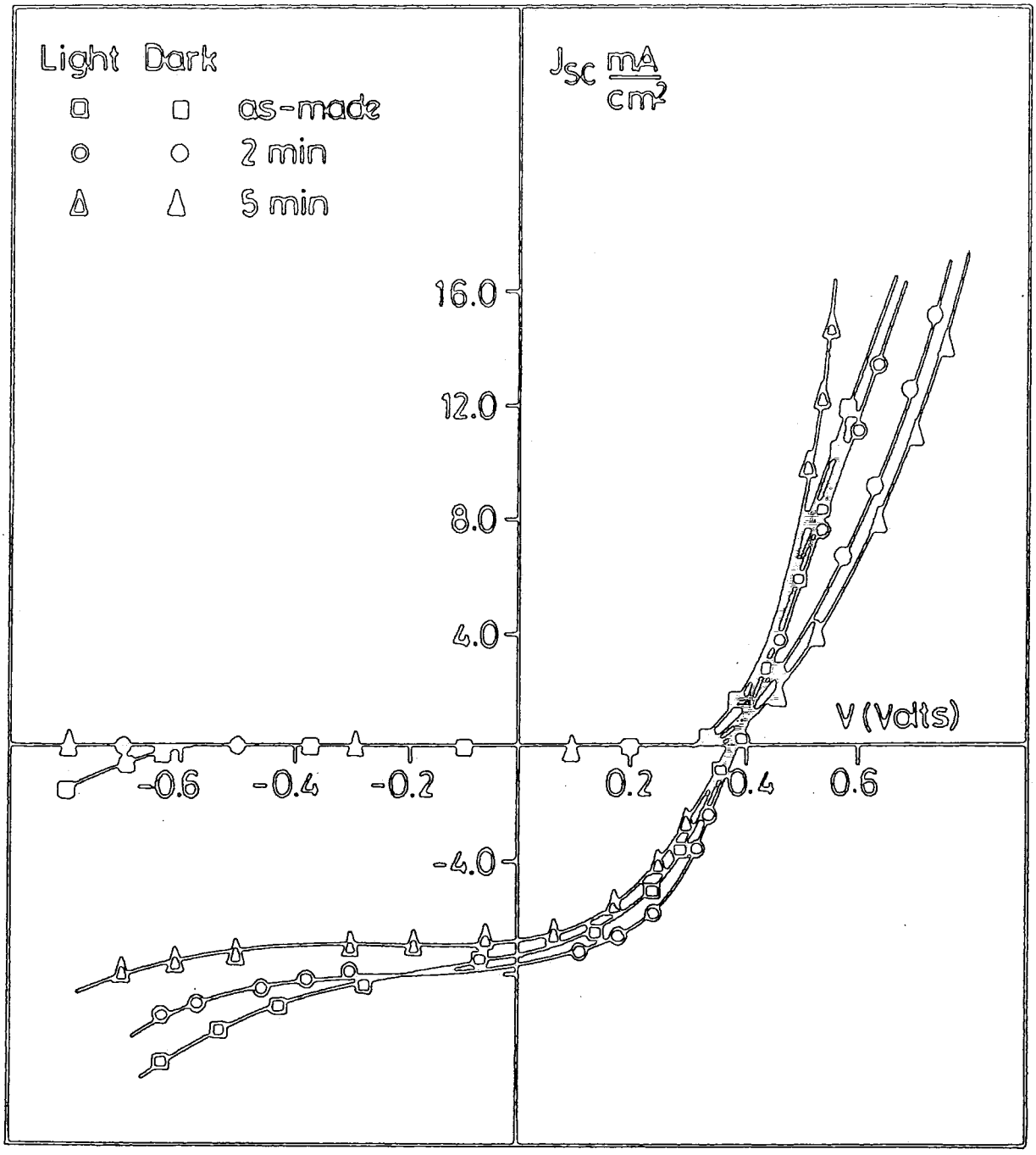

Fig 6.22 : J-V characteristics of a CdS-Cu_2S prepared with +0.1 V electroplating bias on Ag/Cr substrate as a function of Air annealing.

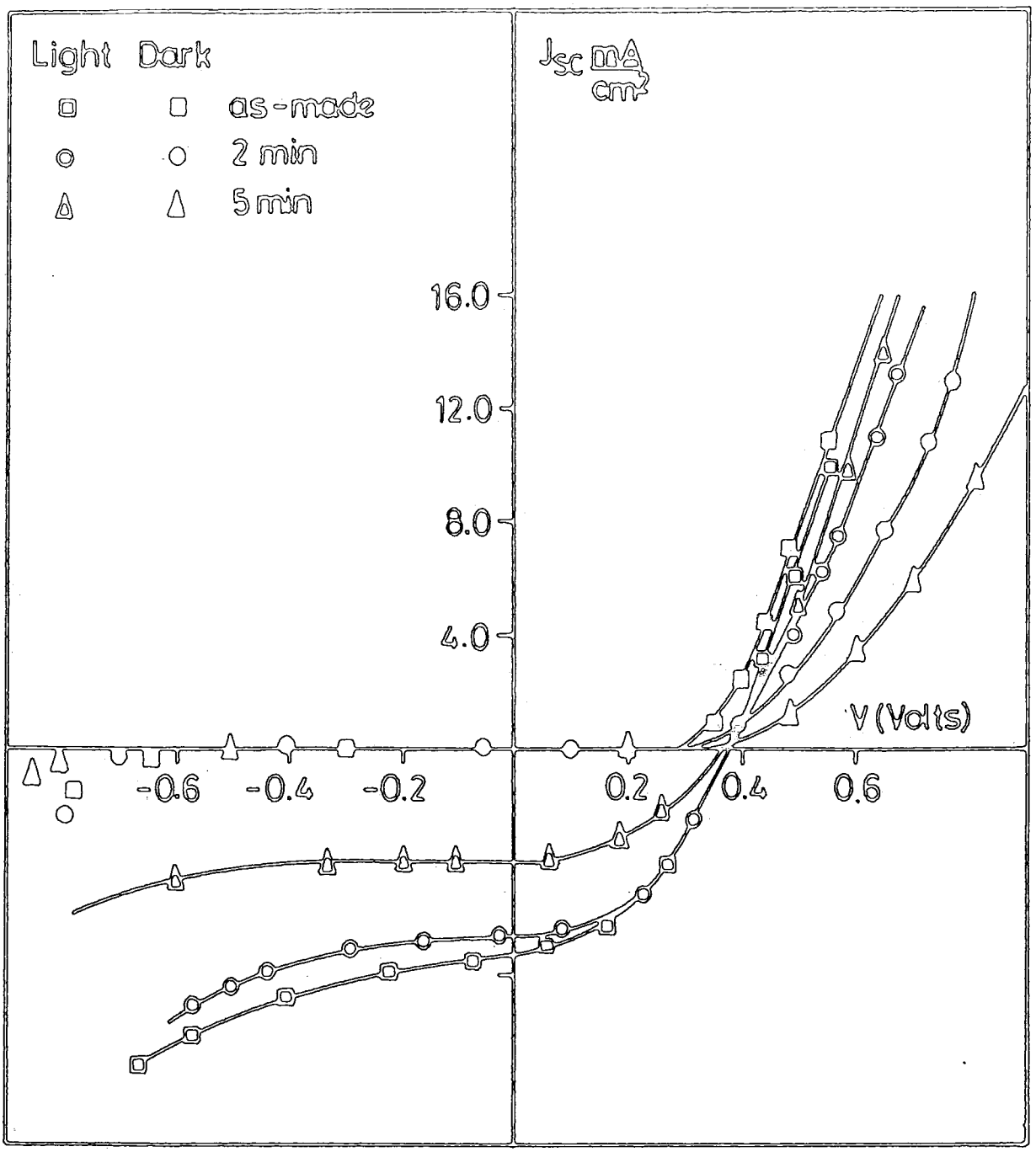

Fig 6.23 : J-V characteristics of a CdS-Cu_2S prepared with +0.1V electroplating bias on Ag/Cr substrate as a function of Argon annealing.

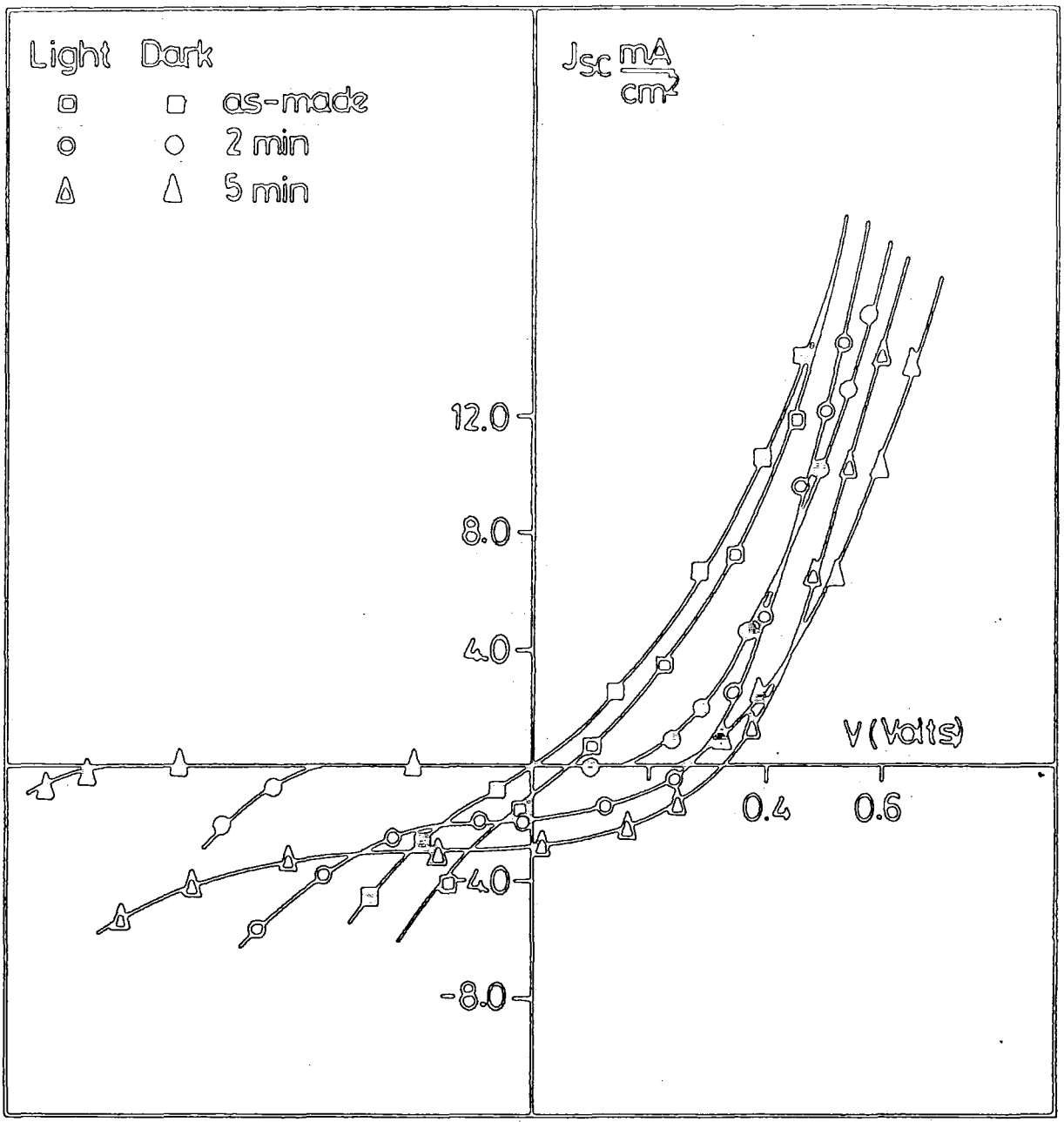

Fig 6.24 : J-V characteristics of CdS-Cu_xS formed on Ag/Cr substrate with -1.0V after annealing in Air for different periods.

In summary argon annealing of devices on SnO_x substrates having a djurleite phase, caused a five-fold increase in V_{oc} and a two-fold increase in I_{sc}. In comparison there was a three-fold increase in V_{oc} but I_{sc} was not affected when air was used as the annealing ambient. However, for a device fabricated on Ag/Cr, V_{oc} increased five-fold and I_{sc} two-fold when air was used. For devices on Ag/Cr a similar result was found when the annealing is carried out in argon except that the increase in V_{oc} was only three-fold.

The variation in the effective parameters V_{oc}, I_{sc}, FF and γ for predominantly djurleite and chalcocite devices in their as-made condition and 2 and 5 minute annealing separately in argon and in air for devices fabricated on SnO_x and Ag/Cr substrates are listed in Tables 6.2 and 6.3.

The devices	V_{oc} (V)	I_{sc} ($mA.cm^{-2}$)	FF	γ(%)
As-made	0.065	1.20	0.22	0.017
SnO_x 2 min Air annealing	0.19	0.80	0.32	0.048
SnO_x 5 min Air annealing	0.22	1.30	0.31	0.088
SnO_x 2 min Argon annealing	0.275	1.90	0.29	0.15
SnO_x 5 min Argon annealing	0.335	2.3	0.41	0.31
Ag/Cr 2 min Air annealing	0.275	1.90	0.34	0.177
Ag/Cr 5 min Air annealing	0.325	2.80	0.40	0.37
Ag/Cr 2 min Argon annealing	0.17	2.30	0.28	0.11
Ag/Cr 5 min Argon annealing	0.23	2.70	0.32	0.20

TABLE 6.2

The junction parameters for CdS-$Cu_{1.96}S$ before and after 2 and 5 minute annealing in argon or in air for devices on SnO_x or Ag/Cr substrate.

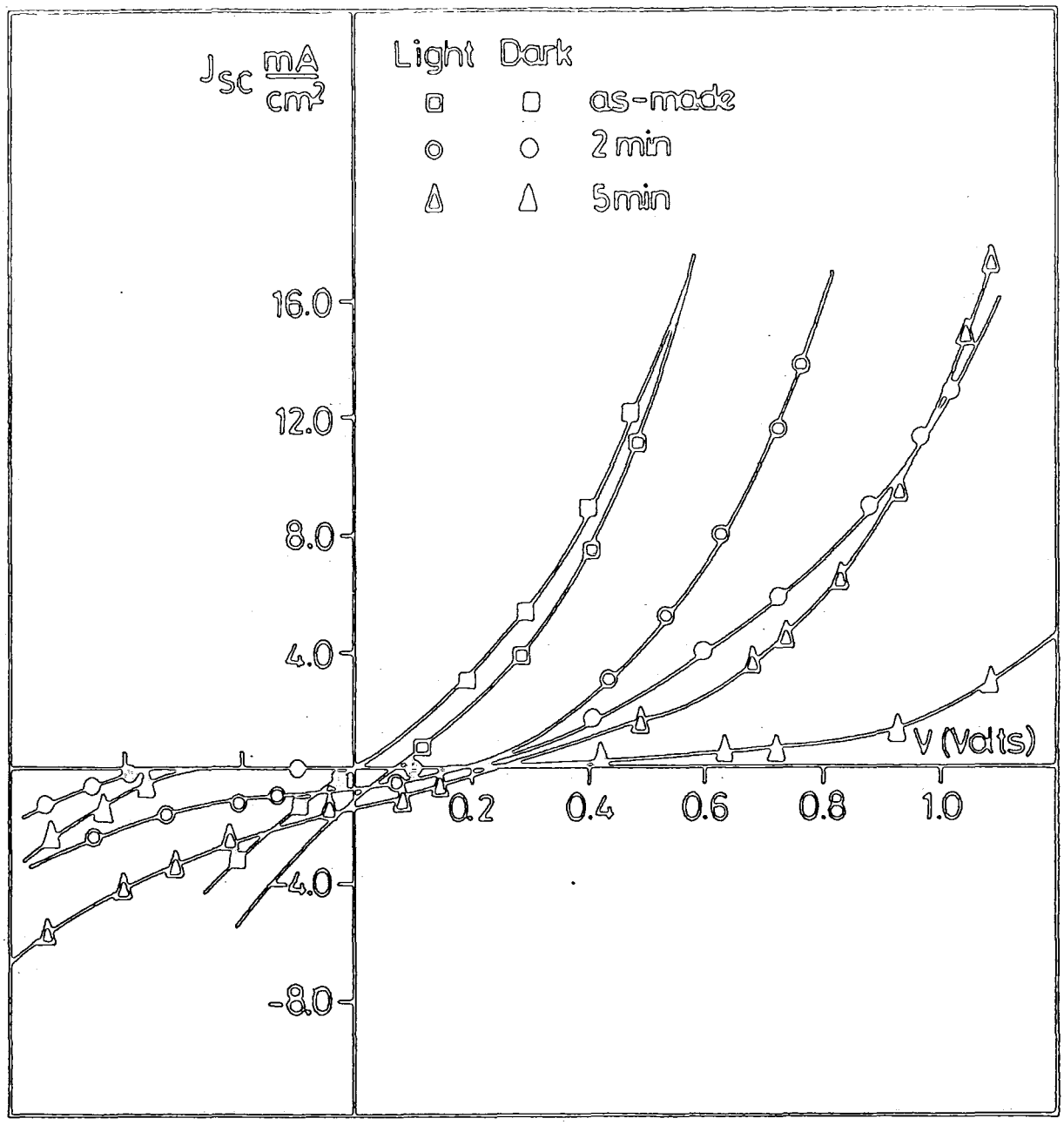

Fig 6.25 : J-V characteristics of CdS-Cu_xS formed on $\underline{SnO_x}$ with -1.0V electroplating bias after annealing in $\underline{Air}$ for different periods.

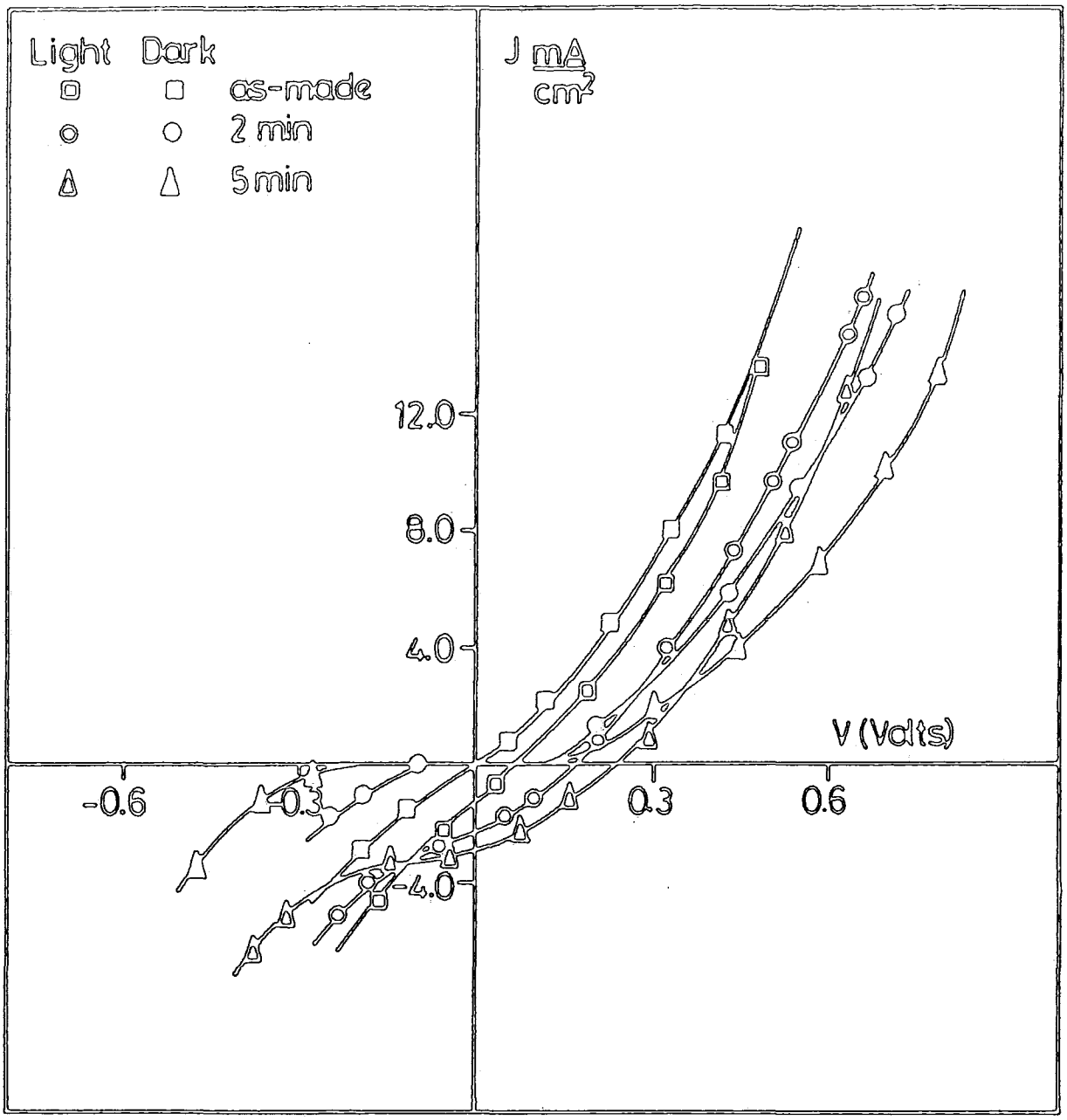

Fig 6.26 : J-V characteristics of CdS-Cu_xS formed on Ag/Cr with -1.0V electroplating bias after annealing in Argon for different periods.

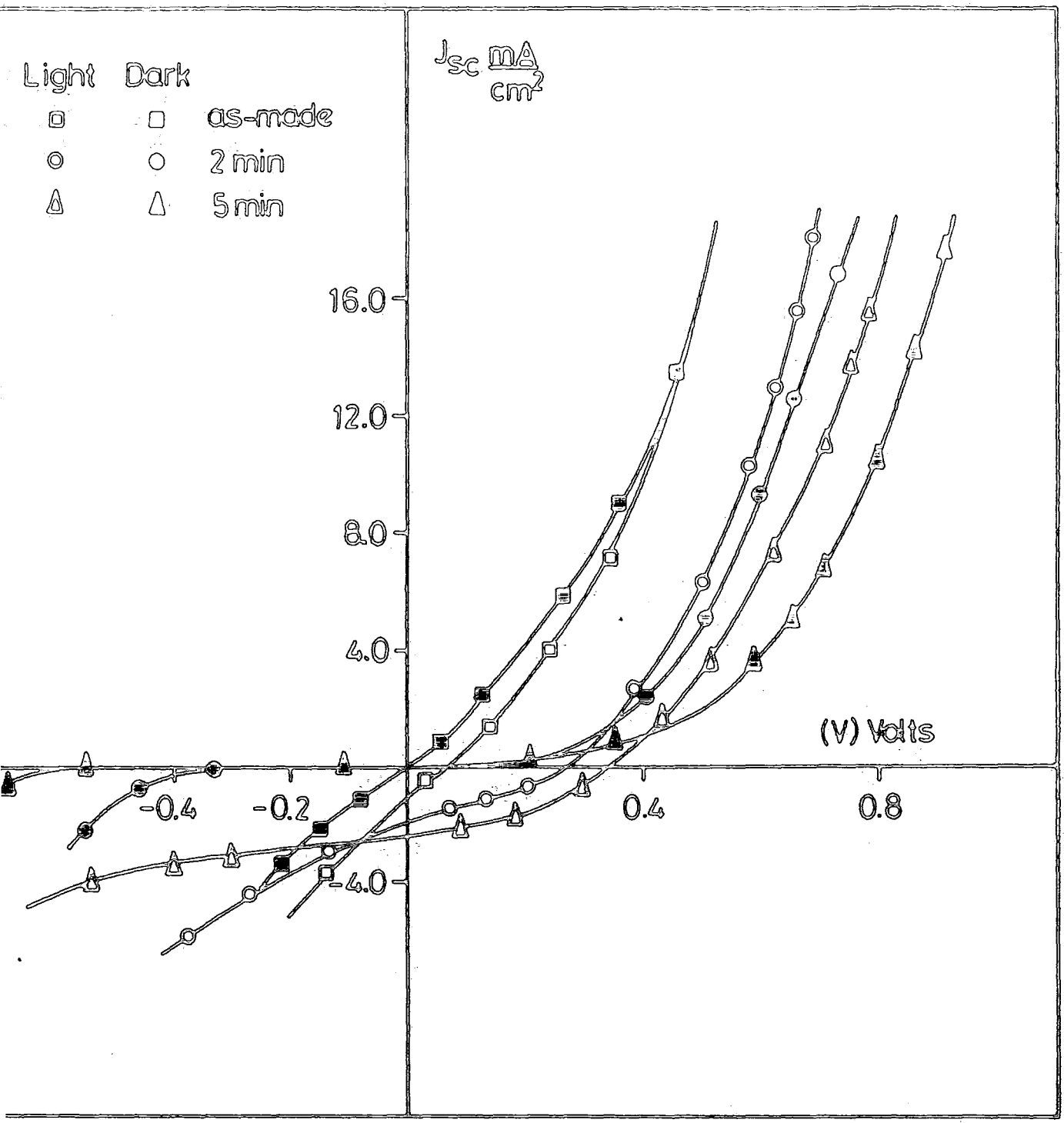

Fig 6.27 : J-V characteristics of CdS-Cu_xS formed on $\underline{SnO_x}$ substrate with -1.0V electroplating bias after Argon annealing for different periods.

The devices	V_{oc} (V)	I_{sc} ($mA.cm^{-2}$)	FF	γ(%)
As-made	0.37	7.30	0.43	1.16
SnO_x 2 min Air annealing	0.39	6.50	0.32	0.82
5 min Air annealing	0.39	4.70	0.27	0.49
SnO_x 2 min Argon annealing	0.40	7.00	0.49	1.37
5 min Argon annealing	0.37	5.50	0.37	0.75
Ag/Cr 2 min Air annealing	0.38	7.60	0.47	1.35
5 min Air annealing	0.37	6.80	0.41	1.03
Ag/Cr 2 min Argon annealing	0.38	6.60	0.48	1.20
5 min Argon annealing	0.37	4.00	0.40	0.59

TABLE 6.3

The junction parameters for CdS-Cu_2S before and after 2 and 5 minute annealing in argon or in air for devices on SnO_x or Ag/Cr substrate.

The effects of similar annealing on the I-V characteristics of devices fabricated with a plating potential of +3.0V have been also studied. While similar trends were observed the inherent inferior parameters do not justify discussion here.

6.6 Discussion Of Results

In the last two decades much work has been carried out on the development and investigation of thermally evaporated cadmium sulphide films, and their application to photovoltaic conversion of solar energy [12,13,14,15,16]. The preparation of thermally evaporated CdS layers has been reviewed by Stanley [17] and Hill [18].

Several workers have recommended the electroplating method for

the production of the chalcocite phase of copper sulphide [19,20,21]. The use of electrochemical techniques also has advantages which improve the control of the process technology without degrading the cell properties [22]. This work described the different conditions under which copper sulphide phases can be formed, and the effect on the properties of the devices of the substrate material upon which the CdS was grown. Annealing in different ambients for different periods of time has also been carried out.

The process of CdS film growth by thermal evaporation is based on the dissociation of CdS into Cd and S_2 vapours [23] which then condense on the substrate and recombine. During the evaporation cycle, the substrate and source temperatures play an important part in controlling the crystallinity of the film which in turn affects its electrical properties [2,24].

During this study, RHEED patterns showed that different phases of copper sulphide were obtained according to the value of the plating bias which was used during topotaxial growth. In Fig 6.7 the distance between two adjacent diffraction spots from the phase of Cu_xS is a quarter of the separation between intense spots from the underlying CdS. This observation is consistant with the presence of a topotaxial layer of chalcocite on the CdS. On the other hand applying -1.0V led to the pattern which contained a series of diffraction arcs/lines lying parallel to the shadow edge of the sample (Fig 6.8). This pattern may be due to a djurleite phase. A polycrystalline covellite phase was identified after applying a bias potential of +3.0V (Fig 6.10). These phases were confirmed by measuring the interplanar spacing which agreed with the A.S.T.M. index data. Leon and Argona [25] have produced different phases of Cu_xS thin films by controlling the concentration and temperature of the plating solution, the dipping time and the film

thickness. As was discussed in Chapter Five the principle of the electroplating technique is to control the ion-exchange ratio during the growth of copper sulphide. A bias potential of +0.1V was found to produce the chalcocite phase of Cu_xS for CdS-Cu_2S thin film solar cells. The optimum bias voltage was larger than that found for a device fabricated on a single crystal substrate. This may be due to the fact that the growth of copper sulphide on a CdS substrate in an ion exchange reaction is dependent on many factors including

i) the relative Cd to S composition at the CdS surface [26],

ii) the CdS morphology [27], and

iii) the grain boundary structure [27,28].

The effects of these parameters as well as the thickness of the CdS film is likely to make the plating of thin film material different from that of single crystals. Nevertheless the control of the kinetics of the Cu^+ and Cd^{++} ions during the topotaxial growth depends on the value of the applied bias. Without bias the replacement of one Cd^{++} ion from the CdS by two Cu^+ ions from the $CuCl_2$ solution leads to the formation of cadmium chloride which dissolves back into the solution. In contrast, using a bias during plating causes the displaced Cd^{++} ions to accumulate at the growing Cu_xS layer on the inside of the CdS film instead of migrating out into the $CdCl_2$ solution. The accumulation of a Cd^{++} ion layer provides a barrier against the deeper penetration of Cu^+ ions and hence more Cu^+ ions are combined in the bulk of the grown Cu_xS layer. The large difference in the thickness between single crystal and thin film substrates may necessitate the use of a higher value of bias in the plating of thin films in order to build up a Cd^{++} ion barrier to prevent the migration of Cu into grain boundaries. It has previously been demonstrated that the growth of Cu_xS along the CdS grain boundaries can be limited by the electroplating technique, [29,30].

The effect of increasing the plating bias to +3.0V probably causes the Cu^{+} ions to accelerate from the solution to the CdS lattice, which may cause breaches in the Cd^{++} barrier and allow Cu_xS to develop at greater depths along the grain boundaries leading to shunting paths [6,31,32]. The application of a plating bias of -2.0V leads to a reduction in the velocity of the ion exchange [33], with the result that a thinner disordered phase is produced as is evidenced by the polycrystalline rings (Fig 6.9). Heat treatment has been considered by several workers: Te Velde [34] found annealing to be essential for optimisation of a device, Bryan et al [35] found the presence of oxygen during fabrication to be beneficial. Burton and Wandow [36] and Massicot [37] suggested that the use of oxygen either during fabrication or operation leads to a change in the stoichiometry from chalcocite to djurleite. It has been shown in this work that when devices fabricated on CdS deposited on SnO_x are annealed in air the Cu_2S is converted to the lower copper sulphide phase $Cu_{1.96}S$ which has a response at energy band 1.8eV, whereas no similar effect occurs for devices fabricated on Ag/Cr (see Figs 6.13 and 6.14). Heat treatment causes Cu to diffuse from the Cu_xS to the CdS layer to form an i-layer at the heterojunction interface. This leads to a reduction in the copper content of Cu_xS layer [2,11]. Also during oxygen heat treatment, the oxygen diffuses to the interface region where it can reduce the sensitivity by increasing the density of interface states[38]. However, Figures 6.13 and 6.14 showed that the diffusion of copper in CdS on a device fabricated on Ag/Cr was less than for devices prepared on SnO_x and the major response was still at 0.96μm even after heat treatment. This is attributed to the presence of silver inhibiting the diffusion of copper. Pfisterer and Bloss [39] found that the advantage of using silver was that it limited short circuiting. Using photocapacitance

measurements Pande et al [24] detected a new electron trap which was located at 0.95eV below the conduction bad on devices prepared on silver based substrate. Furthermore, this trap was shown to inhibit the diffusion of copper in CdS. They also found that after air heat treatment of a device formed on films on SnO_x coated glass, a small response at 0.65 μm was obtained. This was associated with copper, and, consistent with the present result no such response was detected in devices formed on Ag/Cr substrates. It was demonstrated that this trap arises from the combined presence of silver and oxygen probably forming some complex associate in CdS.

The use of argon reduces the effect of Cu diffusion in the device formed on an SnO_x substrate in comparison with air annealing (see Figs 6.13 and 6.15). This may be attributed to loss of sulphur from the surface when compared with Ag/Cr device, the increase in the copper diffusion for these cells may be attributed to the presence of argon reducing the inhibiting effects of silver. So during argon annealing two competing processes are operative;

i) heat treatment in argon removes sulphur from the Cu_xS layer i.e. increases the copper content;

ii) the inhibiting effects of silver on copper diffusion are reduced by argon.

The net result depends on which of these two effects is dominant.

The appearance of three peaks on the spectral response of a device fabricated on SnO_x with +3.0V after heat treatment (Figs 6.17 and 6.18) although no response was obtained in the as-made condition indicated that an improvement in stoichiometry had been produced. The reduction of the peak at 0.49 μm with increasing annealing time enhanced the improvement of the stoichiometry after argon heat treatment. In contrast, using air gave a different result. While a small peak appeared at

electrons are tunneling from the bottom of CdS conduction band and are shunted by ohmic conduction through the Cu_xS which had formed along the grain boundaries [6]. On the other hand, using a lower bias leads to more control of the diffusion of ions which causes a thin layer of Cu_xS to be grown.

Further support for the different diffusion of copper from Cu_xS to CdS by annealing was revealed by the I-V characteristics. The presence of a cross over between the forward current-voltage characteristics measured in the dark and under illumination is normally taken as an evidence of the existence of an i-layer. The i-layer would reduce the instabilities which might be observed in the I-V characteristics of an as-made device. The instabilities are almost all caused by tunnelling through the abrupt junction [41]. After annealing in air, devices formed on SnO_x became very resistive and that is probably due to an increase in the series resistance. A good diode was obtained after heat treatment and this may be the results of widening the space charge region in the CdS. This means that only electrons with sufficient activation energy can tunnel from that side. The thin layer of Cu_2S along the grain boundaries also disappears with it and the concommitant shunting paths [6].

6.7 Conclusion

This work has shown that the phase of copper sulphide which is produced during topotaxial growth depends on the value of the electroplating bias, and these values differ from those required to achieve the same results using single crystal CdS. For thin film CdS, bias potential of +0.1 and -1.0V were found to produce the chalcocite and djurleite phases of Cu_xS respectively. Also the electrical and spectral sensitivities of CdS-Cu_xS thin film devices were affected by the electroplating bias. A cell with good I-V characteristics was obtained with

optimum solar cell operational parameters by applying +0.1V during plating.

One interesting result of this study concerns firstly the effect on device characteristics of the use of argon or air as an annealing ambient, and secondly the relative merits of tin oxide or Ag/Cr substrates. Previously many studies of this cell have been concerned with the role of oxygen during heat treatment, but relatively few have addressed the combined effect of substrate and annealing ambient. The work presented here has gone some way to redressing this omission and the result may be summarised as follows: Devices prepared with a chalcocite layer and fabricated on a tin oxide substrate are significantly affected by the ambient in which the anneal is conducted. Annealing in air leads to a considerable reduction in the chalcocite response and a corresponding increase in that due to djurleite. In contrast when the annealing is conducted in argon the overall spectral response is unchanged. On the other hand, for devices prepared on Ag/Cr substrates, annealing under similar conditions in air leads to a small reduction in the chalcocite response and a small increase in that from djurleite. This can be attributed to the presence of a trap which inhibits the in-diffusion of copper into the CdS during annealing of the CdS-Cu_2S cell due to a complex associate formed between silver and oxygen. Argon annealing for these devices leads to a reduction in the chalcocite response with a larger increase in that from djurleite compared with air annealing.

I-V characteristics from devices prepared on films deposited on SnO_x substrates indicate that these cells become very resistive with air heat treatment and the cross over between the forward light and dark current voltage curves becomes more pronounced. This can be atttributed to the formation of an i-layer at the heterojunction interface

by the diffusion of copper. In contrast, annealing in argon reduces both the amount of copper diffusion and the resistance of these devices. On the other hand I-V characteristics of devices fabricated on Ag/Cr substrate indicate only a small amount of copper diffusion and a small increase in the device resistance following annealing in air. This may be attributed to the presence of silver inhibiting the diffusion of copper. For devices on these substrates the effect on the resistivity of annealing in air was small but the diffusion was increased by heat treating in argon. This may be attributed to the presence of argon which may reduce the inhibiting effect of silver on the diffusion of copper.

Thus, in conclusion, it may be stated that the use of electroplating leads to a better control over the stoichiometry of the Cu_xS and the device parameters of CdS-Cu_xS thin film solar cells can be significantly affected by the choice of the combination of the substrate and the ambient used for the post-fabrication annealing.

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CHAPTER SEVEN

The $CdS-Cu_2S$ Solar Cell Stability Studies

7.1 Introduction

In this chapter the effects of different parameters on the stability of $CdS-Cu_2S$ heterojunctions are described. Studies of the degradation of these devices as a function of storage time in the dark and under illumination for different periods were carried out. Electron spectroscopy for chemical analysis (E.S.C.A.) was employed to measure the ratio sulphur to oxygen (S/O_2) at the surfaces of these devices. The effect on the stability of keeping cells in argon at different temperatures was investigated. A mixture of hydrogen (80%) and nitrogen (20%) gas was used as an ambient during heat treatment. The effect of the polishing and etching time of the CdS substrates on the cross-over between the dark and light current-voltage (I-V) characteristics was found to be important. The dependence of these device properties on dipping time was also investigated. In the final section the dependence of the dark I-V characteristics on the electroplating bias used during the Cu_xS deposition is reported. For most of these investigations the I-V characteristics and spectral responses were measured both at room and at liquid nitrogen temperature.

7.2 The Effect of Ageing on Device Properties

In an attempt to study the effect of storage in light and in dark conditions on the degradation of $CdS-Cu_2S$ devices, pairs of samples were prepared using the chemiplating process as discussed in Chapter Five. One of them was kept in the dark while the other was maintained under illumination provided by a 60W tengsten lamp. By monitoring the characteristics of these devices simultaneously after 7, 14 and

28 days it was ensured that both devices experienced the same ambient.

7.2.1 Current-voltage Characteristics

The I-V characteristics of the CdS-Cu_2S heterojunctions were measured immediately after fabrication, in the dark and under AM1 illumination. Typical I-V characteristics for two unencapsulated cells in the as-made condition and after storage in the laboratory ambient separately in the dark and under light are shown in Figures 7.1 and 7.2 respectively. While the changes in the device parameters and reverse bias leakage were relatively small for the cells kept in the dark (Fig 7.1); those devices kept in the light exhibited a drastic deterioration in their operational parameters, and this is shown in Table 7.1. From this it can be seen that the parameter which degrades most rapidly with storage in light is the fill factor which causes a correspondingly large reduction in the efficiency. These results conclusively demonstrate detrimental effects of exposures to light on the operational parameters of unencapsulated cells.

	AGEING IN DARK				AGEING IN LIGHT			
Length of storage (weeks)	V_{oc}(V)	I_{sc} $mA.cm^{-2}$	FF	γ%	V_{oc}(V)	I_{sc} $mA.cm^{-2}$	FF	γ%
as-plated	0.46	10.80	0.52	2.60	0.46	10.80	0.52	2.60
1	0.45	10.50	0.47	2.20	0.425	10.10	0.37	1.60
2	0.42	9.70	0.42	1.71	0.325	8.70	0.31	0.87
4	0.40	8.30	0.40	1.33	0.22	5.30	0.24	0.28

Table 7.1 : CdS-Cu_2S device parameters in the as-made condition and after ageing.

7.2.2 Spectral Response

In order to study the stability of copper sulphide with ageing,

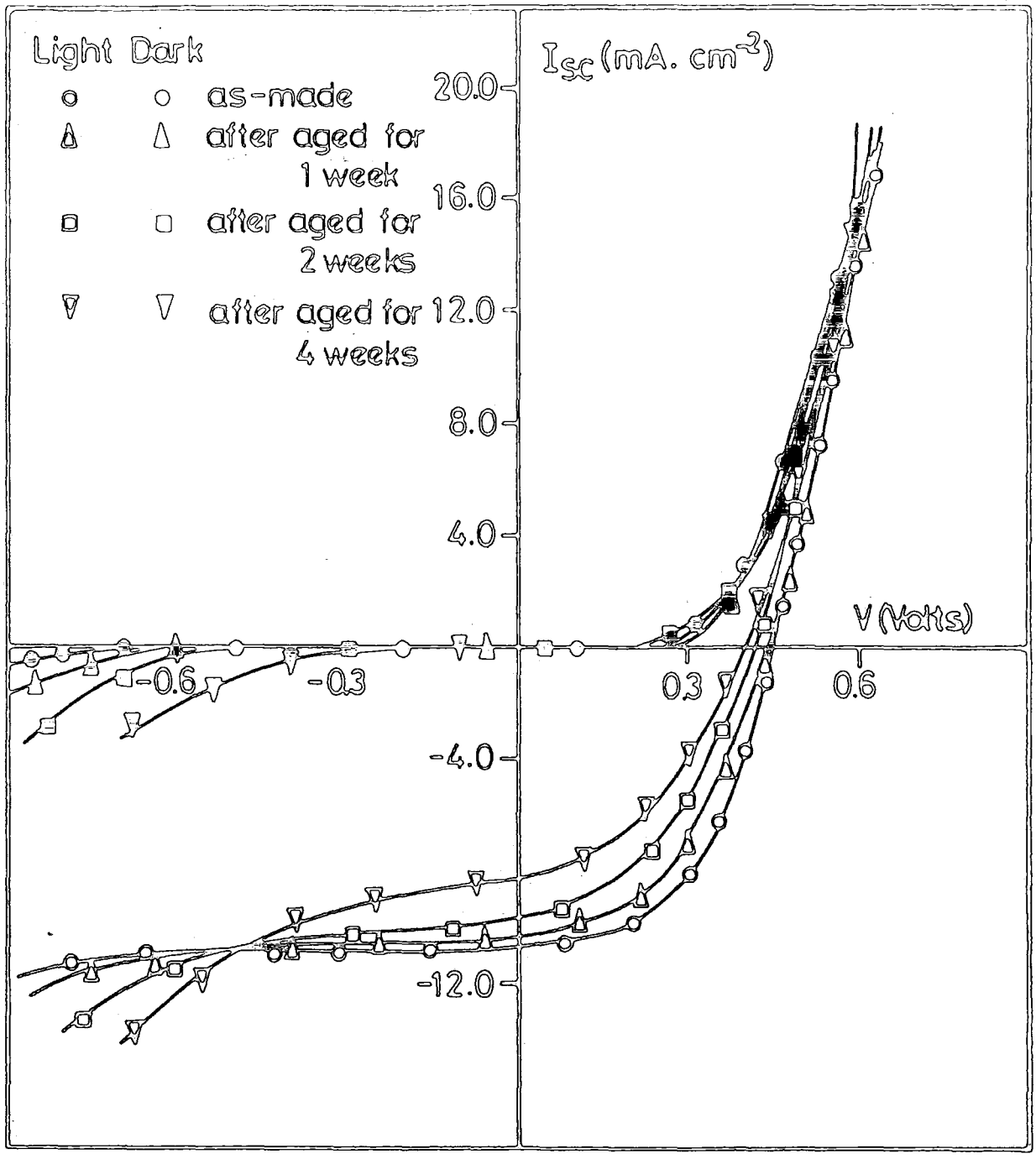


Fig 7.1 : Current-voltage characteristics of a CdS-Cu_2S device after aged in dark at room temperature and lab. atmosphere for a different periods of time

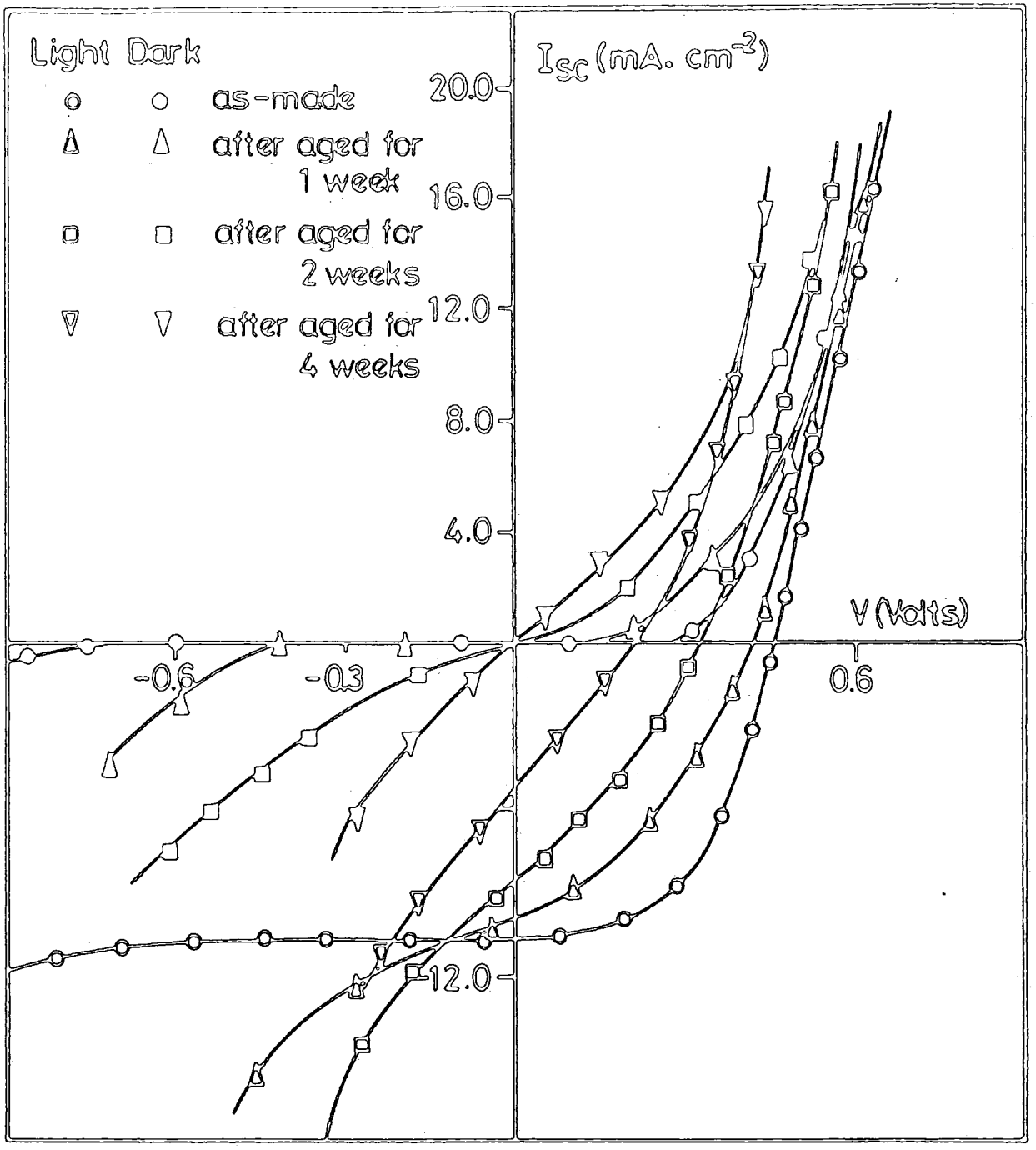


Fig 7.2 : Current-voltage characteristics of CdS-Cu_2S device after ageing under illumination at room temperature in the lab. atmosphere for different periods of time.
(Open symbols : under AM1 illumination and filled symbols dark characteristics).

the spectral response of V_{oc} for devices prepared on a predominantly chalcocite layer was measured at 85 K as a function of storage time at room temperature. The spectral distributions of V_{oc} for such cells, in the as-made condition and after ageing separately for a few weeks in the dark and in the light, measured at 85 K, are shown in Figures 7.3 and 7.4 respectively. The maximum response for as-plated cells occurred in the 0.96 μm band with small shoulders at wavelength of 0.78μm. These bands have been discussed in Chapter Five, and are associated with the chalcocite (Cu_2S) and djurleite ($Cu_{1.96}S$) phases of copper sulphide [1]. From the curves in Figure 7.3 it is obvious that ageing the device in the dark led to a slight increase in the response due to a djurleite, and that only became apparent after four weeks ageing. In contrast, ageing under illumination (Figure 7.4) for 7, 14 and 28 days led to a progressive reduction in the chalcocite peak and a corresponding increase in the response from djurleite. This change was most pronounced between the measurements made after ageing for 14 and 28 days.

7.2.3 Electron Spectroscopy for Chemical Analysis (E.S.C.A.)

ESCA or X-ray photoelectron spectroscopy was employed to investigate the presence of oxygen, as well as the ratio of the sulphur to oxygen, on the surfaces of the copper sulphide layers of the aged devices. This is a unique method to investigate the structure, bonding and reactivity of the elements at material surfaces. It is a non-destructive and powerful surface sensitive technique involving photoelectrons in an ultra high vacuum ($10^{-7} \rightarrow 10^{-10}$ Torr). It is limited to the characterisation of the first few layers (usually to a depth of 20 to 40 Å) of a sample surface. It can be employed to study all elements in the periodic table except hydrogen and helium, and is particularly suited

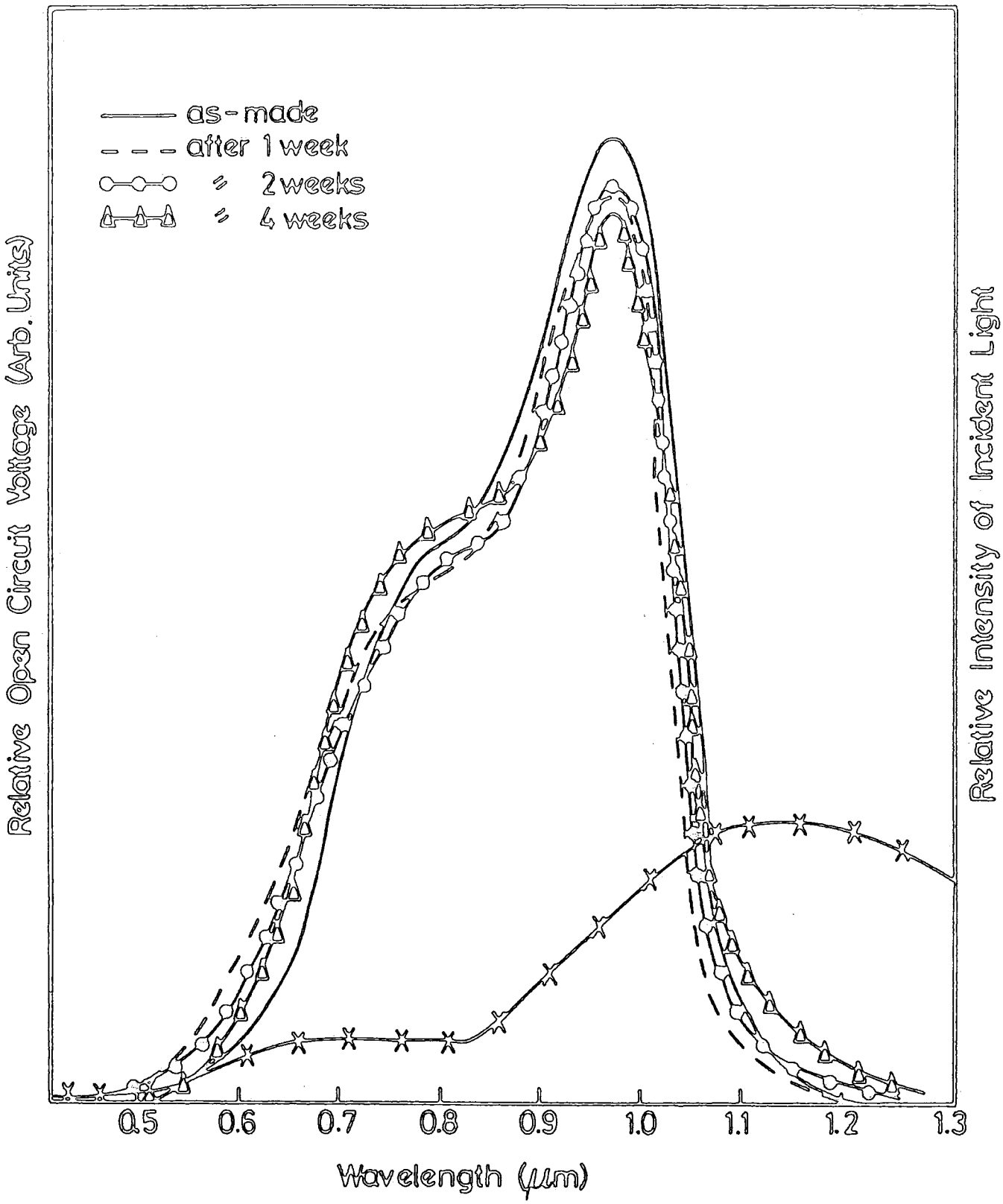


Fig 7.3 : Relative open circuit voltage measured at 85 K for CdS-Cu_2S device aged in dark at room temperature for different periods.

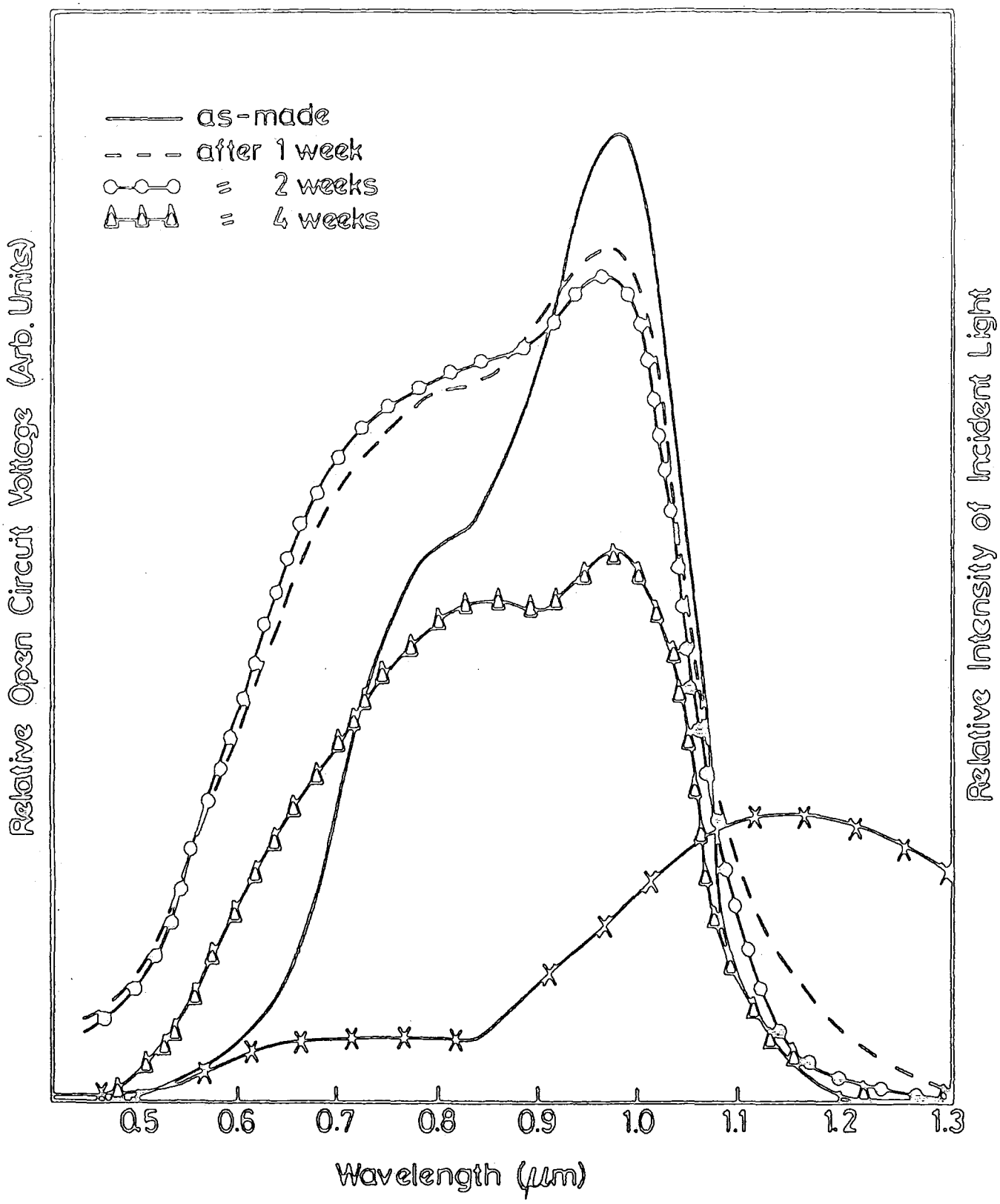


Fig 7.4 : Relative open circuit voltage measured at 85 K for a CdS-Cu_2S device aged under light at room temperature for different periods.

to the investigation of the oxidation state of surface atoms, and of the relative concentration ratios of different elements of a compound material.

In practice, X-rays such as $MgK\alpha_{1,2}$(1.254κeV) or $ALK\alpha_{1,2}$(1.487κeV) of approximately 0.7 to 1.0 eV line width are incident on a sample and the energies of the ejected photoelectrons are analysed in a high resolution spectrometer. The electron count versus kinetic energy yields the photoelectron spectrum. Intensity maxima in the phtoelectron spectrum correspond directly to the band electron energy levels in the sample tested, and the total kinetic energy (KE) of the ejected electron can be used to calculate the electron binding energy (BE) with respect to the fermi level

$$KE = h\nu - BE - Er$$

where h is Planck's constant, ν is the frequency of the incident radiation, BE is the binding energy of the photoemitted electron (defined as the positive energy required to remove the electron to infinity) and Er is the recoil energy of the atom or molecule. The E.S.C.A. investigation demonstrated that the ratio of the oxygen (O_{1s}) to sulphur (S_{2p}) for the device which was kept in the dark for four weeks was

$$O_{1s} : S_{2p} = 2209 : 610$$
$$\simeq 7 : 2$$

while the ratio for the device which was kept under illumination was

$$O_{1s} : S_{2p} = 2334 : 422$$
$$\simeq 11 : 2$$

The conclusion from this is simply that the device maintained under illumination had absorbed more oxygen than that kept in the dark.

Another E.S.C.A. experiment was carried out on two other $CdS-Cu_2S$

devices. One was in the as-made condition, while the other had been heated for two minutes at 200°C in air. The result shows that the oxygen content on the Cu_xS surface of the device which had been heated in air was more than twice that of the as-made device. The ratio of oxygen to the sulphur for the as-made sample was:

$$O_{1s} : S_{2p} = 2278 : 633$$
$$\simeq 7 : 2$$

while the ratio for the air heated device was:

$$O_{1s} : S_{2p} = 2737 : 340$$
$$\simeq 16 : 2$$

7.3 The Effect of an Argon Atmosphere at Different Temperatures on the Stability of CdS-Cu_2S Solar Cells

To determine the effect of an argon ambient on the properties of CdS-Cu_2S heterojunction, two devices were prepared under identical conditions and their current-voltage characteristics and spectral responses were monitored as a function of ageing in this ambient separately at 18 and 50°C. The influence of heat treatment of a degraded device in a mixture gas of hydrogen (80%) and nitrogen (20%) was also investigated.

7.3.1 Cell Performance

Two CdS-Cu_2S devices were prepared with almost the same I-V characteristics and spectral response. Figures 7.5 and 7.6 illustrate the I-V characteristics of the devices in the as-made condition and after different periods of ageing in argon at 18°C and at 50°C. The results show that the storage of a device in argon at room temperature for up to six weeks led to only very small decreases in V_{oc} and in I_{sc} (Fig 7.5). In addition it can be seen that storage beyond one week led to a slight cross-over between dark and light characteristics, which was

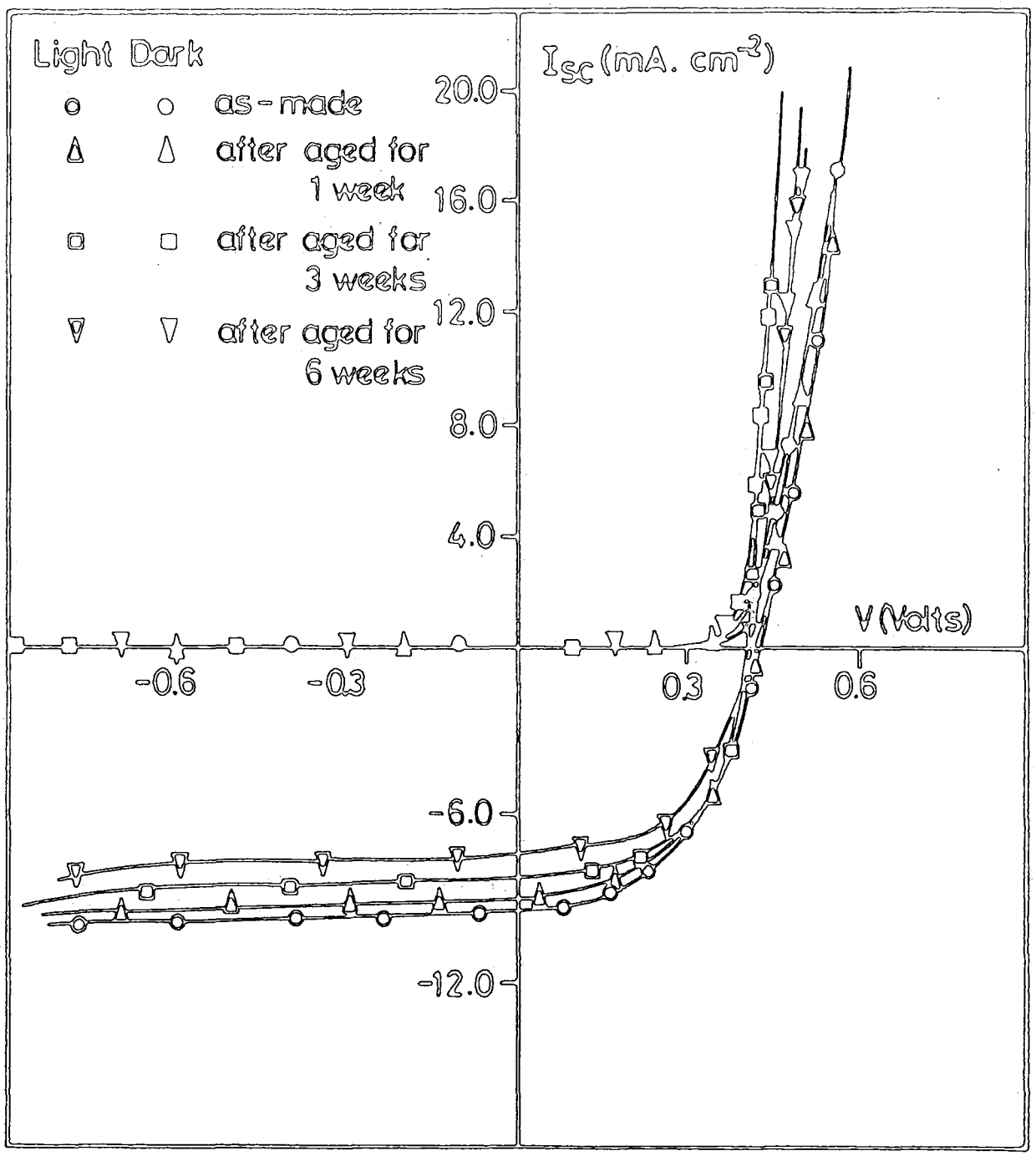


Fig 7.5 : Typical current-voltage characteristics as a function of ageing in argon at room temperature measured in the dark and under illumination.

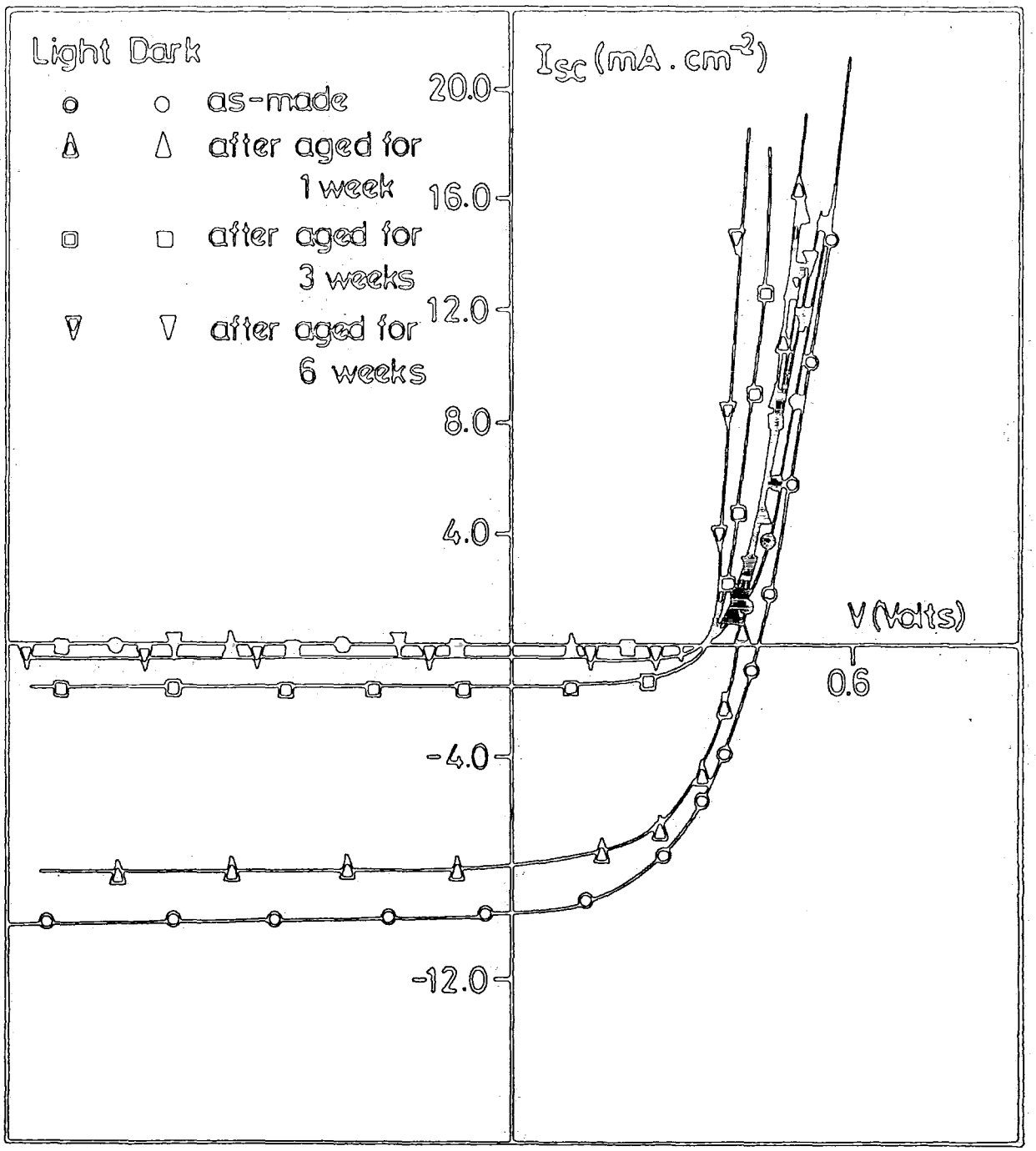


Fig 7.6 : Typical current-voltage characteristics as a function of ageing in argon at 50°C measured in the dark and under illumination.

not evident earlier. In contrast the degradation of the device kept in argon at 50°C (Fig 7.6) was much more pronounced. In particular the deterioration in these characteristics is seen to be rather dramatic after ageing for more than one week at this temperature. In fact the I_{sc} is reduced to $< \frac{1}{5}$ of the value for the as-made cell. Further the cross-over between light and dark characteristics became very obvious when ageing at this temperature. It is important to note that the devices stored at both temperatures retained their hard characteristics after storage, and despite the reduction in V_{oc} and particularly in I_{sc}, the fill factor was improved by ageing. From comparison of the I-V characteristics for devices aged at 18°C in argon (Figure 7.5) and in air (Figure 7.1), it is obvious that an ambient of argon leads to more greater stability than an ambient of air.

The spectral responses of V_{oc} for these devices aged at 18 and 50°C in argon were measured at 85 K as a function of ageing. For the device maintained at 18°C the changes in the response over a three week period were minimal as is confirmed by the curves in Figure 7.7. However the same was not true for the similar device maintained at 50°C. The spectral response of this device measured at 85 K as a function of ageing is shown in Figure 7.8. From this, the response due to chalcocite is seen to decrease progressively with ageing, while a distinct peak at about 0.75 μm develops after three weeks. This peak can be attributed to djurleite rather than to deep copper levels, especially as it was found that the copper response diminished at 85 K.

7.3.2. The Effect of Heat Treatment in H_2/N_2 Ambient

In the previous section, it was demonstrated that the ageing of CdS-Cu_2S devices in argon at 50°C led to a significant degradation in cell parameters. In an attempt to determine the influence of annealing

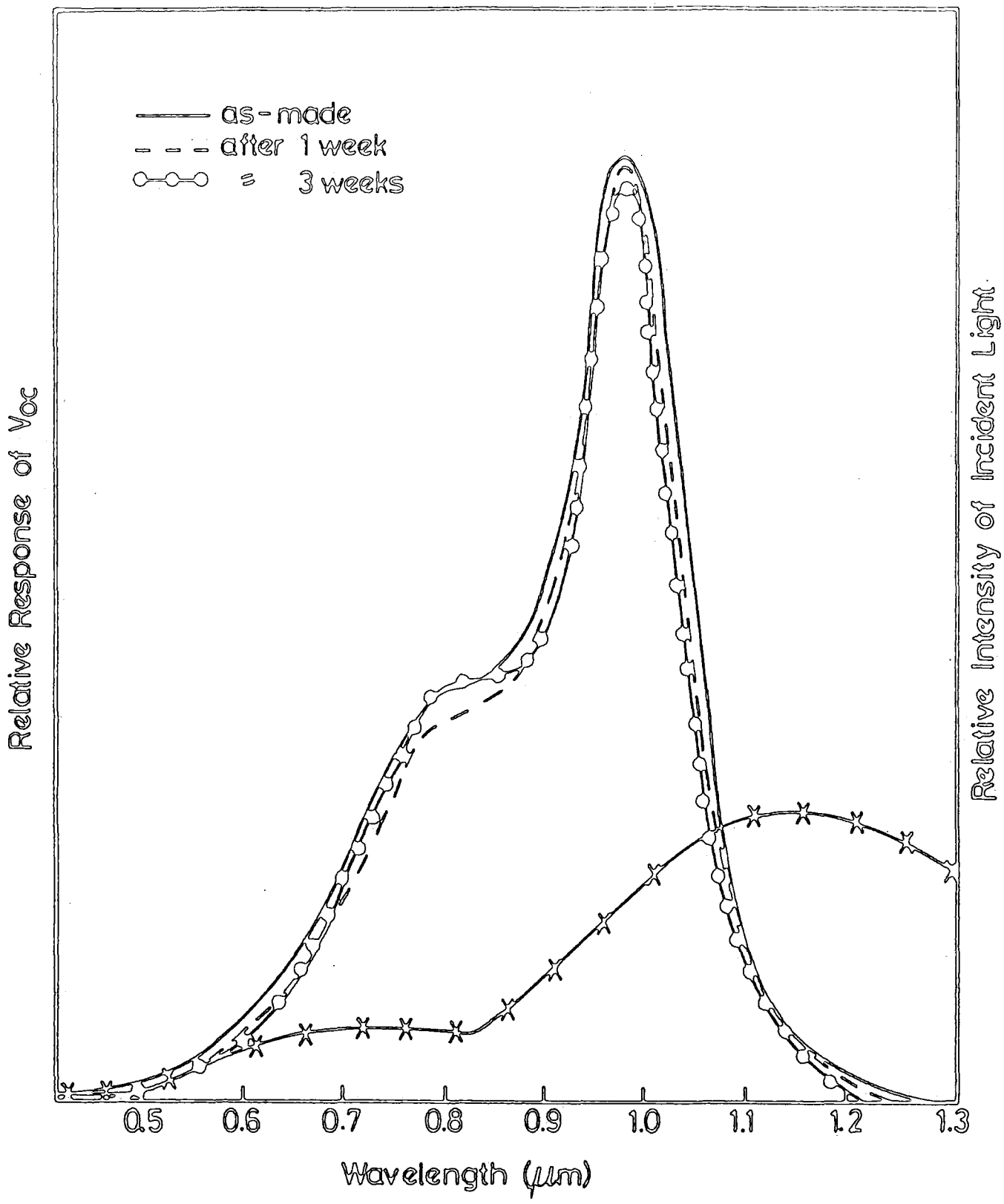


Fig 7.7 : The effect of ageing in argon at room temperature on the spectral response of V_{oc} measured at liquid nitrogen temperature.

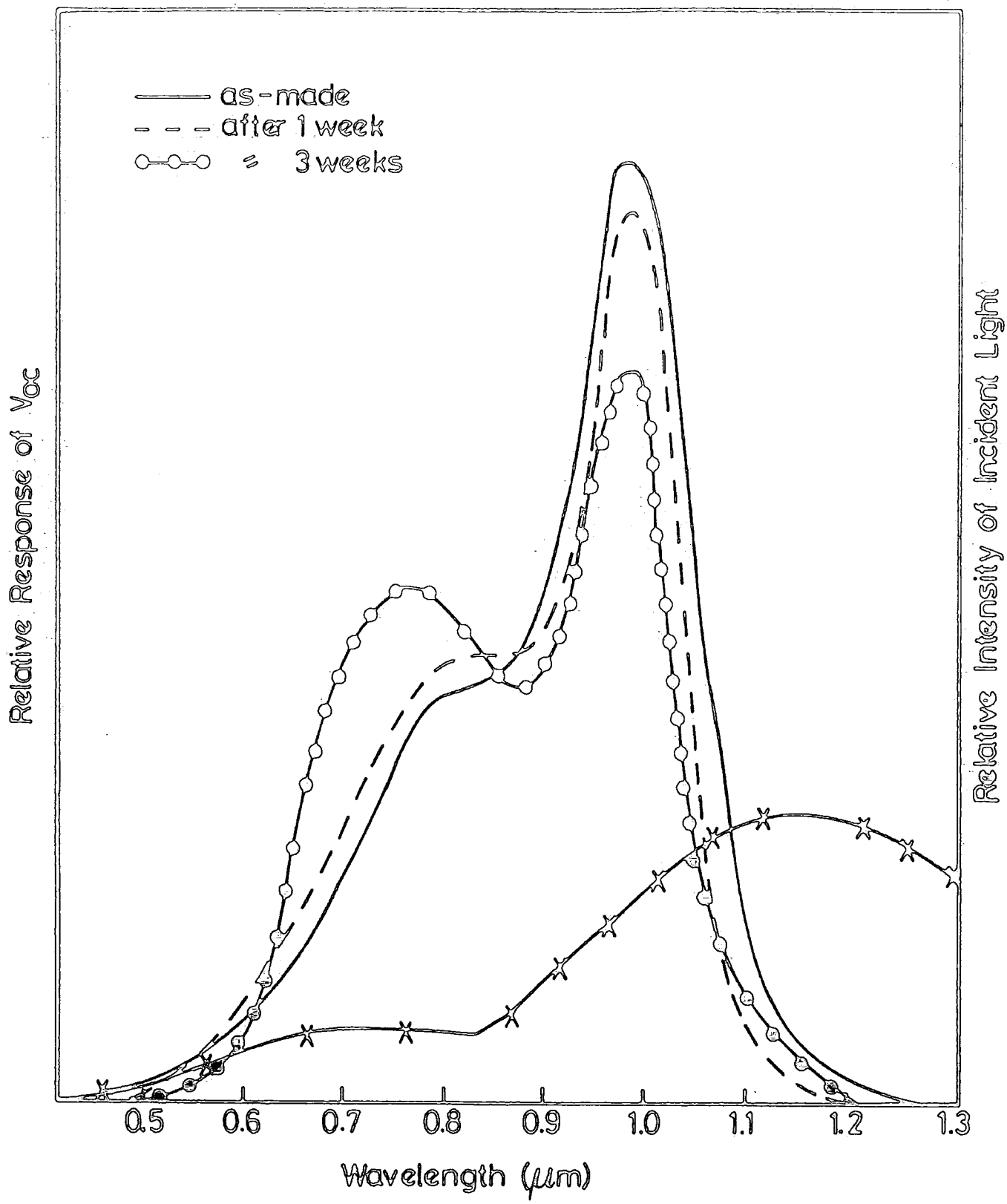


Fig 7.8: The effect of ageing in argon at 50°C on the spectral response of V_{oc} measured at liquid nitrogen temperature.

in a H_2/N_2 mixture, the device aged at 50°C in argon was heated in H_2/N_2 at 150°C for different periods. Typical current-voltage characteristics as a function of bake time in H_2/N_2 are shown in Figure 7.9. This demonstrates that heat treatment in this reducing ambient for relatively long periods does lead to a significant recovery of the cell parameters. The extent of the heat treatment is revealed by the considerable cross-over between light and dark curves, which is an indication of the degree of copper diffusion. This is confirmed by the spectral responses of the cell at 85 and 295 K, shown in Figures 7.10 and 7.11 respectively. At the lower temperature, which provides the better indication of the Cu_xS phase present, it is clear that the effect of annealing in the H_2/N_2 mixture is to increase the relative response for chalcocite at 0.96μm. However, when the measurements were made at 295K (Figure 7.11) the dominant response at 0.6 - 0.65μm following the argon treatment reveals the presence of deep copper levels and these become even more dominant with prolonged heat treatment in H_2/N_2 .

7.4 The Effect of Etching Time on the Cross-over Between Dark and Light I-V Characteristics.

In order to determine the relative effects of the duration of the etching on the I-V characteristics, five samples were polished after which four of them were etched for different periods in concentrated HCl at room temperature. SEM micrographs of the sulphur plane after etching for 5, 10, 20 and 40 seconds are shown in Figures 7.12a,b,c,d respectively and these illustrate the stages of development of the etch hillocks. These micrographs clearly show that extending the etching period results in larger hillocks on the $000\bar{1}$ surface. Next, heterojunctions were made on these etched substrates together with the polished

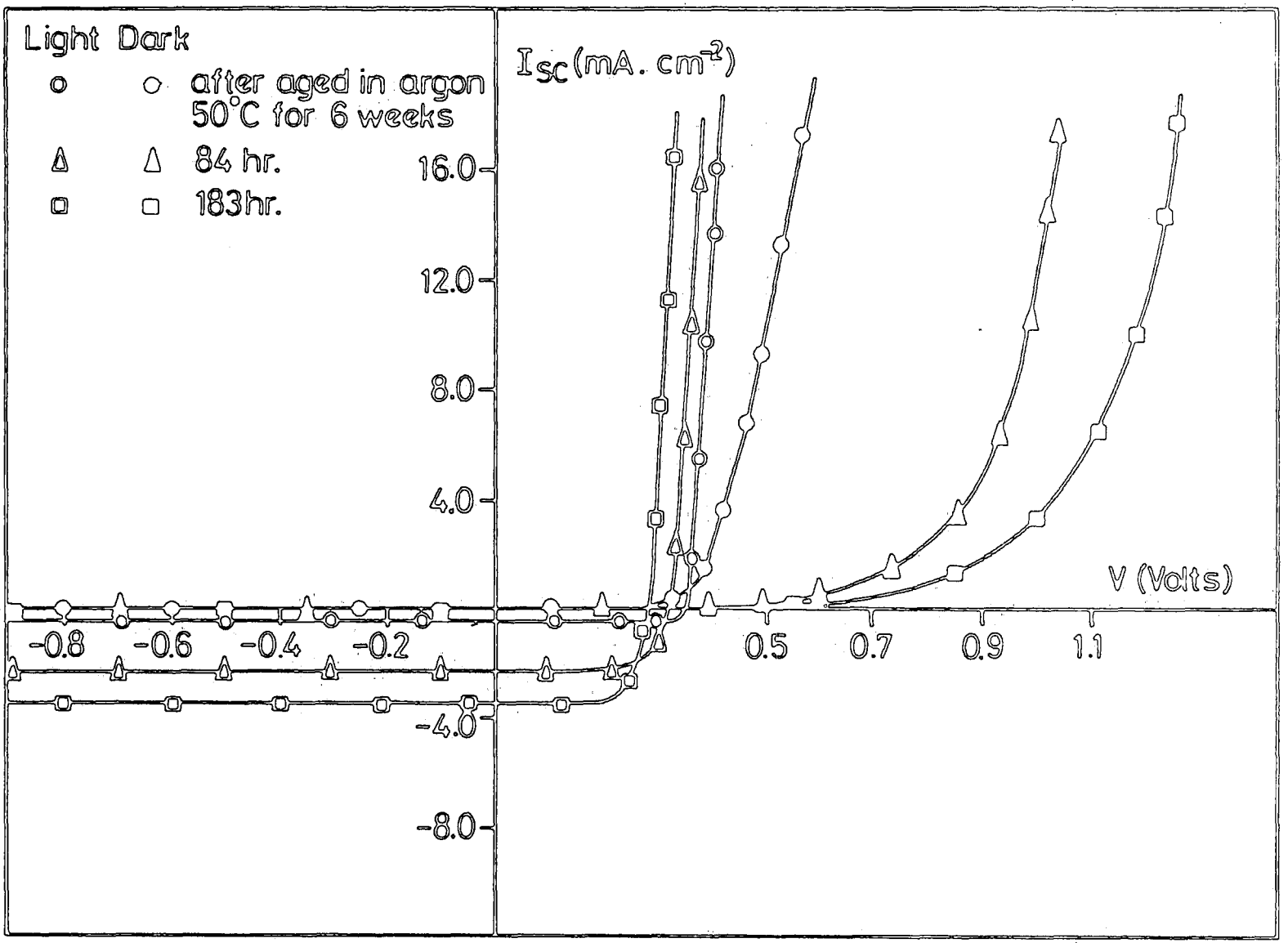


Fig 7.9 : Current-voltage characteristics measured in dark and under AM1 illumination after heat treatment in an H_2/N_2 mixture at 150°C.

(Open symbols : light characteristics, filled symbols : dark characteristics.)

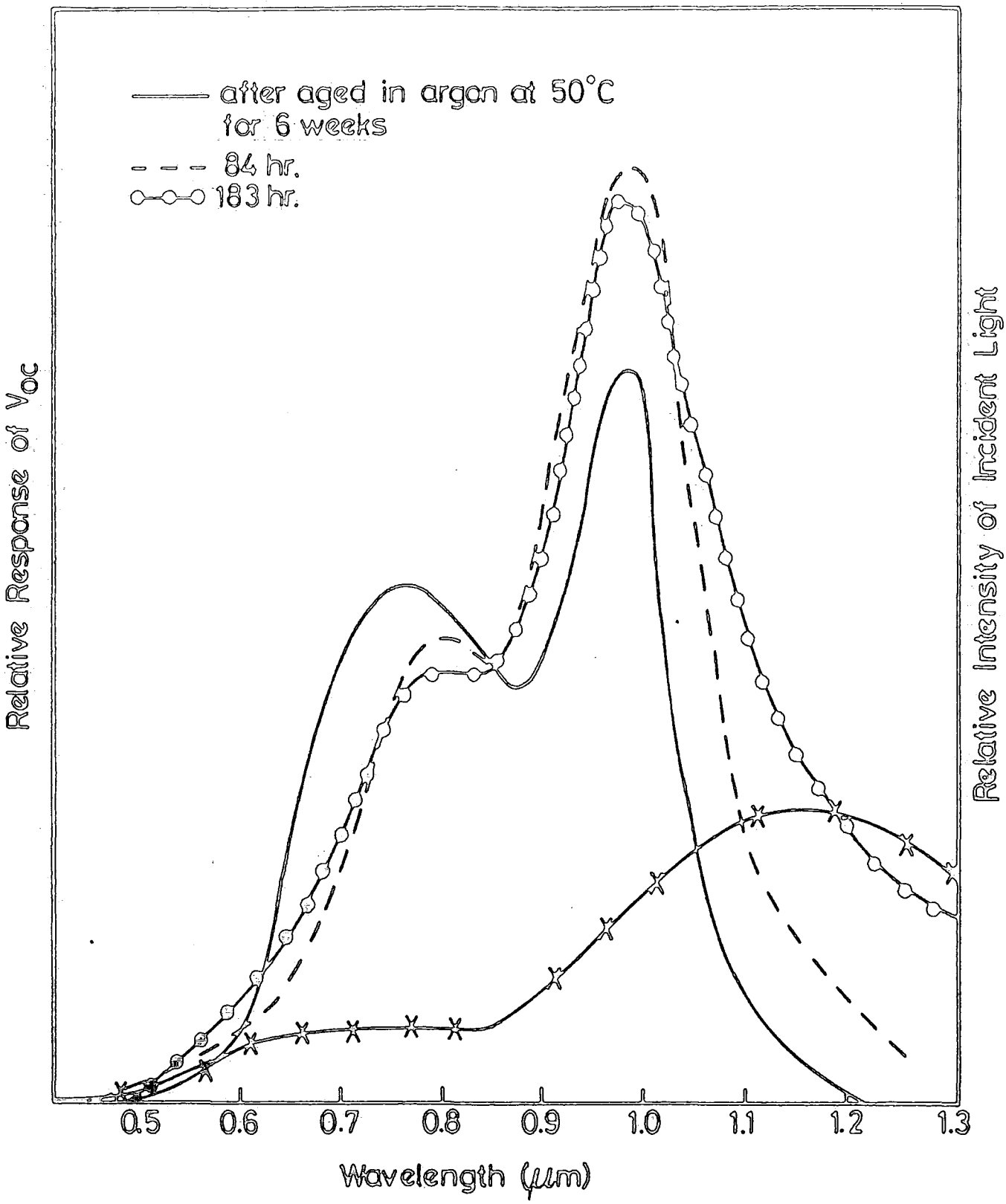


Fig 7.10 : Open circuit voltage spectral response measured at 85 K for CdS-Cu_xS devise after ageing in argon at 50°C for 40 days and heated in H_2/N_2 mixture at 150°C.

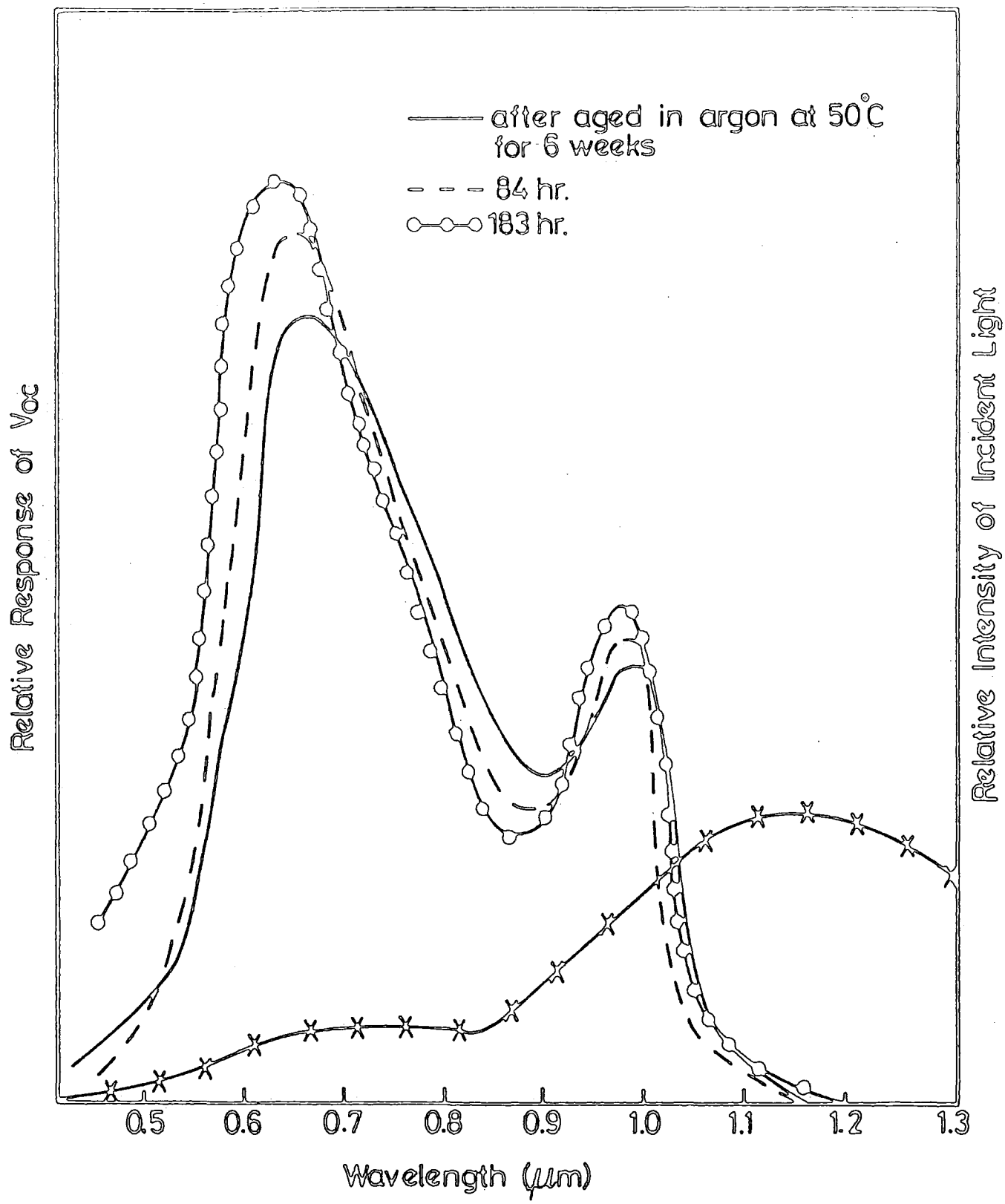
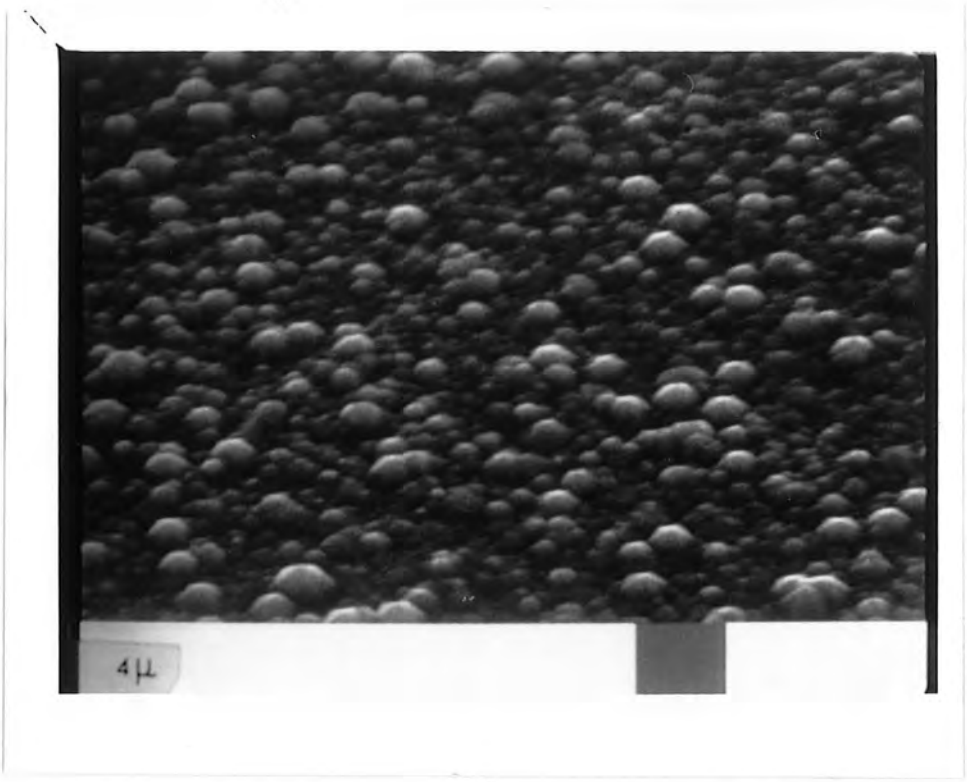


Fig 7.11 : Open circuit voltage spectral response measured at 295 K for a CdS-Cu_xS device after ageing in argon at 50°C for 40 days and heated in H_2/N_2 mixture at 150°C.

one using the same preparational procedure. The I-V characteristics of the as-made devices were measured in the dark and under AM1 illumination, and are shown in Figure 7.13. These curves demonstrate that the cross-over between the dark and light characteristics was clearly pronounced in the device formed on the substrate which was not etched. The degree of cross-over was reduced by extending the etching period. It is important to emphasise that the cross-over effect, which is usually attributed to copper diffusion during heat treatment was observed for an as-made device on a polished surface. The device with the best operational parameters was obtained from the substrate which was etched for 30 seconds (see Chapter 5, micrograph 5). This experiment again demonstrated that etching [2,3] is one of the most important steps in the fabrication of these devices. The optimum period of etching depends on the nature and thickness of the polycrystalline work damaged layer. It is important to remove this layer in order that a monocrystalline topotaxial layer of copper sulphide can be formed on the CdS. The poor characteristics of cells on surfaces etched for 10 seconds or less can probably be attributed to a high density of surface states and to relatively large tunnelling currents. However, etching for 40 seconds introduces shunting paths which give rise to softer characteristics again.

7.5 The Effect of Dipping Time on Cell Properties

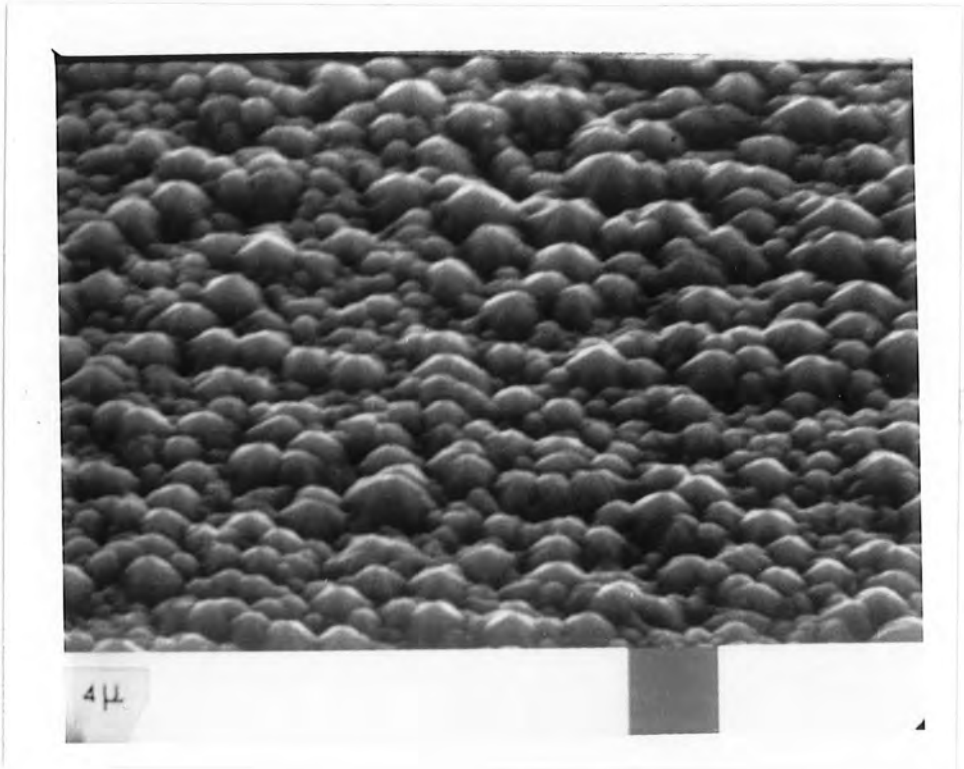
In Chapter Five, it was demonstrated that the optimum value of electroplating bias during the formation of copper sulphide on CdS single crystals was +0.01 V. The optimum dipping period which was associated with this electroplating bias was 10 seconds. The effect on the current-voltage characteristics recorded in the dark and under AM1 of increasing the dipping period to 60 and 120 seconds at the same electroplating bias is shown in Figure 7.14. The as-made I-V characteristics for the



a

5 secs.

Figure 7.12 : Secondary emission micrographs of $(000\bar{1})$ CdS surfaces etched for different periods.



b

10 secs.

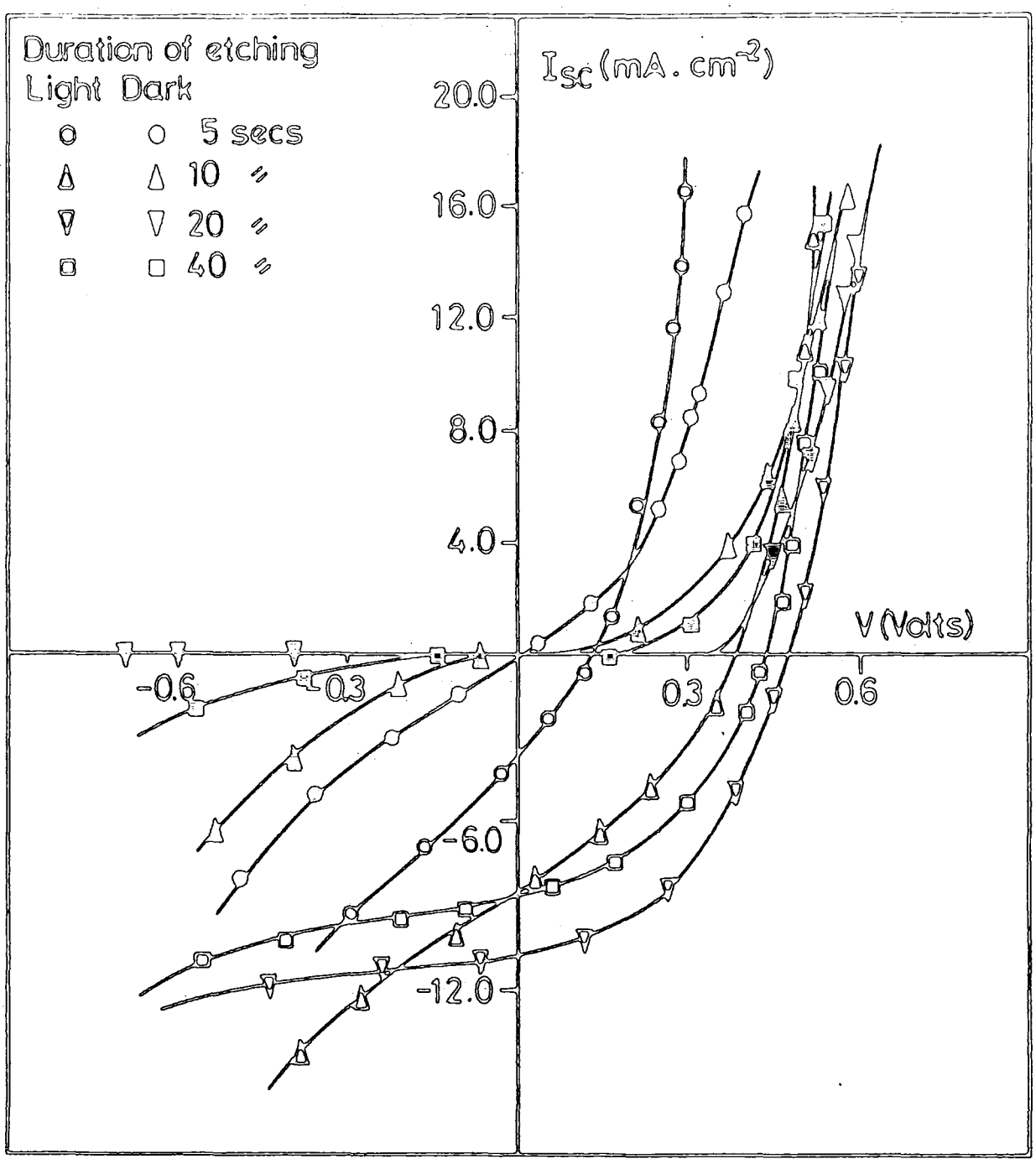
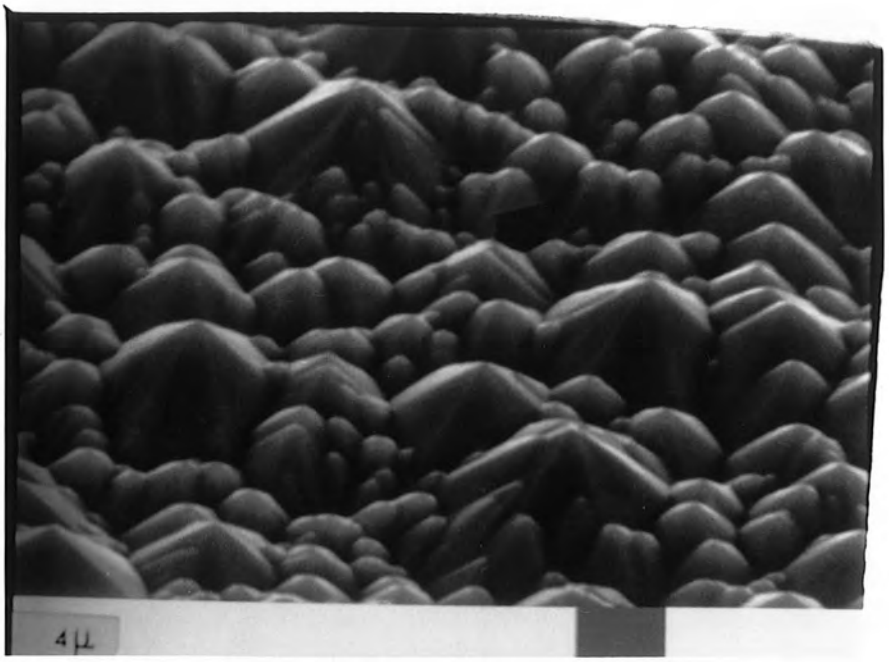


Fig 7.13 : Current-voltage characteristics of devices fabricated on single crystal substrate after different periods of etching.



c

20 secs

d

40 secs

device prepared by dipping for 60 seconds typically exhibited a hard reverse bias behaviour with V_{oc} = 0.32V and I_{sc} = 2.0 mA.cm^{-2} . Extending the plating period to 120 seconds led to a high value of series resistance as evidenced by the drastic reduction in short circuit current to 3.0 μA.cm^{-2}. Conversely dipping for only 10 seconds led to the best device parameters V_{oc} = 0.475 V and I_{sc} = 12.3 mA.cm^{-2}.

The spectral responses of V_{oc} for these three devices were recorded at 295 K and 85 K, but only those measured at the lower temperature are shown in Figure 7.15 because they give a more reliable indication of the phase of the Cu_xS present. For the device dipped for 10 seconds, the maximum response occurred at 0.95μm, corresponding to chalcocite, and there is a small shoulder in the region of 0.78μm and this can be ascribed to djurleite. When the dipping time was increased to 60 seconds, the djurleite response increased significantly, while that due to chalcocite was correspondingly reduced. When the dipping time was further extended to 120 seconds, the dominant peak occurred at 0.65μm with a small response due to the chalcocite phase. The appearance of a peak in the wavelength range between 0.65-0.80 μm in the spectral response for an as-made device is presumed to be a sign of the presence of the djurleite phase [4]. Another peak also appeared at the shorter wave - length of 0.49μm in the response of devices dipped in for 60 and 120 seconds. This peak is attributed to transitions across the bandgap of CdS. Since its magnitude was increased by extending the dipping time, this suggests that prolonged dipping reduces the overall optical absorption of the Cu_xS layer with the result that light of wavelength 0.49μm was able to penetrate the Cu_xS layer to reach the underlying CdS. This suggests that extended dipping leads to a Cu_xS phase with considerably inferior absorption properties.

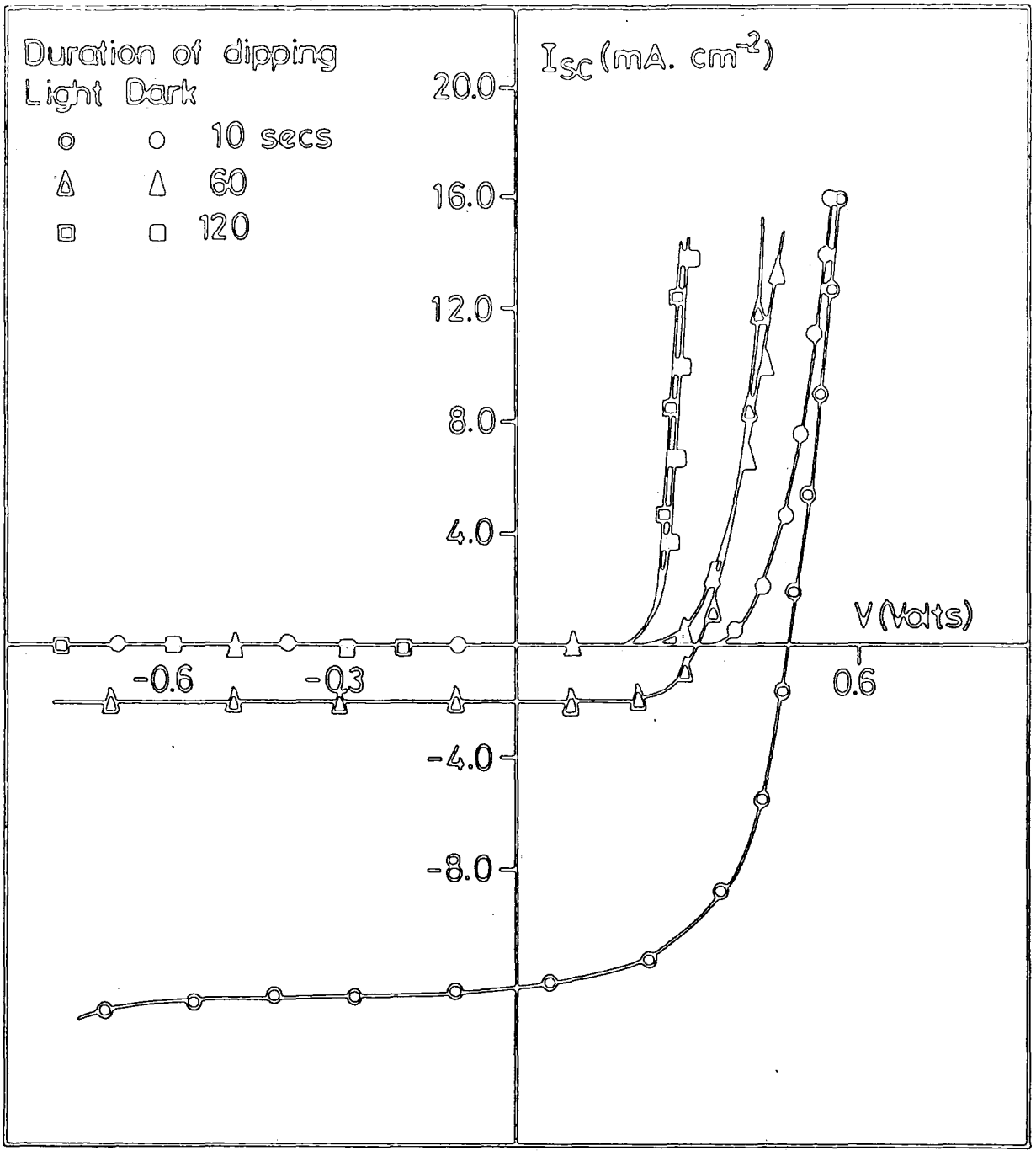


Fig 7.14 : The effect of dipping time on the current-voltage characteristics of as-made devices.
Open symbols : light characteristics, filled symbols: dark characteristics.

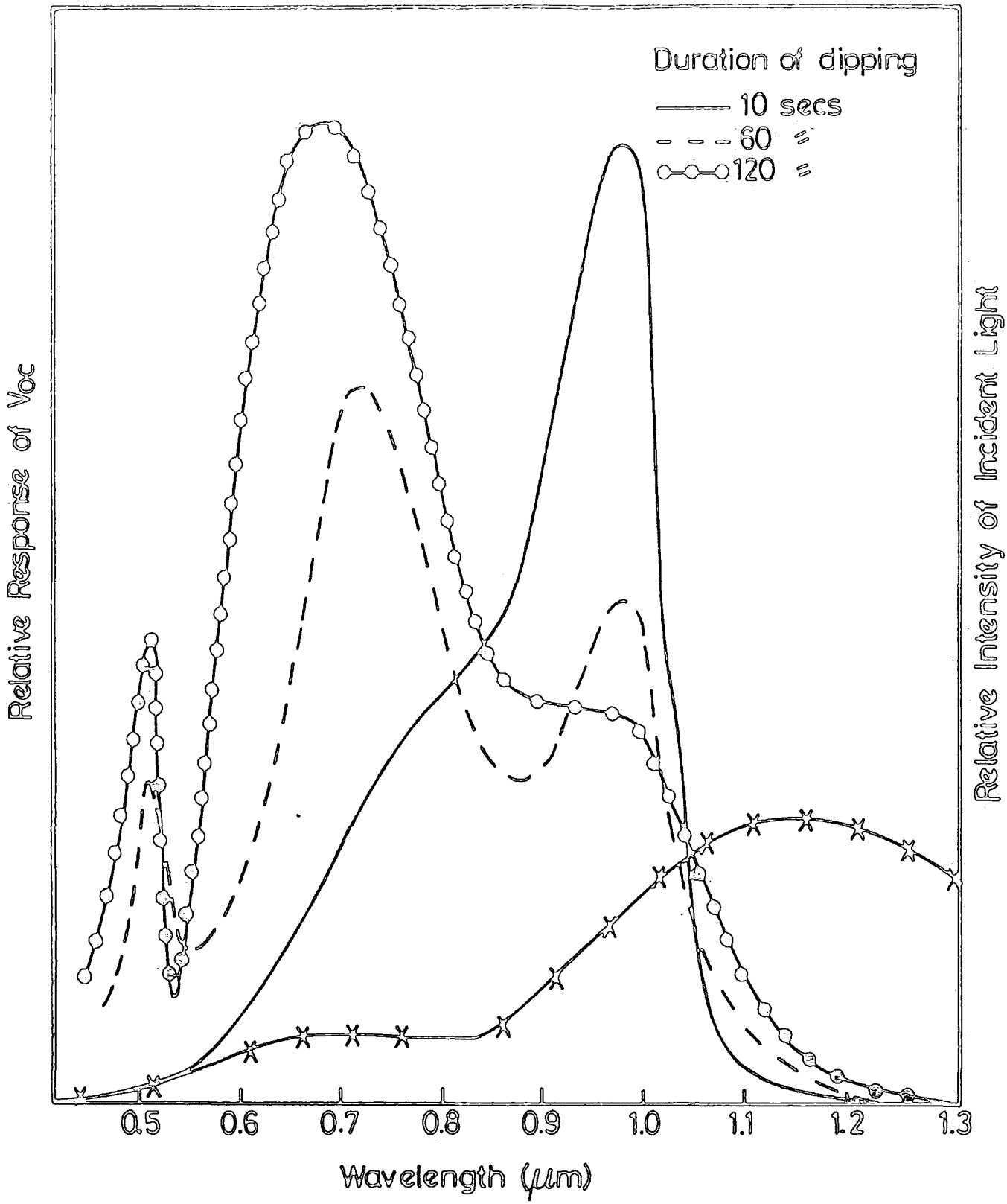


Fig 7.15 : Spectral response of open circuit voltage measured at 85 K as a function of dipping time.

7.6 The Dependence of Dark I-V Characteristics on Electroplating Conditions

The influence of the value of electroplating bias on the phase of copper sulphide grown on CdS single crystals and the properties of CdS-Cu_xS solar cells were discussed in detail in Chapter 5. In this section the dependence of the dark current conduction mechanism on the value of electroplating bias used during the growth of the topotaxial Cu_xS layer on CdS is described. The measurements were carried out at room and liquid nitrogen temperatures. A wide range of biases were applied, and the forward dark current-voltage (I-V) characteristics of as-made devices are illustrated in Figures 7.16, 7.17 and 7.18 For all devices, the forward conduction mechanism at small voltage bias follows a simple ohmic behaviour. Figure 7.16 shows the effect of using +3.0 V plating bias during the growth of Cu_xS. With these curves the ohmic region extended up to a forward bias of 0.03V. For devices which were fabricated with plating biases of +1.0, 0.1 and +0.01V, the corresponding ohmic region extended to 0.1, 0.15 and 0.2V respectively as shown in Figure 7.17. The influence of negative and zero plating bias on the dark current-voltage characteristics is shown in Figure 7.18. The slopes of the log J_F versus V_F plots changed as the electroplating bias was varied. However, the variation in the slopes which was observed at both temperatures can be explained in terms of the temperature dependence of the bandgaps of the material. For example dEg/dT is about $-5.2\ 10^{-4}$ eV/kT for CdS[5]. At forward bias voltages larger than 3kT/q many heterojunctions commonly obey the following empirical relationship

$$J_F = J_o \exp \frac{qv}{AkT}$$

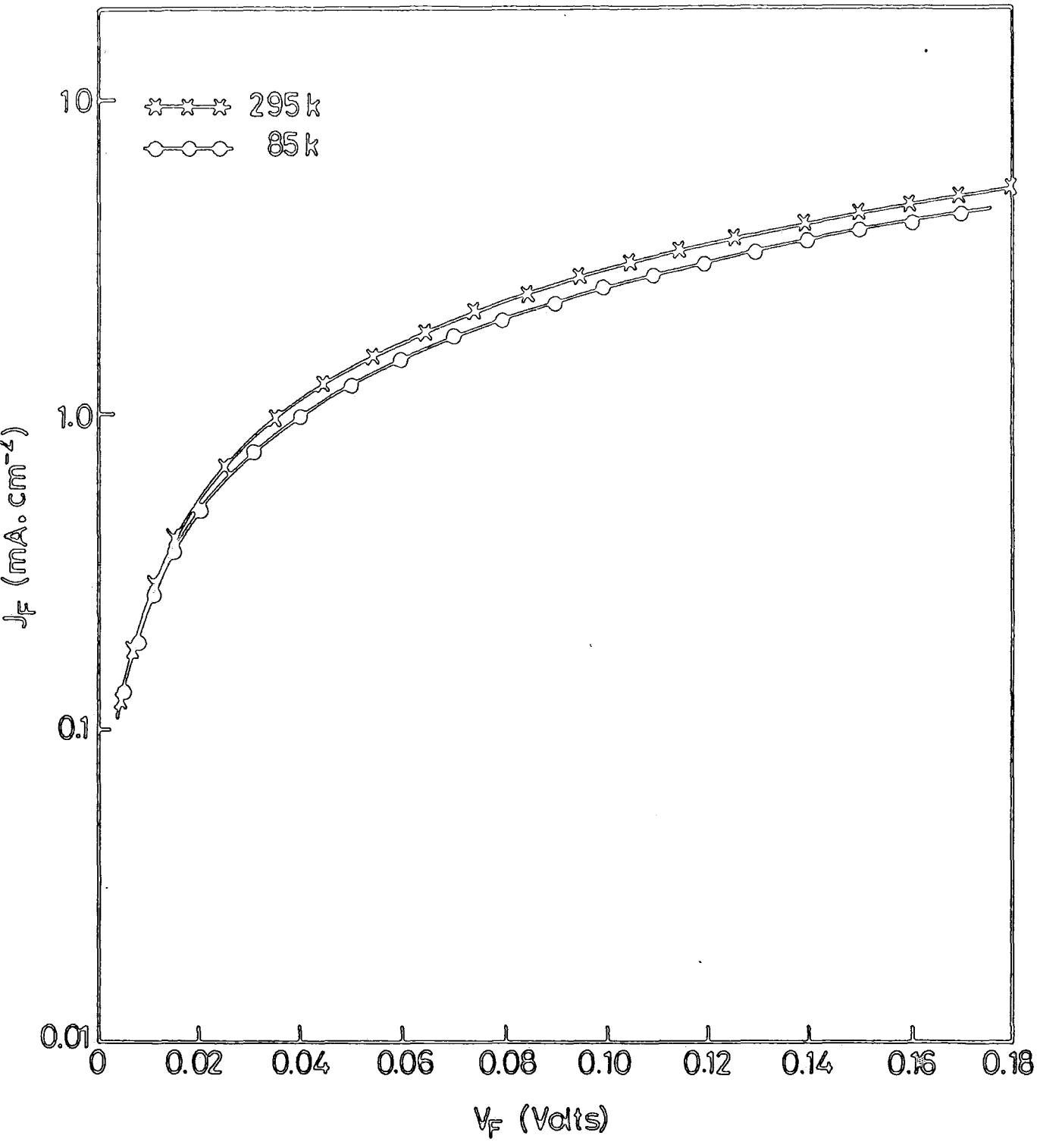


Fig 7.16 : Dark current-voltage characteristics for as-prepared CdS-Cu_xS device fabricated with +3.0V electroplating bias measured at 295 and 85 K

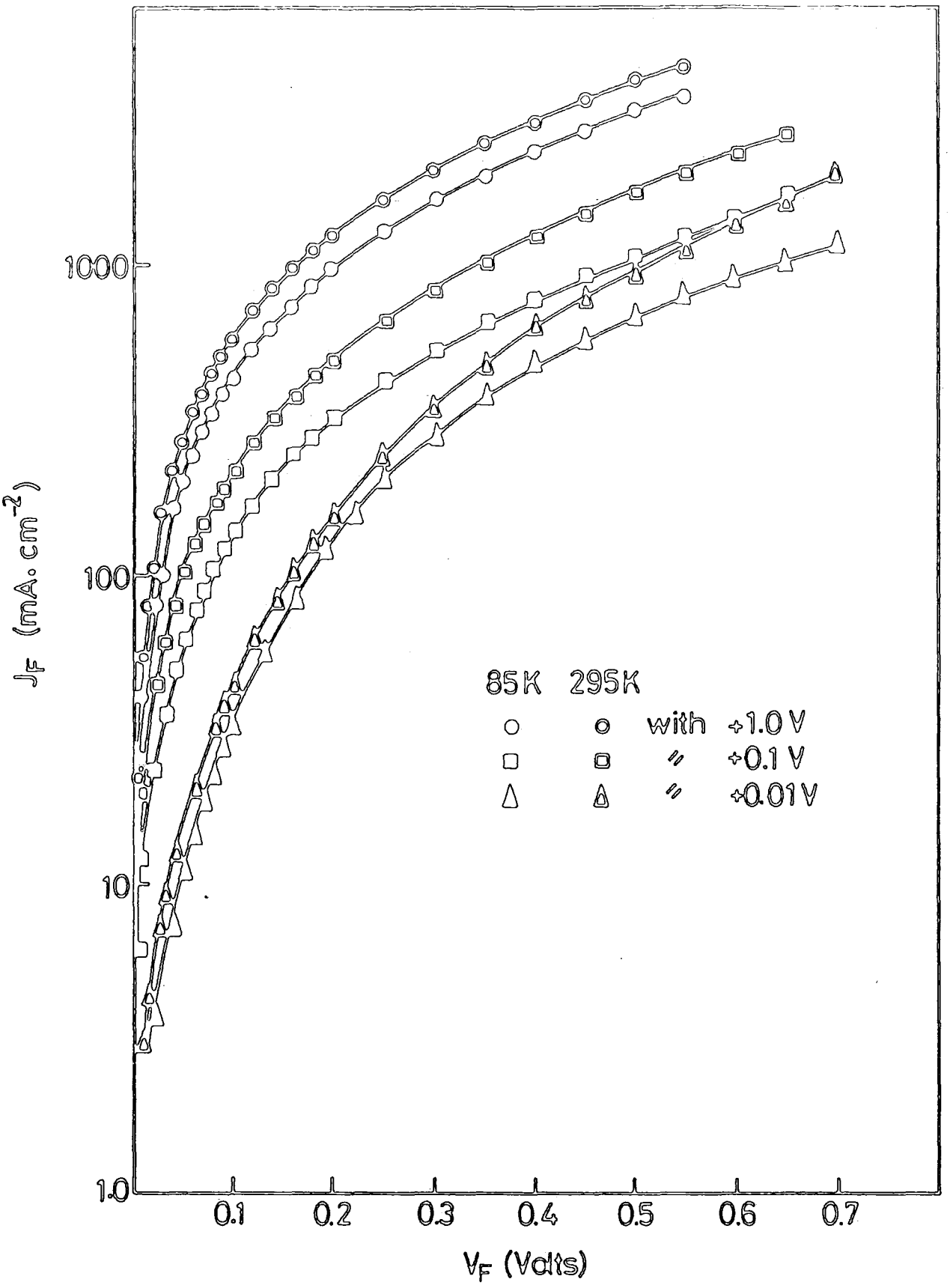


Fig 7.17 : Dark current-voltage characteristics for as-prepared CdS-Cu_xS devices fabricated with different electroplating bias measured at 295 and 85 K

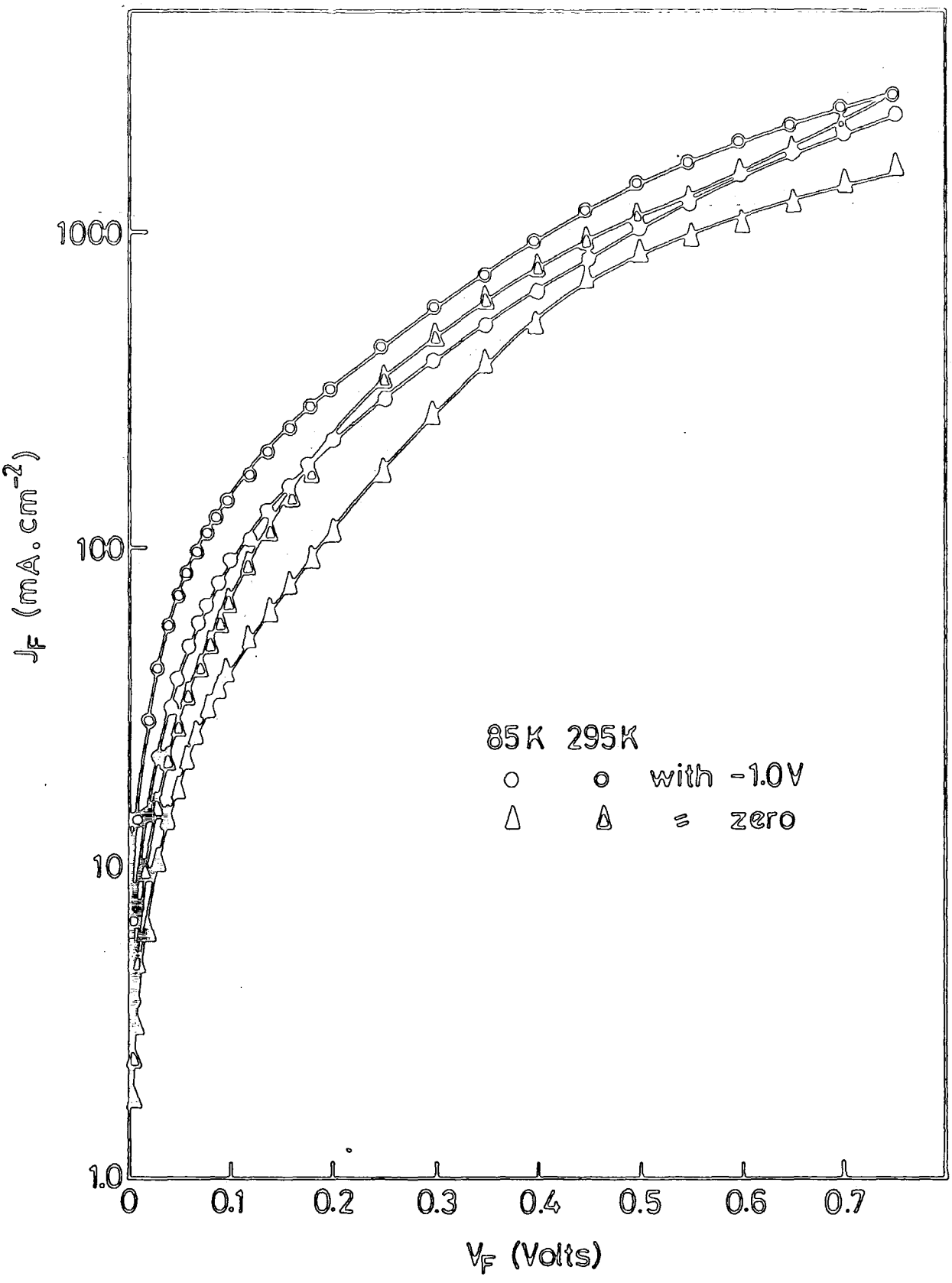


Fig 7.18 : Dark current-voltage characteristics for as-prepared CdS-Cu_xS devices fabricated with different electroplating bias measured at 295 and 85 K

where

$$J_o = J_{oo} \exp \frac{-\Delta E}{kT}$$

J_{oo} is defined by the type of conduction process, and ΔE is the energy at which the space charge region is thin enough to permit tunnelling of electrons to the empty interface states for this process. The current factor (J_o) is determined from the intercept of the straight line to zero bias and the diode factor (A) is calculated from the slope of these curves. The variation of diode and current parameters as a function of electroplating bias are illustrated in the Tables 7.2 a and b.

Electroplating bias (V)	J_o mA.cm^{-2}	A
+3.0	11.0×10^{-1}	0.96
+1.0	7.20×10^{-1}	4.03
+0.1	3.55×10^{-1}	6.57
+0.01	1.60×10^{-1}	9.55
0.0	2.35×10^{-1}	9.10
-1.0	3.90×10^{-1}	7.16

Table 7.2(a)

Electroplating bias (V)	J_o(mA.cm^{-2})	A
+3.0	12.0×10^{-1}	2.10
+1.0	6.30×10^{-1}	8.30
+0.1	2.60×10^{-1}	20.93
+0.01	1.50×10^{-1}	23.96
0.0	2.40×10^{-1}	26.86
-1.0	1.80×10^{-1}	12.64

Table 7.2(b)

Table 7.2 : The variation in current and diode factors with the value of electroplating bias used during CdS-Cu_xS fabrication measured at a: room temperature b: liquid nitrogen temperature.

Table 7.2a shows that the diode factor increased from 0.96 to 9.55 when the electroplating bias was reduced from +3.0 to 0.01V. When the plating bias was taken to a negative value the diode factor decreased further. Similar behaviour was observed when the experiment was carried out at liquid nitrogen temperature. In this case the diode factor reaches a value of 23.96 when a bias of +0.01V was used and it then decreased to 12.65 for a bias of -1.0V. On the other hand, the current factor (J_o) exhibited a complementary relationship with the value of electroplating bias. It decreased from 1.10 to 0.16 $mA.cm^{-2}$ when the bias was reduced from +3.0 to +0.01 and then it increased again to 0.39 when a negative bias of -1.0V was used. Similar behaviour was observed when the measurements were carried out at 85K.

The variations in forward current with temperature at fixed forward voltage for devices which were fabricated with different electroplating biases are shown in Figures 7.19, 7.20 and 7.21. Figure 7.19 indicates that J_F was practically independent of temperature for these devices which were prepared with +3.0V. As these devices were poor diodes, only small values of fixed voltage were used (0.05, 0.1 and 0.15V). When the electroplating bias was reduced to 1.0 and then to -0.1V, two distinct regions were observed for all values of fixed voltage (see Fig 7.20). In the first region at temperatures between ∿85K and ∿120K, the current flowing through the junction was dependent on the temperature, but in the second region (∿120-300K) this dependence was less rapid as measured at fixed forward voltages of 0.1, 0.3, 0.5 and 0.7V. With devices prepared using a larger negative bias of -0.1V (Fig 7.21), three distinct regions in the J_F temperature plot were detected. In the regions below 170K and above 220K the temperature dependence was relatively slight but within this range it was quite pronounced.

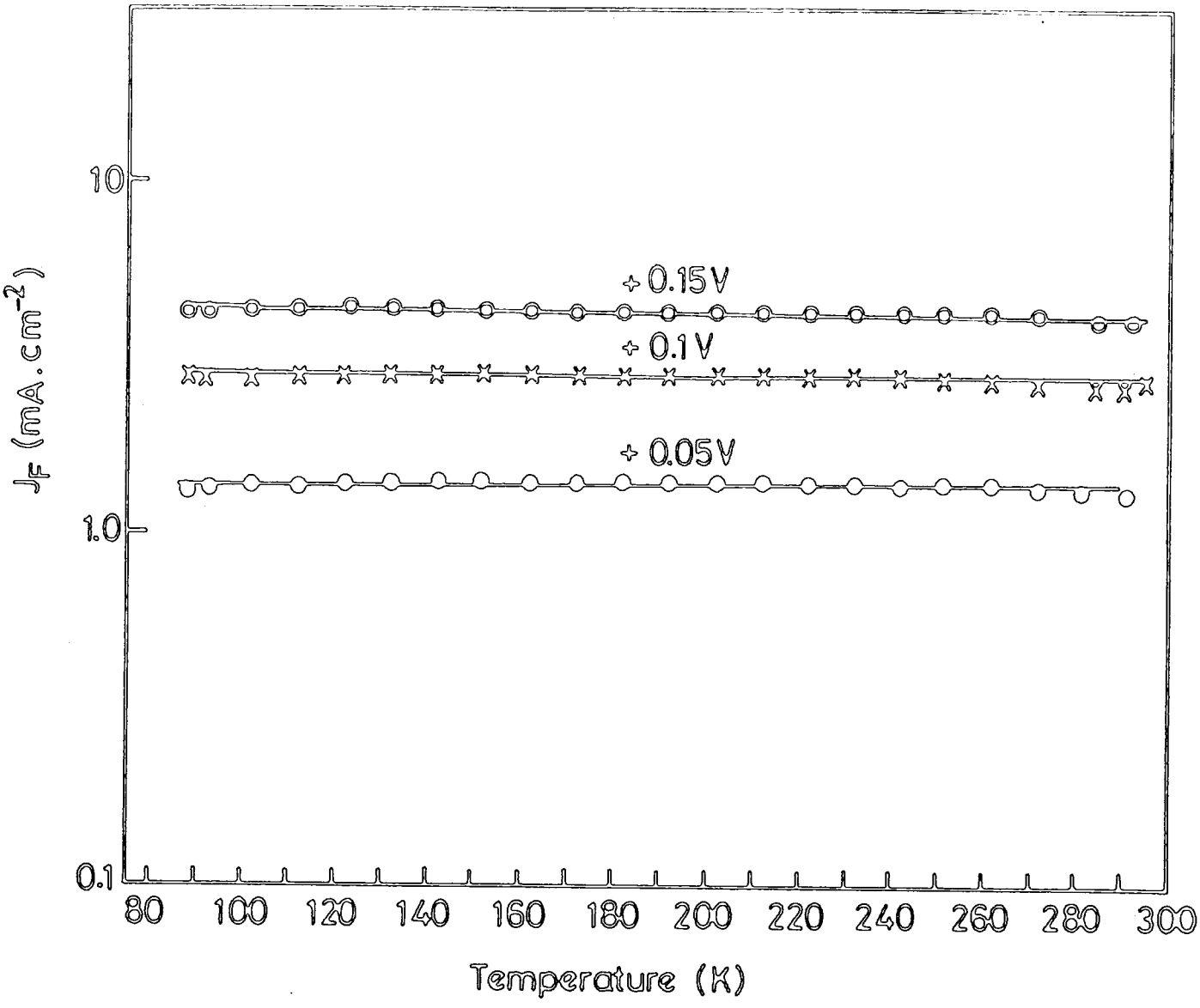


Fig 7.19 : Dark forward current-temperature curves for CdS-Cu_xS device prepared with +3.0V electroplating bias at the different forward applied voltages shown.

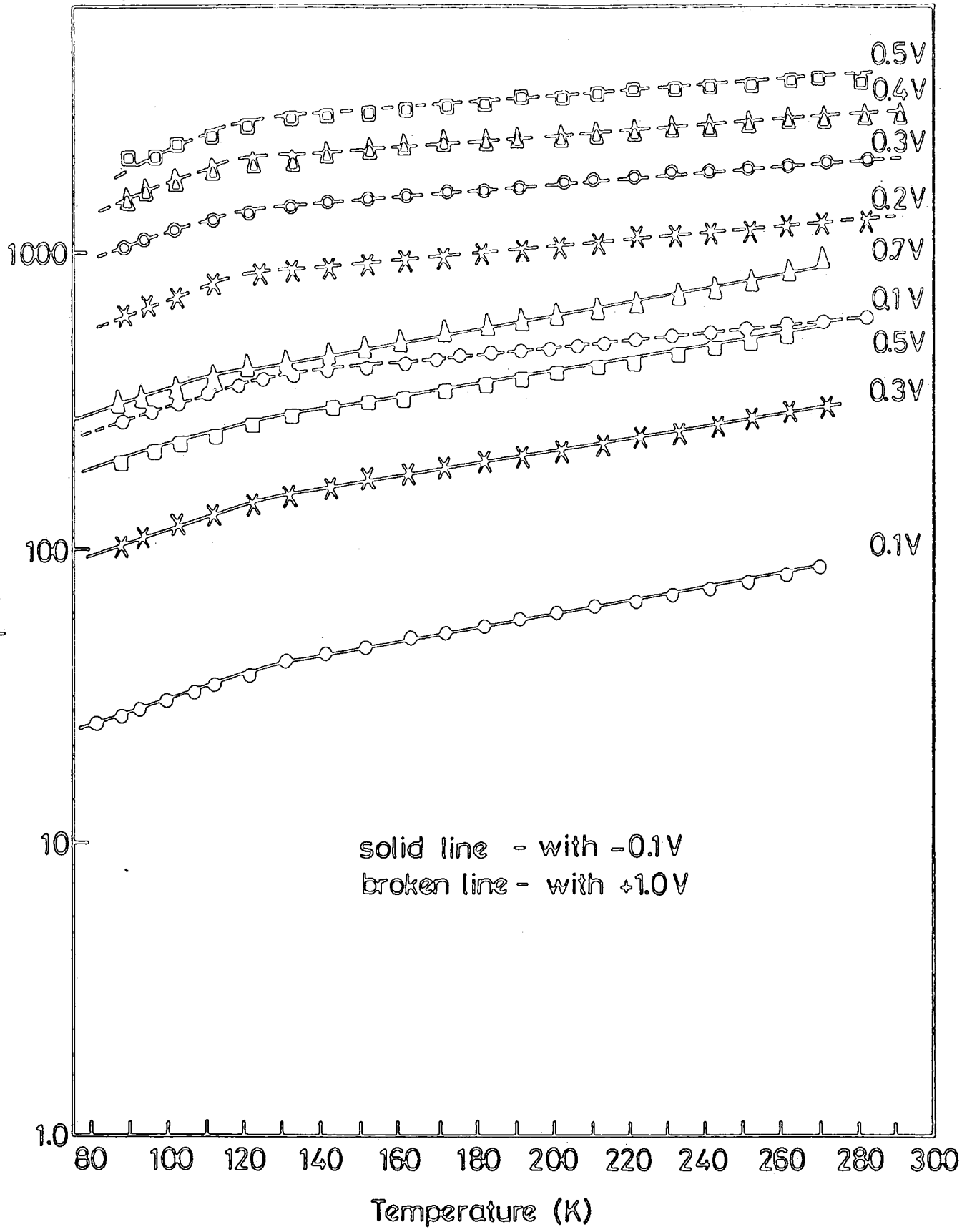


Fig 7.20 : Dark forward current-temperature curves for CdS-Cu$_x$S devices prepared with plating bias of -0.1V (solid lines) and +1.0V (broken lines) for the different applied voltages shown.

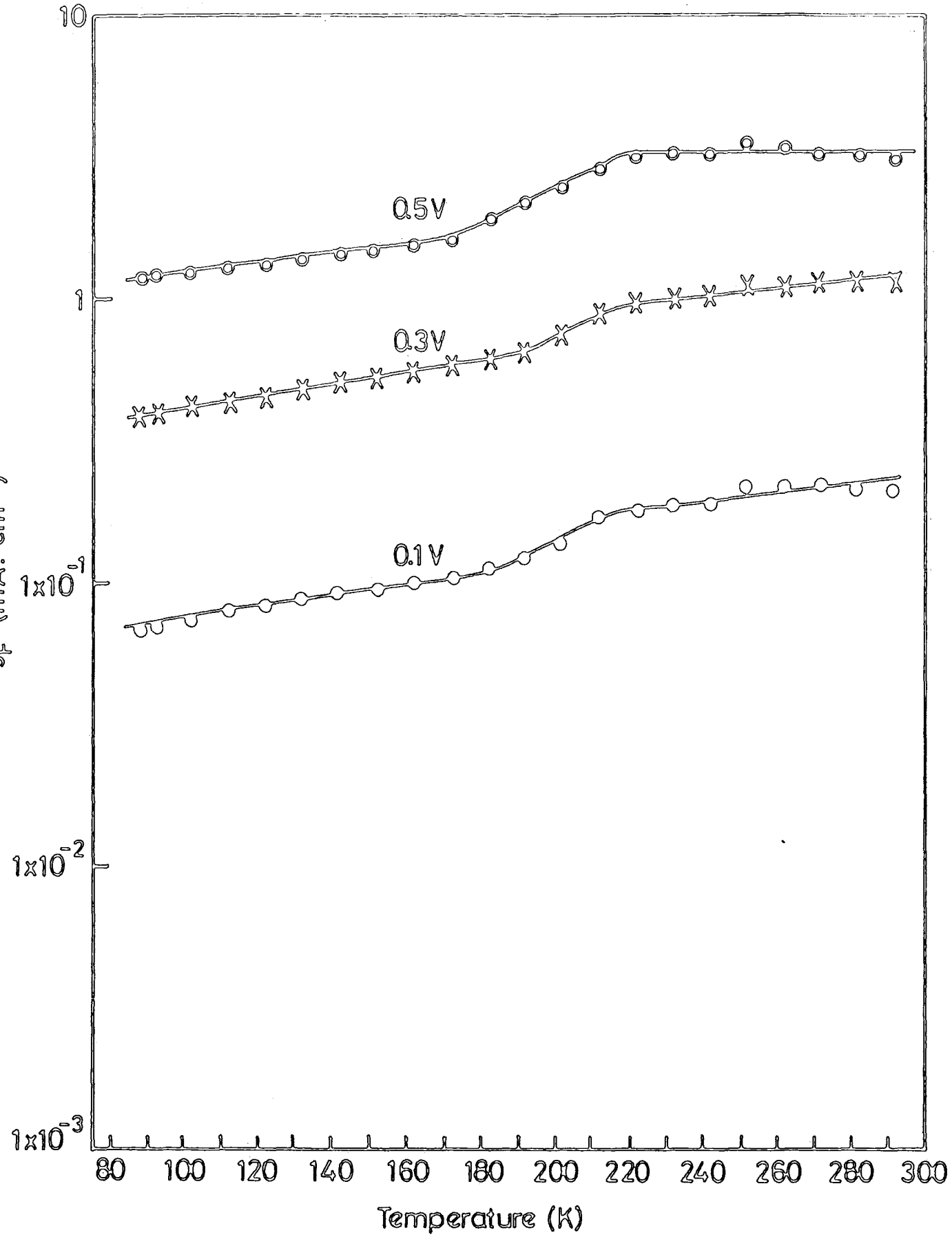


Fig 7.21 : Dark forward-temperature curves for CdS-Cu_xS device prepared with -1.0V electroplating bias measured at the different forward applied voltages shown.

7.8 Discussion

Degradation has long been recognized as a major difficulty with CdS-Cu_xS solar cells [6,7,8]. So in an attempt to obtain a better understanding of this problem, the effects of ambient and illumination on device properties have been investigated. The reason why devices aged under illumination degraded more rapidly than those kept in the dark could be attributed to the increased absorption of oxygen at the surface of Cu_xS in the light. Palz et al [4] found that exposing the Cu_xS surface to strong oxidizers like O_2 caused a substantial loss in the CdS-Cu_xS device performance. They suggested that an oxidized copper compound was probably being formed which decreased the x value of the underlying Cu_xS and increased the concentration of Cu^{+2} ions over Cu^{+} ions. Also Burton and Windawi [9] found that the deterioration in the Cu_xS stoichiometry could be attributed to the formation of an oxide layer on the free surface of the Cu_xS which led to an increase in the sheet resistance of this layer [10]. This would also have a deleterious effect on the series resistance of the device.

The Cd atoms were found to be able to move rapidly to both the Cu_xS surface and the CdS-Cu_xS interface on exposure to air at room temperature [11]. Such an effect has strong implications for the fabrication process and degradation mechanisms in these cells [11,12]. The observation of Cd migration may be explained in the following manner. The reaction of Cu_xS with air to form copper oxide is widely reported [4,13,14,15,16,17,18] and can be described by [11]:

$$Cu_{\alpha+\beta+2\gamma}S + \frac{\beta+\gamma}{2} O_2 \longrightarrow Cu_\alpha S + \beta CuO + \gamma Cu_2O \qquad (1)$$

The possible reaction of the copper oxides with CdS can be specified as:

$$Cu_wO + CdS \longrightarrow Cu_wS + CdO \qquad (2)$$

The net result of equations 1 and 2 is:

$$Cu_xS + \frac{\gamma}{2} O_2 + \gamma\, CdS \rightarrow (1+\gamma)\, Cu_{\frac{x}{1+\gamma}}\, S + \gamma\, CdO \qquad (3)$$

This reaction was suggested by Florio et al [19] as the reason for CdS-Cu_xS heterojunction degradation.

The E.S.C.A. results show that the amount of oxygen absorbed by the Cu_xS surface was greater for the device kept in the light than it was for that kept in the dark. This may explain why the short circuit current and open circuit voltage decreased significantly for the device kept in the light. The greater degradation caused by exposure to light at room temperature is in agreement with the results of Fahrenbruch and Bube [20]. They found extensive degradation in I_{sc} for cells exposed to constant illumination. When devices were exposed to the action of various oxidizers such as Cl_2, Br_2, I_2 and O_2 they also showed a substantial reduction in I_{sc} [4,21]. The explanation for the drop in current could well be the oxidation of Cu_2S to $C_{2-\gamma}S$, where γ is the copper deficiency. These observations are consistent with electrochemical work [4,14,15] which suggested that the degradation of cells in air is the result of the formation of copper oxide on the Cu_xS surface. Windawi [17] suggested that the degradation of cell output in the presence of oxygen is both temperature and time dependent and that I_{sc} would be expected to degrade according to : [9,17]

$$I_{sc} = I_{sco} \exp\left(-\frac{t}{\tau}\right)^{\frac{1}{2}}$$

where τ is a temperature dependent decay time constant and I_{sco} is the initial short circuit current.

Similarly E.S.C.A. studies demonstrated that the heat treatment of a CdS-Cu_xS device at 200°C in air for two minutes led to an increase in the amount of oxygen on the surface.

It is obvious from the spectral responses of V_{oc} (see figures 7.3 and 7.4) that the device which was aged in the light exhibited a phase conversion from chalcocite to djurleite with time. This could be attributed to the formation of copper oxide on the Cu_xS by removal of copper from the copper sulphide layer resulting in a reduction in the value of x to less than 2.0. Cook et al [22] found that the crystal structure of chalcocite crystals aged in air for two years changed to pure djurleite. It is well established that the different phases of Cu_xS have different values of energy bandgap and hence optical absorption properties [23]. In fact, an increase in the copper deficiency produces an associated increase in the effective bandgap of Cu_xS [24].

In contrast with devices kept in the light, than which were kept in dark showed only minimal degradation as evidenced from the spectral responses in Figure 7.3 and 7.4. It is suggested that any oxide layer formed was very thin. These conclusions are consistent with the E.S.C.A. results.

With a device kept in argon at 50°C, the degradation can be attributed to the diffusion of copper from the Cu_xS into the CdS to form acceptor states. These reduce the concentration of electrons which results in an increase in the magnitude of the space charge barrier on the CdS side of the junction. However, the loss of copper by this mechanism leads to a detrimental effect by reducing the Cu/S atomic ratio which leads to a reduction in the photon absorption coefficient and, thus, to a fall in the light-generated current [25,26]. In contrast

the device kept in argon at room temperature remained stable. This can be attributed to the reduction in the diffusion of copper at this temperature. It is also important to note that ageing of the device in argon at room temperature did not cause the spectral response to change as much as did ageing in air under otherwise the same conditions (see figures 7.3 and 7.7). This is attributed to the argon ambient preventing oxidization of the Cu_xS layer at room temperature which in turn leads to the better fill factor as observed.

Generally the migration of copper from Cu_2S causes three major changes in the junction behaviour [27], which finally lead to degradation in the cell performance. They are as follows:

i) The extraction of copper from Cu_2S reduces its photoabsorption and the diffusion length of minority carriers, which leads to a continuous decrease in the I_{sc};

ii) Widening of the compensated layer caused by copper doping of the CdS in the vicinity of the junction results in a reduction in the junction field and increased carrier trapping effects, both reducing V_{oc} and FF;

iii) The formation of shorting paths, causes internal current leakage and reductions in shunt resistance. These processes would give rise to a significant degradation.

The performance of a device which was kept in argon at 50°C could be restored by annealing in hydrogen/nitrogen. It is known that the photovoltaic properties of CdS-Cu_2S cells change dramatically on exposure to air in contrast to comparable treatments in hydrogen or vacuum [28,29, 30]. The recovery can qualitatively be explained by an increase in the diffusion length [11,28]. A similar recovery was also noted by Meakin and Philips [16]. The increase in I_{sc} may be attributed to an improvement in the Cu_xS phase [10,31]. This is clear in Figure 7.10

which shows a dramatic reduction in the response due to djurleite with annealing time in H_2/N_2. Usually one of the advantages of hydrogen annealing is to reduce previously formed copper oxide [10,32]. However, as this device had been annealed in argon at 50°C, there was no possibility of forming copper oxide. Consequently, the improvement must have been due to another parameter. It has also been shown that the use of H_2 reduces the rate of interdiffusion of Cu and Cd across the CdS-Cu_2S interface [33,34]. Independent evidence of the copper diffusion is provided by the I-V characteristics (Figure 7.9). The increase in the extent of the cross-over between dark and light I-V characteristics can be explained in terms of copper diffusion from the Cu_xS to the CdS to establish an i-layer. Another possible explanation for the improvement in the spectral response, which shows a decrease in the djurleite response (figure 7.10), is that there is a loss of sulphur from the Cu_xS in the presence of H_2, thus increasing copper/sulphur ratio. This loss of sulphur under similar conditions has been suggested previously by Pande [35].

The studies of the etching of mechanically polished $(000\bar{1})$ surfaces of CdS with HCl, showed that the size of the hillocks depended on the period of etching (see Figures 7.12 a,b,c and d). The dependence of device properties on etching has been studied by other workers [36,37,38] Cheng et al [37] related variations in device properties to the difference in the structure of the Cu_xS on the tops of the hillocks and on their smooth sides. The mechanically damaged layer was found to consist of polycrystalline disordered wurtzite CdS [39]. The presence of this polycrystalline surface may led to different I-V characteristics (Figure 7.13). The cross-over between dark and light characteristics is frequently observed after heat treatment, but the present study shows that cross-over was obtained even in the as-made condition, for the

device which was prepared on the mechanically polished sulphur face of a CdS single crystal. Further, the extent of this cross-over reduced with increasing periods of etching. Cross-over in the I-V characteristics of a device formed on a polished surface, or on a lightly etched one, can be attributed to the disordered surface. When this disordered material was completely removed after etching for 40 seconds, the cross-over effect was not observed. Thus it may be concluded that the surface preparation is one of the most important parameters determining the performance of the CdS-Cu_xS heterojunctions.

By increasing the dipping period a considerable reduction in short circuit current was observed (Figure 7.14). This may be due to the diffusion of copper into the CdS extending to considerable depth. Coinciding with the reduction in I_{sc}, there was a simultaneous increase in the response due to djurleite, which became larger with extended dipping periods. This shows a more copper deficient layer was established. The appearance of a peak at 0.49μm confirms the presence of a copper deficient phase since the resulting reduction in the absorption coefficient of the Cu_xS [40] allows more light to be transmitted to the CdS.

The effect of electroplating bias on the dark current-voltage characteristics was to change the current and diode factor. It is suggested that by using electroplating to fabricate devices, a different diode behaviour is observed. Rastogi [41] found a significant reduction in J_o by using the electroplating technique. For such devices, the conduction at low voltages follows ohm's law, whereas at higher voltage it follows a diodic behaviour. The behaviour in both ranges can be described by: [42]

$$I = \frac{V}{R_{sh}} + A \exp(\alpha v)$$

where R_{sh} is the shunt resistance in parallel with the diode. The ohmic behaviour of the dark forward characteristics at small voltages measured for different electroplating bias may be attributed to the tunnelling of charge carriers from the bottom of the CdS conduction band to the interface recombination centres. As the applied voltage increases, the gradual increase in forward current indicates that the conduction is more sensitive to the density of interface states than to a reduction in the effective barrier height. The variation in the diode factor with different electroplating bias can be explained in terms of different properties of the interfaces.

For a device fabricated with a bias of +3.0V, the temperature independent current indicates that tunnelling is occurring from the bottom of the conduction band. Devices made with a range of electroplating bias from +1.0 to -0.1V show two distinct regions. In the temperature range 85-120K the temperature dependence of the current suggests a thermally activated process, in which the carriers must be excited to certain energy levels before tunnelling to recombination centres. Over the remaining temperature range (120-295K) the weak dependence of the current on temperature indicates that tunnelling occurs predominantly at energies close to the bottom of the conduction band of CdS. Thus, there is only a very small potential barrier to be overcome before tunnelling. However, for a device fabricated with an electroplating bias of-1.0V, three distinction regions were observed. In the region between 180-220K the current depends on temperature, whereas in the other two regions the dependence was only weak.

7.8 Conclusion

The degradation of the photovoltaic properties of the CdS-Cu_2S solar cells with storage in light and in the dark has been studied.

It has been shown that devices kept in the dark at room temperature degraded much less than those kept under illumination. This is attributed to the formation of copper oxide on the Cu_xS surface. E.S.C.A. studies confirmed that the device kept under illumination contained more oxygen at its surface than that aged in the dark. It has also been shown that when ageing a device at room temperature, argon has a more beneficial effect than air on the stability. This is because of the prevention of the formation of copper oxide on the Cu_xS surface when using argon as an ambient. On increasing the temperature of storage in argon, copper diffused from the Cu_xS to the CdS. This led to the degradation of the devices by a different mechanism. It can therefore be concluded that cells remain most stable when stored in argon at a temperature of about 25^oC.

It has been shown that the effect of degradation of a device after heat treatment in argon at 50^oC for a long period can largely be reversed by re-heating in a H_2/N_2 (80%/20%) mixture. This is due to the loss of sulphur from the Cu_xS surface thus restoring its copper content. The extent of the cross-over between the dark and light I-V characteristics is a function of the period of etching. The disappearance of cross-over has been attributed to the removal of the damaged layer on the CdS surface. The variation in V_{oc} and I_{sc} were found to be dependent on the dipping period. In the study of the effect of electroplating bias on the dark I-V characteristics, the variation of current and diode factor has been established as a function of the bias value. Finally, the dependence of forward current on the temperature at fixed forward voltage has also been investigated.

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CHAPTER EIGHT

$Cd_yZn_{1-y}S$ - Cu_xS Solar Cells

8.1 Introduction

Many researchers have investigated CdS-Cu_xS solar cells and it has been established that the characteristics of these devices are fundamentally limited by the difference in the electron affinities and the lattice mismatch between CdS and Cu_xS. A lattice mismatch of about 4% exists between them, and this results in an interface state density of approximately $5 \times 10^{13} cm^2$. In addition the difference in electron affinity causes a step in the potential energy at the junction [1]. These parameters essentially limit the maximum open circuit voltage which can be obtained [2,3]. To overcome this limit $Cd_yZn_{1-y}S$ can be used as the window material. Palz et al [4] were the first to suggest that the introduction of Zn into the CdS gives rise to better lattice and electron affinity matching, and that this should have two beneficial effects. Firstly, the interface state density is reduced, which should decrease recombination effects and thus improve the current collection, and secondly the junction barrier height is raised so that the V_{oc} of the device is increased. Rothwarf's results [5] confirmed these effects in this film devices. High values of V_{oc} (0.548) have also been achieved for $Cd_yZn_{1-y}S$-Cu_2S single crystal solar cells [6].

It has also been shown that the $Cd_yZn_{1-y}S$ bandgap changes with increase in zinc content [7,8,9], and the variation with composition is given by

$$E_g(Cd_{1-y}Zn_yS) = E_g(CdS) + y\Delta E_g$$

where

$$\Delta E_g = E_g\ (ZnS) - E_g(CdS)$$

In this study, the process of annealing in different ambients and also the effect of electroplating bias have been studied for devices formed on $Cd_{0.8}Zn_{0.2}S$ single crystals. In order to investigate the suitability of this substrate, measurements of photocapacitance, current-voltage (I-V) and spectral response were carried out.

8.2 $Cd_yZn_{1-y}S$ Substrate Preparation

$Cd_yZn_{1-y}S$ single crystals were grown by the same vapour phase technique used for CdS, and (0001) oriented dice were produced from them in a similar manner. It is worth noting that the grain size decreased as the zinc content increased [10]. The mechanical polishing and chemical etching processes were the same as those used for CdS substrates (see section 5.2) as were the heterojunction device fabrication procedures using the wet barrier technique (see section 5.3.1). In addition, to improve both the stoichiometry of the Cu_xS phase and the device parameters, the electroplating technique was applied during the formation of heterojunctions in the manner described in section 5.3.1.

8.3 Photovoltaic Characteristics

8.3.1 Steady State Photocapacitance

The photocapacitance measurements were made by recording the capacitance transient as the wavelength of the monochromatic illumination was decreased. The two processes which are operative during photocapacitance are the emptying and filling of traps. The increase in photo-

capacitance correlates with the excitation of electrons from an acceptor level to the conduction band. In contrast a decrease in photocapacitance corresponds to the excitation of electrons from the valence band to empty traps in the forbiddening gap. The spectral response of the photocapacitance was measured for typical $Cd_{0.8}Zn_{0.2}S$-Cu_2S heterojunction devices in the as-made condition and after annealing at 200°C for different periods of time in argon and in air. Spectra measured at room and liquid nitrogen temperature are shown in Figures 8.1 and 8.2 respectively, for a device after air heat treatment for 2 and 5 minutes. All the curves in Figure 8.1 show that there was quenching of photocapacitance with a threshold of $\sim$0.70eV which was not detected at 85K (see Fig 8.2). Another negative-going step in the photocapacitance measured at 295K occured at an energy of 1.0eV. This means that there were two traps located at 0.70eV and 1.0eV above the valence band. Significant increases in the photocapacitance were observed at photons energies $\sim$1.4eV and 2.3eV, which indicated that there were probably acceptor levels at energies of 1.13eV and 0.23eV above the valence band edge. The decreases in the photocapacitance at 2.0eV and at 2.48eV suggest the presence of two donor levels at 0.53eV below the conduction band and another close to this band. For measurement at room temperature, the spectra were not found to change significantly after heat treatment. When measurements of the same device were made at 85K, a prominent positive-going threshold was observed at 1.05eV indicating the presence of an acceptor level at 1.58eV above the valence band (assuming that the band gap of $Cd_{0.8}Zn_{0.2}S$ at 85K is about 2.63eV). Further increases in photocapacitance were observed at photon energies of 1.46, 2.05 and 2.38eV implying that there were three more acceptor levels located at 1.17, 0.58 and 0.25eV above the valence band. In addition, quenching processes were observed at photon energies of 1.32, 1.85, 2.12 and 2.52eV which correspond to donor levels situated at

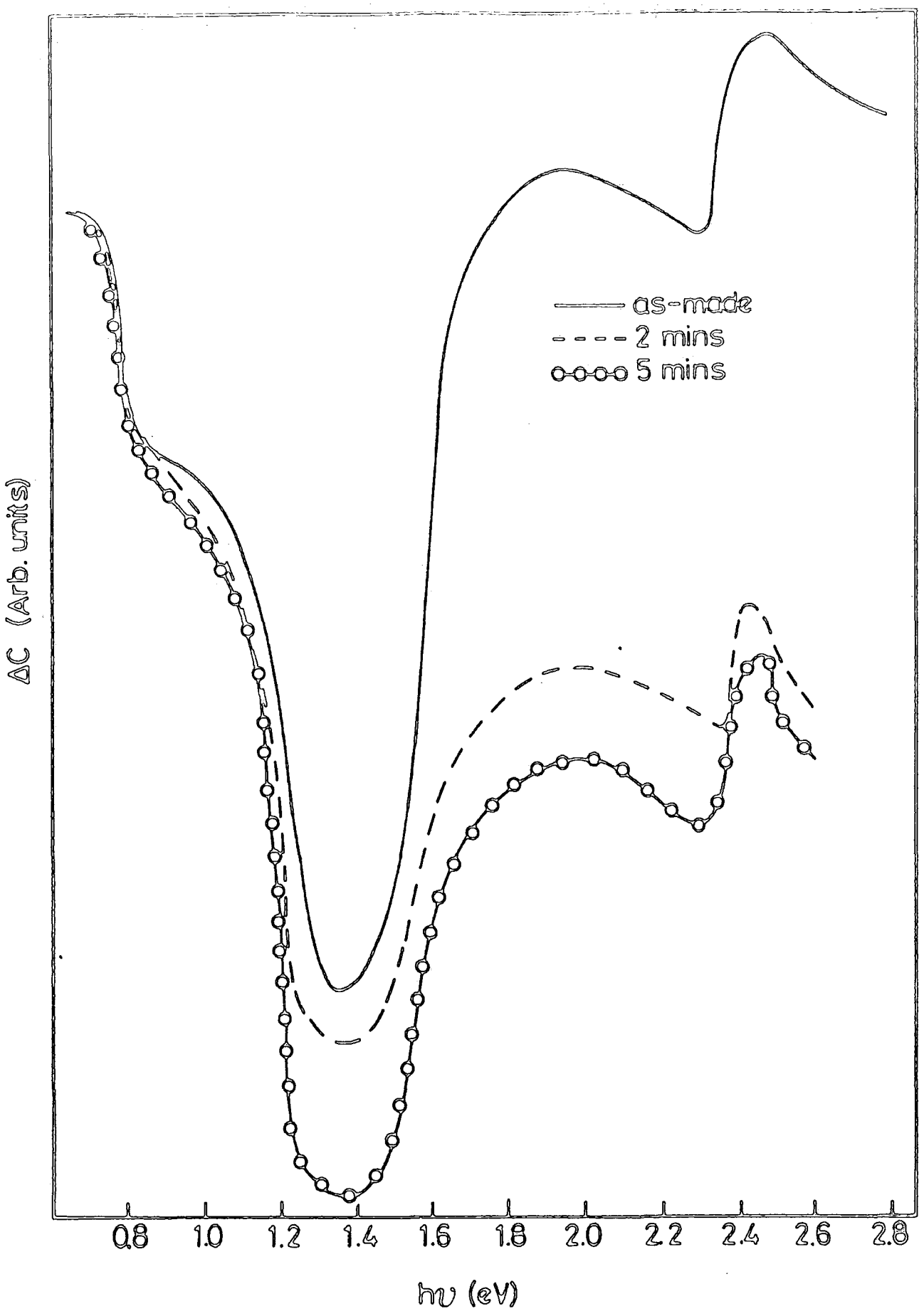

FIGURE 8.1 : Photocapacitance curves for a $Cd_{0.8}Zn_{0.2}S$-Cu_2S device measured at 295K after heat treatment in air at 200°C for different periods.

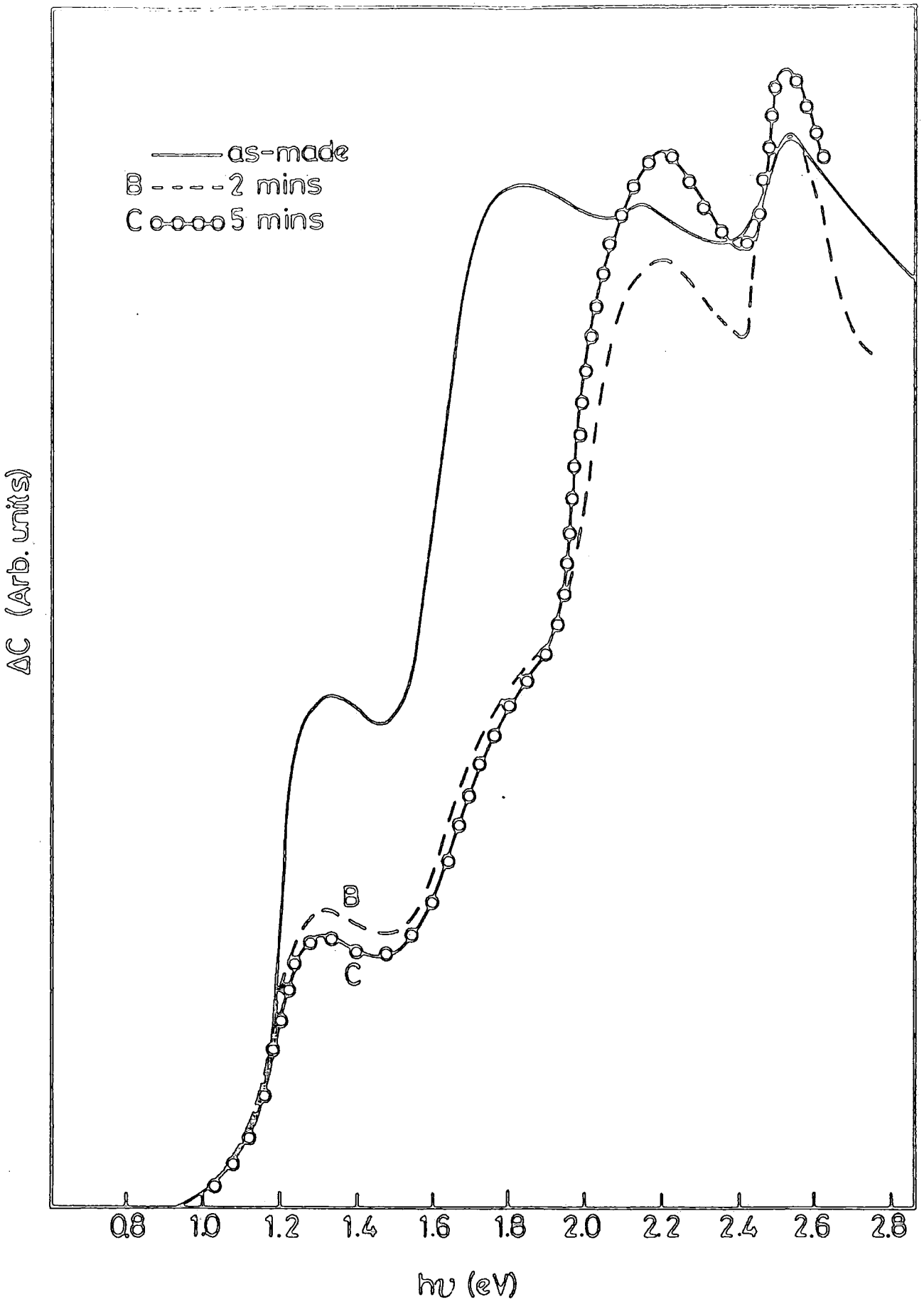

FIGURE 8.2 : Photocapacitance curves for a $Cd_{0.8}Zn_{0.2}S$-Cu_2S device measured at 85K after heat treatment in air at 200°C for different periods.

1.31, 0.78, 0.51 and 0.11eV below the conduction band. The quenching at 1.32eV and enhancement at 1.46eV are probably due to the response of the same centre although the sum of the threshold energies is slightly larger than the band gap.

It is understood of course, that changes in the shape of the photocapacitance spectrum may not be associated with the onset of a new filling or emptying process. There may simply be gradual changes in the transition probabilities. Curves B and C in Figure 8.2 show that air heat treatment for 2 and 5 minutes led to a considerable change in the form of the photocapacitance spectra and an additional threshold was obtained after 2 minutes heat treatment; at a photon energy 1.9eV, which indicated the introduction of a new acceptor level at 0.73eV above the valence band.

In a control experiment a device was prepared under the same conditions except that it was annealed in argon instead of air. Its photocapacitance spectra measured at 295K and 85K are shown in Figures 8.3 and 8.4 respectively. Apart from the difference in the relative magnitudes of ΔC at photon energies > 1.4eV at 295eV these spectra closely resembled those of the devices which had been heated in air. At 85K (Figure 8.4), the introduction of a new acceptor level was achieved more gradually and very slowly in comparison with heat treatment in air. The level located at 0.78eV below the conduction band may play an important role in the photovoltaic behaviour of a cell, especially as it has been demonstrated from spectral response measurements that the decline of the copper sulphide stoichiometry proceeded very slowly when an argon ambient was used.

8.3.2 Spectral Response and Current-Voltage Characteristics

RHEED studies of copper sulphide layers formed on the sulphur

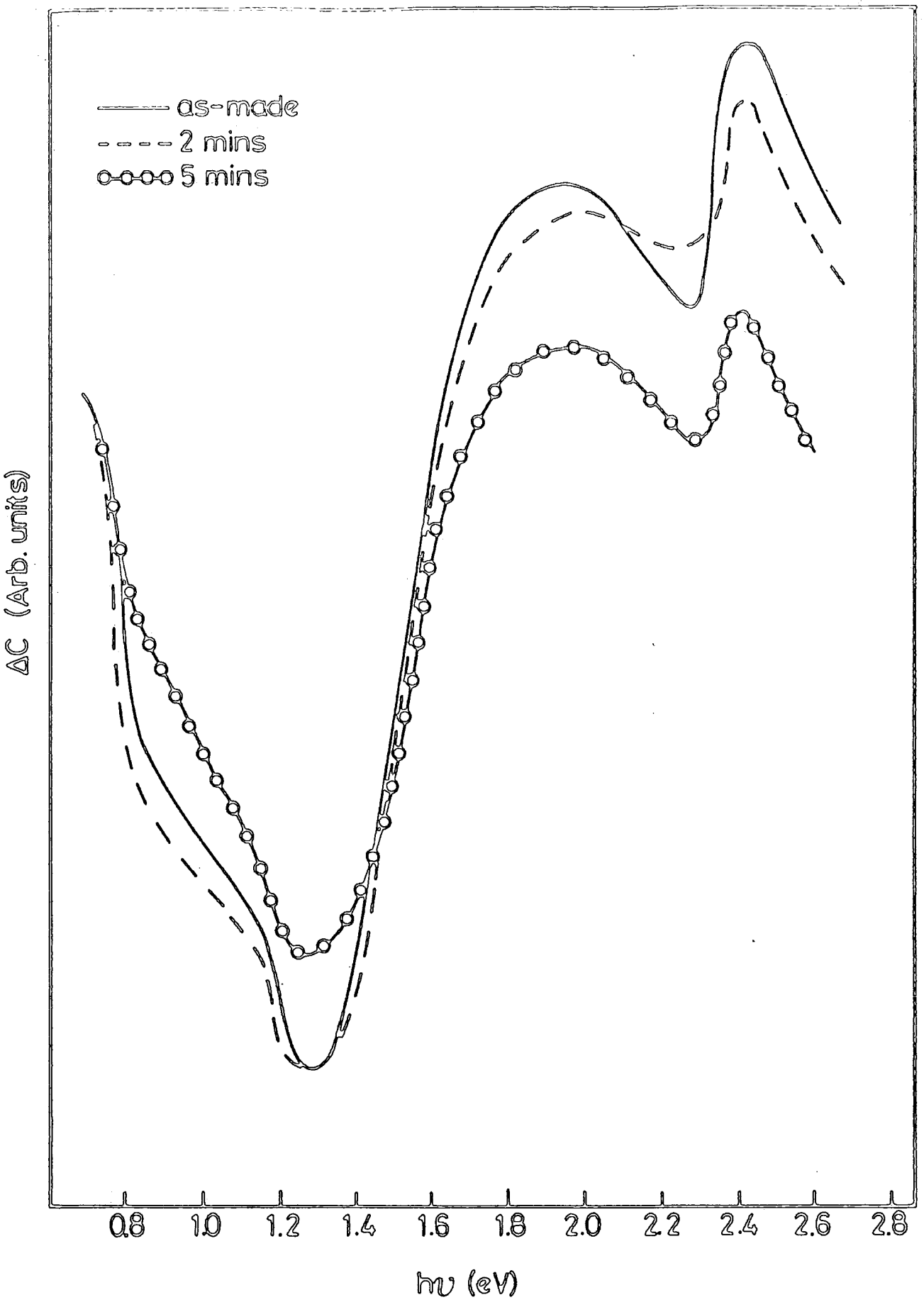

FIGURE 8.3 : Photocapacitance curves for a $Cd_{0.8}Zn_{0.2}S$-Cu_2S device measured at 295K after heat treatment in argon at 200°C for different periods.

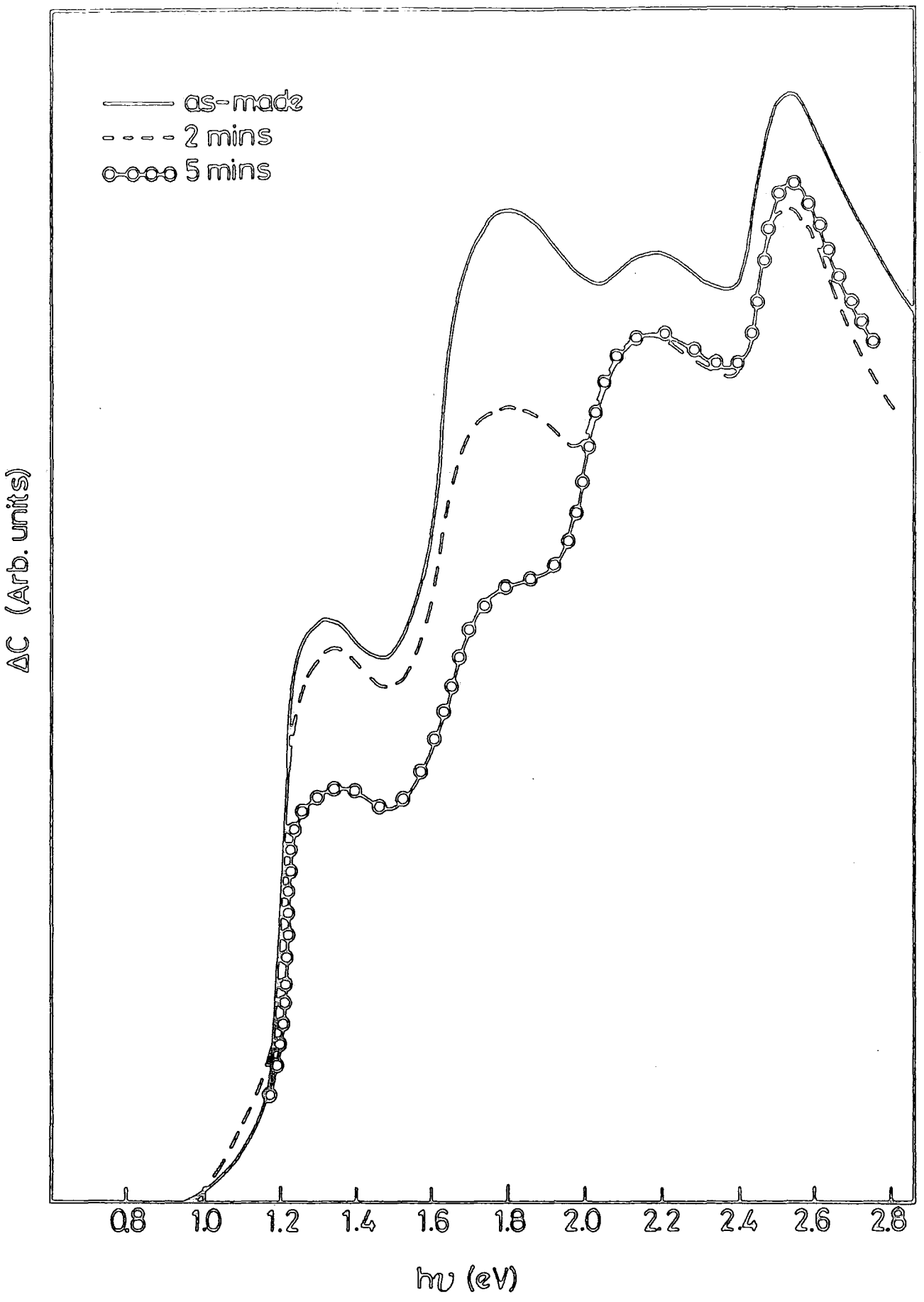

FIGURE 8.4 : Photocapacitance curves for $Cd_{0.8}Zn_{0.2}S$-Cu_2S device measured at 85K after heat treatment in argon at 200°C for different periods.

face of $Cd_yZn_{1-y}S$ single crystals confirmed that different phases of copper sulphide could be formed by varying the bias applied during electroplating, as had happened with CdS substrates. The spectral response of V_{oc} for devices fabricated on $Cd_{0.8}Zn_{0.2}S$ by applying different values of bias during heterojunction formation are shown in Figure 8.5. This figure demonstrates that the sample with the best chalcocite:djurleite ratio was formed using a plating bias of +0.01V. The small peak at 0.50μm can be attributed to light absorption in the underlying $Cd_{0.8}Zn_{0.2}S$. The determination of the Cu_xS phase in the differently formed devices was in good agreement with the RHEED investigation.

Heat treatments in air and argon at 200°C for various lengths of time were carried out for devices made with different phases of copper sulphide. The effects of annealing a device which had a mixture of chalcocite and djurleite phases are shown in Figures 8.6 an 8.7. The most important features revealed in Figures 8.6 and 8.7 are as follows:

i) At 295K (Fig 8.6) there is a significant change after air heat treatment. A deterioration of Cu_xS stoichiometry was observed. Argon annealing leads to a slight improvement in the stoichiometry.

ii) At 85K an important feature in the curves is observed (Fig 8.7). The chalcocite response joined the djurleite to give an envelope shape after 2 minutes air heat treatment. The same shape was obtained when the device was heated for 5 minutes, but in general it gave an inferior response. In contrast annealing in argon for the same length of time revealed that the spectra still had two peaks at wavelengths of 0.96μm and 0.78μm.

Current-Voltage characteristics measured in the dark and under AM1 illumination, for as-made heterojunctions fabricated on both CdS

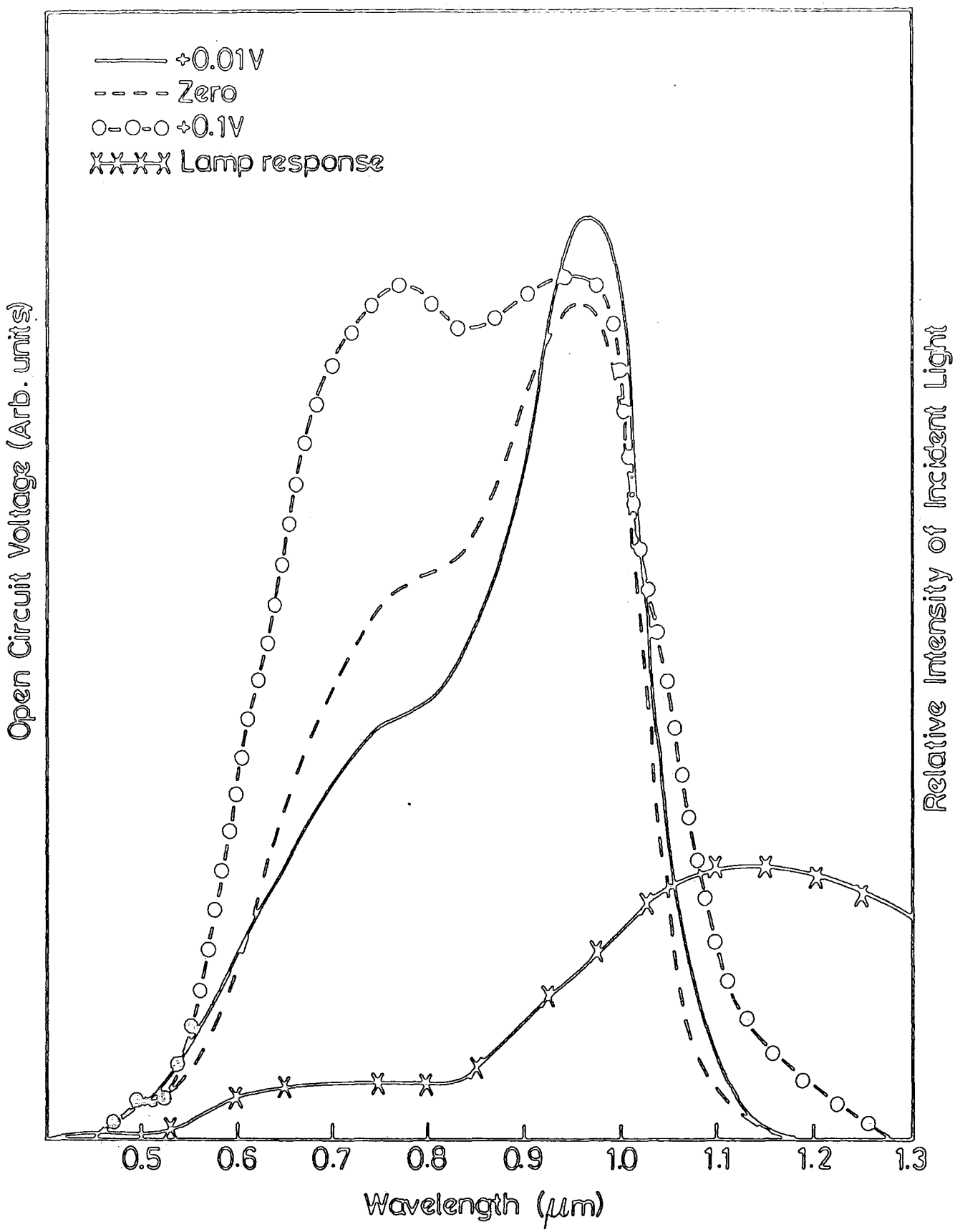

FIGURE 8.5 : Open circuit voltage spectral response measured at 85K of heterojunction formed on $Cd_{0.8}Zn_{0.2}S$ single crystal by electroplating method at as-made condition.

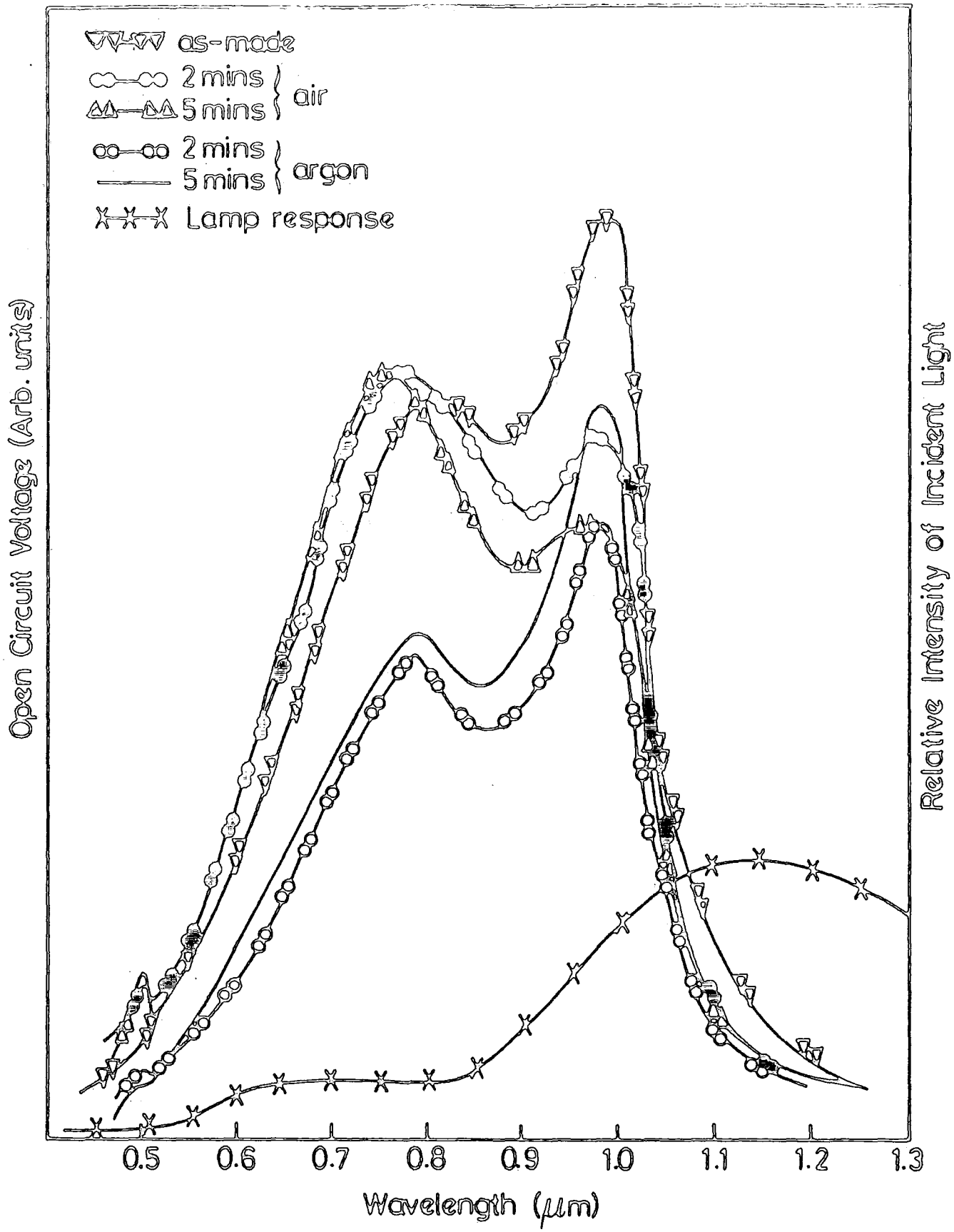

FIGURE 8.6 : The effect of annealing in argon and in air on the spectral response measured at 295K of devices made with a Cu_xS comprised of a mixture of chalcocite and djurleite.

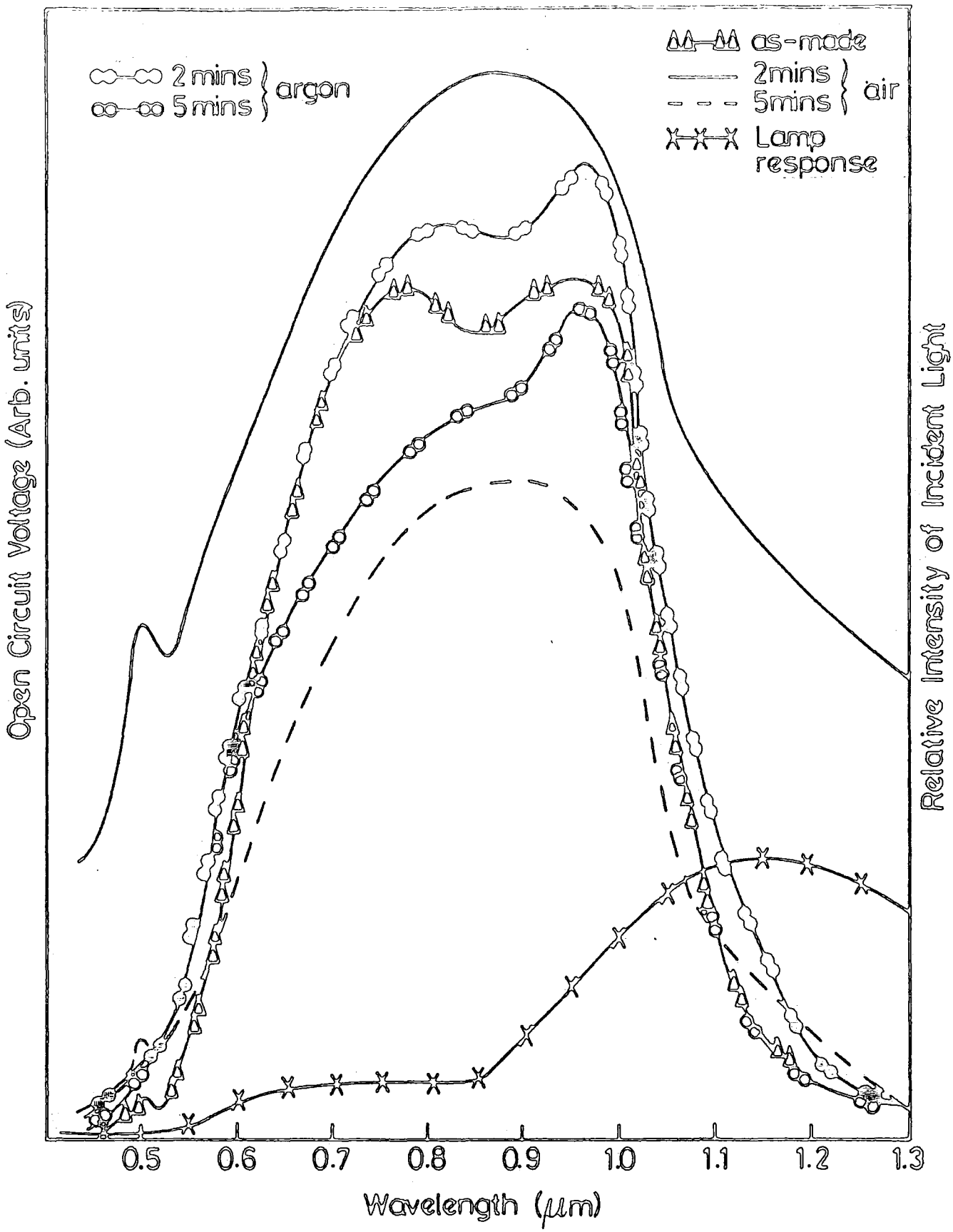

FIGURE 8.7: The effect of annealing in argon and in air on the spectral response measured at 85K of a device with Cu_xS comprised of a mixture of chalcocite and djurleite.

and $Cd_{0.8}Zn_{0.2}S$ using the optimum electroplating bias, are shown in Figure 8.8 for comparison. The value of V_{oc} increased from 0.48 to 0.56V and the I_{sc} decreased from 12.3 to 10.2mA.cm^{-2} when $Cd_{0.8}Zn_{0.2}S$ was used instead of CdS.

The effect of heat treatment in air for two minutes on the I-V characteristics of a device fabricated on $Cd_{0.8}Zn_{0.2}S$ substrate under the optimum conditions was to increase the V_{oc} from 0.56V to 0.60V and to decrease the I_{sc} from 10.2 to 7.9mA.cm^{-2} (Fig 8.9). In contrast to this, post-barrier heat treatment in argon led to no significant change in the V_{oc} but it did produce a slight decrease in the I_{sc} (9.5mA.cm^{-2}). For devices which had low values of V_{oc} and I_{sc} in the as-made condition, annealing either in air or in argon led to improvements in the V_{oc} typically from 0.24V to 0.45V and 0.39V respectively while the I_{sc} was not affected.

8.4 Discussion

It is known that the heat treatment of Cu_xS-$Cd_yZn_{1-y}S$ leads to the diffusion of copper from Cu_xS into the $Cd_yZn_{1-y}S$, forming a photoconducting i-layer. Te Velde [11] suggested that during heat treatment in air, oxygen is absorbed at the interface causing the introduction of acceptor states, which increase the band bending in the CdS. The photocapacitance results of this work demonstrated the presence of a negative-going response at 0.70eV at 290K. This corresponds to an internal transition between the copper ground and excited states. Grimmeiss et al [12] and Suda and Bube [13] found the threshold for this transition to be 0.75eV. The level which can be associated with copper impurity was found, in this work, to be located at $\sim$1.0eV above the valence band. At 85K, the positive going threshold and quenching of the photocapacitance at 1.4 and 1.35eV suggested the presence of

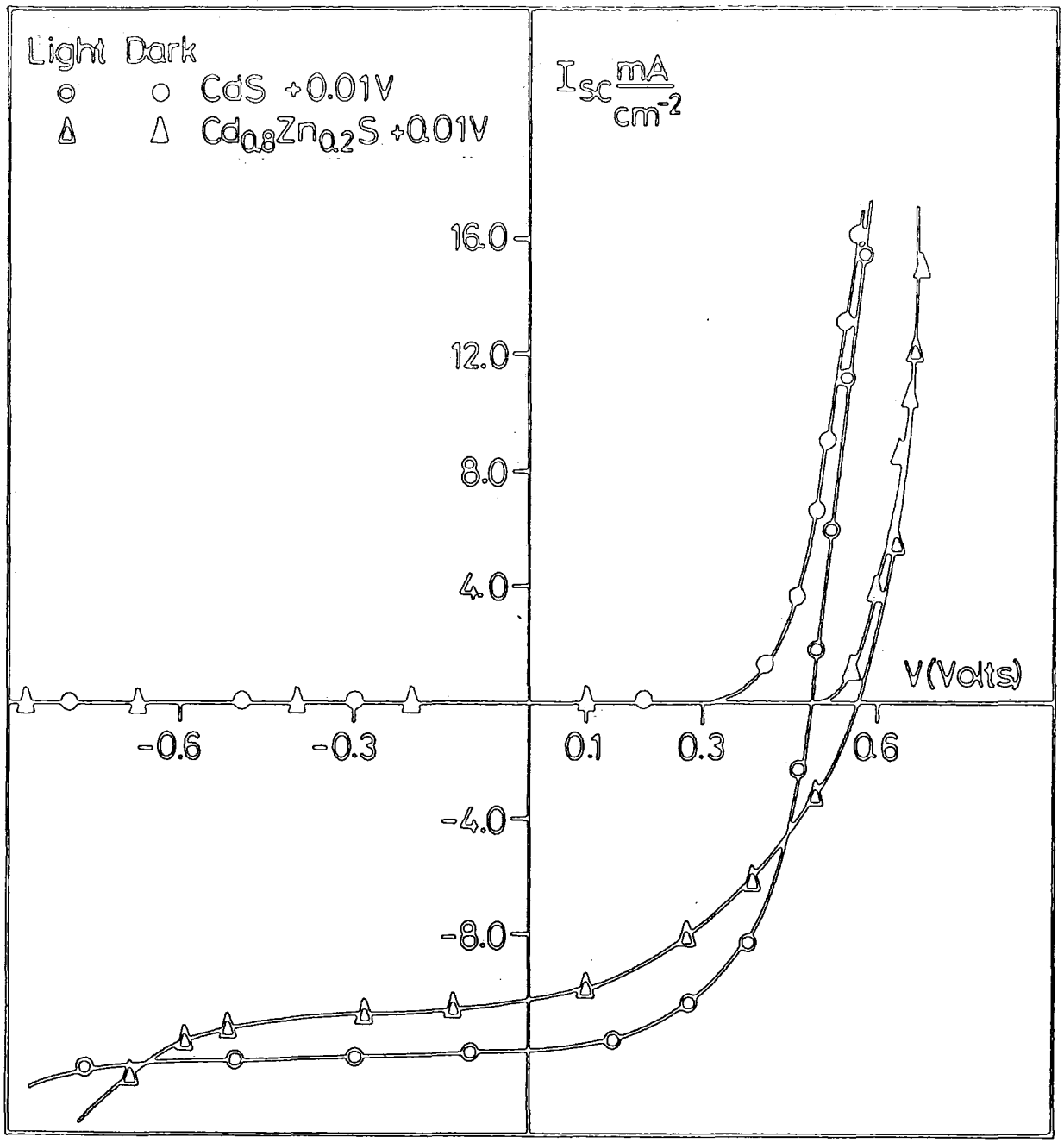

FIGURE 8.8 : Current-Voltage characteristics for two heterojunction prepared on CdS and $Cd_{0.8}Zn_{0.2}S$ single crystal with optimum electroplating bias measured in the dark and under illumination.

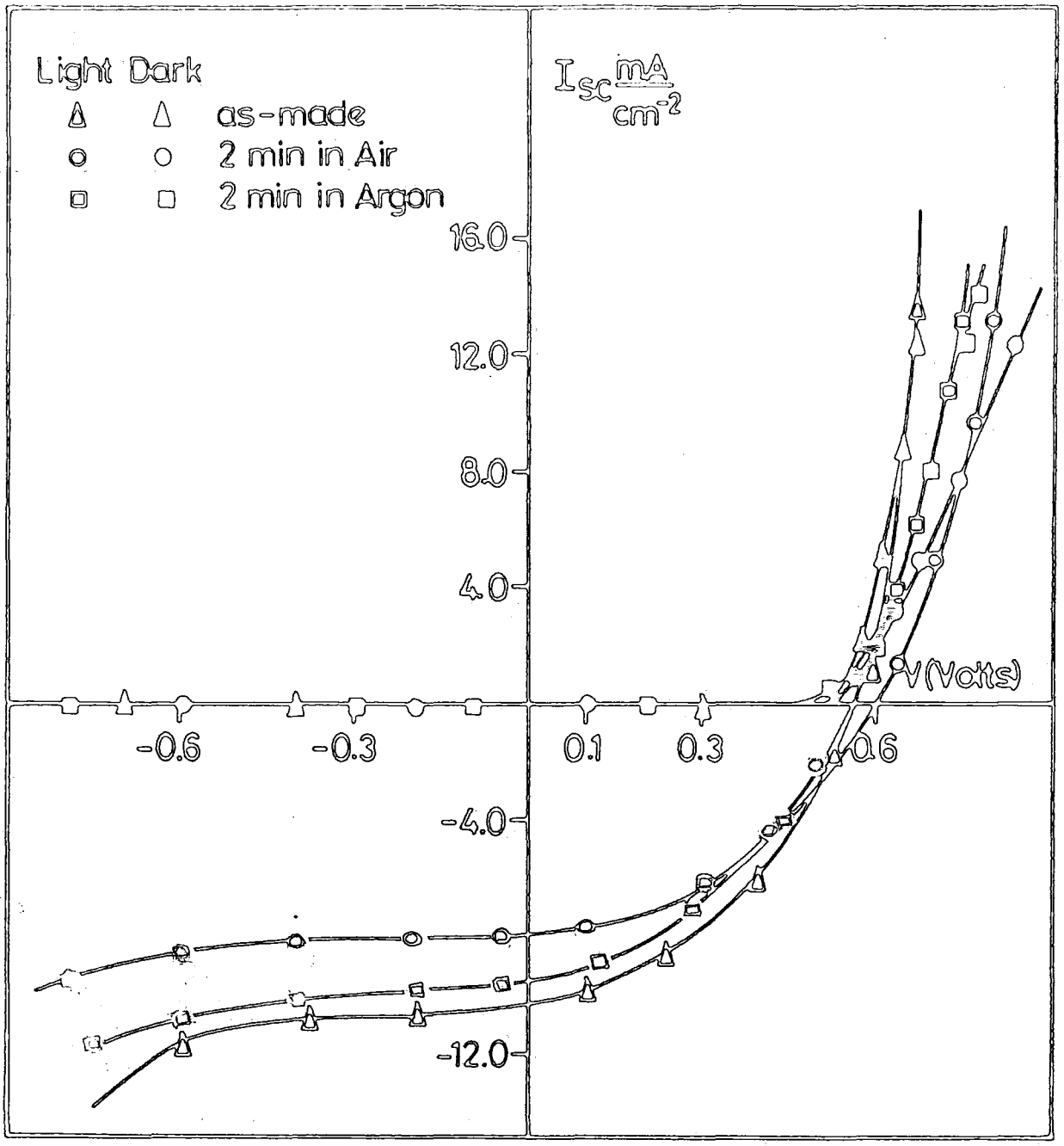

FIGURE 8.9 : Current-Voltage characteristics measured in the dark and under AM1 illumination for $Cd_{0.8}Zn_{0.2}S$-Cu_2S as a function of Air and Argon heat treatment at 200°C.

a recombination centre with a level 1.35eV above the valence band. To account for this centre, it is thought that a layer of zinc accumulated at the interface during the heat treatment, and this led to cation vacancy complexes developing in the zinc rich region thereby forming a new recombination centre.

Pande et al [14] found this new level at 1.27eV and suggested that it was the major reason for the reduction of the current density in the devices formed on $Cd_yZn_{1-y}S$. In addition, a shallow donor level was detected at 0.11eV below the conduction band and this may be the corresponding anion defect in the zinc rich region.

The present work has also shown that the use of $Cd_{0.8}Zn_{0.2}S$ as a substrate for growth of Cu_xS layers leads to an increase in V_{oc} to 0.56V, compared with that of 0.48V for devices which were based on CdS. However, this increase was offset by an accompanying decrease in I_{sc} from 12.3 to 10.2mA.cm^{-2}. Many workers [1,2,9,15-20] have reported a similar increase in V_{oc} and they have attributed it to an increase in the barrier height. It has been found that the addition of zinc to the CdS reduces the difference in electron affinity and the lattice mismatch between CdS and Cu_2S [1,3,10,21,22]. The location of the conduction band edge can be controlled by varying the zinc content in the CdS. Burton [22] found that the height of the conduction band step decreases with a better match of electron affinities, and consequently the barrier height increases. Oktik et al [23] found that the increase in the value of V_{oc} with rising zinc content corresponded to the increase in the value of photothreshold in the spectral response. They further found that the electron affinity decreased as the zinc content increased. Hence, as a result, the difference in electron affinities of $Cd_yZn_{1-y}S$ and Cu_2S should be reduced. Because of the reduction in the lattice mismatch combined with the reduction

in the interface state density, the probability of tunnelling via these states is decreased.

The V_{oc} is controlled by interface states and can be expressed by

$$V_{oc} = \frac{kT}{q} \ln\left[\frac{J_L}{J_o} + 1\right]$$

where J_L is the current density and J_o is the reverse saturation current density and is given by

$$J_o = qN_c S_I \exp \frac{-\phi_B}{kT}$$

where N_c is the density of states in the conduction band, S_I is the interface recombination velocity, ϕ_B is the barrier height for interface state recombination, and the other terms have their usual meanings. According to the above equation, a lower value of J_o leads to an increase in V_{oc}. The interface recombination velocity is given by $S_I = \nu_{th}\delta_n N_I$, where ν_{th} is the electron thermal velocity, δ_n is the electron capture cross section and N_I is the density of interface states. The better lattice match associated with $Cd_yZn_{1-y}S$ should reduce N_I which in turn would lower J_o. By assuming N_I = zero [1] for the $Cd_yZn_{1-y}S$ heterojunction and using the above equation, V_{oc} assumes the value of 0.85V, which represents an upper theoretical maximum. The other factors which play an important role in the improvement of device parameters are the electron mobility (μ_e) and the electric field at the interface. The electron mobility has been found to decrease with increasing zinc content [24,25].

The interfacial collection factor is given by

$$\beta = \mu_e F \frac{1}{S_I + \mu_e F}$$

β is affected by the mobility and the electron field (F). Therefore increasing the density of the interface states by reducing S_I should also increase the interfacial collection factor, thereby leading to a larger photocurrent density. However, in practice, Figure 8.8 shows that the value of I_{sc} was lower in $Cd_yZn_{1-y}S$ devices. This reduction in I_{sc} might be attributed to the different ion-exchange kinetic energy involved in the growth of copper sulphide on $Cd_yZn_{1-y}S$ instead of CdS [23]. Burton [22] attributed this to the lower values of diffusivity and solubility of Zn^{++} relative to those of Cd^{++} in Cu_2S. Pande et al [26], Burton [22,27] and Hsu et al [28] suggested that a zinc rich layer is accumulated at the interface which results in formation of a potential spike in the energy band diagram. Burton [1] supposed accumulation to be the main reason for the decrease in the I_{sc} following the incorporation of Zn in the lattice. In addition, as a result of the high resistivity of $Cd_yZn_{1-y}S$ and the Zn accumulation layer at the interface, these devices have a high series resistance, which decreases the I_{sc} [9,29]. Boer [16] put forward another mechanism that involved a spike in the energy band diagram which was present at the junction and which was transparent to electrons flowing across it. As the Zn content increases, the height of this spike decreases, but its width increases. The increased width makes the electron tunnelling process more difficult so that the current collection is reduced.

Pande et al [14] detected the presence of a deep level defect and suggested that this could act as a recombination path for the photogenerated carriers, and consequently provide another mechanism which would lead to a reduction in the current collection efficiency of the heterojunction.

The improvement of V_{oc} in Figure 8.9 after air heat treatment, might be due to the absorption of oxygen at the interface, which causes

an increase in the barrier height. During heat treatment the Cu diffuses from the Cu_xS into the $Cd_yZn_{1-y}S$ to establish an i-layer [30,31] and Zn and Cd also diffuse into the Cu_xS layer [1,32], leading to compensation of the p-conductivity and thus to a widening of the space charge region and band bending on the Cu_2S side of the junction [33]. The diffusion of zinc was mainly found to have increased after heat treatment [32]. However, the decrease in I_{sc} after heat treatment might be due to the diffusion of Zn from the $Cd_yZn_{1-y}S$ into the Cu_xS layer resulting in its accumulation at the interface, and the zinc concentration at the Cu_2S surface and near the Cu_2S-$Cd_yZn_{1-y}S$ interface increasing more than that of Cd after heat treatment [1,27,32]. In contrast, annealing in argon produced no change so that the barrier height probably remained unchanged.

The spectral response measurements demonstrated that, as with the CdS-Cu_xS heterojunction, the application of different biases to the $Cd_yZn_{1-y}S$ substrate during the growth of Cu_xS led to the formation of devices with different spectral sensitivities. The influence of the electroplating bias on spectral response was found to be the same as it was for CdS substrates, with the chalcocite phase of Cu_xS again being produced preferentially with a bias of +0.01V (Fig 8.5). This can be explained in the same way as was done for CdS devices in Chapter Five. Similarly the effects of heat treatment on the spectral responses shown in Figure 8.6 may be explained as was done for CdS cells (see Chapter Five). When the measurements were carried out at liquid nitrogen temperature (Fig 8.7), the air annealing showed an envelope shape which was not observed for CdS based cells. This could be attributed to the zinc diffusion into Cu_2S layer and accumulation at the interface.

8.5 Conclusion

This work has shown that an increase in the open circuit voltage

can be achieved when $Cd_{0.8}Zn_{0.2}S$ is used as a base for solar cells instead of CdS. This increase is accompanied by a decrease in the I_{sc}. The operational parameters were affected differently by heat treatment in different ambients. This is due to the diffusion of Zn from $Cd_yZn_{1-y}S$ into the Cu_2S and Cu from the Cu_2S into the $Cd_yZn_{1-y}S$ leading to a Zn compensated layer on the Cu_2S side and a Cu compensated layer in the $Cd_yZn_{1-y}S$ side of the junction.

A number of traps were identified through photocapacitance studies. A trap was found at 0.70eV which corresponded to an internal transition between the hole ground and excited states of copper. Another level was found with an activation energy of 1.0eV which is associated with the direct ionization of holes from the ground states of copper impurities introduced by diffusion of copper into $Cd_yZn_{1-y}S$. An important trap was found at 0.78eV below the conduction band. It has been demonstrated that the concentration of the traps decreased much more slowly when the heat treatment was carried out in argon rather than in air. This level may play an important role in controlling the properties of $Cd_{0.8}Zn_{0.2}S$-Cu_2S solar cells.

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CHAPTER NINE

Summary and Conclusions

The work described in this thesis has mainly been concerned with the optical, structural and electrical properties of three types of devices, namely:

i) CdS-Cu_xS single crystal

ii) CdS-Cu_xS thin film, and

iii) $Cd_yZn_{1-y}S$-Cu_xS single crystal photovoltaic cells.

An electroplating method has been used to control the phase of copper sulphide by applying different potentials to the CdS to control the chemical displacement reaction in the plating bath. Different phases have been produced by using a wide range of electroplating biases. RHEED investigations and spectral response measurements showed that the chalcocite peak was most dominant in CdS single crystal cells fabricated using a bias voltage of +0.01V. This optimum bias produced devices with the best values of V_{oc}, I_{sc}, FF and Υ. Chalcocite with a small proportion of djurleite, a mixture of chalcocite and djurleite, pure djurleite and covellite were obtained by applying electroplating voltages of 0.0, +0.1, +1.0, and 3.0V respectively.

This work has demonstrated that the change from the djurleite to the chalcocite phase can be achieved by using an argon heat treatment for 7 minutes at 200°C. This effect was found to be reversible in that layers of chalcocite were converted to djurleite when air was used. A dramatic change from covellite (CuS) to a copper rich phase (Cu_2S) results from the use of argon in heat treatments for 15 minutes at 200°C.

The soft I-V characteristics were improved by annealing in either air or argon. All the operational parameters improved with annealing.

On the other hand, the effect of heating devices which had good photovoltaic properties in the as-made condition, was not beneficial either for argon or air ambients and gave rise to a significant reduction in I_{sc}.

C-V measurements have demonstrated that the donor concentration decreased at first with increasing electroplating bias and then became constant. This led to the effect of decreasing the junction capacitance by changing the width of the depletion region.

The results of an investigation of the electroplating of thin film CdS with Cu_2S are also reported. Again the phase of copper sulphide which is produced during topotaxial growth has been shown to depend on the value of the plating bias, and furthermore these values differ from those required to achieve the same result using single crystal CdS. Bias potential of +0.1 and - 1V were found to be the most suitable for the consistent production of the chalcocite and djurleite phases of Cu_2S respectively on thin film CdS. This was confirmed by both RHEED and spectral response measurements.

The other aspect of this study concerns the stability of the devices. The effect on device characteristics of the use of argon or air as an annealing ambient, and the relative merits of tin oxide or Ag/Cr substrates are reported. These results showed that devices prepared on Ag/Cr substrates were more stable following annealing in air than in argon, while the converse was true for cells fabricated on SnO_x substrates. After annealing in air the dark forward bias characteristics indicated that the device had become very resistive. This was attributed to the formation of an i-layer at the heterojunction interface as a result of the diffusion of copper from the Cu_2S to the CdS. In addition, annealing in air caused reverse bias break down to occur at much lower voltages. In contrast there was less copper

diffusion after annealing in argon, with a correspondingly smaller increase in the device resistance. Annealing the devices prepared on Ag/Cr substrates demonstrated that there was very little copper diffusion following air annealing. This is in direct contrast to the effects achieved by an air anneal of a device on SnO_x. Further, annealing in this ambient showed the improved stability of the operational parameters relative to annealing in argon.

An investigation has been made of the ageing of CdS-Cu_2S single crystal cells separately as a function of illumination, temperature and storage ambient. The devices stored in the dark showed little or no degradation, whereas those maintained under illumination exhibited a significant deterioration in all operational parameters over a four week period. Spectral response measurements confirmed that for storage in the light, the changes could be attributed to the formation of djurleite from the chalcocite in the as-made device. ESCA investigations also showed that the amount of oxygen absorbed by the Cu_xS was considerably greater for devices kept under illumination than for those kept in the dark. As far as the combined effects of temperature and ambient on the stability of cells are concerned, it was found that the ageing of devices in argon at room temperature was negligible. The fill factor was observed to improve marginally. When the devices were stored in the same ambient at 50°C they showed a significant improvement in the fill factor, but simultaneously exhibited a considerable reduction in the short circuit current. These results were consistent with the spectral response measurements, which showed that the response of devices was unchanged after ageing at room temperature in argon for 40 days, whereas that of those kept in argon at 50°C exhibited a large increase in the response due to djurleite. Interestingly, this process was reversible, since the sensitivity of degraded devices could be

restored by annealing in a hydrogen/nitrogen mixture. By combining ESCA studies with measurements of solar cell devices this work has shown that the formation of copper oxide on Cu_xS surfaces plays a significant role in the degradation of CdS-Cu_2S devices.

The extent of the cross-over between the dark and light I-V characteristics is a function of the period of etching prior to the topotaxial growth of Cu_2S. The disappearance of this cross-over has been attributed to the removal of the damaged layer on the CdS surface. The operational parameters and the phase of Cu_xS were found to be dependent on the topotaxial growth period. The effect of electroplating bias on the dark I-V characteristics has been studied. The variation of current and diode factor has been established as a function of the bias value. The dependence of the forward current with temperature at fixed forward voltage, for devices which were fabricated with different electroplating biases has also been investigated.

In junctions formed on $Cd_yZn_{1-y}S$ single crystals, the increase in V_{oc} is accompanined by a decrease in I_{sc}. Also the cell operational parameters were influenced differently by annealing in different ambients. Different traps were identified through photocapacitance investigation. The acceptor level which can be associated with copper impurity was found to be located at $\sim$ 1.0eV above the valence band. Another important trap was found at 0.78eV below the conduction band. It has been demonstrated that this level was found to be diminished much more slowly when annealing was carried out in argon rather than air. This level may play an important role in the $Cd_{0.8}Zn_{0.2}S$-Cu_2S solar cell properties.