Screen printed layers of cds for solar cells

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SCREEN PRINTED LAYERS OF CdS
FOR
SOLAR CELLS

BY

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Dedicated to my Late Father, May Allah forgive him.

> And Say : "Work : Soon will God observe your work, And His Apostle, and the Believers : Soon will ye be brought back To the Knower of what is Hidden and what is Open: Then will He show you The truth of all That ye did."
>
> (Qura'n, s. ix, Tauba : 105)

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ABSTRACT

It is generally accepted nowadays that a significant cost reduction in terrestrial solar cell application could be brought about by investigating alternative fabrication techniques for solar cells. It is believed that screen printing (or the so called thick film technique) is one such technique which promises a potentially low cost method for fabricating flexible, large area solar energy conversion cells.

The active research on this technique started in 1976 in Japan. However, it was not until 1983, that wide interest developed when the Matsushita group in Japan reported an efficiency of 12.8% for their entirely screen printed CdS/CdTe solar cells. This was the highest reported efficiency for any thin film solar cell.

However, the details of the fabrication processes of these cells were not reported and several scientific groups in the world started to explore this technique. The first published report was in 1985. In the last few years these groups have reported results on various aspects of this technique. Nevertheless there are still major parameters to be investigated.

This thesis represents a concise reference for the application of the screen printing technique to solar cells. In the course of this study many new investigations have been made which supplement the previous work by other groups. Starting with a pure CdS powder with suitable grain size and distribution is a prerequisite for achieving the best morphological and electrical behaviour of screen printed layers of CdS.Careful paste mixing is of uppermost importance which can override any other parameters involved in the fabrication processes. It

is essential to impose restricted sintering conditions for adequate utilization of the doping and fluxing function of the $CdCl_2$ material.

Standardization of the printing, preparation and sintering conditions involved in the fabrication processes were necessary to ensure reproducible CdS layers.

Good quality screen printed layers were fabricated on soda lime substrates. The significance of other substrate materials for CdS preparation was also investigated and optimum substrate choice is suggested.

The properties of the CdS screen printed layers were investigated by forming simple Schottky devices and more complicated heterojunction solar cells. Good rectification behaviour of the Schottky diodes was achieved. The CdS/CdTe solar cells revealed a wide spectral response. However, the photovoltaic behaviour was relatively poor largely due to the high resistivity of the CdTe part of the cell structure.

CHAPTER ONE

GENERAL BACKGROUND

1.1 Introduction

The utilization of solar energy is one of the most convenient and reliable methods which could provide substantial energy for the whole world's needs.

One approach to utilization of solar energy is the use of the semiconductor device, namely a solar cell, which allows the direct conversion of light to electricity. Of particular interest in this study is a II-IV Compound Semiconductor application to solar cells.

This chapter will give an overview which includes solar energy, photovoltaic conversion by solar cells, semiconductors and II-IV compounds.

1.2 Solar Energy

The sun is a gigantic thermonuclear spherical reactor of intensely hot gaseous matter with a diameter of 1.39×10^6 km, and is on average, 1.5×10^8 km from the earth (1). The energy emitted from the sun is mainly in the form of electromagnetic radiation ranging from about 30 m short radio waves to 10^{-10} m X-rays.

As the solar photons pass through the earth's atmosphere, the spectrum changes by selective absorption of certain wave lengths by the atmospheric gases (2). The x-rays and other very short wave radiation are absorbed high in the ionsphere by nitrogen, oxygen and other components of the atmosphere. Most of the ultra violet radiation is absorbed by ozone. At wave lengths longer than 2.5 μm, a combination of low extra-terrestrial radiation and strong absorption by CO_2 and H_2O means that very little energy reaches the ground. Thus, from the

viewpoint of the terrestrial application of solar energy, only radiation with wave lengths between .29 and 2.5 μm need be considered.

The effect of the atmospheric attenuation on solar irradiance is described by the term air mass number. Conventionally, solar cell performance is measured in terms of certain standard conditions of illumination, in particular AM0, AM1 and AM2. AM0 (air mass zero) corresponds to the solar irradiance at the top of the earth's atmosphere. AM1 is the irradiance at sea level under a standard atmosphere when the sun is at zenith, and AM2, which is a typical average irradiance at the earth's surface, corresponds to the condition where the angle between the sun and the zenith is 60°. Fig. 1.1 shows the spectral distribution of solar radiation under the various conditions.

1.3 Solar cells and 'Photovoltaic Conversion'

Solar cells were developed during the 1950's, primarily at the Bell Telephone and RCA Laboratories (U.S.A.) (3-5). These cells proved to be the best power sources for extraterrestrial emission, and almost all satellites use solar cells. In the mid-1970's, efforts were initiated to make solar cells for terrestrial applications, and since that time, most of the solar cell market has been for use on earth, although space applications remain buoyant.

Continued efforts during the last two decades to fabricate high efficiency solar cells have succeeded in producing single crystal Si and GaAs solar cells with efficiencies in excess of 20% and 25% respectively. However, the cost of these cells made them too expensive for wide scale terrestrial application and many new techniques have emerged to reduce the cost, such as thin film, thick film and amorphous solar cells.

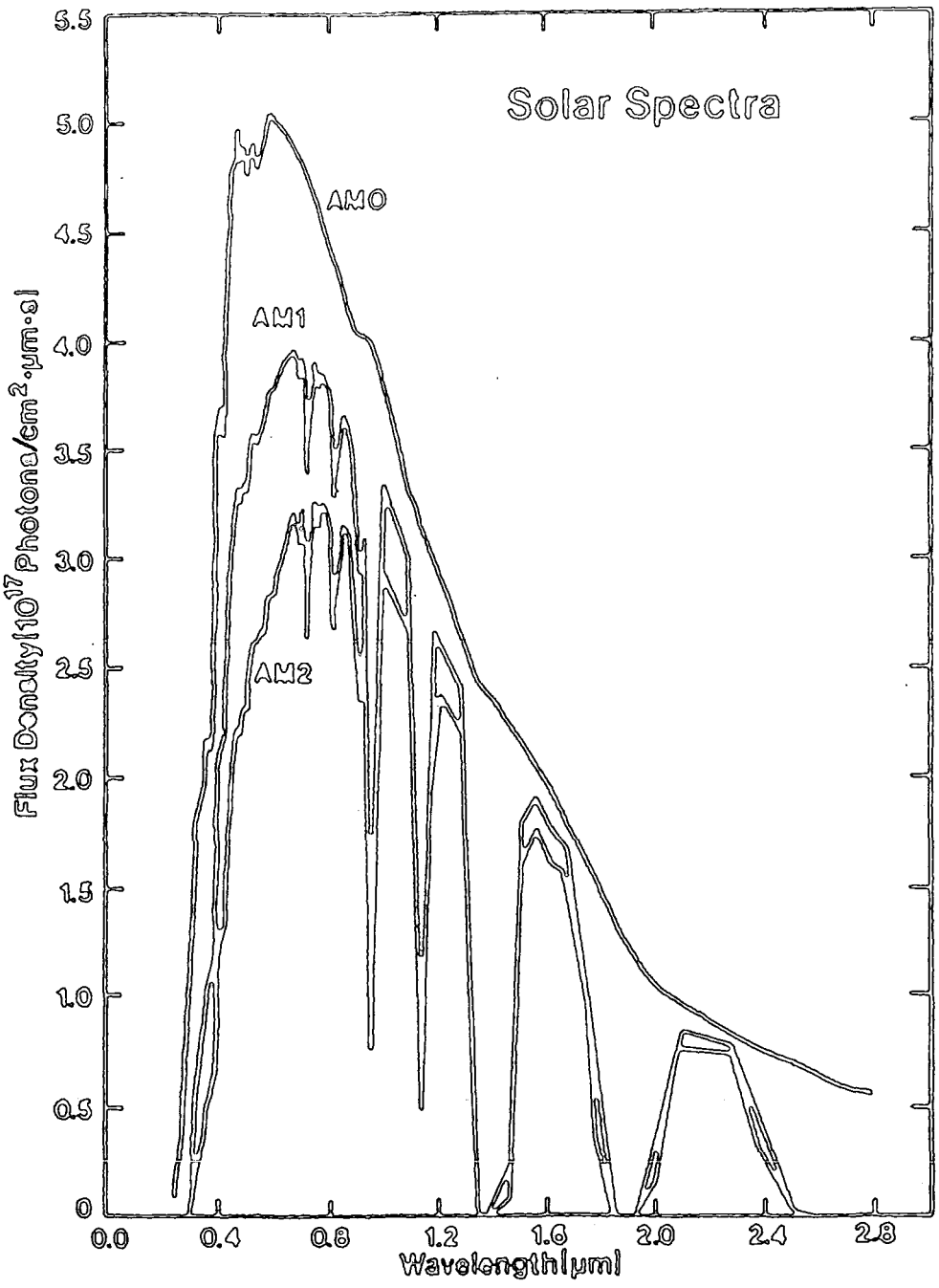


Figure 1.1 : Spectral distribution of solar radiation under dfferent conditions.

The direct conversion of solar energy by solar cells is based upon the photovoltaic effect, which is defined as the generation of an electromotive force as a result of the absorption of solar radiation in an inhomogeneous sytem.

The essential features of a solar cell are, an absorber generator material, in which mobile carriers are created by the absorbed solar energy, and a built-in potential barrier which allows the generated carriers to be collected from the region in which they are produced and converted to majority carriers.

There are four methods of creating such a barrier. One involves adding small amounts of impurities or 'dopants' to pure material to produce a homojunction cell or a PN junction (e.g. silicon solar cell). Another method involves two different semiconductor materials such as Cadmium Sulfide (CdS) and Cadmium Telluride (CdTe) creating a heterojunction cell. A third method involves a junction between the Semiconductor material and a metal, creating a 'Schottky' barrier. The last method is where a very thin layer of some material is sandwiched between the metal and the semiconductor. This creates a metal-insulator- semiconductor or MIS junction.

1.4 Semiconductors

The primary materials used for photovoltaic conversion in solar cells are semiconductors.

Semiconductors are a class of materials with electrical conductivity somewhere between metals and insulators. Their resistivity is usually in the range of 0.001 to 100 ohm cm.

Many of the electronic properties of semiconductors depend on the presence of impurities, known as dopants, which may act as sources of free carriers. Concentrations of the order of parts per million or

less, can change a semiconductor from a poor conductor to a good conductor of electric current.

Semiconducting elements are found in column IV of the periodic table, and semiconducting compounds in combination from neighbouring columns of the periodic table. Table 1.1 demonstrates that there are numerous semiconducting materials. This wide range offers a considerable variety of properties.

1.5 II-VI Compounds

II-VI compounds are these formed between elements from group II and group VI of the periodic table (table 1.1B). They crystallise in two main modifications, namely the cubic zince blende (sphalerite), and the hexagonal wurtzite structures (fig. 1.2).

The II-VI compounds were the first semiconducting materials to be used on a large scale as phosphors, and even today their production volume is comparable with that of silicon (6). One of the most important properties of these compounds is that they have wide and direct band gaps so that they are most useful for optoelectronic devices in the visible and near infrared regions (7). Fahrenbruch (8) has reviewed the uses of II-VI compounds in solar energy conversion and has indicated that the principal advantages of these materials are their low cost and the ease of deposition of good quality films by a variety of methods.

Typical deposition techniques are screen printing, evaporation, electrophoresis and spray pyrolysis. Conversion efficiencies higher than 10% have been achieved in thin film cells (9) and 15% in single crystals have been known and are being actively investigated (10).

However, most of the applications of II-VI semiconductors have not reached their full potential due, in the main, to the difficulty of controlling defects in the materials. Such defects can behave, for

II	III	IV	V	VI
	B	C		
	Al	Si	P	S
Zn	Ga	Ge	As	Se
Cd	In	Sn	Sb	Te

A

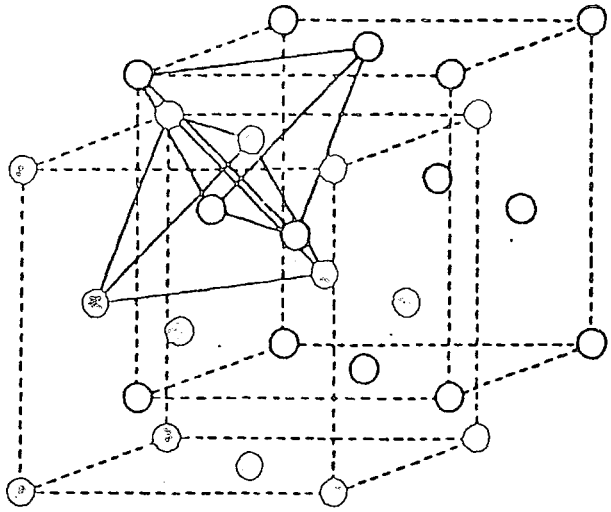
Elemental	IV Compound	III-V Compound	II-VI Compound
Si	SiC	AlP	ZnS
Ge		AlAs	ZnSe
		AlSb	ZnTe
		GaP	CdS
		GaAs	CdSe
		GaSb	CdTe
		InP	
		InAs	
		InSb	

B

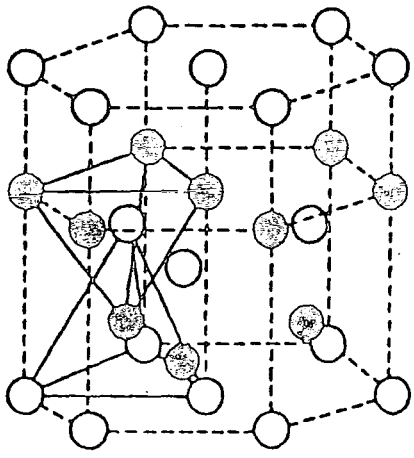
TABLE 1.1 Common Semiconductor Materials

A : Portion of the periodic table where semiconductors occur

B : Elemental and compound semiconductors



A



B

Figure 1.2 : A) The zincblend structure
B) The Wurzite structure

example, as recombination centres and thereby reduce the carrier life time (11) and with it the device efficiency.

1.6 Scope of the Present Study

The problem addressed in this thesis was the preparation of good screen printed CdS layers for use in the fabrication of solar cells. To achieve this a comprehensive study was made of various printing, preparation and sintering conditions involved in the fabrication of such layers. Following the brief general background presented in this chapter, a theoretical background is given in Chapter 2. This includes material characterization and a review of relevant theories. The details of experimental equipments and techniques employed and device preparation are outlined in Chapter 3. Chapter 4 is devoted to various aspects concerning the use of the screen printing technique for solar cell fabrication. Preliminary studies related to the starting CdS powder and the behaviour of the $CdCl_2$ material in the screen printing process are described in Chapter 5. The characterizations of the screen printed layers using Hall Effect and Schottky measurements is discussed in Chapter 6. In Chapter 7 the significance of the substrate is described. In Chapter 8 trials to fabricate a solar cell by evaporation CdTe layers on to the resultant screen printed layers are reported. Finally, a summary of the main objectives achieved are outlined in Chapter 9.

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CHAPTER TWO

THEORETICAL BACKGROUND

2.1 Introduction

In the first part of this Chapter, various aspects related to cadmium sulfide and cadmium telluride will be discussed. In the second part, the relevant theories used in the present work will be reviewed.

2.2 Material Aspects

2.2.1 Cadmium Sulfide (CdS)

i) Properties of CdS

Cadmium Sulfide is a II-VI compound which crystallises in two forms with the zinc blende and wurtzite structures (fig. 1.2). It has a direct band gap of about 2.4 eV giving it a transparent yellow colour.

Although cadmium melts at 320°C and sulphure at 119°C the minimum temperature at which cadmium sulfide melts is about 1475°C, and then only under an equilibrium vapor pressure of ~ 4 atmosphere (1).

There are a number of criteria which suit CdS for use as thin film solar cells reviewed by T. Coutts (2) as follows,

i) Wide band gap : the value of the band gap of CdS is 2.4 eV corresponding to a wave length of 0.5 μm. This means that the bulk of the solar spectrum is transmitted quite freely, thus making CdS suitable as a 'window layer' above the absorber in which photogeneration of excess minority carriers takes place.

ii) Resistivity: in its bulk form CdS has a very high resistivity, but it can easily be doped n-type to have a resistivity of an appropriate value for solar cell applications (10 - 100Ωcm).

iii) Electrical Contacts: it is a straight-forward matter to make ohmic contact to CdS layers.

In general, in the past, CdS has been coupled with P-type Cu_2S (3). However, in recent years CdS has been used in conjunction with InP (4), $CuInSe_2$ (5) and CdTe (6) to produce heterojunctions with very promising efficiencies.

Of particular interest in this thesis is the CdS/CdTe device. In this structure CdS is a good choice as a window material since the electron affinities of both CdS and CdTe are approximately 4.5 eV (7), and therefore the conduction bands of the two materials join smoothly at the interface (8).

ii) Impurity doping

CdS is not amphoteric, and can only be made n-type. Any attempt to diffuse in acceptor impurities results in self compensation by vacancies to maintain charge neutrality. The high resistivity of the bulk CdS can be reduced in several ways. For example, sulphur vacancies introduced by the presence of excess cadmium (Cd) during film fabrication act as donors, and reduce the resistivity (9). Extrinsic impurity dopants such as the halogens (Cl, Br, I) and group III elements (Al, In, Ga) can be introduced substitutionally into CdS to reduce the resistivity (10).

In this work, chlorine was used as the main dopant to reduce the resistivity of the fabricated CdS layer. The recognition of chlorine as a donor in CdS has been reported by many workers (11-13). $CdCl_2$ was used in the present work as the donor source. A simplified picture of the doping procedure is that the divalent sulphur ion is replaced by the monovalent chlorine ion, and an extra electron is present for conduction with a very small activation energy of about .03 eV (11).

iii) Ohmic Contacts

Good ohmic contact can be made between a metal and the n-type CdS if the work function, ϕ , of the metal is less than that of the CdS.

The most commonly used contact to CdS is indium (14) but other metals of suitable work function such as gallium (14), silver/zinc, aluminium and chromium have also been reported (15).

Indium was used to provide the ohmic contact to CdS in this work. There are several methods of achieving this, such as vacuum evaporation (14), alloying (16), electrolytic deposition (17), and more recently screen printing (18).

2.2.2 Cadmium Telluride (CdTe)

i) Properties of CdTe

CdTe is also a member of the II-VI group of compounds, and has very advantageous properties as an absorber material for solar cells, because of its direct band gap of 1.5 eV (19), which is optimum for photovoltaic conversion of solar energy (20), with a high optical absorption coefficient of $>10^4$ cm^{-1} (21).

The high absorption coefficient implies that photons with energies above 1.5 eV will be absorbed within a few micro meters of the CdTe surface, and in principle therefore, less material will be required for device fabrication, with a potential saving in cost.

Polycrystalline CdTe has been the most commonly used heterojunction partner for n- CdS material either in its single crystalline or polycrystalline form (19). Polycrystalline thin films of CdTe have been deposited by a variety of techniques including vacuum evaporation (22) (23), close space sublimation (CSS) (24), electroplating (25) and screen printing (26).

ii) Impurity doping

The as-deposited CdTe layers had a high resistivity and were

slightly p- type, leading to a high series resistance of the devices produced here (see later). Therefore further doping treatment had to be considered.

It is generally accepted that p-type conductivity in CdTe may be obtained by doping from groups I and V of the periodic table. Success has been reported with Cu, Ag, Au and P (27).

P-type doping with copper (Cu), which belongs to group I, has been demonstrated by many workers (28) (23), and was chosen in the present work to reduce the resistivity of the deposited CdTe layers.

Copper, Cu^{+}, presumably substitutes for cadmium and behaves as an acceptor. De Nobel (29) investigated the electrical properties of CdTe doped with Cu and reported a p-type conduction with activation energies in the range of 0.35 ± .05 eV. The ionic radius of Cu+ (0.96 A) is close to that of Cd^{2+} (0.95A) (30) which makes the substituion for Cd easy.

The major problem associated with copper as well as with other dopants, when introduced into polycrystalline CdTe, is segregation at the grain boundaries which lowers the shunt resistance of the device.

iii) Ohmic contacts

It is difficult to make a low resistance ohmic contact to p- type CdTe (30) (31). This is because a true ohmic contact to p- type CdTe, requires a metal with a work function larger than the work function of p- CdTe (of the order of 5.7 eV), which is not available. To overcome this problem it is necessary to produce a heavily doped region in the CdTe adjacent to the contact metal, to the point where easy tunneling is possible (32).

The work functions of Cu, Au, Ag, Zn, In and Pb on p- type CdTe have been determined, and gold (Au) has been found to be the most favourable contact material (33). Since the pioneer work of De Nobel (29), gold has mainly been used to make ohmic contact to P- CdTe.

Recently, the use of a carbon contact to P- CdTe has been suggested by Nakayama et.al. (34) for applications with their screen printed solar cells. They found that carbon contacts led to efficient devices with improved stability.

2.3 Relevant Theories

2.3.1 Hall effect

The Hall effect has been used for many years as an aid in the understanding of semiconductors (35). In this work Hall effect measurements were made on screen printed CdS layers using the Van der Pauw technique to determine the resistivity, carrier concentration and mobility of the layers.

i) Classical Hall theory

When a semiconductor is placed in a magnetic field perpendicular to the direction of current flow, a field E_y is developed across the specimen in the direction perpendicular to both the current and the magnetic field B_z. This field, called the 'Hall Field', is given by

$$E_y = \frac{J_x B_z}{nq} \qquad 2.1$$

where J_x is the current density, n is the number of carriers per unit volume and q is the carrier charge. The ratio

$$R_H = \frac{E_y}{J_x B_z} = \frac{1}{nq} \qquad 2.2$$

is called the 'Hall Coefficient'. A measurement of R_H thus determines

n, and since

$$\rho = \frac{1}{nq\mu} \qquad 2.3$$

where μ is the carrier mobility, then

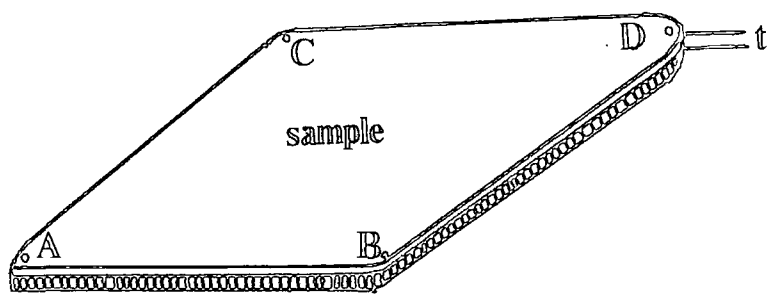
$$\mu = \frac{R_H}{\rho} \qquad 2.4$$

From equations 2.2 and 2.4 the carrier concentration and mobility can be determined.

ii) The Van der Pauw technique

The Van der Pauw method (36) is the most reliable and widely used method of determining the resistivity and Hall Coefficient of semiconducting specimens. It enables measurements to be made on samples with arbitary shapes without the classical bar-or-bridge shaped conventional geometry (37).

In essence this method consists of applying four ohmic contacts A, B, C and D at the periphery of an arbitary shaped sample of thickness t, as shown below.



When a current I_{AB} is allowed to flow across the contacts A and B, a potential drop V_{CD} is produced between the contacts C and D. The ratio of V_{CD} to I_{AB} is defined as the resistance $R_{AB,CD}$. Similarly $R_{BC,DA}$ is determined by establishing a current I_{BC} across the contacts B and C, and measuring the potentila drop V_{DA} between the contacts D and A. The expression for the resistivity P is then given by

$$\rho = \frac{\pi t}{\ell n 2} \left(\frac{R_{AB,CD} + R_{BC,DA}}{2} \right) f(R_{AB,CD}, R_{BC,DA}) \qquad 2.5$$

where $f\ (R_{AB,CD},\ R_{BC,DA})$ is a function which satisfies the relation

$$\left| \frac{R_{AB,CD} - R_{BC,DA}}{R_{AB,CD} + R_{BC,DA}} \right| = \frac{f}{\ell n 2} \text{ arc cosh } \left\{ \frac{1}{2} \exp\left(\frac{\ell n 2}{f} \right) \right\} \qquad 2.6$$

The function f is described graphically by Van der Pauw (36).

2.3.2 Schottky barriers

Because of their simple structure and relative ease of fabrication, Schottky diodes were used in the present study as a means of characterizing the fabricated layers. The following description of the Schottky devices, and their electrical behaviour will be useful in the analysis of the experimental results in Chapter 6.

i) Metal Semiconductor Contacts

Consider a metal and an n-type semiconductor that are electrically neutral and separated from each other; the semiconductor work function ϕ_s is less than that of the metal ϕ_m. If the metal and the semiconductor are brought into contact electrons flow from the semiconductor into the metal. This results in the Fermi level in the semiconductor being lowered by an amount equal to the difference between the two work functions to bring the Fermi levels into coincidence. The negative charge on the metal resides on the surface and an equal and opposite charge is built up in the semiconductor provided by the loss of electrons. This leaves uncompensated positive donor ions in the region depleted of electrons. Since the donor concentration is many orders of magnitude less than the electron concentration in the metal, this depleted zone of uncompensated donors occupies a region of appreciable width extending into the semiconductor. This is known as the space charge or depletion region. The density of free carriers is assumed to fall abruptly from a value equal to the density in the semiconductor bulk to a value at the interface which is negligible compared with the donor concentration; this is known as the depletion approximation. Outside the depletion region the semiconductor is neutral, but within this region there is a charge density of qN_d. The variation of the charge density with distance x from the metal is shown in fig. 2.1a. The electric field, E, is related to the charge density by Gauss's theorem and is such that it increases linearly as the metal is approached reaching a value of qN_dW/ϵ_s at the interface (fig. 2.1b) where W is the width of the space charge region and ϵ_s is the dielectric constant of the semiconductor. The electrostatic potential ($\psi(x)$) is given by

$$\psi(x) = \int_{x}^{w} E dx \qquad 2.7$$

which reduces to the quadratic

$$\psi(x) = -\frac{qN_d}{2\varepsilon_s} (w - x)^2 \qquad 2.8$$

The variation of $\psi(x)$ with x is shown in fig. 2.1 C. For the metal-semiconductor contact, the subsequent parabolic band bending is shown in fig. 2.2 This is known as a Schottky barrier.

The height of the potential barrier on the semiconductor side is

$$V_d = \phi_m - \phi_s \qquad 2.9$$

V_d is the diffusion potential measured from the interior of the semiconductor with respect to the metal surface. The height of the barrier on the metal side is given by

$$\phi_{bn} = (\phi_m - \phi_s) + (\phi_s - \chi_s) = \phi_m - \chi_s \qquad 2.10$$

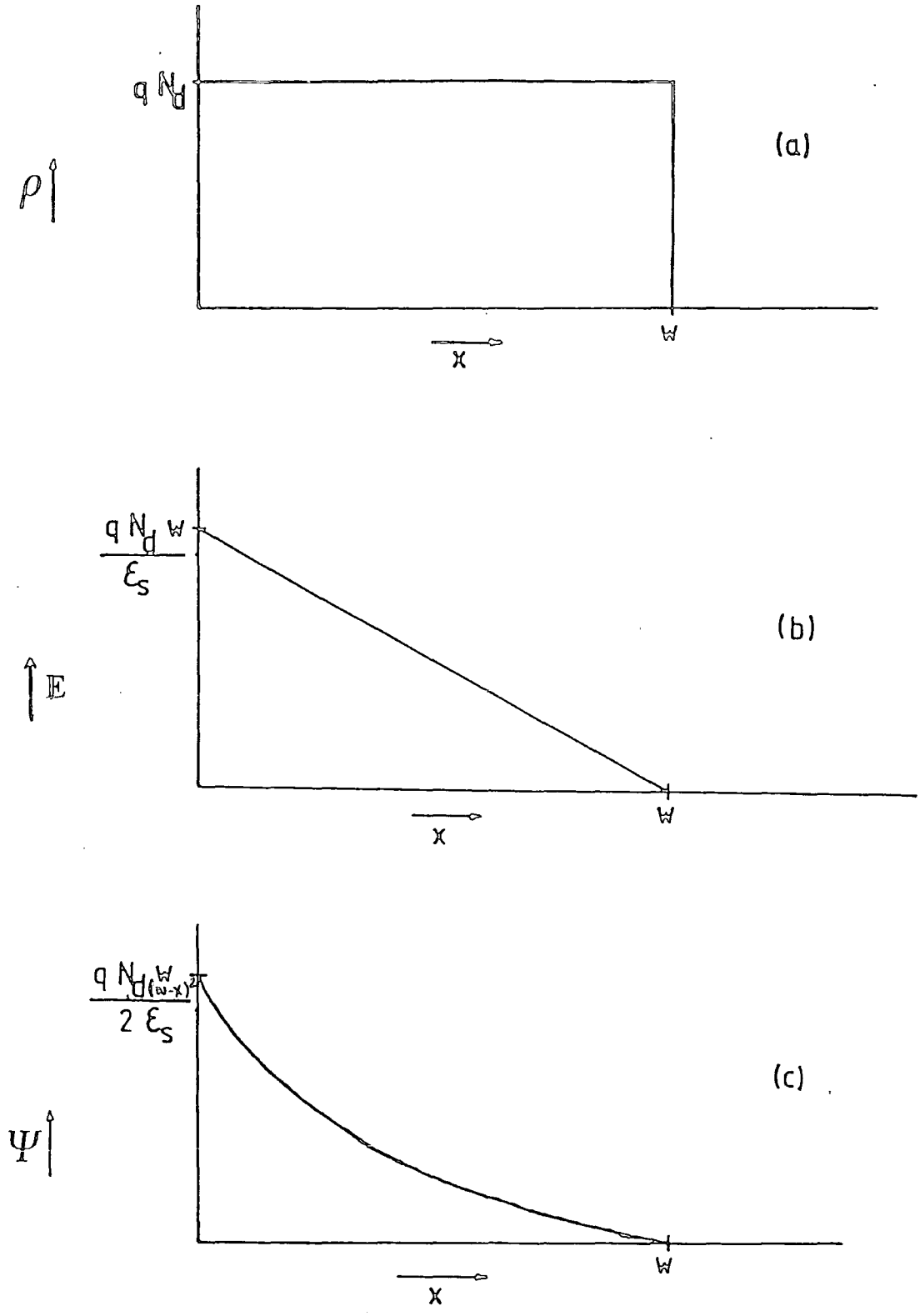


Fig. 2.1 : Variation of (a) charge density (b) electric field strength and (c) electrostatic potential with distance according to the depletion approximation.

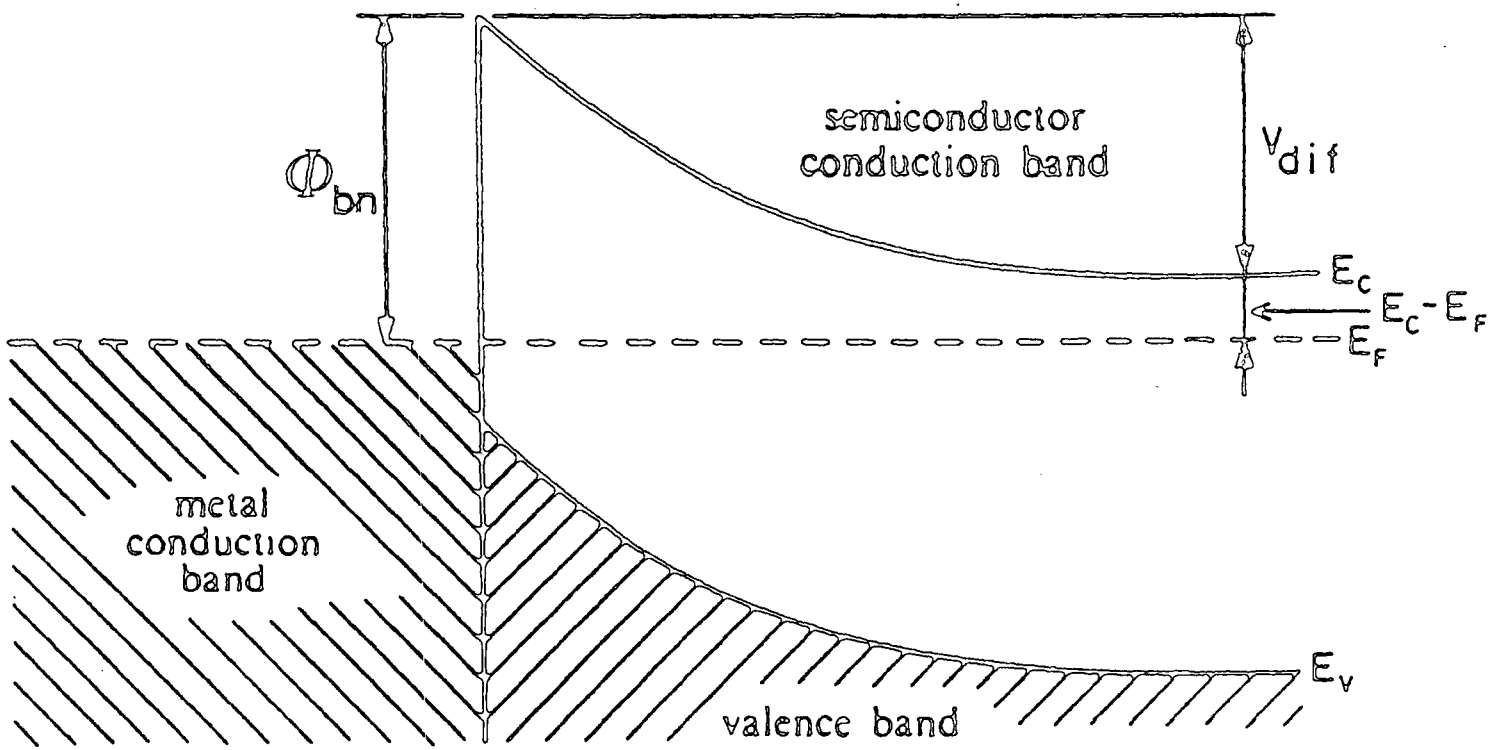


Fig. 2.2 : Energy band diagram of an ideal metal n-type semiconductor contact (Schottky barrier).

In most devices the ideal Schottky barrier shown in fig. 2.2 is never achieved, because there is a thin insulating layer on the surface of the semiconductor, which is generally developed during the fabrication processes prior to the formation of the metal contact. This usually leaves a thin, interfacial layer. The barrier presented by such a layer may be sufficently narrow to allow electron tunnelling. The band diagram of this structure is shown in fig. 2.3.

ii) Current transport

When a metal n-type semiconductor contact is biased in the forward direction (i.e. the metal electrode is positive) there are four ways (38) in which the charge can be transported across the barriers, these are:

a) Thermionic emission of electrons over the top of the barrier

b) Quantum mechanical tunneling through the barrier

c) Recombination in the depletion region

d) Minority carrier injection

These processes are shown in fig. 2.4. In most devices the major contribution to the current transport is provided by the first process. The processes (b), (c) and (d) usually arise from non-ideal behaviour.

For the thermionic process, electrons must be transported first through the depletion region of the semiconductor. This occurs by the normal processes of diffusion and drift which take place in this region. Schottky and Spenke (39) proposed that the current flow is limited by diffusion processes, whereas Bethe (40) proposed that thermionic emission was the limiting mechanism. Both these ideas were later combined in a joint thermionic emission-diffusion theory by Crowell and Sze (41).

If the width of the space-charge region is less than the diffusion length of the electrons, according to the thermionic emission theory,

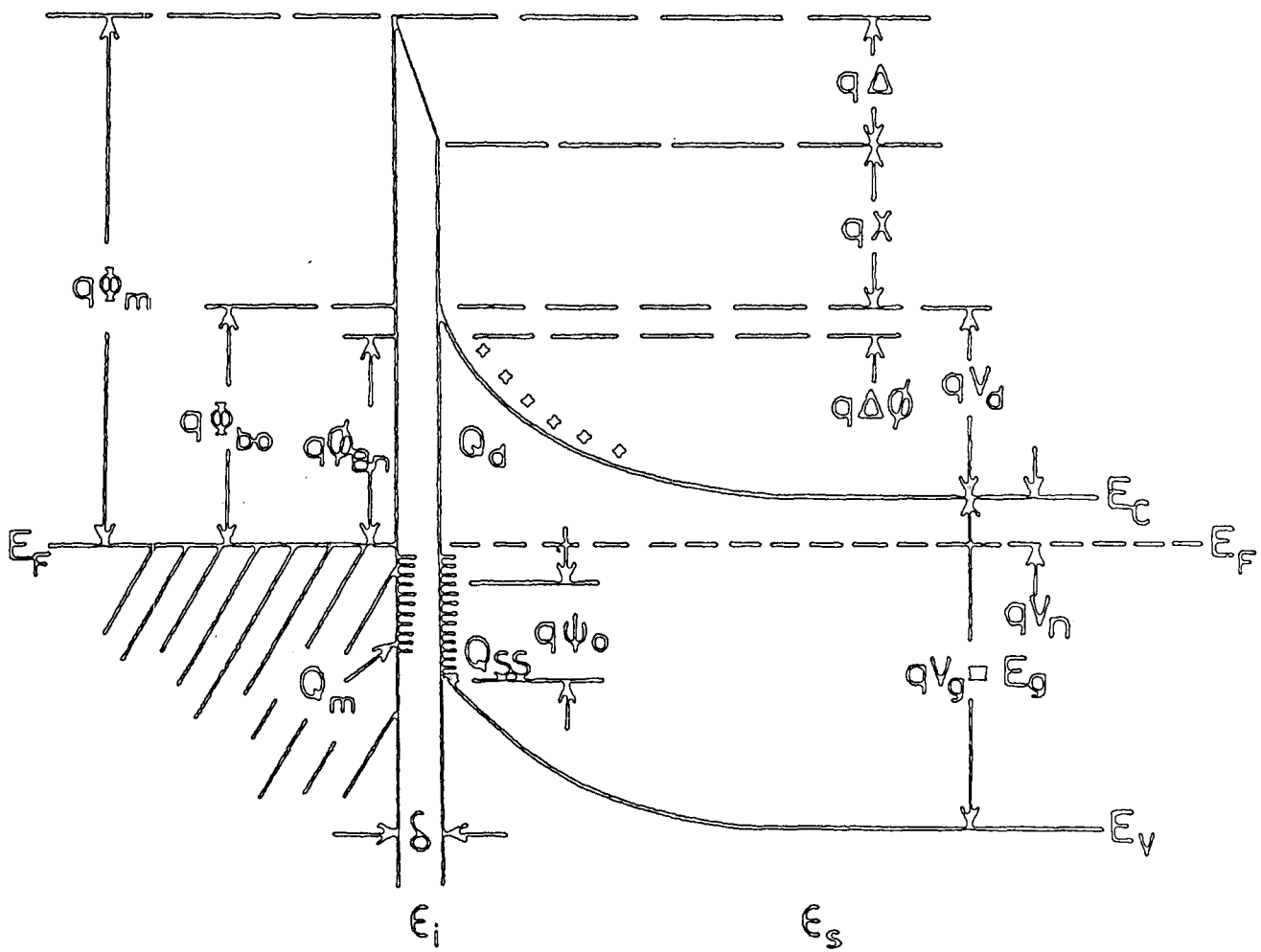


Fig. 2.3 : Detailed energy band diagram of a metal n-type semiconductor contact with a thin interfacial layer

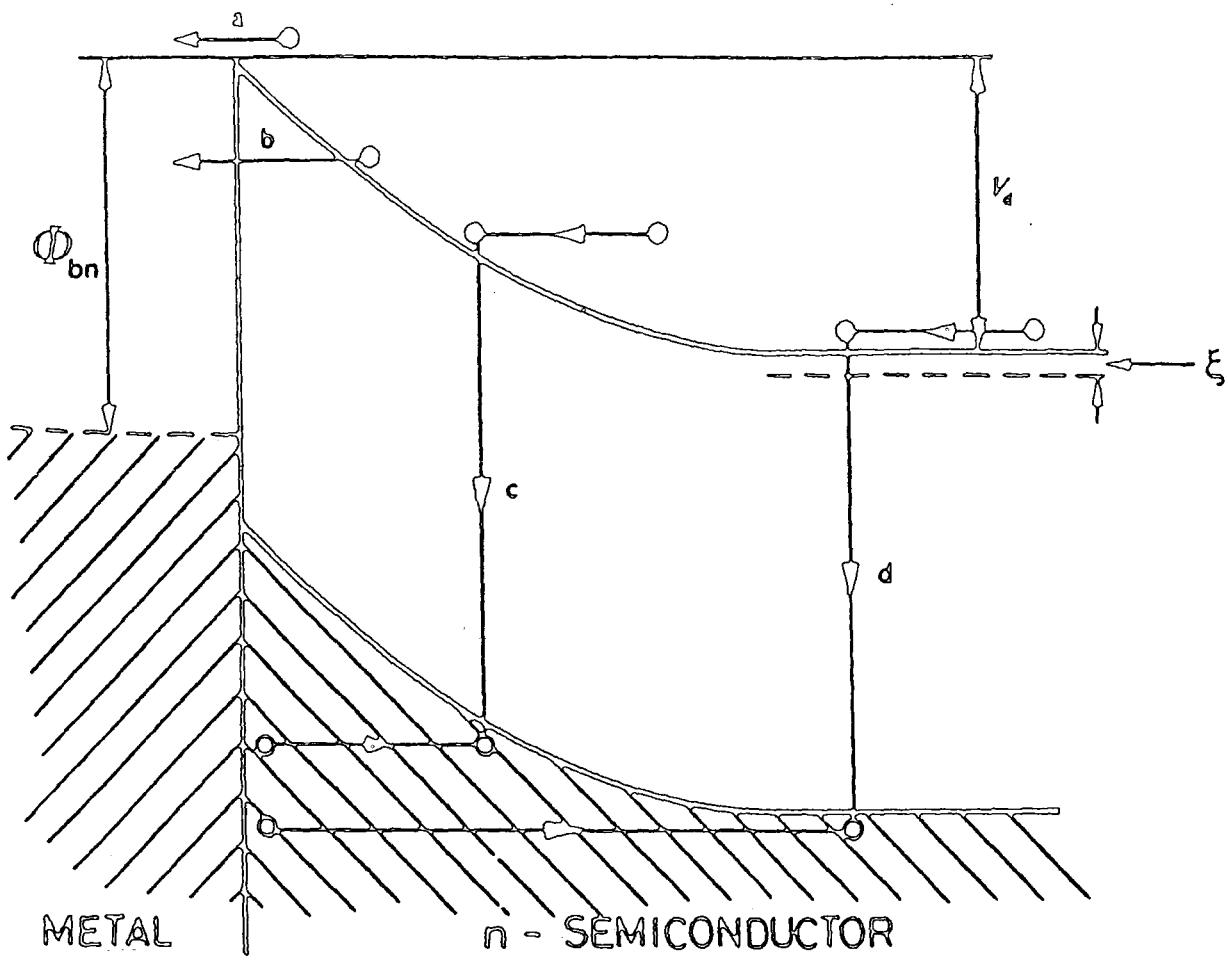


Fig. 2.4 : Current transport mechanisms in a forward-biased Schottky barrier

the forward biased current density can be expressed by : (42)

$$J_F = J_S \left[\exp (qV/KT) - 1 \right] \qquad 2.11$$

conversely if the space-charge region is greater than the diffusion length, the forward current is limited by the diffusion mechanism, and the current-voltage relationship becomes (42)

$$J_F = q\, N_c \mu_e E_{max} \exp\left(\frac{-q\phi_{bn}}{KT}\right) \left[\exp(qV/KT) - 1\right] \qquad 2.12$$

where E_{max} is the maximum electric field at the junction, μ_e is the electron mobility and N_c is the effective density of states in the conduction band.

For the general case in which the space charge region is comparable in thickness to the diffusion length, both mechanisms apply, and the current-voltage relationship becomes (41)

$$J_F = qN_cV_r \left(1 + \frac{V_r}{V_d}\right)^{-1} \exp(-q\phi_{bn}/KT) \left[\exp(qV/KT) - 1\right] \qquad 2.13$$

where V_r is an effective recombination velocity at the potential energy maximums, and V_d is an effective diffusion velocity for the transport of electrons from the edge of the depletion region to the potential energy maximum. If $V_d \ll V_r$ the pre-exponential term in equation 2.13 reduces to qN_cV_r and the diffusion theory applies. If $V_d \gg V_r$ the thermionic emission process is dominant.

However, in practice Schottky barriers deviate from the ideal behaviour, and the experimental forward current-voltage relation is usually expressed as : (43)

$$J_F = J_s \exp (qv/AkT) \qquad 2.14$$

for bias voltages $V \gtrsim 3\ kT/q$. The parameter A is known as the ideality or quality factor and is normally greater than unity as a result of non ideal interface conditions. A detailed discussion of non-ideal diode mechanisms such as recombination and tunneling has been given by Rhoderick (38).

iii) The Capacitance of a Schottky barrier

The capacitance of a diode is determined by the distribution of the charge density ρ in the space charge region of the function. With a Schottky barrier device, and assuming that the charge density ρ in the depletion region is given by $\rho = qN_d$ ($N_d = N_D - N_A$ = donor density) for $x < w$ and $\rho = o$ for $x > w$, where w is the depletion width, integration of Poisson's equation yields (44)

$$V(x) = \frac{qN_d}{\varepsilon_o\varepsilon_s} (wx - \tfrac{1}{2}x^2) - \phi \qquad 2.15$$

The electric field then becomes

$$| E(x) | = \frac{qN_d}{\varepsilon_o \varepsilon_s} (w-x) \qquad 2.16$$

and the depletion width is

$$W = \frac{2\varepsilon_o \varepsilon_s}{qN_D} \left[(V_d + V - \frac{KT}{q}) \right]^{\frac{1}{2}} \qquad 2.17$$

where ε_s is the relative permittivity of the semiconductor and V_d is the diffusion potential at zero bias. KT/q is a contribution from the Kinetic energy of the mobile charge carrier. The space charge Q_{sc} per unit area and capacitance, c, per unit area are given by

$$Q_{sc} = qN_d w = \left[2q \varepsilon_o \varepsilon_s N_d (V_d + V - \frac{KT}{q}) \right]^{\frac{1}{2}} \qquad 2.18$$

and

$$C = \frac{\partial Q_{sc}}{\partial V} = \left[\frac{q \varepsilon_o \varepsilon_s N_d}{2(V_d + V - KT/q)} \right]^{\frac{1}{2}} = \frac{\varepsilon_o \varepsilon_s}{w} \qquad 2.19$$

Thus the depletion layer capacitance is voltage dependent, and inversely proportional to N_d, i.e. it narrows as the density of

uncompensated donors increases. At higher temperature more donors are ionized and $N_d = N_D^+ - N_D^-$ is large, so that the depletion region is smaller. At lower temperature N_d decreases and w increases.

Equation 2.18 may be re-written as

$$\frac{1}{C^2} = \frac{2(V_d + V - \frac{KT}{q})}{q\varepsilon_o\varepsilon_s N_d} \qquad 2.20$$

or

$$N_d = \frac{2}{q\varepsilon_o\varepsilon_s} \quad \frac{dv}{d(C^{-2})} \qquad 2.21$$

Providing that N_d remains constant throughout the depletion region, a plot of $1/C^2$ vs V should produce a straight line, the voltage intercept of which gives the diffusion potential V_d, while the gradient yields the donor density N_d. If there are electron traps present in the depletion layer then some traps above the Fermi level will be emptied when reverse bias is applied. This would contribute an additional capacitance. With polycrystalline films, the intergranular barriers also provide depleted regions in the grains of the interface and may affect the capacitance measurement (45).

The carrier mobility in the sample can be calculated using the following equation

$$\mu = \left[N_d q \rho \right]^{-1} \qquad 2.22$$

where ρ is the resistivity of the sample.

2.3.3 Heterojunction theory

A heterojunction is a junction formed between two dissimilar semiconductors. If the two semiconductors have the same type of conductivity, the heterojunction is referred to as an isotype, otherwise it is referred to as an anisotype.

Heterojunctions have been extensively studied for applications such as light-emitting diodes, photo-detectors and solar cells. Heterojunctions have been reviewed by many authors (46) (47) (48).

The energy band models of semiconductor heterojunctions were first described by Anderson (49). When the effect of dipoles and interface states are negligible, the energy profile of the n-Cds/p-CdTe heterojunction at thermal equilibrium and zero bias is as shown in fig. 2.5 (a) and (b) before and after the formation of an abrupt junction (50). Both semiconductors are characterized by their electron affinities, band gaps and work functions. In the ideal situation, the barrier height is given by : (48) (50)

$$V_b = E_{gp} + \Delta E_c - E_c - \delta_n - \delta_p \qquad 2.23$$

where ΔE_c is the conduction band discontinuity at the hetero-interface, and δn and δp are the displacements of the Fermi level from the conduction band edge in the n(CdS) and p(CdTe) type materials, respectively. Egp is the band gap of the p-type material.

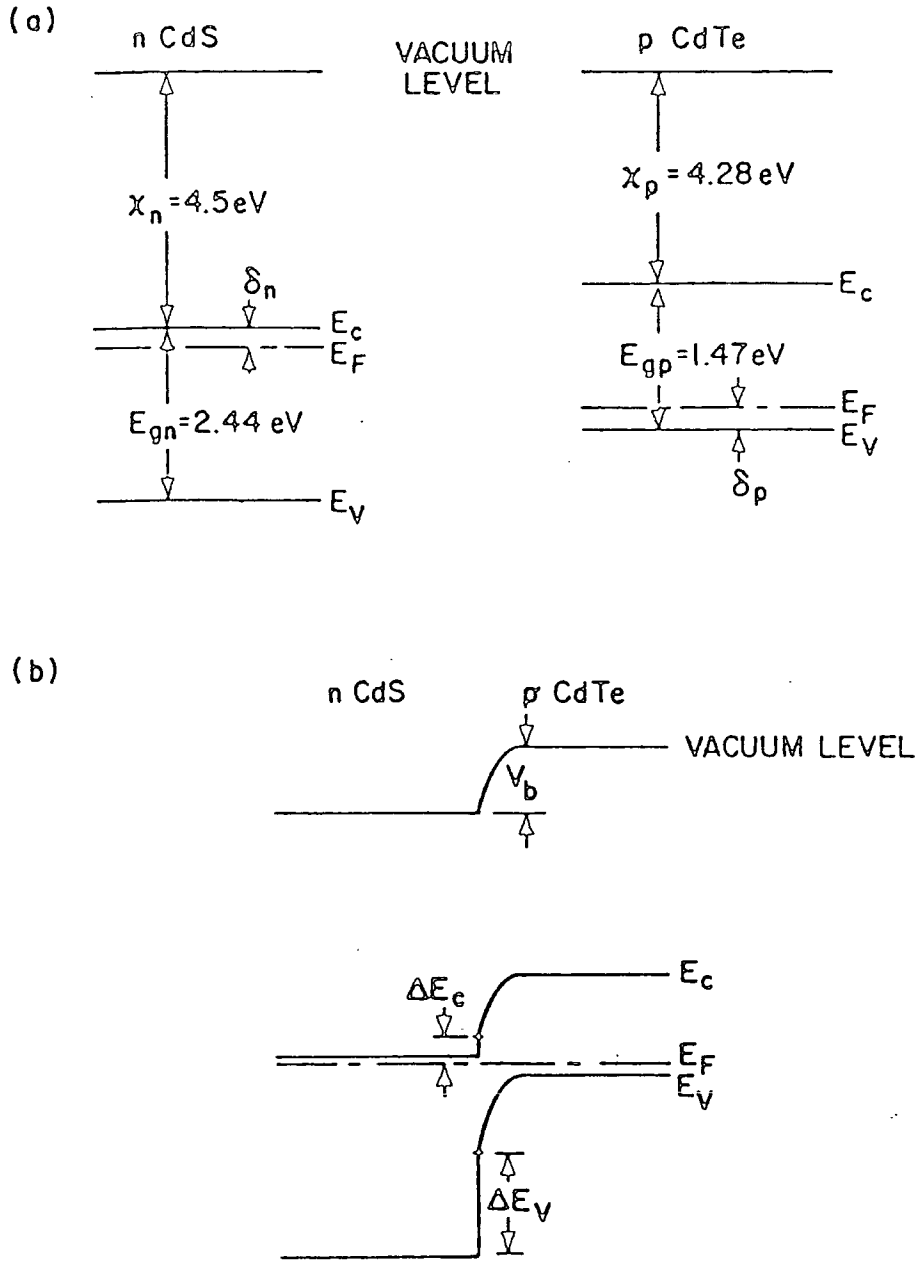


Fig. 2.5 : Equilibrium energy band diagram for the CdS/CdTe heterojunction (Ref. 49): (a) before; and (b) after the formation of an abrupt p-n junction.

The discontinuities are given by:

$$\Delta E_c = \chi_p - \chi_n \qquad 2.24$$

$$\Delta E_v = (E_{gn} - E_{gp}) - \Delta E_c \qquad 2.25$$

where Egn is the band gap of n-type material.

The current-voltage relationship takes the form : (47) (50)

$$J = J_{oo} \exp(-qV_{bp}/KT) \left[\exp(V_p/kT) - \exp(-qV_n/kT) \right] \qquad 2.26$$

where

$$Joo = XqD_nN_D/L_n$$

and

$$V_{bp} = K_pV_b \text{ where } K_p = (1 + N_A \epsilon_p/N_DE_n)^{-1}$$

$$V_p = K_pV$$

$$V_n = K_nV \text{ where } K_n = 1 - K_p$$

V_{bp} is the portion of the built-in voltage on the p-side of the junction; V_p and V_n are the portions of the applied voltage appearing on the p and n-sides of the junction; x is the transmission coefficient for electrons to pass the interface; D_n, L_n are the diffusion constant and diffusion length respectively for electrons in p-type semiconductors. The contribution to the current from the injection of holes into the wider band gap semiconductor is negligible because of the large energy barrier to hold injection arising from ΔE_v.

2.3.4 The Solar Cell

i) Equivalent Circuit

When light of sufficent energy ($h\nu > Eg$) falls on a solar cell, electron-hole pairs are generated. These carriers diffuse to the junction where they are separated to yield useful electrical energy. This can be modelled as a light independent current generator connected with a diode. This is illustrated in the equivalent circuit of fig. 2.6 which includes series and shunt resistance components.

The general expression for the total current through an illuminated solar cell is given by the following equation (51)

$$J - \frac{V - JR_s}{R_{sh}} = \sum_i J_{oi} \left[\exp\left\{ \frac{q}{A_i kT} (V - JR_s) \right\} - 1 \right] - J_L (V) \qquad 2.27$$

where J_L is the light generated current. Under illumination, the dark current voltage characteristics are translated by the amount of light generated current. The dark and light current-voltage characteristics for an ideal case are shown in fig. 2.7.

ii) Operational Parameters

The performance parameters of a solar cell are derived from the output characteristics. Usually four main parameters are used:

a) Short-Circuit Current (ISC) : This is the current that flows through the junction under illumination with zero applied bias. In ideal conditions (if the series and shunt resistance effects are negligible) it is equal to the light generated current I_L and is proportional to the incident number of photons with energy greater than or equal to the energy gap of the absorber.

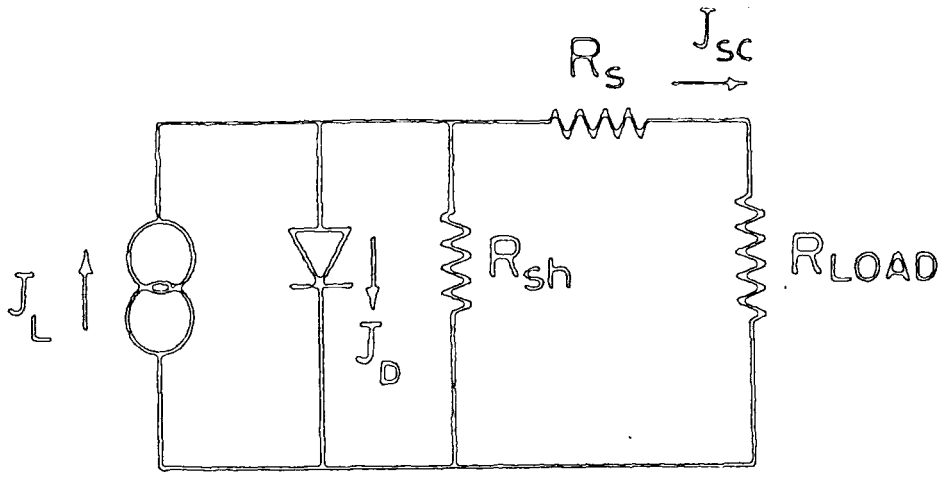


Fig. 2.6 : Equivalent circuit of a solar cell.

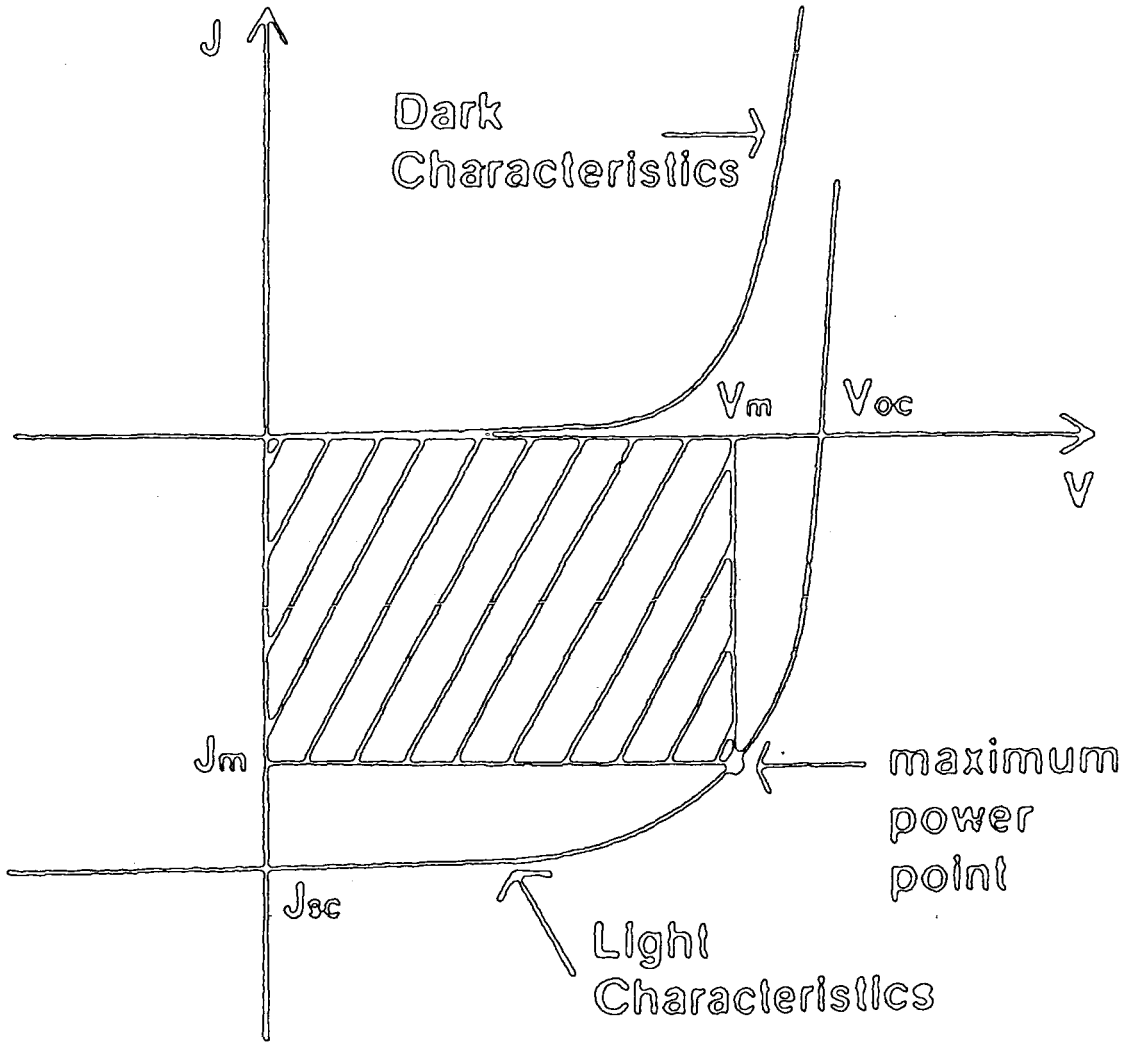


Fig. 2.7 : Typical dark and light J-V characteristics of an ideal solar cell

b) Open-Circuit Voltage (V_{OC}) : This is the voltage across the terminals of an illuminated solar cell at zero current flowing through the junction. It is given by (52)

$$V_{OC} = (1/A)\ [(I_{SC}/I_0) + 1] \qquad 2.28$$

where $A = q/nkT$ and I_0 is the reverse saturation current.

c) Fill Factor (FF) : This is defined as the ratio of the maximum electrical power output to the product of V_{OC} and I_{SC}. It describes the rectangularity or squareness of the photovoltaic output characteristics. The fill factor is mainly affected by the series resistance (R_s) and shunt resistance (R_{sh}). The effect of these parameters on the J-V characteristics is shown in fig. 2.8. It is obvious that as the series resistance increases and shunt resistance decreases, the fill factor deteriorates (53).

d) Efficiency (η) : This parameter describes the overall performance of a solar cell. The three parameters, I_{sc}, V_{oc} and FF, determine the efficiency of a cell, which can be expressed as (48):

$$\eta = \frac{I_{sc}\ V_{oc}\ F.F.}{P_{inc} \times \text{Area}} \qquad 2.29$$

where P_{inc} is the incident radiation power density, usually expressed in mW/cm^2.

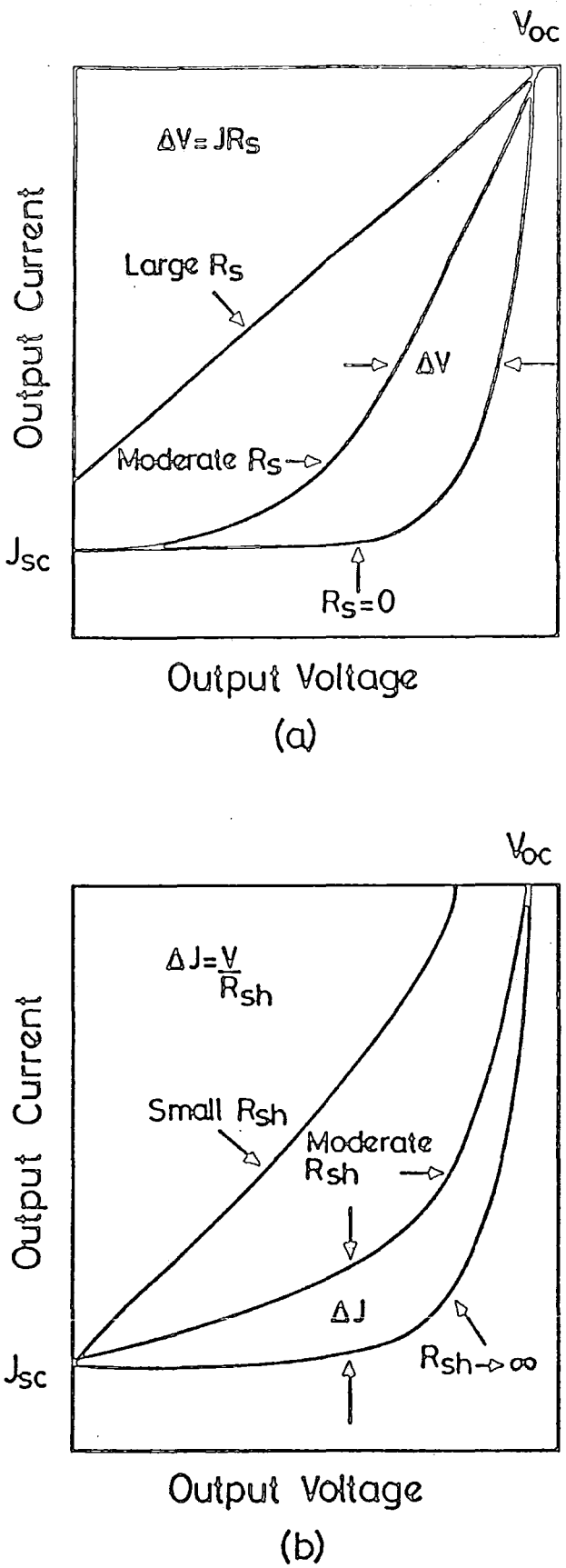


Fig. 2.8 : Effect of parasitic resistances on the output characteristics of cells (ref. 53)

a : Effect of series resistance, R_s

b : Effect of shunt resistance, R_{sh}

iii) Spectral Response

The photocurrent collected at each wavelength relative to the number of photons incident on the surface at that wavelength determines the spectral response of the device (48) (some times known as the quantum efficiency or collection efficiency at each wave length). Measurement of the spectral response can provide detailed information about the design parameters of any particular solar cell (53).

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CHAPTER THREE

EXPERIMENTAL TECHNIQUES AND DEVICES PREPARATION

3.1 Introduction

In this Chapter the most important experimental equipments and techniques used in the present work will be described. The electrical measurements will be presented in section 3.3, while in the final section the fabrication of Schottky diodes and CdS/CdTe heterojunction solar cells will be described.

3.2 Structural Analysis Techniques

3.2.1 Scanning Electron Microscopes (SEM)

A Cambridge Stereoscan S600 SEM was used in this work for morphological observations and thickness assessment of the screen printed CdS layers.

A schematic diagram of the SEM device is shown in fig. 3.1. The SEM may be operated in several modes by imaging various signals derived from the different interactions that occur between the incident electron beam and the specimen (1). These are shown in fig. 3.2. Only the secondary emission mode was used in this work.

i) Secondary emission mode

The basic principle of operation in this mode is that as the electron beam is scanned across the sample in a raster, the secondary electrons that are emitted from the specimen surface are collected by an Everhart-Thornley (ET) detector consisting of a scintillator and photo multiplier (PM). The output from the photomultiplier is taken through the PM tube amplifier and is fed into the input of the cathode ray tube (CRT) monitor which is scanned with the same raster generator as that used to scan the electron beam across the sample. In this way a micrograph of the secondary emitted electrons from the specimen surface is formed.

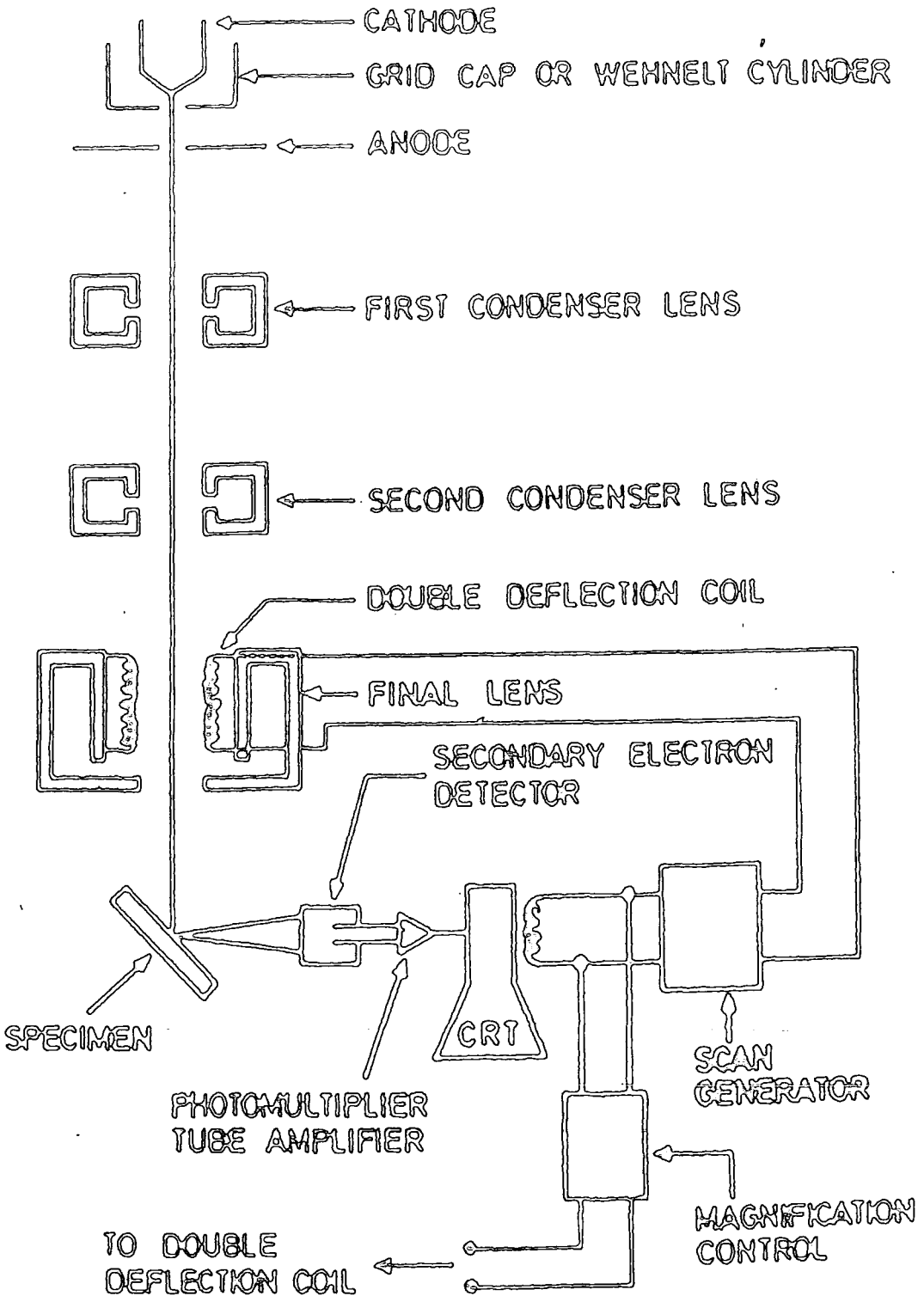

Figure 3.1 Schematic diagram of the SEM.

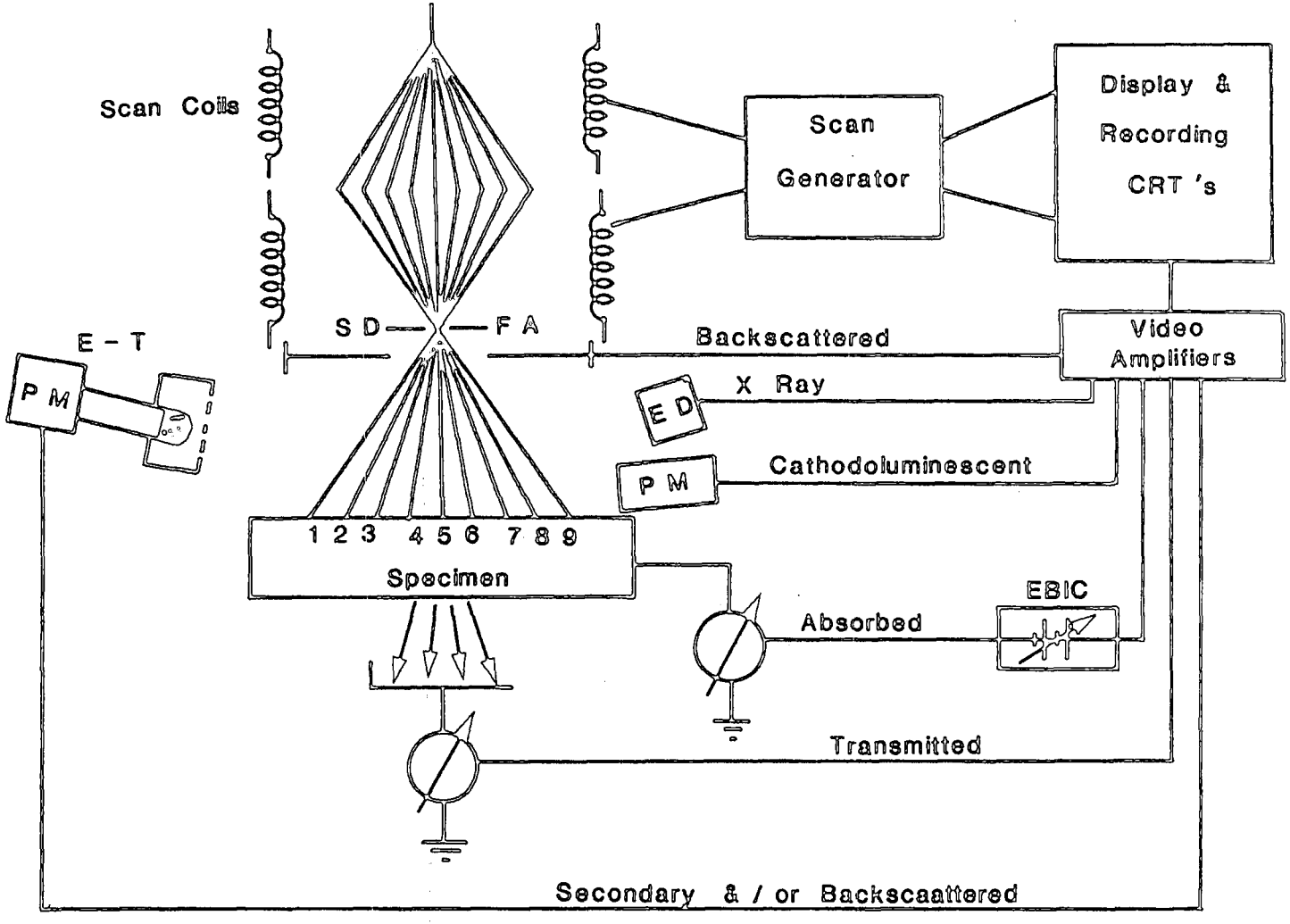

Figure 3.2 : Schematic diagram showing some of the various modes of operation of the SEM.

ii) Energy Dispersive Analysis by X-Rays (EDAX)

X-rays may be produced by the interaction of the electron beam with the specimen. These may be analysed for their energy in order to identify the elements from which they originated. Each element produces its own characteristic x-rays and the intensity of them can give an indication of the stoichiometry.

This technique was employed by using a Link System 860 series 2 Analyser. The block diagram of the system is illustrated in fig. 3.3

The x-rays emitted from the surface of the specimen pass through a thin beryllium window into a cooled, reverse-bias p-n Si (Li) detector (2). This leads to the ejection of a photo electron which gives up most of its energy to the formation of several electron-hole pairs. These are swept away by the applied bias to form a charge pulse which in turn is converted to a voltage pulse by a charge-sensitive preamplifier. The amplitude of this voltage pulse is proportional to the magnitude of the charge released by the photoelectron which in turn is proportional to the energy of the incident x-ray photon. Thus an energy spectrum of the incident x-rays can be built-up by sorting and summing the voltage pulses according to pulse-height in a multi-channel analyser (MCA).

The resulting spectrum is then (in the Link System) displayed on a cathode ray tube and may be "screen-dumped" to a matrix printer for permanent record. The contents of the MCA memory can be further processed, for example, for peak identification by comparison with the known position of characteristics x-ray lines.

3.2.2 Electron Spectroscopy for Chemical Analysis (ESCA)

The ESCA technique has been used in this study to investigate the presence of oxygen, as well as the ratio of the sulphur to oxygen on the surface of the sintered CdS layers.

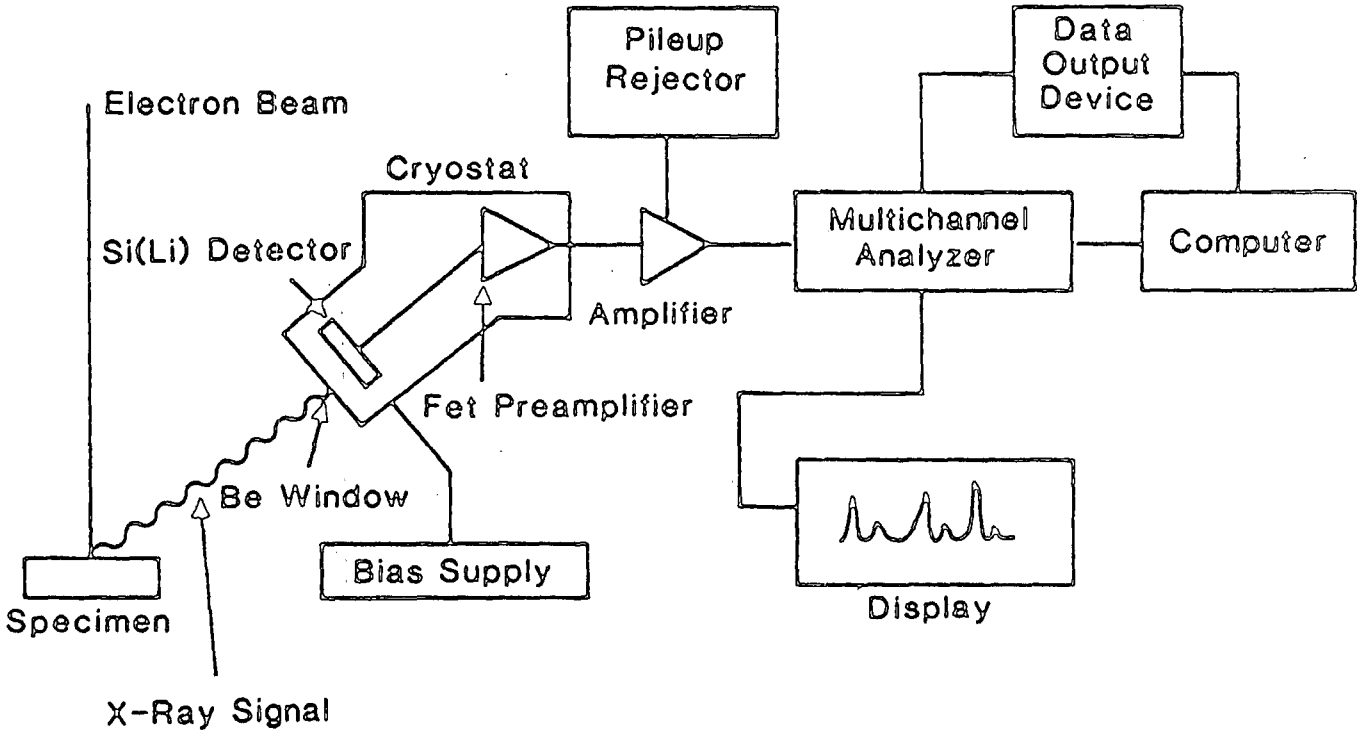

Figure 3.3 Energy dispersive X-ray analyser.

ESCA is a non destructive and powerful method for surface analysis which relies upon x-rays interacting with deep core electrons in an ultra high vacuum system (10^{-7} - 10^{-10} torr). Energetic photoelectrons are emitted and the material may be analysed by counting their number and measuring their velocity. The technique is limited to the characterization of the first few layers (usually to a depth of 20-40A°) of the sample surface.

3.2.3 X-Ray Diffraction (XRD)

The structure of the screen printed CdS layers after various sintering conditions were investigated in a Philips PW 1130 diffractometer using Cobalt K α radiation (λ = 1.7902A°) with a goniometer scanning rate of one degree per minute. The diffractometer was operated with target voltage and current of 40 KV and 20 mA.

The scan was made on samples with dimensions of 2.5 x 2.5 cm^2 and x-ray diffraction was recorded from 2θ = 28° to 2θ = 34°. The analysis of the films was carried out using the standard joint Committee for the powder diffraction standard (J.C.P.D.S.) index 1974 (3). The hexagonality value of the layers was calculated using the following equation (3.1)

$$H = \frac{15.9R - 8.1}{13.5R + 25.1} + \frac{33.2 - 2.5R}{32.5 + 71.2R} \qquad (4)$$

where R is the intensity ratio of the (101) to (002) reflections of the diffraction pattern.

3.2.4 X-Ray Fluorescence (XRF)

The quantity of chlorine remaining in the screen printed CdS layers after various treatments was determined in counts per second using a Philips PW 1400 x-ray spectrometer with a rhodium x-ray tube (3KW) which was operated at 80 KV and 35 mA with flow counter, using a PET analysis crystal.

3.2.5 Chemical Analysis by Atomic Absorption Spectroscopy (AAS)

The indirect method of AAS analysis was used to determine the chlorine content remaining in the sintered layers in atomic percent ratio using a Perkin Elmer 5000 Atomic Absorption Spectrometer.

3.3 Electrical Measurements

3.3.1 Hall Effect Measurements

Hall measurements were made to determine the carrier concentrations and mobilities of the screen printed CdS layer under various preparation and sintering conditions. The Van der Pauw technique was employed and this allowed both the resistivity and Hall coefficient to be measured.

a) Sample preparation

Square samples with dimensions of 1 x 1 cm^2 were used for all measurements. Contacts to the samples were made by pressing four small slices of 1.5 mm diameter indium wire on the periphery of the sample and then heating for 10 minutes in argon. The sample was then fixed with silicone grease to a glass microscope cover slip. Electrical contact to the sample was made with fine copper wires soldered to the cover slip with indium. The wires were connected to the sample with quick drying silver paste. The sample was then fixed on the sample holder and connected to the electrical circuit shown in fig. 3.4

b) Hall Apparatus

The measuring circuit was designed and constructed in this laboratory. A BBC micro computer was used to control a programmable current source capable of providing currents from 2 μA to 10 mA over 3 ranges in both forward and reverse directions. This current could be fed to any pair of the 4 V.D.P. contacts via the relay unit. The relay unit also allowed sample voltages to be measured across the non current V.D.P. contacts using a Hewlett Packard HP 3456a D.V.M. Current

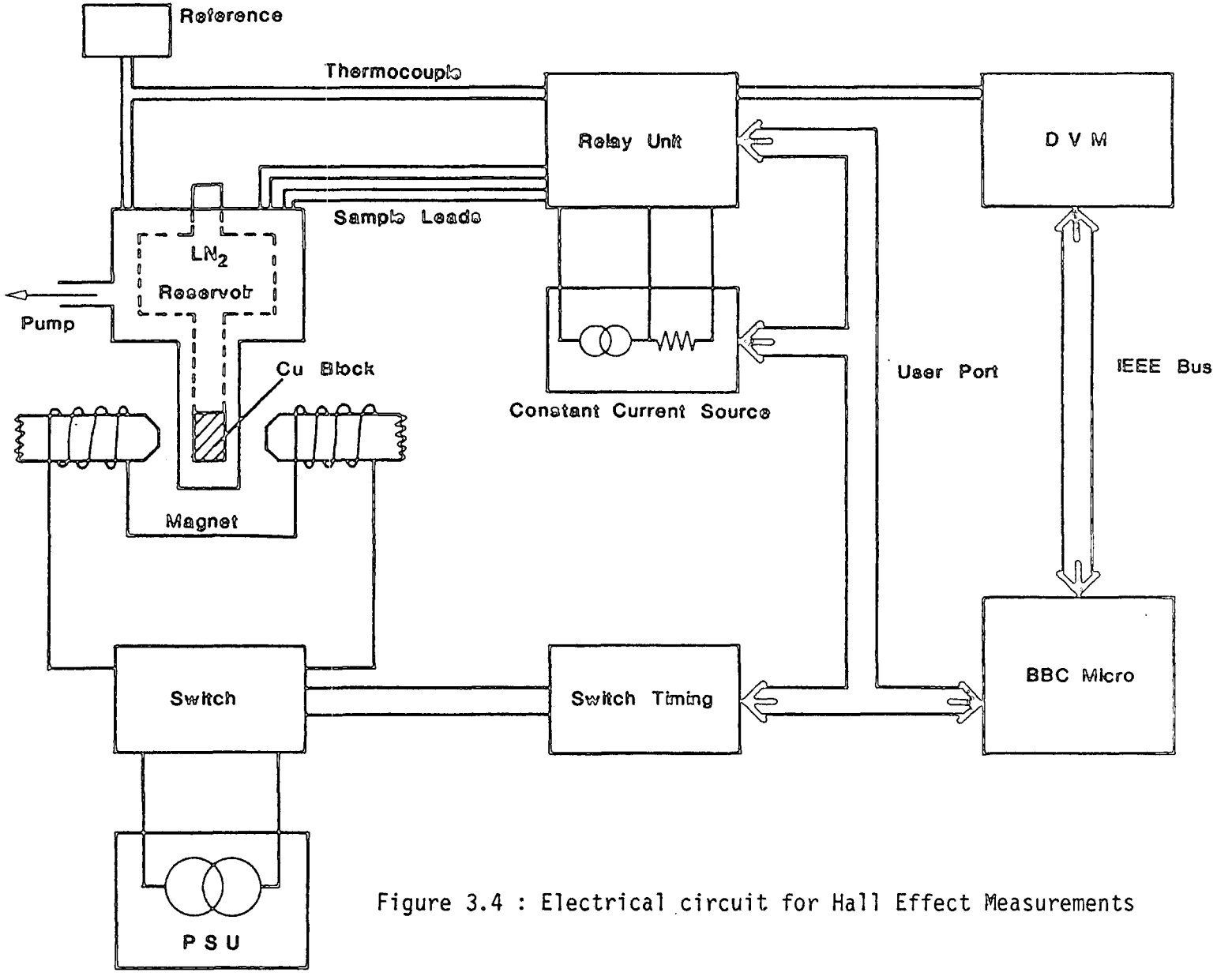

Figure 3.4 : Electrical circuit for Hall Effect Measurements

sensing resistor and thermocouple voltages were also measured with this meter again via the relay unit. Data from the voltmeter was passed to the computer along an IEEE 488 bus for storage and subsequent analysis.

The electromagnet provided a 0.16 T field constant to within 5% in a 1 cm^3 volume around the centre of the pole piece gap. The magnet power supply was a variable constant current source. Field switching and reversing was accomplished by relays which were protected from the back e.m.f. of the magnet by diodes in parallel with the coils. The necessary timed switching of the relays and diodes was provided by a synchronous circuit controlled by the computer.

I-V characteristics were taken for each of the V.D.P. resistivity and Hall configurations. These could be plotted to check for ohmic contacts. A computer analysis program performed a least squares fit to each set of data and so obtained resistance values for the V.D.P. formulae.

From the measurements of the Hall coefficient and the resistivity of the sample, the carrier concentration and mobility were calculated using equations 2.2 and 2.4.

3.3.2 Current-Voltage Characteristics

Current-Voltage characteristics were measured in the dark and under AM1 illumination at room temperature. Simulation of AM1 illumination was accomplished using a 1.5 kw quartz halogen strip lamp with a parabolic reflector housing, and a tray of water 2 cm deep acting as a filter to reduce the infrared content (fig. 3.5). The source was calibrated using a standard silicon PIN diode (type 10 Df, United Detector Technology) and adjusting the distance between the source and the sample to provide 100 mA/cm^2 constant illumination. Measurements of the current-voltage characteristics were carried out point-by-point using a high impedance Bradley Voltmeter (type 173B) and

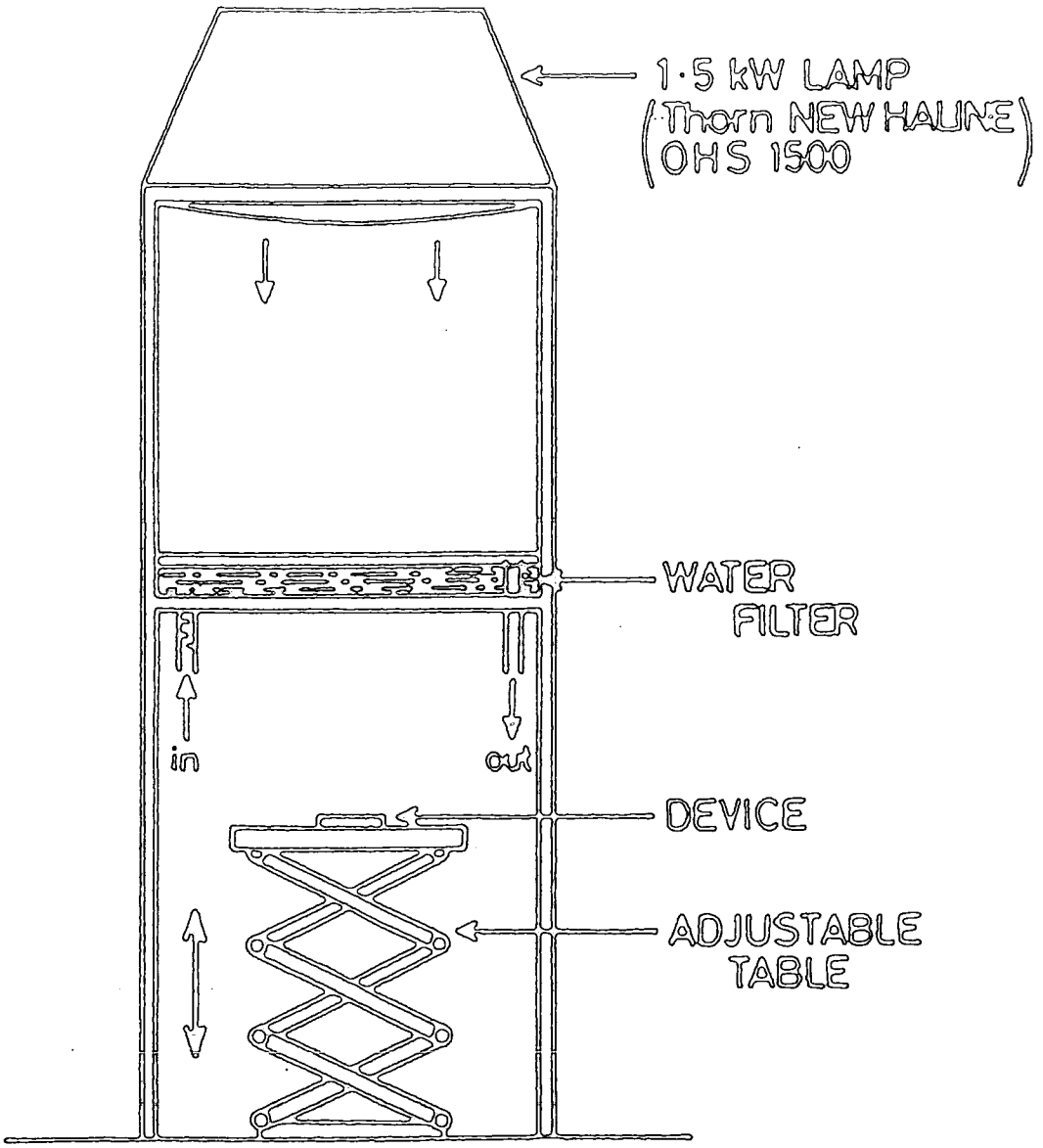

Figure 3.5 : Solar simulator for AM1 illumination

a low impedance Hewlett Packard ammeter (type 3465B). The bias voltage was provided by DC Voltage Calibrator type 2003 (Time Electronics Ltd.). An automated current-voltage tracer employing an X-Y plotter was also used to monitor the effects of different treatments.

3.3.3 Capacitance-Voltage Characteristics

The Capacitance (C) of the Schottky diodes was measured as a function of bias voltage (V) to yield information about uncompensated donor concentration and the carrier mobility in the screen printed CdS layer. By using a Boonton 72B Capacitance meter operated at 1MHZ; C-V characteristics were recorded point-by-point using a calibrated voltage source to provide the bias.

3.3.4 Spectral response measurements

The spectral response of a solar cell was measured using light from the exit slit of a Barr and Stroud double prism monochromater, Type VL2, fitted with Spectrosil 'A' silica prism. A 250 watt quartz halogen lamp driven by a 200 V d.c. stabilised power supply was used as the light source. The energy distribution of the source at the exit slit, which includes the varying dispersion of the prism monochromator was measured using a Hilger and Watts Schwartz compensated linear vacuum thermopile, type FT 16.

The voltage was measured using a Keithley electrometer model 602 which has a high impedance for voltage measurements. The output from the electrometer was plotted on a Honeywell Electronic (Model 196) high impedance chart recorder.

A schematic diagram of the arrangement used for the spectral response measurements is shown in fig. 3.6.

3.4 Device preparation

3.4.1 Schottky diode formation

For the preparation of the Schottky diodes, the CdS samples were

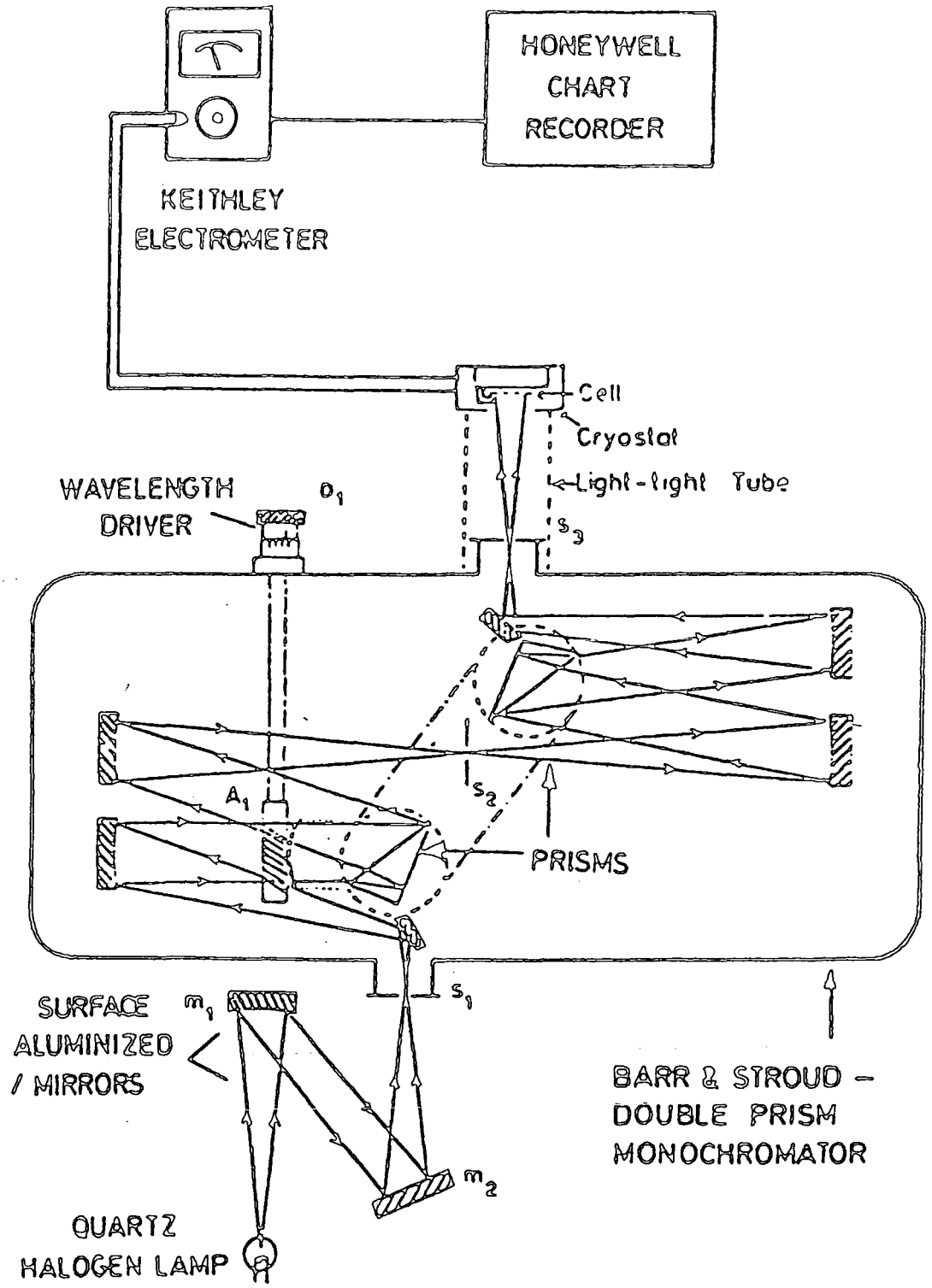

Figure 3.6 : Schematic diagram of spectral response measurement system.

first etched in 3% HCl for 3 seconds, and then Au-CdS diodes were formed by the vacuum evaporation of gold dots (1 mm diameter) onto the etched surfaces. The underlying SnO_2 conductive coating beneath the CdS was used as the back contact of the Schottky device.

3.4.2 CdS/CdTe Solar Cell Fabrication

The main structure of the CdS/CdTe solar cell used in the present work was:

Soda Lime glass/screen printed CdS/thermal evaporated CdTe layer/Ohmic contacts to CdS and CdTe.

The preparation of the screen printed CdS layer will be described in Chapter 4. The other parts of the cell structure were prepared as follows:

i) Preparation of CdTe

CdTe junctions were deposited on the screen printed CdS layers in an Edwards Coating Unit, which is shown schematically in fig. 3.7.

The 'CdS' substrates were mounted in a stainless steel mask and heated radiantly during growth by an infrared lamp (750W). The temperature of the substrate was monitored by a NiCr/NiAl thermocouple attached to the back of the substrate. A quartz crucible with a spirally wound molybdenum wire heater was used as the evaporation source. The charge temperature was measured using a Pt (13%) Rd/Pt thermocouple fixed in a way that its junction touched the bottom of the crucible through a special narrow tube provided for this purpose.

The source material was high purity synthesized CdTe. A small quantity (5-10g) of the charge was placed in the crucible for each run. In order to prevent spattering of the charge the mouth of the crucible was baffled with a thin layer of silica wool. The evaporation rate was calculated from the thickness of the film as measured in the SEM, and

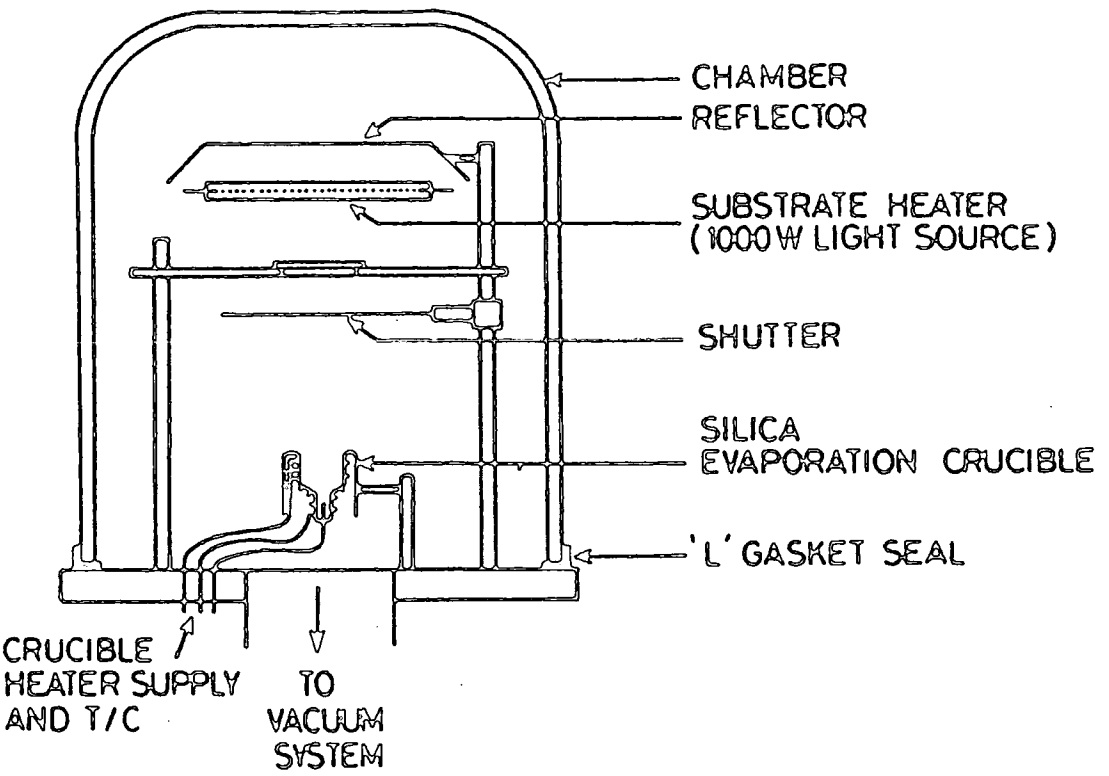

Figure 3.7 : Bell jar fixtures of the evaporator used in the deposition of CdTe films.

the deposition time. The evaporation cycle for the CdTe film deposition was as follows:

1) After loading the system it was pumped down to a pressure of 5×10^{-5} torr, and the substrate were heated to the selected temperature e.g. 150° - 200°C.
2) The evaporation source was then gradually heated to 450° and the CdTe charge was outgassed for 30 mins.
3) Depending on the expected deposition rate the source temperature was raised to lie within the range 750°C to 950°C. When steady state conditions were reached, the mechanical shutter was opened to start the deposition.
4) At the end of the deposition (4-6 mins) the mechanical shutter was closed, and the source and substrate heaters were switched off.
5) The system was allowed to cool down to room temperature, while pumping was continued.

ii) Copper doping

Copper was employed to reduce the high resistivity of the deposited CdTe layer (see later). This was achieved by evaporating a calculated quantity of high purity elemental copper under high vacuum onto CdTe surface, which was then annealed for copper diffusion as will be described later (Ch. 8).

iii) Contact Formation

To complete the cell structure ohmic contacts to CdS and CdTe were made. Contacts to p-CdTe were obtained by vacuum evaporation of gold or by painting a small quantity of carbon paste onto CdTe surface, while for CdS a 1.5 mm pellet of indium wire was pressed and alloyed to form the contact on the screen printed CdS layer near the CdTe junction. With CdS films prepared on conducting glass, the tin oxide layer beneath the CdS film provided the ohmic contact.

References to Chapter III

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CHAPTER FOUR

SCREEN PRINTING FOR SOLAR CELL APPLICATIONS

4.1 Introduction

The screen printing technique essentially consists of the transfer of the print paste of the desired material through a screen onto a special substrate and sintering them to form electronic components.

In general, there are various conditions and controlling factors involved in the application of this technique for the fabrication of solar cells which need to be closely understood and optimised if reproducible results are to be achieved. Otherwise many conflicting results can easily be obtained.

The purpose of this chapter is to examine the significance of the printing parameters and other controlling factors with respect to solar cell applications. This includes device parameters, screen parameters, the substrate, the screen printing paste and various aspects related to the sintering procedure. This chapter will end with a description of a typical procedure for the preparation of a screen printed CdS layer.

It is useful to start this Chapter by reviewing the screen printing technique and giving a short history of its application to solar cells.

4.2 Screen Printing Technique; review and short history

Screen printing, also known as 'thick film' or 'screen and fire' (1) processing is a long established technique which was born in the graphic art industry (2). An extensive review of the early history and application of this technology can be found in an article by Brunettei et al (3). The name thick film was given in the 1960s to differentiate this technique from the already existing thin film technology (4) (5) (6).

The many interesting properties of this technique such as cheap design, reliability and automation (4) have made this technology very useful in various applications.

It was adapted in the late sixties by the microelectronic industry for the fabrication of resistors, capacitors, conductors and related circuit elements on virtually any substrate or printed circuit board material (7) (8).

Recently, this technique has been used for various aspects of solar cell preparation. It has been used for the deposition of diffusion source layers, front grid metalization, back contact metallization, back surface field and for antireflection coatings (9). Today screen printing is accepted as the most effective method for solar cell metallisation in a production environment. Most of the world's largest photovoltaic products use this technology (4) (10).

The utilization of this technique in the preparation of active semiconductor layers for the use in solar cell fabrication was first reported in 1973 by Vodjani et al (11). In 1976 the wireless research laboratories of the Matsushita Company took the lead in developing this technique (12). By 1983 they reported an efficiency of 12.8% for an entirely screen printed CdS/CdTe solar cell of an active are of 0.78 cm^2 (13). A reliable performance of their cells was observed under roof top conditions (14). The major achievement of the Matsushita group was reviewed very recently by S. Ikegami (15).

A typical manufacturing procedure for entirely screen printed CdS/CdTe solar cells is shown in Fig. 4.1.

Several other groups in the world have started using screen printing techniques in producing other solar cells structures such as CdS/$CuInSe_2$ (17), CdS/polysilicon solar cells (18) and screen printed particulate silicon solar cells (19).

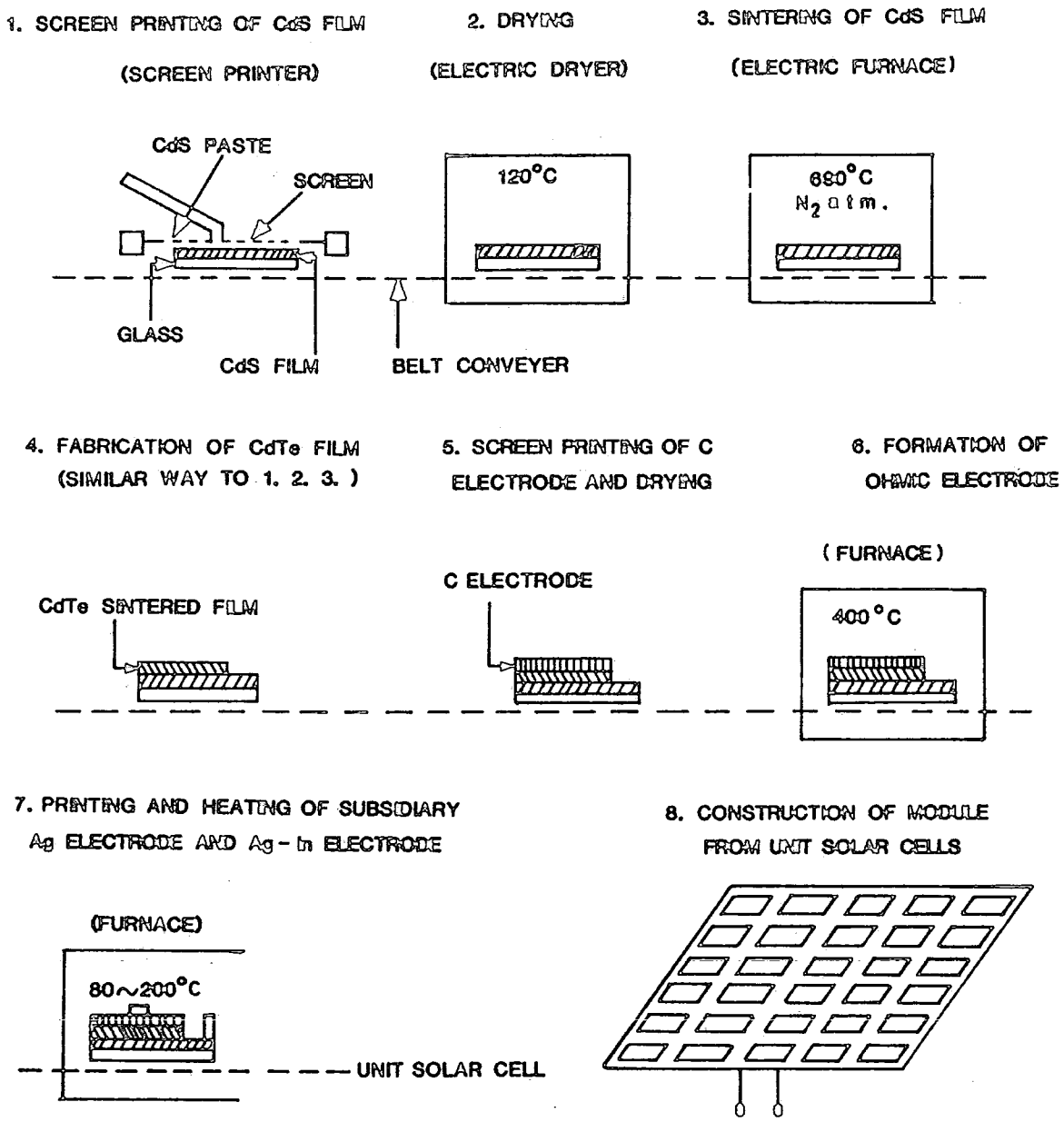


Fig. 4.1 A typical manufacturing process for entirely screen printed CdS/CdTe solar cell (ref.16)

Since the work reported by Matsushita group was described in terms of solar cell parameters, effort has begun to understand the effect of various parameters involved in the fabrication of the screen printed devices (20-23). The work described in this thesis forms a further contribution.

4.3 Screen Printing device

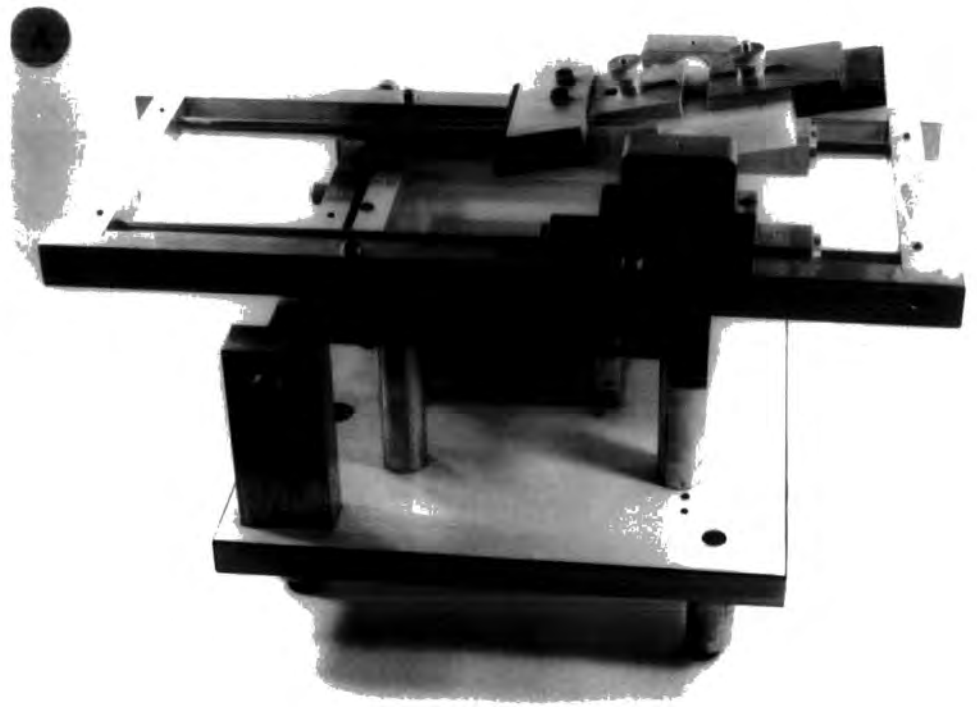
The availability of a proper screen printing device is very necessary for reproducible printing procedure. To fulfil this requirement a screen printer was designed and built in this laboratory and optimised, following a series of trials, to produce an accurate print quality. The device has the following specifications.

1) A printing base with a vacuum to keep the printed material (substrate) in place and prevent it from adhering to the bottom of the screen.
2) A raising mechanism for adjusting the substrate from screen (snap off distance).
3) A proper screen frame with stretching mechanism to hold the printing screen tight.
4) A squeegee with controlling mechanism to adjust the angle and pressure, which can travel forward and backward on a linear track.
5) The screen frame as well as the squeegee mount to be securely held by special clamps.

A photograph of the screen printer together with its main components are shown in Figs. 4.2A and B.

4.4 Effect of printing parameters

There are a large number of variables which may affect the quality of the print produced by the screen printing processes (24). However, it is believed that device parameters and screen parameters are the two major ones which can largely influence the printing conditions (1).



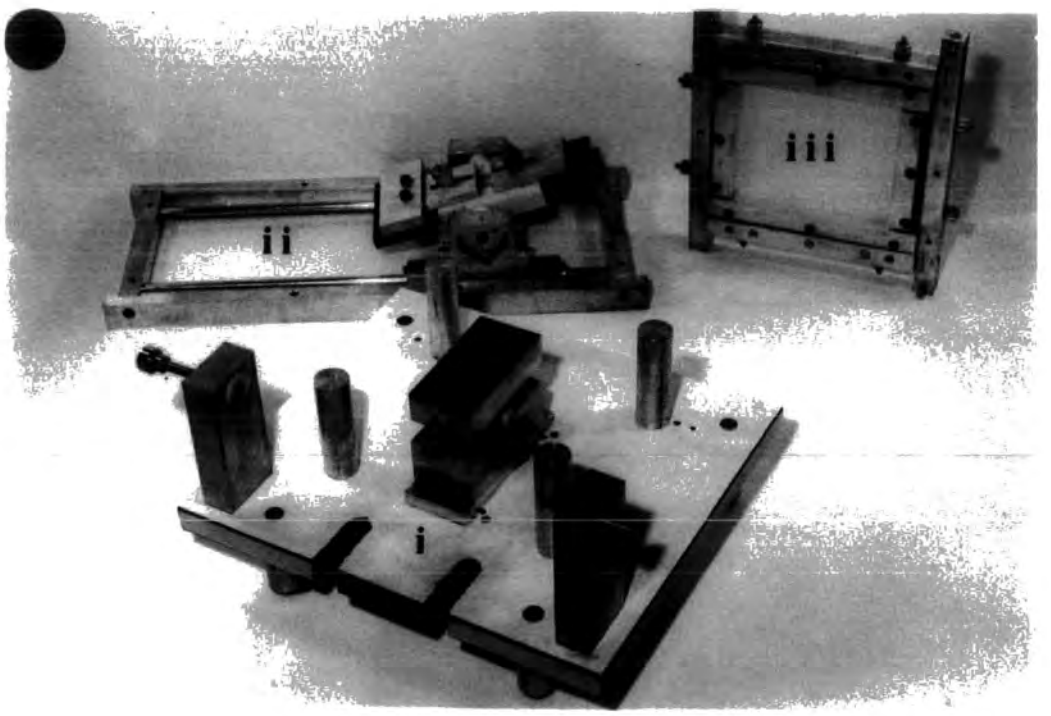


Fig. 4.2

A The screen printing device

B Device components

i Substrate vacuum base and raising mechanism
ii Squeegee mountain
iii Screen frame

In the following sections the magnitude and effect of these parameters will be briefly described.

4.4.1 Device parameters

The most important device variables are the squeegee, the snap off distance and volume of paste on the screen.

1) The Squeegee: It is made of a special rubber blade held by a metal handle. In principle, it is used to force the printing paste through the screen and deposit it on the substrate. The role of the squeegee in the printing procedure has been reviewed by many authors (1) (25).

However, for the purpose of this study special care must be taken to ensure the following: i) the use of an inert squeegee which does not react with the printing paste, ii) a relatively hard squeegee blade with square edge shape to help in maintaining the squeegee angle of attack and removing the surplus paste from the screen surface sharply, iii) the squeegee should be applied at a special angle which helps in using the area immediately below the edge to push the paste through the screen. The angle of attack has to be decided for each experiment since it varies with screen parameters and paste properties and finally iv) the squeegee pressure must be adjusted with the snap off distance such that it should not deform the squeegee edge and change the angle of attack.

The normal squeegee stroke is shown in Fig. 4.3.

ii) Snap off distance: This is the distance between the substrate and the screen at rest. This distance depends on the tension of the screen (4) and it is desirable that it should be as small as possible and consistent with achieving a satisfactory peeling action of the screen immediately behind the squeegee blade. This peeling is very important in the screen printing process as the rate of separation of the screen

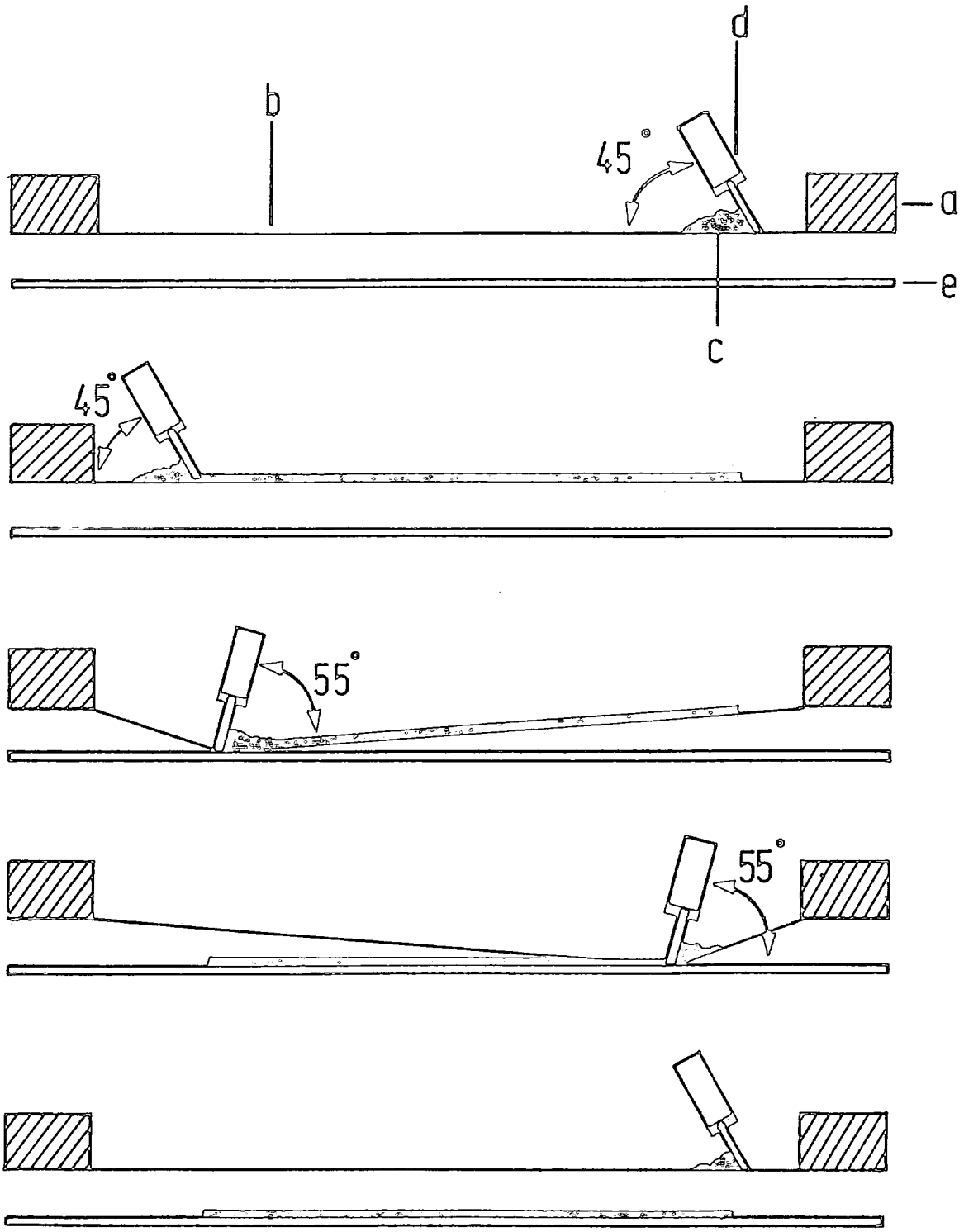


Fig. 4.3 The normal Squeegee Stroke

a) Frame; b) Screen; c) Paste; d) Squeegee; e) Substrate

from the substrate is the principal factor controlling the ratio of paste transferred to the substrate to that left in the screen (1). In practice the snap off distance varies between 0.6 and 1 mm (4).

iii) Amount of paste on the screen: It is necessary to apply a controllable amount of paste to the screen since a large volume of paste tends to reduce the squeegee attack angle and produce a heavier deposit.

Following a series of trials the device parameters in this study were optimised to the following:

Using a polyurethane squeegee blade with hardness of 70 Shore A (Serical Co.) with a square section, two angles of attack were used, 45° for paste distribution on the screen and 55° for the deposition of paste on the substrate through the screen (see Fig. 4.3). Care was taken to apply the same amount of paste each time using a spatula for each print.

4.4.2 Screen parameters

The screen is the most important part of the screen printing process (26). It acts as a metering device for the deposition of a controlled amount of paste (5). Different screens are characterized by various parameters (1). The most important ones are; screen material, screen tension, mesh number, wire diameter and percentage of open area. The significance of these parameters has been reviewed in detail by several authors (1) (26) (27).

In what follows, brief comments in each parameter will be given.

i) Screen material: Three types of screens are currently being used for screen printing, namely, nylon, polyester and stainless steel. The latter has been widely used in electronic circuit applications. However, it is costly and has a low life. In addition, stainless steel loses its resilience quickly. On the other hand a nylon screen has a

high resilience but it is inclined to stretch when under pressure from the squeegee. The polyester screen represents the best compromise between the lack of resilience of the stainless steel and the high elongation of the nylon (27). Moreover it is a low cost material.

ii) Screen tension: Different types of screen have different stretching values. To obtain a high quality print, it is important that the screen is tensioned to the recommended values. Screens which are too loose will not release properly from the substrate and will pull off some of the printed paste, while very tight screens may cause splitting of the screen and premature loss of tension.

Information about screen stretching and tension level, together with the proper tension mechanism, can be found in the accompanying sheet of information of the screen used.

iii) Screen thickness: This parameter plays an important part in controlling the thickness of the final screen printed layer. The thickness of the screen is normally measured in microns. A coarse screen will result in a thick coating of paste, consuming a lot of paste and requiring a long drying time (28), while a fine screen will result in a light coating, less paste used and less drying time.

iv) Mesh number: This is defined as the number of wires per inch. The mesh number is usually considered as a measure of the expected deposit thickness, the lower count gives a thicker deposit while the higher the count the finer the deposit.

v) Wire diameter: Measured in microns. Normally a thin diameter is desirable to allow a small distance between mesh opening.

vi) Percentage of open area: A large percentage of open area is needed since the paste will pass more readily through the screen without hanging in the mesh opening. The mesh opening in particular must be large enough so that the larger paste particles do not clog the

screen. It is recommended that the mesh opening should be approximately $2\frac{1}{2}$ to 5 times larger than the average grain size of the paste material (26).

The above described parameters are shown in Table 4.1 for some selected screens.

Screen Material	Mesh No.	Stretching %	Thickness µm	Wire diameter µm	Mesh opening µm	Percentage of open area (%)
Polyester	53	3	290	160	216	44
Polyester	125	4	125	70	134	43
Polyester	196	4	100	55	74	32
Stainless Steel	165	.5	106	50	104	46%

Table 4.1 : Major screen parameters

Fig. 4.4 illustrates the importance of some of the above parameters in producing the final thickness of the deposit. It is clear that by using a thinner wire diameter (d), the paste cubes will have very small gaps between them so that they only have small distance to flow to form an even layer. With thick wires the cubes will not flow out sufficiently and hence will produce a non uniform layer.

A trial to investigate the thickness of the deposit by varying the mesh number of the screen and the screen material is illustrated in Fig. 4.5. It is clear that a '53 mesh' polyester screen produced the thickest deposit (~ 70µm), while a '196 mesh' polyester screen gave the thinnest deposit (~ 15µm). A '125 mesh' poly screen gave a thickness

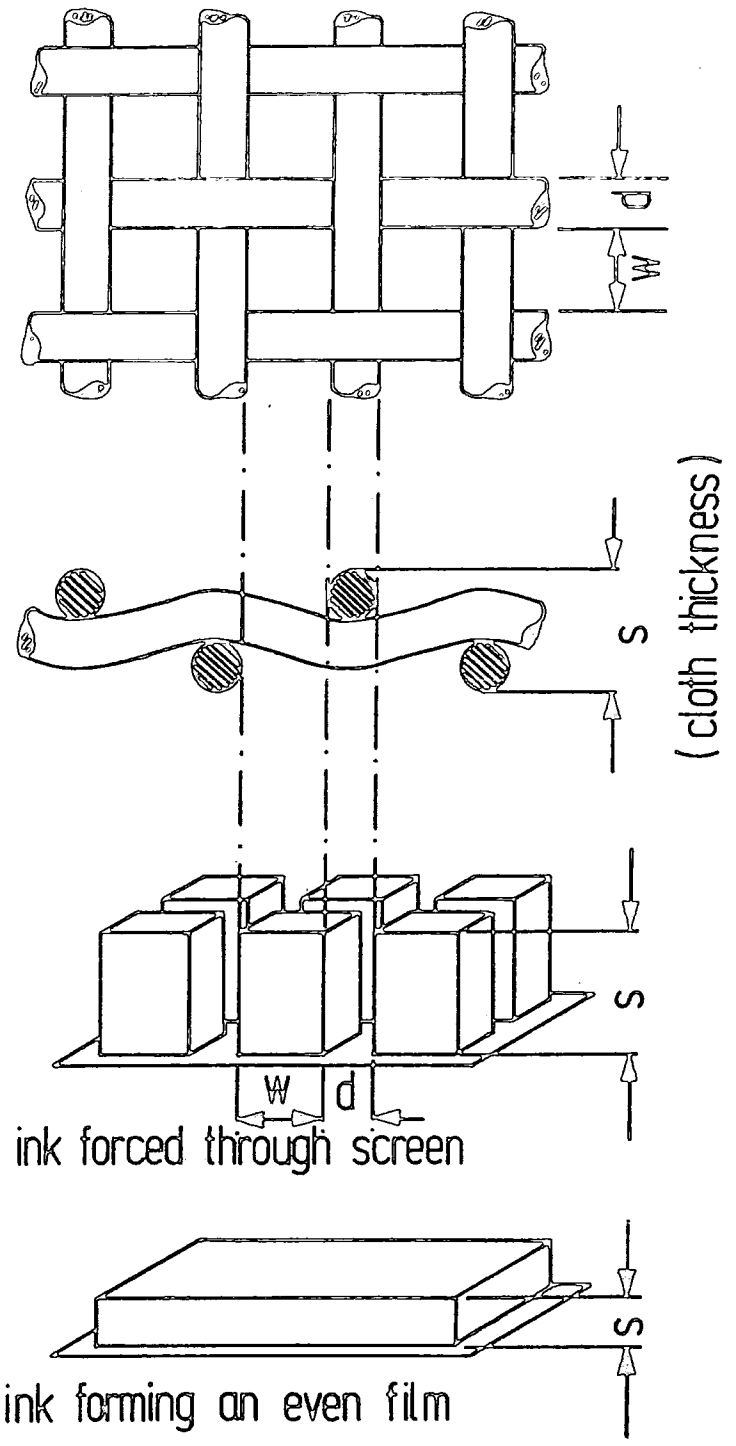


Fig. 4.4 Significance of screen parameters on print quality (W : mesh opening; d : wire diameter; S : screen thickness and S* : theoretical thickness)

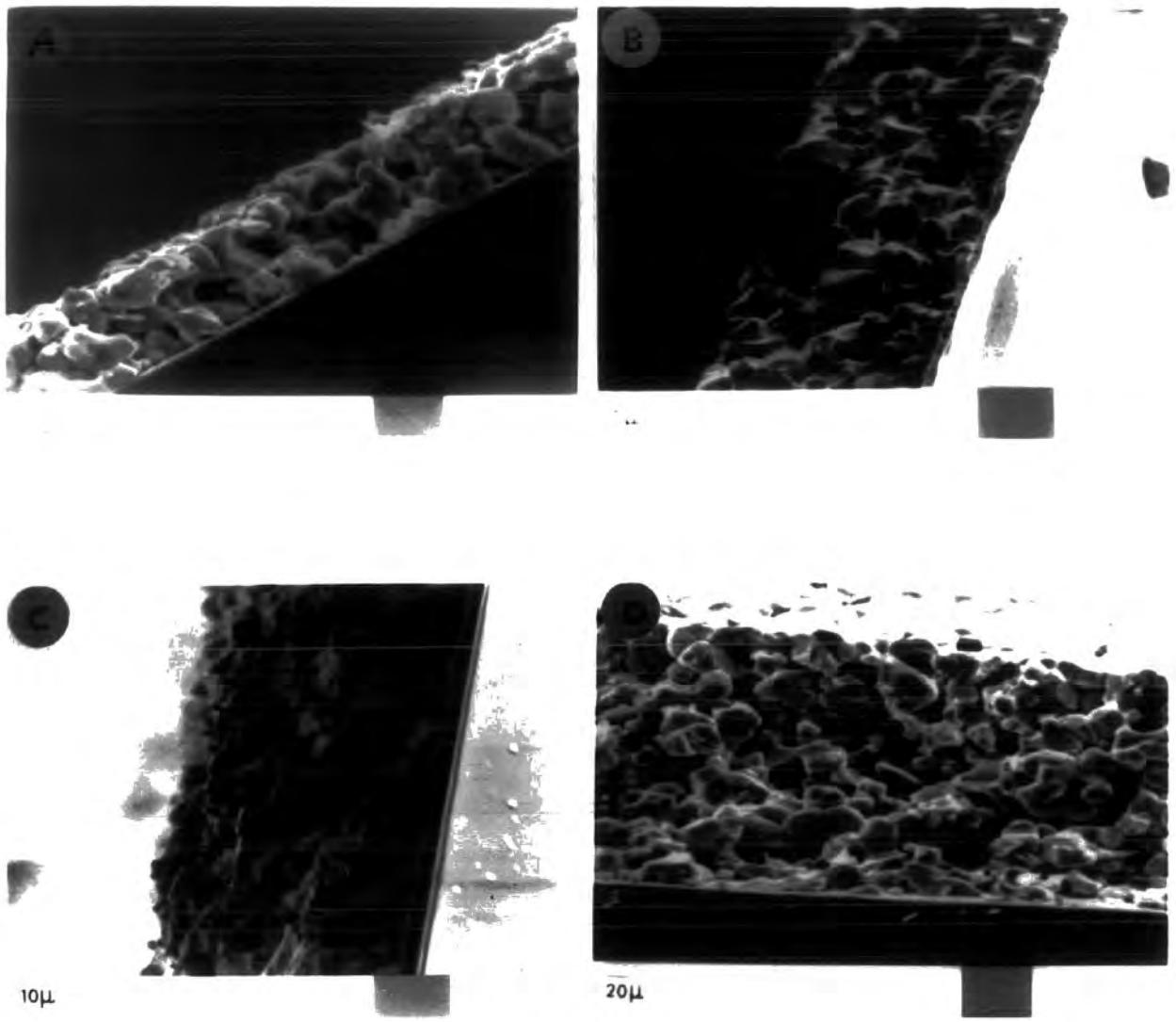


Fig 4.5 Variation of screen printed film thickness with different screens

A 196 mesh polyester screen

B 125 mesh polyester screen

C 165 mesh stainless steel screen

D 53 mesh polyester screen

of 25μm. It is interesting to note that although '165 mesh' stainless steel had a higher mesh number than '125 mesh' poly screen, and would therefore be expected to yield a thinner deposit thickness (sect. 4.4.2-iv), nevertheless, the thickness produced was larger (~ 35μm). This may be attributed to the finer wire diameter, and larger percentage of open area (Table 4.1) (27).

It should be mentioned here that although the ultimate thickness of the paste deposit is additionally influenced by other factors (e.g. viscosity of the paste (see later), device parameters (section 4.4.1) etc.) the mesh opening, wire diameter and screen thickness are the most important features.

For the purposes of this study '125 mesh' polyester screen was used most of the time.

4.5 The substrate

4.5.1 Substrate properties

The substrate plays an important part in the screen printing process and its effect on the final film properties is very significant (29).

In general the major requirements of a substrate for screen printing application may be summarized as follows:

(1) It should have good electrical insulation properties

(2) provide a strong, stable support for printed components and attached device.

(3) maintain dimensional stability without bowing at the temperature used.

(4) have high thermal conductivity for greater heat dissipation.

(5) have a similar coefficient of thermal expansion to that of the film to reduce the stress.

(6) be chemically and physically compatible with the appropriate paste components, so that a strong bond between the screen printed film and the substrate is formed.

(7) have a low cost in quantity production (5).

The most frequently used substrates in screen printing are of glass. The properties of these vary widely depending on their chemical composition (30). Some typical chemical compositions of commonly used glasses and their major properties are shown in Table 4.2.

Three glass substrates were mainly used in this study; namely, soda lime, borosilicate 7740 and a soda lime coated with 'SnO_2'.

The significance of these substrates in screen printing applications will be discussed in detail in Chapter 7.

4.5.2 Substrate Cleaning

Glass substrates must be thoroughly cleaned before the deposition of the printing paste to ensure reproducible results (1).

A variety of cleaning procedures exist, depending on the nature of the substrate, the type of the contaminants and the degree of cleanliness required (30). The following procedure is normally adequate for cleaning glass substrates (31) and is used in this work: The gross contaminants are first removed by warmed detergent mixed with dionized water in an ultrasonically agitated bath. The glass is then rinsed thoroughly several times in deionized water and later subjected to a vapour degreaser using Isopropane Alcohol (IPA) for several minutes to ensure that no strains persist on the dry substrate.

4.6 The screen printing paste

4.6.1 Introduction

The materials that are to form the desired device are made up into the form of viscous paste, for application to the substrate.

no.	Glass type	Major Compositions							Strain Point (°C)	Thermal Expansion Coeff. (0-300°C)	Thermal Conductivity W cm^{-1} deg^{-1}
		SiO_2	NaO	CaO	MgO	Al_2O_3	BaO	B_2O_3			
1	Soda Lime Corning 008	67.7	15.6	5.6	4.0	2.8	2.0	1.5	472	9.2	.009
2	Borosilicate Corning 7746	80.6	4.1	-	-	2.5	-	10.3	520	3.25	.018
3	Borosilicate Corning 7059	50.2	-	-	-	10.7	25.1	13	613	4.5	-
4	Fused Silica Corning 7940	99.5	-	-	-	-	-	-	990	.56	-

Table 4.2 Composition and major properties of some common glass substrates (Ref. 30)

The main paste constituents and a typical formation mechanism will be described below.

4.6.2 Paste constituents

The paste used in this study contained three major constituents, i) the active powder, ii) the flux and iii) an organic binder.

i) The active powder. This is the functional constituent in the paste. After sintering it determines the electrical properties of the layer. Various aspects related to the powder application in screen printing will be discussed in chapters 5 and 6 . In general, purity, grain size and grain size distribution of the powder will greatly influence the paste formation and the subsequent sintering procedure (1) (4).

ii) The flux. This is a special material which is included in the paste and has a low melting point so it helps to promote contact between the powder particles during sintering, and causes adhesion of the paste onto the substrate. Further discussion of the role of the flux in the sintering procedure will be given in the next section, while the significance of using a controlled ratio of flux in the printing paste will be discussed in Chapter 6. It is worth mentioning here that the flux material also provided the donor dopant (see later).

iii) Organic binder. This is a viscous liquid in which the powder and flux are mixed and suspended. In general, the binder should have the following functions (28) a) joining the powder particles together, b) making possible the processing of printing and c) adhering the paste to the substrate.

Due to the carbon content of the binder it should burn off completely during the sintering procedure leaving no residue. The proportion of binder in the paste is expressed in volume percent and a proper ratio used should be sufficient to wet the powder particles and

to fill all the voids between them. When the proportion is greater than the critical point, air filled voids form in the dry film. The correct ratio will result in a void free continuous printed film. This correct ratio is influenced by many parameters such as powder grain size and purity (32).

Various types of binder such as cellulose derivatives, vinyls and glycols may be used for screen printing applications depending on the properties desired.

Glycols are often used in screen printing since their slow evaporation maintains the film open or wet for a long time to allow a satisfactory coalescence and a more coherent film in the room ambient.

Among various glycol types, the most commonly reported in the screen printing literature is 'propylene glycol' which has the following properties:

° Composition : $CH_3CHOHCH_2OH$

° Boiling Point : 187°C

° Density : 1.036

This binder was used in the present study.

4.6.3 Paste formation

i) Mixing Procedure

Probably the most critical part of a screen printing process is the mixing procedure of the paste constituents. Great care must be taken to apply the same mixing procedure for every paste preparation. The function of mixing in this study was to achieve the following purposes:

a) Flux and dopant distribution : Since flux material and impurities are normally mixed with the initial screen printed paste, proper mixing is of great importance to ensure the correct distribution and intimacy of these materials with other paste constituents (i.e. powder and

binder). Otherwise unsatisfactory results would occur. Experimental results will be described in Chapter 6.

b) A good screenable paste, which is required for smooth printing operation, can be achieved by the rubbing action between the paste constituents, which will make each particle of the ingredients wet and completely mixed with the binder. Also during the process the powder agglomerates will break down helping to expose more particles to the paste (33).

A proper paste mixing equipment is needed, and specialized roller mills are best for preparing a proper paste. A mortar and pestle is also beneficial. The mixing procedure followed in this study was performed manually using a glass beaker and a rod, where the paste was mixed thoroughly with the help of ultrasonic stirring. Ultrasound is very effective in dislodging mechanically interlocked particles (34) and produces a fine and uniform dispersion.

ii) Paste Characteristics

The flow behaviour (rheology) of the screen printing paste is mainly controlled by the viscosity of the paste. Other influencing parameters are described in the literature (35-37).

The viscosity of the paste can be described as "how a substance flows" (28). It is a measure of the inner resistance of the paste, which is also called its consistency. The greater the inner resistance of the paste, the more slowly it flows.

The viscosity is mainly influenced by two factors, i) the characteristics of the paste constituents (e.g. powder purity and particle size) and ii) the volume ratio of binder to powder.

The viscosity requirements of the paste are complex (4) (37). Generally, during screen printing the paste must be viscous enough (thin) whereas immediately after the printing the viscosity must

increase (thick) to allow a levelling off of the printed layer. Fig. 4.6 shows the variation of paste viscosity with time. It is clear that a sharp decrease in the viscosity at the moment of printing through the screen will allow the printing of more material in a shorter time. This behaviour is called thixotropy (4). A good thixotropic paste is one which will allow (a) easy smooth distribution over the screen to fill the mesh without excessive pressure, and (b) smooth release of the screen from the substrate leaving a minimum of paste in the mesh after printing.

Non-optimum paste properties can lead to undesirable printed layers. For example, a porous structure can result from an increased binder ratio, cracks can occur if water is used in an attempt to improve the viscosity, and screen marks may occur if levelling properties of the paste are lacking. A set of these printing faults is shown in Fig. 4.7 A, B and C together with a normal printed structure in Fig. 4.7 D.

4.6.4 Correlation

Paste properties and printing variables are closely inter-related and a strong correlation exists between them. G. Dubey (38) indicated that with every paste, the mesh size, the material of the screen, the snap off distance, and the squeegee parameters have to be optimised, otherwise completely meaningless results would be obtained. For example, the thickness of the printed layer depends largely on two parameters; the viscosity and the mesh number. It is necessary in studying the effect of changing one parameter to ensure that the others remained unchanged.

In general, the printing faults which occur in screen printing are usually concerned either with improper paste formation or with improper printing parameters.

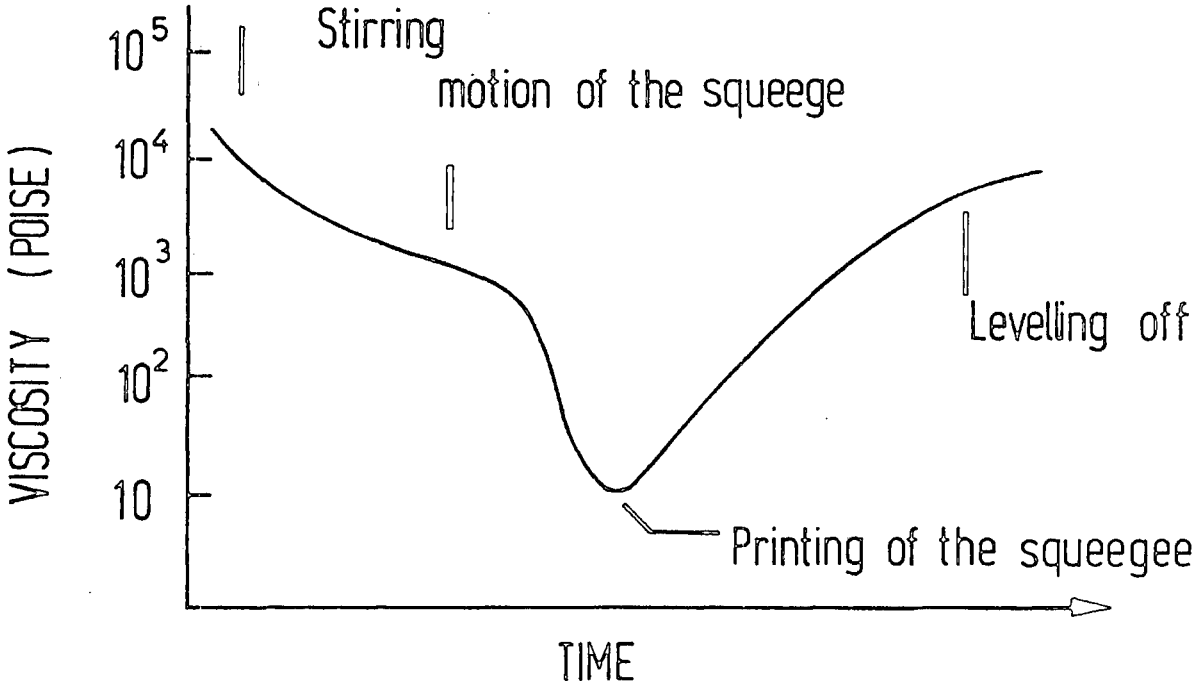


Fig. 4.6 Paste viscosity as a function of time (ref.4)

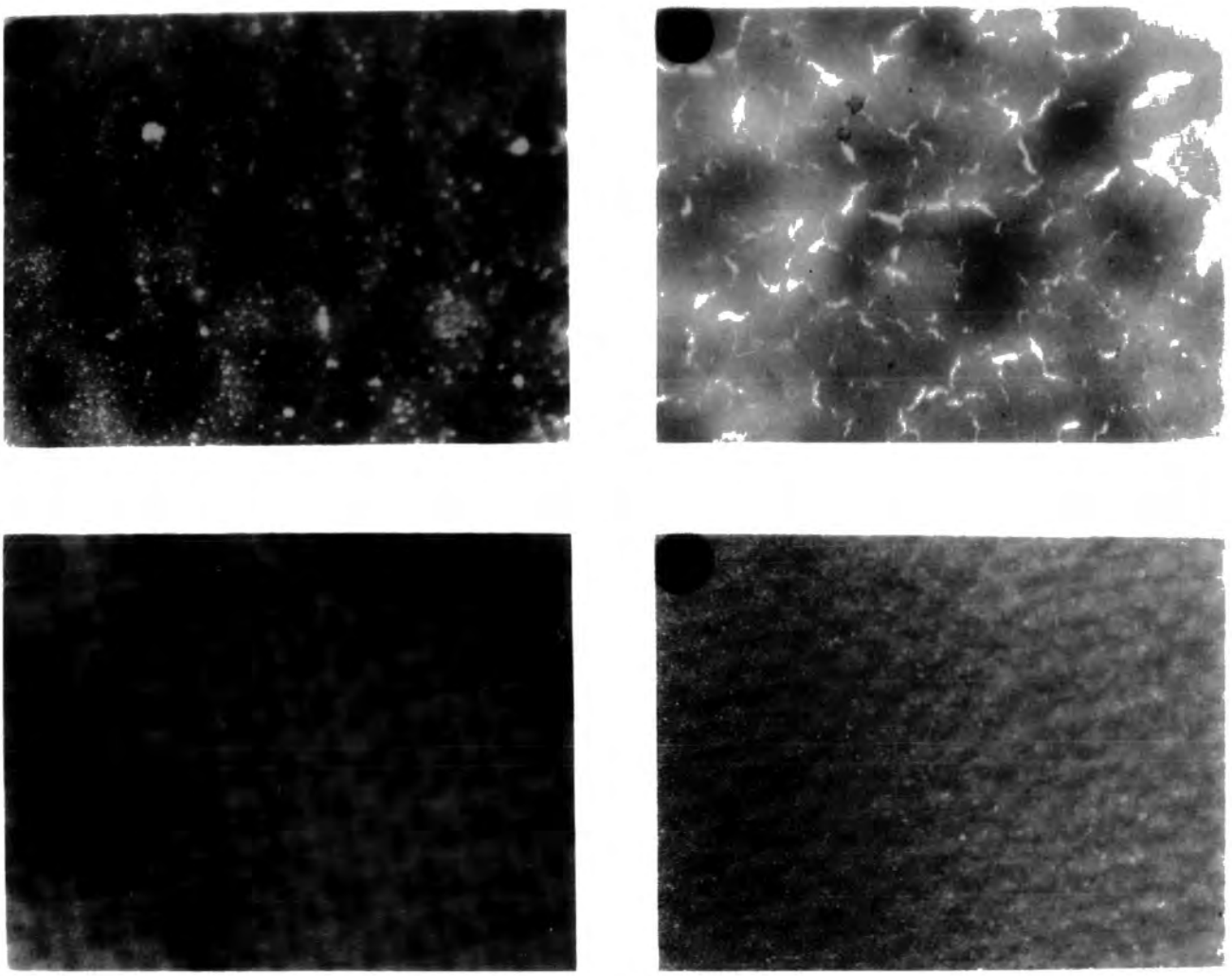


Fig. 4.7 Optical microscope micrographs of different screen printed layers using non proper paste constituents

A porous structure
B cracks
C screen marks
D normal structure

The most commonly occurring faults together with their possible causes have been discussed by many workers (1) (5).

4.7 The Sintering Stage

4.7.1 Introduction

The sintering stage is an essential part in the screen printing process. In fact the process is frequently known as the screen and sintering technique (15). It is during the sintering process, that the electrical and mechanical properties of the film are developed (1).

In what follows a brief description is given of the various furnaces used for the sintering process, as well as of the sintering envelope. The sintering procedure and the sintering theory will be presented.

4.7.2 Furnace Studies

i) Furnace type

The sintering operation is performed in a special furnace in an inert atmosphere. The literature of screen printing indicates that there are three furnaces which are normally used for sintering purposes; the belt furnace (15) the muffle furnace (39) and the tube furnace (21).

i) The belt furnace, this is the most commonly recommended furnace for sintering screen printed layers (4) (40). It uses infrared radiation for heating and has an accurately controlled sintering profile. It is designed so that it is long enough to complete the whole sintering procedure. The printed layer simply rests on a belt which has a preset speed depending on the desired sintering time. The belt moves through various sintering zones. The first zone is the prefiring zone. The second is the high temperature sintering zone and the third is the cooling zone. In passing through the length of the furance, the sample is gradually raised to the desired sintering

temperature and then gradually cooled down to approximately room temperature. Each zone has its own atmosphere and changes over from one to the other with the opening and closing of special valves. The volatile fumes from burning the binder from the sintered layer are disposed through a special central exhaust.

Unfortunately, these furnaces are too costly to be used for Laboratory purposes. As a result other options are needed.

ii) Muffle furnace : this furnace has a major application in ceramic screen printing (39). It consists of a rectangular cavity and was tried here in an attempt to provide a better closed atmosphere during the sintering process. However, the major disadvantages of this furnace were its slow sintering rate and very long cooling period, in addition to difficulties in removing the vollatilized fumes and burning the binder. Experimental results using this furnace will be discussed in Chapter 6.

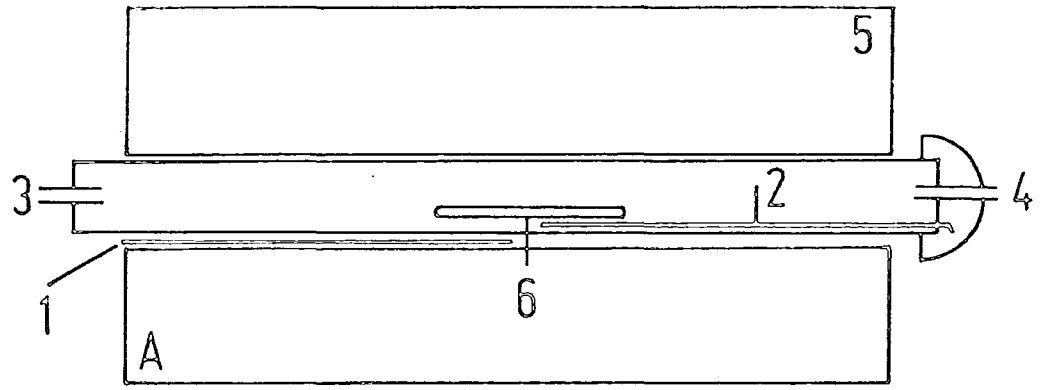
iii) Tube furnace : this conventional furnace was mainly used in this study. It consists of a silica tube overwound with the heating element. The sample was placed in the central zone.

The furnace system used and its temperature profile are shown in fig. 4.8 A and B.

ii) Sintering rate

Close control of the sintering rate of the furance is important (41). The sintering rate must be chosen to meet the desired requirements of a final layer.

A study of various sintering rates of the tube furnace is illustrated by the curves in fig. 4.9 together with those for the muffle furnace for comparison. The numbers shown on the sintering rate curves are representative of the maximum power used to change the



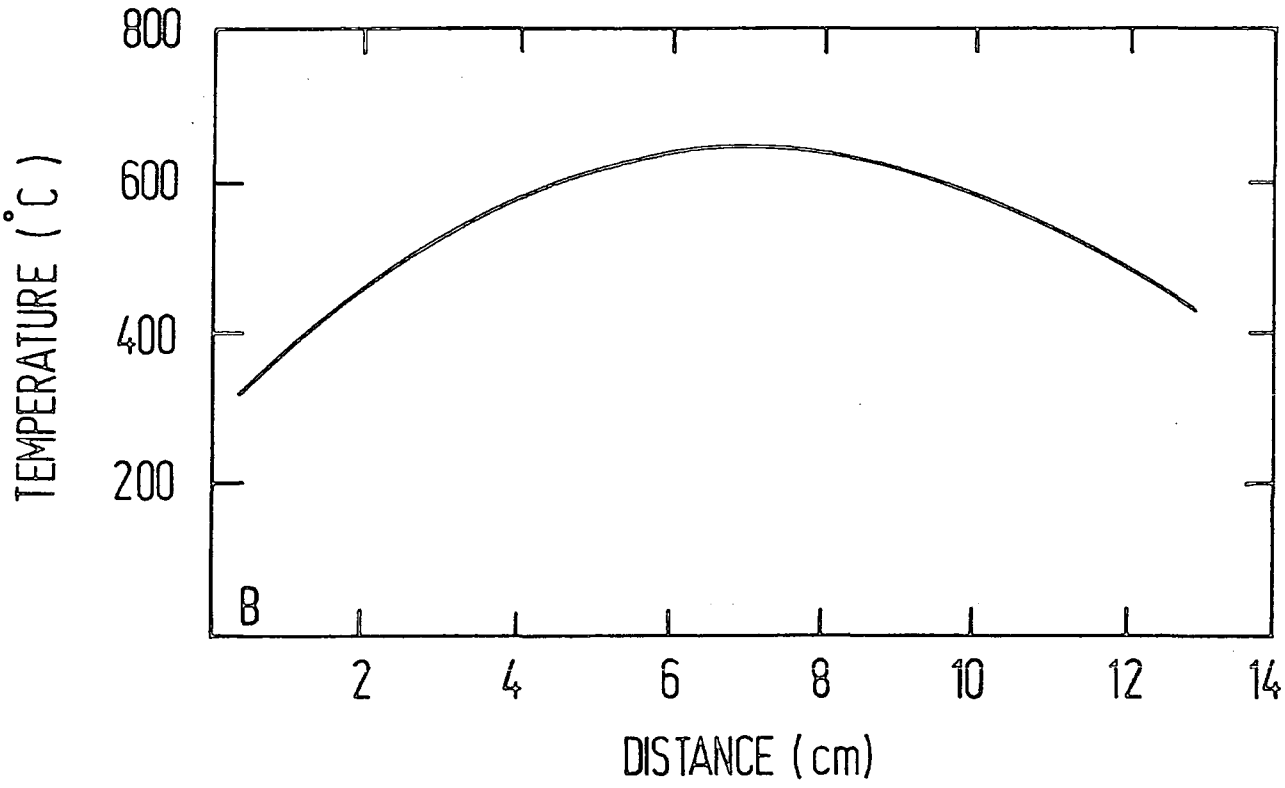


Fig 4.8 Furnace System and temperature profile.

A Furnace System
1. Controll thermoconple
2. Measuring "
3. Argon inlet
4. Argon outlet
5. Furance
6. Sample

B Temperature Profile

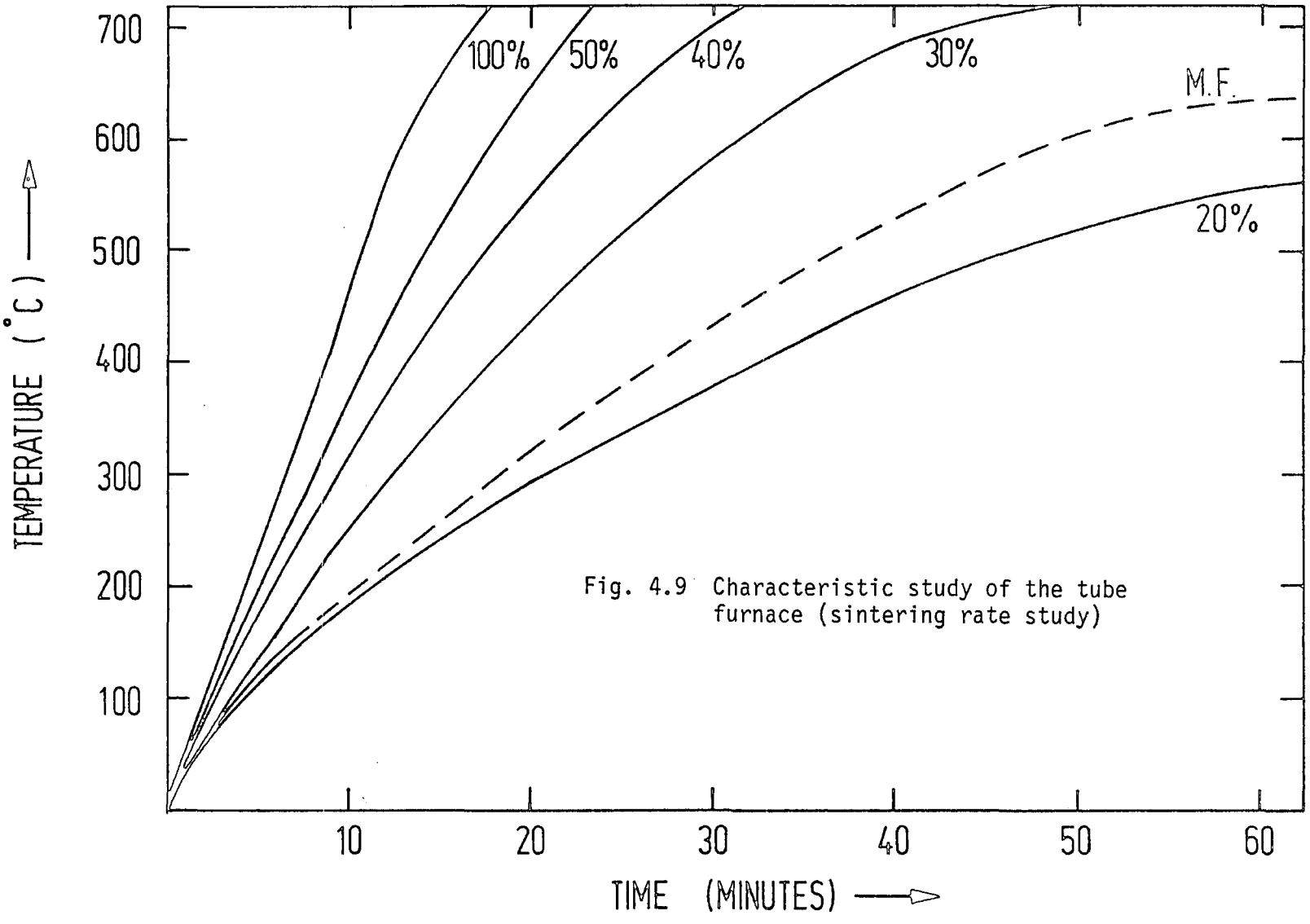


Fig. 4.9 Characteristic study of the tube furnace (sintering rate study)

sintering rate. Their interpretation and significance will be discussed in Chapter 6.

Different tube furnaces have different sintering rates depending on the windings of the heating elements.

iii) Cooling rate

The cooling rate of the furnace must be closely controlled to avoid undesirable effects. Fast cooling can induce stacking faults with cubic structure (42) and it can also disturb the compactness of the layer. Very slow cooling can cause deviation from proper stoichiometry through the differential evaporation of sulphur.

The cooling rate curve of the tube furnace used is shown in fig. 4.10. It indicates that a long time was needed to cool the sample from the high sintering temperature to room temperature. As a result a typical cooling procedure was followed to minimize the effects of the cooling period as will be described later.

4.7.3 Sintering envelope

The screen printed layer is placed in a specially designed sintering envelope and inserted into the central zone of the tube furnace (see fig. 4.8 A). A schematic diagram of the sintering envelope used is shown in fig. 4.11. It consists of a cylindrical boat which is covered with another specially designed boat such that it leaves an elongated 2mm opening. The sample rests on a special support to equalize the temperature of the printed substrate which might otherwise vary due to the geometry of the cylindrical boat. The choice of the support is not crucial, it is very critical. It is easy to obtain misleading results with an inadequate support. A good support is one with (1) high thermal conductivity which will allow good heat transfer and (2) low thermal expansion so as not to be affected by the high sintering temperature and thus always offer a flat surface with

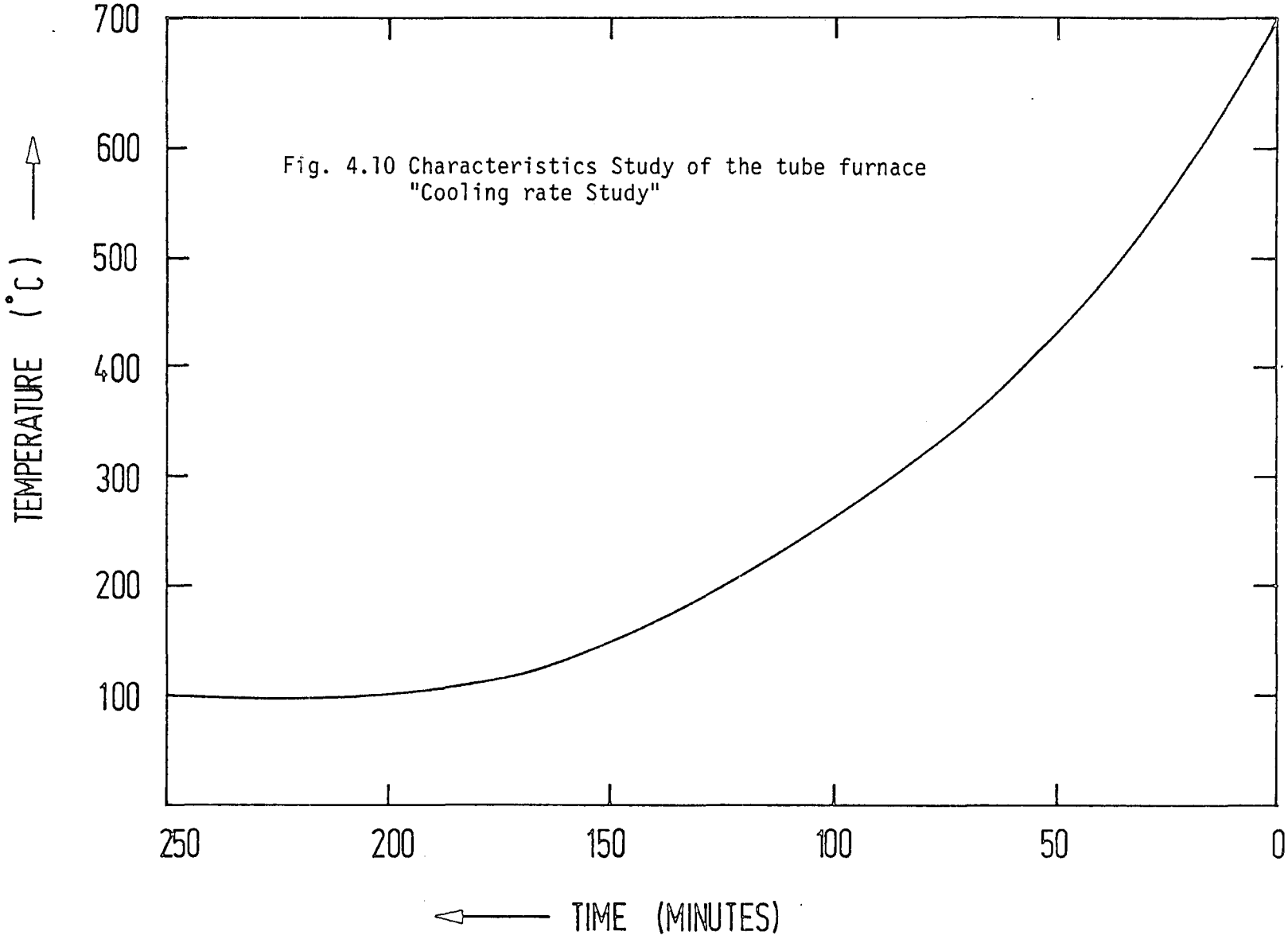


Fig. 4.10 Characteristics Study of the tube furnace
"Cooling rate Study"

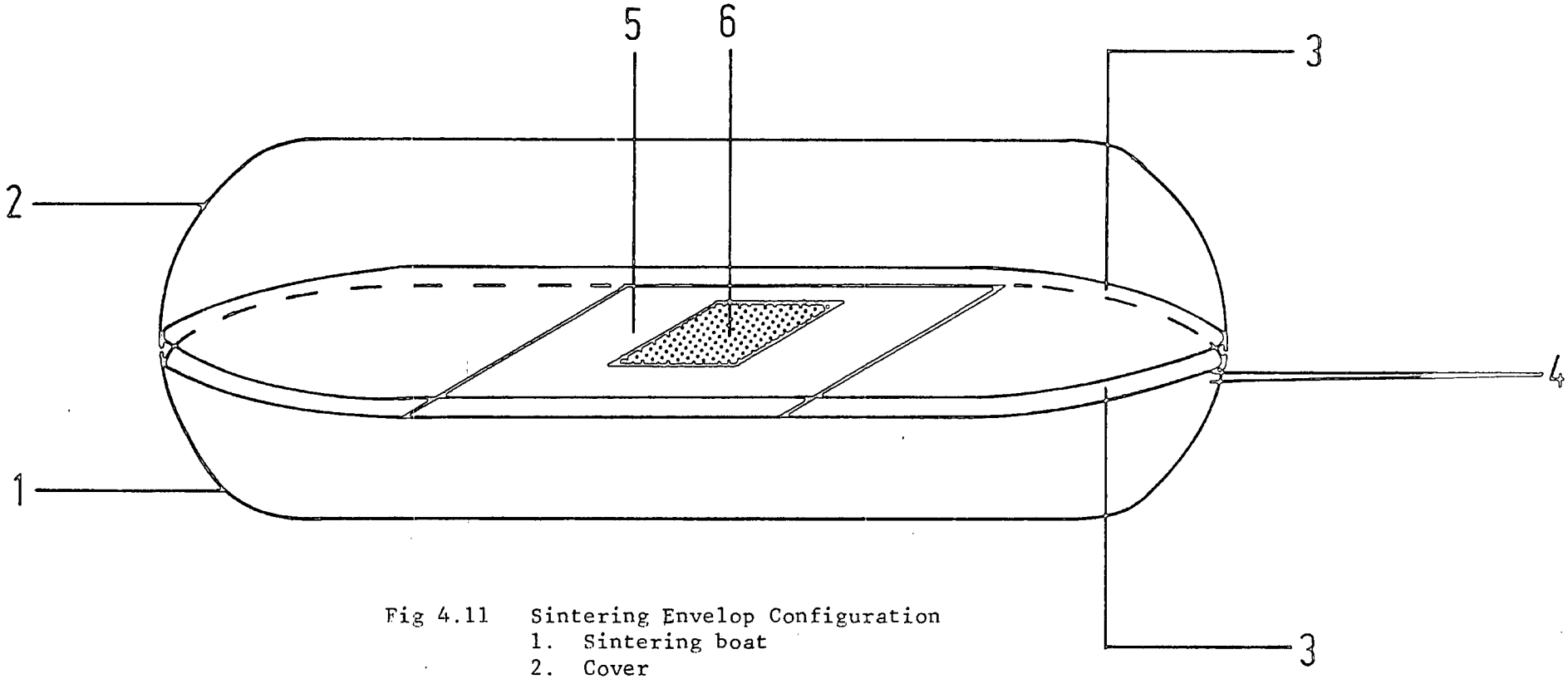


Fig 4.11 Sintering Envelop Configuration

1. Sintering boat
2. Cover
3. Long side opening
4. Handle
5. Support
6. Sample

isothermal heating. Among the various support materials tried silica was found to yield the best results.

4.7.4 Sintering Procedure

In general, the processes following the actual screen printing of the layer can be classified into four operations (5), namely, paste coalescence, drying, burning off the organic binder and finally high temperature sintering.

i) Paste coalescence : a short period is needed directly after the printing for the sufficient levelling of the paste on the substrate. This time depends mainly on the paste composition (5).

ii) Drying process : This is a relatively low temperature process (70°-150°C). Drying is usually understood to be the elimination of moisture in the film. However, when solvents are used with the paste constituents (32) this process is also needed for solvent evaporation. In general, the drying time depends on the thickness of the paste and the method used for drying. It has been claimed that infra red is best for drying the printed layers (1) (4) since it penetrates deeply, causing bulk heating of the paste and hence ensures moisture and solvent free layers.

iii) Burning-off the organic binder : Efficent binder removal is very necessary for a high performance of the final layer since any retained carbon residue can cause pin holes or bubbling in the composition (1). This burn-off process occurs at 200°-350°. A flow of air is necessary to ensure rapid oxidation of the carbonaceous residue (5).

In the tube furnaces the burning of the binder is generally carried out as the first phase of the final firing process, so that in the belt furnace, for example, the temperature profile provides an adequate period at low temperature for effective binder removal.

iv) Final Sintering : At this stage the flux material melts, and the powder particles partially dissolve in it. A brief description of the role of the flux in sintering and the actual sintering theory will be given here.

a) Flux role Flux is a term used generally to describe a material which lowers the fusion point of another material for the purpose of obtaining more rapid liquifaction than obtained by temperature alone.

In this study $CdCl_2$ in the paste acts as a flux for the fusion of CdS material. $CdCl_2$ melts at a low temperature and the CdS dissolves in the molten $CdCl_2$. Then sintering process promotes growth of the powder particles by fusion and granule regrowth at temperatures well below the normal CdS sublimation point (7).

b) Sintering theory (Liquid Phase Sintering) The sintering enhancement of $CdCl_2$ is called liquid phase sintering (21). This refers to the sintering of a powder mixture of two or more components, of which at least one has a melting temperature lower than the others (43). The sintering temperature is then selected in such a manner that a liquid phase is formed in which the solid powder particles of the other components join together and are re-arranged by the action of the liquid phase (1).

Unless the liquid phase penetrates completely between solid particles, the presence of the liquid is not effective as a sintering aid (4).

An excellent general discussion of liquid phase sintering has been presented by W. Kingery (44) (45).

4.7.5 Sintering parameters

Standardizing the correct sintering procedure is very important in the interdependent processes of screen printing. There are a large number of parameters which have to be controlled to produce the best

screen printed layer. Included among others are the following, powder grain size and distribution (4) (44), purity of the powder (46), paste viscosity and mixing procedure (45), flux ratio (6), furnace type (4) and the confinement of the sintering ambient. The influence of most of these parameters upon the final performance of the screen printed layer will be described in Chapter 6.

4.8 Preparation of the screen printed CdS layers

The preparation procedure of the screen printed CdS layer involves five stages, viz: initial setting-up of the printing device, paste preparation, paste application, sintering procedure and finally cooling the screen printed layer.

i) Initial setting of the device Before printing commences, certain device parameters must be estimated to be approximately in the correct range. The most important parameters are the snap-off, squeegee angle of attack and squeegee pressure. It is impossible to give specific values for these parameters as the optimum values will depend upon such factors as paste viscosity, screen types, etc. (1). However useful starting points for snap-off distance would be in the range of .6-.8 mm. The squeegee angle for paste distribution was 45° while it was fixed at 55° for paste deposition. The squeegee pressure was adjusted with the help of an indicator on the squeegee. The criterion sought was a smooth movement of the squeegee travel.

ii) Paste preparation The CdS screen printed paste was prepared by mixing CdS powder with 10-15 wt% $CdCl_2$ (flux and dopant) and 35-45 vol% of propylene glycol (binder).

The paste constituents were mixed thoroughly as described in section 4.6.3-i to produce a smooth paste (section 4.6.3.-ii).

iii) Paste application A clean substrate was placed on the vacuum printing base. A controlled quantity of CdS paste was placed on the

clean screen just at the top of the substrate edge using a spatula. The paste was then spread with the distribution squeegee head to cover the image area of the substrate. The paste was then forced through the screen mesh with the required deposition angle. On removal of the squeegee, the screen regained its original position by its natural tension, leaving behind the printed paste on the substrate.

The initial settings of the printing parameters were then slightly adjusted to match the paste viscosity, so that a clean smooth and evenly distributed paste was always produced.

A simple printing procedure can be seen in fig. 4.3.

iv) Sintering procedure The printed CdS layer was allowed to settle for 10-15 minutes in a clean environment and was then dried for 1 hour at 120°-150°C in a small oven. The dried layer was then placed in the sintering envelope and inserted into the central zone of the tube furnace. The temperature of the furnace was set initially to 350°C for 15-30 minutes to burn off the binder and then the temperature was raised to a higher value between 620°-680°C for 60-120 minutes. The sintering rates used varied from 30% to 100% while flow rates between .04 L/min and .4 L/min were investigated.

v) Cooling procedure The sintered layer was allowed to cool naturally in the central zone until the temperature of the furnace reached 350°C then the layer was gradually moved towards the exit, and finally removed at room temperature.

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CHAPTER FIVE

PRELIMINARY STUDIES

5.1 Introduction

The purpose of this Chapter is to introduce some preliminary studies concerning the two major constituents of the CdS screen printing paste, namely, the CdS powder and the $CdCl_2$.

5.2 CdS Powder Studies

The significance of the starting CdS powder was mentioned in section 4.6.1. In this study various powders from different suppliers were tried and examined with a view to choosing the best one for the purpose. The following four powders were the major ones examined which represent a variety of features. The first one was supplied by General Electric Co. (U.S.A.). The second, was an old powder with unknown origin while the third one was supplied from B.D.H. Ltd. (U.K.). The fourth powder was from Haën Co. (Germany). For simplicity these powders will be referred to as powders A, B, C and D respectively.

In what follows a brief description is given of the various powders in relation to their major parameters i.e. purity, grain size and grain size distribution (sect. 4.6.1). The results of preliminary sintering trials will also be described.

5.2.1 Various Powder Types

i) Purity

Powder A : This is a luminescent grade powder which is known to be comparable to or slightly below that of semiconductor grade.

Powder B : This powder has been available in the Laboratory for a long time. A large density of absorbed impurities from the atmosphere is expected to exist.

Powder C : This powder was presublimed at 700°C in an Argon flow to remove volatile impurities. The resultant flow powder was of light yellow appearance.

Powder D : is a high purity 5N grade powder which is the powder usually described in the literature of screen printing CdS layers.

ii) Grain Size Consideration

Careful control of the grain size and distribution is essential to ensure dense compaction (1) of the screen printed layer. However, it is not always possible to obtain the proper grain size for screen printing applications. Some powders from the chemical suppliers are very fine (<.5 μm) so that they have to be calcined, then crushed to a suitable grain size (2). Other powders with very large grains have to be crushed to the desired size. The CdS powders examined in this study have the following grain size characteristics.

Powder A This powder has a blend of grain sizes which vary from 1-3 μm. This is near the optimum grain size of 1-2 μm reported as appropriate for screen printed CdS layer applications (3). The grain size distribution of this powder is shown in fig. 5.1 A.

Powder B The grain size of this powder was examined under the SEM, and found to be of the order of 60-80 μm (fig. 5.1 B). This is too large a size for screen printing application. Various techniques have been tried to obtain the appropriate grain size such as swing milling, manual grinding in a mortar and ball milling. The latter was found to be the most convenient method. The ball mill consists of three bottles with special ceramic balls for grinding purposes. Different milling times with different quantities of CdS powder have been tried. Figs. 5.1 C and D show the best grain size distribution obtained with 9 hours and 16 hours milling time respectively. The latter was chosen in this study. However, the appearance of non uniform grain size distribution

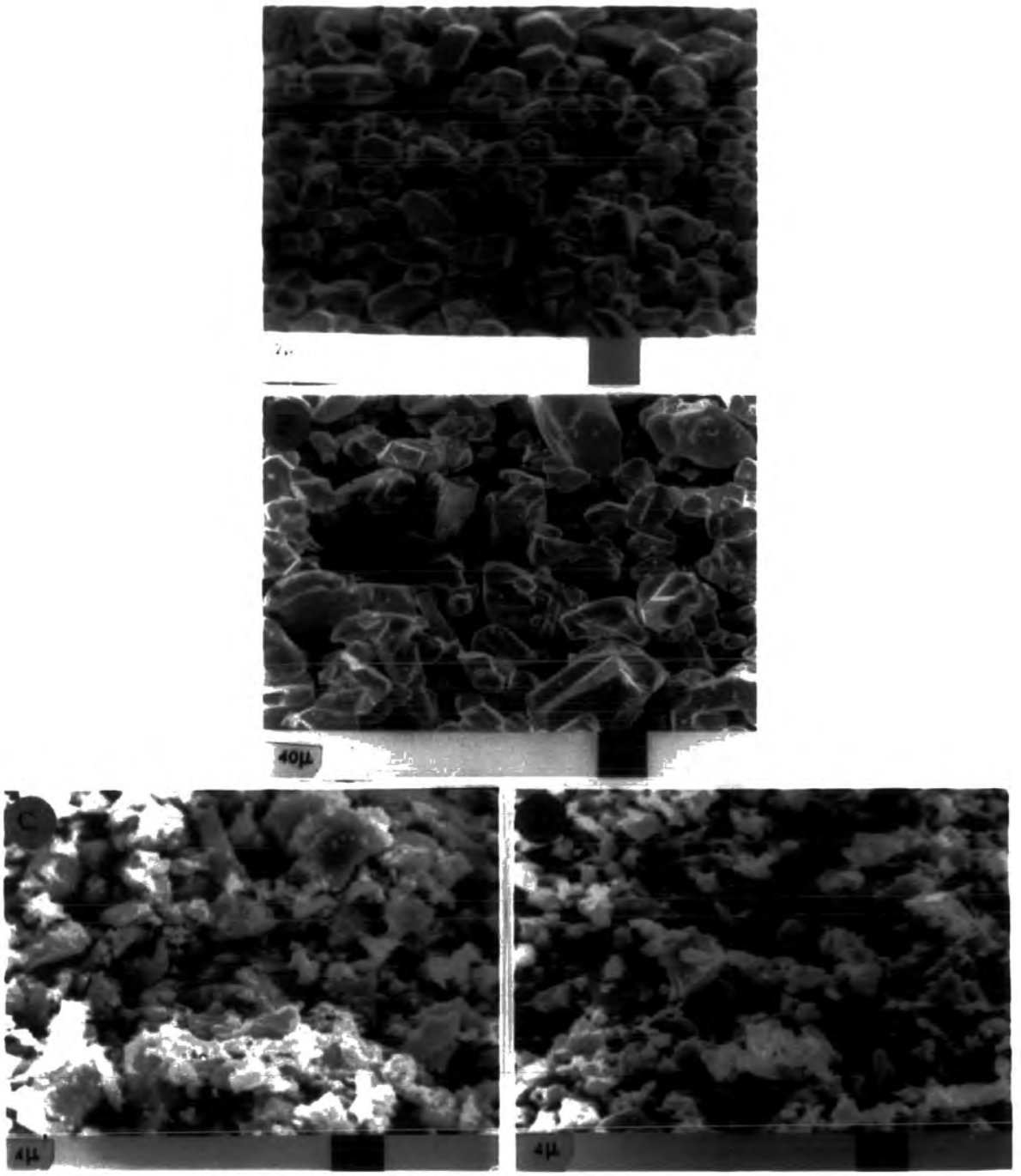

Fig 5.1 Grain size distribution for various powders.

A) Powder A (As received)

B) Powder B (As received)

C) Powder B (9 hrs. milling time)

D) Powder B (16 hrs. milling time)

is very evident with submicron grains mixed together with a large grain size. It should be noted that milling unavoidably introduces undesirable contaminants either from the milling balls or during the filtering procedure. In addition, a phase change could occur as a result of a milling action (4). This could introduce a further complication.

Powder C The resultant flow powder was in the form of large rods and platelets which needed to be crushed to a powder with small grain size. The same milling procedure used for powder B was followed again. By optimizing the milling time, a powder was obtained with a similar grain size distribution to powder B.

Powder D SEM examination of this powder revealed agglomerates of 200 μm size, each agglomerate containing grains ranging from 10-15 μm in size. After a short milling period, the agglomerates were broken, and the resultant powder had a good grain size distribution of 3-5 μm.

iii) Preliminary sintering trials

A preliminary sintering trial of screen printed layers utilizing the powders described above revealed an interesting phenomenon concerning powder D. This powder produced the best thixotropic paste when compared with the pastes prepared using the other powders. However, sintering the printed layer using powder D led to a peculiar appearance with black spots distributed all over the surface. An overall view of this feature is shown in fig. 5.2 A. The SEM observation of the black spots is shown in fig. 5.2 B and revealed faceted crystallites nucleated above the surface of the sintered layer. These were identified using EDAX as a simple cadmium crystallites (Figs. 5.3 A and B). It is clear that a major sulphur loss occurred in the faceted area and a non stoichiometric CdS layer had been produced.

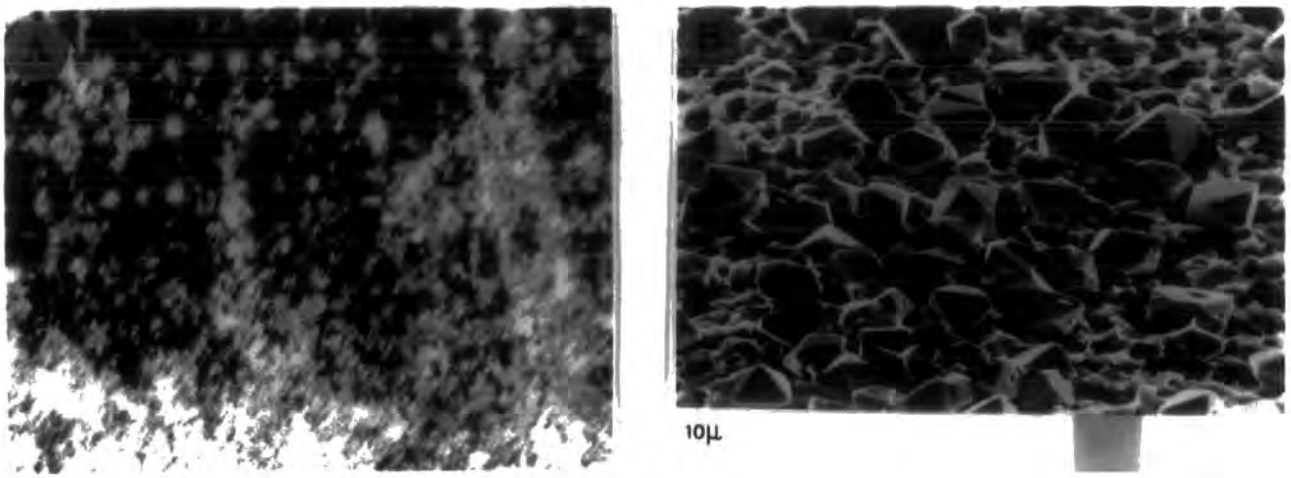

Fig. 5.2

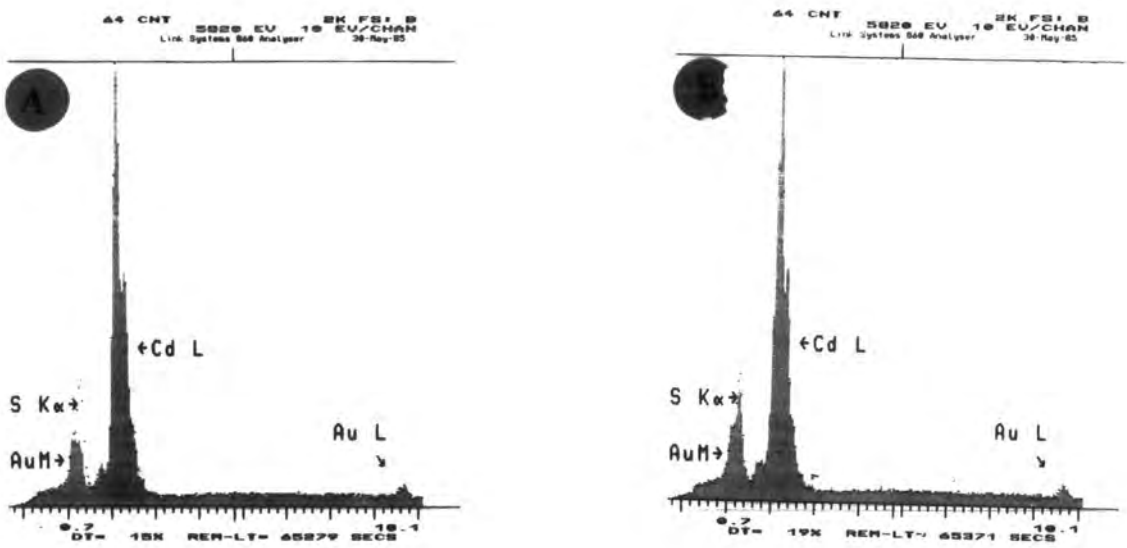

Fig. 5.3

Fig. 5.2 A : Optical micrograph of Powder D layer
B : SEM micrograph of Powder D layer

Fig 5.3 EDAX spectra of the above surface

A : Faceted particles
B : Large area

The layers sintered from powders A, B and C had normal stoichiometric surfaces with clear appearances. Facete only occurred when a very slow inert flow was used.

These results suggested that powder 'D' had a great tendency to loose S and to become non stoichiometric more rapidly than the other powders. As a result, and also in view of the high cost of the Haën powder, the present study was confined to powders A, B and C. Major studies of these powders will be described in Chapter 6.

5.2.2 Powder resistivity trials

In general, an intrinsic semiconductor may exhibit a relatively large change in electrical resistivity with pressure due to the change in band structure, which accompanies a compression of the lattice (5). Brentano et al (5) in their studies of the effect of pressure on powdered semiconductors used a vacuum press and the simple V-I measurements of resistance.

The same technique was used here. The resistivity of a powder can be changed by varying the impurity incorporated. Unfortunately, although a lot of work was done, the results were difficult to analyse and no true estimate of resistivity was obtained. Nevertheless, a good indication of the effect of impurities on CdS powder was obtained.

5.3 $CdCl_2$ Studies

5.3.1 Introduction

$CdCl_2$ has a dual function in the formation of the screen printed CdS layers as a donor (section 2.2.1-ii) and as a flux (section 4.7.4-iv-a). In discussing the fluxing and doping effects of $CdCl_2$ it is important to know whether the initial concentration of $CdCl_2$ present in the paste changes during the course of the sintering procedure. Such a change is very likely to take place because of the volatile nature of $CdCl_2$. It starts to volatilize at 400°C and is completely

volatilized at 600°C (6) (7). Since high temperatures are normally required in the fabrication of screen printed CdS layers, >600°C (see later) it is very crucial to stress that sufficient $CdCl_2$ must be available for fluxing and doping purposes and this imposes very restricted sintering conditions.

The purpose of the following sections is merely to monitor the behaviour of $CdCl_2$ with various sintering temperatures using EDAX, XRF and AAS techniques. The impact of this behaviour upon the performance of the CdS screen printed layers will be considered in the next Chapter.

5.3.2 EDAX Studies

The EDAX spectra from CdS layers using 10 wt % $CdCl_2$, as starting ratio, after three different sintering temperatures are shown in fig. 5.4. The maximum chlorine peaks are shown by the 300°C layer; this temperature is well below the initial volatilization temperature of $CdCl_2$ (i.e. 400°C). The height of the peak decreased significantly at 450°C and at 550°C the chlorine peak was not detected, which suggests that the remaining chlorine is less than 1 wt %.

5.3.3 XRF Studies

XRF was also employed to observe the variation of the quantity of chlorine remaining after different sintering temperatures. The residual amount is shown here by CPS (counts per second). The values obtained after sintering at 350°, 450° and 550°C were 1700, 1292 and 310 CPS respectively. For a layer sintered at 620°C it dropped to 230 CPS. Clearly the chlorine content decreased considerably at 550°C from its value at 450°C, while when the temperature was raised to 620° the value was only slightly reduced further which indicated that the significant reduction occurred between 450° and 550°C.

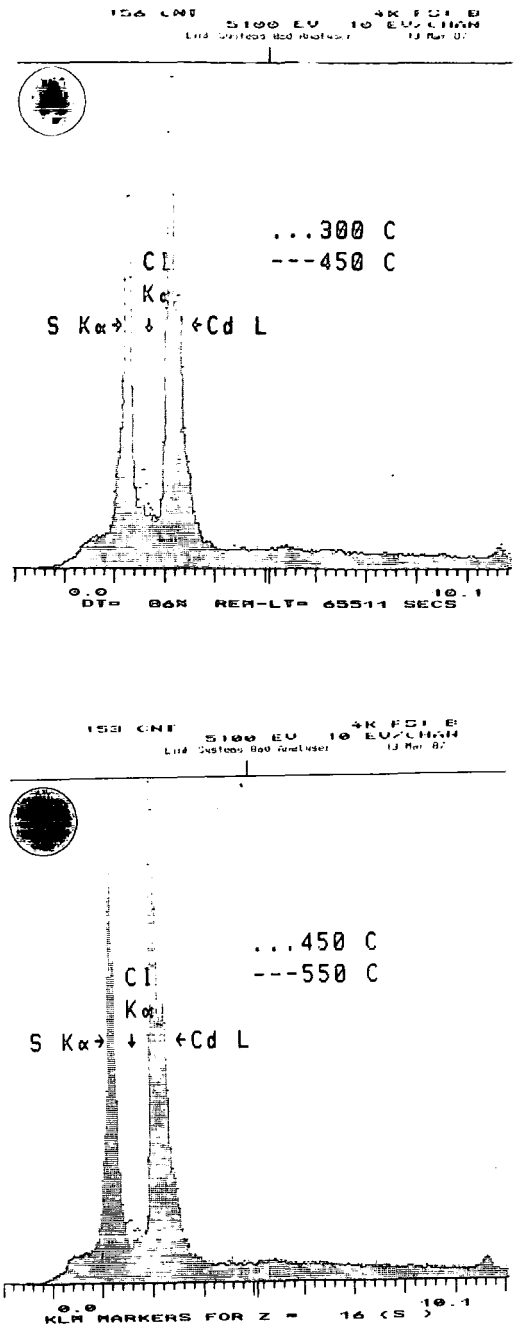

Fig. 5.4 EDAX spectra from CdS surface at different sintering temperature

A : Chlorine peaks at 300°and 450°C
B : Chlorine peaks at 450°and 550°C

5.3.4 AAS Studies

The amount of chlorine left in the sintered layers was also measured by atomic absorption spectroscopy. The equivalent values with those obtained from XRF analysis for the three temperatures investigated here; 350°, 450° and 550°C were 2.75, 2.21 and .27 wt% of chlorine. For a layer sintered at 620°C the value was less than .05 wt%.

For comparison purposes it is worth mentioning that Uda et al (3) detected more than 4% chlorine ions in a CdS layer sintered at 550° and at 620° the remaining amount was about 1.5%. These values are significantly higher than those measured here. Further discussion will be found in Chapter 6.

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CHAPTER SIX

CdS FILM CHARACTERIZATION

6.1 Introduction

The characterization of the screen printed CdS layers which will be presented in this chapter are concerned with the optimization of the parameters involved in the printing conditions discussed in Chapter 4. This is very important, because this optimization plays a significant role in the reproducibility of the electrical and structural behaviour of the final sintered layers.

This chapter will discuss the characterization of CdS layers deposited on both insulating glass (Soda Lime and Borosilicate), and conducting glass (SnO_2 coated glass). The preparation and sintering conditions were investigated mainly using Hall effect and Schottky barrier measurements.

There are two major purposes of this characterization.

1) To determine the preparational and sintering parameters which lead to the optimum electrical and structural behaviour of the CdS layer.
2) To assess the suitability of the sintered CdS layer for junction fabrication by choosing a simple device structure, namely a Schottky barrier diode, in order to avoid the complexity associated with the formation of a CdTe heterojunction which is the final goal.

SEM observations were made in parallel with Hall effect measurements in an attempt to correlate the morphology of the sintered layer with the electrical behaviour.

Resistivity data will be presented with Hall and Schottky data of donor concentration and carrier mobility. However, some aspects

related to the resistivity of the sintered layer will be given in Section 6.2.1.

Finally, EDAX, ESCA and XRD analysis will be presented as further means for the characterization of the sintered layer. This leads to a better understanding of the structure and composition of the layers.

It was hoped that a coherent relation between the optimum methods of preparation and sintering conditions, and the optimum CdS layer would be revealed with the aid of the characterization techniques used in this study.

6.2 Electrical Characterization

6.2.1 Resistivity Considerations

6.2.1.1 Introduction

Resistivity measurements give an initial characterization of the quality of the sintered layer. A low resistivity CdS layer is usually taken as an indication of a good sintered layer.

The as printed layers were normally of very high resistance ($>10^6 \Omega$ cm). The preparation and sintering conditions have to be closely controlled to produce a low resistivity layer. The resistivities of CdS layers deposited on insulating and conducting glass have been measured and compared with Hall and Schottky data, to draw a final conclusion of each specific condition under investigation.

6.2.1.2 Ohmic contact formation

Among the various methods described in Chapter 2 for achieving ohmic contact to CdS, alloying and evaporation methods were tried here. Alloyed indium contacts were fabricated by pressing small slices of 1.5 mm diameter wire on the CdS surface and then heating at 200°C for 10 minutes in an inert atmosphere. In the second method an indium contact was realised by evaporating indium dots 1 mm in diameter through a mask, and heating at 100°C for 10 minutes in an inert atmosphere.

Following a series of trials with both methods of contact fabrication, pressed and alloyed In contacts were utilised rather than the evaporated ones because the latter occasionally gave rise to non ohmic behaviour as shown in Fig. 6.1a. This is probably due to the formation of an InO_2 layer (1). In contrast, Figure 6.1b and Figure 6.1c show ohmic behaviour for pressed and alloyed contacts on low resistivity CdS layers sintered on conducting and insulating glass respectively. However, non ohmic behaviour was occasionally found for high resistivity layers probably because of the unsuitable work function of In for these layers (2). The choice of pressed/alloy contacts also avoided the complexity associated with evaporated In especially when considering the vast number of samples which were investigated in this study where it was necessary for the contact to be made in a reproducible manner which is essential for ohmic contacts (1).

It is worth mentioning here that although the ohmic behaviour shown for pressed/alloyed contacts is necessary, it is not a sufficient condition for neglecting contact resistance (3) (4), which is a very important parameter, which can affect the series resistance of the final fabricated solar cells.

6.2.1.3 Resistivity measurements

For CdS deposited onto conducting (SnO_2) glass, estimates of the resistivity were made by measuring the resistance between alloyed In and the SnO_2 back contact, whereas the Van der Pauw method was used to determine the resistivity of CdS deposited onto insulating glass, where the contacts were provided by pressing four small slices of 1.5 mm diameter indium wire on the periphery of the CdS sintered layer. All measurements were conducted at room temperature.

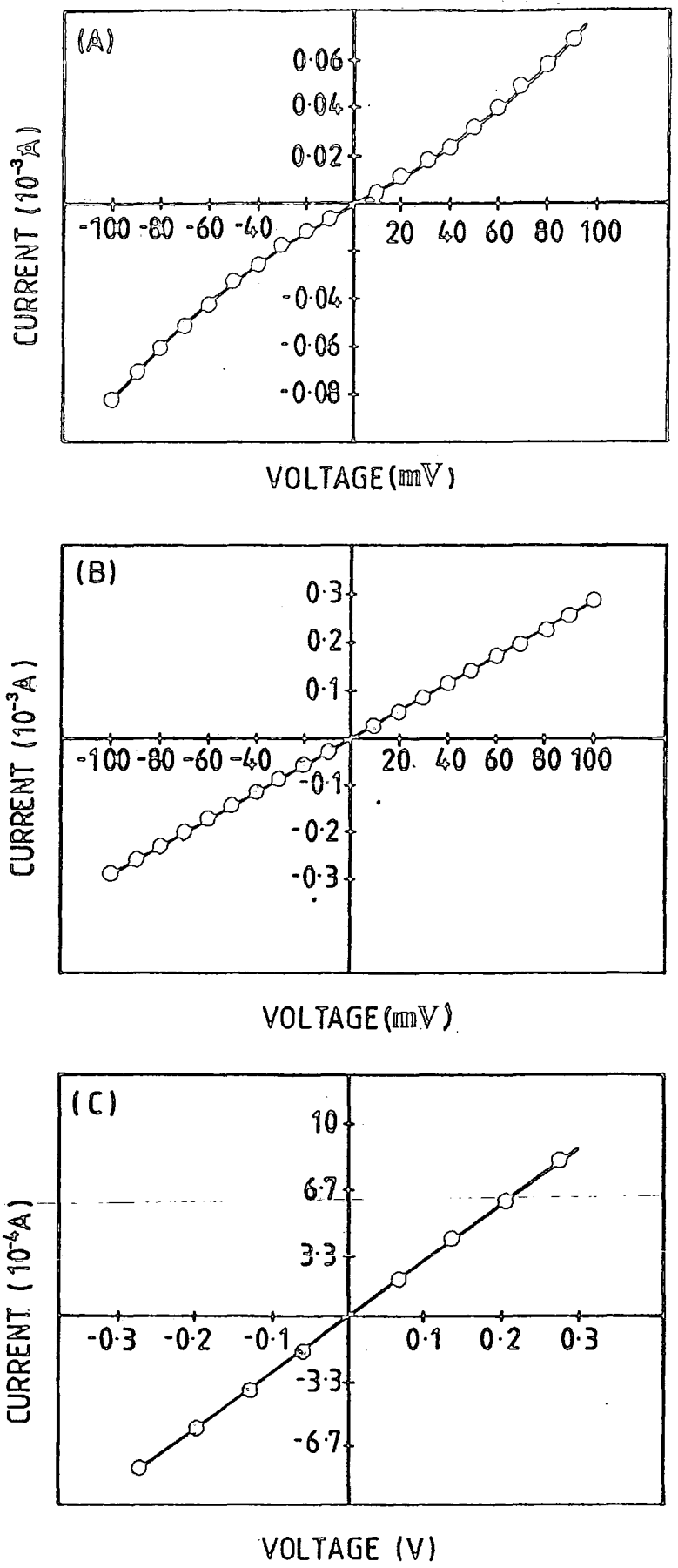


Fig. 6.1 Current-Voltage Characteristics

A) Evaporated Indium contact (SnO_2)

B) Pressed/alloyed Indium contact (SnO_2)

C) Pressed/alloyed Indium contact (soda lime) (Hall Plot)

6.2.2 Hall Effect Measurements

6.2.2.1 Introduction

Hall measurements were made using the Van der Pauw technique reviewed in Chapter 2. A description of the Hall apparatus was provided in Chapter 3. Ohmic contacts to the sample were made as described in section 6.2.1, and the ohmicity of the contacts was checked using Hall plots (Figure 6.1c).

Most of the following results are for CdS layers deposited on to soda lime glass, with reference to borosilicate glass in a few cases. SEM observations were made in parallel with Hall measurements as a diagnostic tool for monitoring various conditions of preparation and sintering processes in an attempt to correlate the morphology of the layer with its electrical behaviour.

6.2.2.2 Effect of preparation conditions

There are large numbers of preparational parameters to be optimized if the best screen printed CdS layer for junction fabrication is to be produced. The following are the most important: (i) powder choice, (ii) flux ratio and (iii) paste mixing.

(i) Powder Choice:

Close examination of the three powders under investigation described in Chapter 5 suggested the superiority of type A powder in satisfying various requirements for producing a good screen printed layer. This was largely due to its purity, optimum grain size, and grain size distribution.

Hall measurements on CdS layers utilizing these powders presented in Table 6.1 support the previous suggestions that CdS layers using powder 'A' produced the best electrical behaviour, i.e. lowest resistivity. The morphology of such a layer, Figure 6.2a, also has the best microstructure with appreciable grain growth and a compact

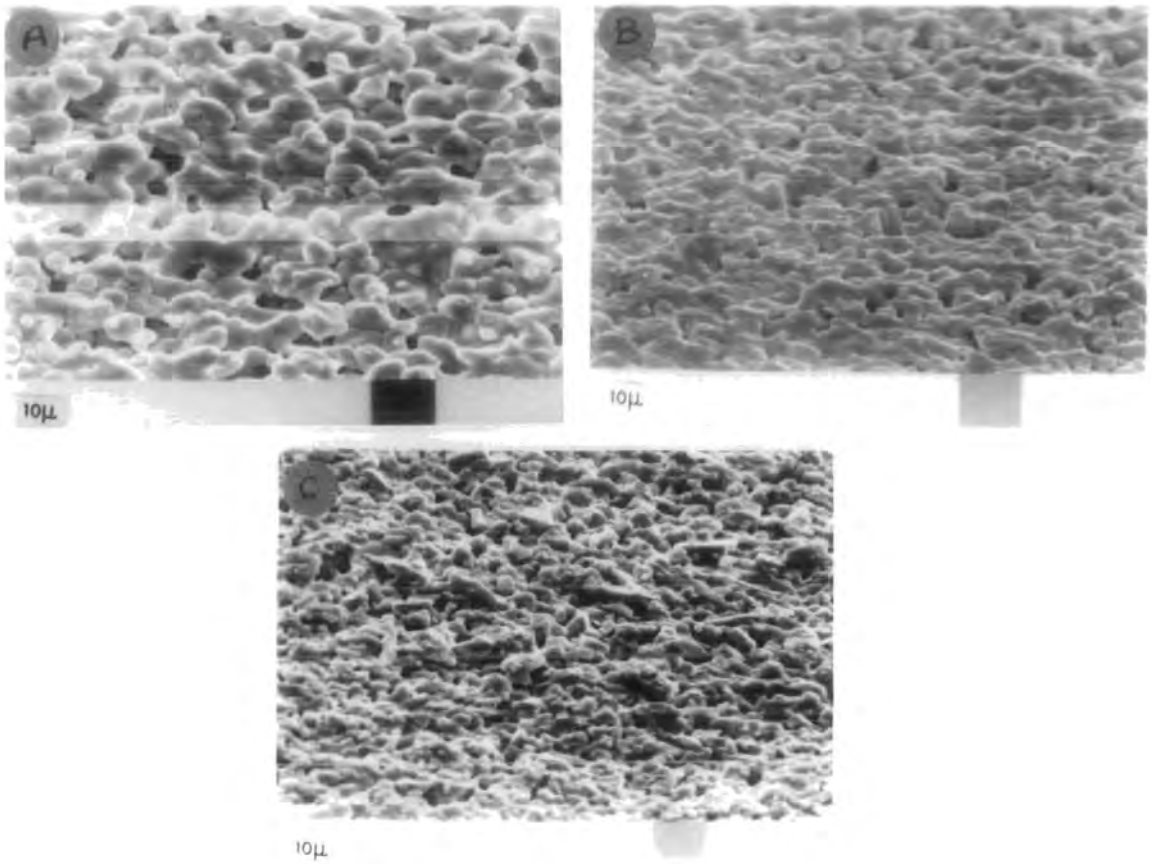
pattern. The electrical behaviour of 'type B' and 'type C' powders layers was very poor with peculiar morphology as shown in Figure 6.2b and 6.2c. Although appreciable surface melting had occurred with type B powder, nodules and angular grains were the general features. Type C powder had a porous structure, with no grain growth, and an agglomeration of grains with some very distinct straight flat edged grains. The morphology of type B and C powders reveals strong inhomogeneties which can have an adverse influence on overall device performance as shown in Table 6.1.

(ii) Flux ($CdCl_2$) ratio

$CdCl_2$ has a dual function in the fabrication of the screen printed layer; i.e. as a flux and as a donor. Various aspects of the use of this material were discussed in Chapter 5. It is very important to use the correct ratio of $CdCl_2$ in the printing paste. Two different ratios were studied and Table 6.2 shows the Hall data of two CdS layers with 10 wt % and 7 wt % $CdCl_2$. It is clear that this layer with 10 wt % $CdCl_2$ gave the better electrical behaviour with a good compact structure with an average grain size of (8 - 10 μm). The layer with 7 wt % $CdCl_2$ had a porous structure with an average grain size of (2 - 4 μm). Typical micrographs of the two layers are shown in Figure 6.3a and Figure 6.3b. Higher $CdCl_2$ contents were not studied here. However, some trials will be mentioned later in section 6.2.3.2.

(iii) Paste mixing

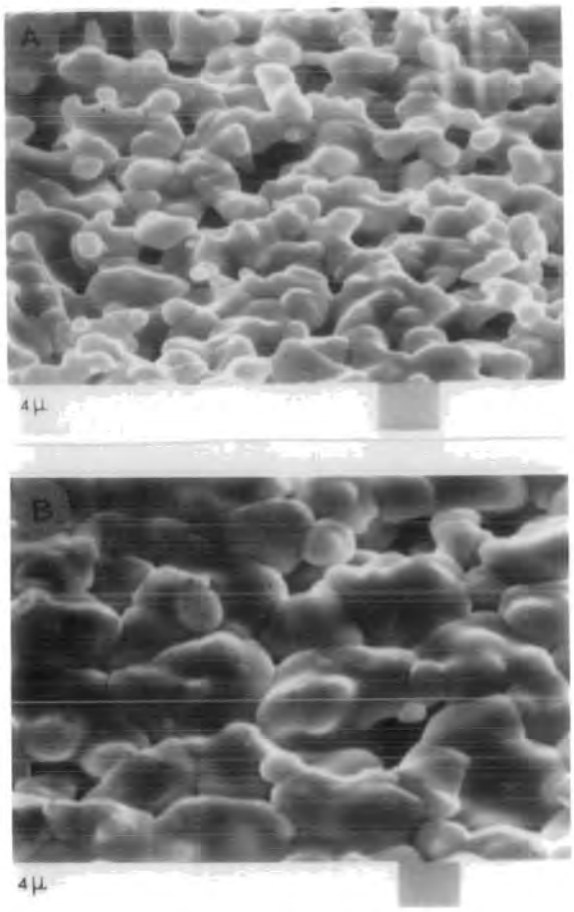
The significance of proper mixing of the constituents of the CdS paste can be clearly seen from the Hall data presented in Table 6.3. A major difference in resistivity, carrier concentration and mobility between an optimum mixed paste and a non optimum paste is apparent. Figure 6.4a shows a dry printed CdS layer of a well mixed paste. The layer has a powdery structure as expected before sintering, with narrow



Micro-graph	Condition	ρ (Ωcm)	n (cm^{-3})	$\mu(cm^2v^{-1}s^{-1})$
A	Type A powder	3	$8.2\ 10^{16}$	16
B	Type B powder	22	$2.9\ 10^{15}$	95
C	Type C powder	27.1	$7.85\ 10^{15}$	29.4

Fig. 6.2 SEM micrographs of CdS surfaces of the three powder investigated

Table 6.1 Hall measurements of the above films.



Migro-graph	Flux ratio	ρ(Ωcm)	n (cm^{-3})	$\mu(cm^2v^{-1}s^{-1})$
A	7 %	16.7	6.18 10^{16}	6.04
B	10%	3	8.2 10^{16}	16

Fig. 6.3 SEM micrographs of CdS surfaces using different ratio of flux under optimum conditions.

Table 6.2 Hall measurements of the above films.

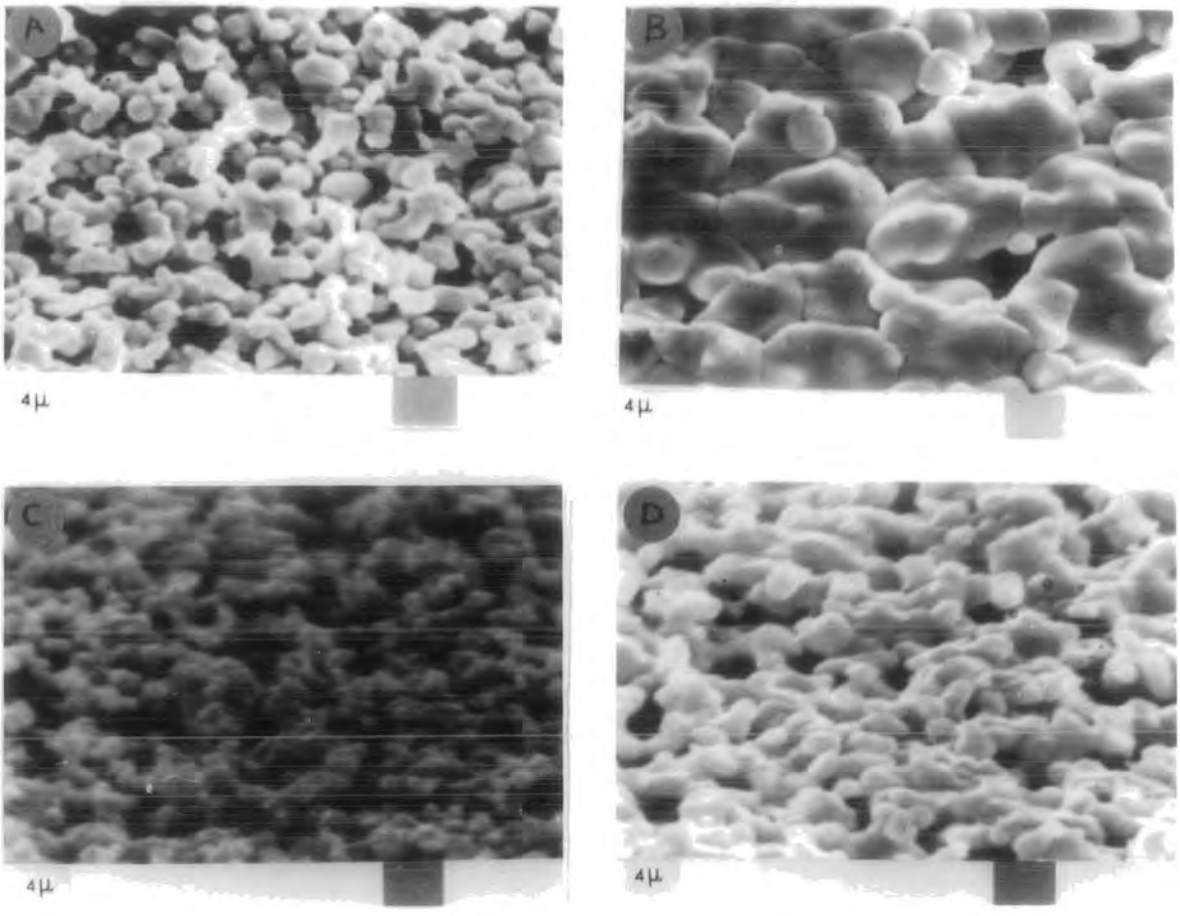
grain size distribution. These conditions aid sintering at high temperature (5) Figure 6.4c shows a dry printed CdS layer of a non optimum mixed paste with an agglomerated microstructure which affects the sintering and compactness of the grains. The results of sintering the two dry layers are shown in Figure 6.4b and Figure 6.4d. A dramatic change in the overall morphology of the two sintered layers is apparent and there is a good correlation between the morphology and the electrical behaviour. The good electrical behaviour in a well-mixed paste sintered layer is associated with a tightly packed structure with few voids and appreciable grain growth.

6.2.2.3 Discussion

In the following section an attempt is made to give an explanation for the above results.

Powder choice : The optimum choice of CdS powder depends mainly on three parameters: purity, grain size and grain size distribution. Chapter 5 gives a description of each powder type in relation to these parameters. Type A powder with its relative purity and optimum grain size of 3 µm with optimum grain size distribution (Chapter 5, Fig. 5.1A) produced the best sintered layers with good compaction and electrical behaviour.

Type B powder has two main problems; i) a large contamination and ii) a non uniform grain size disttribution (Fig. 5.1D , Chapter 5). The presence of foreign contamination could be very harmful since it can collect preferentially on grain boundaries by diffusion as the sintering temperature is increased (6), and subsequently it may inhibit grain boundary migration and hence influence grain growth (7) (8). Moreover, the high density of morphological defects, such as coarse grain standing out from the paste, voids and grain boundaries may modify the electrical behaviour either by acting as scattering centers



Micrograph	Description	ρ (Ω cm)	n (cm^{-3})	μ($cm^2 v^{-1} s^{-1}$)
A	Dry sample optimum mixing	-	-	-
B	Sample A (After sintering)	3	$8.2\ 10^{16}$	16
C	Dry sample non optimum mixing	-	-	-
D	Sample C (After sintering)	96	$2.5\ 10^{15}$	35

Fig. 6.4 SEM micrographs of CdS surfaces under optimum and non optimum paste mixing

Table 6.3 Hall measurement of the above films.

or by causing chemical inhomogenity through the segregation of impurities (9).

Type C powder, which is an Optran grade powder was reported to be an optimum choice for thermal evaporated CdS layers (10). Unfortunately, it was not a good choice for screen printed CdS layers. This is probably due to the large excess of sulphur in the starting material (Chapter 5). It is known that some sulphur evaporated preferentially in the sintering process due to its higher vapour pressure leading to a non-stoichiometric layer. These vacancies supply free electrons when ionized (12) resulting in low resistivity layers. Although this is what should normally be expected, it is possible that the sintering temperature was not high enough to remove all the excess sulphur from type (C) CdS layers, or it just removed the excess S without creating native S vacancies and thus resulted in a highly resistive layer. The poor morphology of this layer is probably due to the grain size distribution of the starting powder (see Chapter 5, Fig. 5.1D). Powders B and C have undesirable grain size distributions with some large particles reducing the fluxing effect of the $CdCl_2$.

Flux ($CdCl_2$) ratio : $CdCl_2$ is an important constituent of the CdS screen printed paste. A controlled amount of $CdCl_2$ has to be added to provide a low sintering temperature and also to act as a donor source (Chapter 5). The sample which contains 10 wt % of $CdCl_2$ produced the better morphology and electrical behaviour. This ratio was also reported by others (11) (13) as the optimum ratio for screen printed CdS layers. When the ratio was decreased to 7 wt % it resulted in a porous structure with smaller grain size and poorer electrical behaviour. The higher resistivity and lower mobility were also probably due to the decrease in the average grain size (11) (14). The carrier concentrations of both sintered layers using 10 wt % and 7 wt %

were nearly the same (8.2×10^{16} cm^{-3} and 6.18×10^{16} cm^{-3}). This agrees with H.G. Yang et al (11) who found an increase in the carrier concentration with increasing quantities of $CdCl_2$ from 0 wt % to 6 wt % which then saturated with more $CdCl_2$. Nonetheless further improvement in morphology and conductivity would probably require a somewhat higher ratio of $CdCl_2$ to give a molten flux content which would lead to complete fusing of the CdS grains and hence help grain growth as described in Chapter 4.

Paste mixing : Although the most important single parameter in the whole screen printing process is proper paste mixing (15), no previous effort to investigate the significance of this parameter has been reported in the literature. It is very important that the paste mixing process be carried out with great care and standardization to ensure satisfactory and reproducible results, otherwise, very misleading results can occur. The main concern for the moment is the $CdCl_2$ part of the paste. The significance of other paste constituents is discussed in Chapter 4. However, their contribution can be omitted at this point since the same powder (type A) with the same binder type and ratio was used for both optimum mixed and non optimum mixed paste. The compact structure with appreciable grain growth, together with the good electrical behaviour achieved with an optimum mixing is an indication of the correct distribution of $CdCl_2$ particles in the paste, where it is in intimate contact with the other constituents. This feature is very important in avoiding the direct evaporation of $CdCl_2$ at the early stages of sintering. In contrast, the porous structure with small grain size obtained with non optimum mixing is an indication of a loss of $CdCl_2$. This is probably because $CdCl_2$ particles will be loosely bonded with other constituents of the paste and so will be preferentially lost at the early stages of sintering before their real

function has started. The amount of $CdCl_2$ remaining would be much smaller than the starting ratio. Bearing in mind that $CdCl_2$ is used as a flux and as a donor this explains the poor morphological and electrical behaviour of the "non optimum mixed" CdS layer. It is important to stress here that non proper mixing will cancel the effect of the optimization of all other fabrication parameters to a very large extent.

6.2.2.4 Conclusion

The investigation of the preparational conditions described above suggested the following as optimum conditions for preparing the best screen printed CdS layer:

i using pure CdS powder with an average grain size of 3 μm.

ii using 10 wt % $CdCl_2$ as a flux and a donor source.

iii precise control of mixing procedure is strongly advisable to ensure correct distribution of constituents.

6.2.2.5 Effect of sintering conditions

As well as the optimization of the preparational parameters described in section 6.2.2.2, there are also a large number of sintering parameters to be optimized to yield the most reproducible CdS layers for solar cell fabrication. The most important parameters to be optimized fall into three groups: Firstly, parameters related to the sintering ambient which involve sintering rate, sintering envelope configuration and flow rate. Secondly, parameters related to the sintering temperature and finally post sintering annealing parameters.

The discussion of the first three sintering parameters will be referred to in Figure 6.4b and Table 6.3b as representative of an ideal CdS layer utilizing optimum parameters for its fabrication. This is justified since it is assumed that in investigating the significance of any parameter, all other parameters are chosen to achieve optimum

conditions. This assumption is necessary to avoid interrelated effects. The optimum sintering conditions were investigated and established for the sintering ambient parameters and the presentation will concentrate on the extreme cases to show their influence on the morphological and electrical behaviour. Using Figure 6.4b and Table 6.3b as examples of optimum conditions will also help avoid displaying too many micrographs.

i) Sintering rate

From the fact that, $CdCl_2$ volatilizes above 400°C while at 600°C the volatilization is complete, it is obvious that the results are sensitive to the time spent totally from 400° to 600°, since the full utilization of the effects of $CdCl_2$ should occur during this period. Some aspects related to the sintering rate in the tube furnace used in this study were described in Chapter 4. Figure 6.5a and Figure 6.5b reveal the microstructures of two sintered layers using 30% and 100% sintering rates respectively, while Table 6.4a-b shows the corresponding Hall data. Figure 6.4b is representative of the microstructure of a CdS layer using 50% sintering rate, with the Hall data shown in Table 6.3b. Figure 6.6a is a graphical representation of the data presented in Tables 6.4a, 6.4b and 6.3b. The superiority of using a 50% sintering rate in producing the best morphological and electrical behaviour is clearly seen.

ii) Sintering envelope configuration

Because of the volatile nature of $CdCl_2$ it was necessary to impose a restriction on the sintering ambient in order to control the evaporation of $CdCl_2$. Figures 6.5c-d show the microstructures of two CdS layers sintered in open and closed boats respectively. The associated Hall data is shown in Table 6.4c-d. Figure 6.4b is representative of the microstructure of a CdS layer sintered in an

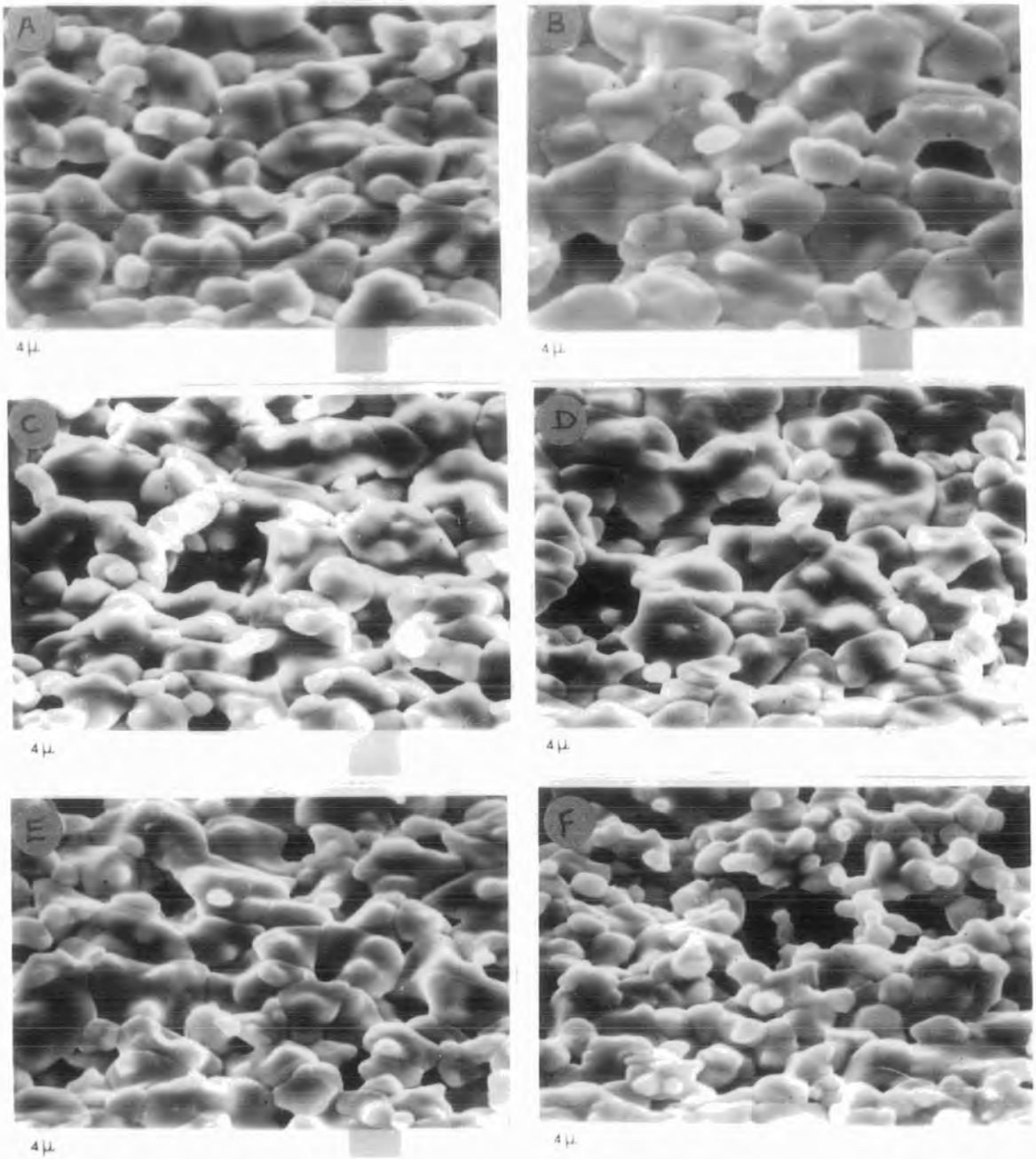
open boat with the corresponding Hall data shown in Table 6.3b. Figure 6.6b is a graphical representation of the data shown in Tables 6.4c, 6.4d and 6.3b the superiority of using an open boat configuration is clearly apparent in producing a good morphological and electrical behaviour of a sintered CdS layer.

iii) Flow rate

Again, the significance of this parameter is related to the $CdCl_2$ function in the sintering process. With a very slow flow rate faceting will occur and there is a strong possibility of CdO formation. With a very fast flow rate a very soft sintered layer is produced. Both extremes were not successful for contact formation and are simply included to illustrate the importance of controlling the flow rate. Figures 6.5e-f show the microstructures of two sintered CdS layers using flow rates ·04 L/min and ·4 L/min respectively. The corresponding Hall data are shown in Table 6.4e-f. Figure 6.4b represents the microstructure of a sintered CdS layer using .1 L/min with its Hall data shown in Table 6.3b. Figure 6.6c is a graphical representation of the data shown in Tables 6.4e, 6.4f and 6.3b. Although there were some similarities in the electrical behaviour of the three layers, the best morphological and electrical combination was achieved for a CdS layer using .1 L/min flow rate.

iv) Sintering temperature and duration

Trials have been made to observe the changes in the morphology and electrical performance by progressively increasing the sintering temperature and duration, in order to find the conditions to produce CdS layers with the best morphological and electrical behaviour. CdS layers deposited onto soda lime and borosilicate substrates have been investigated.



Conditions	Micro-graph	Change	ρ (Ωcm)	n (cm^{-3})	$\mu(cm^2v^{-1}s^{-1})$
Sintering rate	A	30%	6.2	3.4×10^{15}	193
	B	100%	4.7	8.4×10^{15}	104
Boat Con-figuration	C	Open boat	6.67	5.6×10^{16}	11
	D	Covered boat	16.67	2.2×10^{15}	111
Flow rate	E	.04L/min	2.57	3×10^{16}	53.8
	F	.4 L/min	10.6	2.3×10^{16}	16

Fig. 6.5 SEM micrographs of CdS surfaces under various sintering conditions
Table 6.4 Hall measurements of the above films

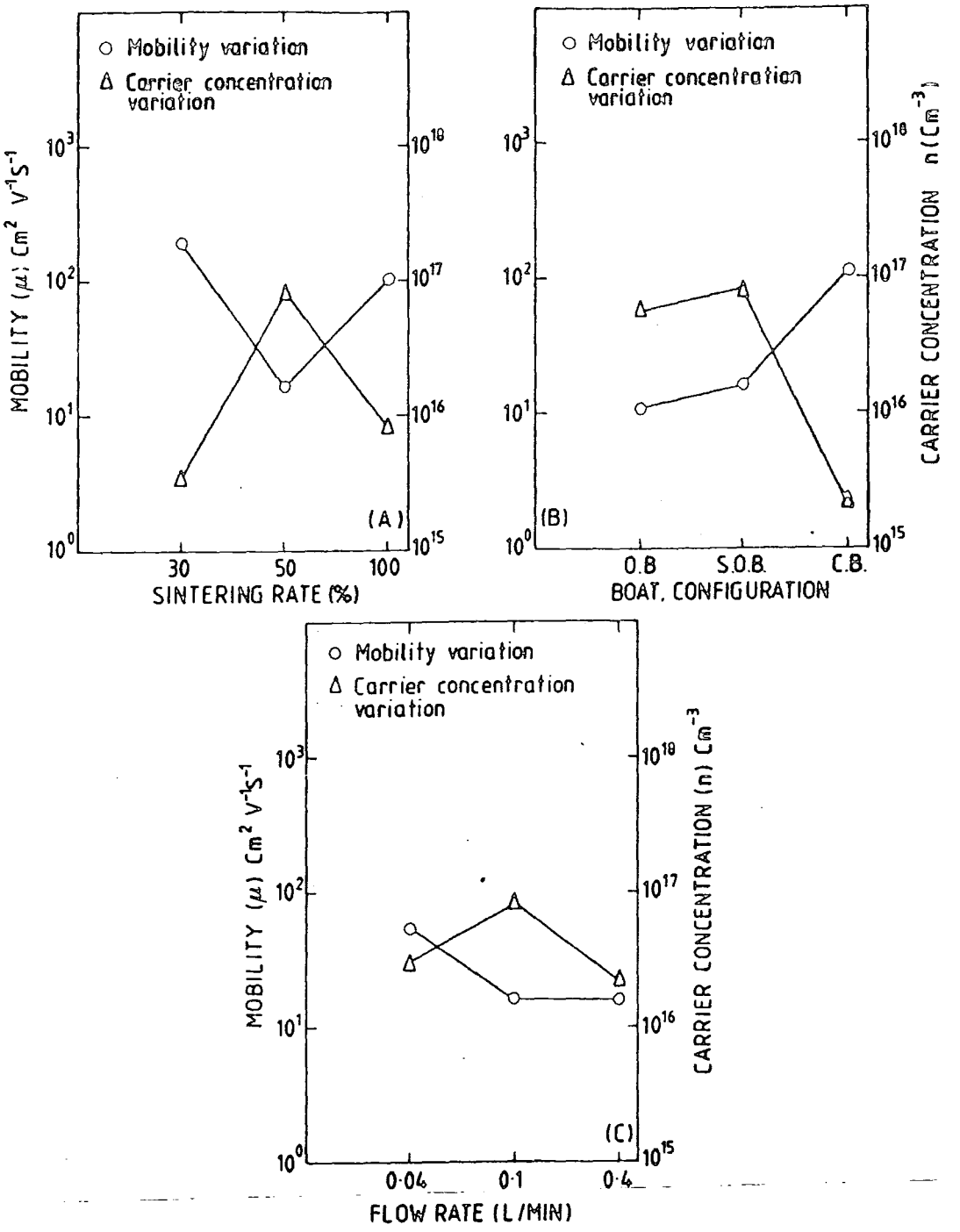


Fig. 6.6 : Variation of mobility and carrier concentration with

A Sintering rate

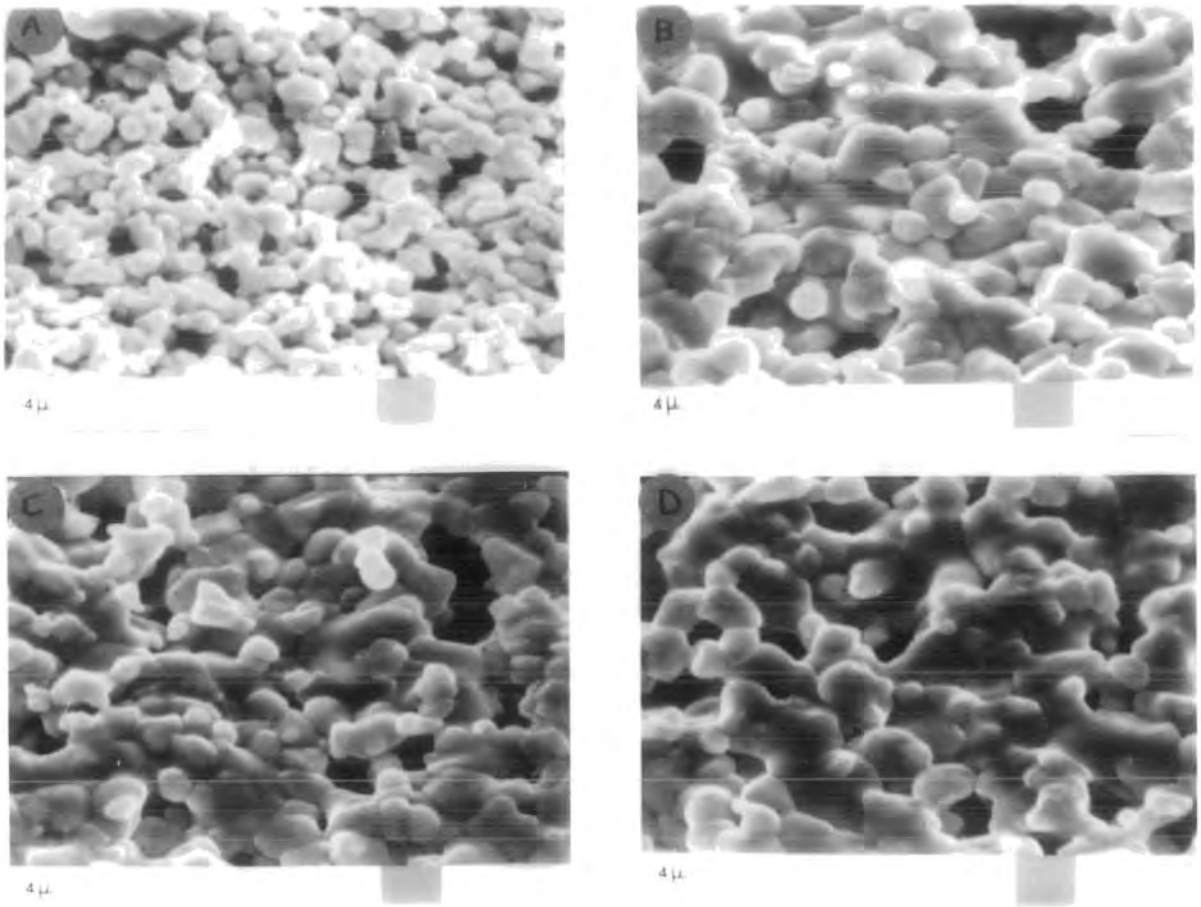
B Boat configuation

C Flow rate

a) Soda Lime substrate trials

The morphological behaviour of screen printed layers as a function of various sintering temperatures is shown in Figure 6.7. The dry printed layer before sintering is shown in Figure 6.7a. The micrograph reveals a soft powdery structure where the grains are loosely bonded and held mechanically by the binder. The resistivity of this layer was very high ($>10^6 \Omega$ cm), and therefore it was very difficult to obtain Hall data. Figures 6.7b,c and d show the morphological changes which occurred when the temperature reached 550°, 580° and 620° respectively, where it was held for 5 minutes duration at each temperature. Although significant grain growth occurred, the structures were still very disordered with non uniform grain size. Hall measurements are presented in Table 6.5 and show a sharp reduction in resistivity with a corresponding marked increase in carrier concentration and abnormally high mobility values. A graphical representation is shown in Figure 6.11A.

When the time of sintering at 620° was increased to 60 minutes a significant improvement in the morphology occurred as shown in Figure 6.8a. The corresponding Hall data are shown in Table 6.6a. Although, preliminary tests on soda lime glass suggested a maximum usable temperature of 620° for this type of glass, a further trial was made to investigate the effect of heating at higher temperature. Figure 6.8b shows the microstructure of a CdS layer sintered at 650°. It is clear that it has an improved morphology with appreciable grain growth. However, some secondary particles could be seen above the surface, and the Hall data in Table 6.8b indicate a reduced carrier concentration with abnormally high mobility values. Sintering temperatures higher than 650° were not tried. In an attempt to improve the performance further the annealing time was increased from 60 minutes to 90 minutes.



Micrograph	Sintering temp.(5 min)	ρ (Ω cm)	n (cm^{-3})	$\mu(cm^2 v^{-1} s^{-1})$
A	120°	-	-	-
B	550°	22.3	$1.2 \quad 10^{14}$	1550
C	580°	6.3	$1.52 \quad 10^{16}$	43.29
D	620°	2.1	$2.97 \quad 10^{16}$	66.88

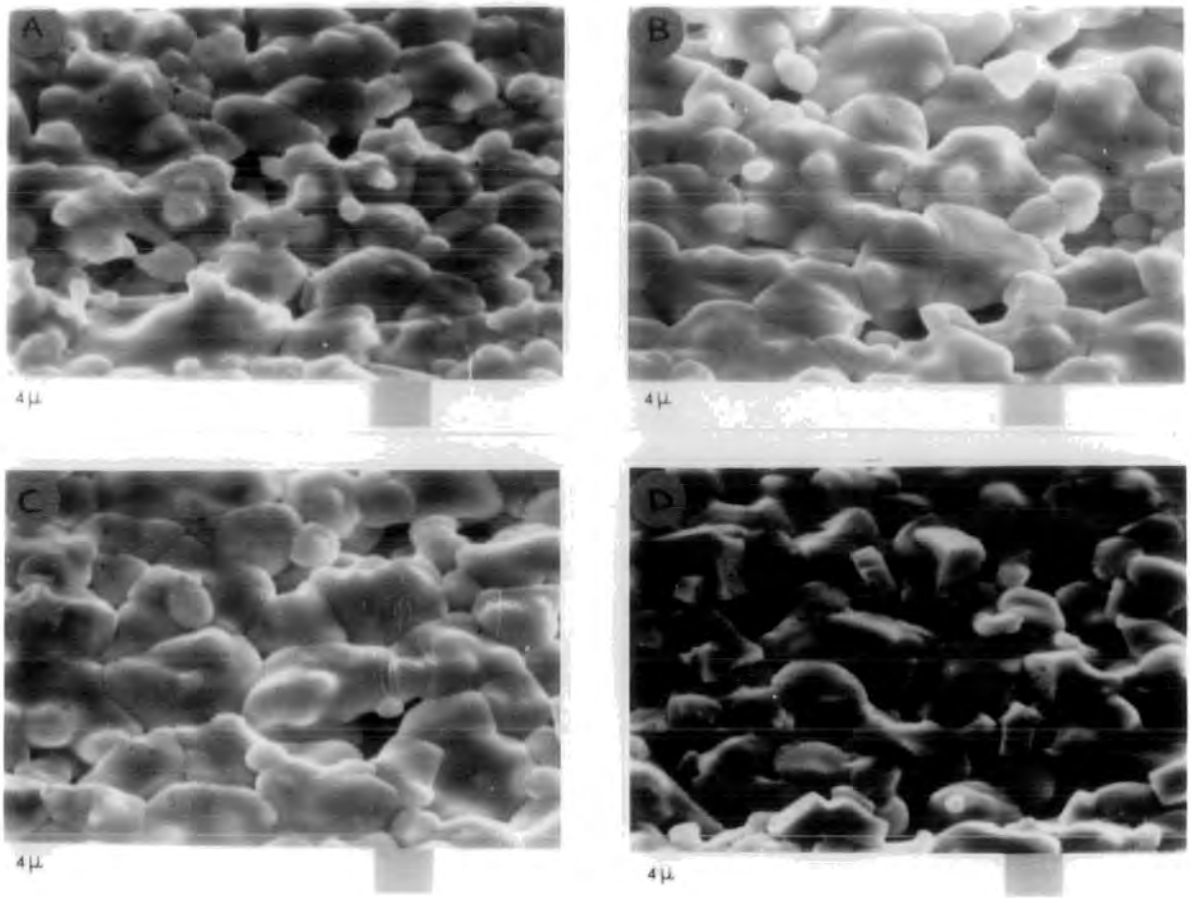
Fig. 6.7 Effect of sintering temperature on CdS morphology.

Table 6.5 Hall measurement of the above films.

Figure 6.8c shows the microstructure of a CdS layer sintered at 620° for 90 minutes. A reasonably dense and compact grain structure with few holes and a good grain growth was achieved with these conditions. The associated Hall data in Table 6.6c indicate good electrical behaviour. When the duration of sintering was increased further to 120° minute, the morphology was distorted by the appearance of sharp cubic particles emerging from the grain boundaries and nucleating above the surface as shown in Figure 6.8d. Hall data in Table 6.6d indicate a major deterioration in the electrical behaviour. It appears therefore that the optimum temperature and duration for sintering CdS layers deposited on soda lime glass is 620° for 90 minutes.

b) Borosilicate substrate trials

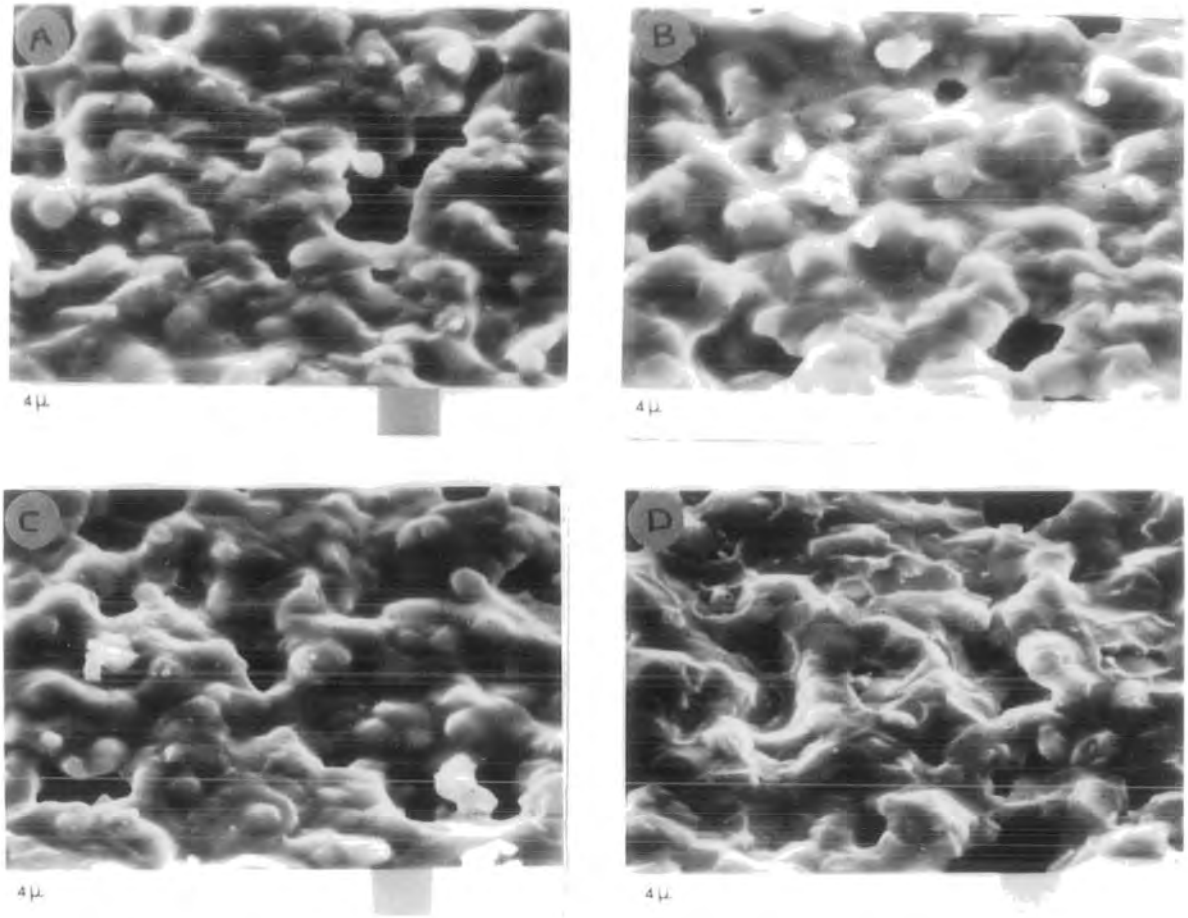
The investigation of screen printed layers on borosilicate substrates was made to examine the high temperature effect. Although the manufacturers information sheet did not recommend high temperature application, it was hoped that this study would illustrate some useful features about the value of the substrate. Figures 6.9a-b show the microstructure of CdS layers sintered at 620° for 60 minutes and 90 minutes respectively, while Figures 6.9c-d are for two CdS layers sintered at 680° for 20 minutes and 60 minutes respectively. The morphologies shown in Figure 6.9 contain a dense and transgranular structure which make it difficult to estimate the grain size. Also there is an apparent segregation of an unknown secondary phase visible along the grain boundaries, very clearly shown at high temperature. The resistivities and carrier concentrations (Table 6.7) are better than those obtained under the same conditions with CdS layers sintered on soda lime glass. However, the rather high mobilities make the results difficult to interpret at this stage. Finally, for more



Micro-graph	Sintering temp.	Time	ρ (Ωcm)	n (cm^{-3})	μ ($cm^2v^{-1}s^{-1}$)
A	620	60	5.2	6.88 10^{16}	11.55
B	650	60	3.12	8.22 10^{15}	161.45
C	620	90	3	8.2 10^{16}	16
D	620	120	31.3	2.6 10^{15}	52.12

Fig. 6.8 SEM micrographs of CdS surfaces under various sintering temperature and duration using Soda Lime glass.

Table 6.6 Hall measurement of the above films.



Micro-graph	Sintering temp.	Time (minute)	ρ (Ωcm)	n(cm^{-3})	μ($cm^2v^{-1}s^{-1}$)
A	620	60	.68	1.78 10^{17}	33.9
B	620	90	.44	2.5 10^{17}	38
C	680	20	1.18	1.33 10^{17}	70
D	680	60	5.56	9.1 10^{15}	82.27

Fig. 6.9 SEM micrographs of CdS surfaces under various sintering temp. and duration using Borosilicate glass.

Table 6.7 Hall measurement of the above films.

clarification a graphical representation of the data presented in Tables 6.6 and 6.7 is given in Figures 6.11 b and c.

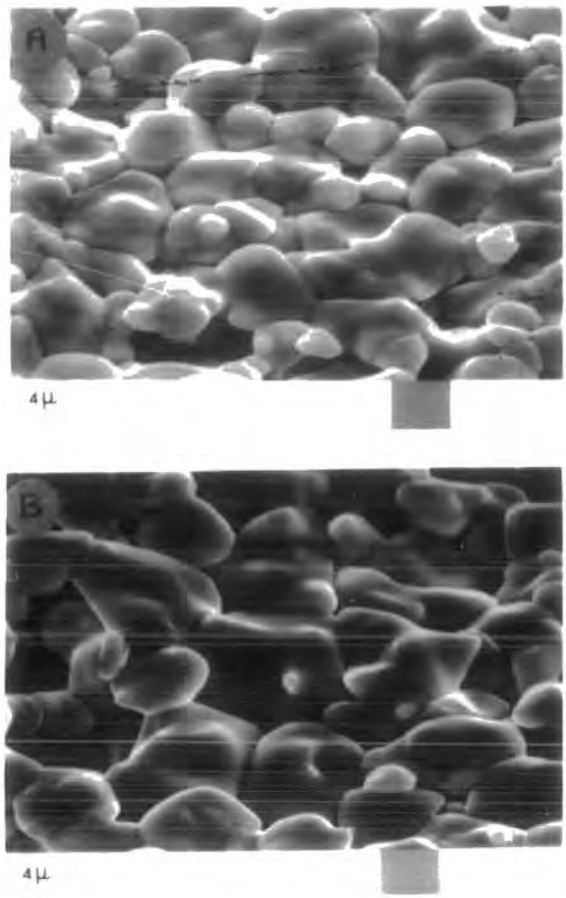
v) Post sintering annealing

To investigate the effects of post sintering treatment on the CdS layers two similar layer sintered at 620° for 60 minutes (Figure 6.8a) were annealed in hydrogen and vacuum respectively at 350°. Figure 6.10 shows the significant improvement in the morphology of both annealed layers in comparison with the starting layer in Figure 6.8a. A very good compact grain structure resulted with few voids, and it would seem that vacuum annealing yielded a better grain growth. The electrical properties of the annealed layers are presented in Table 6.8 together with those of a non-annealed layer for comparison purposes. It is interesting to note that although the resistivity decreased slightly the carrier concentration also decreased but both mobility values became very large. These results are shown graphically in Figure 6.11d.

6.2.2.6 Discussion

Sintering rate : It was mentioned in Chapter 4 that the sintering rates used in the study are actually representative of the maximum power which gave different sintering rates. Thus 30% maximum power (M.P.) delivered to the furnace was equivalent to a sintering rate of 15°C per minute. 50% M.P. was equivalent to 28°C per minute, whereas 100% M.P. was equivalent to 44°C per minute. However, for simplicity these maximum power figures were used to represent the sintering rate term.

The control of sintering rate is more important than that of the peak temperature (17) this becomes clear when it is recognized that $CdCl_2$ starts to volatilize at 400° and volatilizes completely at 600°. This makes the period that the sample remains between 400°C and 600°C very critical. With the optimum 50% sintering rate, this time was 7 minutes as estimated from Figure 4.9 (Chapter 4). It was found to be



Micro-graph	Post sinter-ing ambient	ρ(Ωcm)	n(cm^{-3})	μ($cm^2V^{-1}s^{-1}$)
A	Hydrogen	.92	$3.6 \quad 10^{16}$	120
B	Vac uum	2.6	$1.84 \quad 10^{16}$	128.78
Fig. 6.8A	Sample without treatment	5.2	$6.88 \quad 10^{16}$	11.55

Fig. 6.10 SEM micrographs of CdS surfaces under hydrogen and va cuum post sintering treatment for an optimum film.

Table 6.8 Hall measurement of the above films.

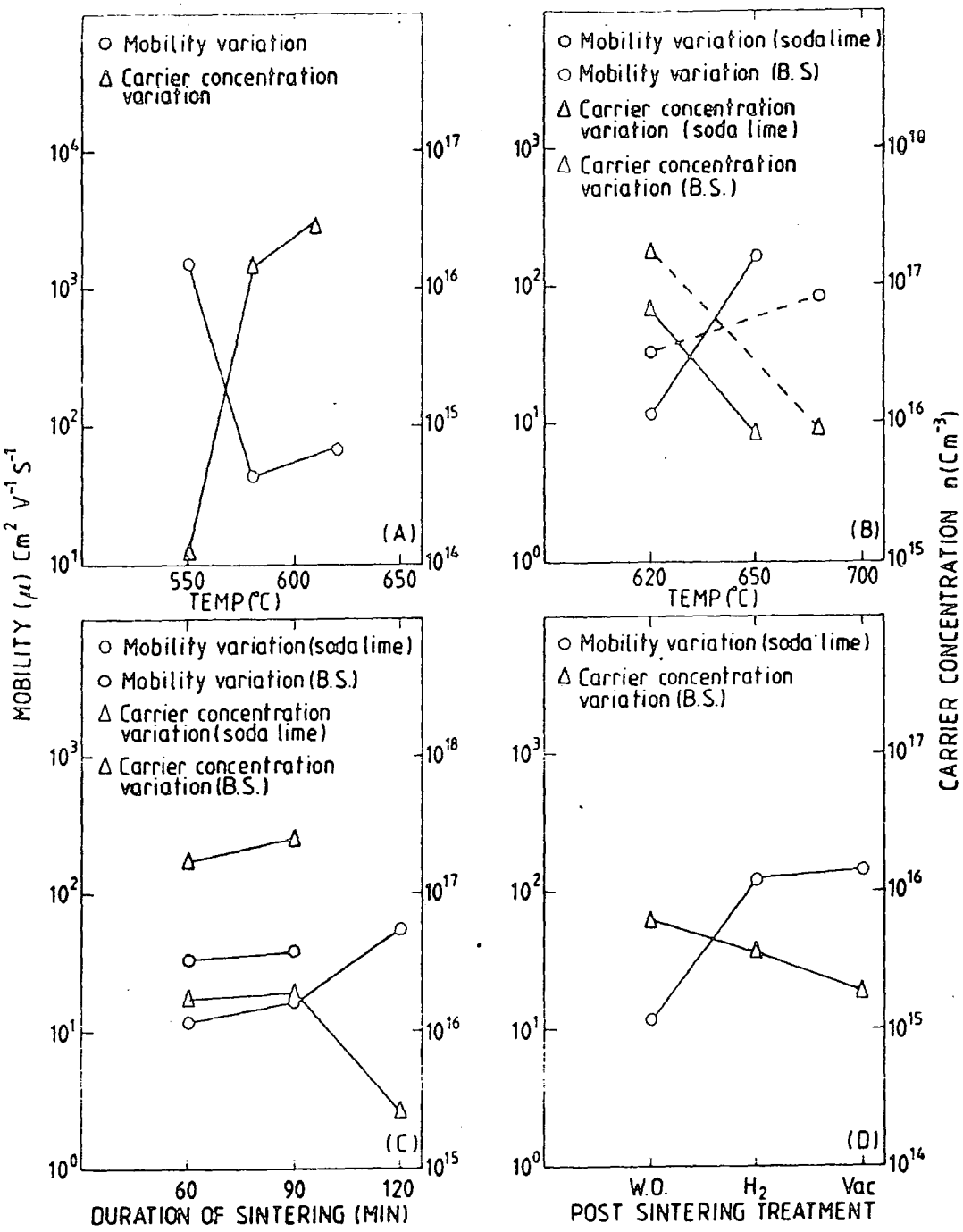


Fig. 6.11 : Variation of mobility and carrier concentration with

A Sintering temperature (5 mins duration)

B Sintering temperature (60 mins duration)

C Duration of sintering

D Post sintering treatment (optimum condition)

optimum for complete utilization of the $CdCl_2$ as a flux and as a donor, i.e., the molten $CdCl_2$ was able to dissolve CdS particles and promote grain growth, and it was also able to donate adequate donors. By decreasing the sintering rate to 30%, the time span between 400° and 600° was estimated to be 14 minutes, twice as long in the critical zone. This would lead to a large loss of $CdCl_2$ before reaction at the melting point of $CdCl_2$, which is 568°C (16), could occur. Although a reasonably compact structure was produced, a major reduction in the carrier concentration resulted, probably due the loss of Cl doping. The occurrence of high mobility values is very unusual and will be discussed in Chapter 7. When the sintering rate was increased to 100%, the time span for the sample in the 400°-600° 'critical zone' was estimated to be only 4 minutes. A fast sintering rate was reported (17) to cause the flux to flow to the film interface before sintering is well advanced. Although the 100% sintering rate did promote sintering, it resulted in a low density film with non homogeneous structure as shown in Figure 6.5b. The electrical behaviour was also affected by a loss of $CdCl_2$ as donor.

The importance of the sintering rate has also been reported by H. Yang et al (14).

Sintering envelope configuration : The most important component of the sintering envelope is the cover which should be designed in a controlled fashion to retard the direct evaporation of the high vapour pressure $CdCl_2$ at the early stages of sintering, thus ensuring that adequate $CdCl_2$ remained before its melting point was reached. The three different cases studied here reflect the significance of the cover where the best layer was achieved with an open side envelope configuration which imposed some restriction on the $CdCl_2$ pressure. However, this is still not the best configuration since the long side

opening is similar to a very big hole as shown in Figure 4.11. This is probably the reason for the similarity of the electrical behaviour between this configuration and the open boat configuration. However, the morphologies of the two layers shown in Figure 6.4b and Figure 6.5c show a marked difference which is a good indication of the effect of the open sided envelope in maintaining a higher $CdCl_2$ ratio. Trials to cover the envelope completely to utilize the maximum amount of $CdCl_2$ resulted in unexpectedly poor morphological and electrical behaviour (Figure 6.5d and Table 6.4d). This is probably due to the large amount of $CdCl_2$ remaining because evaporation of $CdCl_2$ could only occur when the vapour pressure of $CdCl_2$ lifted the cover slightly. The presence of excess $CdCl_2$ in the layer hindered grain growth (14) because of its presence on the surface and on the grain boundaries. In addition, too much Chlorine will result in a heavily doped CdS layer (19) leading to a higher resistivity and lower carrier concentration.

It is concluded therefore that the open side configuration is the best choice as a compromise. The significance of the envelope cover has been studied extensively by H. Uda et al (19). Their optimum CdS layer was achieved by sintering in an alumina case with a perforated cover with a hole area of between .39 and 1.42 cm^2. They achieved a resistivity lower than .5 Ω cm with a carrier concentration of the order of 10^{18} cm^{-3} and mobility of 14 cm^2 v^{-1} s^{-1}. When they increased the hole area to 7.07 cm^2 the resistivity increased and the carrier concentration and mobility decreased, i.e. the electrical behaviour became poorer. J.S. Lee et al (20) also studied the significance of sintering CdS layers in a boat with a controlled opening and they also found this as an important condition to achieve a transparent CdS sintered layer. They sintered their layers in a quartz ampoule which had four 1mm holes, and obtained a low resistivity of 0.5 Ω cm.

Flow rate : The furnace ambient is very critical in the sintering procedure. An adequate flow of inert gas over the surface of the layer is normally required to prevent oxidation. A very slow flow will result in faceting effects, while a very high rate will result in a fast drive-out of Cl_2. Both situations will prevent a proper sintering. The optimum layer was achieved with a 0.1 L/min flow rate.

It is worth mentioning that the optimum inert gas flow rate is possibly a characteristic of each experiment and could vary slightly from one experiment to another. H. Young et al (20)(21) used a flow rate of .1 L/min, and they increased the flow to .2 L/min in their recent work (22). Although these variations are small they nevertheless confirm that the flow rate is a characteristic of each experiment.

Sintering temperature and duration : The correct sintering temperature and duration are probably the most important parameters in the whole screen printing procedure, since they define the optimum morphological and electrical behaviour of the layer (18). However, they are not easy quantities to determine because the optimum choice depends on many parameters such as paste components, substrate material and furnace type (23). The optimum sintering temperature was found to be 620°C which is lower than that reported by many workers. The Matsushita group in Japan started with a sintering temperature of 630°(24)(25), but in their recent work they increased it to 690° to reduce the residue of excess Cl ions present in the layer after sintering at 630°(13)(26)(27) The Korean group used 650°C as their optimum for sintering CdS layers (14)(20)(21). It is believed that they were able to use such high sintering temperatures because of the superior quality of their substrates. The significance of substrate choice will be discussed in detail in Chapter 7.

The powdery structure of the dry layer shown in Fig. 6.7 was expected because the $CdCl_2$ had not melted and was trapped in the printed paste. The structure had a narrow grain size distribution about an average grain size of 1-3μm. When the sintering temperature was raised to 550° significant grain growth occurred, which is unexpected, since the melting point of $CdCl_2$ is 568°C. The $CdCl_2$ is supposed to melt and dissolve some of the CdS grains. However, the microstructure (Fig. 6.7B) suggests that significant sintering started at least 18°C below the reported melting point. This early sintering phenomenon was observed by H.G. Yang et al (11)(14) at 560° which is still 8°C below the melting point. They explained this was due to the difference in the melting temperature between the surface and the bulk of fine particles. The sharp reduction in the resistivity which occurred after sintering at 550° (22 Ω cm), from the very high resistivity of the dry layer (10^6 Ω cm), is largely attributed to the creation of S vacancies (12). It is not certain if any Cl doping occurred at this temperature because of the very low carrier concentration of ($1.2 \cdot 10^{14}$ cm^{-3}). It has been reported that a similar carrier concentration can be produced by S vacancies in a layer which has no $CdCl_2$ (11). The other feature of sintering at this temperature is that the residual concentration of Cl ions left in the sintered layer is .27 wt% as found by atomic absorption spectroscopy (Chapter 5) which indicated a great loss of chlorine at low temperature. H. Uda et al (19) found more than 2 wt% of Cl ions still remaining at temperatures below 560°, which is an order of magnitude more than the amount found in this study. This could be related to their very controlled envelope configuration.

When the sintering temperature was raised further, the resistivity decreased until it reached a 2Ω cm at 620° (5 min duration). The carrier concentration showed a marked increase of two orders of

magnitude over the value obtained at 550°, as shown in table 6.5 B,D. This improvement in electrical behaviour is attributable to the onset of Cl doping as reported by many authors (11)(28). It is suggested here that significant Cl doping begins once the $CdCl_2$ was melted as tables 6.5C - 6.5D show. It is also clear that increased Cl donor doping occurs at higher temperatures. Prolonged sintering at 620° favours further grain growth, where the molten material solidifies, and the grains tend to rearrange themselves to yield a compact structure. Growth was almost complete in 90 minutes (Figure 6.8C). The electrical behaviour in table 6.6C shows a similar improvement under these conditions, where the mobility lies in the range reported by others as optimum for screen printed layers. H. Uda et al achieved a value of 14.2 $cm^2v^{-1}s^{-1}$, while H. Yang et al (14) reached 25 $cm^2v^{-1}s^{-1}$. The resistivity and carrier concentration values for the optimum layer produced here were 3Ω cm and 8.6 x 10^{16} cm^{-3} respectively, as compared with .36Ω cm and 1.2 x 10^{18} cm^3 reported by H. Uda et al (6). It is clear that the higher resistivity and lower carrier concentration obtained here is attributed to the loss of $CdCl_2$ by evaporation in the sintering procedure. This is obvious from the amount of Cl detected by AAS in the present layers which was less than .05 wt%, whereas for example; although H. Uda et al (19) sintered their layers at 690°C, they contained .1 wt% of Cl. Such a quantity of chlorine was estimated to give a carrier concentration of 8 x 10^{20} cm^{-3}, although their experimental values show 500 times less. The difference arises from the presence of $CdCl_2$ at the grain boundaries and on the surface. A further increase in the sintering time to 120 min (Figure 6.8D) led to the appearance of Cd faceting as confirmed by EDAX analysis. The resistivity increased sharply to 31Ω cm with a large reduction in the carrier concentration. The reason for this is probably due to the out

diffusion of chlorine, which increases the height of the potential barriers of the grain boundaries (14). Sintering at 650°C for 60 min, although yielding a better structure than that of a similar layer sintered at 620° for 60 min, led to lower values of carrier concentration and mobility (table 6.6B). This is also, probably due to the out diffusion of chlorine. The term high temperature as used here is a characteristic of the type of glass used. Although 650° is considered a high temperature for soda lime glass it is not particularly high for a high quality borosilicate or silica glass. Increasing the sintering temperature to a value above that recommended for any particular glass will certainly result in glass distortion, and hence a considerable mis-match between the glass and material deposited on it. This will make a major contribution to the properties of the layer. Although according to report, 620° for 90 min is high for soda lime glass, it was nonetheless found to be the optimum condition for sintering CdS layers.

The trials made on borosilicatate glass resulted in a non homogeneous microstructure with high mobility values for all the layers examined. However, the values of resistivity and carrier concentration for the optimum case for sintering at 620° for 90 min were apparently better than for layers on soda lime glass, whereas the morphology was better in the latter case. This contradictory behaviour can perhaps be interpreted in terms of the thermal expansion and thermal conductivity of the glasses. Borosilicate glass has a much lower thermal expansion (3.3×10^{-6} per deg^{-1}) than soda lime glass (9×10^{-6} per deg^{-1}). By considering the thermal expansion of CdS (5.7×10^{-6} per deg^{-1}) (16), this would suggest that the fully fired CdS paste would expand at a much higher rate than borosilicate glass, leading to a pore structure. On the other hand the thermal expansion of soda lime glass is much

higher than that of the thermal expansion of CdS paste, which will not allow flow out of the paste under normal conditions, so that a more compact microstructure is formed.

The above discussion would suggest the use of soda lime substrates as the best choice for depositing screen printed CdS layers.

Post Sintering treatment : post fabrication annealing has been reported as over-riding some of the various conditions involved in the fabrication processes of CdS films deposited by thermal evaporation (2) (29) and spray pyrolysis (30) (31). However, for screen printing CdS layers the only published work is by S.L. Fu et al (32). Their sintered CdS films had high resistivity with non uniform morphology, and they used vacuum annealing to reduce the resistivity by more than 5 orders of magnitude with a more regular morphology.

In the present work greater grain growth was achieved with vacuum annealed layers, probably due to the better close atmosphere obtained in this case, compared with the open atmosphere when hydrogen was used. The electrical behaviour of the annealed layers, whether in vacuum or hydrogen was unexpectedly poorer than before annealing; with a smaller carrier concentration and abnormally high mobility. This may be because the films were sintered under optimum conditions with the desirable non stoichiometry of the CdS layers. Post sintering annealing probably disturbed this balance by increasing the loss of sulfur.

6.2.2.7 Conclusions

The investigation of the sintering conditions described above suggests the following as the optimum conditions for sintering CdS screen printed layers.

i) Use a moderate sintering rate equivalent to 50% M.P.

ii) Use an open side envelope configuration to ensure controlled evaporation of the $CdCl_2$ vapor.

iii) Use a compromise argon flow of .1 L/min.

iv) Use soda lime glass for the best combination of morphological and electrical behaviour of the CdS layer.

v) Avoid post-sintering treatment of an optimum layer.

6.2.2.8 Comments and Conclusion of Hall effect Measurements

It turned out that there are three different conditions to be optimized in the screen printing process namely:-

1 the Printing Conditions

2 the Preparation Conditions

3 the Sintering Conditions

These conditions are interdependent and in order to have a reproducible result the procedure must be standardized as much as possible.

With such care taken, it was possible to obtain an optimum CdS screen printed layer with reasonably compact morphology (see Figure 6.4B) and a low resistivity of (3)Ω cm with a carrier concentration of (8.2×10^{16}) cm^{-3} and a mobility of (16) $cm^2v^{-1}s^{-1}$. These values are suitable for the fabrication of good solar cells.

6.2.3 Schottky Barrier Diode Measurements

6.2.3.1 Introduction

A further method of characterising CdS layers is via the formation of simple Schottky barrier devices on them. This had additional consequences, viz:-

1. Another substrate, namely, SnO_2 coated glass was examined.
2. The optimum preparation and sintering conditions found by Hall Measurements were confirmed.
3. The usefulness of the sintered layers for junction formation was assessed before more complicated heterojunctions were formed.

Schottky barrier devices were simply obtained by thermal evaporation of 1mm diameter gold dots onto a screen printed CdS layers at a vacuum of

about 1 x 10^{-5} torr. The resultant devices were investigated using conventional current-voltage (I-V) and capacitance-voltage (C-V) measurements. Useful information can be extracted as described in Chapter 2.

6.2.3.2 Effect of preparation conditions

In the following sections the properties of Schottky devices formed on differently prepared CdS layers are presented. In addition to the previously discussed parameters in section 6.2.2.2, two more parameters were introduced here including etching effects and a higher $CdCl_2$ ratio.

i) Powder choice

The current-voltage (I-V) characteristics for Schottky barrier diodes prepared on CdS layers using the main three powders under investigation are shown in Figure 6.12A. The diode with 'powder A' gave the best rectification with the least series resistance. The diode on 'powder B' had a higher series resistance, while that on 'powder C' had very little rectification, with the highest series resistance observed. The calculated resistivities were 177, 2500 and 12,500Ω.cm for the three layers.

The corresponding semilogarithmic plots of forward bias I-V characteristics are shown in Figure 6.12B. The values of the diode factors were calculated from the slopes of the plots of LnJ_F-V_F using equation (2.14). These values were 2.1, 2.5 and 4.5 for the three Shottky diodes on powders A, B and C respectively. Although the lowest diode factor (for powder A) was still above the optimum value of an ideal diode (Chapt. 2) it did indicate the superiority of the powder A diode.

The capacitance-voltage (C-V) characteristics measured at 1 MHz for the three diodes are shown in Figure 6.12C. The curves reveal a

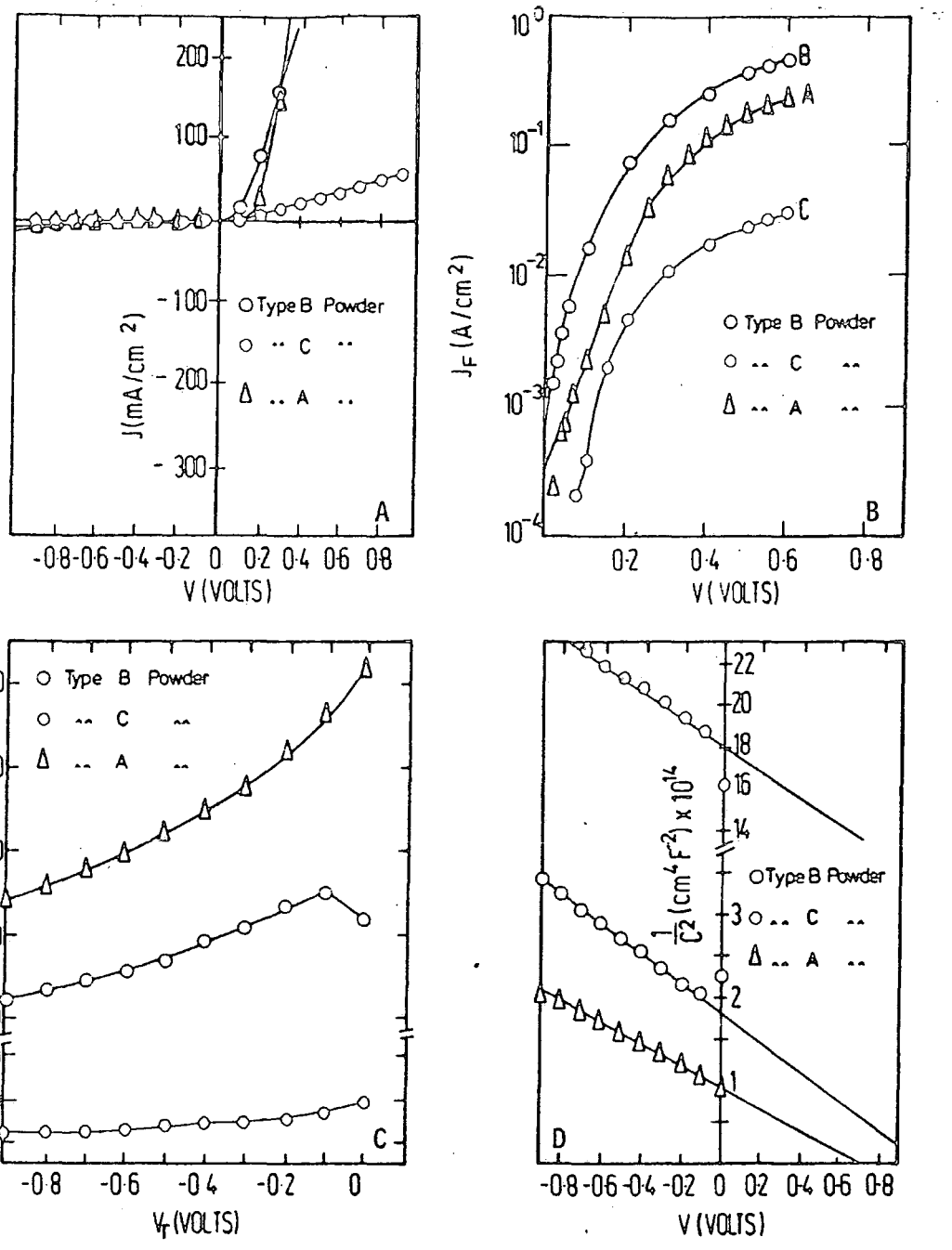
decreasing capacitance with reverse bias for all three diodes. However, this was rather smooth for the type A powder diode, with a high value of capacitance. Type B and C powder diodes had lower capacitances with little change with reverse bias.

C^{-2}-V plots were also obtained and there were straight lines for all diodes. The net carrier concentrations were calculated from the slopes of each plot using equ. 2.2 1 (Chapter 2) and the carrier mobility was calculated using equ. 2.2 2 (Chapter 2). The calculated values are recorded in Table 6.9 together with the resistivity values of the CdS layers. The diode on powder A clearly gives the best electrical behaviour. The intercept on the voltage axis gives the value of the diffusion potential (V_d). The intercept is smaller with the powder A diode, which suggests that the thinest interfacial layer is present in these diodes as discussed in Chapter 2. Furthermore, the widths of the depletion regions, W_d, were calculated using equ. 2.19 (Chapter 2) leading to values of .07, .11 and .31 μm for A, B and C diodes respectively. This again shows that the powder A diode had an optimum value (35) whereas, for example, powder C diode had a very wide depletion region (.31 μm) which would be too large to allow direct tunnelling from the bottom of the conduction band into the metal (33). This probably explains the very poor behaviour achieved for 'powder C' diodes.

The above data reflects the superiority of the 'powder A' diode and hence confirmed the good choice of type A powder suggested in section 6.2.2.2.i.

ii) Etching significance

In general, starting with a clean CdS surface is a necessity for proper junction formation. Etching in dilute HCl is one of the methods which is currently used for surface treatment for the removal of



Powder Type	ρ(Ω cm)	$N_D(10^{17})cm^{-3}$	$\mu(cm^2v^{-1}s^{-1})$
A	177	2.08	.17
B	2500	1.5	.02
C	12500	.42	.01

Fig. 6.12 Characteristics of CdS screen printed Schottky diodes using different CdS power types

A) I - V plots
B) $\ln J_F - V_F$ plots
C) C - V plots
D) $1/C^2$ - V plots

Table 6.9 Electrical data of the above diodes

undesirable material. For example, faceted cadmium can occur on the surface of the sintered CdS layers. Figure 6.13 shows a micrograph of a faceted CdS surface before and after etching, while Figure 6.14 reveals the behaviour of Schottky diodes prepared on each type of surface. There is a significant improvement in the diode behaviour after etching. The ohmic behaviour of the diode facricated on the faceted cadmium before etching can be attributed to the formation of an Au/Cd intermetalic compound (2).

Surprisingly, all the resultant CdS layers sintered on SnO_2 coated substrates were dark yellowish in appearance, unlike the CdS layers sintered on glass which showed a normal yellow appearance. Attempts to remove the darkness by washing in alcohol was not successful. However, immersion in dilute aqueous 3-5% HCl for 3-5 sec. was successful and the colour became the normal yellow. The subsequent Schottkys were made on etched layers.

iii) Flux ($CdCl_2$) ratio

Typical forward current characteristics of the Schottky diodes on layers using 7%, 10% and 15% $CdCl_2$ ratios are shown in Figure 6.15A. The diode on the layer with 10 wt% $CdCl_2$ gave the best I-V behaviours with the least series resistance. Higher or lower $CdCl_2$ ratios resulted in a higher series resistance with very soft behaviour with the higher ratio. The estimated resistivity of CdS layers using 7%, 10% and 15% were 8742, 2500 and 3100Ωcm. The lowest value was observed with the CdS layer using 10 wt% $CdCl_2$.

The capacitance-voltage (C-V) characteristics for the three diodes are shown in Figure 6.15B. They reveal a smoothly decreasing capacitance with reverse bias for the diode with the 10 wt% ratio, while the capacitance variation with reverse biase is very small for the other diodes. The highest capacitance value was obtained with the diode using the 10% ratio.

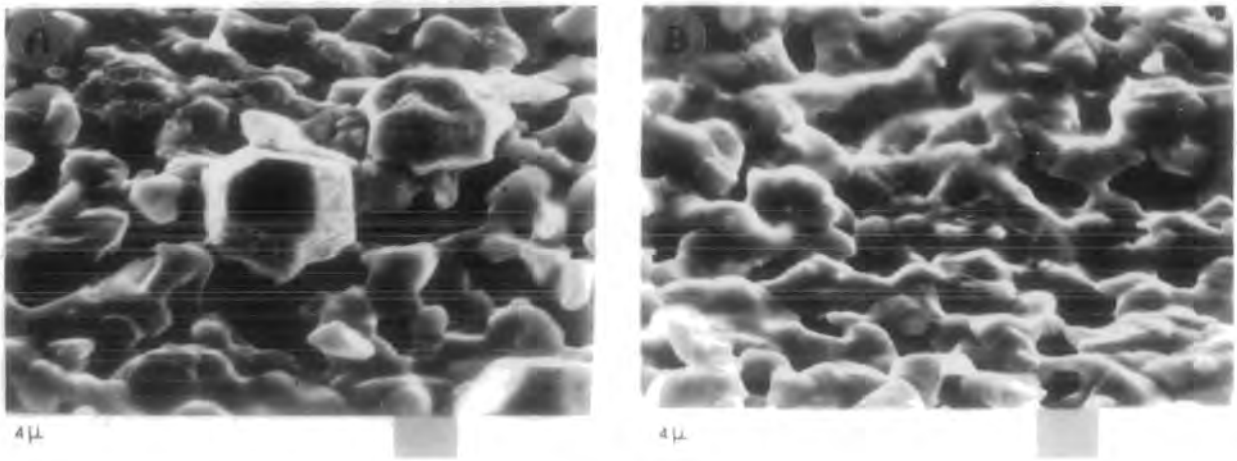


Figure 6.13 : SEM micrograph of CdS surface.

A) CdS surface before etching (Cd facets)
B) CdS surface after etching.

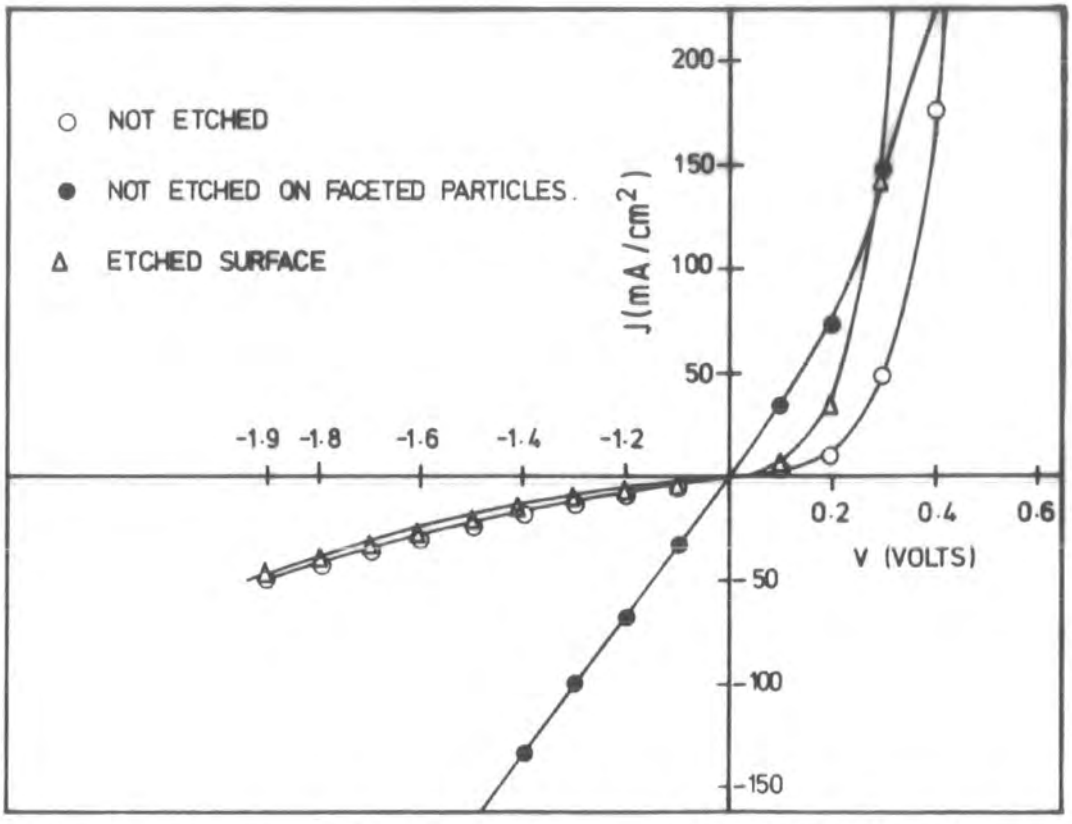
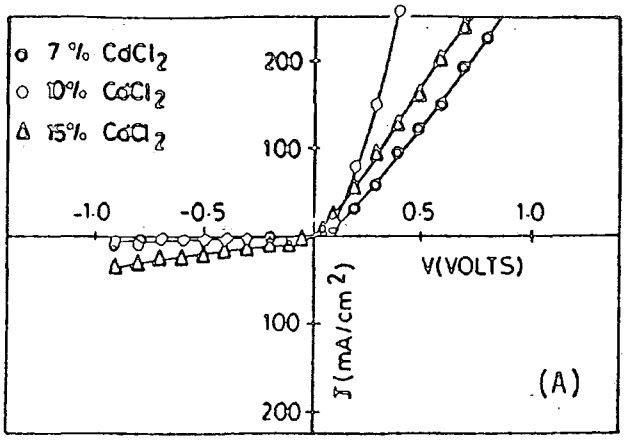


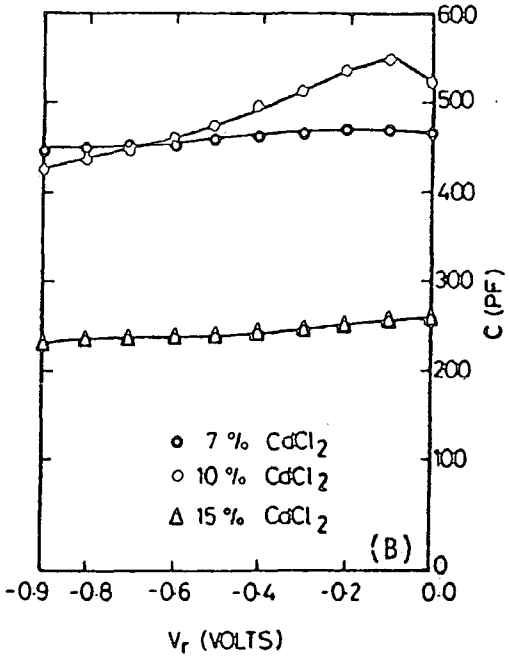
Figure 6.14 : Effect of etching on screen printed CdS Schottky barrier diode I-V characteristics

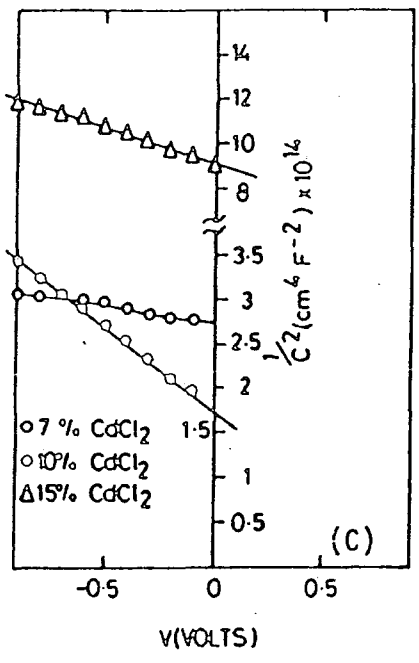
The Linear C^{-2}-V plots shown in Figure 6.15C give the smallest intercept with the V-axis for the '10% ratio' diode. The net carrier concentration and mobility values are recorded in table 6.10 together with the layer resistivities.

6.2.3.3 Discussion

i) Powder choice : The results achieved with the optimum powder (A) in this investigation (table 6.9A) were very poor by comparison with the Hall measurements of the same powder on insulating Soda Lime glass (Table 6.1A). The resistivity of a layer sintered on SnO_2 coated glass was 177Ω cm compared with 3Ω cm for a similar layer sintered on soda lime glass. The corresponding mobility values were .17 $cm^2v^{-1}s^{-1}$ and 16 $cm^2v^{-1}s^{-1}$. Such high resistivity and very low mobility values were not considered to be suitable for further solar cell fabrication. P.C. Pande et al (34) obtained similar high resistivity (600Ω cm) and low mobility values (.38 $cm^2v^{-1}s^{-1}$) for their electrophoretically deposited layers on SnO_2 coated glass and they explained this due to the presence of potential barriers between .14 and .18 eV high at the intergranular boundaries. In contrast H. Yang et al (14) reported a value of .048 eV for the potential barriers in their screen printed layers deposited on insulating glass; and they obtained a low resistivity CdS layer of .5Ω cm with carrier mobility of 25 $cm^2v^{-1}s^{-1}$. Comparing our results and those of P.C. Pande et al on SnO_2 glass with those of H. Yang et al on insulating glass, it seems obvious that the only apparent difference is the SnO_2 on the glass. The effect of SnO_2 on the screen printed layer is probably quite complicated, although contamination with tin undoubtably occurs, and would appear to be responsible for the high intergranular potential barriers. The relatively high carrier concentrations of (2×10^{17} cm^{-3}) in those layers with such high







$CdCl_2$ ratio	ρ(Ωcm)	N_D $(10^{17})cm^{-3}$	$\mu(Cm^2v^{-1}s^{-1})$
7%	8792	.6	.01
10%	2500	1.5	.02
15%	3100	.78	.03

Fig. 6.15 Characteristics of CdS screen printed Schottky diodes using various $CdCl_2$ ratios.

A) I - V plots
B) C - V plots
C) $1/C^2$ - V plots

Table 6.10 Electrical data of the above diodes

resistivity and low mobility values is rather unusual. In single crystal CdS, such carrier concentrations would lead to a resistivity of approximately 0.1 Ωcm.

ii) Etching significance : Etching in dilute HCl was necessary for all the CdS layers sintered on SnO_2 glass to remove the darkish appearance. The optimum concentration and etching period were 4% and 4 sec respectively.

It is well known that etching is important in the preparation of clean surfaces of CdS single crystals (35) and thin films (36). This etching procedure has frequently been found to affect the junction properties.

Interfacial layers on screen printed CdS surfaces are very likely to occur in a variety of ways; for example it was initially thought that the darkness was due to the incomplete burning of the binder. However after increasing the prefiring at 300°C for a sufficient time to assure complete burn-off the darkness remained. The possible decomposition of the SnO_2 at high temperature leads to a non stoichiometry in the coating may have caused the darkening. Another possible source of an interfacial layer is the non avoidable chemisorption of oxygen during sintering. M. Höung et al (37) reported that O_2 chemisorption occurred on the surface of the sintered CdS layer, no matter how the films were prepared. The chemisorption of oxygen in our experiments could have resulted from oxygen in the sintering atmosphere and during the gradual cooling procedure. The existence of an oxide layer can lead to the formation of a bulk like oxide over layer. D. Litchman et al (38) and D. Hounge et al (37) identified this oxide layer as a thin sulphate layer such as an SO_4^{-2} like compound. The sintered layer could also absorb O_2 from the atmosphere while transferring to the vacuum jar for Au deposition. L.

Mahdjunbi et al (36) found an interfacial layer resulting in this process. They fabricated the best Schottky diodes on their vacuum evaporated CdS layers when they were prepared in situ i.e. under the same vacuum. The quality of the vacuum can also affect the interfacial layer. The gold was evaporated onto the CdS in a relatively low vacuum of 1×10^{-5} torr, with a greater chance of an interfacial layer being formed. An oil diffusion evaporation system can add another source of contamination from the back streaming diffusion-pump oil (39).

Finally of course, etching itself can produce an interfacial layer (35). Although etching was necessary to remove the dark colour and any possible interfacial layer, it is not certain if it can remove any bulk oxide compound, such as SO_4^{-2} and a further treatment may be needed in such cases (37).

Flux ($CdCl_2$) ratio : The trials made to fabricate Schottky diodes on sintered layers with various $CdCl_2$ ratios confirmed the results obtained in section 6.2.2.2 ii concerning the optimum ratio of $CdCl_2$ (10 wt%). Lowering the $CdCl_2$ ratio resulted in very poor Schottkys. The high series resistance and very slow variation of capacitance with reverse bias, together with the expected large intercept in C^{-2} vs V plot were indications of the presence of a thick interfacial layer. It is believed that the occurrence of this interfacial layer is due to the poor morphology of the CdS layer with 7 wt% $CdCl_2$.

Increasing the $CdCl_2$ ratio in the paste beyond 10 wt% would do more harm than good. The I-V characteristics of diodes formed on layers using 15 wt% $CdCl_2$ were soft. H. Yang et al (11) found some recrystallized $CdCl_2$ on the surface of sintered layers with high $CdCl_2$ ratio. This unreacted $CdCl_2$ would lead to a shunting effect and would also result in a high density of interfacial states confirmed by the

very low capacitance value and slow variation with reverse bias, together with the very high intercept of the C^{-2}-V plots.

The occurrence of a secondary phase of unreacted $CdCl_2$ on the CdS surface when using higher than optimum $CdCl_2$ ratio will lead to an increase in the series resistance of CdS layer (20), and will not enable a proper junction to be formed. The harmful effects of excess $CdCl_2$ in screen printed solar cells have been reported by many authors (13) (20) (22) (25).

6.2.3.4 Conclusion

The characterization of various Schottky diodes under different preparation conditions confirmed the superiority of powder A, and the optimum choice of 10 wt% $CdCl_2$ ratio for the fabrication of the best CdS layer, as was also concluded from the Hall measurements. A brief treatment of all layers sintered on SnO_2 coated glass in dilute HCl is recommended to remove the dark colouration.

6.2.3.5 Effect of sintering conditions

In the following sections the properties of Schottky diodes on layers prepared under various sintering conditions will be presented. The significance of the furnace type will also be discussed here.

i) Furnace type

The preliminary studies described in Chapter 4 suggested that the muffle furnace was not suitable for sintering the CdS layers mainly because of its long sintering and cooling rates. Other difficulies associated with the use of a muffle furnace were mentioned in Chapter 4. However, trials were made to sinter similar CdS layers in both muffle and tube furnaces, to investigate the behaviour of Schottky Diodes fabricated on them. The current-voltage plots shown in figure 6.16A, indicate a lower series resistance for the diode formed on the layers sintered in the tube furnace.

The capacitance-voltage plot shown in figure 6.16B reveals a smoother behaviour of the 'tube furnace' diode compared to the 'muffle furnace' diode. The C^{-2}-V plots in figure 6.16C showed a large intercept in the latter case which was improved by hydrogen annealing.

The electrical properties of the diodes investigated are recorded in Table 6.11. Interestingly, although the mobilities were generally low, the 'muffle furnace' diodes showed an even lower value of mobility by about one order of magnitude.

ii) Sintering rate

The current-voltage (I-V) characteristics of Schottky diodes prepared on CdS layers using sintering rates of 30%, 50% and 100% are shown in figure 6.17A. The '50%' diode had the lowest series resistance.

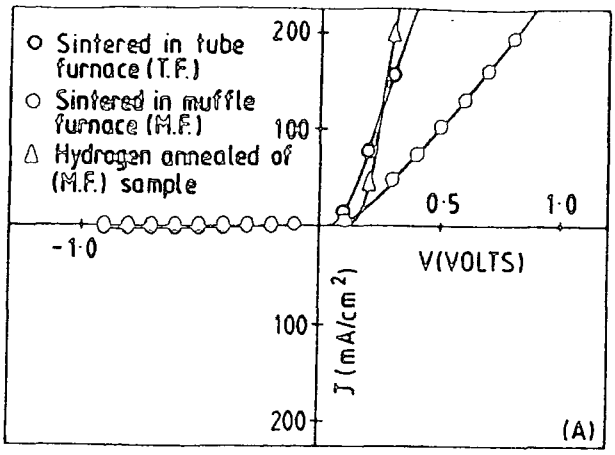
The capacitance-voltage (C-V) plots in figure 6.17B also reveal the superiority of '50%' diode. The C^{-2}-V plots in figure 6.17C showed the lowest intercept for this diode.

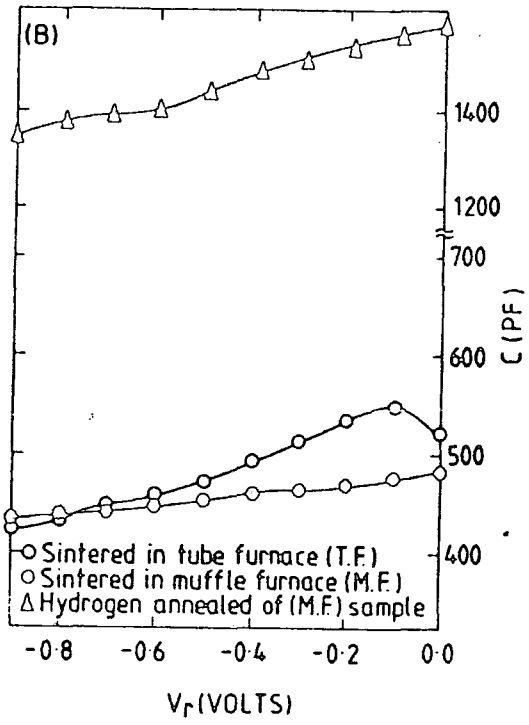
The electrical data of all three diodes are recorded in Table 6.12.

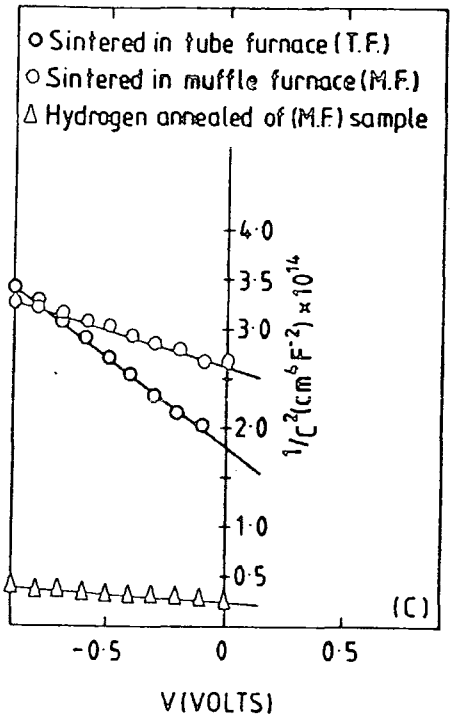
iii) Sintering envelope configuration

The current-voltage plots of diodes prepared on CdS layers sintered using three different envelope configurations are shown in figure 6.18A. The layer sintered in an open side envelope configuration produced the best behaviour with the least series resistance.

The C-V plots in figure 6.18B revealed a marked variation between diodes on layers sintered in closed or open side configurations. The C^{-2} vs V plots in figure 6.18C also gave the smallest intercept for the O.S. configuration diode.





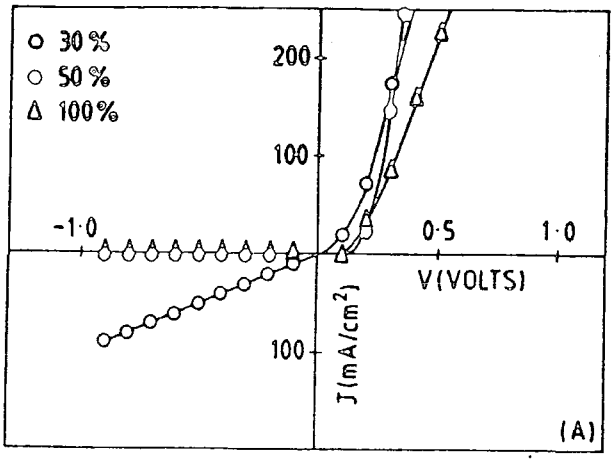


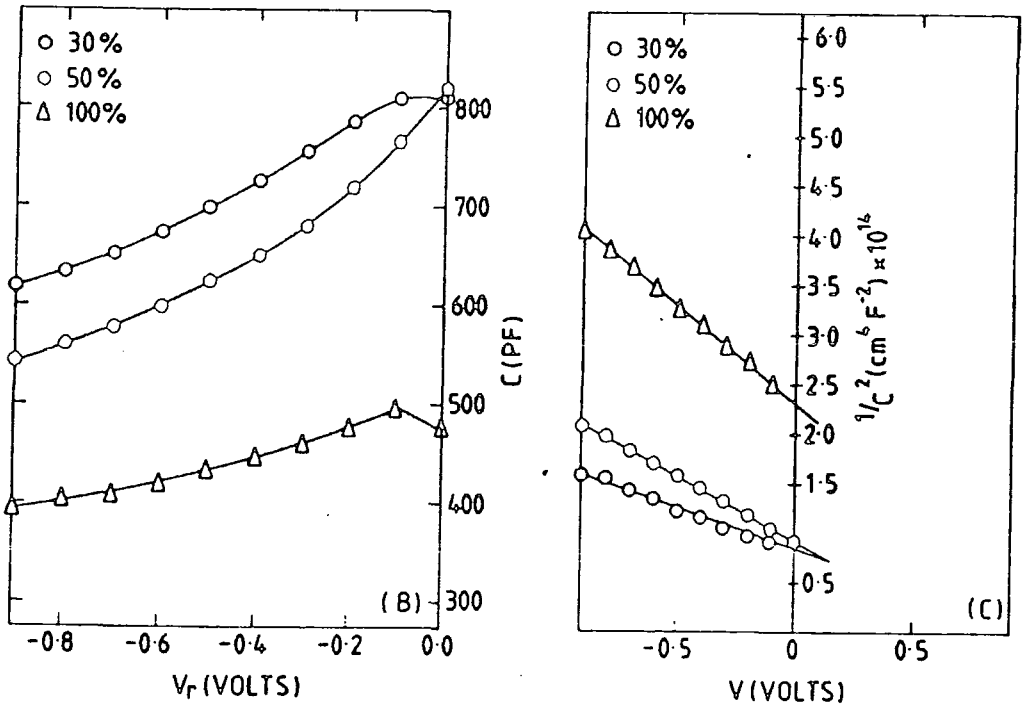
Furnace type	ρ (Ωcm)	$N_D(10^{17})Cm^{-3}$	$\mu(Cm^2v^{-1}s^{-1})$
T.F.	2500	1.5	.02
M.F.	3640	4.5	.004
M.F.(H_2)	500	25	.005

Fig. 6.16 Characteristics of CdS screen printed Schottky diodes using different furnaces

A) I - V plots
B) C - V plots
C) $1/C^2$ - V plots

Table 6.11 Electrical data of the above diodes



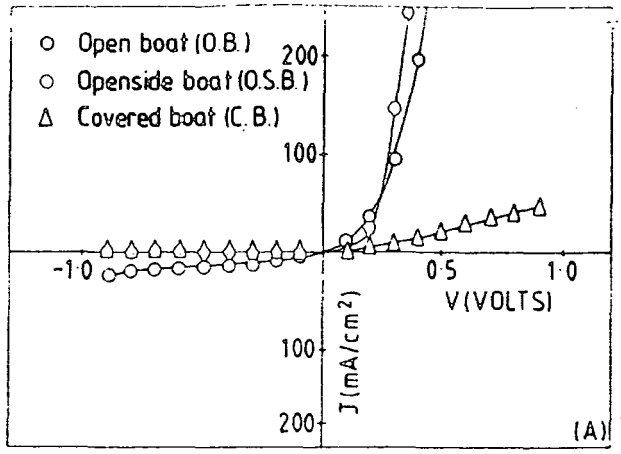


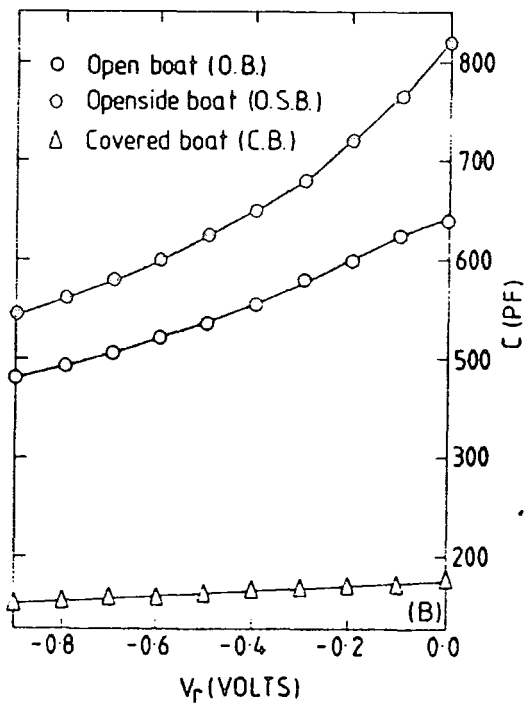
Sintering rate	ρ (Ω-cm)	$N_D(10^{17})cm^{-3}$	$\mu(Cm^2v^{-1}s^{-1})$
30%	314	3	.07
50%	177	2.08	.17
100%	300	1.43	.15

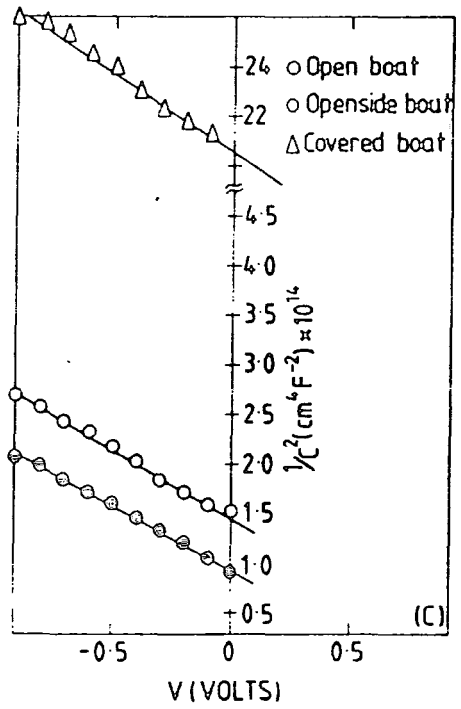
Fig. 6.17 Characteristics of CdS screen printed Schottky diodes with different sintering rates

A) I - V plots
B) C - V plots
C) $1/C^2$ - V Plots

Table 6.12 Electrical data of the above diodes







Boat Configuration	ρ(Ω cm)	$N_D(10^{17})cm^{-3}$	$\mu(cm^{-1}v^{-1}s^{-1})$
O.B.	376	1.93	.09
O.S.B.	177	2.08	.17
C.B.	795	.46	.17

Fig. 6.18 Characteristics of CdS screen printed Schottky diodes with different boat configuration

A) I - V plots
B) C - V plots
C) $1/C^2$ - V plots

Table 6.13 Electrical data of the above diodes

The electrical behaviour for the three diodes under investigation is recorded in table 6.13.

iv) Flow rate

The current-voltage characteristics of Schottky diodes prepared on CdS layers sintered in the tube furnace using three different flow rates of .04, .1 and .4 L/min are shown in figure 6.19A. The diodes formed on the layer sintered under .1 L/min flow rate provided the best device with the least series resistance.

The C-V plots in figure 6.19B showed the highest capacitance with a smooth variation for the '.1 L/min' diode. The C^{-2} - V plots in figure 6.19C gave the smallest intercept for the same diode.

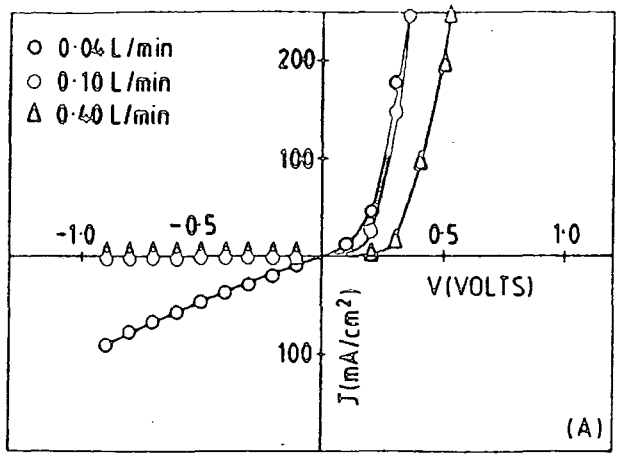
Table 6.14 lists the electrical data of the three diodes in question.

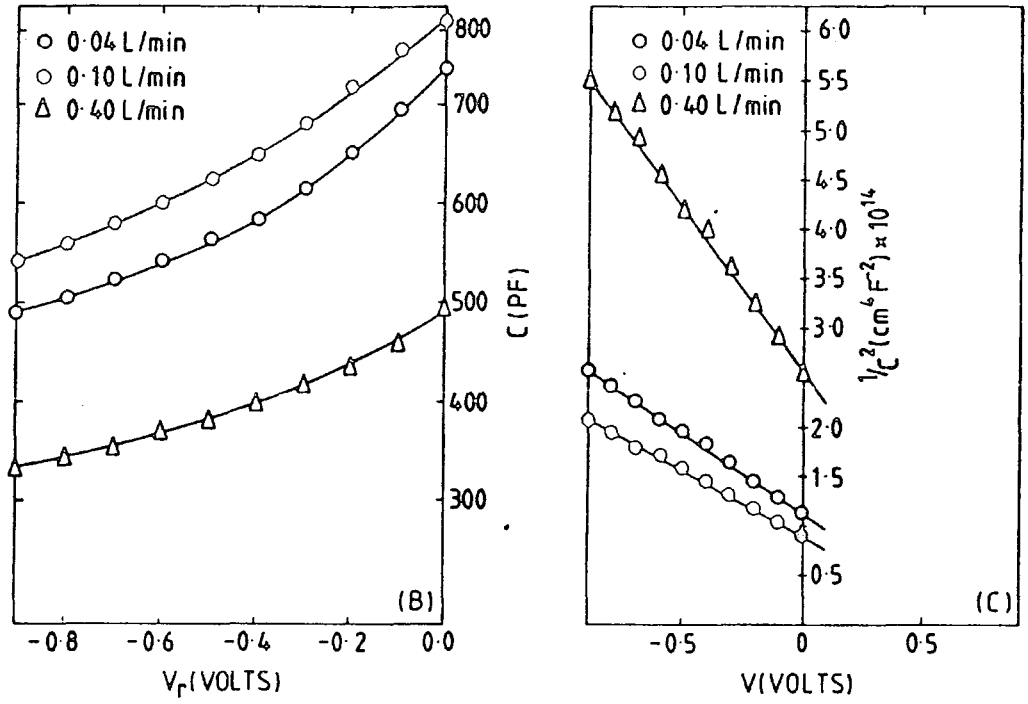
v) Sintering temperature and duration

Typical current-voltage characteristics of diodes prepared on CdS layers sintered at 620°C for 60 minutes, 90 minutes and 120 minutes, and at 650° for 60 minutes are shown in figure 6.20A. There was a clear dependence on sintering temperature and duration, 90 minutes at 620°C led to a diode with the lowest series resistance and hard reverse bias characteristics. Larger or smaller times at 620° resulted in a higher series resistance and inferior Schottky behaviour.

The C-V plots for the four diodes are shown in figure 6.20B. The highest capacitance and larger variation with reverse biase were found with the diode fabricated on the layer sintered at 620° for 90 minutes. The corresponding C^{-2} vs V characteristics shown in figure 6.20C were linear plots for all diodes. The diode formed on layers sintered at 620° for 90 minutes had the smallest interfacial layers.

The electrical data of the diodes together with resistivity values of the sintered CdS layers are recorded in table 6.15.



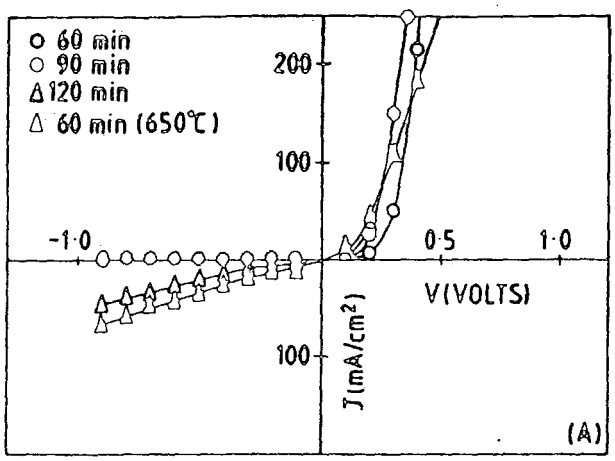


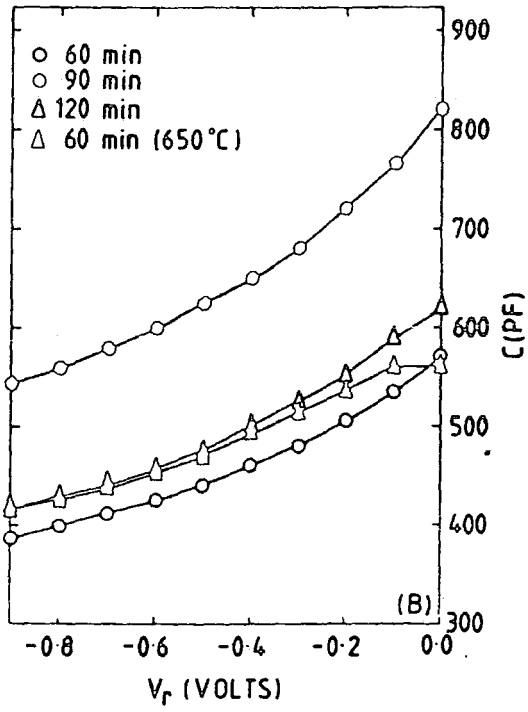
Flow rate	ρ (Ωcm)	$N_D(10^{17})cm^{-3}$	$\mu(cm^2v^{-1}s^{-1})$
.04	345	1.71	.12
.1	177	2.08	.17
.4	471	.84	.16

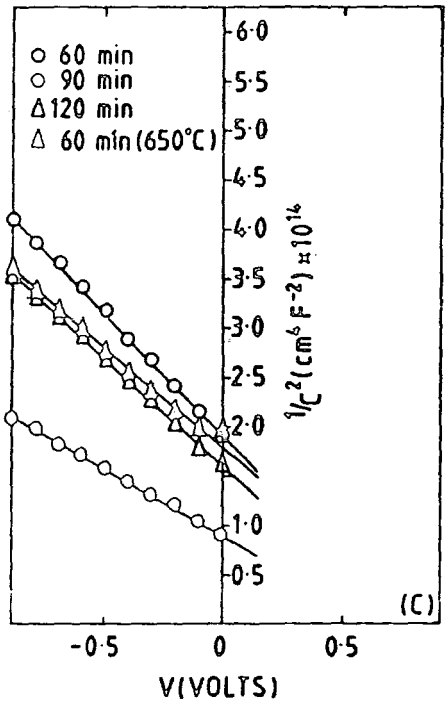
Fig. 6.19 Characteristics of CdS screen printed Schottky diodes with different flow rates.

A) I - V plots
B) C - V plots
C) $1/C^2$ - V plots

Table 6.14 Electrical data of the above diodes







Temperature (°C)	Duration (min)	ρ(Ωcm)	$N_D(10^{17})cm^{-3}$	$\mu(cm^2v^{-1}s^{-1})$
620	60	345	1.14	.16
620	90	177	2.08	.17
620	120	680	1.24	.07
650	60	523	1.44	.08

Fig. 6.20 Characteristics of CdS screen printed Schottky diodes with different sintering duration.

A) I - V plots
B) C - V plots
C) $1/C^2$ - V plots

Table 6.15 Electrical data of the above diodes

The SEM micrographs in figure 6.21 were taken in an attempt to relate the diode behaviour with the surface morphology of the sintered layers. The best morphology was indeed achieved with the CdS layer sintered at 620° for 90 minutes. Increasing the temperature or the duration led to the loss of the good morphology and the appearance of undesirable secondary particles.

vi) Post sintering treatment

a) Optimum 'Condition' Diodes

To investigate the effects of post sintering treatment for a possible improvement in the electrical behaviour of an optimum diode, three similar CdS layers prepared under optimum sintering conditions were chosen. Two of them were annealed in hydrogen and vacuum respectively at 350°, while the third was used as a reference untreated layer. Schottky diodes were formed on all of them.

The current-voltage characteristics of the three diodes are shown in figure 6.22A, where it is clearly seen that annealing in both hydrogen and vacuum resulted in inferior Schottky behaviour.

The C-V and C^2 - V plots in figure 6.22B and figure 6.22C respectively suggested the presence of interfacial layers for Schottky diodes formed on layers annealed in either atmosphere and confirmed the superiority of the untreated diode.

The electrical data of the three diodes together with the resistivity data of the three sintered layers are shown in table 6.16.

b) Non optimum diodes

To investigate the effects of post sintering treatment on non optimum diodes, CdS layers fabricated from powder B and powder C were chosen in a view of a large interfacial layers expected as discussed in sections 6.2.2.3 and 6.2.3.3.

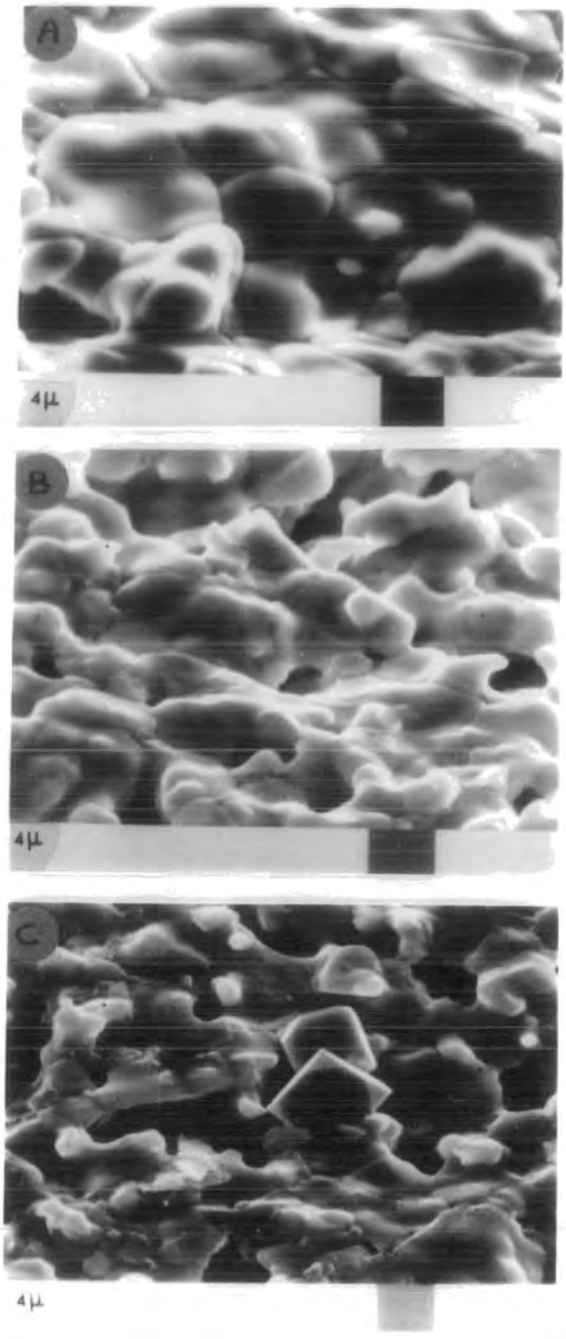
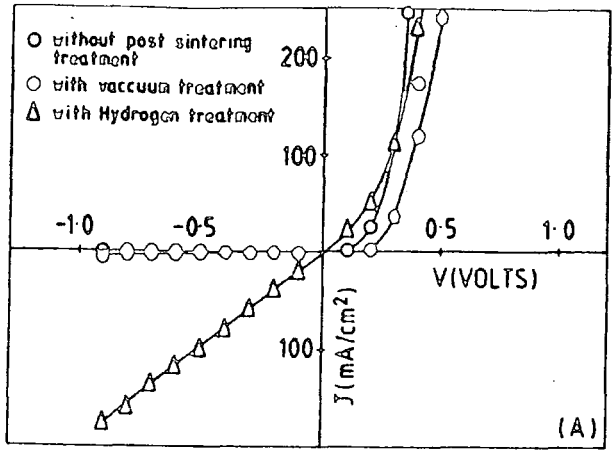
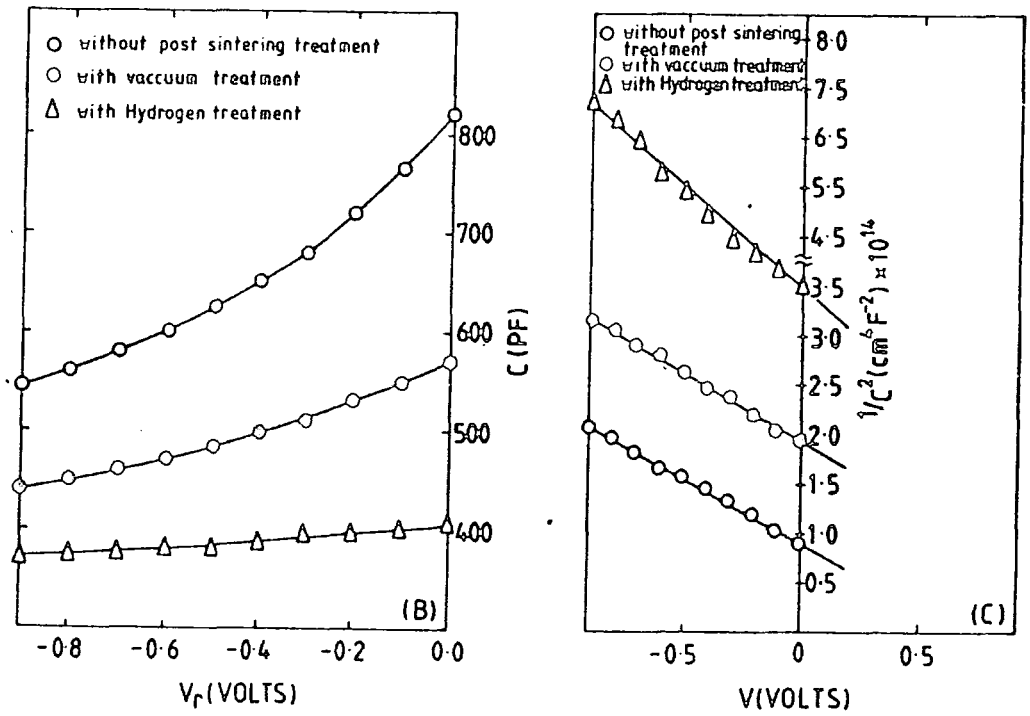


Fig. 6.21 SEM micrograph of CdS surface sintered on conducting (SnO_2) glass under various sintering temperatures

A : 620°C 90 min.
B : 650°C 60 min.
C : 620°C 120 min.





Treatment	ρ (Ωcm)	$N_D(10^{17})cm^{-3}$	$\mu(cm^2v^{-1}s^{-1})$
W.O.	177	2.08	.17
Vac.	491	1.7	.08
H_2	439	.7	.2

Fig. 6.22 Characteristics of CdS screen printed Schottky diodes with post sintering treatment
(i) optimum conditions.
A) I–V plots
B) C - V plots
C) $1/C^2$ - V plots

Table 6.16 Electrical data of the above diodes.

The current-voltage characteristics of Schottky diodes fabricated on CdS layers using powder B and powder C with and without post sintering treatment are shown in figure 6.23A. In contrast with the post annealing effects on an optimum 'diode', a significant improvement occurred here after vacuum annealing at 350°C.

C-V and C^{-2}-V plots in figure 6.23B and figure 6.23C respectively reveal similar improvement in the annealed Schottky behaviour. The electrical data are recorded in table 6.17.

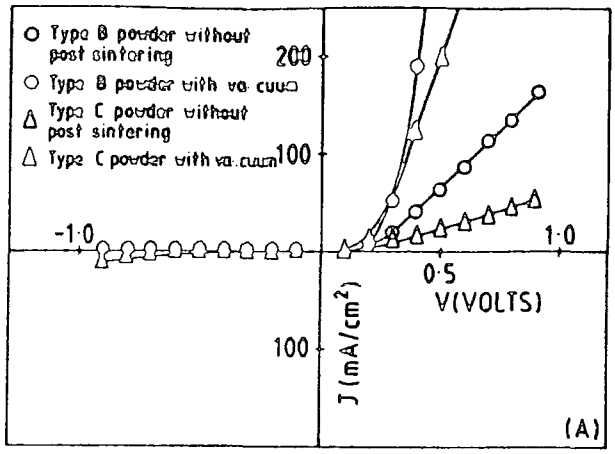
It is concluded therefore that post sintering annealing is only recommended for non optimum CdS layers.

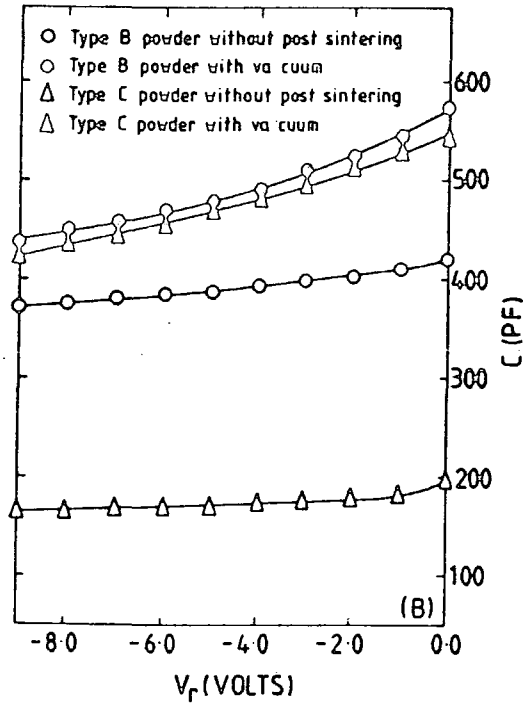
6.2.3.5 Discussion

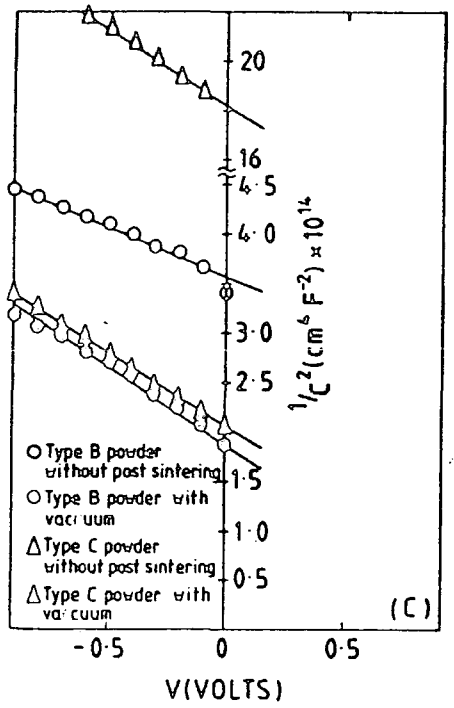
i) Furnace types : one possible advantage of the muffle furnace is its closed cavity which provides a good insulation from the room atmosphere, but it may cause a problem by creating a slight over-pressure inside the cavity which could harm the sintered layer. However, the major disadvantages of this furnace are its slow sintering rate and the difficulties of controlling the cooling procedure as described in Chapter 4. In addition the sintering envelope configuration is like an open boat and is therefore not optimised.

The significant improvement in the diode performance with post sintering annealing in hydrogen would confirm the presence of a high density of interfacial states on the layers sintered in the muffle furance. The tube furnace has proved to be superior to the muffle furnace in sintering the layers and it has been used by many authors (11) (14) (21).

The most efficient screen printed solar cells have been sintered in the so called belt furnace (6) (26) (40). A description of the features of this furnace was presented in Chapter 4.







Powder type	Treatment	ρ(Ωcm)	$N_D(10^{17})Cm^{3}$	$\mu(Cm^2v^{-1}s^{-1})$
B	W.O.	6280	2.8	.004
B	Vac	560	3	.01
C	W.O.	7780	.24	.03
C	Vac	628	1.72	.06

Fig. 6.23 Characteristics of CdS screen printed Schottky diodes with post sintering treatment.
(ii) non optimum condition

A) I-V plots
B) C- V plots
C) $1/C^2$ - V plots

Table 6.17 Electrical data of the above diodes

ii) Sintering rate : The optimum sintering rate in this study was found to be 50% which agreed with the Hall measurement investigation described in section 6.2.2.5 ii. The shunting behaviour in the I-V plots of the '30%' diode (figure 6.17A) suggested the occurrence of secondary recrystallised particles on the surface or at the grain boundaries, whereas the higher series resistance of the '100%' diode is probably due to the fast drive out of Cl donors at a fast sintering rate.

The effect of sintering rate on the electrical behaviour of the CdS layers was clearer from this work where Schottky diodes were fabricated since this reflected the conduction of carriers through the sintered surfaces rather than the in-plane properties investigated by Hall measurements. The optimum sintering rate of 50% would suggest a clean surface appropriate for Schottky diode fabrication and also for other junction formation.

iii) Sintering envelope configuration : The optimum configuration of the sintering envelope is not ideal as discussed in section 6.2.2.5, because of the large side opening. It has however been shown here that this minimum confinement of $CdCl_2$ pressure inside the envelope is very effective in improving the behaviour of Schottky diodes. A closed envelope configuration results in the maximum confinement of $CdCl_2$ vapour above the layer, which leads to a high doping level, with undesirable products remaining on the surface. That this is undesirable can be seen clearly from figure 6.18, where a diode fabricated on a CdS layer sintered in a closed envelope hardly rectified and contained a high density of interfacial states.

iv) Flow rate : Sintering CdS layers in an inert atmosphere is necessary to prevent oxidation at high temperature. In the tube furnace a correct flow of inert gas is required during the sintering process. Too slow a flow rate will not prevent oxidation completely.

On the other hand, with high flow rates the volatilised $CdCl_2$ will be driven off too fast and a high resistivity of the sintered CdS layer will result.

v) Sintering temperature and duration : The optimum temperature of sintering confirmed the assumption made in Chapter 4 that the glass under the SnO_2 coating was of soda lime type. However, the existence of the SnO_2 conductive coating would have increased the thermal conductivity of the glass, and this is probably the reason for the more compact morphology with larger grain growth which was achieved by sintering on SnO_2 coated glass (Figure 6.21). The morphology of the sintered CdS layer is more sensitive to a high sintering temperature on SnO_2 coated glass than on soda lime glass as figures 6.21A and 6.8B show. This again may be due to the higher thermal conductivity expected for SnO_2 coated glass.

The poor morphology of CdS layers sintered at high temperature (650°C) on SnO_2 glass, or for a long period (120 min) was accompanied by a loss of chlorine ions and cadmium faceting as discussed in section 6.2.2.6. This explains the shunting behaviour observed in the I-V plots of figure 6.20A.

The surface morphology of the CdS layers sintered at 650° for 60 min. and at 620° for 120 min., as shown in figure 6.21B and C, suggests that good junctions cannot be made on such surfaces in comparison with those on layers sintered at 620°C for 90 min. This is confirmed by the behaviour of Schottky diodes formed on these surfaces.

vi) Post sintering treatment :

a) 'Optimum condition' diode : Post sintering annealing was undertaken in an attempt to achieve: i) a reduction in the high resistivity of the sintered layer of (177 cm); and ii) an increase in the low mobility value of (.17 $cm^2v^{-1}s^{-1}$) obtained for the optimum

diode fabricated on the best CdS layer. Unfortunately the results obtained were not encouraging, since the resistivity of the annealed layers increased while the mobility remained anomalously low.

b) 'Non optimum condition' diode : A significant improvement in the behaviour of Schottky diodes formed on layers prepared under non optimum conditions, after post annealing in vacuum was expected for these conditions. It has been reported that post sintering treatment may over-ride some of the previous conditions (10) (29). S. Fu et al (32) found a marked improvement in the morphology and a major reduction in the resistivity of their non optimum as 'sintered' screen printed layers. The improvement observed with the 'powder B' diode was probably due to the removal of a thick interfacial layer together with an improvement of the surface morphology. The improvement in the 'powder C' diode after vacuum annealing could be due to the creation of S vacancies, in addition to the removal of an oxide layer. The improvements in the annealed layers can only be properly appreciated by referring to the nature of powder B and powder C as described in Chapter 5.

6.2.3.7 Conclusion

This investigation of the various sintering conditions suggests the following as the optimum procedure for producing the best CdS layers on SnO_2 coated glass : i) using a 50% sintering rate, ii) sintering in an open side envelope configuration, iii) using a flow rate of .1 L/min and iv) sintering at 620° for 90 minutes.

These conditions are in line with the optimum conditions found from the Hall measurements on layers on insulating glass.

The tube furnace was found to be superior to the muffle furnace in sintering CdS layers. Post sintering annealing is detrimental to 'optimum condition' diodes, but very effective with 'non optimum condition' diodes.

6.2.3.8 Comments and Conclusions from Schottky diode Measurements

It is well known that when a metal is evaporated onto a semiconductor surface, the metal and semiconductor may not be in intimate contact (41). This is due to the presence of an inevitable interfacial layer between the two. This layer can influence the behaviour of the diode in many ways (39) (42) (43). For example, a thick interfacial layer between Au and CdS will provide an extra barrier to carrier transport through the junction, and hence will lead to high series resistance and high ideality factors. In contrast a very thin interfacial layer is assumed to have no significant effect on current transport and is transparent to tunneling carriers (44) (33).

The above criterion was used to assess the CdS layers sintered onto SnO_2 coated glass. It was assumed that a layer with the thinnest interfacial layer would yield a good diode which was taken as an indication of optimum CdS layer fabrication.

1) Analysis of I-V Characteristics. The I-V characteristics can provide a wealth of information such as i) the rectification ratio of the diode, and whether a contact is rectifying or ohmic; ii) It can reveal any improvement in the behaviour of the diode with changing fabrication conditions (45). The variations in the gradient of the forward bias regime serve as an indication of the diode series resistance. The reverse bias regime also shows the hardness of a diode; iii) the slope of a semilogarithmic I-V plot yields the ideality factor, which is strongly affected by interfacial layers. For example, the lowest ideality factor measured for a 'powder A' diode in section 6.2.3.2, indicates the thinnest interfacial layer is produced with powder A. The value of the ideality factor can also provide information about the conduction mechanisms in the diode. For example, the value of the ideality factor of the optimum diode was found to be

2.1, this is larger than the optimum value of a good Schottky diode (Chapter 2). It indicates the non-applicability of the thermionic emission of electrons from CdS to Au and suggests that generation recombination in the space charge region is the dominant mechanism (46).

2) Analysis of the C-V plots. The degree of the change of capacitance with reverse bias can be used as a good indication of the thickness of the interfacial layer (47). For example, a smooth and large variation of capacitance with reverse bias in the 'powder A' diode, shown in figure 6.12C, is a good indication of a good junction with the thinnest interfacial layer. On the other hand, very slow variations of capacitance with reverse bias are an indication of a thick interfacial layer. This is because this thick layer will add capacitance in series with the depletion capacitance, making the change in applied voltage appear almost entirely across the interfacial layer (47).

3) Analysis of C^{-2}-V plots. Capacitance-voltage data in the form of C^{-2} vs V plots can be used to extract valuable information about the space charge region. However, because of the complexities associated with the possible decomposition of SnO_2 suggested in section 6.2.3.3, the utilization of C^{-2} vs V should be treated with caution. Nevertheless, it is known that the voltage axis intercept is extremely sensitive to the presence of an interfacial layer (45). Higher intercept values imply thicker interfacial layer (39), which generally mean a higher density of surface states, and lead to lower donor concentration values (35). This fact was used here to give an approximate picture of the investigated diodes. For example, the intercept for the 'powder C' diode in figure 6.12D predicts a very high intercept compared with 'powder A', and hence a high density of surface

state would be expected. The optimum diode was the one which had the smallest intercept, which in this investigation was 0.7 V, which is larger than the report 0.65 V for a diode on a CdS single crystal (33).

The roughness of the sintered screen printed layer (11) (22) will also make the above measurements more unreliable. With rough surfaces the intimacy of the junction will change from site to site and also the actual junction area will be considerably larger than the geometrical area of the contact. This situation will become worse in very non uniform surfaces, as in layers sintered for long time, as shown in figure 6.21C, where there is a pore grain structure with the emergence of faceted particles.

Despite these limitations the I-V and C-V plots do point out real differences between various diodes formed on CdS screen printed layers under various preparational and sintering conditions.

6.3 Structural Characterization

6.3.1 Introduction

Structural characterization was carried out to obtain an overall picture of the resultant CdS screen printed layer under various conditions, and to resolve ambiguities associated with some of the results described in the previous sections.

The four techniques employed were : SEM, EDAX, ESCA and XRD.

6.3.2 SEM observations

The scanning electron microscrope (SEM) is a powerful instrument for the assessment of the morphology of screen printed CdS layers. SEM micrographs obtained in parallel with the Hall measurements enabled a more rigorous control of the fabrication conditions to be established. Optimum preparation and sintering conditions produced a compact structure with few voids and appreciable grain growth, whereas non optimum conditions resulted in a non homogeneous and porous structure

with small grain growth. Good morphology led to good electrical behaviour as with CdS single crystal Schottkys (33). This correlation was found to exist in most layers investigated, and has been reported by many investigators of screen printed layers (11) (14). However, it is suggested that the correlation between a good morphology and good electrical behaviour does not always occur with polycrystalline layers, because of the complications introduced by the grain boundaries. An example can be seen from Schottky measurements where regardless of the good compact morphology of an optimum layer (figure 6.21), the corresponding electrical data for a diode formed on such a layer was poor. It is difficult to generalise about the correlation between morphology and electrical properties. Obviously good morphology is necessary but not always sufficient.

6.3.3 EDAX observations

Energy Dispersive Analysis by X-rays (EDAX) is a means of identifying the bulk composition of a material and of the localised features observed in the SEM. A particular example is shown in figure 6.8A, where the odd faceted particles were identified by EDAX as of pure cadmium. The shunting behaviour of the diodes formed on layers using a high $CdCl_2$ ratio was found to be due to unreacted $CdCl_2$ using EDAX. EDAX does however have some limitations since it cannot detect the presence of foreign species in the very top surface of the CdS layer because the X-rays come from a depth of 1 micron. Therefore, although the surface morphology might look clean in the SEM and show a stoichiometric composition according to EDAX, it might possibly still contain a substantial contamination in the surface layers. More sensitive methods in parallel with EDAX would then be required.

6.3.4 ESCA characterization

Electron Spectroscopy for Chemical Analysis (ESCA) is a very useful technique for the identification of foreign impurities in the top 20 Angstroms of a sintered layer. This study was undertaken to investigate whether an interfacial layer was present on the surface of a screen printed layer prepared under optimum conditions. An interfacial layer was believed to occur after sintering, and it was thought to contain sulphate ions (SO_4^{2-}) (37) (38). A high resolution scan was therefore made for an optimum CdS fabricated layer before and after sintering, and the results were shown in figures 6.24A and B. A peak centred at 165.5 ev is revealed in both layers. This was identified by M. Houng et al (37) as due to S^{2-} ions. However, the additional peak centered at about 172 ev only occurred for the sintered layer. Litchman et al (39) reported the formation of a thin sulphate layer with a peak around 170 ev. The second peak therefore may be the SO_4^{2-} related complex. This result is very important for Schottky analysis since it confirms the presence of an interfacial layer even in an optimum layer.

It is interesting to note here that when examining the SO_4^{2-}/S ratio after vacuum annealing the sintered layer, the ratio decreased slightly, which could mean that the chemisorbed oxygen was very strongly bonded to the surface forming the oxide compound. It is believed that the majority of this oxygen is formed during the sintering procedure as confirmed by the presence of the SO_4^{2-} peak only in the sintered layer. ESCA trials to investigate the presence of chlorine, and the suspected migration of tin were not successful.

6.3.5 XRD characterization

Preliminary trials to investigate the crystalline structure of the screen printed layers using RHEED were not successful. This is because

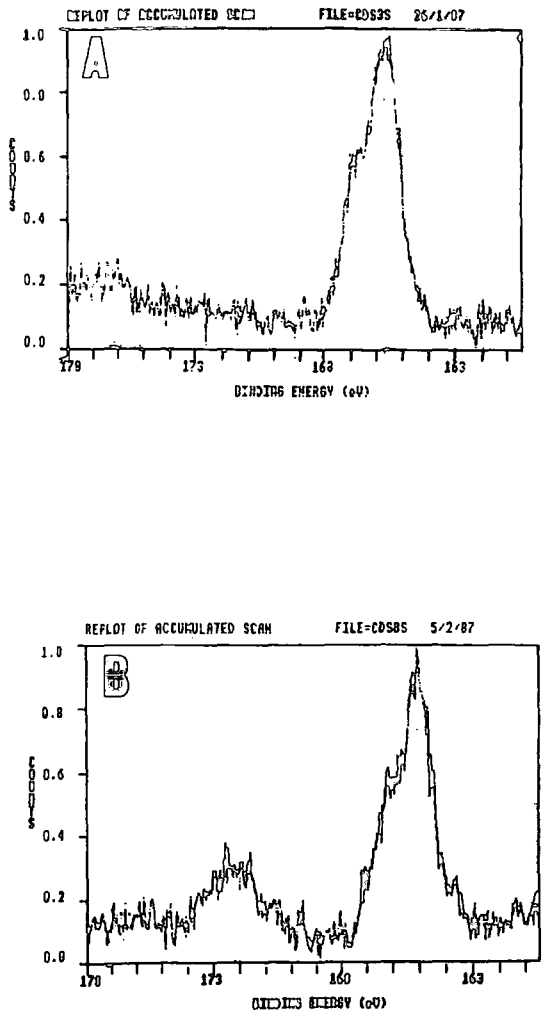


Fig. 6.24 ESCA spectra of S(2P) peaks in the high resolution scan

A : Dry CdS layer

B : Sintered CdS layer

of the rough surface which causes diffuse scattering of the electrons at the film surface (48) (20).

Consequently an X-ray diffraction technique was used to assess the crystal structure. XRD was used to examine the changes in the structure of the CdS layer following the progressive increase in the sintering temperature.

The diffraction patterns of the layers were measured using the X-ray diffractometer described in Chapter 3. The diffractometer spectra are shown in figure 6.25. The spectra of all layers exhibited three peaks at 2θ equal to 28.82, 30.80, 32.80 which correspond to diffraction from the (100), (002), (101) planes (49). These were identified as the three dominant diffraction lines of hexagonal CdS (PDF Card 6-0314).

The sequence of spectra in figure 6.25 clearly shows that as the temperature was increased progressively from 120°C a noticeable change in the X-ray diffraction pattern took place. The progressive increase in the 002 reflection in particular is a strong indication of a preferential growth of the 002 plane (32) (50), which means that the basal plane of the hexagonal system is parallel to the surface of the substrate (50), and that the C-axis of the majority of the grains is perpendicular to the substrate (51). This feature of C-axis orientation should make it possible to achieve a solar cell efficiency with polycrystalline material comparable to that of single crystal CdS (16).

The hexagonality value of the optimum layer sintered at 620° for 90 minutes calculated from equ. 3.1 (chap. 3) was 59%, which is close to the value of 62% found by S. Fu et al (32). When the sintering temperature was increased to 650°, the intensity of the 002 reflection increased slightly (figure 6.25E), but the intensity of the 101

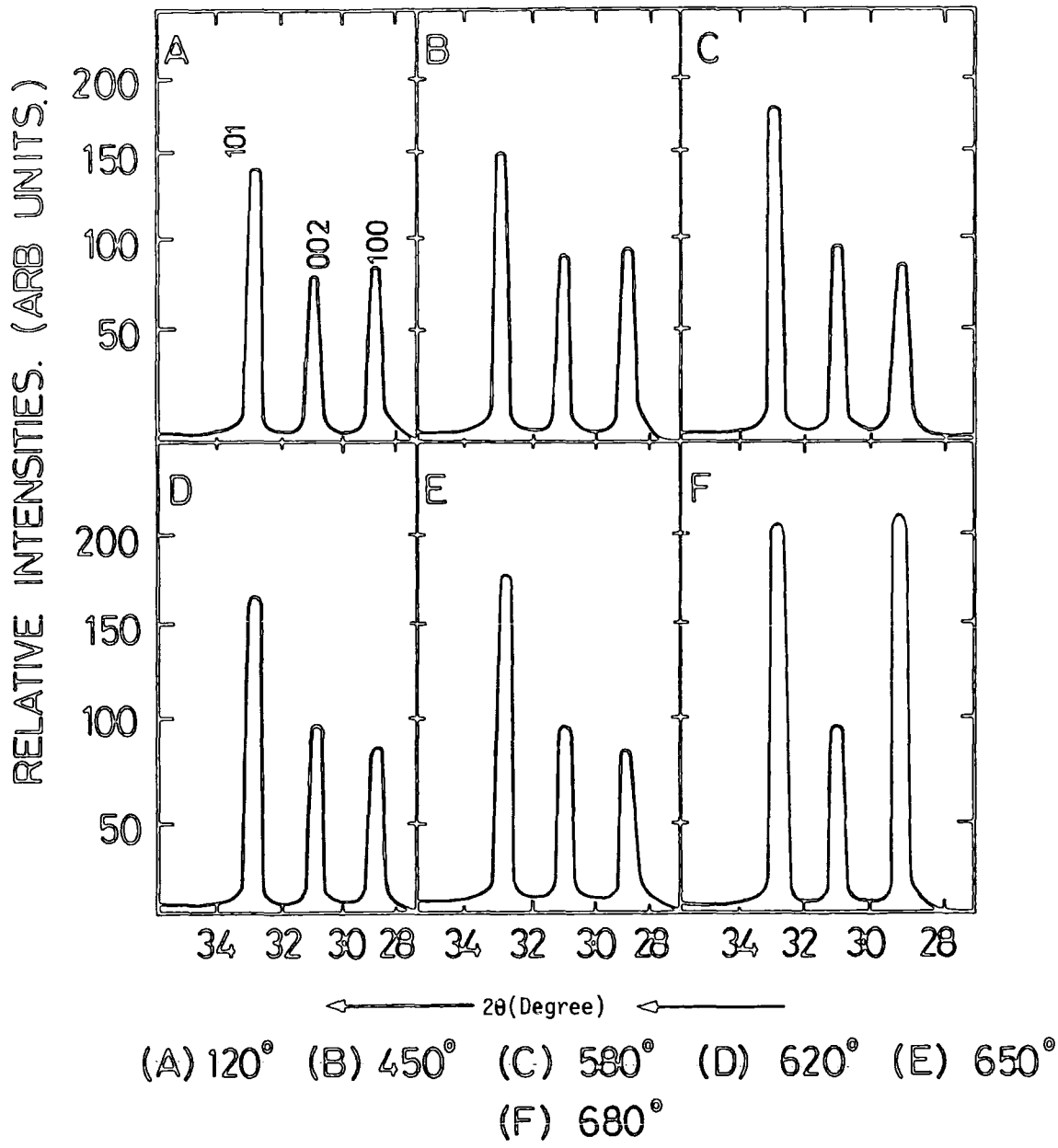


Figure 6.25 : X-ray diffraction patterns of screen printed CdS layers at various sintering temperature.

reflection increased as well. This suggests that a small number of crystallites grew with the C-axis parallel to the substrate (32). This may explain why the hexagonality value was reduced to 56%.

The change in the structure was more obvious when the sintering temperature was increased still further to 680°C (this was shown with borosilicate glass) where a significant increase of the 001 and 101 reflections was observed.

The observation that 620°C is the optimum sintering temperature for maximum hexagonality is in close agreement with the results obtained in sections 6.2.2.4 iv and 6.2.3.5 v.

6.4 Conclusion of CdS film characterization

The accumulated results obtained from the electrical and structural characterization discussed in the previous sections reflect the care needed in the fabrication of screen printed CdS layers.

Such characterization is important and will lead to a better understanding of the fabricated layer. It is a necessary step required before further junction fabrication can take place.

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CHAPTER SEVEN

SIGNIFICANCE OF THE SUBSTRATE IN THE FABRICATION OF CdS SCREEN PRINTED LAYERS

7.1 Introduction

In principle the substrate should only provide mechanical support for the deposited film and not interact with the components of the film except for the necessary adhesion. In practice however the substrate exerts a marked influence on the behaviour of the film (1).

The selection of the substrate material for screen printing of CdS layers is a very important aspect which can influence the whole process. No attention has been given to this in the literature. The significance of this choice arises because of the high sintering temperatures involved in the fabrication processes of the CdS layers.

The various requirements for the optimum choice of substrate are summarized in section 4.5.i. The properties of the substrate must be compatible with the chemical, electrical, thermal and mechanical properties of CdS. There are many possible substrates which can fulfill all these requirements, but cost presents a major obstacle. This is an important parameter since the fabrication of cheap screen printed solar cells is the final objective.

To achieve this a compromise must be reached between reasonable overall substrate properties to match those of CdS and the cost of the substrate.

Glass represents a good, low cost choice, and its application as a substrate for thick film components has long been established (2). There are of course various types of glass substrates which vary markedly in their properties. These are summarized in table (4.2).

The three substrates investigated in the previous chapter reflected such differences and showed clearly the influence of each type of substrate on the morphological and electrical properties of the deposited layers.

The purpose of the present chapter is to demonstrate this dependence more clearly by presenting a brief comparison between the optimum results achieved with the three substrate types.

It is believed that the substrate material played a major role in the appearance of the anomalous Schottky and Hall data, by affecting the complex nature of the polycrystalline screen printed layers. For example the grain boundaries are particularly sensitive to any small changes.

It will be useful to start this chapter by introducing a few concepts which are thought to be important in interpreting the anomalous results. These include i) a brief description of some properties of the substrates used, ii) the significance of grain boundaries and iii) short comments on the occurrence of stresses both in the substrate and in the deposited polycrystalline material.

7.1.1 Substrate properties

A general summary of substrate properties was presented in table (4.2). The following description will only concentrate on the most significant properties such as composition, strain, thermal expansion and thermal conductivity.

a) Composition : The major compositional consideration is the alkali content. This should be very low (3) (4) since it is known that the alkali ions are the most mobile constituents in the substrate, and they can be leached out very readily by chemical treatment (5). This leaching is more likely to be enhanced at the high sintering temperatures involved. The presence of these ions in the CdS layer

will increase the resistivity (6). The high alkali content in the substrates used, particularly in the soda lime glass suggests such contamination did take place.

b) Strain : The appearance of strain at 470°C with soda lime glass and 515°C with borosilicate glass was very undesirable because higher sintering temperatures were required. A minimum of 620°C was needed to produce the optimum layer. In general the use of glass substrates is limited to temperatures below the strain point, above which viscous flow becomes perceptible (1) (7). It is therefore recommended that the strain point should be regarded as the maximum safe operating temperature. When sintering above this temperature a great risk of permanent stress in the glass is to be expected. For example the literature of borosilicate 7740 used in this study suggests that this strain point should not be exceeded except for a short time, and at 600°C there is a danger of deformation. The situation is expected to be worse for soda lime substrates. These undesirable features may be a possible cause of the anomalous behaviour observed in some layers, especially since the strain occurred before the $CdCl_2$ flux melted at 568°, which could possibly affect the main sintering mechanism.

c) Thermal expansion : The thermal expansion coefficient of the substrate must be matched as closely as possible to the expansion coefficient of the deposited film (8). Poor matching will produce internal stress (9). W. Kingery (10) reported that high internal stress due to a substantial difference in expansion coefficients will cause boundary cracking and the appearance of micro cracks, which will have a harmful influence on the overall behaviour of the deposited layer. However, it is difficult to achieve a good match and consequently some strain should be expected in most cases.

The linear expansion coefficients of the soda lime and boro silicatate substrates used in this work are 9.5 x 10^{-6} per deg and 3.35 x 10^{-6} per deg respectively, which vary considerably from the thermal expansion of CdS of 5.8 x 10^{-6} per deg. The mismatch between both substrates and CdS is very clear, and may introduce complications in the overall behaviour as mentioned above.

d) Thermal conductivity : The thermal conductivity of the substrate is the most important factor which is relied upon to dissipate heat to the printed layer and hence has a considerable effect on the temperature distribution among the components of the layer. Therefore, a substrate with a high thermal conductivity will enable the paste based upon it to dissipate greater power.

Unfortunately, glass substrates usually have low thermal conductivity (1) (10) (11). For example, the room temperature thermal conductivity of the soda lime and borosilicate glasses used in this study were .009 W $cm^{-1}deg^{-1}$ and .018 W $cm^{-1}deg^{-1}$ respectively. This low value can be more clearly appreciated if it is compared with the high thermal conductivity of alumina of 2.7 W $cm^{-1}deg^{-1}$ (1).

In contrast, the thermal conductivity of crystalline substances whether single crystalline of polycrystalline is considerably higher than the thermal conductivity of glass (10). Thus the thermal conductivity of CdS single crystal at room temperature was measured by M. Holland (12) as .2 W $cm^{-1}deg^{-1}$. There is no reported value for the thermal conductivity of polycrystalline CdS but it is expected to be slightly lower than that of single crystals (11).

It should also be mentioned that these thermal conductivities of both glasses and the polycrystalline layer behave differently with increasing temperature. The thermal conductivity of CdS decreases fairly sharply (10) (12), whereas that of glass increases by about 10%

per 100°C temperature rise (1). Further complications are that impurities in the layer reduce the thermal conductivity markedly (13), and this reduction depends on how much they disrupt the lattice (14).

Moreover, the opening of the grain boundary cracks caused by internal stress leads to an even lower value of thermal conductivity (14).

7.1.2 Grain boundary contributions

Grain boundaries have major effects on the electrical behaviour of doped poly crystalline semiconductors in several ways : (i) They act as sinks of segregated impurity atoms or other contaminants which occur during fabrication processes (15). This will lead to a localization of impurities at the grain boundaries where they become electrically inactive (16). (ii) Because of the structure of the grain boundaries with disorder due to incomplete bonding, a large number of trapping states are produced (16). This would reduce the number of free carriers available for electrical conduction, and account for the low mobilities observed in poly crystalline materials (17) (18).

These grain boundaries become electrically charged by depleting the trapped carriers and create potential barriers surrounding the grain boundaries, and these barriers can vary significantly with the net effect of the doping concentration of the poly crystalline material and the trap density of the grain boundary (19). R. Petritz (20) introduced a simple theory which accounts for the effect of intergrain boundaries on the performance of a poly crystalline layer. In this theory the grain boundaries act as reverse biased p-n junctions with an effective barrier height (21) which controls the carrier mobility (18) (29). Large barrier heights reduce the mobility and vice versa. The dependence of mobility upon the barrier height of the grain boundaries has also been reported by many other authors (22) (23).

The barrier height depends on the fabrication conditions (19) and good control should be maintained to minimize variable properties.

7.1.3 Stress Phenomena

Stress phenomena are common in polycrystalline films. Stress should be kept to the minimum. It can be introduced in different stages of the fabrication procedure, and can be generated in both the substrate and the over layer.

1. Stresses associated with the substrate

Stresses caused by the substrate are very significant and their occurrence can be appreciated from the description of various substrate properties presented in section 7.1.1. These stresses have an impact on the grain boundaries of the poly crystalline layer since they can lead to a migration of substrate constituents at high temperature which will probably lead to their localization at the boundary regions. Also, the permanent stress which occurs when sintering above the strain point of the substrate will result in deformation of the grain boundaries. In consequence these stresses and others mentioned in Section 7.1.1 will influence the electrical behaviour of the over layer as reported by many authors (21)(24).

2. Stresses associated with the poly crystalline material

The stresses associated with the starting material are also an important factor for the following reasons:

i) The presence of impurities in the starting material can cause strain in the CdS layer during sintering (25) by evolving violent bursts of vapour, which can accumulate in the boundary region or nucleate on the surface.

ii) Another possible source of impurity is the carbon deposit (26) which can arise from incomplete burning of the binder.

The concentration of such combinations can vary throughout the sintering procedure and it can also vary with different preparation and sintering conditions. This will lead to discrepancies in the achieved results.

Stress either in the substrate or in the poly crystalline layer can have a strong influence on grain boundary behaviour. For example, the opening of grain boundary cracks due to stress will prevent the production of a good compact structure and will allow the trapping of more contamination. A possible segregation of dopant from the semi conductor material may also occur at the grain boundaries. Such changes can obviously control the properties of the layer (19).

7.2 The Optimum Condition 'A Comparison Study'

7.2.1 Introduction

The series of experiments described in the previous chapter were carried out to study the effects of various preparational and sintering parameters on the morphological and electrical behaviour of screen printed CdS layers deposited on substrate such as soda lime, borosilicate and SnO_2 coated glass.

In this section a comparison is made between the optimum results achieved using each substrate.

7.2.2 Morphological Behaviour

The typical morphology of the optimum CdS layers on soda lime, borosilicates and SnO_2 coated substrates can be seen in Figures 6.8C, 6.9B - 6.21A.

The layers sintered on soda lime and SnO_2 coated glass resulted in compact structures, while the layer sintered on borosilicate glass resulted in an inhomogeneous structure. The better growth and more compact structure of the layers on SnO_2 coated glass can be attributed to the conductive nature of the SnO_2, which would increase the thermal

conductivity and compensate for the low thermal conductivity of the soda lime glass. Although borosilicate glass has high thermal conductivity, its very low thermal expansion compared with soda lime glass (Sect. 7.1.1.c) may be responsible for the different morphologies of the layers deposited on both substrates. The high thermal expansion of soda lime glass (9.3×10^{-6} per deg.) makes a reasonable match with the thermal expansion of CdS (5.1×10^{-6} per deg.) under certain conditions, which would lead to a compact structure. This could also apply to layers deposited on SnO_2 coated glass. However, the poor morphology of layers on borosilicate, despite its higher thermal conductivity could be attributed to the different expansion between the B.S substrate and the deposited layer.

On the other hand, the cross sectional views of CdS layers on soda lime and borosilicate glass shown in Figure 7.1, reveal an interesting feature, namely that the CdS layer on borosilicate glass in Figure 7.1B indicates a fusing of the CdS grains in some parts from the surface down to the substrate, as if tending to form a monograin layer. This is a useful feature since it reduces the harmful effects of grain boundaries. It is suggested that this feature can be attributed to the relatively high thermal conductivity of borosilicate glass as compared with soda lime glass. Further confirmation of this suggestion can be found in the literature. N. Nakayam et al (3) and H. Uda et al (4) obtained a 20-30μm mono grain CdS layer by using a borosilicate glass 7095. Also, more recently M. Bohm et al (27), in their new trial of screen printed particulate silicon layer, were able to obtain a mono grain layer by using a high thermal conductivity alumina substrate for their layers.

From the above observations it is recommended that the optimum substrate should have a combination of high thermal expansion and high

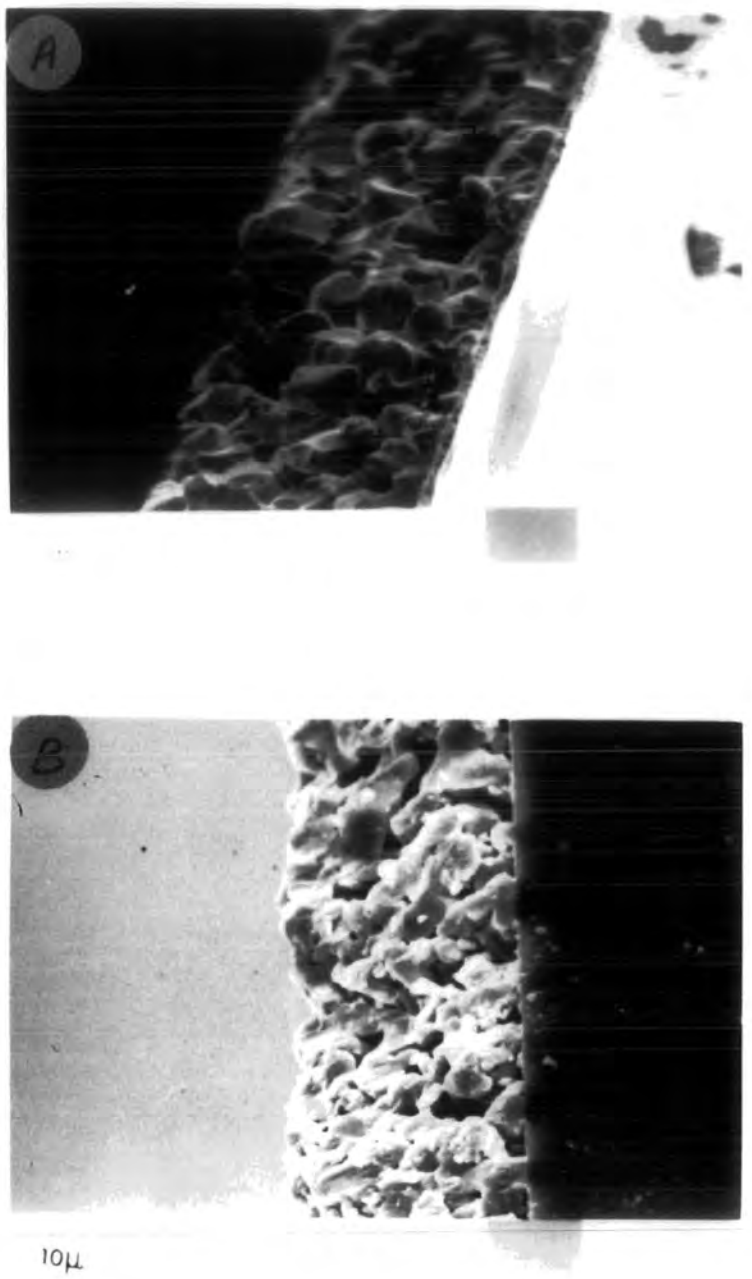

Fig. 7.1 Cross Sections of CdS Screen Printed Layer fabricated under optimum conditions.

A : SnO_2 (Soda Lime Coated) glass

B : Borosilicate glass

thermal conductivity. A similar dependence of morphology on the nature of the glass substrate and its various properties has been reported by A Vecht et al (28).

7.2.3 Electrical behaviour

The characterization of CdS layers described in Chapter 6 suggested that sintering at 620° for 90 min. was the optimum for the production of the best screen printed layer. These sintering conditions are critical, since lower or higher values resulted in poorer electrical behaviour.

Table 7.1 summarizes the resistivity variations of CdS layers deposited onto the three substrates under investigation using different durations of sintering at 620°C.

Substrate type	Resistivity (Ωcm)			
	60 min.	90 min.	120 min.	Table of results
Soda Lime	5.2	3	31	6.6
Borosilicate	.68	.44	-	6.7
SnO_2	345	177	680	6.15

Table 7.1 Resistivity variations with different sintering periods

A Graphical representation of the above data is shown in fig. 7.2.

Clearly the lowest resistivity occurred after sintering at 620° for 90 min. with all three substrate. This is thought to be due to the early appearance of strain in all three substrates. However, the lowest resistivity values were found in CdS layers on borosilicate glass, while the highest were on layers deposited on SnO_2 coated glass.

The variation of donor concentration and carrier mobility together with the resistivity variation under optimum conditions of fabrication are presented in table 7.2 for the three different substrates.

Substrate type	ρ (Ω cm)	N_d (cm^{-3})	μ ($cm^2 n^{-1} s^{-1}$)	Table of results
Soda Lime	3	$8.2\ 10^{16}$	16	6.6
Borosilicate	.44	$2.5\ 10^{17}$	38	6.7
SnO_2	177	$2.08\ 10^{17}$	.17	6.15

Table 7.2 Electrical data variation under optimum conditions

Graphical representation of the donor concentration and carrier concentration data is shown in fig. 7.3.

It is clear that CdS layer deposited on soda lime substrate represented a good combination of electrical data. The fact that the lowest resistivity and the highest donor concentration was achieved for CdS layers deposited on borosilicate glass is probably attributable to the good cross sectional structure shown in figure 7.1 B where the apparent fusing of grains would reduce the grain boundary effect and thus enhance the carrier concentrations.

The data for CdS layers on SnO_2 coated glass is very unusual regardless of the good morphological structure shown in fig. 6.21 A. The analysis of this data will be presented in section 7.4.

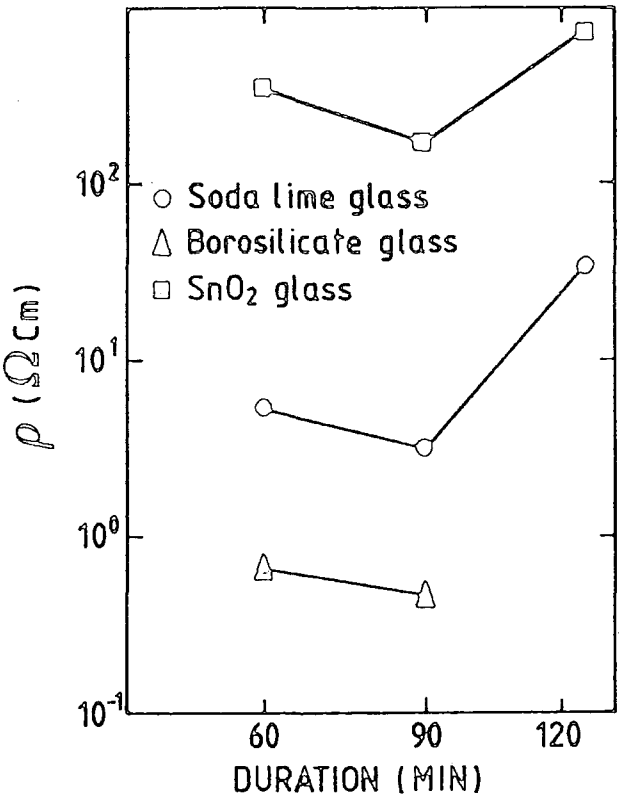

Figure 7. 2 : Resistivity Variation with Substrate Materials under various sintering temperatures

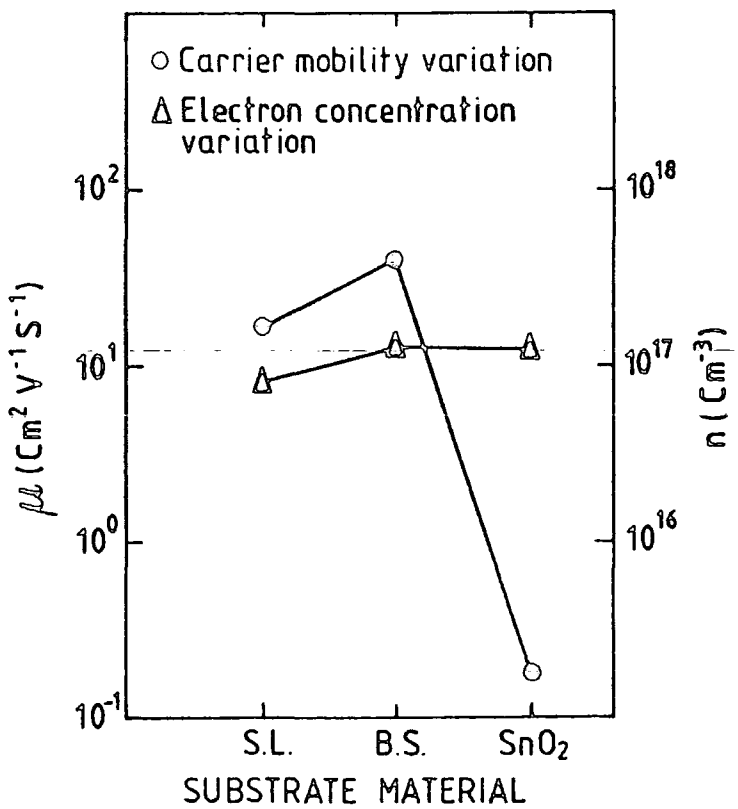

Figure 7.3 : Carrier mobility and electron concentration variations of CdS screen printed layers deposited onto various substrate materials under optimum conditions.

7.3 Analysis of results on Insulating Substrates

7.3.1 Introduction

The term insulating substrates is used throughout this study to differentiate them from the conductive SnO_2 coated glass.

This section will investigate the possible reasons for the occurrence of high mobility values for CdS layers deposited on borosilicate glass and also for some CdS layers deposited on soda lime substrate as found in section 6.2.2.

7.3.2 High mobility values

The discussion of the high Hall mobility data will be based upon the concepts introduced in section 7.1 which depended on the effect due to stress, alkali content, thermal expansion mismatch and low thermal conductivity. Stress will have a great influence upon the electrical properties of the over deposited layer, since it will lead to the opening of the grain boundary microcracks which make them preferential sites for precipitation of impurities. This will lead to the modification of the grain boundary barrier height and subsequently influence the mobility values.

A close look at the morphology of the optimum layer as shown in fig. 6.4B reveals separated grains not in intimate contact, and the grain boundary clearly distinguished. P. Pande (29) observed these boundaries more clearly using the EBIC mode in the SEM.

L. Kazmerski et al (21) and J. Wilson et al (22) used Petritz' model of electron scattering at grain boundaries in a poly crystalline film to measure the barrier height at the grain boundaries by applying the mobility expressions:

$$\mu_K = \mu_B \exp(\phi/KT) \qquad (7.1)$$

where μ_K, is the bulk mobility including the effect of grain boundaries and impurity scattering

μ_B, is the single crystal mobility

and $\emptyset$, is the barrier height at the grain boundary.

If this equation can be used to calculate the barrier height for the optimum condition case in this study, where μ_K is 16 $cm^2v^{-1}s^{-1}$ and μ_B is assumed to be 300 $cm^2v^{-1}s^{-1}$ for single crystals CdS, this gives a value of .07 eV as a measure for potential barrier height. This value is larger than the value of .048 eV reported by H. Yang et al (30) which resulted in a mobility value of 25 $cm^2v^{-1}s^{-1}$.

The above argument means that high mobility values suggest a reduction in the barrier height at the grain boundaries.

J.I. Wilson (31) found enhanced mobility values in In doped, thermally evaporated CdS layers, and also found the same increase in mobility in layers which contained excess Cd. He explained this as due to a reduction in barrier height by local excess of metal.

The precipitation of impurities at grain boundaries is more likely to occur in screen printed layers, particularly if the mixing and cooling procedure are not optimised. The presence of such precipitation will be enhanced by stresses as described above.

It is strongly believed therefore that the high mobility values are due to the reduction of the intergranular barrier height by the precipitation of impurities.

An attempt to examine the above ideas for some selected non optimum conditions which yield in high mobility would justify this further. This will be tried for the following conditions:

A. Borosilicate substrate case

The trials made to fabricate CdS screen printed layer on borosilicate substrates resulted in a low resistivity CdS layer with high donor concentrations, and abnormally high mobility values (table 6.7B). Close examination of the morphology of the CdS surface fig.

(6.9B) revealed some precipitation in the grain boundary regions. Although the composition of the precipitants could not be identified by EDAX, it is believed they increased the conductivity of the grain boundary by reducing the height of the potential barriers at these boundaries. Using Petritz' formula the barrier height was found to be .05 eV as compared with a value of .07 eV with soda lime substrates which have a carrier mobility of 16 $cm^2v^{-1}s^{-1}$. Thus it is concluded that the lowering of the barrier height led to the higher mobility value of 38 $cm^2v^{-1}s^{-1}$.

The influence of the precipitation on the mobility can be seen more clearly when considering the highest sintering temperature of 680°C used with this substrate. This led to a non homogenous structure (fig. 6.9D) and it can be clearly seen that the grains are surrounded by precipitated layers. This produced an even higher mobility of 82 $cm^2v^{-1}s^{-1}$ due to a reduction in the barrier height to .03 eV from .05 eV.

B. Sintering temperature and duration

The differences in mobility values obtained with increasing temperature and/or the duration of sintering as shown in tables 6.5 and 6.6, suggest that complex changes take place during sintering. For example, the stoichiometry, grain size, segregation of dopant impurities, and evolution of contamination changes throughout the process. As a result, the behaviour can vary at any specific stage until the optimum condition is reached.

At the first stage of sintering, a significant amount of volatile compound will start to be driven off, such as the binder burning components and other contaminants. Also, $CdCl_2$ starts to volatize at 400°C and continues to do so until it is completely volatized at 600°C.

The voltization products should find their way out to the exhaust. However, since early strain can occur in the glass even at a temperature lower than the melting point of $CdCl_2$ (568°C), considerable disturbance will occur, which will affect the smoothness of the above distillation process, and will lead to some precipitation of impurities in the open grain boundary regions, instead of being driven off completely.

It is suggested that this effect is responsible for the lowering of the barrier height at the grain boundary causing an increase in the carrier mobility.

At the optimum condition of 620°C for 90 min. it is believed that a balance occurred between the substrate and the deposited CdS layer, and most of the precipitations were then driven off. However, further increase in the temperature and/or duration would disturb the balance again, probably by the out diffusion of chlorine and the segregation of cadmium as shown in fig. 6.8D.

C. Post sintering annealing

Post sintering annealing was undertaken in an attempt to improve the electrical and morphological properties of a near optimum layer, fig. (6.8A) table (6.6A). Although the morphology improved markedly fig. (6.10), the mobility values increased anomalously (table 6.8). This is again thought to be a grain boundary effect, where post annealing in hydrogen or vacuum disturbed the optimum balance.

It is interesting to note that although the post annealed structure shown in fig. 6.10 appeared compact, it is clear that the grains are not in intimate contact providing favourable intergranular regions for possible impurity precipitation.

D. Other non-optimum conditions

A similar explanation of high mobility values due to the lowering of intergranular barriers by the precipitation of non desirable impurities, can also be applied to other conditions shown in tables 6.1, 6.3 and 6.4.

However, an important observation should not be omitted. This concerns the two conditions of an open envelope and a fast flow rate discussed in sect. 6.2.2.5ii-iii. These two, although non-optimum for producing screen printed CdS layers, due to the poor morphology as shown in figs. 6.5C and 6.5F, nevertheless led to normal mobility values of 11 $cm^2v^{-1}s^{-1}$ and 16 $cm^2v^{-1}s^{-1}$ respectively, which are comparable with the optimum value of 16 $cm^2v^{-1}s^{-1}$ obtained.

The nature of these two conditions suggests that direct evaporation of the $CdCl_2$ occurs in an open envelope configuration, while with a fast flow, chlorine will be driven off before its complete utilization to form donors. It may be that some of the precipitated impurities in the grain boundary regions are chlorides. This can perhaps be justified when considering the covered envelope and the slow flow rate conditions, which yield high mobility values of 111 $cm^2v^{-1}s^{-1}$ and 53.8 $cm^2v^{-1}s^{-1}$.

However, the presence of other sources of contamination in the layer, for example, carbon residue from the binder, alkali ions from the substrate and contamination from the starting powder, suggest that more than one type of impurity is precipitated in the grain boundary, which could be driven off quite readily in open envelope or fast flow conditions.

Although, it could be argued that these are desirable conditions, since all the contamination would be driven out, the fact that the $CdCl_2$ is also driven out, judging from the poor morphology and higher

resistivity, is very undesirable. Therefore, a compromise has to be made to preserve the required amount of $CdCl_2$, regardless that some contamination would still remain in the boundary regions.

7.3.3 Conclusion

It is worth mentioning here that in addition to the high mobilities, there is evidence that in some cases the mobility does vary with grain size and donor concentration as reported by many authors (17) (30), which is regarded as normal. This is apparent from the use of two flux ratios shown in fig. 6.3 and table 6.2. CdS layers which used 7% $CdCl_2$ had a grain size of 2-4 μm and a donor concentration of $6.18 \times 10^{16} cm^{-3}$, with a mobility of 6 $cm^2 v^{-1} s^{-1}$. Increasing the $CdCl_2$ ratio to 10% resulted in a layer grain size of 8-10 μm and a higher donor concentration of 8.2×10^{16} cm^{-1}, with an increased mobility of 16 $cm^2 v^{-1} s^{-1}$.

7.4 Analysis of results on SnO_2 Coated Substrates

7.4.1 Introduction

Conductive coated substrates have been used extensively in solar cells. They are usually applied as optically transparent electrodes, as antireflective coatings (AR), or as a major component part of hetrojunction solar cells (32). Of particular interest are SnO_2, InO_3, ITO and ZnO coated substrates, which are those most frequently used.

Recently interest in SnO_2 substrates has been revived because of their prospective application in photovoltaic solar cells (33). SnO_2 films exhibit a wide band gap of 3.87 - 4.3 ev (34). The most popular methods for the deposition of SnO_2 coatings are chemical vapour deposition, spray pyrolysis and sputtering onto soda lime or borosilicate glass. The SnO_2 coatings used in this study were deposited by spray pyrolysis onto soda lime glass, and had a thickness of .1μm.

SnO_2 substrates have been used as AR coatings (35). SnO_2 has also

been used as a back contact layer (36). However, its major application is as a main component in silicon (single crystals, polycrystalline and amorphous) solar cells (37-41), and also in GaAs and Ge heterojunction devices (42).

With CdS solar cells, SnO_2 is often used as a back electrode (43-47). However, the use of SnO_2 coatings with screen printed CdS layers has not been reported. Preliminary work used other conductive coatings (48-50), which were unsatisfactory because of shorting problems (51).

SnO_2 substrates were used in this study to test the usefulness of screen printed CdS layers for solar cell fabrication, by forming simple Schottky diodes on the layers. However, the results obtained were very anomalous and raised many questions about the validity of such a substrate for solar cell applications. In the following section the reasons for this will be discussed.

7.4.2 Anomalous results

The first measurements of CdS layers deposited onto SnO_2 coated glasses revealed that they were high resistivity layers. This is unusual since the reverse effect was expected, because of the presence of the conductive coating.

The Schottky data were summarized in tables 6.9-6.17 and these reveal anomalously low mobility values, with unexpectedly high donor concentrations considering the high resistivity values. For example, the donor concentration of the best CdS layer deposited onto SnO_2 glass was $2.07 \times 10^{17} cm^{-3}$, which is high compared with the resistivity of 177 Ωcm. A similar high donor concentration in a single crystal would have led to a resistivity of approximately .1 Ωcm.

Similar abnormal electrical behaviour using SnO_2 substrates was reported by P. Pande et al (23). They obtained a high resistivity value of 600 Ωcm for a CdS layer deposited electrophoretically onto

SnO_2 coated glass. They found a donor concentration of 2.7×10^{16} cm^{-3} and a mobility of .38 $cm^2v^{-1}s^{-1}$, which they attributed to the presence of high potential barriers at the grain boundaries with a height of .14 eV.

The barrier height for the best screen printed layer on SnO_2 glass in this study, which had a resistivity of 177Ω cm and a mobility of .17 $cm^2v^{-1}s^{-1}$, was found to be 0.18 eV using Petritz's formula (7.1). This value is substantially higher than that of 0.07 eV for the optimum CdS layer on soda lime glass.

Since there is no report about the way which the conductive SnO_2 substrate surface might interact with CdS layer, the following discussion will attempt to investigate this in some detail.

i) Reaction between SnO_2 and CdS

A reaction with the SnO_2 layer was reported to occur in amorphous silicon solar cells (52) (53). The main reaction products were tin in metallic form and SiO_2, despite the low temperature used in the fabrication. A chemical reaction is more likely to occur between SnO_2 and CdS because of the high sintering temperatures used. Cumberbatch et al (7) (44) indicated that high sintering temperatures with this type of substrate are not recommended, since the glass will soften considerably and permit viscous flow. Their observation can also suggest the presence of a reaction between the CdS layer and the SnO_2 substrate possibly in the form:

$$CdS + SnO_2 \longrightarrow Cd + Sn + SO_2\uparrow$$

ii) Migration of metallic species

Although SnO_2 will only decompose at the very high temperature of 1850° (54), the possibility of the migration of the constituents of SnO_2 layer is very likely to occur. The migration of metallic species

into the over coated layer has been reported by many authors (55) (56). The migration of O_2 and Sn from SnO_2 must therefore be considered.

a. O_2 migration

The suggestion of O_2 migration may be a little confusing due to the unavoidable presence of O_2 in the screen printed CdS layer, either at the surface or in the grain boundary, as discussed in the previous chapter. However if more O_2 is introduced into the CdS from the SnO_2 coated layer, its effect will be to reduce the donor concentration either by filling the native S vacancies at the surface (57) (58), or by introducing a high density of surface states if it is trapped in the grain boundaries. This will reduce the mobility (59) and result in a lower donor concentration (58).

b. Sn migration

There is strong evidence from the literature to suggest that the metallic species of the conductive substrate migrates into the over coated layer. For example, S. Naseem et al (60) observed tin migration from ITO into an over coated sputtered InP layer, and they reported this to cause an inversion type in the InP layer. A. Saidane et al (55) also found a segregation of tin from ITO substrates into thermally evaporated ZnSe.

The above examples involved the segregation of Sn from ITO which is less stable than SnO_2. However, very recently, Cumberbatch (7) found some evidence for Sn migration into CdS layers on SnO_2 which had been heated to 550°C.

The next questions to be answered are: 1) where does the Sn go inside the material? and 2) what is its influence upon the behaviour of the layer?

First, the diffusion of Sn will take place along grain boundaries, where it will accumulate. For this assumption to explain the observed

results, the Sn should increase the trap density at the grain boundary and increase the barrier height. This would explain the low mobility values but would not explain the high donor concentration value. A second possibility is that tin may dope the CdS. This has much supporting evidence from the literature.

Several workers have deliberately doped II-VI compounds with Sn (61) (62). Y. Mita (62) doped ZnS with Sn and he concluded that this element is electrically active and substitutes for Zn. Also, H. Tuboto et al (61) used Sn to dope CdSe in order to decrease its resistivity. Fahrenbruch and Bube (63) indicated that CdS is easily doped n-type with Sn which forms shallow donors.

It is suggested therefore that Sn replaces host Cd atoms and donates two free electrons to the conduction band. This seems a reasonable possibility since the atomic radii of Sn and Cd are 1.4A° and 1.48A° respectively (61).

In conclusion, the above arguments suggest that, Sn doping is the most probably cause of the anomalous results of CdS layers deposited onto SnO_2 substrates.

7.5 Final Remarks

The chapter will be concluded by presenting two important remarks which are closely related to the scope of the present work. These involve the optimum substrate choice for screen printing and the high sintering temperature requirement in the fabrication processes.

7.5.1 Optimum substrate choice

In view of the above discussion of the anomalous results with both insulating and conductive substrates, a more precise picture can be obtained for each substrate used, from which the optimum choice of substrate for screen printing can be recommended.

A renewed examination of the three substrates suggests the following for the possibility of each of them as candidates for screen printing applications.

a. Soda Lime substrates

The unusual high mobility value achieved by using this substrate is largely attributed to the complexity associated with the occurrence of early strain of this glass at 470°C, in addition to its high alkali content. These form two major obstacles for the successful utilization of this substrate type for efficient screen printed layers of CdS.

b. Borosilicate substrates

Although borosilicate type 7740 has a higher strain point of 520°C, this is still low for CdS screen printing applications. Another major problem of this substrate is its low thermal expansion which has an adverse influence on the electrical and morphological behaviour of CdS layer. The relatively higher thermal conductivity of this substrate is advantageous in producing a better cross sectional layer and would probably have a marked influence if this glass had a better thermal expansion matching with the over coated layer.

c. SnO_2 coated substrates

Initial observations of CdS layers deposited on SnO_2 substrates would not encourage further use of these substrates. This is because of the darkish appearance, and the bad adhesion of the sintered CdS layers. Moreover, the anomalous results for all screen printed layers deposited onto these substrates would further support the above suggestion.

In view of the above observation the following recommendation can be made for the optimum choice for screen printed layers of CdS.

1. Avoid using conductive substrates because of the uncertainty associated with the migration of the metallic species.

2. Choose an inert insulating glass which should have the following features.

   . a high strain temperature above 600°C. For example, the strain temperature for B.S. 7095 (which is mostly used for screen printed CdS layers) is 613°C.

   . a very low alkali content

   . a high thermal conductivity for more heat absorption

   . proper thermal expansion matching with CdS layer.

7.5.2 Substrate Vs. sintering temperature

From the economic point of view a low sintering temperature is desirable to save energy. In the fabrication of screen printed CdS layer, however, there is a minimum temperature which must be employed to produce an optimum layer and the maximum temperature can vary with varying fabrication conditions.

It is known that a minimum temperature of 568°C is needed to melt $CdCl_2$ and form a molten solution to dissolve the surfaces of the high melting CdS grains. However, the presence of a $CdCl_2$ residue is not desirable after the completion of the sintering processes. In general, $CdCl_2$ starts to volatilize at 400°C and is completely volatilize at 600°C. This would put a maximum temperature of 600°C for complete removal of $CdCl_2$. However, this is not always the case, because the necessary very constrained sintering envelope configuration needed for proper sintering will allow a high percentage of chlorine ions to remain, probably by trapping of the grain boundaries. This will imply raising the sintering temperature above 600° to ensure the complete removal of any undesirable $CdCl_2$ residue. The Japanese workers found more chlorine remained at 630°C after using a very constrained envelope (64). Consequently they employed a sintering temperature of 690°C to ensure that a minimum of chlorine remained. However, the Korean

workers reported 650° as their optimum temperature. Although they found complete growth occurred at 620°C (30), the lowest resistivity occurred at 650°C.

These temperatures are too high to be employed in our work, mainly because of the early strain in our substrates. The Japanese used a high quality substrate, B.S. 7095, to meet their sintering requirement. The Koreans did not specify quality of their B.S. substrate but it is believed to be of inferior quality to 7095.

The fact that very little chlorine remained in most sintered layers in this study, even at temperatures below 600°C is largely attributed to the non ideal sintering envelope (6.2.2.5ii) which allowed a relatively fast evaporation of $CdCl_2$ at the early stages of sintering.

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CHAPTER EIGHT

CdS/CdTe SOLAR CELLS

8.1 Introduction

In chapter 6 the suitability of CdS screen printed layers for solar cell fabrication was discussed and in this chapter attempts to fabricate solar cells on screen printed CdS layers are described.

Although various junction combinations have been reported to produce photovoltaic cells on screen printed CdS layers (1-5), the best one was the CdS/CdTe structure fabricated entirely by screen printing processes (5).

The fabrication of a cell of this type ideally requires a thorough characterization of the CdTe screen printed layer to optimise the efficiency of the cell, but this promises to be lengthy. Therefore a new structure has been investigated utilizing thermal evaporation to fabricate the CdTe part of the cell structure.

This method was chosen from the point of view of simplicity of preparation.

Following the recommendations made in Chapter 6, optimum CdS layers were prepared on soda lime glass to give the best electrical and morphological characteristics for the fabrication of solar cells.

All the CdTe layers were prepared in a conventional vacuum evaporation system as described in sect. 3.4.2.i. The starting material was high purity CdTe, which was evaporated from a quartz crucible at temperatures between 780° and 980° in a vacuum of the order of 1×10^{-5} torr. The evaporation rate was adjusted from 1.5 to 2.5 μm/min by controlling the crucible temperature.

This chapter will start by introducing some preliminary work in section 8.2 followed by optimization studies of the CdTe evaporated

layer in section 8.3. In section 8.4 the influence of variously prepared CdS screen printed layers will be described, with the aim of correlating the photovoltaic properties of the cell with the method of fabrication of the screen printed layer. In section 8.5 a general discussion of some of the features apparent in this new structure will be presented.

8.2 Preliminary Studies

8.2.1 Mode of illumination

In heterojunction solar cells, two modes of illumination are possible; the front wall configuration, where the light is incident through the thin layer of the smaller band gap absorber material (i.e. CdTe), and the back wall configuration where the light is incident through the large band gap window material (i.e. CdS).

The preliminary trials made to investigate the optimum mode of illumination are shown in fig. 8.1A. The photovoltaic behaviour under AM1 illumination using both modes revealed the back wall configuration to be the best mode. This produced higher values of short circuit current (S.C.C.) of 0.65 mA and open circuit voltage (O.C.V.) of 0.36 V as compared with 0.2 mA and 0.26 V for S.C.C. and O.C.V. values respectively for the front mode configuration.

The reason for this improvement is obvious since in the front wall configuration, most of the electron-hole generation will occur close to the CdTe surface because of the high absorption coefficient of CdTe (6) (7). Then the short diffusion length of minority carrier (6) means that most of the recombination occurs near the top surface before the carriers reach the junction. On the other hand, in the back illumination mode, the region of the maximum photo carrier generation is displaced away from the CdTe surface (8), and the absorption takes

place close to the CdS/CdTe interface, where maximum photo carrier collection occurs.

It should be noted that the nature of the CdS surface will affect carrier transport due to the presence of grain boundaries (9) (10) which can trap minority carriers. However, the increased number of effective photons transmitted by the window material, and the high resistivity of the CdTe material (see later), which enhances the surface recombination, ensure that the back wall mode is superior to the front wall mode in these cells.

8.2.2 Annealing temperature

Various annealing temperatures between 250° and 350° were tried to investigate the best temperature for diffusing the Cu dopant (section 2.2.1.i) into the CdTe layer in order to lower the resistivity of the P-type layer.

The J-V characteristics of the two devices annealed at 250° and 350° are shown in fig. 8.1B, together with the characteristic of an unannealed device for comparison. It is clear that the optimum behaviour was found when the device was annealed at 350°C, giving a S.C.C. of 2 mA and an O.C.V. of 0.53 V. This compares with a S.C.C. of .8 mA and O.C.V. of 0.32 V for the device annealed at 250°C. The unannealed device showed a very poor S.C.C. (0.4 mA) and O.C.V. (.2 V), which is to be expected, since the evaporated copper has not then diffused into the highly resistive CdTe layer. This study indicated the necessity of annealing the Cu doped device to drive the dopant into the layer. It also revealed the importance of the correct annealing temperature to ensure proper diffusion.

Trials to anneal the device at high temperature (e.g. 400°C) resulted in a high series resistance of the device and produced inferior photovoltaic behaviour.

8.2.3 Annealing Ambient

A vacuum ambient of 10^{-5} torr was chosen for the post annealing treatment in view of the possibility of introducing additional P-type doping by creating Cd vacancies, which result from the different vapour pressures of Te and Cd. Cadmium vacancies are reported to act as acceptors (11-14) and help in reducing the resistivity of the CdTe layer.

The behaviour of two devices annealed for comparison in argon and in vacuum are shown in fig. 8.1C. The vacuum annealed device had higher values of S.C.C. (2 mA) and O.C.V. (0.53 V), in comparison with 1.7 mA and 0.47 V for the argon annealed device.

An additional possible advantage of vacuum annealing is the creation of an excess of tellurium on the surface as a consequence of the cadmium vacancies. This feature would lead to a lower contact resistance (14) because the heavily doped region adjacent to the contact metal would permit easy tunneling (15).

8.2.4 Contact Problem

Various aspects of ohmic contact formation to P-type CdTe were reviewed in sect. 2.2.2iii. The two metals mostly employed nowadays to achieve a reasonably ohmic contact to P-type CdTe are gold (Au) and carbon (C). However, both materials still have considerably lower work functions of 5.1 ev and 5.05 ev (16) than that of CdTe which is 5.9 ev (17). The normal procedure followed to over come this mis-match problem, and obtain a barrier free contact necessary for a good ohmic behaviour, is to dope the CdTe heavily under the contact to promote easy tunneling (15) (17) (18). For carbon contacts this was done by incorporating the copper impurities in the carbon paste and then heating to produce the needed P^+ layer (19). With the Au contact this layer was provided by producing a Te rich surface under the contact.

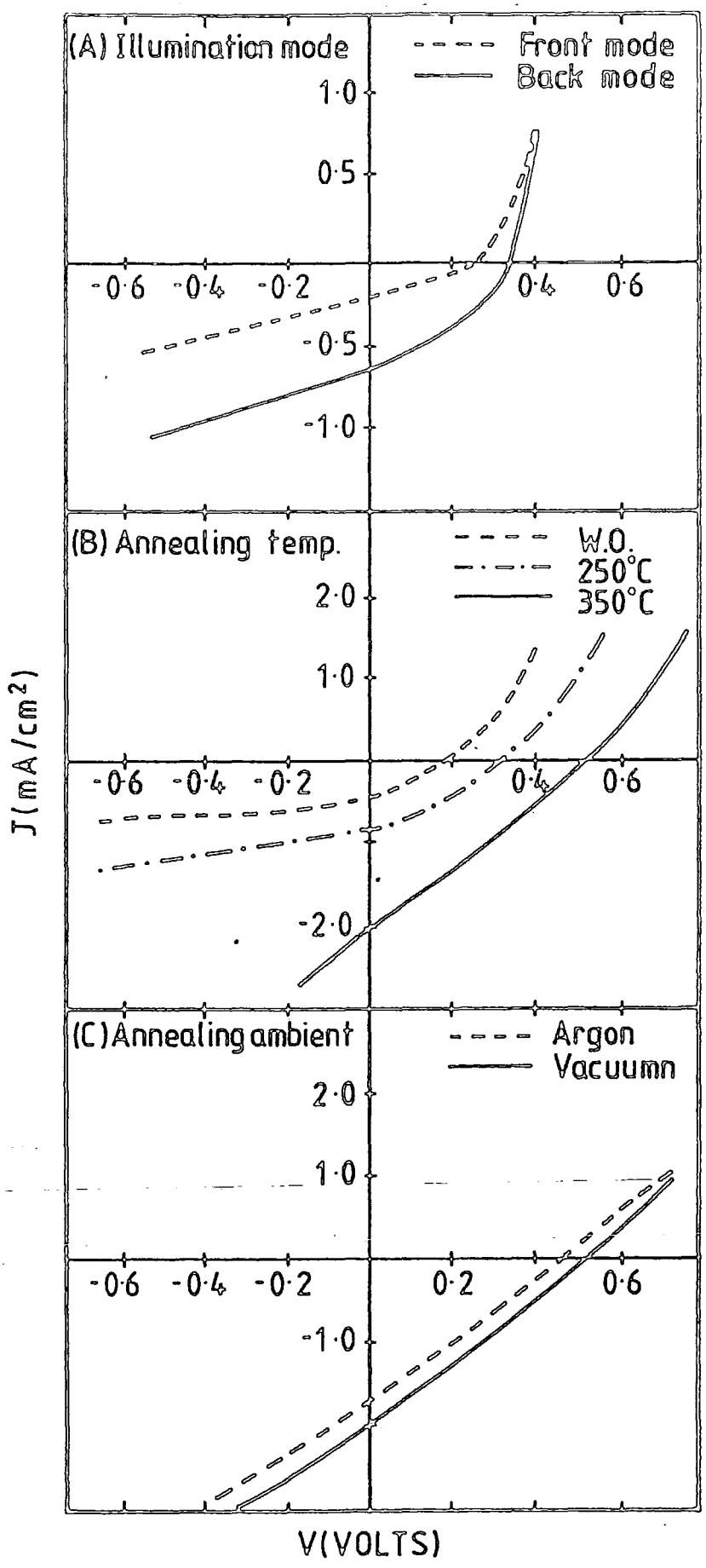

Fig. 8.1 J-V Characteristics of CdS/CdTe Hetrojunction under various conditions.

In this work, trials of carbon contacts were unsuccessful and led to junction deterioration following the heating required for Cu diffusion. This may have been due to the introduction of some contamination from the carbon paste, such as Al (20), into the CdTe during the heat treatment which would increase the series resistance.

As a result, gold was employed as the contact material for all CdTe evaporated layers.

8.3 Optimization of CdTe layers

8.3.1 Substrate temperature

The influence of the substrate temperature at which the CdTe is deposited is very significant in controlling the behaviour of the resultant layer (10) (13) (21) and the subsequent performance of the fabricated device.

Two substrate temperatures were tried, 150°C and 200°C (here the term substrate refers to the screen printed CdS layers upon which CdTe was evaporated to form the hetrojunction). The photovoltaic behaviour under AM1 illumination of the devices fabricated at the two substrate temperatures are shown in fig. 8.2.

It is clear that the best values of S.C.C. of 5.6 mA and O.C.V. of 0.51 V were from the device produced using a substrate temperature of 200°C. The device made at 150°C produced lower values of S.C.C. (1.9 mA) and O.C.V. (0.48 V).

The spectral responses of the O.C.V. of the two devices are shown in fig. 8.3. The device manufactured using a substrate temperature of 200°C gave the highest response, while that using a temperature of 150°C was less sensitive in the short wave length region (high energy region). Both devices showed a low energy threshold at 0.85 ev, well below the energy of the CdTe band gap (1.5 ev), with the high energy response extended to energies slightly greater than that of CdS band

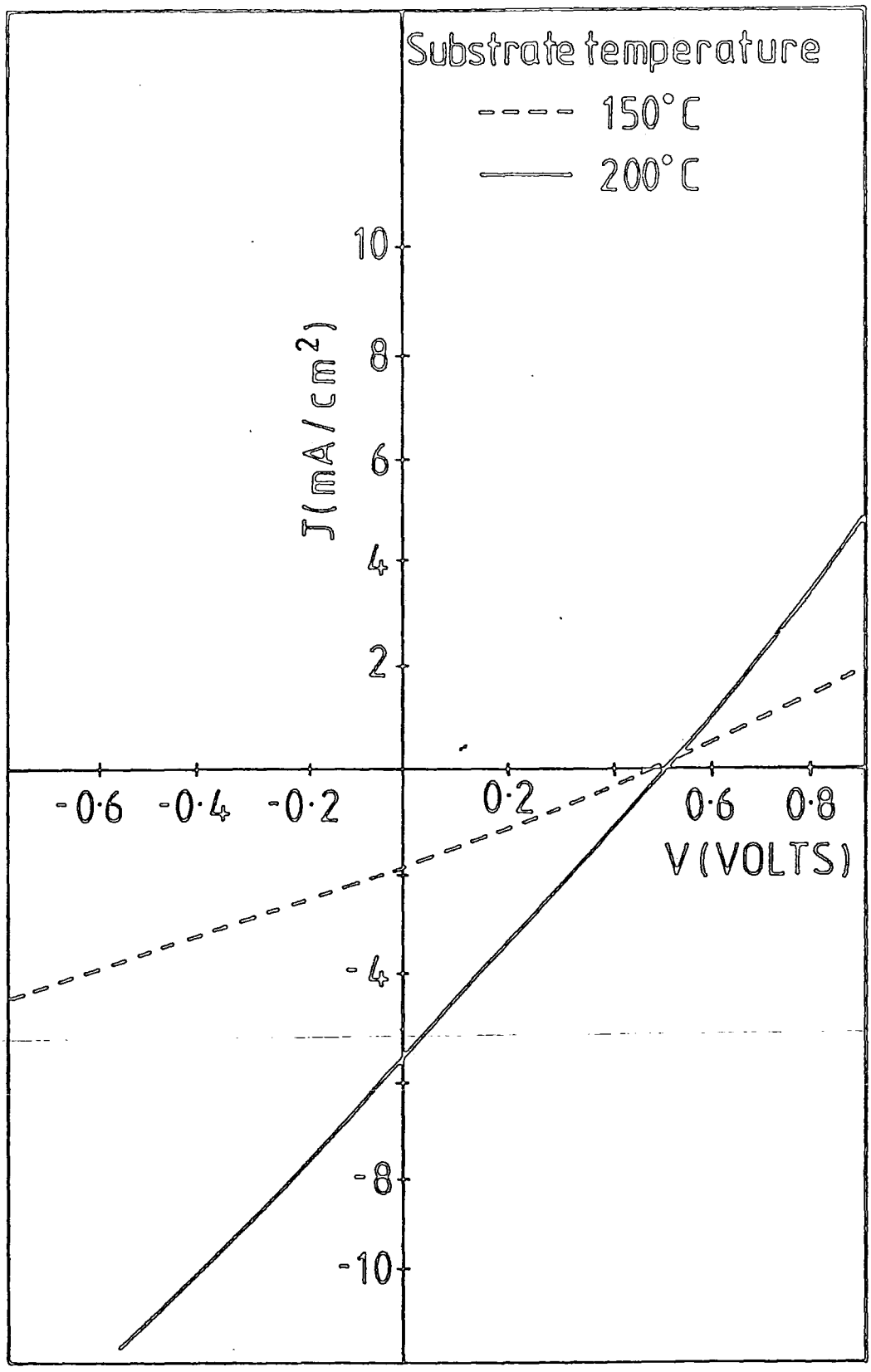

Fig. 8.2 : Photovoltaic behaviour of Hetrojunction using different CdTe layers.

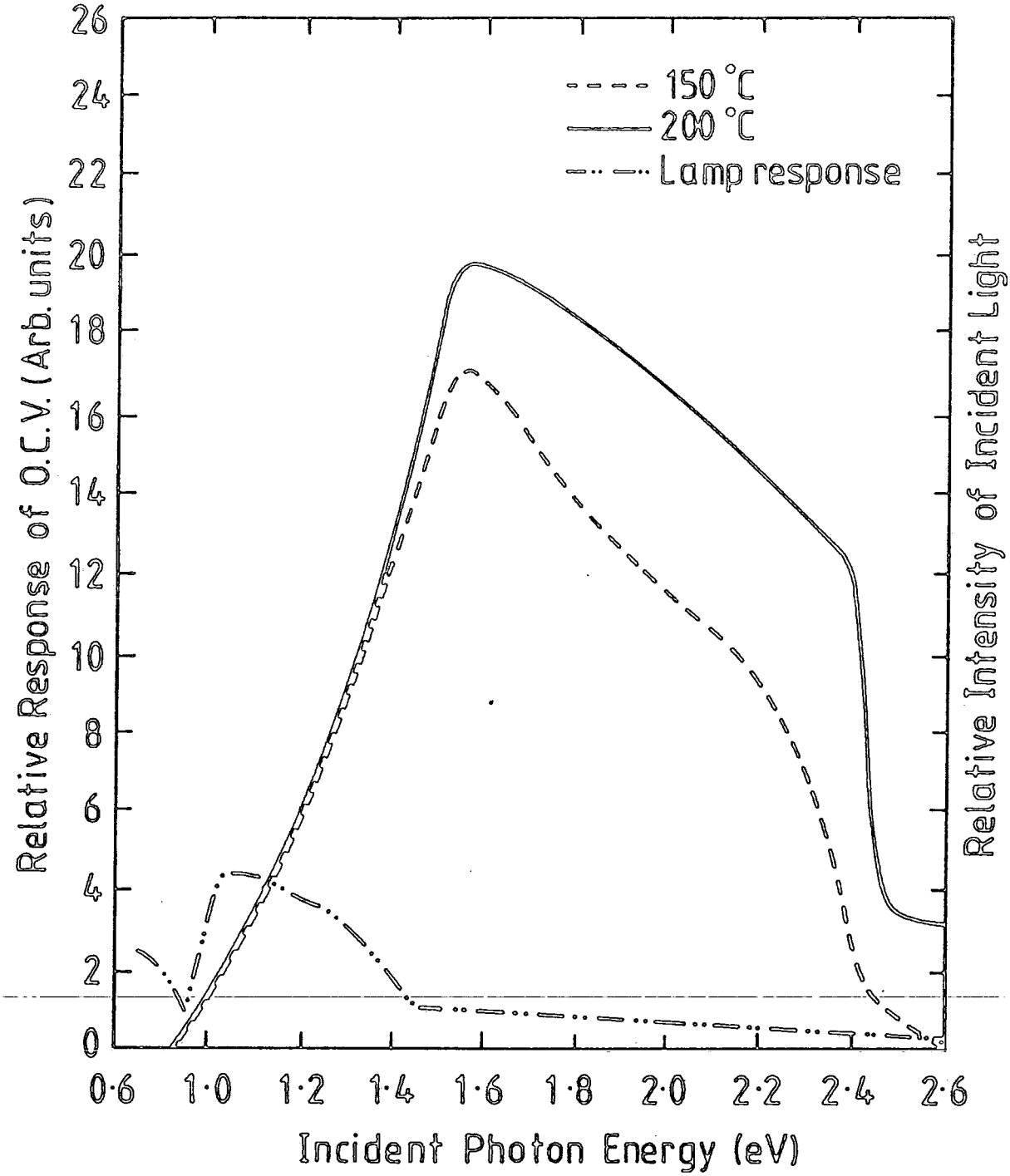

Fig. 8.3 : Open circuit voltage spectral response of CdS/CdTe Hetrojunctions using different CdTe layers.

gap (2.4 ev). The possible reasons for the occurrence of these features will be discussed in section 8.5.3. The maximum peak response of the two devices was close to the band gap of CdTe (1.5 ev).

In order to understand the superiority of the device produced using 200°C as the substrate temperature, an attempt was made to observe the structure and crystallinity of the evaporated CdTe layer using RHEED. However, this was not successful because of the roughness of the underlying screen printed CdS, which affected the deposited CdTe layer and caused diffused scattering. As a result, representative RHEED pictures were taken for CdTe layers deposited onto plane glass located very close to the CdS substrates, these are shown in fig. 8.4 for the two temperatures employed in this study.

The superiority of the higher substrate temperature in producing better crystallinity is very obvious from the smaller arc width (10) which indicates preferred orientation. Similar structures for CdTe layers deposited at 200°C were found by G. Awan (10) to display good columnar growth when examined by SEM. Such layers are very useful in solar cell devices, since the charge carriers can flow down the columnar crystallites without crossing grain boundaries which results in better photovoltaic behaviour.

The columnar growth was less evident with the 150°C layer with a greater proportion of randomly orientated material. This implies that the carriers would have to cross different crystallites during transport, which would lead to increased recombination losses and poor photovoltaic behaviour.

If the structures on the plane glass, shown in figs. 8.4A and B, are replicated on the CdS printed layers, then the above observations by Awan would explain the performance of the two devices shown in figs. 8.2 and 8.3, i.e. the good photovoltaic performance of the 200°C device

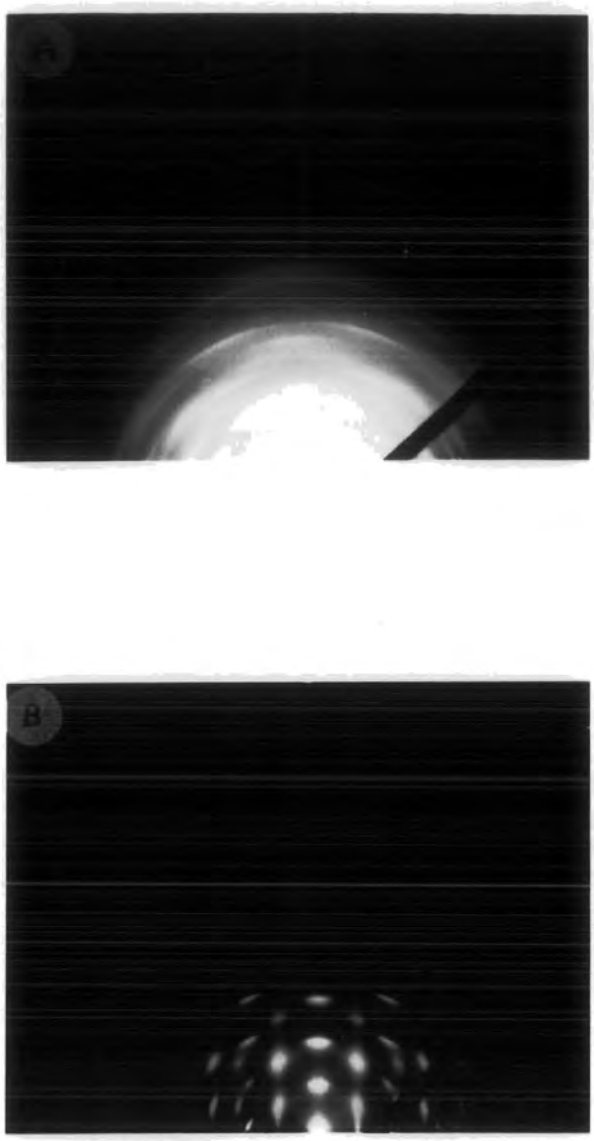

Fig. 8.4 RHEED Pattern of CdTe films deposited at different substrate temperatures

A : 150°C
B : 200°C

would be attributed to the good columnar growth of the CdTe layer deposited at 200°C, while the poorer photovoltaic performance of the 150°C device would be attributed to poor columnar growth.

8.3.2 The importance of doping

The as-deposited CdTe layer had a high resistivity of the order of $10^6 \Omega$ cm, which is not suitable for photovoltaic power conversion. Doping with elemental copper is one of the various methods (section 2) employed for reducing the resistivity by introducing acceptors into the layer as has been demonstrated by many workers (10) (11) (22-24). The actual doping mechanism and procedure is described in sect. 2.2.2ii and sect. 3.4.2ii respectively. Judging the literature (10) (25) only two doping concentrations were tried here, 100 ppm and 300 ppm. Fig. 8.5 shows the photovoltaic behaviour of two devices doped with the above concentrations of Cu. The behaviour of an undoped device is shown for comparison.

It is apparent that the undoped device has a high series resistance, and shows a poor photovoltaic behaviour. The S.C.C. value was 0.075 mA with an O.C.V. of 0.26 V. However, by using 100 ppm Cu the behaviour improved considerably, and the S.C.C. and O.C.V. reached values of 1.55 mA and 0.38 V respectively. By increasing the Cu concentration to 300 ppm, these parameters improved further to give higher values of 5.6 mA and 0.51 V.

The spectral responses of the devices doped with 100 ppm and 300 ppm Cu are shown in figure 8.6, together with the data for an undoped device. The peak of the poor response of the undoped device was shifted toward higher energies (1.69 ev) compared with the band gap of CdTe. A substantial improvement was obvious with both doped devices. The two responses show some similarity in shape, although the magnitude of the response was greater for the 300 ppm Cu doped device. With the

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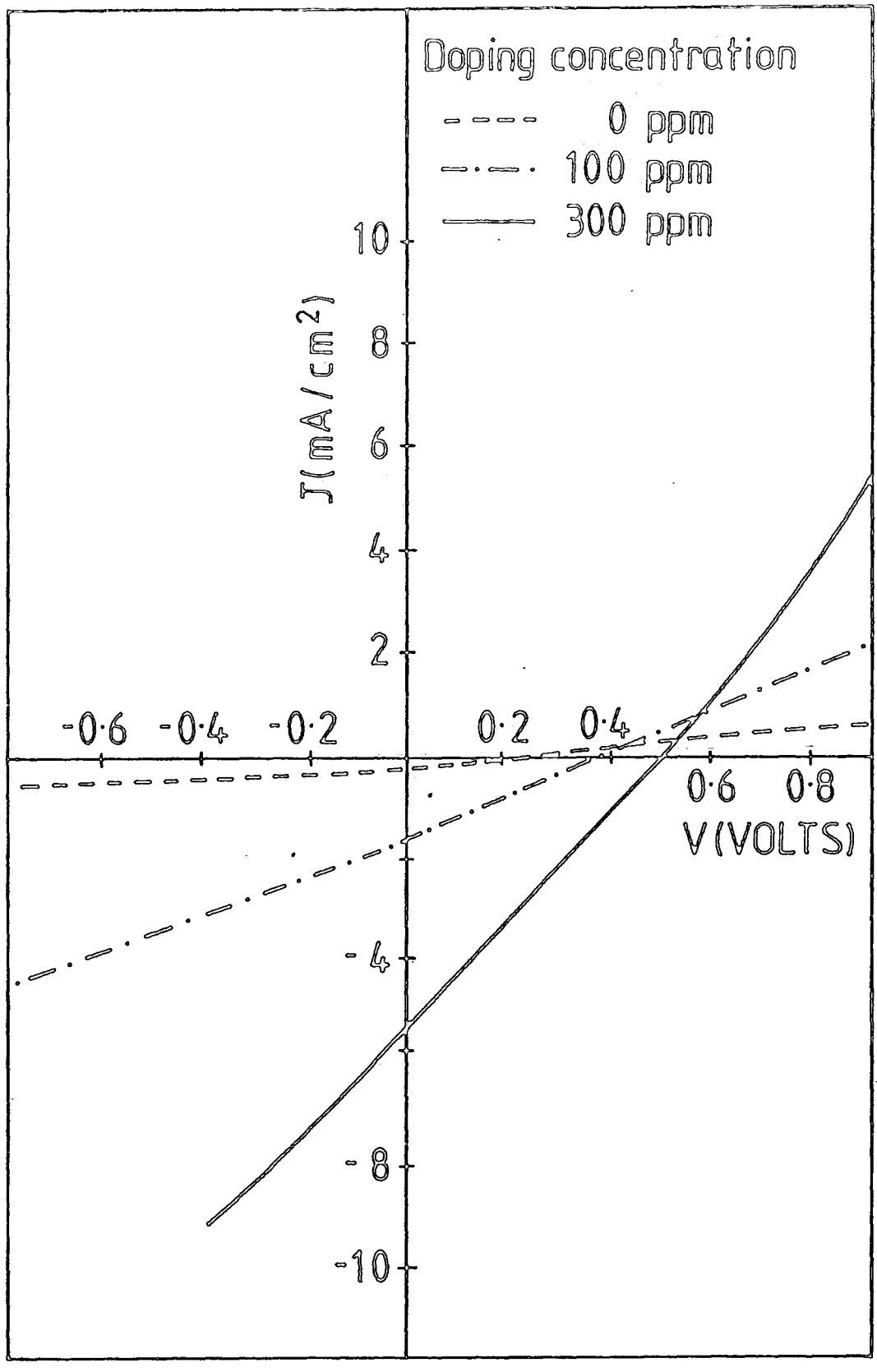

Fig. 8.5 : Photovoltaic behaviour of Hetrojunction with different Cu concentrations.

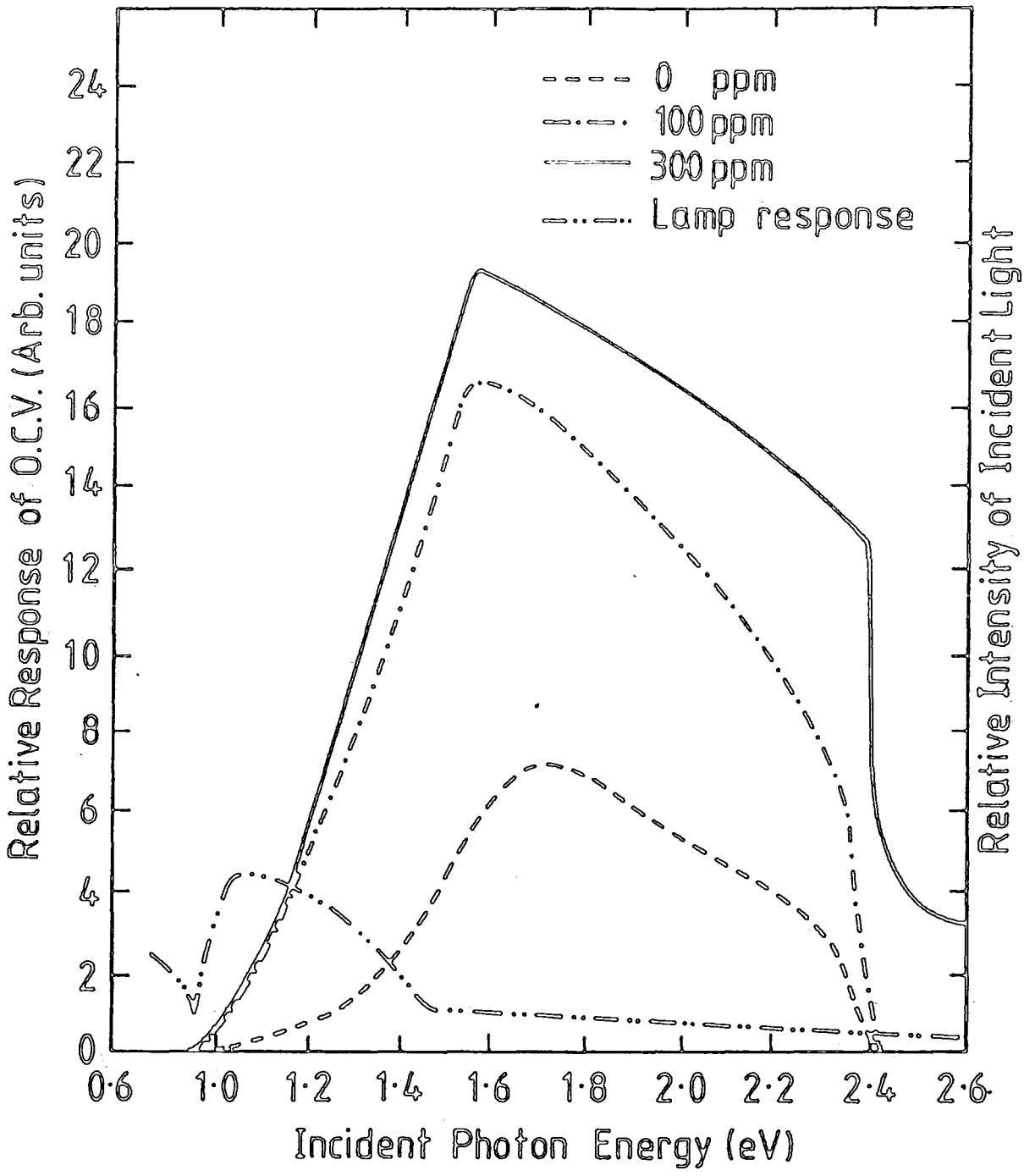

Fig. 8.6. : Open circuit voltage spectral response of CdS/CdTe Hetrojunctions with different Cu concentrations.

100 ppm Cu device, the peak response lay close to the CdTe band gap. Also, the short wave length cut off occurred at the CdS band gap with no extension to higher energy. With the 300 ppm device the short wave length response extended further into the blue region.

8.3.3 Thickness effects

Because of the large absorption coefficient of CdTe ($>10^4$ cm^{-1}) (6) nearly all photons from the solar spectrum which have energies equal to or greater than the band gap of CdTe (1.5 ev) are absorbed within a distance of 1-2 μ of the surface (26-28). Therefore a large CdTe layer thickness is inefficient and a waste of material, especially with the short minority carrier diffusion length in CdTe (26), which means that all carriers created in the first few microns will recombine before reaching the junction where useful collection of carriers occurs (6). Although, this can be alleviated partially by using back mode illumination (section 6.2.1), the influence of the thickness would still be significant.

Fig. 8.7 shows the photovoltaic behaviour of three devices with different CdTe thicknesses of 0.5, 5 and 15 μm. It is clear that the '5 μm' device produced the best photovoltaic parameters, with a S.C.C. of 5.6 mA, O.C.V. of 0.51 V and a fill factor of 26%, The device with the thinnest layer of CdTe gave low values, of 1.5 mA and 0.32 V for S.C.C. and O.C.V. respectively, but with a higher fill factor of 55%. The device using 15 μm thick layer produced the poorest values of S.C.C. (0.1 mA) and O.C.V. (0.28 V), with an extremely low fill factor of .2%. Obviously the thick CdTe layers (15 μm) increased the series resistance. On the other hand a thin CdTe layer (.5 μm) is not thick enough for complete absorption of light (10) (28), and of course the Cu doping may not have been fully optimized (10). The possibility of Cu diffusion into CdS layer through the thin CdTe layer is quite a problem and this would increase the resistivity of the CdS layer.

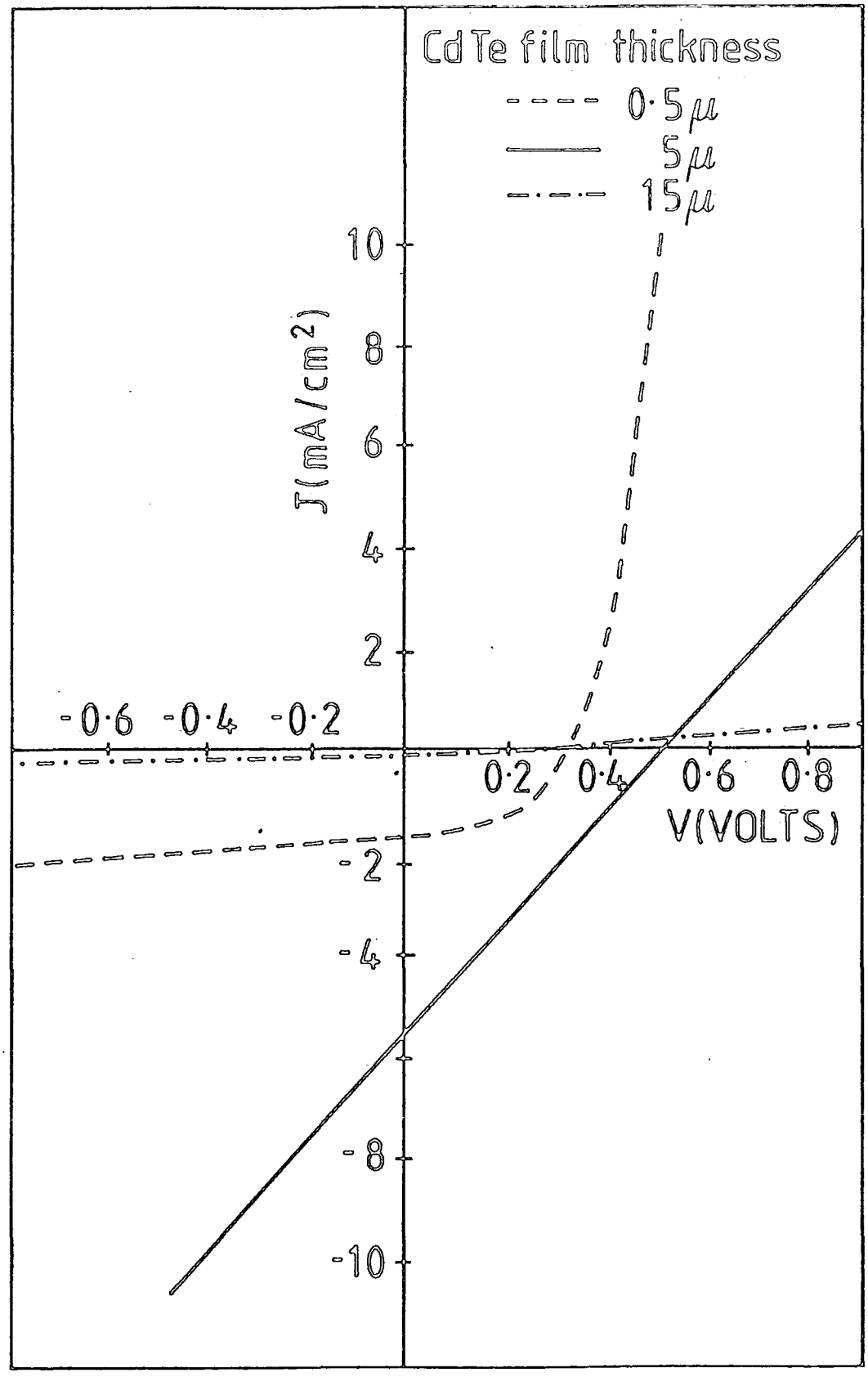

Fig. 8.7 : J-V characteristics of a CdS/CdTe Hetrojunctions using different CdTe film thicknesses.

It is therefore suggested that a CdTe thickness of 5 μm is required as a compromise to obtain a good light absorption and a low CdTe resistance.

8.3.4 Post deposition annealing

Post deposition annealing is necessary to allow copper diffusion into the CdTe layer (section 8.2.2), and this makes the layers more P-type. The superiority of a vacuum ambient over argon has been discussed in section 8.2.3. In this section a trial of post deposition annealing in hydrogen as another possible ambient is described.

The photovoltaic characteristics of devices annealed in both vacuum and hydrogen ambients are shown in fig. 8.8. Both devices displayed similar S.C.C. values of 5.6 mA. However, the O.C.V. was higher for the vacuum annealed device at 0.51 V than that of 0.45 V for the hydrogen annealed device.

The O.C.V. responses of the two annealed devices are shown in fig. 8.9. These revealed a low energy threshold at .85 ev for the vacuum annealed device with a sharp cut off at the band gap of CdS. In contrast, a sharp obsorption edge on the CdTe side of the hydrogen annealed device was observed, with a threshold at 1.2 ev. However, there was no sharp cut off at the CdS band gap in this device.

8.3.5 Conclusion

The optimization studies presented above suggest the following as the conditions for producing the best CdTe layer for hetrojunction formation:

- A deposition substrate temperature of 200°C
- A Cu dopant concentration of 300 ppm
- A CdTe layer thickness of 5 μm
- Post deposition annealing at 350°C for 15 minutes in a vacuum ambient

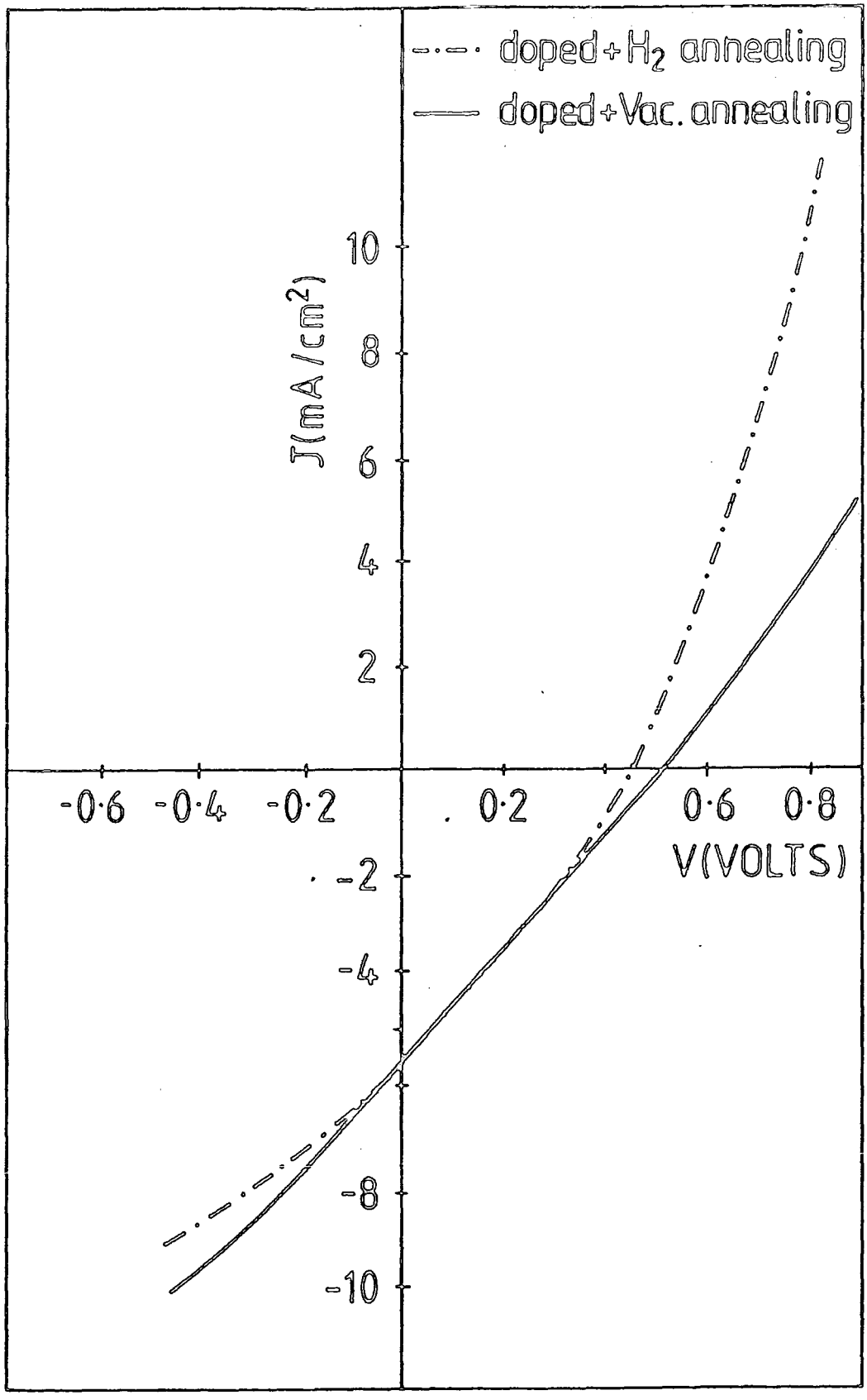

Fig. 8.8 : Photovoltaic behaviour of Hetrojunctions under various annealing conditions.

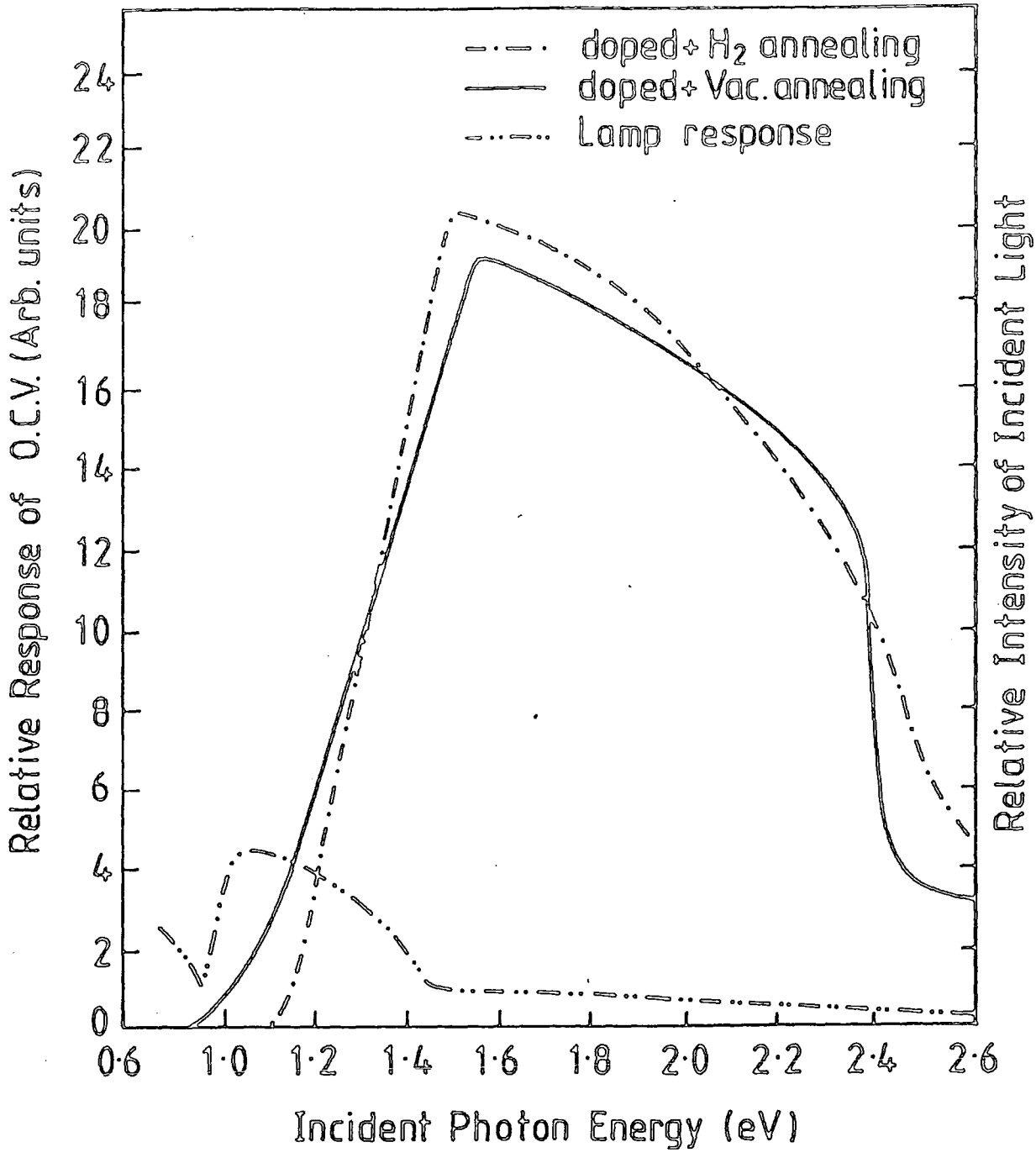

Fig. 8.9 : Open circuit voltage spectral response of CdS/CdTe Hetrojunctions under various annealing conditions.

8.4 Effects of CdS layers

8.4.1 Introduction

The great influence of the various preparational and sintering conditions involved in the fabrication of the screen printed layer, upon the behaviour of a simple Schottky device has already been described in section 6.2.3. In this section the effect of the CdS upon the more complicated hetrojunction CdS/CdTe structure will be described.

8.4.2 Substrate effects

Major variations in the morphological and electrical behaviour of CdS layers deposited onto different substrates (Soda Lime, Borosilicate and SnO_2) are summarized in section 7.2.

Attempts were made to fabricate CdTe heterojunction cells using the optimum CdTe recipe, and the three optimum CdS layers deposited on the three different substrates, in order to obtain more information about the significance of the substrate in the overall process.

Fig. 8.10 shows the photovoltaic behaviour of the devices fabricated on these different CdS layers under AM1 illumination. The photovoltaic parameters are presented in table 8.1.

Substrate type	O.C.V. Volts	S.C.C. mA/cm^2	F.F. %	Eff. %
Soda Lime	0.51	5.6	26	.74
Borosilicate	0.48	8.3	28	1.1
SnO2	0.43	12.8	30	1.6

Table 8.1 Effect of Substrate type on device parameters

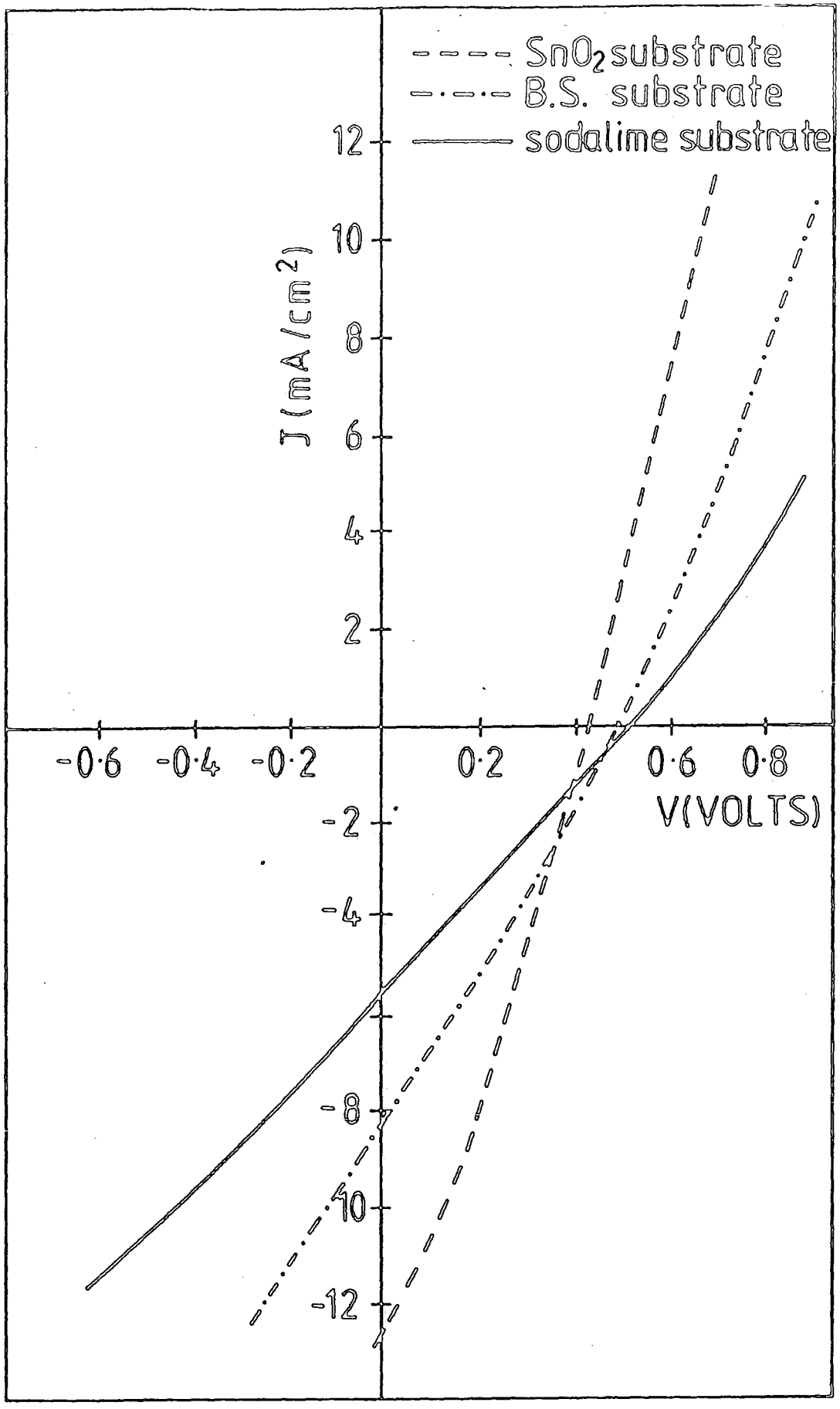

Figure 8.10 : Photovoltaic behaviour of Hetrojunctions using different substrate types.

It is clear that the device on soda lime glass produced the highest O.C.V. (.51 V), but on the other hand it had the lowest S.C.C. of all (5.6 mA). In contrast, the SnO_2 device produced the highest S.C.C. (12.8 mA) but it had the lowest O.C.V. (.43 V). The borosilicate device had an intermediate values of O.C.V. (.48 V) and S.C.C. (8.3 mA).

These differences are believed to be related mainly to the substrate materials which in turn affect the deposited over layer. For the SnO_2 device the occurrence of a low O.C.V. value may be the result of a heavy Sn doping as suggested in section 7.4.2. An increase in donor concentration was found to reduce the value of the O.C.V. (5). The fact that this device exhibited the highest value of S.C.C. could be attributed to an increase in the number of photons entering through the wide band gap SnO_2 window in the back mode illumination (29). With the borosilicate device the improved structure of the deposited CdS layer (fig. 7.1 B) plays an important role in contributing to the relatively high S.C.C. value (8.3 mA) compared with the soda lime device, because more carriers will flow because of the smaller number of grain boundaries. Conversely the presence of more boundaries in the CdS layer on soda lime glass (fig. 7.1 A) is probably responsible for the lower S.C.C. value, because of the increased probability of carrier loss in the powdery structure. Th occurrence of the highest O.C.V. in the soda lime device may be due to its cleaner CdS surface (fig. 6.8 C).

The fill factors and efficiencies of the three devices were very poor. The reasons for the low values of fill factor will be discussed later in Section 8.5.1. However, it is interesting to note that the SnO_2 device showed the largest F.F. of 30% and the highest efficiency regardless of its low O.C.V.

The spectral responses of the O.C.V.'s of the three devices are shown in fig. 8.11. The largest response is given by the soda lime device, while the poorest is for the borosilicate device, which shows a narrow response, falling off faster in short wave length region than the other two.

The soda lime and SnO_2 devices showed considerable similarity in the shape of the response. However, the magnitude of the Soda Lime device was greater than the SnO_2 device.

8.4.3 Post sintering annealing effect

ESCA studies described in section 6.3.4 revealed the presence of a sulphate (SO_4^{-2}) layer on all sintered CdS layers. This was found to be reduced, but not totally removed by post sintering annealing in an inert atmosphere. To investigate the possible effect of this layer upon the cell performance, two devices were fabricated on unannealed and hydrogen annealed CdS layers.

The photovoltaic performance of both devices is shown in fig. 8.12. It is clear that the device on annealed CdS produced poorer photovoltaic parameters, i.e. a S.C.C. of 2.9 mA and O.C.V. of 0.48 V, compared with a S.C.C. of 5.6 mA and O.C.V. of 0.51 V for the unannealed device.

The O.C.V. responses of the two devices are shown in fig. 8.13. The annealed devices show a marked increase in the threshold energy of the red response which starts at an energy of 1.2 ev. They also reveal a better CdTe absorption edge. This contrasts with the unannealed device which has a threshold energy of 0.85 ev and a peak response shifted to slightly higher energy. The annealed device exhibited a poorer response in the blue region with a fast decay whereas the unannealed device revealed a larger and wider response over the same wave length region.

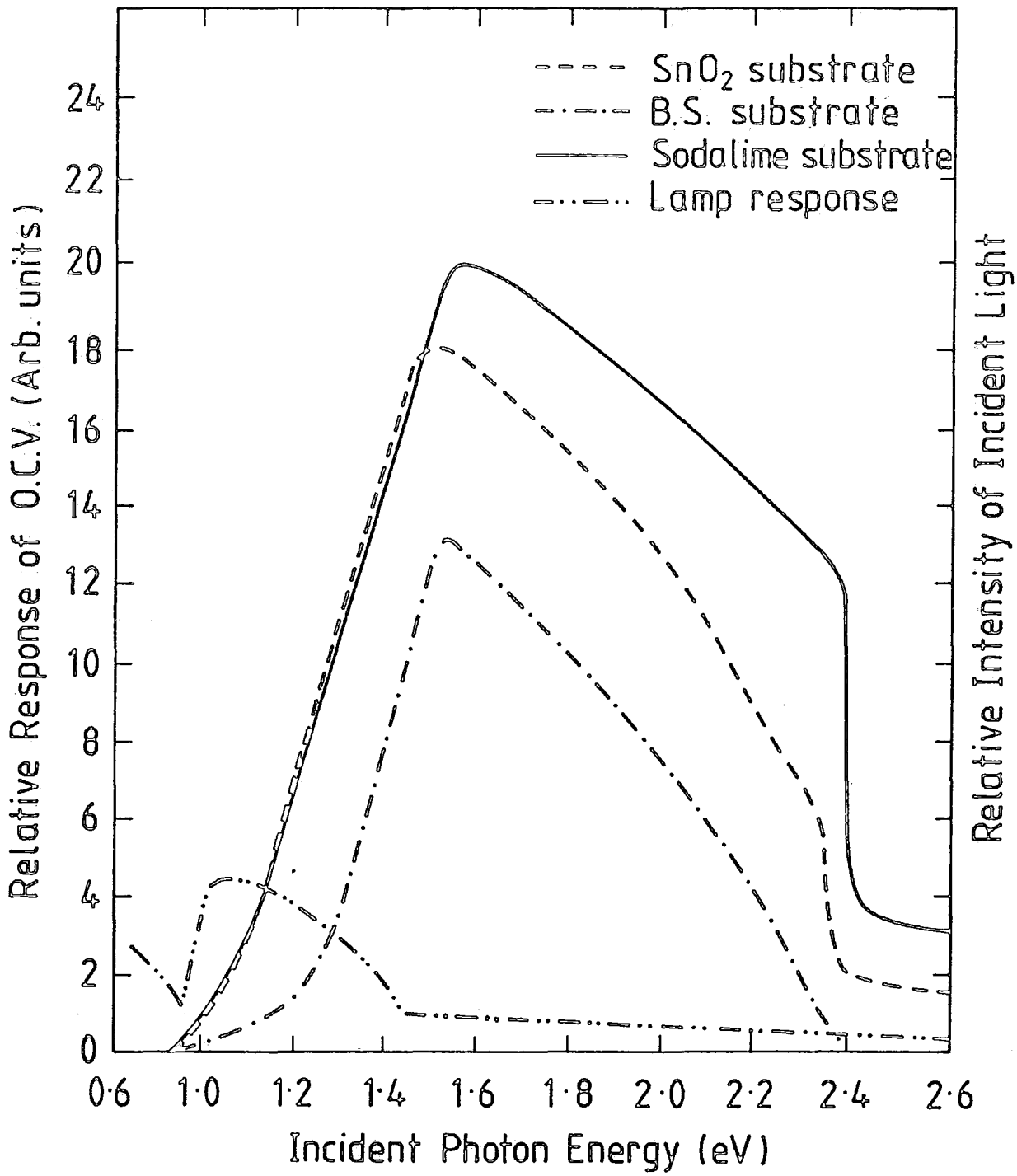

Fig. 8.11 : Open circuit voltage spectral response of CdS/CdTe Hetrojunction using different substrate bypass.

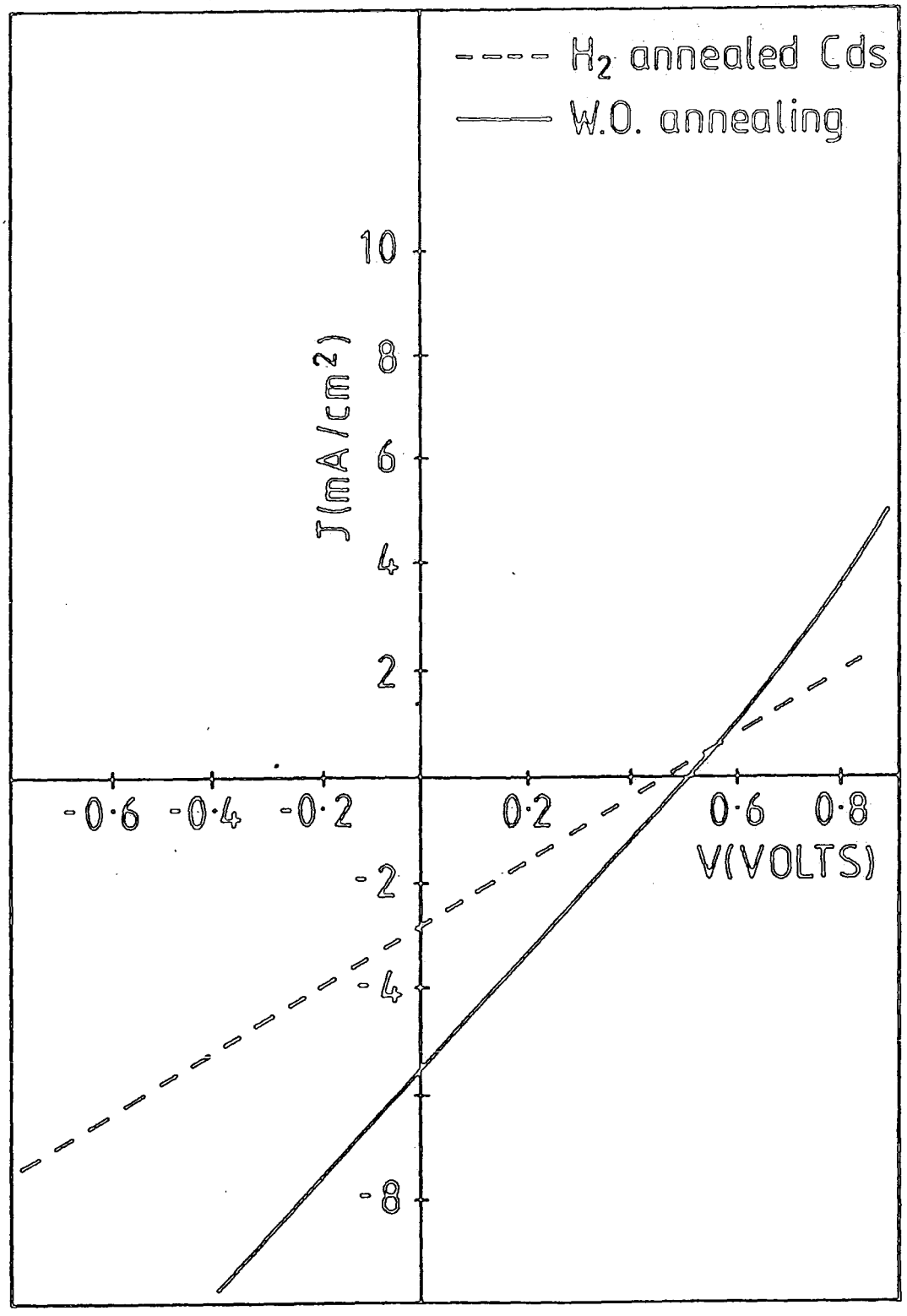

Fig. 8.12 : Photovoltaic behaviour of Hetrojunctions using Hydrogen annealed CdS layers.

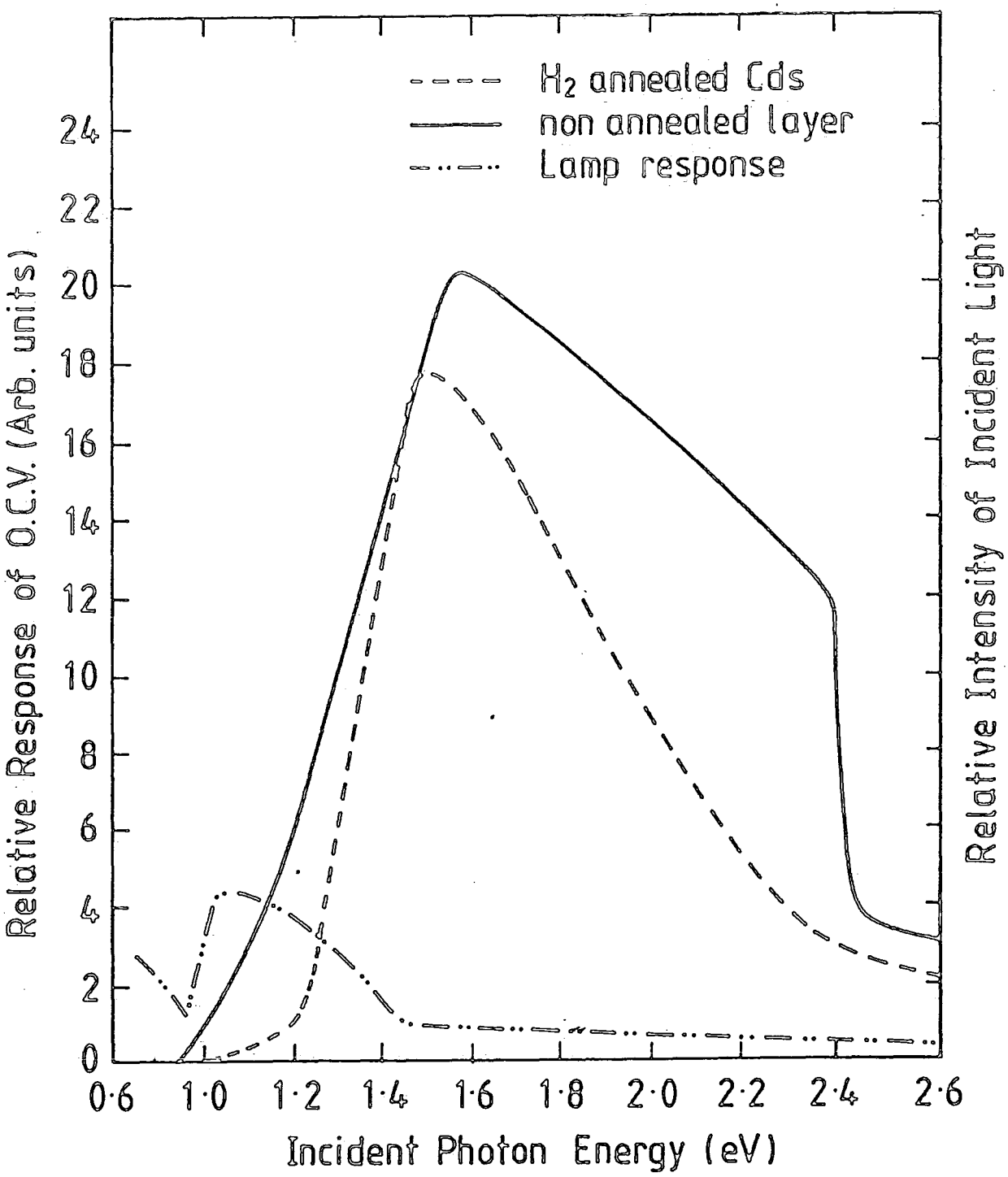

Fig. 8.13 : Open circuit voltage spectral responses of Hetrojunctions using Hydrogen annealed CdS layers.

Hall measurements made on both annealed and unannealed layer (section 6.2.2.5 v) indicated the occurrence of unusually high mobility values in the annealed CdS layers. This is believed to be due to the presence of precipitated impurities in the grain boundary region (section 7.3.2) as a result of post annealing. It is very likely that the presence of these precipitates would influence the interface between CdS and CdTe junctions. Therefore, regardless of the improvement in the bulk properties of the CdTe in the CdS annealed devices, the adverse effects of other parameters would suggest the use of unannealed CdS layers for device fabrication. Therefore any improvement in the device performance should be sought without further treatment of the as made CdS layer. Nevertheless, this study shows the influence of the unavoidable sulphate layer present on the sintered CdS layer.

8.4.4 Conclusion

The work described in the above sections indicates the strong influence of the nature of the CdS layer on the CdS/CdTe hetrojunctions. It also confirms the undesirable effects of post annealing the optimum CdS layers on the performance of the fabricated device on these layers.

8.5 Discussion

Most of the devices described in the previous sections have many features in common. The object was to select the best conditions for fabrication of the device. In what follows an attempt will be made to explain some of the features observed in more detail with a view to gaining a better understanding of the processes involved.

8.5.1 Analysis of the Photovoltaic Results:

Oben Circuit Voltage: The relatively low O.C.V. for the soda lime device of 0.51 ev has many possible explanations. The following are

believed to be the most likely; i) the presence of grain boundaries in the polycrystalline CdTe layer produces a major problem due to the increased impurity concentration (i.e. Cu) in the boundary regions, which will increase the shunt resistance of the cell and result in a lower O.C.V. (30). ii) the difficulties encountered in obtaining good P-type CdTe doping (sect. 2.2.2ii) also gives rise to a low barrier height (31) and iii) the rough CdS surface would disturb the desirable crystallinity of the CdTe layer giving a low shunt resistance and hence, a low O.C.V. (10).

Short Circuit Current: The relatively low S.C.C. of 5.6 mA can be attributed to both the CdS and the CdTe layers; the powdery structure of the printed CdS layer introduces an increased number of grain boundaries which will act as traps for most of the photocarriers before they reach the junction. An improvement in the structure would lead to increased current collection as with the borosilicate devices (section 8.4.2). Moreover, the roughness of the CdS surface also has some influence in reducing the current value in general. This is possibly because the disordered area of the p-n junction for CdTe deposited on rough CdS layer produces one part of the active area of the cell and hence causes loss of current (32). On the other hand, the non optimized P-type doping of the CdTe layer implies a high resistivity CdTe layer, which will reduce the life time of the minority carriers resulting in less efficient current collection.

Although the effect of the CdTe could be minimised by employing back wall mode illumination (section 8.2.1) it would still play a major role in limiting higher current values.

Fill Factors: The very low values of the fill factor for the optimum device is largely attributable to the high series resistance and the low shunt resistance of the devices.

The high series resistance of the cell is very clear from the shallow gradient of the I-V curve (fig. 8.10). This high resistance derives from the resistivity of both the CdS and CdTe layers, and the contact resistance to both layers. The relatively low resistivity of CdS used in this study (3 Ω cm) made little contribution to the total series resistance (33) (34), and therefore would have had little influence upon the resultant low F.F. value. On the other hand, the difficulties in obtaining a high level of P-type doping in the CdTe layer would suggest that the series resistance was dominated by the high CdTe resistance (10). Moreover, non optimised P-doping may well have led to a higher contact resistance to the CdTe layer (34). Finally, a contribution of the indium contact to CdS to the total series resistance is also possible regardless of the good ahmicity obtained (section 6.2.1).

A second reason for the low fill factor in the low shunt resistance of the cell, which can be clearly seen from the soft knee of the light I-V curve, and the large gradient of the curve after crossing the current axis. This is fairly typical of most devices in this study.

The low shunt resistance is associated mainly with the presence of grain boundaries, and unavoidable pinholes in the thin film structure which produce leakage currents (35). The roughness of the CdS surface is an additional problem which could create shunting paths.

8.5.2 Analysis of Spectral response

The shape of the spectral response of the best device shown in fig. 8.11 revealed a wide sensitivity over the whole visible spectrum. However, there are some features of this typical response, and of the response of the other devices examined which need to be investigated.

These include the low energy threshold occurring below the CdTe band gap and the poor blue response of some non optimum devices.

Low energy threshold: The long wave length spectral edge is associated solely with the collection of photo carriers in the CdTe layer (6), and the shape of the absorption edge should ideally occur at energies corresponding to the CdTe band gap (36). However, the present devices in general have a spectral sensitivity which starts at a much lower energy (.85 ev) than that of CdTe (37), and have an exponential tail rather than an abrupt edge. This may be due to the presence of impurity or defect states close to the valence band of CdTe (9) (10) (13). J. Pickozewsk et al (38) have indicated that the presence of a large concentration of compensating donor and acceptor impurities will give rise to band gap narrowing and create a high field in the junction. Because of this, electron hole pairs can be generated at photon energies substantially less than the band gap (Eg) (39) by a tunneling assisted transition (Franz-Keldysh effect) (10). The larger the built-in field, the further the tail of the photo response extends into the infrared. The improvement in the threshold energy in the hydrogen annealed devices (figs. 8.9 and 8.13) reflects the formation of fewer impurity states and a lower field strength in these devices.

Poor blue response: The sharp wave length cut off at the CdS band gap for the best device (fig. 8.11) in the blue region, is an indication of the presence of a true heterojunction (40). On the other hand, the poor blue response for most other devices is an indication of a buried homojunction (41). This may be the result of a large density of surface states at the CdS/CdTe interface which could act as a window and absorb most of the short wave length radiation with energy above the band gap (42).

8.6 Conclusion

Although the present performance of the best device in this study is relatively poor, the study has confirmed the validity of the fabricated CdS layer for heterojunction formation.

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CHAPTER NINE

SUMMARY AND CONCLUSION

The work presented in this thesis can be categorized under two major headings: i) preparation of CdS screen printed layers and ii) device trials.

9.1 Preparation of CdS layers

The ultimate aim was to prepare screen printed CdS layers with reproducible morphological and electrical behaviour for use in the fabrication of solar cells. To achieve this the interdependent printing, preparation and sintering conditions involved in the fabrication processes were investigated and optimized.

A screen printer was built in this laboratory. The device and screen parameters were optimized to ensure the best printing conditions.

The preparation and sintering conditions were then optimized. The fabricated CdS layers under these conditions were characterized using a variety of experimental techniques including Hall effect, Schottky diodes, SEM, EDAX, ESCA and XRD. Many new parameters were investigated such as CdS powder type, mixing significance, furnace type, flow rate, post sintering annealing and a rule of substrate. In general it was found essential to start with a pure powder which has an average grain size of 3 μm. Adequate paste mixing was necessary to ensure dopant and flux distribution and to produce a thixotropic printing paste. The sintering in a tube furnace produced the best results rather than in a muffle furnace. The argon flow rate in the furnace was maintained at 0.1 L/min as the best compromise to provide an inert sintering ambient and to minimize the fast drive-off of the volatilized $CdCl_2$ material. Post sintering annealing was tried and is only recommended for non optimised fabricated layers.

The best sintering rate was 28°C per min. and the optimum sintering temperature and duration was 620°C for 90 min. The detailed investigation of various substrate materials suggested that soda lime glass was best. The use of SnO_2 coated glass as a substrate material presents a great risk of metallic migration into the over layer CdS leading to a deterioration in the electrical behaviour of the layer. The abnormally high mobility values obtained with layers on borosilicate glass 7740 was related to the precipitation of impurities at the grain boundary regions.

By standardizing the printing, preparation and sintering conditions a reproducible CdS layer was prepared which had a good compact morphology with a hexagonal structure. Such layers had a low resistivity of 3 Ω cm with a corresponding carrier concentration of 8.2×10^{16} cm^{-3} and a mobility of 16 cm^2 $v^{-1}s^{-1}$.

9.2 Device trials

Trials of a Schottky device formation resulted in good rectification behaviour of the fabricated diodes. C-V measurements suggested the formation of an interfacial layer on the surface of the sintered layer. This was confirmed by ESCA analysis since a layer containing SO^{-2}_4 ions was suggested to form on the surface of all sintered layers.

The fabrication of solar cells by evaporation of CdTe layers on the screen printed layer was also investigated. By optimizing the quality of the evaporated layers of CdTe a solar cell with a wide spectral response was achieved using CdS layers deposited on Soda Lime glass. The photovoltaic parameters were 0.53 V, 5.6 mA for O.C.V. and S.C.C. values respectively. The question of high resistivity of CdTe layer and high contact resistivity has to be solved to improve the overall efficiency.

Finally, the fast reduction of the chlorine ions in the process of sintering as indicated from XRF and AAS analysis suggests that the performance of the CdS layers can be further improved if a better method of sintering confinement can be contrived for precise control of the $CdCl_2$ evaporation.