Characterisation of thin films of silicon rich oxides

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Characterisation of Thin Films of Silicon Rich Oxides

by

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Abstract

The electrical characteristics of a Metal-Semi-insulator-Semiconductor diode have been comprehensively studied at various temperatures. In particular the electrical, structural and compositional properties of the semi-insulator, silicon-rich-oxide (SRO), have been thoroughly investigated. The SRO films were all deposited by atmospheric pressure chemical vapour deposition, (APCVD), at 650° C with silane (SiH_4) and nitrous oxide (N_20) reactant gases and a carrier gas of nitrogen. The reactant gas ratio, γ, was held at 0.22 and the deposition time varied between 0.5 and 8 minutes. The effects of film thickness, film annealing, forming, top contact metal (i.e. work function difference), top contact metal area, substrate material and temperature on the electrical characteristics in both forward and reverse bias have been reported.

Various techniques have been employed to elucidate the physical and structural properties of the SRO film. These include: Auger Electron Spectroscopy; Secondary Ion Mass Spectroscopy; Glow Discharge Optical Emission Spectroscopy; Scanning Electron Microscopy; Transmission Electron Microscopy; Rutherford Backscattering Spectroscopy; Optical Ellipsometry and Alpha Step Analysis.

A model for the structure of SRO films has been put forward. The films are thought to be extremely random in structure, containing many voids with a gradual variation in composition from substrate to top metal contact. Various models for conduction in the SRO film were investigated over a range of electric fields and temperatures to determine the predominant conduction mechanism for a particular set of conditions. Conduction in SRO is thought to be dominated by Schottky emission across the SRO-substrate interface. Once this Schottky barrier is conducting, at suitably high biases, conduction across the remainder of the device is thought to be by thermionic emission at high temperatures and by a Poole-Frenkel process at low temperatures.

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Declaration

I hereby declare that the work reported in this thesis has not been previously submitted for any degree, and is not being currently submitted in candidature for any other degree.

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The work reported in this thesis was carried out by the candidate.

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Director of Studies

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Candidate

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For Jennifer, Andrew and Jasmine

Contents

1 Introduction **1**
- 1.1 Introduction . . . 1
- 1.2 Silicon-rich oxide . . . 1
- 1.3 The MISS device . . . 3
  - 1.3.1 MISS operation . . . 4
  - 1.3.2 Thesis outline . . . 5

2 Metal-Insulator-Semiconductor (MIS) Devices **7**
- 2.1 Introduction . . . 7
- 2.2 The ideal equilibrium MIS diode . . . 8
  - 2.2.1 Structure of an ideal MIS diode . . . 8
  - 2.2.2 Ideal MIS diode under zero bias . . . 8
  - 2.2.3 Ideal MIS diode under forward bias . . . 10
  - 2.2.4 Ideal MIS diode under reverse bias . . . 12
- 2.3 Capacitance-voltage curves . . . 13
  - 2.3.1 Accumulation . . . 15
  - 2.3.2 Depletion . . . 15
  - 2.3.3 Inversion . . . 16
- 2.4 Non-idealities in equilibrium MIS structures . . . 16
  - 2.4.1 Introduction . . . 16
  - 2.4.2 The effect of metal work function . . . 17
  - 2.4.3 Insulator charge . . . 25
  - 2.4.4 Silicon-SRO interface traps . . . 29
  - 2.4.5 Interface traps and capacitance . . . 32
  - 2.4.6 Traps within bulk SRO . . . 32
  - 2.4.7 Effect of temperature . . . 33
  - 2.4.8 Effect of illumination . . . 34
- 2.5 A non-equilibrium non-ideal MIS diode . . . 34

3 Electrical Conduction Mechanisms in Thin Films **37**
- 3.1 Introduction . . . 37
- 3.2 Summary of the conduction processes . . . 38
  - 3.2.1 Electrode limited conduction . . . 38
  - 3.2.2 Bulk limited conduction . . . 39

3.3 General models for conduction 40
3.3.1 Tunnelling 41
3.3.2 Thermionic emission 42
3.3.3 Schottky emission 42
3.3.4 The Poole-Frenkel effect 44
3.3.5 Extended state conduction in amorphous solids 48
3.3.6 Conduction in localised states 49
3.4 Theories for conduction in silicon-rich oxide (SRO) films 49
3.4.1 Introduction 49
3.4.2 The models 50
3.5 Conclusions 58

4 Experimental Details **62**
4.1 Introduction 62
4.2 Fabrication of MIS devices 62
4.2.1 Introduction 62
4.2.2 Silicon substrates 62
4.2.3 Cleaning procedure 63
4.2.4 The field oxide 63
4.2.5 Field oxide thickness 64
4.2.6 Field oxide resistivity 64
4.2.7 Chemical deposition of SRO 64
4.2.8 Annealing 67
4.2.9 Metallisation 67
4.2.10 Printed circuit board (PCB) 69
4.2.11 Testing gold bonds 70
4.3 The electrical measurement system 70
4.3.1 Current-voltage measurements 71
4.4 Temperature measurements 72
4.4.1 The cryostat 74
4.5 Data acquisition and display 78
4.5.1 Signal connections 78
4.6 Compositional analysis 82
4.6.1 Glow discharge optical emission spectroscopy 82
4.6.2 Secondary ion mass spectroscopy 83
4.6.3 Auger electron spectroscopy 84
4.6.4 Rutherford backscattering spectroscopy 86
4.7 Physical characterisation 89
4.7.1 Thickness measurements 89
4.8 Structural characterisation. 91
4.8.1 Scanning electron microscopy 91
4.8.2 Transmission electron microscopy 93
4.9 Summary 94

5 Physical characterisation **96**
5.1 Introduction 96
5.2 Models for silicon-rich oxide microstructure 97
5.3 Compositional analysis 101
5.3.1 Glow discharge optical emission spectroscopy 101
5.3.2 Secondary ion mass spectroscopy 105
5.3.3 Electron spectroscopy 109
5.3.4 Rutherford backscattering spectroscopy 113
5.3.5 Thickness measurements 115
5.3.6 Structural analysis 128
5.3.7 Comparison of results for different techniques 131
5.4 The microstructure of SRO 136
5.5 Conclusions 137

6 Electrical Characterisation **143**
6.1 Introduction 143
6.2 Typical I-V characteristics 143
6.3 Capacitance-voltage curves 145
6.3.1 Introduction 145
6.3.2 A typical C-V characteristic 145
6.4 Reproducibility 146
6.4.1 Reproducibility of devices on the same wafer 146
6.4.2 Reproducibility of wafers processed simultaneously 147
6.4.3 Reproducibility of wafers processed in different APCVD runs . 147
6.4.4 Reproducibility and C-V measurements 148
6.4.5 Reproducibility on temperature cycling 148
6.5 Forming 150
6.6 Edge effects 151
6.7 Device area 151
6.8 Thickness comparisons 152
6.8.1 C-V evidence 152
6.8.2 I-V evidence 152
6.8.3 The effect of film thickness on MISS devices 153
6.9 Top contact metal 153
6.9.1 Introduction 153
6.9.2 Forward bias results 154
6.9.3 Reverse bias results 154
6.9.4 Discussion of results for the three top contacts 155
6.9.5 C-V evidence 156
6.9.6 Summary 156
6.10 Substrate doping 157
6.10.1 I-V evidence 157
6.10.2 C-V evidence 158
6.11 Effect of temperature on I-V characteristics 160

6.12 Device breakdown . . . 162
6.13 The effect of annealing . . . 164
6.13.1 Introduction . . . 164
6.13.2 Forming investigations for annealed SRO MIS devices . . . 165
6.13.3 I-V characteristics . . . 165
6.14 Recommendations for MISS devices . . . 168
6.15 Summary . . . 169

7 Device Modelling **173**
7.1 Introduction . . . 173
7.2 Electrical measurements . . . 173
7.3 The Proposed SIS Energy band structure . . . 174
7.4 The SIS Schottky barrier properties . . . 179
7.4.1 Theory . . . 179
7.4.2 Ideality factor . . . 181
7.4.3 Reverse characteristic . . . 185
7.4.4 Barrier height estimation . . . 186
7.4.5 The barrier voltage determination . . . 187
7.4.6 Comparison of theoretical and experimental curves . . . 190
7.5 Conduction in the bulk of the SRO film . . . 193
7.5.1 Ohmic conduction . . . 193
7.5.2 Thermionic emission . . . 193
7.5.3 The Abeles model . . . 195
7.5.4 Fowler-Nordheim tunnelling . . . 195
7.5.5 The Hamasaki model . . . 198
7.5.6 Percolation theory . . . 200
7.5.7 The Ni and Arnold model . . . 200
7.5.8 The Schottky and Poole-Frenkel mechanisms . . . 203
7.6 Summary . . . 211

8 Conclusions and suggestions for further work **214**
8.1 Introduction . . . 214
8.2 Summary of results . . . 214
8.2.1 Structural properties . . . 214
8.2.2 Electrical properties . . . 215
8.2.3 Device modelling . . . 216
8.3 Suggestions for further work . . . 217
8.3.1 Conduction models . . . 217
8.3.2 Temperature range . . . 217
8.3.3 Electrode material . . . 217
8.3.4 Breakdown . . . 218
8.3.5 Annealing . . . 218
8.3.6 Structural analysis . . . 219
8.3.7 Equipment . . . 219

A Image Force Lowering **221**
A.1 The metal-vacuum system 221
A.2 The metal-semiconductor system 223
A.3 The MIS system 226

B Fabrication Techniques **227**
B.1 Wafer cleaning 227
B.2 Growing the field oxide 228
B.3 Photolithography 228
B.3.1 Mask making 228
B.3.2 Wafer processing 229
B.4 Etching the field oxide 230
B.5 Cleaning 230
B.6 Chemical vapour deposition (CVD) 230
B.7 Evaporation of aluminium 231
B.8 Etching aluminium 231
B.9 Lapping the back of the wafer 231
B.10 Gold evaporation 232
B.11 Molybdenum evaporation 232
B.12 Chromium evaporation 232

C Gold Wire Bonding **233**
C.1 Cratering 233
C.2 Cleaning pads 233
C.3 Intermetallic compounds 234
C.4 Bonding wire loop height 235
C.5 Pcb metallisation 235
C.6 Metal systems 236

Chapter 1

Introduction

1.1 Introduction

Insulating films are of great importance in today's silicon device technology. For example, relatively thick (1 μm) layers of silicon dioxide are used to provide surface passivation and structural and electrical separation of one device from another. There are also devices that require a dielectric film to pass substantial currents at a low applied bias. The MISS (Metal-Insulator-Semiconductor Switch) structure is such a device. It is possible to grow thin layers of silicon dioxide through which tunnel currents can flow but it is difficult to grow consistent layers of an even depth over large areas. Thicker layers of more conducting films provide an easier solution. A suitable semi-insulating film is silicon-rich oxide, SRO. Although SRO has been used successfully in MISS devices at Durham, its properties are far from being fully understood. The aim of this thesis, therefore, is to investigate the physical and electrical properties of silicon-rich oxide.

1.2 Silicon-rich oxide

Silicon dioxide, SiO_2, should theoretically consist of 33 atomic % silicon and 67 atomic % oxygen. The percentage of silicon present in the films under study is greater than the stoichiometric 33%, hence the term silicon-rich oxide. This material is also known as oxygen-rich polysilicon (ORPS) or more often in the literature as semi-insulating polysilicon (SIPOS). The chemical formula for SRO is SiO_x where x lies between 0 and 2. The system used to grow the films is **critical** in determining the nature of the films produced. For example, the value of x is determined by the deposition

temperature and relative proportions of the reactant gases. Silicon-rich oxides have attracted a great deal of interest in recent years because of the wide range of properties attainable by simply changing the amount of oxygen in the film. For instance, these have been used as passivation materials to replace the silicon dioxide in high voltage semiconductor devices [1– 3]. The SRO film offers a means to overcome three problems which challenge modern IC technologies:

(i) fixed charges, which are usually positive ions, occur in oxide films. These tend to accumulate electrons at the silicon-oxide interface, which causes problems for high voltage planar transistors [4];

(ii) oxide films do not confine ionic contamination such as sodium to the passivation layer [5, 6]; and

(iii) a hot carrier in the oxide stays there a long time causing changes in the breakdown voltage of the pn junction.

The presence of charges within the oxide and induced charges around it affect the reliability of circuit passivation for high voltage semiconductor devices. In contrast, SRO films are only semi-insulating and tend to pin the Fermi level near midgap [7, 8]. This makes SRO suitable for surface passivation of both p- and n-type materials. When a silicon surface is passivated by SRO, the contaminating ions drift into the passivation layer. This causes an induced opposite charge that neutralises the charges or forms a space-charge region within the SRO layer [9]. The SRO layer therefore shields the silicon surface region. Studies have been reported of using SRO passivation layers in high voltage transistors [1, 2, 10]. As a new optoelectronic material, SRO has been incorporated in solar cells [11]. Besides a continuously adjustable bandgap, the refractive index of SRO changes significantly with oxygen concentration.

The semi-insulating nature of SRO and the ease with which it was possible to change its silicon content, and hence its conductivity, has made it a suitable material for use in the four layer metal-insulator-semiconductor switch, the MISS device. Previous workers at Durham have studied the room temperature electrical characteristics of these MISS devices (outlined below) with SRO as the semi-insulator. The SRO films were deposited in an atmospheric pressure chemical vapour deposition (APCVD) reactor. Using a range of conditions, various compositions of SRO were investigated until a suitably semi-insulating layer was produced. The performance of the resulting MISS device was then studied as a whole, neglecting a thorough investigation of the SRO film itself. This research seeks to characterise the SRO films used

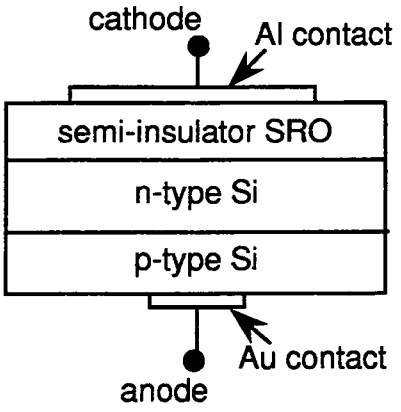

Figure 1.1 Basic structure of the MISS device.

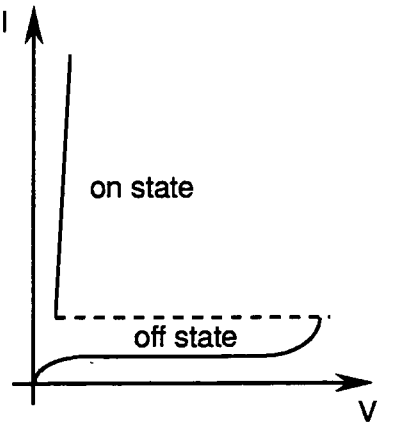

Figure 1.2 I-V characteristic for a typical MISS device.

in the successful switches. It would be advantageous to determine which parameters are important and which should be carefully controlled to optimise the performance of the SRO film in such devices. Although the use of SRO as a semi-insulating layer in the MISS component initiated the interest in this material at Durham, the objectives of the work are much wider. The aim of this research is to investigate the structural and compositional physical properties of the film and also to determine the predominant conduction mechanisms for a range of electric fields and temperatures.

1.3 The MISS device

The structure of the MISS device is shown in Figure 1.1. MISS devices have been found to exhibit a current-controlled negative resistance. Figure 1.2 shows schematically the current-voltage characteristic with the metal biased negatively with respect

to the p-type substrate. The negative differential (NDR) resistance region is shown by the dashed line in Figure 1.2 . This region is the switching of the device from the high-impedance low-current condition (the off-state) to the low-voltage, high-current condition (the on-state). The off-state has been found to correspond to deep depletion of the n-type semiconductor layer. The on-state has been found to correspond to inversion of this semiconductor layer [12]. The semi-insulator is very important in obtaining the NDR region and the on-state and this is explained in the next section.

1.3.1 MISS operation

At low forward bias (negative potential on the aluminium electrode) and if the oxide layer is only slightly conducting, the silicon surface is depleted and the total current is due to the generation of electron-hole pairs in the depletion region. This is the high-impedance state. As the applied voltage is increased the silicon becomes more depleted. The increased depletion width increases the generation current which causes a higher voltage to be dropped across the oxide and pn junction. This higher voltage across the pn junction increases the number of holes arriving at the SRO-silicon interface. An increased positive charge at the interface attracts electrons from the metal and further increases the voltage across the oxide and pn junction. When the rate of hole flow to the insulator-silicon interface is higher than that passing through the oxide, inversion occurs. At this point the voltage across the device decreases due to the decreasing semiconductor surface potential. Any increase in the applied voltage causes more current to flow through the oxide and more voltage to be dropped across it and the pn junction. This is the low-impedance state. The current is oxide limited.

If the oxide is too conducting, the semiconductor remains in depletion. Any minority carriers at the SRO-n-type silicon interface leak through to the metal. Inversion of the semiconductor surface cannot occur. The current is said to be semiconductor limited. If the applied voltage is increased the increase appears across the semiconductor and a saturation plateau shows on the current-voltage characteristic as shown in Figure 1.3. Finally, if the insulator were non-conducting then a simple capacitor would result. Again, the device would be unable to switch. The semi-insulating layer is therefore very important to the switching characteristics of the MISS device. Further reference to the MISS device will not be made in this thesis. The first three layers of the MISS device form what is called an MIS diode and this forms a suitable vehicle for the study of the SRO film properties.

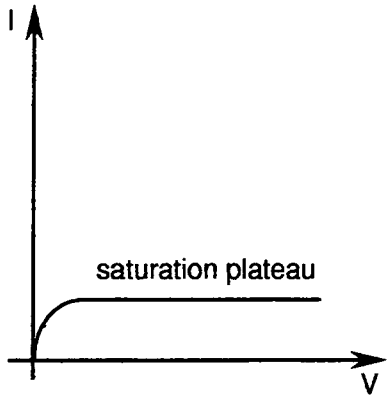

Figure 1.3 Current-voltage characteristic for depletion in the n-type layer.

1.3.2 Thesis outline

A theoretical treatment of the electrical behaviour of several types of MIS diode under forward and reverse bias is presented in Chapter 2. These include:

(i) an ideal MIS diode, i.e. one in which the insulator is non-conducting;

(ii) an MIS diode with a good insulator but with interface states and charges; and

(iii) a non-ideal MIS diode with a leaky insulating layer and interface states.

Possible conduction mechanisms are reviewed in Chapter 3. Device fabrication and measurement techniques are outlined in Chapter 4. Chapter 5 covers the theoretical models for SRO structure and contains experimental results for compositional and structural analysis. The structure is discussed and a model put forward. Chapter 6 contains the electrical characterisation of various types of metal-SRO-semiconductor diodes, in both forward and reverse bias over a range of temperatures. Experimental data for the effects of temperature, contact metal, top contact area, annealing, n and p-type substrates and film thickness are presented and important factors for MISS device applications identified. Chapter 7 presents theoretical and experimental curves for the various conduction mechanisms over combinations of high and low electric fields and a range of temperatures. These are discussed and conduction mechanisms identified. Finally, in Chapter 8 the experimental results and conclusions are summarised together with suggestions for further work made, with emphasis on a closer examination of the process of annealing and its effect on the structure of the SRO film and on the interface charges. More detailed analysis of capacitance-voltage curves (at both high and low frequencies) are necessary especially for very thin films of SRO.

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Chapter 2

Metal-Insulator-Semiconductor (MIS) Devices

2.1 Introduction

The structure and operation of a metal-insulator-semiconductor switch (MISS) were outlined in Chapter 1. In particular, the importance of the semi-insulating layer was explained. Silicon-rich oxide (SRO) has been shown to have the properties required by the semi-insulating layer of MISS switches [1]. As explained in Chapter 1, MIS devices provide a simple structure for the study of SRO film properties. Systematic modifications can be made to basic MIS structures, such as changing the silicon substrate from n-type to p-type and changing the top contact metal. The resultant effects on the current through the device can be predicted, by reference to energy band diagrams.

Real MIS devices differ from the ideal models. This Chapter describes the ideal equilibrium MIS diode and its energy band structure under various biases. The equations that quantify the voltages dropped across the oxide, the silicon and the silicon-oxide interface are given. The ideal Capacitance-Voltage (C-V) curves are also shown with a brief description of MIS behaviour under various voltages. Non-idealities which are likely to occur in M-SRO-Si diodes are then described. The first non-ideality considered is the effect of metal work function. Modifications are made to the ideal equations and to the energy band diagrams. Both n- and p-type substrates are described. The next non-ideality considered is the presence of charge distributed throughout the oxide and that which is trapped at the silicon-oxide interface. In addition, traps due to defects within the bulk of the oxide are considered. Finally,

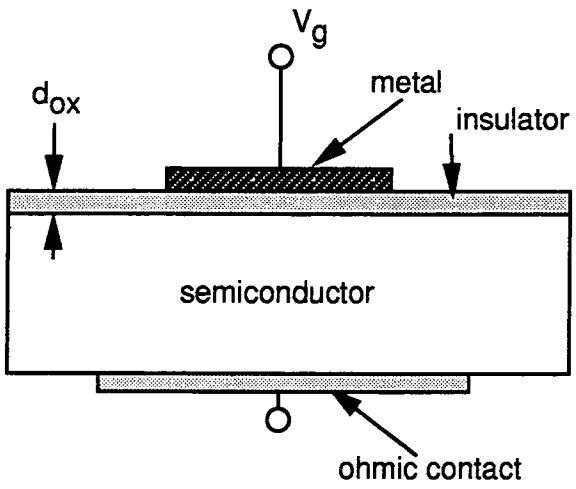

Figure 2.1 The structure of an ideal MIS diode.

the effects of external conditions such as illumination are explained.

2.2 The ideal equilibrium MIS diode

2.2.1 Structure of an ideal MIS diode

The structure of an ideal MIS diode is shown schematically in Figure 2.1, where d_{ox} is the thickness of the insulating layer and V_g is the bias voltage applied to the metal with respect to the semiconductor. Often this voltage is termed the gate voltage, hence the symbol, V_g. The insulator in this case has an extremely high resistance, for example, a thick layer of silicon dioxide.

2.2.2 Ideal MIS diode under zero bias

The energy band diagram of an ideal MIS diode is shown in Figure 2.2. The energy bands are flat and this condition is known as 'flatband'. This is a rare situation in which there is no work function difference between metal and semiconductor.

$$\phi_{ms} = \phi_m - \phi_s \tag{2.1}$$

where ϕ_m and ϕ_s are the metal and silicon work functions, respectively. At flatband ϕ_{ms} is zero. From the diagram it can be seen that ϕ_{ms} is also given by

$$\phi_{ms} = \phi_m - (\chi + \frac{E_g}{2q} - \phi_B) \tag{2.2}$$

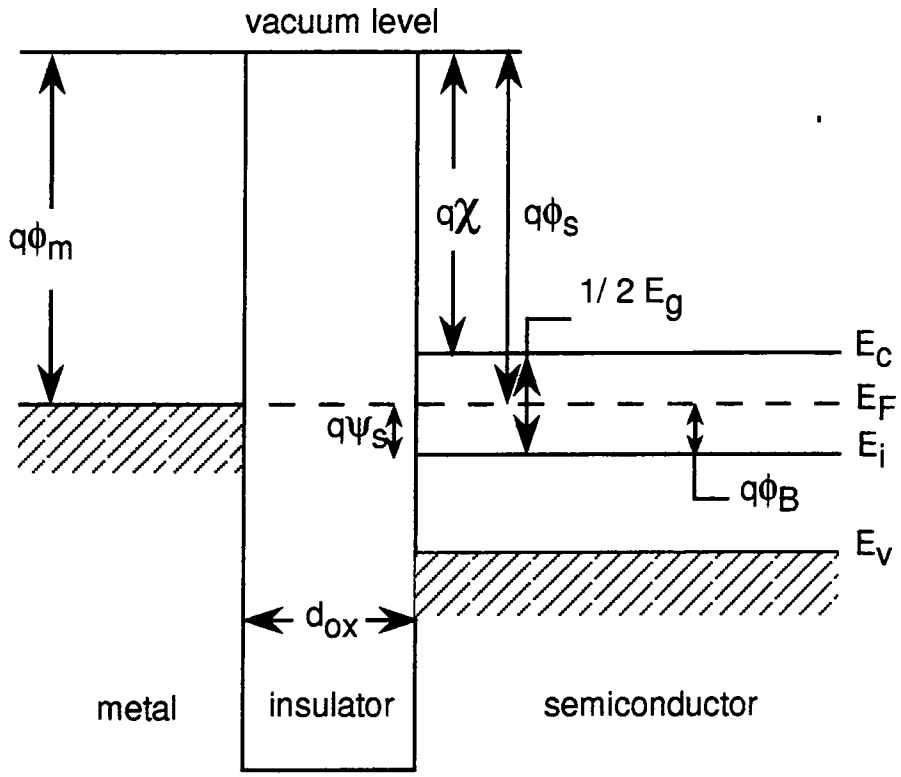

Figure 2.2 Energy band diagram for ideal MIS diode under zero bias, i.e. $V_g = 0\,V$.

where χ is the electron affinity of silicon, E_g is the silicon energy gap and ϕ_B the potential difference between the Fermi level E_F and the intrinsic level, E_i, in the bulk of the semiconductor. When the energy bands are flat, the potential at the silicon surface, Ψ_s has the same value as that in the bulk of the semiconductor, ϕ_B. In this condition the numbers of electrons and holes at the semiconductor surface, are the same as those throughout the bulk. For n-type silicon the number of carriers is given by

$$N_D = n_i \exp\left(\frac{q\phi_B}{kT}\right) \tag{2.3}$$

where n_i is the intrinsic number of electrons at thermal equilibrium, N_D is the donor impurity concentration, k is the Boltzmann constant and T is the absolute temperature.

The insulator and semiconductor are in series and therefore any applied voltage would be dropped partly across the oxide, V_{ox} and partly across the silicon surface, Ψ_s. The voltage dropped across the MIS device, V_{MIS}, is therefore

$$V_{MIS} = V_g = V_{ox} + \Psi_s = 0 \tag{2.4}$$

Since there is no charge stored within the oxide or at its interfaces, once a bias voltage is applied any charge on the metal is balanced by an equal and opposite charge on the semiconductor.

2.2.3 Ideal MIS diode under forward bias

If V_g is positive the MIS structure is **forward biased** for an **n-type** silicon substrate. Figure 2.3(a) shows the energy band diagram for this situation. By convention since electron energy increases in the upward direction an arrow pointing up denotes a negative applied potential and an arrow pointing down a positive potential. If the electric field resulting from such an applied potential is assumed not to alter the density of states of electrons in the conduction band then the band bending approximation can be applied and the energy levels are shifted with respect to the Fermi level as shown in Figure 2.3(a). With increased forward bias the diagram shows that the conduction band bends towards the Fermi level. This increases the number of electrons at the insulator-silicon interface, given by

$$n_s = n_i \exp\left(\frac{q\Psi_s}{kT}\right) \tag{2.5}$$

where Ψ_s can be seen from Figure 2.2 to be

$$q\Psi_s = E_F - E_i \tag{2.6}$$

Ψ_s is the potential at the surface with respect to the bulk of the semiconductor and represents the total band bending. Since there is a wider gap between E_F and E_i at the surface compared with the bulk of the semiconductor, there is a difference in the potentials at the surface and in the bulk. This difference increases as the number of electrons at the surface increases. The condition is known as accumulation, since the majority carriers accumulate at the semiconductor surface. The negative charge at the semiconductor surface is balanced by an equal positive charge on the metal and the MIS device acts as a capacitor. The voltage dropped across the semiconductor surface is negligible. The silicon has so many carriers accumulated on its surface it acts like a metal. Almost all of the applied voltage is therefore dropped across the relatively high resistance of the insulator.

$$V_{MIS} = V_{ox} + \Psi_s \approx V_{ox} \tag{2.7}$$

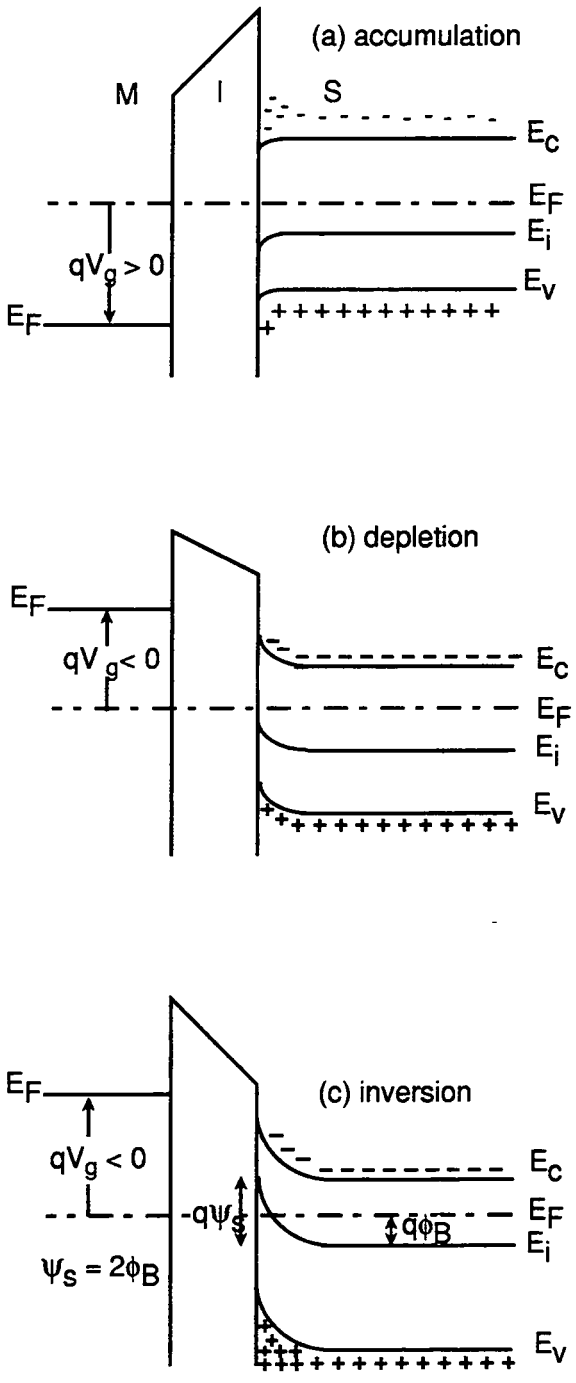

Figure 2.3 Energy band diagram for an MIS structure showing (a) accumulation, (b) depletion and (c) inversion.

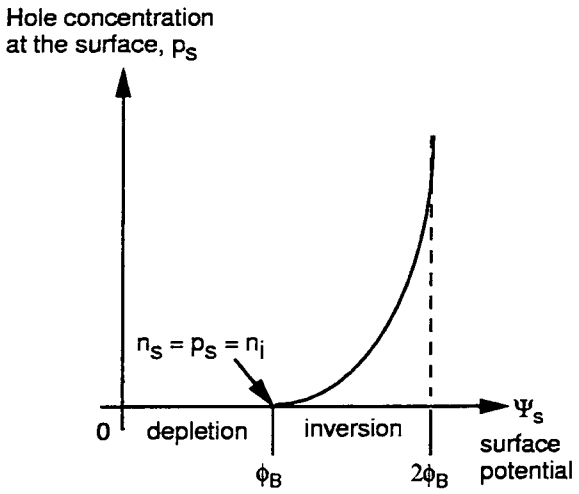

Figure 2.4 Point of inversion.

2.2.4 Ideal MIS diode under reverse bias

Depletion

With a negative voltage applied to the metal the bands bend upwards as shown in Figure 2.3(b). The majority carriers are swept away from the semiconductor surface leaving behind the positively charged donor ions. This condition is known as depletion. For the MIS structure in depletion

$$V_{MIS} = \Psi_s + V_{ox} \tag{2.8}$$

Inversion

Inversion is shown in Figure 2.3(c). If a large negative voltage is applied to the metal the bands bend even more. The MIS structure is in **strong** inversion if the intrinsic Fermi level at the surface is below the Fermi level by an amount ϕ_B. The surface potential $\Psi_s = 2\phi_B$, as shown in Figure 2.3(c). For strong inversion, as the field across the oxide increases, the inversion layer supplies any increased charge necessary to absorb any increase in surface field strength. The width of the depletion region is now independent of voltage. The inversion region therefore becomes important when the hole density exceeds the ionised donor density, as shown in the Figure 2.4. At the onset of inversion the maximum depletion layer width is reached.

$$\Psi_s = 2\phi_B = \frac{qN_D}{2\epsilon_s} w_{max}^2$$

$$w_{max} \approx \left(\frac{4\phi_B \epsilon_s}{qN_D}\right)^{1/2}$$
$$\phi_B = \left(\frac{kT}{q}\right)\ln\left(\frac{N_D}{n_i}\right)$$

and therefore

$$w_{max} \approx \left[\frac{4\epsilon_s kT}{q^2 N_D}\ln\left(\frac{N_D}{n_i}\right)\right]^{1/2} \tag{2.9}$$

Ψ_s, w_{max} and ϕ_B have been determined as 0.64 V, 411 ± 30 nm and 0.32 ± 0.02 V for p-type and approximately 0.68 ± 0.03 V, 300 ± 30 nm and 0.34 ± 0.02 V for n-type. The range in values is due to the range of resistivities ($1.8 - 2.2\,\Omega$ cm for p-type silicon and $6 - 13\,\Omega$ cm for n-type) quoted by the wafer manufacturer. This corresponds to a doping level of approximately 5×10^{15} cm^{-3} for p-type silicon and $10^{15} - 10^{16}$ cm^{-3} for n-type silicon. The voltage dropped across the device is now divided between the oxide layer and the silicon, i.e.

$$V_{MIS} = V_{ox} + \Psi_s \tag{2.10}$$

Assuming no charge at the interface, the displacement across the silicon-silicon dioxide interface is continuous.

$$\epsilon_{ox}\mathcal{E}_{ox} = \epsilon_s \mathcal{E}_s$$
$$\epsilon_{ox}\frac{V_{ox}}{d_{ox}} = \epsilon_s \frac{\Psi_s}{w_{max}}$$

The potentials and electric fields are as shown in Figure 2.5 for a p-type silicon substrate.

2.3 Capacitance-voltage curves

Ideal MIS curves with a good insulating oxide produce the high and low frequency capacitance versus gate voltage curves shown in Figure 2.6 [2]. There are three distinct regions to the curves and these represent accumulation, depletion and inversion of the semiconductor surface. The characteristic shape of these curves is described below and shown in Figure 2.6.

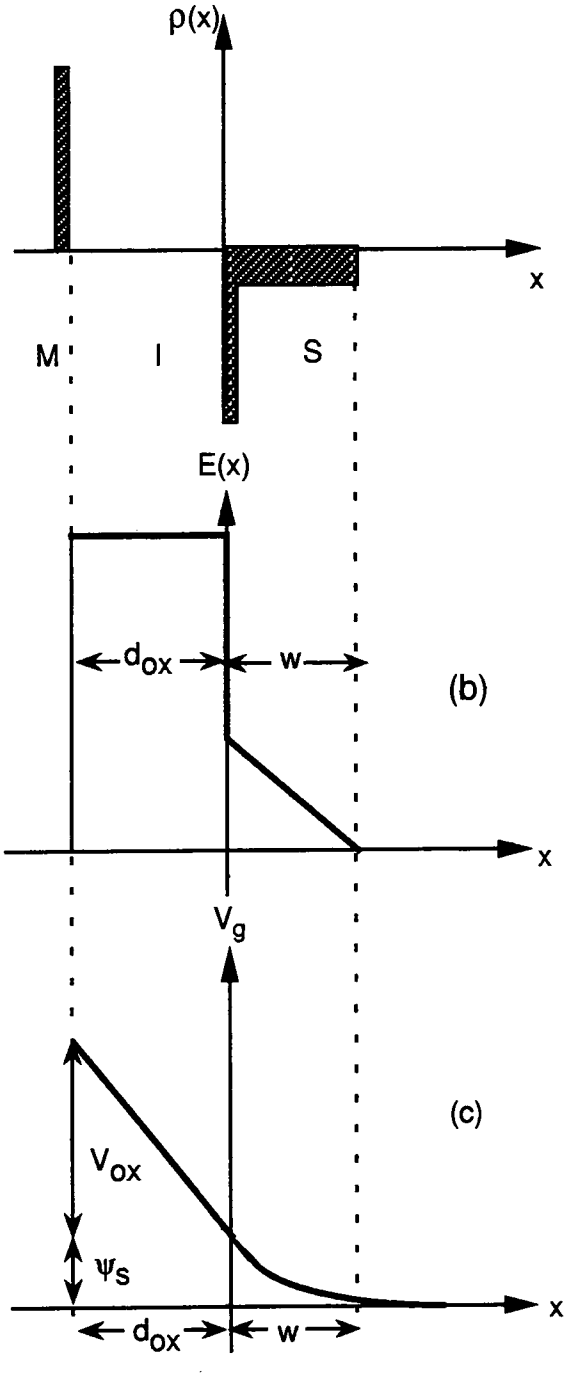

Figure 2.5 Theoretical charge layers, electric and potential fields across silicon-oxide interface for an MIS with a p-type substrate in reverse bias.

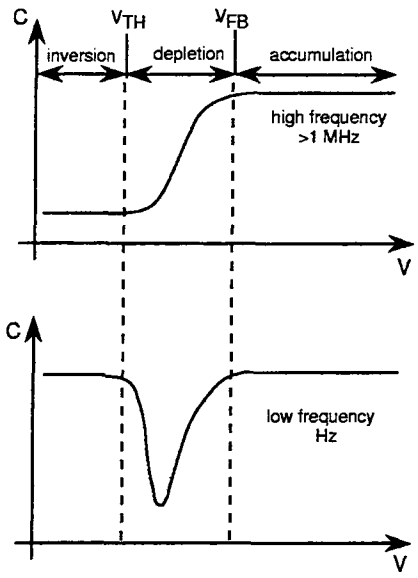

Figure 2.6 Ideal C-V curves.

2.3.1 Accumulation

The majority carriers in the semiconductor are attracted to the oxide-silicon interface by a gate voltage of opposite sign. This interface contains a thin, highly concentrated layer of charge equal in area to the top contact. The resulting capacitance,

$$C_{MIS} = C_{ox} = \frac{\epsilon_{ox} A_{gate}}{d_{ox}} \tag{2.11}$$

is determined by the gate area, A_{gate} and the oxide thickness, d_{ox}.

2.3.2 Depletion

In depletion, the capacitance changes rapidly with gate voltage. The gate voltage repels the majority carriers and so forms a thicker insulating layer between the effective capacitor's plates. The resulting capacitance

$$C_{MIS} = \frac{\epsilon_{ox} A_{gate}}{d_{ox} + w} \tag{2.12}$$

is determined by the gate area, A_{gate}, the oxide thickness, d_{ox} and the width of the depletion region, w.

2.3.3 Inversion

At the onset of inversion, the minority carriers out number the majority carriers and the capacitance is again

$$C_{MIS} = C_{ox} = \frac{\epsilon_{ox} A_{gate}}{d_{ox}} \tag{2.13}$$

at low frequency. The minority carriers are slow and cannot respond to high frequencies, the resulting build-up of charge is low and the capacitance has a low value.

2.4 Non-idealities in equilibrium MIS structures

2.4.1 Introduction

Real MIS devices do not have the same energy band diagrams or C-V curves as those described above. This non-idealistic behaviour comes from the structure of the device. Ideally there is a sudden change in energy gap, from 1.1 eV of silicon to a large forbidden gap of the insulator (9 eV for silicon dioxide), across the whole device. If the junction is not abrupt there may be localised areas where the true width of the oxide is different from the ideal case. This changes the capacitance. Gradual transitions introduce new electron energy levels in the forbidden gap of the insulator at the interface. Even in an ideal MIS diode, the sudden change in the silicon atomic periodicity at its surface introduces new electron energy levels. The silicon-oxide interface may, therefore, contain a charge layer. This charge resides in energy levels called interface states. During MIS device manufacture the clean silicon surface, covered in a layer of dangling bonds, is likely to become contaminated and the contaminants can cause additional energy levels within the forbidden gap. These impurities can trap electrons or donate them. The insulator is an amorphous material and may therefore contain energy levels within the forbidden gap. Interface states and trap levels are specific to the particular chemical treatments used in device manufacture and are often beyond the control of the manufacturer. The effects of such changes are described in detail later.

Some changes are within the control of the experimentalist. Obviously, in an MIS device there are three different classes of materials. There are a number of elements that can make up the metal and semiconductor layers and a wide range of materials that can be used as the insulator. The resistivity of the insulator may be extremely high, as in capacitor manufacture, or a semi-insulator may be used. An MIS device with a conductive I layer would be unable to store charge. The more

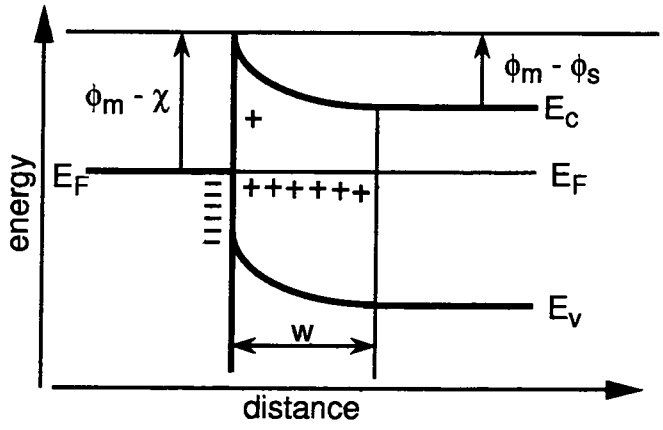

Figure 2.7 Metal-n-type semiconductor junction in contact $\phi_m > \phi_s$

conductive the semi-insulator, the closer the band structure becomes to that of the semiconductor. The difference in the energy levels of the conduction bands of the semiconductor and the semi-insulator therefore can be varied. ϕ_{ms} can be altered by using various electrode materials on n- and p-type silicon of differing doping densities. These combinations often produce charge layers at the oxide interfaces. Such charge layers affect the device capacitance, the energy band diagrams and the flow of current through the device.

Considerations of the effect on current flow has been left for discussion in Chapter 3. The effects of these non-idealities on the energy bands and capacitance values are discussed in the following sections.

2.4.2 The effect of metal work function

The Schottky barrier

Whenever a metal and a semiconductor come into contact electrons flow from one material to the other until the Fermi levels align and equilibrium is established. If $\phi_m > \phi_s$ and the semiconductor is n-type then the semiconductor surface becomes depleted. The bands in the silicon bend as in Figure 2.7. The amount of band bending is determined by $\phi_m - \phi_s$. As the diagram shows the barrier $(\phi_m - \chi)$ for electrons crossing from metal to semiconductor is larger than the one separating the semiconductor from the metal, which is $\phi_m - \phi_s$. This uneven barrier is termed a Schottky barrier. A Schottky barrier is created with a metal and p-type silicon when $\phi_m < \phi_s$.

Once a voltage is applied to the system it is no longer in equilibrium and a current

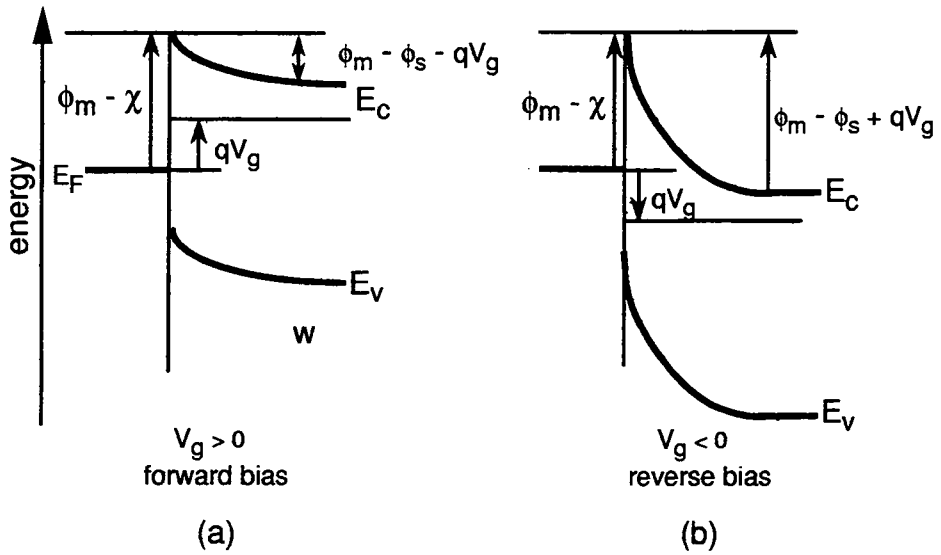

Figure 2.8 Metal-n-type semiconductor junction in contact $\phi_m > \phi_s$: (a) $V_g > 0$ i.e. the metal is positively biased with respect to the semiconductor, forward biased: (b) $V_g < 0$, reverse biased.

flows. The current size is dependent on voltage polarity. Figure 2.8 shows the effect on barrier heights of voltage polarity for n-type silicon. There is a very resistive space charge region. All of the applied voltage appears across this region and the bands in the interior of the semiconductor remain flat but are shifted in energy level. The resulting difference in barrier heights gives rise to rectifying behaviour and for this reason metal-semiconductor contacts are called Schottky diodes.

The MIS system

The effects of changing the top contact metal used with n- and p-type substrates are described by reference to typical energy band diagrams. The voltages required to produce zero bias, flatband, accumulation, depletion and inversion are shown for values of ϕ_{ms} other than zero. The equations which describe the various states of the semiconductor must change in order to accommodate the value for ϕ_{ms}. At flatband V_{MIS} is no longer zero.

$$V_{MIS} = V_{FB} = \phi_m - \phi_s = \phi_{ms} \tag{2.14}$$

With an applied bias

$$V_{MIS} = \phi_{ms} + \Psi_s + V_{ox} \tag{2.15}$$

ϕ_{ms} affects the value of Ψ_s and so alters the band bending. In addition, the number of free carriers alter since Ψ_s is changed. Figure 2.5 was modified to take into account the effect of ϕ_{ms}. The result is shown in Figure 2.9 for an n-type MIS device. The effects of positive and negative ϕ_{ms} values on the energy bands of the MIS system are detailed below.

P-type silicon

Negative ϕ_{ms}

In Figure 2.10(a) the Fermi level is shown as being constant, corresponding to equilibrium conditions. With no applied bias and negative ϕ_{ms}, the energy bands of the semiconductor bend and the hole density near the surface reduces. The semiconductor is in depletion. The depletion region contains the immobile negative acceptor ions. Neutrality requires that the acceptor charge be balanced by the electronic charge existing on the surface of the metal. (No band bending occurs in the metal because of the very much higher density of free carriers.)

A small negative applied voltage would result in the flatband condition (shown earlier in Figure 2.2) where the charge density is zero throughout the structure and $V_g = \phi_{ms}$. This gate voltage would precisely cancel out the difference in the work functions.

Figure 2.10(b) shows that when V_g is more negative the charge on the metal is negative and holes accumulate at the semiconductor surface to produce a p^+ layer or an accumulation region.

Figure 2.10(c) shows that when a large positive voltage is applied to the metal, holes are repelled and electrons are attracted to the silicon-oxide surface so that an n-type layer is formed in the p-type substrate, i.e. an inversion layer is formed.

Positive ϕ_{ms}

A positive work function difference changes the silicon surface charge completely. For zero bias the silicon surface is accumulated. To achieve flatband a small positive voltage is required, i.e. $V_g = \phi_{ms}$, and a larger negative voltage is needed to cause inversion. For any gate voltage value below zero, charge accumulation and current flow would be higher than for the negative ϕ_{ms} case. However, in reverse bias a larger voltage would be required to cause the same level of current flow. Similar energy band diagrams result for n-type silicon devices.

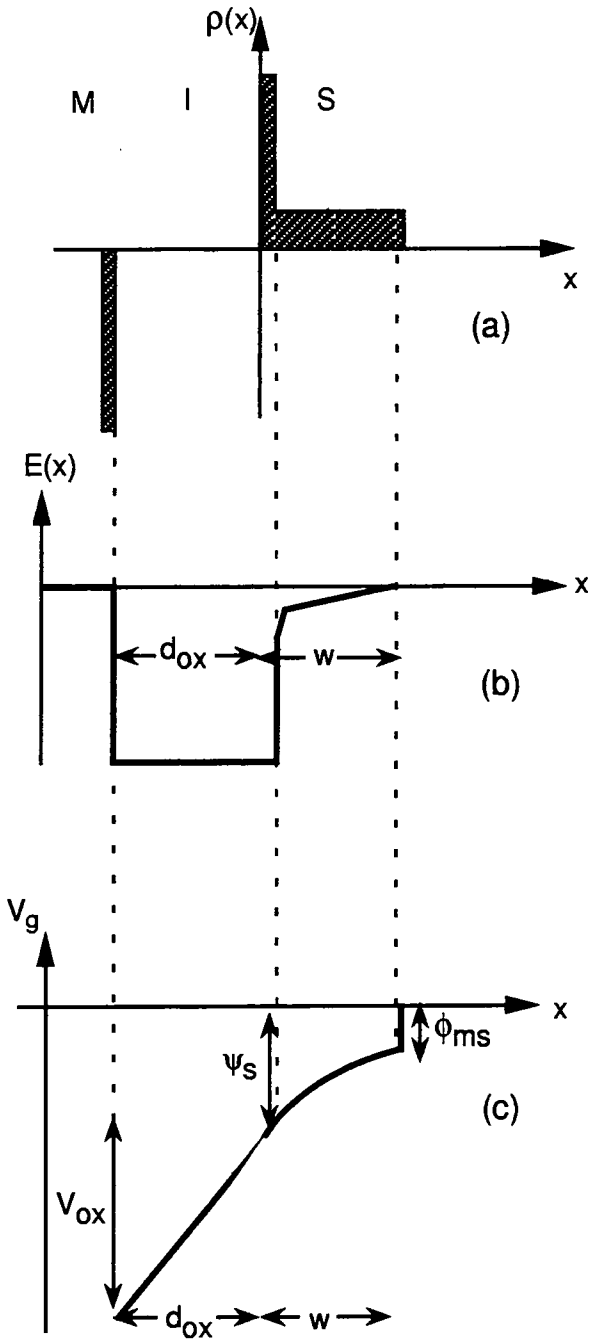

Figure 2.9 Theoretical charge layers, electric and potential fields across silicon-oxide interface for an MIS with a n-type substrate in reverse bias.

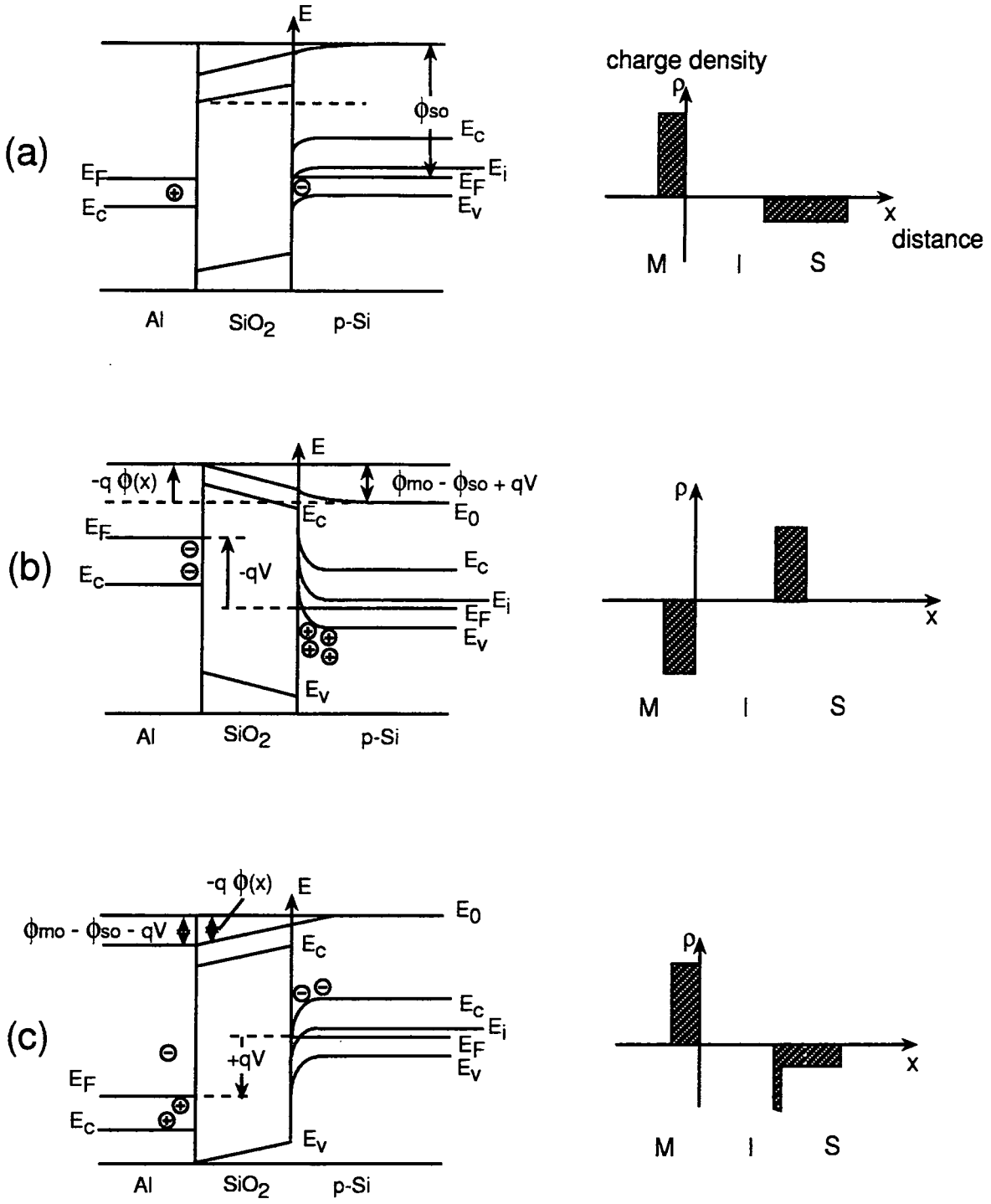

Figure 2.10 Simplified energy band diagrams for a p-type silicon MIS structure showing the effect of various gate voltages on band shape and charge density in the absence of any oxide charge and assuming $\phi_{ms} < 0$: (a) zero gate voltage, (b) negative voltage and (c) positive voltage.

Material	Contact potential (V)
Al	-0.6
Au	0.3
Si(intrinsic)	0.0
Si(p-type)	0.07

Table 2.1 Approximate theoretical contact potential of materials with intrinsic silicon (ϕ_{ms}) [3].

Element	Work function (V)
Si	4.9
Al	4.4
Au	5.1
Cr	4.6
Mo	4.8

Table 2.2 The metal work functions ϕ_m for **clean** metal surfaces deposited in a vacuum [4].

Values for ϕ_{ms}

Theoretical values of ϕ_{ms} are shown in Table 2.1 for various elements in close contact with intrinsic silicon. From this, theoretical values of ϕ_{ms} for aluminium-oxide-p-type silicon are $-0.6 - 0.07 = -0.67\,\text{V}$ and $+0.3 - 0.07 = 0.23\,\text{V}$ for gold-oxide-p-type silicon. Completing the same calculations using the experimental vacuum work functions from Table 2.2 yields values of -0.57 and $+0.13\,\text{V}$, respectively. There is a difference in the values of ϕ_{ms} for each of the two systems. In fact, different methods of measuring ϕ_m produce results which can vary by nearly as much as 1 V [4].

Deposited metal films are polycrystalline and the oxide metal interface is very different from the vacuum metal (single crystal) interface used to produce Table 2.2. Schottky barrier heights for vapour deposition of pure metals onto chemically cleaned silicon in a vacuum have been measured at 300 K. The results are shown in Table 2.3. These conditions are closer to those used by experimentalists but the values are just a **guide** as to which metal contact has the highest barrier to electron flow. Theoretical calculations of ϕ_{ms} yield values which differ from those of real systems. Pollack and Morris [5] measured J-V curves for a supposedly symmetrical system: $\text{Al} - \text{Al}_2\text{O}_3 - \text{Al}$. They found that the barrier heights were not identical (at 1 and 1.5 V in forward and reverse bias). This difference is due to the structure of the

Element	ϕ_{ms}, n-type Si (V)	ϕ_{ms}, p-type silicon (V)
Au	0.8	0.34
Al	0.72	0.58
Mo	0.68	0.42
Cr	0.61	0.50

Table 2.3 Metals and their Schottky barrier heights

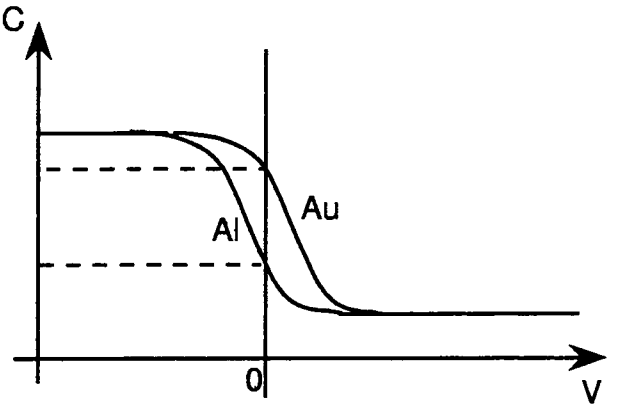

Figure 2.11 C-V curves used by Sze to measure the difference in metal work functions [4]

interfaces. The junction between the electrode and the grown oxide would be less abrupt than that between the oxide and the deposited metal.

Sze [4] reported metal work functions of MIS diodes using photoresponse and C-V measurements. If two metals are deposited as field plates on the same oxidised silicon sample then the displacement in the C-V curves, as shown in Figure 2.11, represents the difference in the metal work functions. Hence if the value ϕ_m for any one metal is known the ϕ_m values for the other metals can be determined. The results for n-type silicon and an oxide of SiO_2 are summarised in Table 2.4. These metal work functions are assumed to be the closest to those of the M-SRO-Si diodes investigated here.

Metal	ϕ_m (photoresponse) (V)	ϕ_m(C-V) (V)	ϕ_m (vacuum)
Al	4.1	4.1	4.25
Au	5.0	5.0	4.80

Table 2.4 Measured metal work functions ϕ_m for MIS devices. Silicon dioxide has a bandgap of 9 eV and an electron affinity (q χ) of 0.9 eV. The values given in the table for ϕ_m consist of the barrier height plus SiO_2 electron affinity [4].

Metal	ϕ_m (V)	ϕ_{ms} (p-type) (V)	ϕ_{ms} (n-type)
Si_p	4.9	-	-
Si_n	4.3	-	-
Al	4.1	-0.8	-0.2
Au	5.0	+0.1	+0.7
Cr	4.6*	-0.3	+0.3
Mo	4.8*	-0.1	+0.5

Table 2.5 Estimated ϕ_{ms} for M-SRO-Si devices * These values have been taken from Table 2.2 and may be too high since the other metal work functions have a reduced value when compared with that given in Table 2.2

ϕ_s has been calculated for the silicon wafers used in this research. Using the doping densities quoted earlier in this Chapter and equation 2.3

$$\phi_B = \frac{kT}{q} \ln\left(\frac{N_D}{n_i}\right) \tag{2.16}$$

Assuming n_i is $1.6 \times 10^{10} cm^{-3}$ at 300 K [6], ϕ_B is 0.286 V for the p-type wafers at 300 K, then ϕ_s can be calculated using equation 2.2

$$\phi_s = \chi + \frac{E_g}{2q} + \phi_B = 4.9 \pm 0.01\,\text{V}. \tag{2.17}$$

ϕ_B for the n-type wafers is 0.346 V at 300 K. Using equation 2.2, ϕ_s is

$$\phi_s = \chi + \frac{E_g}{2q} - \phi_B = 4.3 \pm 0.1\,\text{V}. \tag{2.18}$$

Using the values calculated above and those of Table 2.4 ϕ_{ms} may be estimated in Table 2.5 By an appropriate choice of the top contact metal it should be possible to vary n- and p-type silicon surfaces from accumulation to depletion at zero bias. Referring to Table 2.5, aluminium should accumulate n-type and deplete p-type surfaces in the M-SRO-Si devices whereas gold should deplete n-type and accumulate p-type silicon. Chromium and molybdenum are expected to deplete both n- and p-type.

The work functions are only estimated values and therefore it is difficult to say precisely how the top electrode material will affect device behaviour. For n-type devices, aluminium is expected to require the lowest positive gate voltage to the same current flow in forward bias, then chromium and then molybdenum. In reverse bias aluminium would require the highest bias, then chromium with molybdenum needing

the least.

Real values of ϕ_{ms} may be quite different from those shown in Table 2.5. The oxide layer is not SiO_2 and ϕ_{ms} changes with each system used to grow the oxide films. Real MIS devices are likely to have contamination of the insulating layer and also the metal-oxide interface. Some interfaces have been found to have so many electron traps that the electrons vacate or occupy the traps with applied bias. The semiconductor surface may be completely screened from the gate voltage. In addition, charges stored in the oxide could have a greater effect on the silicon surface than the top contact metal. These effects are briefly described in the following sections.

2.4.3 Insulator charge

Much work has been done on the metal-SiO_2-Si system since a major difficulty encountered with early MIS capacitors was that the flatband voltage was unstable under bias [7]. This drift was thought to be due to the movement of positive charge from the metal interface to the silicon interface through the oxide layer. Various models have been put forward to explain the presence of the moving ions in SiO_2, which may be due to H^+ ions, alkali ions or oxide ions. However, there is agreement that the presence of charge in the insulator is a result of the fabrication process. In general, the overall oxide charge density has been found to be positive and has been given the symbol $\rho(x)$ [9]. In addition to the charge distributed throughout the oxide, there is a fixed charge, Q_{ss}, located at the silicon-oxide interface, within 200 Å of the silicon. Q_{ss} is dependent upon the oxidation procedure used and on the orientation of the silicon crystal. Q_{ss} values have been found to be three times higher in the $<111>$ orientation compared to the $<100>$ direction for silicon dioxide on silicon [7]. There are many models for the SiO_2 interface. These include defect models that explain the presence of charge at the interface. Four different types of defect which could exist are excess silicon, excess oxygen, impurities and an oxide charge which induces an attractive Coulombic potential well in the silicon.

The total charge within the oxide is made up of $\rho(x)$ and Q_{ss}, which overall are thought to be positively charged for silicon [4]. The presence of charge within the oxide affects the energy band diagrams and the situation has been demonstrated for a positive oxide charge in the diagrams below, where the total charge is represented by an equivalent positive charge at the silicon-oxide interface.

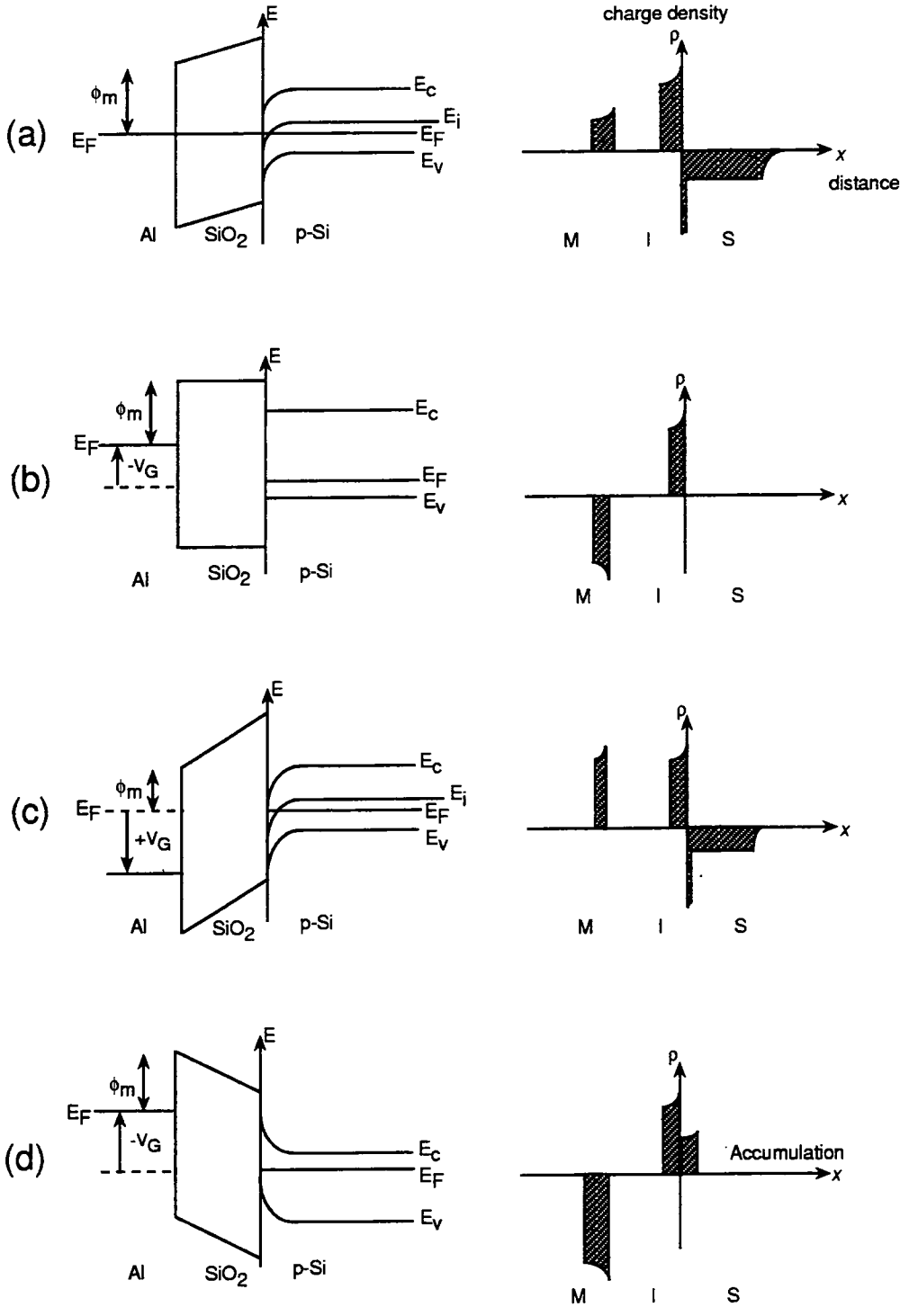

Figure 2.12 Simplified energy band diagrams showing the effect of an equivalent oxide charge (present at the **p-type** silicon-oxide interface) on the electrostatic potential, for various gate-semiconductor voltages and assuming $\phi_{ms} < 0$: (a) zero gate voltage, (b) negative gate voltage, (c) positive voltage, (d) large negative voltage.

P-type silicon

In Figure 2.12, ϕ_{ms} is negative. The resulting band bending causes depletion of the silicon surface. Normally the metal would obtain a positive charge. The presence of a positive oxide charge could counteract part, all or even exceed the negative charge on the silicon surface. The metal would therefore gain a positive, zero or negative charge, respectively. Figure 2.12(a) shows that charge neutrality demands that for large ϕ_{ms} and positive oxide charge, the p-type silicon becomes inverted.

In Figure 2.12(b) V_g is made large and negative and this causes all of the oxide charge to be balanced by the metal charge and the flatband condition occurs.

In Figure 2.12(c) When V_g is large and positive a large positive charge on the metal results and the silicon becomes inverted.

In Figure 2.12(d) a large negative voltage causes a negative charge on the metal which more than compensates for the positive oxide charge and the semiconductor is accumulated.

N-type silicon

Figure 2.13(a) shows that, with zero applied voltage, electrons transfer from metal to silicon since ϕ_{ms} is negative. The positive charge on the oxide increases the number of electrons at the silicon interface and accumulation results. For large negative voltages as shown in Figure 2.13(b) inversion results. Figure 2.13(c) shows that a positive voltage on the gate results in accumulation.

It can be seen from the above descriptions that a positive charge in the oxide would be expected to enhance the current for n-type under forward bias but reduce that for p-type substrates under forward bias. In reverse bias a larger voltage is needed to obtain inversion for n-type as compared with that required p-type substrates.
The equations for voltages around the MIS circuit now become

$$\text{Flatband} \qquad V_{FB} = \phi_m - \phi_s - \frac{Q_{ss}}{C_{ox}} - \frac{1}{C_{ox}} \int_0^{d_{ox}} \rho(x)\, dx \tag{2.19}$$

where C_{ox} is the insulator capacitance, Q_{ss} represents the interface charge and $\rho(x)$ is the density of charge trapped in the bulk of the oxide. This equation simplifies to

$$V_{FB} = \phi_m - \phi_s - \frac{Q_{ox}}{C_{ox}} \tag{2.20}$$

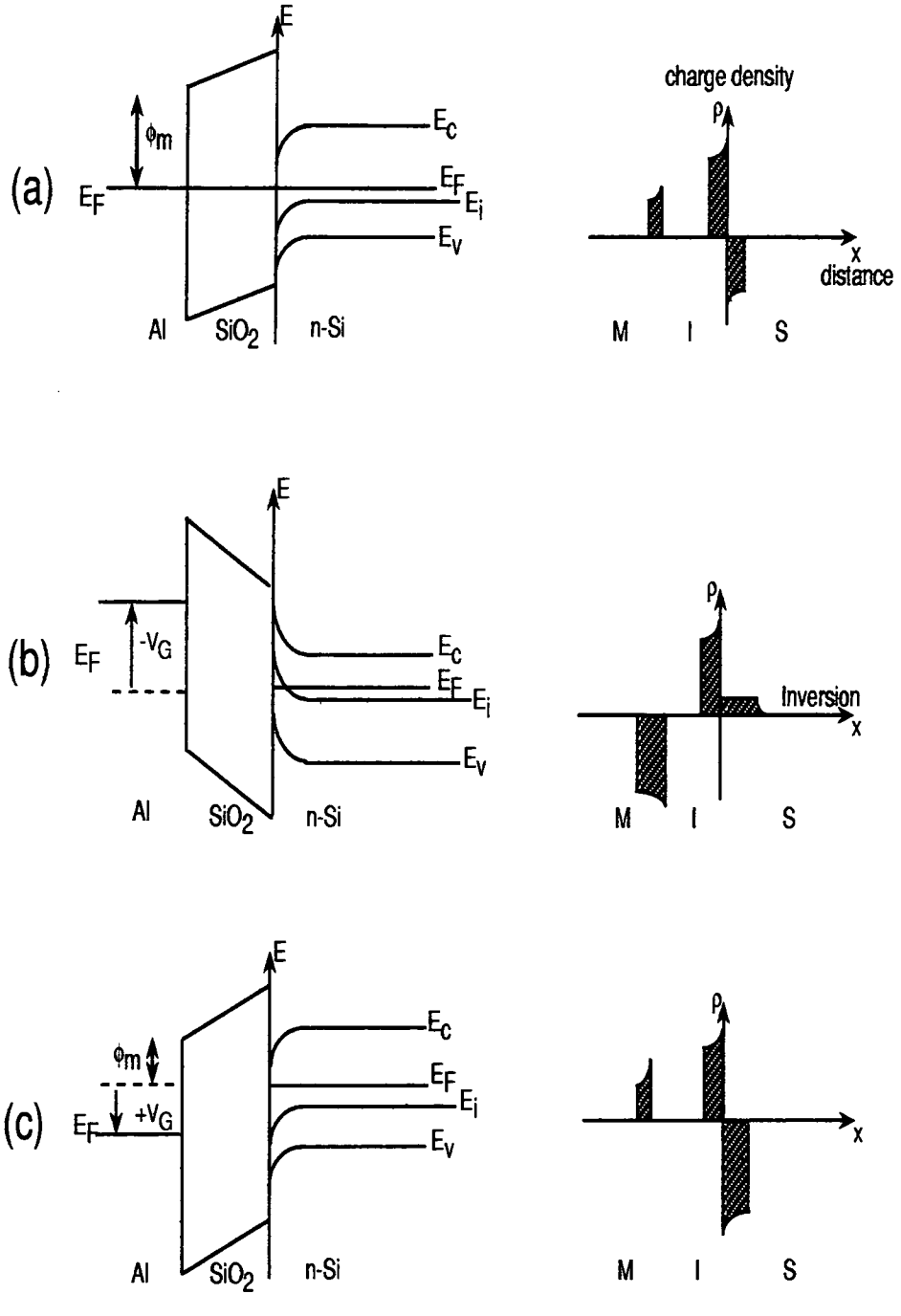

Figure 2.13 Simplified energy band diagrams showing the effect of an equivalent oxide charge (present at the n-type silicon-oxide interface) on the electrostatic potential, for various gate-semiconductor voltages and assuming $\phi_{ms} < 0$: (a) zero gate voltage, (b) inversion, large negative gate voltage, (c) positive voltage.

Q_{ox} is the equivalent charge at the interface which represents the total charge within the oxide and the interface charge.

Under bias

$$V_{MIS} = \Psi_s + V_{FB} \tag{2.21}$$

where Ψ_s was defined earlier as

$$\Psi_s = \phi_s - \phi_B \tag{2.22}$$

At the semiconductor interface the continuity of the displacement vector causes the fields in the two materials to be related by the equation

$$\epsilon_{ox}\frac{V_{ox}}{d_{ox}} = \epsilon_s \mathcal{E}_s - Q_{ox} \tag{2.23}$$

In addition to charges within the oxide traps at the silicon-oxide interface termed interface traps or sometimes fast surface states affect the energy band diagrams. These effects are described in the following section.

2.4.4 Silicon-SRO interface traps

At the silicon-SRO interface there is an abrupt termination of the silicon crystal lattice. The change in periodicity gives rise to localised changes in band structure which gives rise to discrete electron energy levels within the band gap. Figure 2.14 shows an abrupt change from the energy bands to the forbidden energy gap in the bulk silicon crystal. A more gradual change is shown for the conduction band at the silicon surface. The valence band would also have this smearing of the band edges at the silicon surface. These extra energy levels are termed extended states.

Extended states also arise due to the high reactivity of the bare silicon surface. Dangling bonds may cause the incorporation of foreign atoms, which along with minimisation of the silicon surface, produce lattice defects and deviations from stoichiometry. The electron and hole traps so created have energy levels which lie within the normally forbidden gap. Some impurity atoms are a source of positive holes which when released take part in the conduction process. Such an impurity atom is termed an acceptor centre. An acceptor is neutral when empty and negative when filled. Generally these impurities cause energy levels below E_F at a level termed E_a. Some impurity atoms are a source of electrons, these are donors. Once an electron has been lost the donor centre is positively charged and is able to trap an electron from the

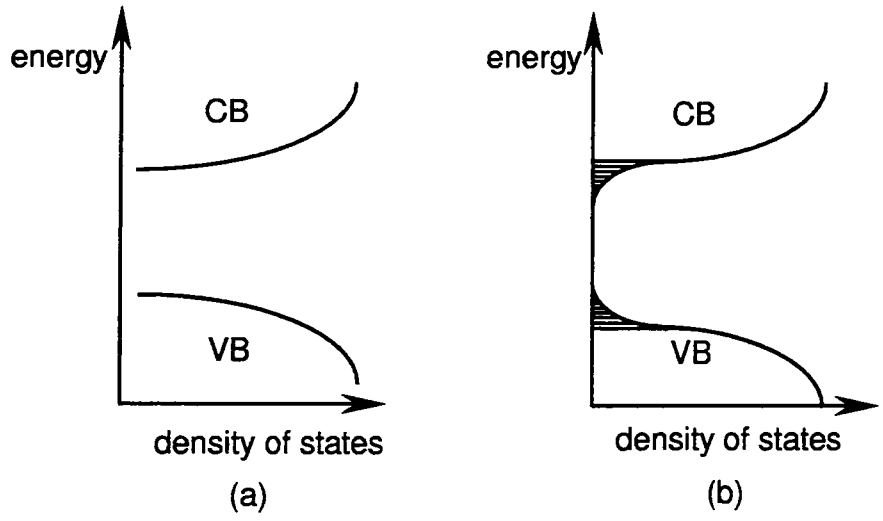

Figure 2.14 (a) Band structure without interface traps. (b) Band structure with silicon-SRO interface traps showing the extended states.

conduction band. The energy level associated with the donor, E_d lies between E_F and E_c. The energy $E_c - E_d$ is the ionisation energy of the donor.

The number of electrons in traps depends upon the trap position within the band gap, their density and their capture cross-section. Once the traps are filled, at zero bias, the area just under the silicon surface is depleted of electrons, hence in theory there is a p-type layer in n-type substrates and an enhanced p-type layer in p-type substrates. Real surfaces have contaminants and cleaning treatments affect the density of states and the energy distribution of trapping centres. Silicon tends to exhibit n-type properties due perhaps to donor impurities adsorbed by the surface.

When a bias voltage is applied band bending occurs and changes the occupancy of the interface states, as shown in Figure 2.16. The trap levels move up or down with the valence or conduction bands. A change of charge in an interface trap occurs when it crosses the Fermi level as shown in Figure 2.15 [9]. In accumulation, the bands are pulled downwards in n-type silicon and the valence band moves away from the Fermi level. More electrons are trapped. In depletion some states emit their trapped electrons. The value for Ψ_s is altered by the presence or lack of trapped electrons. A different applied bias is needed to cause the same value of Ψ_s which would occur in the ideal MIS case. Most of the work in this research has been undertaken with samples that have not been annealed. Grove [7] suggests that the interface states of such samples tend to lie near the valence and conduction band edges and therefore do not affect the characteristics of the semiconductor devices. The positive ions present in oxide layers upon silicon may be counteracted by the negative charge layers expected

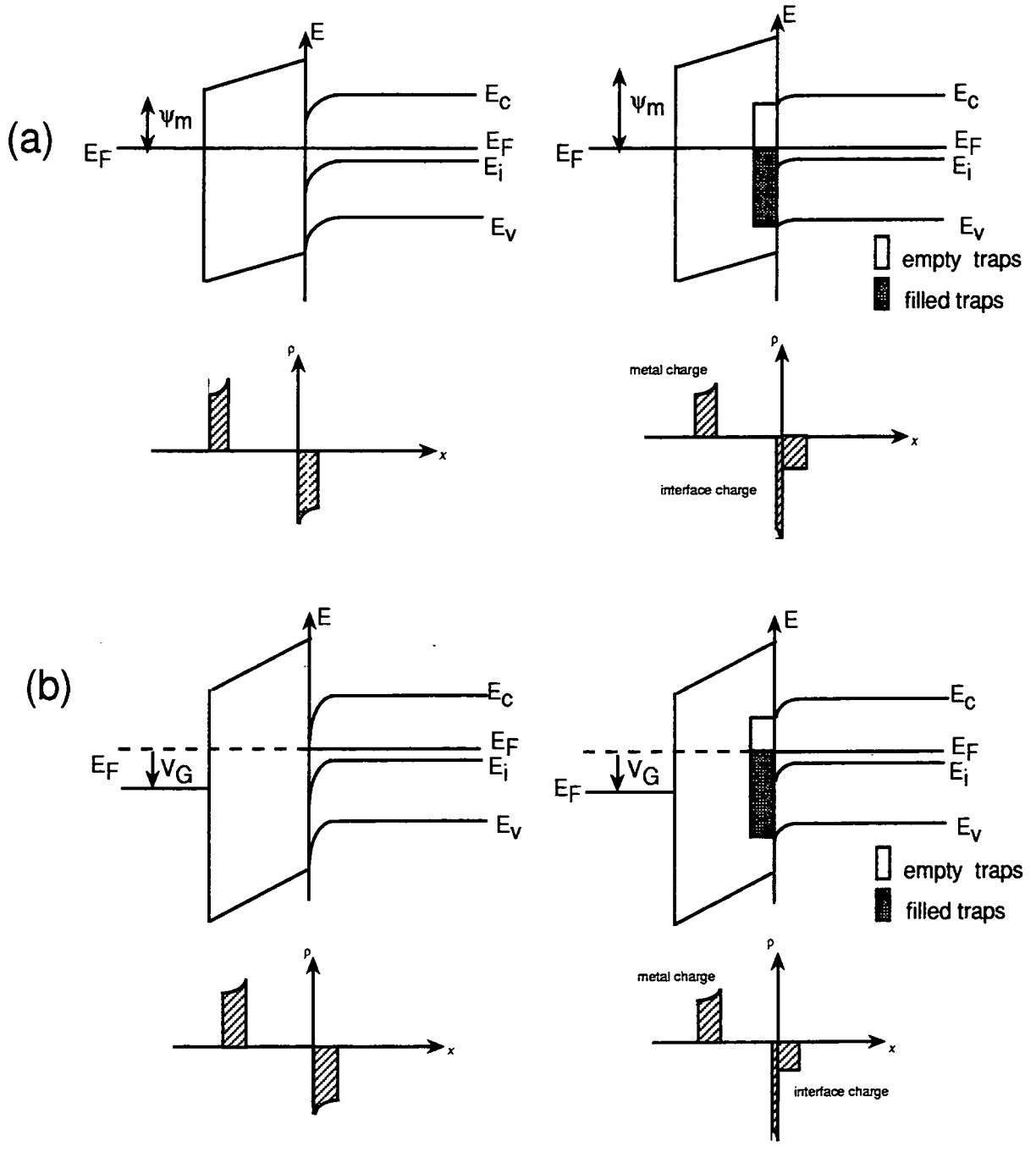

Figure 2.15 Effect of interface traps on energy band diagrams for MIS structures ($\phi_{ms} <$ 0 and for n-type silicon). Left diagrams without traps, right diagrams with traps (a) gate voltage is zero, (b) positive.

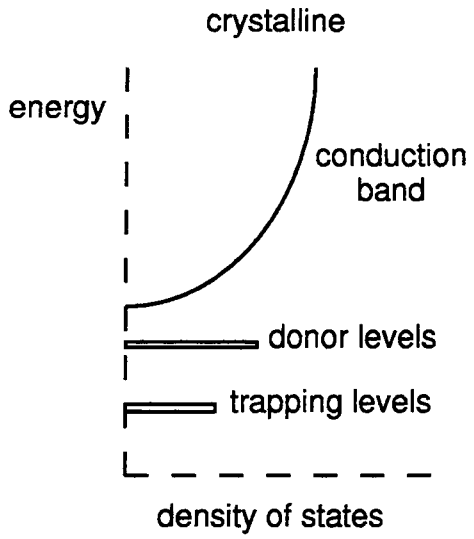

Figure 2.16 Localised states within the forbidden gap.

to occur at the silicon-SRO interface.

2.4.5 Interface traps and capacitance

Traps located at the silicon-oxide interface may be charged or discharged. When charged they increase the device capacitance. Some traps may respond slowly to changes in gate voltage and therefore they affect device capacitance at high frequencies but not at low frequencies. The larger the gap between the high and low frequency plots the greater the number of traps.

2.4.6 Traps within bulk SRO

Like SiO_2, SRO is thought to be an amorphous material with an inherent defect nature. The stresses present in SRO induce further trapping centres. Amorphous materials show a smearing of valence and conduction band edges, due to a lack of long range order. There is a transition from the continuous nature of the conduction and valence bands to strictly localised states (density of states tail) [8], shown previously in Figure 2.14. Traps within the bulk of the oxide cause localised energy levels within the forbidden gap as shown in Figure 2.16. The number of traps and their energy levels determine the position of the Fermi level in the insulator. The localised energy states have a lower activation energy for conduction than would occur in a trap-free insulator. This has been found to correspond to less than $1/2\,E_g$ [8] and therefore a higher conductivity results.

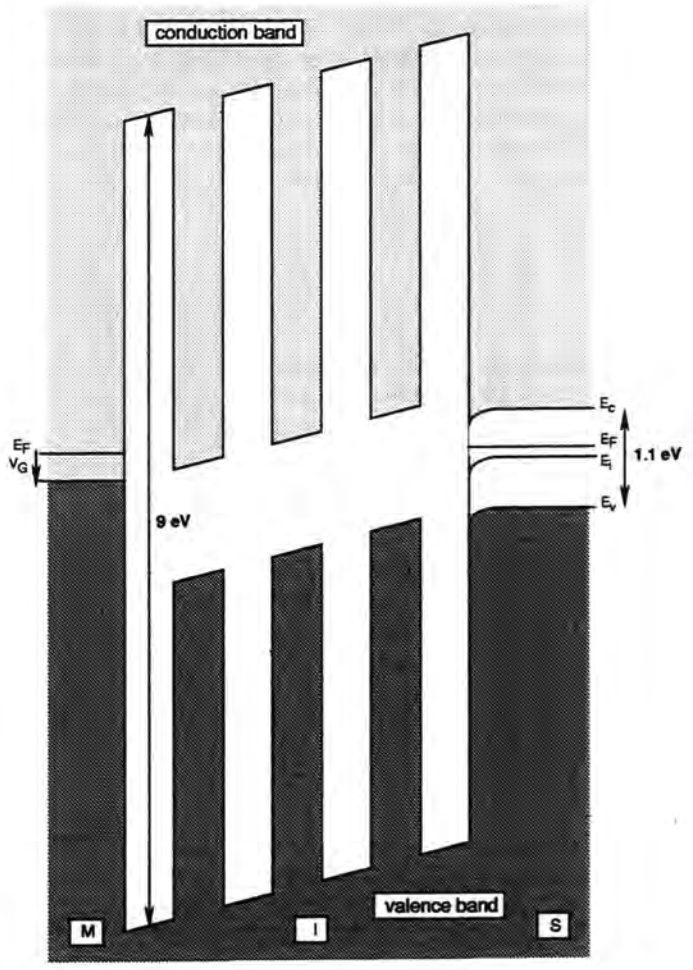

Figure 2.17 MIS band structure with silicon-rich oxide as the semi-insulator.

The structure of SRO has been postulated by many [10–16] to consist of amorphous regions of SiO_x, within which are embedded tiny silicon islands. These crystallites together with traps within the bulk of the insulator reduce the energy gap from 9 eV for stoichiometric SiO_2 to less than 1.1 eV for silicon crystallites. The insulator therefore has a variable energy gap. A typical energy band structure is depicted in Figure 2.17. This band structure has implications for the conductivity of the insulating layer.

2.4.7 Effect of temperature

Temperature increases should increase the number of current carriers in the MIS diode and so the conductivity would be expected to increase at all biases. The effect of temperature is discussed in more detail in Chapter 3.

2.4.8 Effect of illumination

The effect of light falling on an MIS device also increases the number of current carriers. It is particularly important in reverse bias. The generation of electron-hole pairs at the surface causes a decrease in Ψ_s for a given applied bias. This reduces the depletion width. To aid reproducibility, all electrical measurements were made in the dark!

2.5 A non-equilibrium non-ideal MIS diode

If the insulator in an MIS structure is **very** thick, a capacitor is formed. At the other extreme if the insulator is **very** thin, a Schottky barrier is formed. Even if the insulator thickness is such that a very small finite current flows through the MIS, an equilibrium diode still results if the current flow is tunnel-limited or bulk-limited. In this case the majority and minority carriers flow across the oxide are in equilibrium with supply. Under reverse bias inversion still occurs, when the surface potential $\Psi_s = 2\phi_B$ as described earlier.

$$\phi_B = \frac{-kT}{q} \ln\left(\frac{N_D}{n_i}\right) \tag{2.24}$$

for n-type silicon and

$$\phi_B = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right) \tag{2.25}$$

for p-type silicon. Once inversion occurs, further increases in applied voltage are taken up by the oxide and the current increases with applied voltage. In forward bias the semiconductor is accumulated and most of the applied voltage appears across the oxide. As the bias increases the current flow increases.

A thin insulating layer, or one which is designed to be conductive, no longer follows equilibrium statistics. Current flow is not limited by the insulator but is semiconductor-limited. This is more important in reverse bias. The minority carrier diffusion from the bulk semiconductor to the semiconductor-insulator interface fails to keep pace with the increasing current flow. The resultant MIS diode is a non-equilibrium device. Inversion cannot always take place since any extra minority carriers are removed across the semi-insulator. Increased applied voltage is dropped across the semiconductor and the depletion region grows. $\Psi_s > 2\phi_B$ Figure 2.18 shows the reverse I-V characteristic with its distinctive saturation plateau. If the reverse bias increases then eventually the semiconductor would breakdown. A non-equilibrium

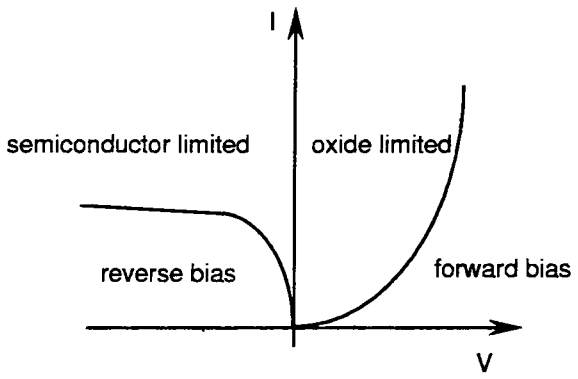

Figure 2.18 I-V characteristic for a non-equilibrium MIS device.

diode is changed to an equilibrium type by increasing the supply of minority carriers. Such an increase can be brought about by increasing the temperature, by illumination, by carrier injection through a suitably biased external electrode or in the case of the MISS device extra carriers are provided by a pn junction. In this research all such external sources have been eliminated.

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Chapter 3

Electrical Conduction Mechanisms in Thin Films

3.1 Introduction

Thin films ($< 10\,\mu$m) have been investigated for over one hundred years, but little interest was shown in this subject until the 1960s. At this time, miniaturisation of components required thin film circuits but technical difficulties delayed progress. Nowadays, improvements in vacuum technology, material purity and microelectronic fabrication techniques have led to the production of reliable MIS devices.

If the insulating layer in a MIS device is made suitably conducting, current flows through the device when a voltage is applied across it. This current flow is governed by:

(i) the size and polarity of the applied bias;

(ii) the ambient temperature;

(iii) the doping level of the silicon;

(iv) the conductivity of the semi-insulator;

(v) the quality of the contact metals; and

(vi) the properties of each of the metal-insulator and insulator-semiconductor interfaces.

In the 1960s and 70s Metal Insulator Metal (MIM) structures were widely investigated. Basic models for the behaviour of electrons in disordered thin films were

elaborated and some new models were developed. Research has shown that it is often difficult to decide which conduction mechanism predominates in a particular material. This is because many conduction mechanisms occur simultaneously. However, each mechanism is affected in different ways by changes in the temperature and applied electric field. By altering these external conditions and certain device parameters the conduction mechanisms can be separated.

Conduction mechanisms fall into two categories: those limited by the semi-insulator, i.e. bulk limited; and those limited by a metal-insulator interface, i.e. contact limited. Contact limited processes include Fowler-Nordheim, Schottky and Thermionic emissions. Bulk limited processes include Ohmic, Ionic, Space Charge Limited and Poole-Frenkel conduction. The following section outlines the salient features for each of the major conduction mechanisms.

3.2 Summary of the conduction processes

3.2.1 Electrode limited conduction

Direct tunnelling

Direct tunnelling involves an electron moving from the cathode to the anode, without at any time occupying the conduction band of the dielectric. Generally speaking a thickness of dielectric of 4 nm or less is required [1].

Thermionic emission

If the oxide layer is too thick to allow direct tunnelling, or if the barrier between the Fermi level of the metal and the conduction band of the insulator is too high, then it is possible to thermally excite electrons over the barrier, at the interface, into the insulator conduction band. This is thermionic emission. The current flow shows a strong temperature dependence.

Schottky emission

Schottky emission is thermionic emission across either a metal-oxide interface or across an oxide-semiconductor interface, where the potential barrier is not a constant but is lowered by the applied field (image force lowering), as described in Chapter 2 and Appendix A. Electrons travel from the contact at a negative potential into the conduction band of the insulator. Both the barrier and current are functions

of the applied field. The current flow shows a temperature dependence and a field dependence.

Fowler-Nordheim emission

Electrons tunnel from the metal Fermi level to the conduction band of the insulator. Image force lowering occurs in this model, which is independent of temperature. This mechanism dominates at low temperatures and high electric fields.

3.2.2 Bulk limited conduction

Ohmic conduction

The current is carried by thermally excited electrons (or holes) hopping from one isolated state within the oxide to the next. This mechanism is often the low field limit of other conduction models. The temperature dependence of electronic conductivity depends on the concentration of carriers, n, and their mobility, μ [2].

Ionic conduction

Ionic conduction is similar to a diffusion process. Generally, the dc ionic conductivity decreases with time for a constant electric field. There are two reasons for this:

(i) electrode-controlled process
After an initial current flow, positive and negative space charges build up at each interface causing a distortion in the potential distribution. When the applied field is removed some ions return to their equilibrium positions.

(ii) dielectric relaxation process
The observed initial current is that due to the ionic conductivity plus the transient current due to the relaxation of the bulk material. After this transient current has died away the remaining current is the true ionic conductivity. The field across the specimen remains uniform in this process.

If this conduction mechanism is prevalent, the resistance of the specimen changes with time. Since no such phenomenon has been observed for the Durham SRO films, this mechanism is not considered further.

Space charge limited conduction

A space charge limited (SCL) mechanism can occur in semiconductors at relatively large currents. The electrode at negative potential injects electrons into the insulator and a space charge region is formed. If the insulator is trap-free, current flow is dependent on the applied field. The conduction is Ohmic. As the applied field is increased the injection level is increased. If there are traps present, once these are filled the current increases rapidly. The energy distribution of the traps determines the shape of the current-voltage curve. Typically, at low fields the current is proportional to the voltage (ohmic behaviour). At higher fields the current is proportional to V^2 or V^n. This mechanism is therefore strongly dependent on field and is characterised by a sudden change in the current-voltage (I-V) curve at the trap filled limit.

Poole-Frenkel conduction

This is similar to Schottky emission. Applied electric fields enhance thermal excitation of electrons into the conduction band of the insulator. The barrier does not occur at the interface as in Schottky emission but lies instead within traps in the bulk of the insulator. Image force lowering reduces the potential barrier seen by the trapped electrons. The barrier lowering is usually twice that observed in the Schottky case. This mechanism is observed at high temperatures and high electric fields.

Percolation theory

The material is described as a series of barriers, which are unevenly spaced and variable in height. These barriers block current flow. When an electric field, $\mathcal{E}$, is applied, the barrier heights in the transmission direction decrease. As the field increases, the effect on current flow depends on the number of barriers at particular heights. Increasing fields overcome more and more barriers but the relationship is not necessarily a linear one, hence the non-ohmic behaviour of the current.

3.3 General models for conduction

The models most relevant to conduction in SRO are described in more detail in the following sections. These will not match experimental results perfectly but should approximate them. Theoretical models for conduction in SRO films combine some of these mechanisms and are described later in this Chapter.

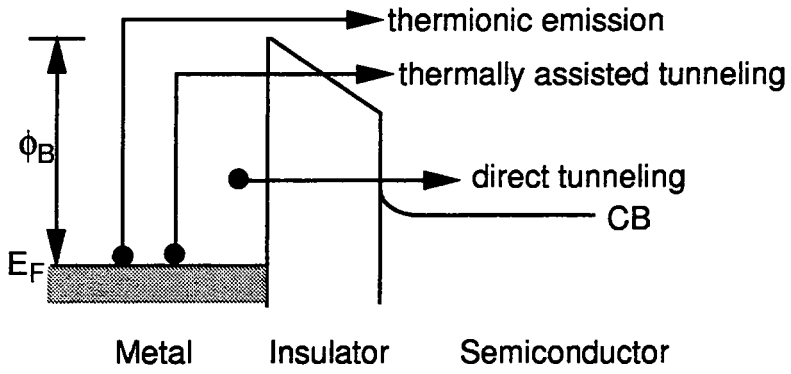

Figure 3.1 Schematic diagram showing thermionic emission, thermally assisted tunnelling and direct tunnelling.

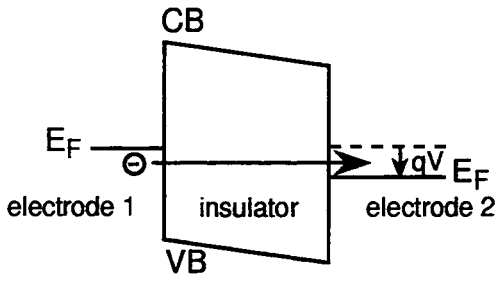

Figure 3.2 Direct tunnelling.

3.3.1 Tunnelling

Figure 3.1 summarises three conduction mechanisms, i.e. direct tunnelling, thermionic emission and thermally assisted tunnelling. Direct tunnelling occurs in extremely thin insulators. Electrons transfer from the Fermi level of one electrode to the Fermi level of the other electrode without occupying the conduction band of the insulator. This is shown in Figure 3.2. Thermionic emission may dominate at low electric fields and high temperatures. Electrons are thermally excited over the potential barrier between the metal Fermi level and the insulator conduction band. At low temperatures and high electric fields Fowler-Nordheim tunnelling occurs. The applied field lowers the potential barrier height and width at the metal-insulator interface. Between these two extremes thermally assisted tunnelling occurs. Thermally assisted tunnelling (TAT) is therefore a mixture of thermionic emission and field emission.

3.3.2 Thermionic emission

Thermionic emission dominates at low electric fields and high temperatures. The current density is determined by the number of electrons with sufficient energy to overcome the potential barrier ϕ_b. ϕ_b is the total barrier experienced by an electron moving from metal to semiconductor. A general expression for the current density for electrons moving from metal to semiconductor is [7]

$$J_{ms} = A^* T^2 \exp\left(\frac{-q\phi_b}{kT}\right) \exp\left(\frac{qV_g}{kT}\right) \tag{3.1}$$

where A^* is the Richardson constant for thermionic emission and has the value $120\,\mathrm{A\,cm^{-2}\,K^{-2}}$ and V_g is the voltage applied across the device. The electrons moving in this direction have energy supplied by the field as well as thermal energy. The total current density, J, is made up of $J_{ms} - J_{sm}$, where J_{ms} is the current density from metal to semiconductor and J_{sm} is the current density from semiconductor to metal. The barrier height with no applied voltage is the same whether the electrons travel from metal to semiconductor or vice-versa at thermal equilibrium. Therefore the reverse current, J_{sm}, can be obtained by assuming the voltage, V_g, in the above expression is zero. The current density formula becomes

$$J = \left[A^* T^2 \exp\left(\frac{-q\phi_b}{kT}\right)\right]\left[\exp\left(\frac{qV_g}{kT}\right) - 1\right] \tag{3.2}$$

This equation therefore represents the thermal excitation of electrons over a potential barrier. When a higher voltage is applied, the barrier is lowered by an effect called image-force lowering (see Appendix A). The reduction in barrier height is a small effect in thermionic emission since the applied fields are low. This effect becomes much more pronounced at high fields such as those needed for Fowler-Nordheim tunnelling and Schottky emission as shown in Figure 3.3.

3.3.3 Schottky emission

This emission is an extreme case of the mechanism described in the previous section. The interfacial barriers between the metal and insulator or semiconductor and insulator are lowered by the application of a suitable electric field. As shown in Figure 3.3. The applied voltage is high so that $\frac{qV}{kT} \gg 1$. The current density equation becomes

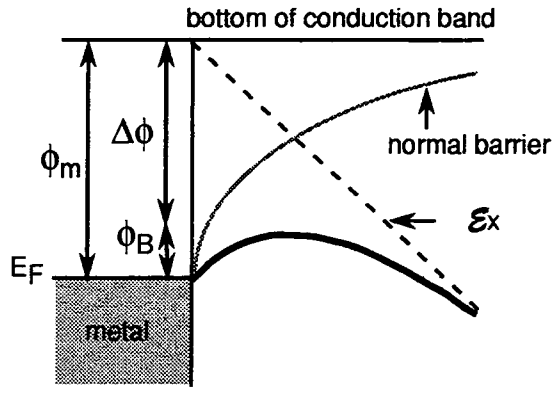

Figure 3.3 Schematic diagram showing image force lowering [8].

$$J = A^*T^2 \exp\left(\frac{-q\phi_b}{kT}\right) \exp\left(\frac{qV_g}{kT}\right) \exp\left(\frac{q\Delta\phi_b}{kT}\right) \tag{3.3}$$

where $\Delta\phi_b$ represents the barrier lowering. This is described in Appendix A. $\Delta\phi_b$ is given by

$$\Delta\phi_b = \sqrt{\frac{q\mathcal{E}}{4\pi\epsilon_{ox}}} \tag{3.4}$$

At zero field $J = J_s$ where

$$J_s = A^*T^2 \exp\left(\frac{-q\phi_b}{kT}\right) \exp\left(\frac{q\Delta\phi_b}{kT}\right) \tag{3.5}$$

By replacing $\Delta\phi_b$ by equation 3.4, the Richardson-Schottky equation is obtained.

$$J_s = A^*T^2 \exp\left(\frac{-q\phi_b}{kT}\right) \exp\left(\frac{\beta_s\mathcal{E}^{1/2}}{kT}\right) \tag{3.6}$$

where

$$\beta_s = \left(\frac{q^3}{4\pi\epsilon_{ox}}\right)^{1/2} \tag{3.7}$$

More accurately

$$J = J_s\left[\exp\left(\frac{qV_g}{kT}\right) - 1\right] \tag{3.8}$$

For a given voltage high fields are possible if the insulating layer is very thin. These high fields have a two-fold effect. First the thinner the oxide the greater the field and the smaller the barrier width, as shown in Figure 3.4. In addition, higher fields cause

a deeper lowering of the interfacial barrier as shown in Figure 3.5. Therefore, the application of an electric field reduces the barrier and enhances the number of electrons, with enough thermal energy, to pass from the negative electrode to the positive electrode. Schottky emission is a **contact** limited process. Schottky emission may be considered to be thermionic emission with image force lowering taken into account. Figure 3.4 demonstrates image force lowering for a typical metal-insulator system. Once electrons have accessed the insulator conduction band in an MIS system, they would be accelerated to the conduction band of the semiconductor.

3.3.4 The Poole-Frenkel effect

The Poole-Frenkel effect is similar to that of the Schottky effect but applies to the thermal excitation of trapped electrons into the conduction band of the semi-insulator. Since the traps lie within the bulk of the insulator this process is **bulk** limited. In the Poole-Frenkel case the barrier exists within the bulk of the insulator rather than at an interface as in Schottky emission. The barrier between the energy level of a trap and the conduction band of the insulator is lowered by an applied electric field as shown in Figure 3.6.

In analysing data, it is often difficult to distinguish between Schottky emission and Poole-Frenkel emission since the resulting current density expressions are very similar. One way to tell one from another is to decide whether the conduction is contact limited or bulk limited.

The image force for an electron at an interface is given by

$$F_{im} = -\frac{q^2}{16\pi\epsilon_0\epsilon_r(2x)^2} \tag{3.9}$$

(see Appendix A). In the Poole-Frenkel model, the image force of an electron in a Coulombic field involves a fixed distance of 'x' rather than '$2x$'. This is because the positive image charge is fixed for Poole-Frenkel barriers but mobile for Schottky emission and so the above expression changes slightly and the resulting image force is

$$F_{im} = -\frac{q^2}{16\pi\epsilon_0\epsilon_r(x)^2} \tag{3.10}$$

The image force for a neutral contact lowers the potential barrier by $\Delta\phi$ where

$$\Delta\phi = 2\mathcal{E}x_m = 2\mathcal{E}\sqrt{\frac{q^3}{16\pi\epsilon_0\epsilon_r\mathcal{E}}} = \sqrt{\frac{q^3\mathcal{E}}{4\pi\epsilon_0\epsilon_r}} = \beta_s\mathcal{E}^{1/2} \tag{3.11}$$

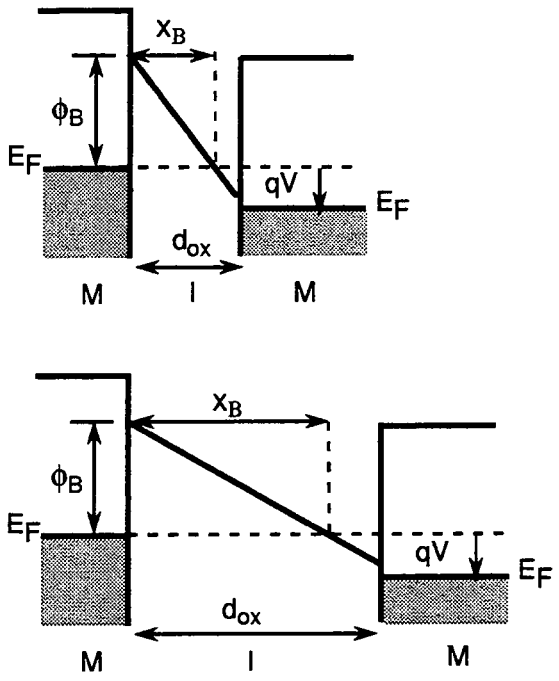

Figure 3.4 Schematic diagram showing the effect of oxide width on barrier width for a thin oxide and for a thick oxide, under the same applied voltage.

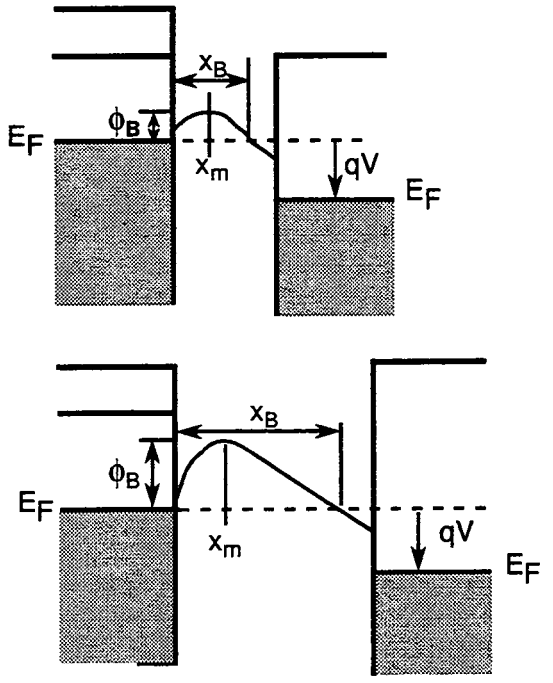

Figure 3.5 Schematic diagram showing image force lowering demonstrated for a thin oxide and a thick oxide, under the same applied voltage.

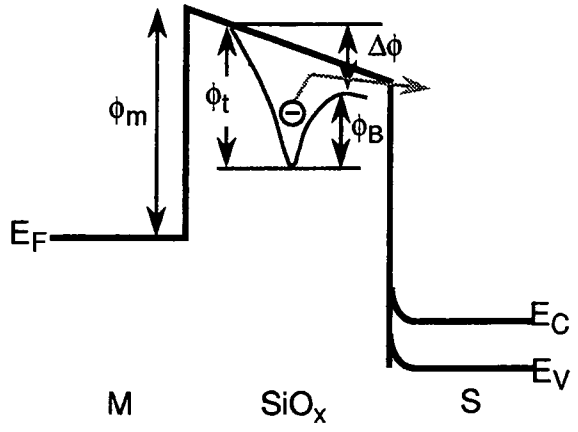

Figure 3.6 Schematic diagram showing image force lowering of the barrier between an electron trap and the conduction band of the insulator.

For a **donor** centre or trap, the electric field interacts to lower the potential barrier by

$$\Delta\phi = 2\mathcal{E}x_m = 2\mathcal{E}\sqrt{\frac{q^3}{4\pi\epsilon_0\epsilon_r\mathcal{E}}} = \sqrt{\frac{q^3\mathcal{E}}{\pi\epsilon_0\epsilon_r}} = \beta_{PF}\mathcal{E}^{1/2} \tag{3.12}$$

In obtaining the above expressions it is assumed that the field is constant throughout the insulator and that the space charge is not large enough to perturb the local field. From the above expressions it can be seen that $\beta_{PF} = 2\beta_s$. The reduction due to the Poole-Frenkel effect is *twice* that due to the Schottky effect.

The barrier lowering in the direction of the electric field is shown in Figure 3.7. The figure also shows that the barrier is increased in the reverse direction. The field dependence of the barrier height makes the conduction field dependent. In the absence of an applied field, the number of electrons in the conduction band because of thermal ionisation from traps is proportional to

$$\exp\left(\frac{-\phi_b}{2kT}\right) \tag{3.13}$$

where ϕ_b is the barrier height between the metal Fermi level and the dielectric conduction band. When a field is applied the conductivity is proportional to

$$\exp\left(\frac{\phi - \Delta\phi}{2kT}\right) \tag{3.14}$$

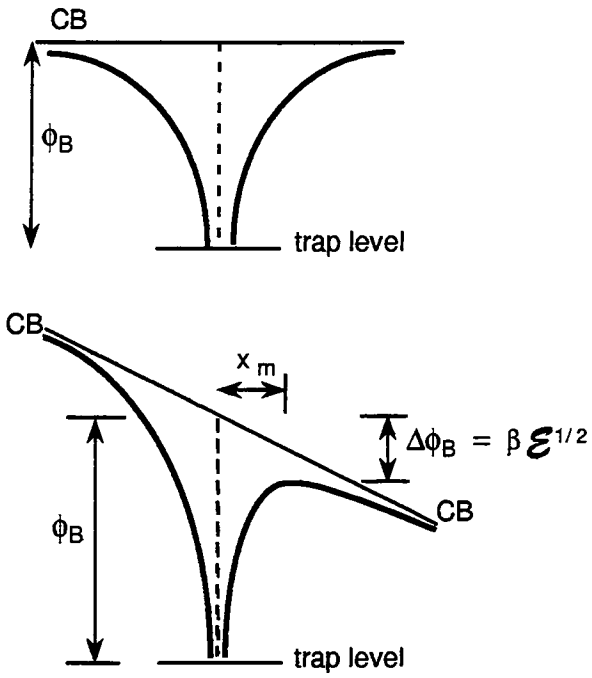

Figure 3.7 Schematic diagram showing the Poole-Frenkel effect. (a) shows the potential barrier, ϕ_b between a trap level and the insulator conduction band and (b) shows the image force lowering $\Delta\phi_b$ in the applied field direction.

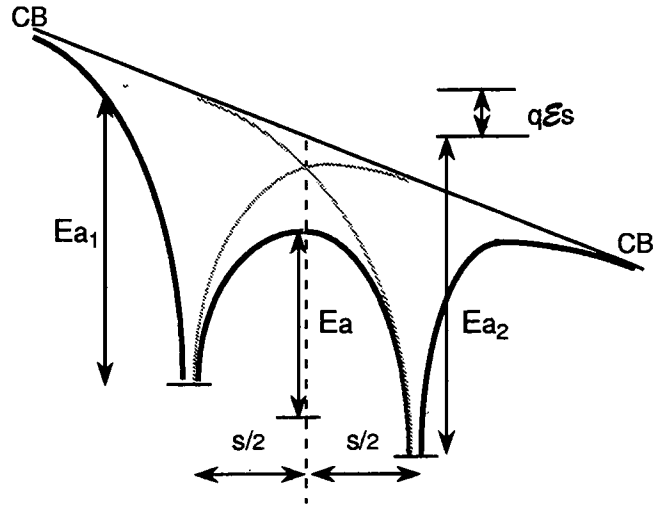

Figure 3.8 Interaction between two traps in the Poole-Frenkel mechanism [10].

Using the result of equation 3.12

$$\sigma(\mathcal{E}) = \sigma_{(0)} \exp\left(\frac{\Delta\phi}{2kT}\right) \tag{3.15}$$

$$\sigma(\mathcal{E}) = \sigma_{(0)} \exp\left(\frac{\beta_{PF}\mathcal{E}^{1/2}}{2kT}\right) \tag{3.16}$$

$$\text{where } \sigma_{(0)} = e\mu N_c \exp\left(\frac{-E_g}{2kT}\right) \tag{3.17}$$

$\sigma_{(0)}$ is called the low field conductivity and N_c is the density of states in the conduction band of the insulator. Instead of using conductivity the equation can be written as

$$J_{(\mathcal{E})} = J_{(0)} \exp\left(\frac{\beta_{PF}\mathcal{E}^{1/2}}{2kT}\right) \tag{3.18}$$

where $J_{(0)} = \sigma_{(0)}\mathcal{E}$. Although the effective barrier lowering is double for Poole-Frenkel compared to Schottky emission the $\mathcal{E}^{1/2}$ term in the exponential is the same for both mechanisms.

The amorphous nature of SiO_x causes the dielectric constant to vary throughout the material. Also the position and occupation of traps will be unknown so that the theoretical model will show only a rough guide for the level of J. If the Coulombic potentials from adjacent centres overlap, Schottky-Richardson and Fowler-Nordheim mechanisms could take place as well as Poole-Frenkel emission. Figure 3.8 shows two trapping centres which are closely spaced. The two sites produce an activation energy for tunnelling as shown in Figure 3.8. Effectively these two sites are combined to give a single doubly ionised site located at the mid-point between the two sites. Very close interaction, i.e. at around interatomic distances, would produce a band of energies around the trapping centres but this is unlikely to occur.

3.3.5 Extended state conduction in amorphous solids

As described in Chapter 2, electrons within the extended states are not free as they are in the conduction band of a crystalline solid. The mean free path is only of the order of an interatomic distance [2]. Therefore the mobility is a diffusion process. The Fermi level tends to be pinned at around mid gap.

3.3.6 Conduction in localised states

Localised states occur in the forbidden gap as described in Chapter 2. These provide an alternative path for electron conduction but the mobility is smaller than in the extended states. At low temperatures, and if the number of electrons activated to the conduction band is small, localised state conduction can become the predominant mechanism. At low fields thermally assisted tunnelling causes electrons to hop from one state to the other. At high fields Poole-Frenkel or Schottky emission takes place.

The 'basic' models outlined above have been used by experimentalists in the analysis of their I-V curves for SRO devices. Often these models are adapted or used as the basis for the development of new models for SRO conduction. The following section reviews the SRO conduction models which have been proposed to date.

3.4 Theories for conduction in silicon-rich oxide (SRO) films

3.4.1 Introduction

The science of SRO is an inexact discipline. The growth gas flow rates, temperature, pressure and post-deposition treatments have resulted in a material which is very varied in structure and composition. Despite this variation in properties SRO is recognised as an amorphous material which contains silicon crystals typically of the order of 1–5 nm.

The sharp band edges of crystalline solids change in more random materials varying from free carriers to immobile carriers caught in deep traps. Many workers agree that electronic conduction in SRO occurs by a 'hopping' movement from silicon crystallite to crystallite. However, different models have been used to describe the precise process involved in this hopping motion. These include direct tunnelling, thermally assisted tunnelling, Fowler-Nordheim tunnelling, a symmetrical Schottky barrier mechanism, Poole-Frenkel conduction and percolation theory. Some theories suggest that the hopping sites are randomly arranged both in space and energy level. If this is so then the activation energy required by an electron to move from one site to another is a continuous quantity. Others suggest that the conduction is by localised sites at or near the middle of the forbidden gap. The activation energy would be more discrete, close to $(E_g/2)$. Numerical data may therefore be difficult to relate to some

models if structural parameters are included in the analysis. Jonscher [14] suggests that film resistance, and therefore current flow, are often insensitive to the precise composition of a film and are mainly determined by the type of disorder present.

The following section reviews how some of the conduction models have been applied to experimental current-voltage, I-V, curves to explain the conduction in SRO devices.

3.4.2 The models

Abeles

Abeles [15] modelled carrier transport in cermets, which are particles of a metal embedded in insulators, such as SiO_2. The conductivity was assumed to be controlled by direct tunnelling from metal grain to metal grain. The high field region was defined by $\mathcal{E} \gg \frac{kT}{qw}$, where w was the diameter of the metal particle plus the depth of the oxide to the next particle. Fowler-Nordheim tunnelling was found to predominate at high fields. The low field region was governed by the relation

$$J \propto \exp\left(-2\sqrt{\frac{c}{kT}}\right) \tag{3.19}$$

where c was a constant. These ideas were used and extended by DiMaria *et al* [16] to describe conduction in SRO.

DiMaria

DiMaria et al [16] proposed that small silicon islands $< 50\mathring{A}$ in cross-section were distributed throughout their SRO film. Closely spaced islands were thought to interact to produce discrete energy levels within the forbidden gap. In addition, lattice mismatches between the SiO_x matrix and silicon crystals further modified the allowed energy levels. Expressions were derived for the average electric field within the SiO_x lying between silicon crystallites [17].

$$\mathcal{E} = \frac{V_g - \phi_{ms} - \Psi_s}{d_{ox}} \tag{3.20}$$

where V_g is the applied voltage, ϕ_{ms} is the difference in the metal-semiconductor work function and Ψ_s is the silicon surface potential. Experiments revealed two current

regimes and these were given by the formula

$$J = a\ f(\mathcal{E}) \exp\left(\frac{-b}{\mathcal{E}}\right) \tag{3.21}$$

a and b are constants. $f(\mathcal{E}) = \mathcal{E}^n$, $n = 1$ if direct tunnelling from silicon island to island occurs, $n = 2$ if Fowler-Nordheim tunnelling occurs from the bottom of the conduction band of the silicon island to the bottom of the conduction band in the SiO_x.

In a later paper [18] the WKB approximation was used to obtain a more detailed tunnelling mechanism formula. The barrier to electron flow was assumed to be rectangular with voltage, V, dropped across it. The new expression was used successfully to interpret their experimental results and was given by

$$J \propto \exp\left(\left[\frac{-4(2m^*)^{1/2}}{3\hbar q\mathcal{E}}\right]\phi_{eff}^{3/2}\right) \tag{3.22}$$

where the effective barrier height was given by

$$\phi_{eff} \approx \left[\phi^{3/2} - (\phi - qV)^{3/2}\right]^{2/3} \tag{3.23}$$

By comparing this relation for J with that of Poole-Frenkel

$$J \propto \exp\left(\frac{-\phi}{kT}\right) \tag{3.24}$$

It can be seen that for tunnelling to dominate over thermally activated conduction

$$\frac{\phi}{kT} \gg \frac{4(2m^*)^{1/2}\phi_{eff}^{3/2}}{3\hbar\mathcal{E}} \tag{3.25}$$

Ron & DiMaria

A further model was developed which accounted for silicon island size variations [19]. As shown in Figure 3.9, the islands were treated as spherical potential wells with sharp boundaries. These wells were assumed to be widely spaced so that the electrons occupied discrete energy levels. Each well caused a local conduction and valence band. The wells were randomly arranged throughout the SRO and had a range of energy

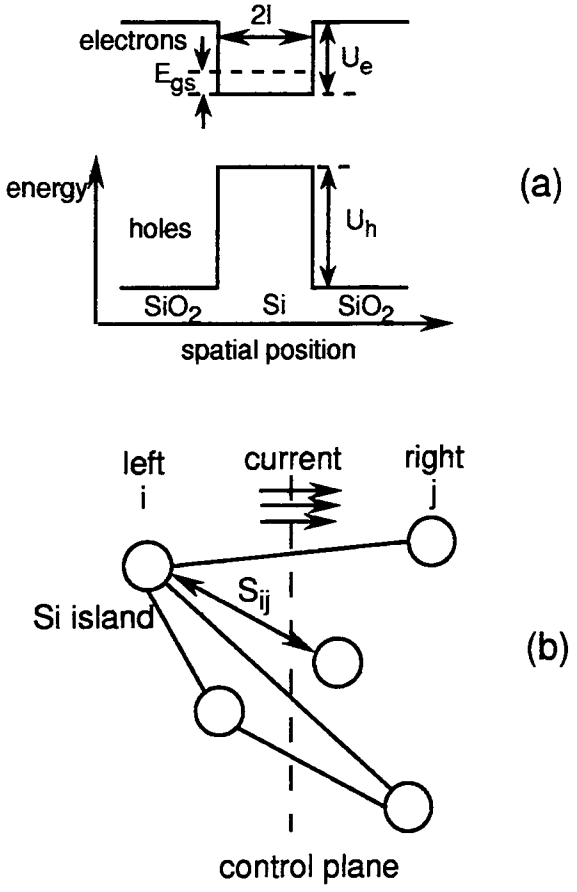

Figure 3.9 (a) Schematic diagram of a potential well associated with a silicon island within an SiO_x matrix (b) Schematic representations of the silicon islands and possible currents [19].

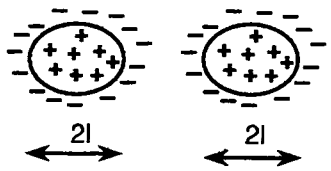

Figure 3.10 Grain structure postulated by Tarng in the symmetrical Schottky barrier (SSB) model [21].

levels. Tunnelling between wells occurred when a suitably high field was applied. The resulting mechanism was therefore governed by percolation. In summary

$$I \propto \exp\left(\frac{K}{\mathcal{E}_{av}}\right) \tag{3.26}$$

where $\mathcal{E}_{av}$ was the average applied field and K is a constant. The more detailed equation, derived in this paper [19], is of limited use to the experimentalist because it contains too many unknowns. In general, this model predicted Fowler-Nordheim tunnelling at high fields.

Tarng's model

This model was developed from the work of Petritz [20]. It is called the symmetrical Schottky barrier(SSB) model. Typical Schottky barriers show a reverse saturation, Tarng's samples did not have this property but did follow a Schottky-type mechanism [21]. The SRO film was described as tiny silicon grains separated and surrounded by thin amorphous grain boundaries as shown in Figure 3.10 A high density of surface states was assumed in the grain boundaries of polycrystalline materials. At equilibrium the Fermi levels in the grain and grain boundary must align. This causes charge redistribution, space charge and band bending surrounding each grain. The built in electric field $\mathcal{E}_x$ was given by

$$\mathcal{E}_x = \frac{q(N_D - N_A)x}{\epsilon_{ox}} \tag{3.27}$$

where ϵ_{ox} was the dielectric constant and N_D and N_A were the donor and acceptor state densities, respectively. The band structure was a series of Schottky barriers lying back to back, as shown in Figure 3.11. The Richardson-Schottky equation was modified to

$$J \approx A^* T^2 \exp\left(\frac{qV}{2gkT}\right) - \exp\left(\frac{-qV}{2gkT} - 1\right) \tag{3.28}$$

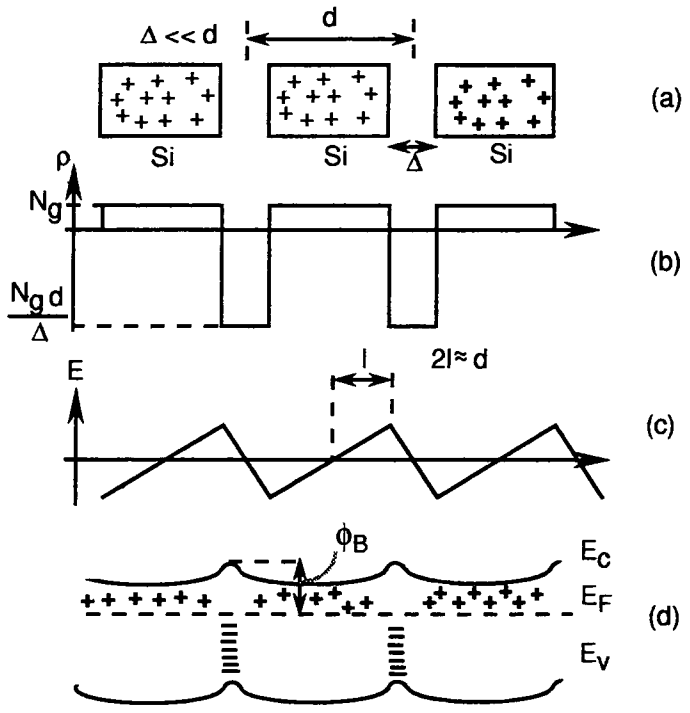

Figure 3.11 Schematic diagram of the SSB model showing a) physical structure, b) charge distribution, c) electric field and d) energy band structure [21].

or

$$J \approx J_s \sinh\left(\frac{qV}{2gkT}\right) \tag{3.29}$$

where

$$J_s = A^* T^2 \exp\left(\frac{-q\phi_b}{kT}\right) \tag{3.30}$$

ϕ_b is the barrier height for the MIS system, V is the voltage dropped across the oxide and g was the number of grains in series in the direction of current flow. Therefore an average electric field was assumed since $\frac{V}{2g}$ represents an average voltage drop across each grain. Tarng analysed his experimental results using this modified Schottky expression and the results yielded a high activation energy at high temperatures, a low activation energy at low temperatures and a variable value at intermediate temperatures. This analysis suggested that for his SRO carrier transport was dominated by thermionic emission at temperatures above 373 K and by tunnelling at lower temperatures.

Bolt & Simmons

Bolt and Simmons [22] modified Tarng's model slightly to account for the difference in top contact metals used. The new expression developed was

$$J = J_s \exp\left(\frac{qV}{2gkT}\right) - \exp\left[\frac{-q(V - 2gV_o)}{2gkT}\right] \tag{3.31}$$

where $2gV_o$ was the barrier height difference between the two electrodes.

A good agreement was found between the theoretical and experimental curves in both forward and reverse bias. The average barrier height was found to be 0.56 eV for SRO with 10.5 atomic % oxygen. Values for the Richardson's constant were found to be 110 and 30 $\mathrm{A\,cm^{-2}\,K^{-2}}$, for electrons and holes respectively. The value of A^* varies with temperature and applied field but this is in reasonably good agreement with theoretical values. 0.56 eV is approximately half the forbidden energy gap in silicon.

Zommer

Zommer simplified the expression used at a 5% cost in accuracy [23]. For voltages such that $qV/2gkT \geq 1.5$, the following expression was derived

$$J = A^*T^2 \exp\left[\frac{-(2g\phi_b - qV)}{2gkT}\right] \tag{3.32}$$

and for low voltages where $qV/2gkT \ll 1$

$$J = J_s \frac{qV}{2gkT} \tag{3.33}$$

Theory and experimental results were reconciled by using g as a 'fit' parameter rather than a structural parameter.

Black

A layer of SRO 500 nm thick made up the I layer in MIS devices. TEM photography revealed a large number of silicon dendrites at the SRO-Si interface [24]. Like Tarng's results, Black's current as a function of $\mathcal{E}^{1/2}$ plots revealed two separate conductivity regimes. This worker concluded that there was a transition between a field emission regime, mediated by the silicon dendrites and a bulk conduction regime similar to that of the SSB model.

Hamasaki *et al*

Hamasaki *et al* [25] obtained a similar J-T behaviour to that observed by Tarng in their transverse conduction measurements. However, they used an amorphous band structure to explain their results. The high activation energy regime was due to conduction in the extended states, as described earlier at high temperatures and the low activation energy was due to a hopping mechanism through localised states at low temperatures. Electron and hole activation energies were found to be the same and therefore the Fermi level was situated in mid-gap.

$$\sigma = \sigma_0 \exp\left(\frac{-E_0}{kT}\right) + \sigma_1 \exp\left(\frac{-E_1}{kT}\right) \tag{3.34}$$

σ_0 and E_0 are the conductivity and activation energies above room temperature and σ_1 and E_1 are the same quantities below room temperature.

England & Simmons

Using a Plasma-Enhanced Low-Pressure Chemical Vapour Deposited (PECVD) SRO, England and Simmons [26] found that, like Hamasaki *et al*, the conductivity revealed two activation energies. At high temperatures the current density was governed by

$$J_0 = \left(\sigma_{0(0)} - aV\right) \frac{V}{d_{ox}} \exp\left(\frac{E_{A0(0)} - bV}{kT}\right) \tag{3.35}$$

and at low temperatures by

$$J_1 = \left(\sigma_{1(0)} - cV\right) \frac{V}{d_{ox}} \exp\left(\frac{-E_{A1(0)} - dV}{T^{1/4}}\right) \tag{3.36}$$

where $\sigma_{0(0)}$ and $E_{A0(0)}$ are the conductivity and activation energy extrapolated to $V = 0$. $\sigma_{1(0)}$ and $E_{A1(0)}$ are similar quantities for the higher temperature and a, b, c and d are constants. Simmons used Hamasaki's model rather than Tarng's SSB model to describe conduction in these SRO films.

Ni & Arnold

Each silicon grain within the SRO layer was proposed to be surrounded by a thin silicon dioxide layer. Conduction was by tunnelling of the thermally generated carriers [27]. Electrons within the silicon islands tunnelled through the oxide barriers separating adjacent grains. Hole tunnelling was less likely since the valence band

separation between the silicon and SRO is more than the 3 eV separation between the conduction bands. (The value of 3 eV is only an estimate since this is actually the gap between the conduction bands of silicon and silicon dioxide.)

The average electric field throughout the SRO was given as

$$\left(\frac{V_{ox}+V_g}{l_{ox}+2l}\right) \tag{3.37}$$

and the conductivity by

$$\sigma = \frac{J}{\mathcal{E}} = 4\pi q^2 h^{-3} mkT \left(\frac{V_{ox}+V_g}{l_{ox}+2l}\right) \exp\left(\frac{-E_g}{2kT}\right) \exp\left(-2l_{ox}\left[\frac{8\pi^2 m\phi}{h^2}\right]^{1/2}\right) \tag{3.38}$$

where V_{ox} is the potential dropped across the oxide between the grains V_g is the voltage across the grain, l_{ox} is the oxide thickness separating the grains, $2l$ is the grain diameter and ϕ is the silicon to SRO barrier height. Ni and Arnold [27] found that like Bolt and Simmons [22] the activation energy was roughly half that of the silicon band gap. However the pre-exponent factor was calculated to be four times too large. At lower temperatures the activation energy of their samples decreased which suggested the presence of a competing mechanism.

Bruesch *et al*

Tarng's SSB model was criticised by Bruesch [28] because it contains a numerical error. For nanocrystalline substances the theory does not hold. Tarng's model depends on the relation

$$N_D - N_A \propto \frac{1}{L^2} \tag{3.39}$$

As the crystal size decreases to nanometres the doping level increases beyond acceptable levels. Bruesch used Ni and Arnold's model [27] which gave good agreement between theoretical and experimental conductivities for various oxygen concentrations and therefore silicon crystallite sizes.

The shell model of Ni and Arnold [27] was also used successfully by Lombardo *et al* [29]. Carrier transport was found to be controlled by thermionic field emission over the temperature range 80–400 K. Again, an activation energy of around the value for the mid-gap of silicon was obtained, i.e. 0.53 eV.

This value of activation energy occurs frequently and suggests that Fermi level pinning is taking place at the silicon grain boundaries.

Ozguz *et al*

SRO films of various oxygen concentrations were deposited on SiO_2. The films were doped with As, B or P and were annealed. A linear characteristic was obtained which indicated ohmic conduction [30]. Ni and Arnold [27] suggest that, for a particular oxygen concentration, the larger the grain size the thicker the oxide barrier between grains and the higher the resistivity of the films. Annealing increased grain size. Therefore annealed films were expected to show increased resistivity. In fact, Ozguz *et al* found that the conductivity increased with annealing. Bulk properties of the grains were thought to be unimportant whereas the grain-oxide interfaces were all-important in controlling the conductivity. The dopants used altered the conductivity by affecting the charge redistribution mechanisms and so changed the oxygen and dopant concentrations at the grain boundaries. It was difficult to state the precise mechanism involved but it was either by tunnelling or by a hopping conduction via impurity levels.

3.5 Conclusions

Amorphous materials, such as SRO, do not behave in the same way as crystalline substances under the influence of electric fields. The basic models were developed to describe conduction in crystalline insulators with a well-defined band structure. It is assumed that silicon rich oxide, whether it be amorphous, polycrystalline or a mixture of the two forms, has a band structure. The energy bands are caused by the splitting of discrete energy levels of electrons as atoms approach one another. It is therefore the chemical bonding between atoms which determines the energy band structure irrespective of whether the atom spacing is periodic or variable. Short range, rather than long range order, is important [3]. Therefore, it is assumed that amorphous materials possess a band structure in a similar manner as that found in crystals. This approximation means that when some of the conduction mechanism theories are applied to amorphous films, a rigorous agreement between experimental and theoretical results cannot be expected.

Analysis of experimental results is made more difficult when interface states are present, as described in Chapter 2. These states introduce energy levels within the forbidden gap and are sources of charge, which can strongly influence any conduction mechanism. Traps may disguise the field dependency of the current by introducing a temperature dependency. Current density formulae are of limited use if the current

is not constant over the entire device area. All models assume that the field strength is uniform throughout the film. This does not allow for any build up of space charge or structural non-uniformities. Many of these assumptions are necessary to simplify the mathematics required to synthesise the conduction models.

Some workers have gone to great lengths to account for the presence of traps, space charges etc. However, many of the 'improved' models are of little help to the experimentalist because these effects vary with method of production. The main features of the current-voltage characteristic should be recognisable and it should therefore be possible to interpret these characteristics using the models described in this Chapter.

Extended band tails and the presence of localised states within the band gap play an important role in semi-insulator current flow. Conduction is likely to be by a hopping of carriers from one localised state to the next, rather than by the acceleration of free electrons in the conduction band. The size of the silicon grains, intervening oxide width and most importantly the structure of the grain boundaries dominate conduction. Measurements of activation energies suggest that: (i) there are interface states at the grain boundaries which pin the Fermi level to mid-gap; and (ii) there are at least two competing conduction mechanisms.

Although the deposition parameters are critical in determining the nature of the SRO films some teams have found common agreement between experiment and a particular model.

Selection of the most suitable models will be aided by knowledge about the structure and composition of the SRO films grown here. Such characteristics are investigated and reported in Chapter 5. The theories in this Chapter will be applied to the measured I-V curves in Chapter 6. The following Chapter describes the equipment, processes and techniques used in the manufacture and characterisation of the MIS devices, used to investigate the properties of the SRO film.

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Chapter 4

Experimental Details

4.1 Introduction

This Chapter describes the equipment used in the fabrication and electrical characterisation of MIS devices, which contain SRO as the I layer. The equipment used in the physical characterisation of SRO films deposited on silicon substrates is also described. Specific details of the methods employed and the processes involved are given in detail to assist future workers in this field.

4.2 Fabrication of MIS devices

4.2.1 Introduction

The devices were fabricated at Durham University in the microelectronics laboratory, a class 1000 clean room. All of the SRO films were deposited in an atmospheric pressure chemical vapour deposition (APCVD) reactor. The fabrication steps are outlined below and can be obtained in more detail from Appendix B.

A meticulously clean and controlled procedure was adopted. All chemicals used were ultra pure and all PTFEware was dedicated to a particular set of chemicals.

4.2.2 Silicon substrates

N- and p-type wafers were used. The n-type wafers were 2 inches in diameter and were orientated in the <100> direction. A resistivity of $6-13\,\Omega\,\mathrm{cm}$ was quoted by the manufacturer, corresponding to a doping level of approximately $10^{15}-10^{16}\,\mathrm{cm}^{-3}$ [1].

Each wafer was scribed into 4 quarters for economy before being cleaned. The p-type wafers were one inch in diameter and were orientated in the <111> direction. The resistivity was $1.8 - 2.2\,\Omega\,\mathrm{cm}$, corresponding to a doping level of approximately $10^{15}\,\mathrm{cm}^{-3}$ [1].

4.2.3 Cleaning procedure

Each wafer was cleaned in exactly the same way, with the time for each stage of the process precisely monitored. Surface contamination was removed by boiling twice in 1,1,1 trichloroethane. The slice was then rinsed in propan-2-ol and then in deionised water. A 'bomb', that is a mixture of 1:1 H_2SO_4 : H_2O_2, was freshly prepared for each slice and the silicon wafers were boiled in this strong oxidising agent. The resulting oxide layer was removed by dipping the slice in 10% hydrofluoric acid. The slice was then rinsed thoroughly in ultrapure water and left in recirculating deionised water for at least 1 hour.

4.2.4 The field oxide

The field oxide was very important and had to be at least $1\,\mu\mathrm{m}$ in thickness if a good insulating layer was to result. Several cleaned quarter wafers, straight from the recirculator, were placed in the mouth of a dedicated field oxide furnace (through which nitrogen was constantly flowing) and left to dry for 10 minutes. Samples were then placed in the middle of the furnace and allowed to reach the oxidation temperature of 980 °C. The nitrogen was then turned off and the oxygen turned on. Oxygen entered the furnace having passed through ultrapure water at 87 °C; the process was therefore a wet-oxidation. Early experimentation yielded conductive films, part of this conductivity was found to be due to leaky field oxides. Oxide growth in the Durham furnace was found to be lower than had been previously expected and therefore the time of oxidation was increased. The rate of oxidation is linear at first but then decreases logarithmically with time [2]. Since the timing of this process was not critical, the furnace was left running for about 24 hours. At the end of the process, the oxygen was turned off and the nitrogen was turned on. After 10 minutes, the samples were moved to the mouth of the tube and left for 10 minutes before removal to the next stage in the processing. The field oxide was etched from the back of the wafer and device areas using hydrofluoric acid and standard photolithographic techniques using masks designed by the author. Sharply cut wells were formed in the field oxide

ready for the subsequent deposition of SRO to form the devices, (see Appendix B for more details). Before deposition of the SRO, the wafers were again dipped in 10% hydrofluoric acid, rinsed in deionised water and blown dry with nitrogen immediately prior to being loaded into the APCVD reactor.

4.2.5 Field oxide thickness

The thickness of the field oxide was measured before device processing with the Alpha step and ellipsometer. These techniques are described later in this Chapter. Agreement between the two methods was found to be within 5% and was typically 2%. The thickness did vary slightly across the wafer but only by approximately 1%. The thickness of the field oxides was 1874 ± 131 nm.

4.2.6 Field oxide resistivity

The resistivity of the field oxide was calculated to be of the order of $10^{12}\,\Omega$cm. This was lower than the theoretical value of $10^{14} - 10^{16}\,\Omega$cm. New, thicker field oxides were grown but the resistivity remained at $10^{12}\,\Omega$cm. The current through the field oxide was of the order of 10^{-12} A, which was small when compared with the lowest current through the smallest device at low voltages. This oxide current was therefore noted but was considered to be too small to affect the minimum of 10^{-7} A observed in the devices. The field oxide showed Ohmic behaviour in the voltage range from -30 V to $+30$ V. The typical device voltage ranges were much smaller, -3 V to $+3$ V.

4.2.7 Chemical deposition of SRO

The SRO films were deposited on the silicon substrates using nitrogen (N_2) as the carrier gas and with nitrous oxide (N_2O) and silane (SiH_4) as the reactant gases. The chemical reaction [3] is outlined below

$$SiH_4 + \gamma N_2O \longrightarrow pSiO_x + (1-p)SiH_4 + 2pH_2 + (\gamma - px)N_2O + pxN_2 \qquad \text{where } 0 < x < 2 \tag{4.1}$$

The SRO layer is thought to be made up of silicon oxides with silicon in crystalline and amorphous forms deposited throughout. The conductivity is determined by the amount of silicon present. This can be controlled by varying the gas phase reactant flow ratio, γ

$$\gamma = \frac{\text{flow rate of } N_2O}{\text{flow rate of } SiH_4} \tag{4.2}$$

Gas	Valve Setting	Mass Flow Controller setting	Gas flow rate
N_2O	3.9	513	$0.013 \pm 0.0005\ \mathrm{l\,min^{-1}}$
SiH_4	14	379	$0.06 \pm 0.002\ \mathrm{l\,min^{-1}}$ *

Table 4.1 Gas flow settings

It can be seen that the lower the value of γ, the higher the silicon content. The relationship between γ and silicon content is not linear and is dependent on the temperature of deposition [4]. For conductive films, γ must be less than 2 [4]. All samples were grown at a constant temperature of 650 °C using a constant composition, which was fixed by holding γ equal to 0.22. To achieve this ratio, the flow rates of the gases were maintained as in Table 4.1:

$$\gamma = \frac{[N_2O]}{[SiH_4]} = \frac{0.013}{0.06} \approx 0.22 \tag{4.3}$$

The carrier gas was fixed at 35 $\mathrm{l\,min^{-1}}$ of N_2. This composition was found to provide a good switching action in the MISS devices grown by previous workers [5, 6] and therefore this same composition was used to investigate the properties of the SRO films. The parameter, γ, is very dependent upon the particular system used for film growth and is not transferable between films grown using different systems. This work therefore concentrates on SRO produced in the APCVD reactor in Durham. The APCVD system is shown in Figure 4.1. The mass flow controllers and gas flow system are shown in Figure 4.2. Wafers were placed onto the carbon susceptor which has a large thermal mass, so aiding temperature stability during deposition. Tungsten halogen lamps heated the reactor chamber from below and the temperature was measured and controlled by detecting radiation from the susceptor. The chamber walls were relatively cool. This was an advantage, since this reduced wall deposits which could lead to particles falling onto the films. Accurate control of both temperature and flow dynamics was important. The latter has been improved by the installation of two mass-flow controllers which allowed more accurate control of the gas flow rates. The high flow rates of the carrier gas, nitrogen, may cool the wafers. An improvement might have been to heat the gases before they entered the chamber. The position on the susceptor also influenced the uniformity of the films, probably because the flow of gas was more turbulent towards the inlet and outlet. The wafers were therefore

*1.2 $\mathrm{l\,min^{-1}}$ of 5% silane in nitrogen is equivalent to a silane flow rate of 0.06 $\mathrm{l\,min^{-1}}$.

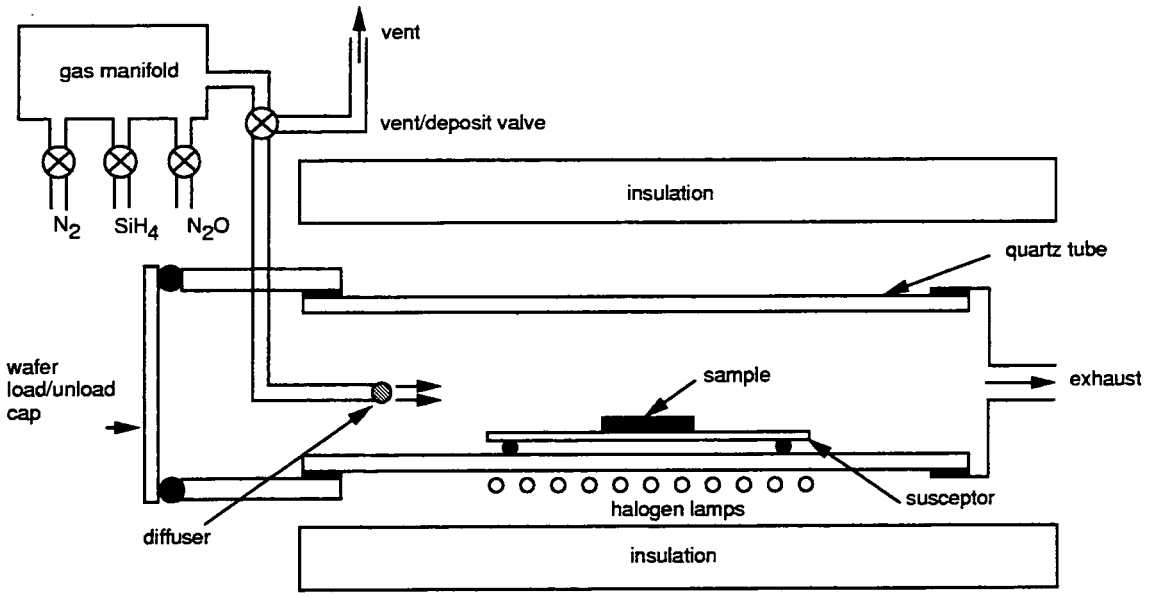

Figure 4.1 Simplified view of an APCVD reactor.

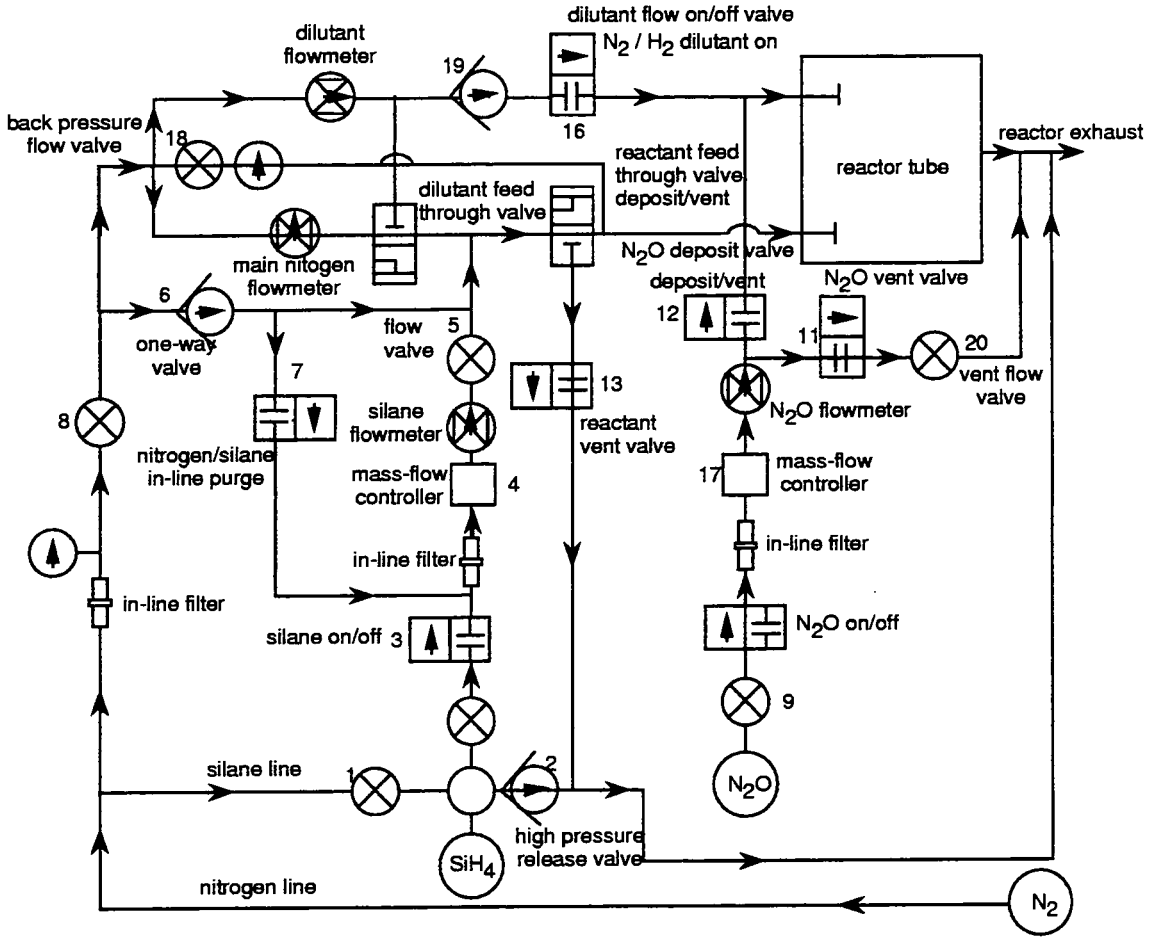

Figure 4.2 Durham APCVD gas flow system.

positioned in the centre of the susceptor and always in exactly the same position to aid device reproducibility. Even so, an average 5-6% [7] variation in thickness was observed across the film and as much as 12% was noted in some films. Whenever a device quarter wafer was placed in the APCVD reactor, a test quarter wafer was placed alongside it. This was part of the same wafer as the device wafer and was cleaned in exactly the same way. Structural analysis and thickness measurements were carried out on the test wafer. The time for deposition was varied from 0.5 to 8 minutes. More precise details of the deposition procedure are given in Appendix B. After film deposition, the device and test wafers were placed in labelled petri dishes under vacuum to await metallisation.

4.2.8 Annealing

To observe the effect of annealing, four quarter wafers were placed in the APCVD reactor and were processed simultaneously. A thickness variation was expected in the four wafers because of their different positions on the susceptor. However, the thickness variation was expected to introduce less error than by placing the four wafers in exactly the same susceptor position and performing several individual depositions. From the batch of four: one was used as the test piece for thickness measurements; one was used as-deposited; one was annealed in dry nitrogen at 1000 °C for two hours; and the remaining quarter was annealed under the same conditions for a period of four hours. After annealing, the wafers were treated in exactly the same way as the unannealed samples.

4.2.9 Metallisation

The top contacts were added to the wafer with a bonding pad to the side of the device area. Metal thickness was obtained from Alpha step measurements. Top contact materials included aluminium, chromium and molybdenum. The back of the sample was lapped and back contacts of gold added. The metallisation processes are described in more detail below.

Top contact preparation

For most devices, aluminium of a very high purity (99.999%) was evaporated onto the film using an electron-beam evaporator. Evaporation was performed at a pressure of 10^{-7} mbar and the aluminium was vapourised by focusing a high intensity electron

beam onto it. To avoid over-heating of the samples, the deposition was carried out in several stages with 6 seconds for evaporation and a 10 minute interval between each deposition. The electrode pattern was defined by standard photolithography and the unwanted aluminum removed by an aluminium etch consisting of 30:2:7 (by volume) orthophosphoric acid:nitric acid:water. This would normally take 1–2 minutes. Any photoresist remaining on the wafer was removed with acetone in an ultrasonic bath and then cleaned in propan-2-ol and dried with a nitrogen gun. Molybdenum was evaporated and etched under the same conditions as those used for aluminium. The chromium-gold evaporator was similar, but slightly inferior at a pressure of 10^{-5}-10^{-6} mbar. The gold was etched in iodine in potassium iodide and the chromium was etched with potassium ferricyanide. More details are given in Appendix B.

Alpha-step readings were taken of the thickness of the thickness of the top contacts from glass plates placed in the evaporators during metallisation. The results were as follows: aluminium, 116 ± 3 nm; molybdenum, 1119 ± 45 nm; chromium/gold, 1119 ± 45 nm in total. Ideally these metal layers should have been of the order of $1\,\mu$m for perfect gold wire bonding pads.

Lapping the back

During processing, the back of the slice may become covered with oxide. It was therefore necessary to clean the back of the sample immediately before deposition of the back contacts. A diamond paste and a drop of lapping fluid were ground over the entire area of the back of the wafer for approximately 10 minutes. The slice was then cleaned in acetone in the ultrasonic bath and in propan-2-ol. A drop of hydrofluoric acid was then painted onto the back surface of the slice to remove any oxide and this was then removed with deionised water. The sample was then immediately placed in the gold evaporator.

Back contact preparation

Gold was evaporated onto the substrate by means of thermal evaporation in a conventional diffusion and rotary pump evaporator. The aluminium sample holder acted as a mask with two 5 mm slots 5 mm apart. Gold of 99.99% purity was placed in the boat and the current through the heating element set at 30 A. Evaporation took place at a pressure of 10^{-5} mbar for 30 s. A curve tracer was applied to the two gold strips and the resistance between them determined. This needed to be less than $200\,\Omega$ and Ohmic in both forward and reverse bias if the back contacts were to be considered to

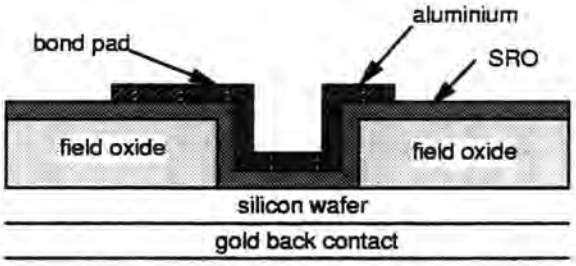

Figure 4.3 Cross-section through SRO devices.

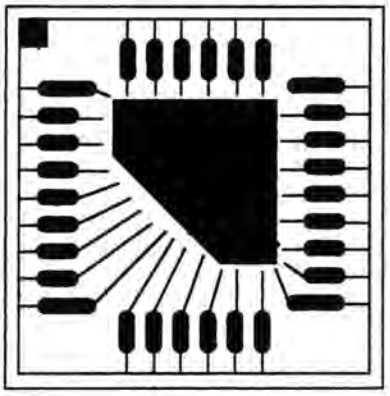

Figure 4.4 Printed circuit board design (actual size).

be good. Unacceptable contacts were cleaned off and the process repeated.

Gold with n-type silicon forms a Schottky barrier. The back contact, therefore, would have been susceptible to the non-symmetrical I-V characteristics observed in such barriers. In reverse bias, the silicon at the back contact was in depletion and therefore some of the applied voltage was dropped across this depletion layer. In forward bias the silicon at the back contact was accumulated and therefore acted as a metal with a negligible voltage drop. This non-uniformity in resistance of the back contact could be reduced by using gold doped with antimony. The antimony diffuses into the silicon forming an n^+ layer onto which the gold made contact. Although an $Au-Si\,n^+$ contact acted as a Schottky barrier, the surface depletion layer was so thin that it broke down due to tunnelling and near Ohmic conduction occurred. The final device structure was as shown in Figure 4.3.

4.2.10 Printed circuit board (PCB)

The PCBs were made to the design shown in Figure 4.4 and the copper pattern was gold-electroplated. The quarter wafers containing the devices were then held in position in the central area of the pcb by quick drying silver paint, made by Agar

Scientific Ltd. This electrodag acted as an adhesive and as a thermal and electrical conductor of negligible resistance. Gold wire bonds were used to connect the pads of the devices to the pads of the pcb.

4.2.11 Testing gold bonds

A destructive pull test was used on spare pads as a preliminary assessment of the initial bond strength on newly processed wafers. The second bond was always weaker than the first but the pull test was applied to both bonds. Even a poor bond was stronger than the wire. This is because each bond was 6–8 times the diameter of the wire, which tended to break in the recrystallisation zone above the ball. In addition to the pull-test, therefore, a shear test was applied. The blunted end of a pair of tweezers was pushed against the ball, at an angle of 20–25 degrees to and above the substrate. This test revealed weak bonds, caused, for example, by contamination, which could be rectified before the device pads were bonded. Further points to be considered by future workers are included in Appendix C.

4.3 The electrical measurement system

This section of the work is a detailed account of the equipment, the interconnections necessary, the settings required and software used to perform the electrical characterisation of the material under review.

Communication with printer, voltmeters and ammeter took place through the IEEE 488 interface bus. The data and commands were transmitted in parallel through eight data lines. The software package used enabled commands to be sent to assign each instrument to be a talker or a listener.

The source voltage was delivered from a Keithley 617 electrometer, which was also programmed to act as a voltmeter. A Keithley 485 picoammeter was used for current measurements and a Black Star multimeter for thermocouple/temperature measurements. The measurements of current, voltage etc were stored on floppy disks, from which data could be plotted using specially written software in Microsoft Excel. An overall block diagram of the system is shown in Figure 4.5.

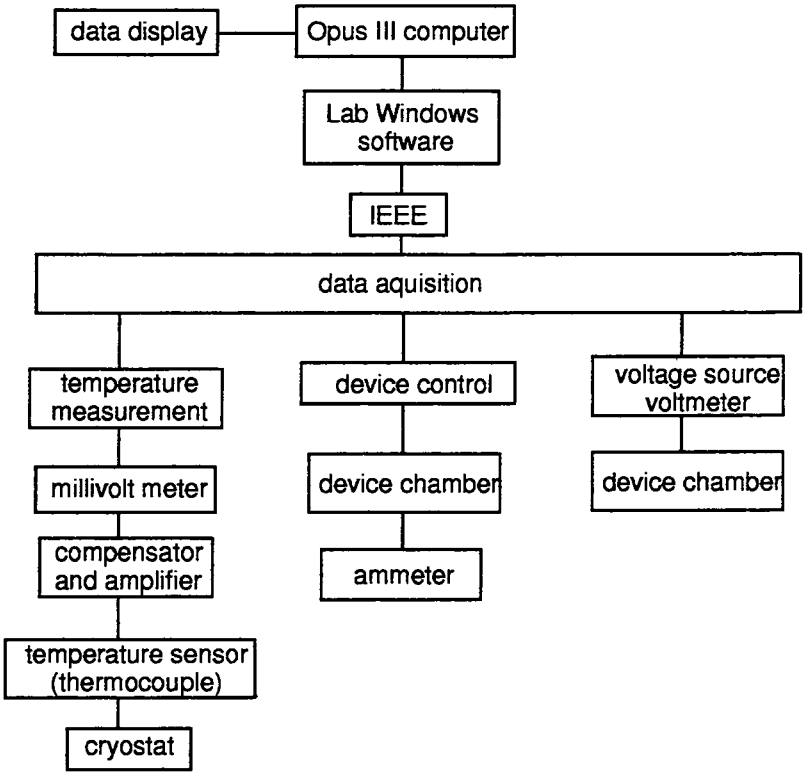

Figure 4.5 Simplified representation of data, control, collection and display.

4.3.1 Current-voltage measurements

The electrical connections to the devices were made initially through flying leads of gold wire. These were bonded to the aluminium top contact and were then wrapped around the gold probe which was connected to one side of the voltage supply. The other side of the supply was connected, via an ammeter, to a conducting vacuum chuck which held the sample firmly firmly and ensured good electrical contact between the back contacts and the chuck. A schematic diagram of the probe chamber used for the electrical characterisation measurements is shown in Figure 4.6.

The metal box was earthed to screen the sample from electromagnetic interference. Co-axial cables were made as short as possible to minimise leakage. The current was found to be sensitive to light incident upon the sample and therefore the screened metal box was made light-tight.

Preliminary measurements were made with this equipment. However, investigation showed that the electrical signals were often swamped by mechanical noise; also, only measurements at room temperature were possible. Various probing arrangements were investigated and subsequently abandoned in favour of a gold-wire-bonded

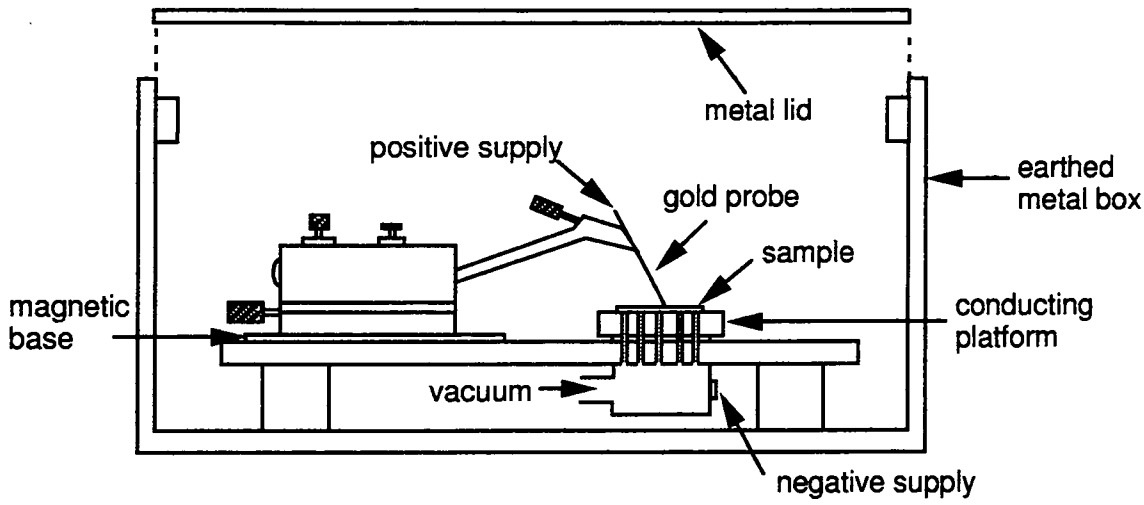

Figure 4.6 Diagram of a simple probe chamber.

system. This eliminated the problems associated with mechanical noise. A new earth-screened light-tight device chamber was then developed for use within a cryostat.

Within the new chamber, the electrical cables connect from the voltage source to the spring mounted contacts in the cryostat to a 25-way ribbon cable and 16-way multiplexer and then to a digital I/O board which enabled one of the 16 devices to be switched into circuit. The arrangement is shown in Figure 4.7. The voltage across the device was estimated as

$$V_{supply} - IR_{switch} - V_{ammeter} - IR_{back-contact} = V_{device} \tag{4.4}$$

These voltages were automatically subtracted in the software. Typically, the on-state switch resistance was $270\,\Omega$.

An Opus III micro computer was used to control the multiplexer switching, voltage source value, all instrument settings and data collection. The timing of the data collection was governed by time delays or by temperature intervals (recorded as thermocouple output voltages in millivolts), set in the software by the user.

4.4 Temperature measurements

Most of the current-voltage measurements were made over a range of temperatures, approximately $20\,°C$ to $-50\,°C$. Some measurements were made at temperatures as low as $-100\,°C$. The timing of the measurements was software controlled and a flexible system was designed so that a selected number of devices were individually

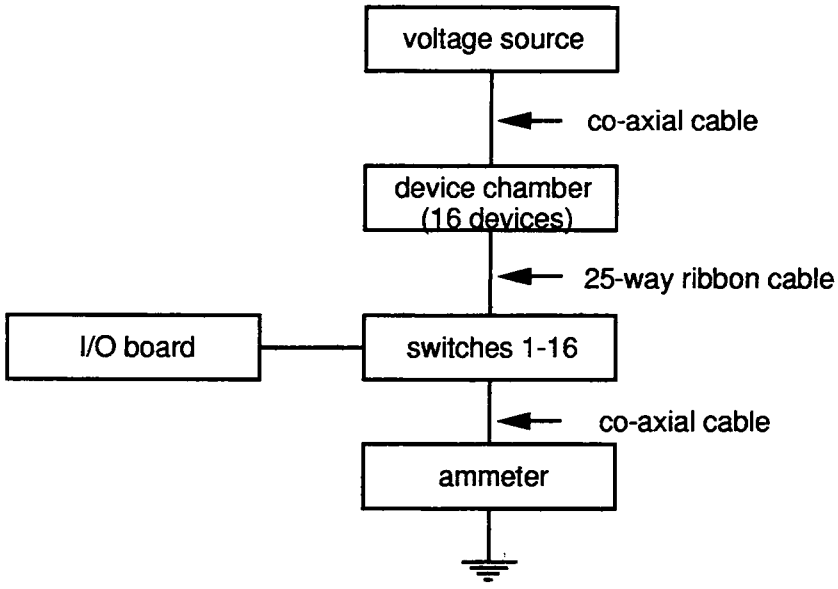

Figure 4.7 System overview for electrical connection to devices.

switched into circuit. The data were recorded once the temperature reached the value programmed by the user. A type T thermocouple was used to measure the temperature, T_1, of the device chamber. This copper and copper/nickel thermocouple was ingeniously spring mounted so that one junction rested immediately above the device surface. The other junction was at room temperature, T_2. The resulting thermocouple voltage, V_S, was proportional to the temperature difference between the two junctions, that is

$$V_S = \alpha(T_1 - T_2) \tag{4.5}$$

where α is the Seebeck coefficient. Usually the T_2 junction would be held at 0 °C in an ice-water slurry. This condition was electronically simulated by a cold junction compensator. A temperature dependent voltage was added to V_S such that the voltage sum was the same as if the T_2 junction was held at 0 °C. The compensator had special curvature correction circuitry which matched the non-linear response of the thermocouple to maintain compensation over a wide temperature range.

Type T thermocouples typically produce an output voltage of 40.6 μV per degree Celsius difference between the two junctions. This was amplified to a scaled output of 10 mV per degree Celsius by an amplifier which was matched to the cold junction compensator. These integrated circuits were purchased as a package (the LTK001) from RS Components.

The circuit operates with a $\pm$15 V supply and is as shown in Figure 4.8. The

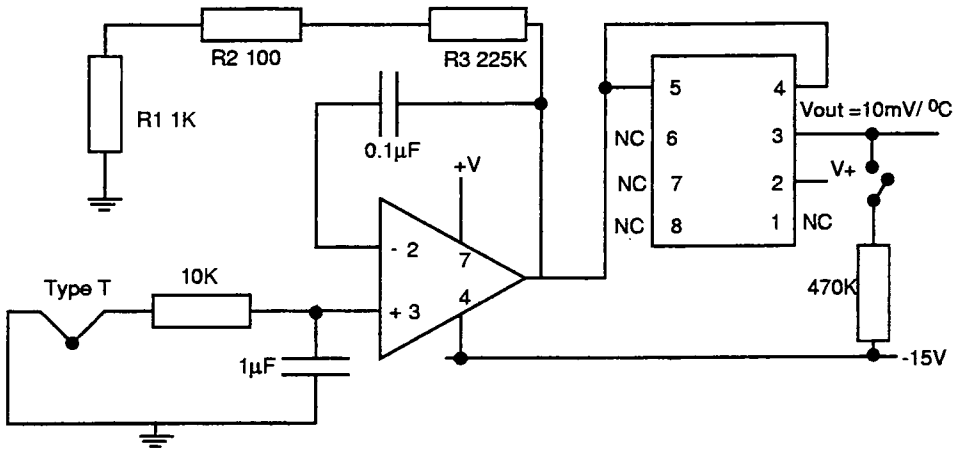

Figure 4.8 Amplifier circuitry for temperature compensation.

circuit output was checked by comparison with a mercury thermometer. A schematic diagram of the temperature measurement system is shown in Figure 4.9. The circuit output was fed to a millivoltmeter and the output from this was fed via an IEEE cable to the computer. Scaling from millivolts to degrees Celsius was then performed by the software. The software basically followed the sequence of instructions below:

(i) At temperature 1.

(ii) Select device 1.

(iii) Open file 1.

(iv) Take I, V, and T readings.

(v) Close file 1.

(vi) Repeat at temperature 2 to N.

(vii) Repeat for device 2 to 16.

The temperature accuracy was $\pm 1^{\circ}$ C.

4.4.1 The cryostat

The sample chamber was designed by the author and fabricated in the mechanical workshop in Durham. A schematic diagram is shown in Figure 4.10. The chamber consists of two parts:

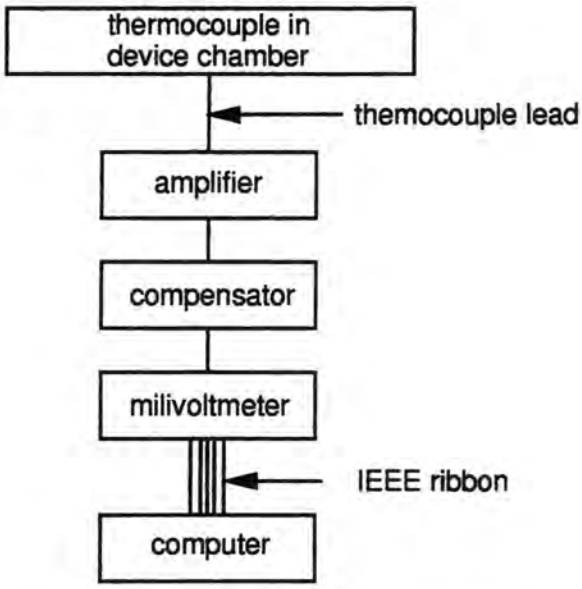

Figure 4.9 Block diagram of temperature measurement system.

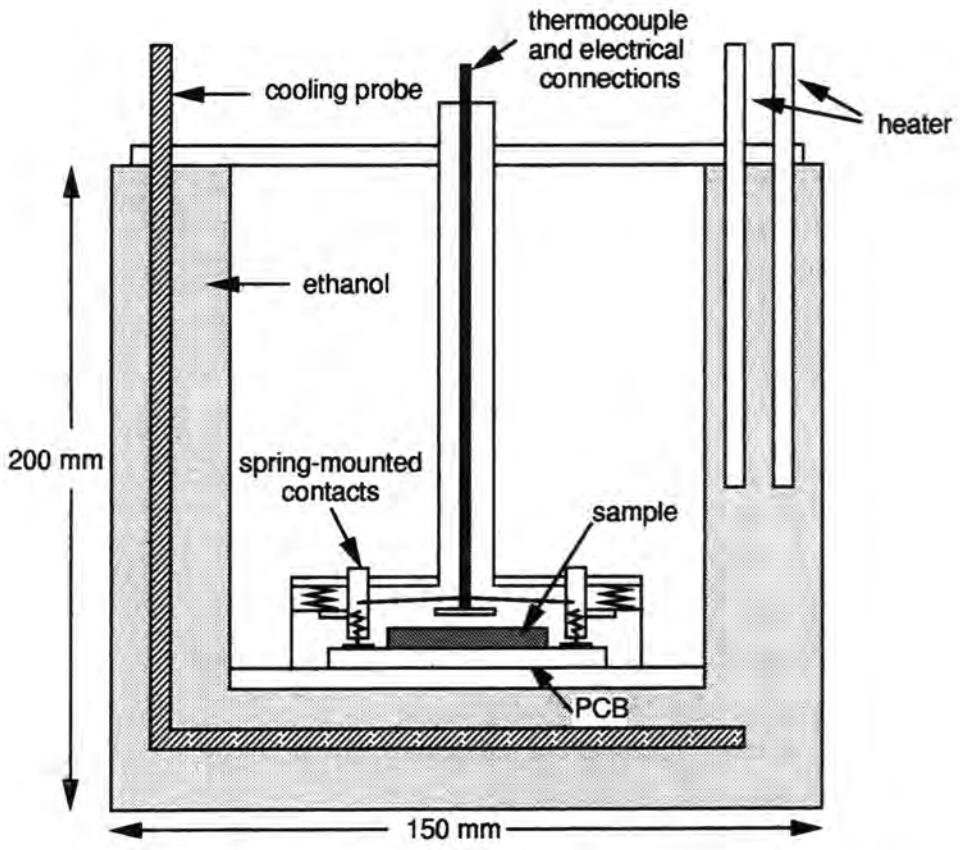

Figure 4.10 Diagram of cryostat and device chamber.

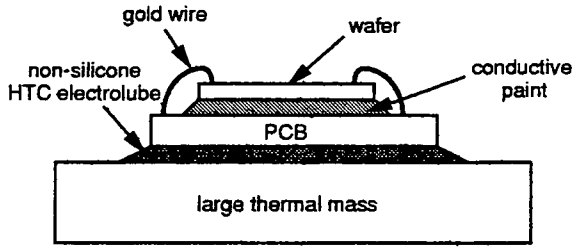

Figure 4.11 Pcb mounting arrangements within cryostat chamber.

(i) the inner chamber which was earthed to provide screening and was also light tight

(ii) the outer chamber (which surrounded the inner chamber) was an insulated bath containing the coolant.

The heat transfer fluid used was ethanol since its melting point is $-117°$ C and its boiling point is 78° C, thus providing a wider range than that required by the system. Ethanol has the advantage of not becoming exceedingly viscous at the lowest temperature of operation and importantly, of all the cooling fluids reviewed, ethanol offers minimal health hazards. Unfortunately, the cooling fluid collects water vapour from the air at low temperatures and so it must be replaced periodically. Some experiments were carried out using liquid nitrogen as the coolant. A wider temperature range was obtained but data could only be collected as the samples warmed to room temperature. The ethanol coolant enabled slower cooling of the device chamber and so allowed current-voltage measurements to be taken on cooling and warming. A coiled 450 mm, nickel-plated bronze cooling probe was wrapped around the inner chamber submerged in the ethanol. An insulated coaxial host assembly was used to carry refrigerant from the refrigeration compressors to the probe. The refrigeration unit used was a Neslab Cyrocool CC100 II immersion cooler.

The base of the inner chamber was made 1 cm thick to provide a high thermal mass and so prevent sudden temperature changes within the device area. Good thermal contact between the PCB, upon which the devices were mounted, and the base of the chamber was provided by a non-silicone heat transfer compound made by Electrolube. Silicone based compounds cause poor electrical conductivity and have therefore been avoided. The sample mounting is shown in Figure 4.11. Strong spring-mounted contacts held the pcb in place and also formed the electrical connections to the exterior of the chamber.

16-Channel Multiplexer
Control Lines

EN Line 4	A3 Line 3	A2 Line 2	A1 Line 1	A0 Line 0
MSB				LSB
PB4	PB3	PB2	PB1	PB0
Pin 23	Pin 25	Pin 27	Pin 29	Pin 31

Table 4.2 Control line assignments.

4.5 Data acquisition and display

The temperature at which electrical measurements were made, the delays between current and voltage readings, the voltage source value and the device selection for test were all governed by the software. A very powerful, flexible investigative tool has been developed for the control of data acquisition, data collection and display. This control was provided by a National Instruments software development system, for Quick Basic and C programmers, called Lab Windows.

4.5.1 Signal connections

At each of the required temperatures, a number of devices (1–16) were individually switched into circuit and the current-voltage-temperature measurements were made and the data stored in individual device files. The control signals required for device switching were software driven. This section describes the hardware needed to achieve co-ordination of the switching of the devices together with the instrumentation necessary for data acquisition, display and storage.

An input/output (I/O) interface board was purchased from National Instruments which was compatible with the National Instruments' Lab Windows instrumentation and control software package. This board, the PC-DIO-24 was a 24-bit parallel I/O interface for use with a personal computer. It has three I/O ports (PA, PB and PC) each with 8 bits. Port B (referred to as port 1 in the software) was configured as an output port. By writing to the five least significant of the eight bits which make up the port, each line was set to a logical HI or LO. These five lines were used to code the switching of the solid-state relays contained within the HI506 integrated circuit (IC) multiplexer chip.

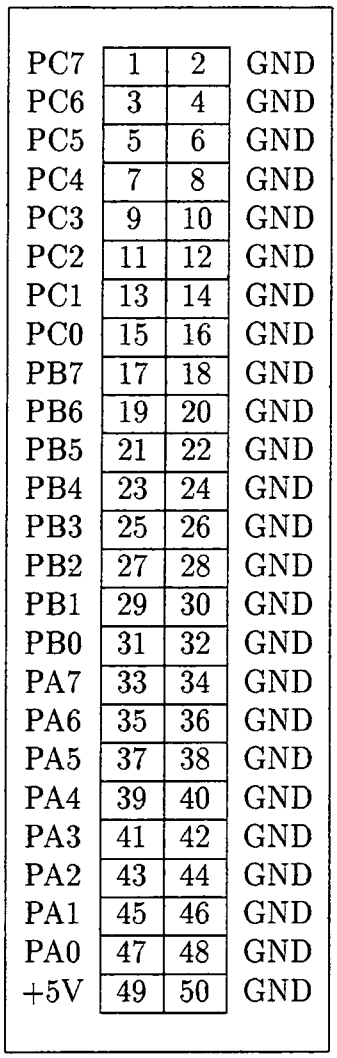

Figure 4.12 Digital I/O connector pin assignments.

Dec	Bit Pattern to I/O board					Switch made
0	0	x	x	x	x	None
16	1	0	0	0	0	1
17	1	0	0	0	1	2
18	1	0	0	1	0	3
19	1	0	0	1	1	4
20	1	0	1	0	0	5
21	1	0	1	0	1	6
22	1	0	1	1	0	7
23	1	0	1	1	1	8
24	1	1	0	0	0	9
25	1	1	0	0	1	10
26	1	1	0	1	0	11
27	1	1	0	1	1	12
28	1	1	1	0	0	13
29	1	1	1	0	1	14
30	1	1	1	1	0	15
31	1	1	1	1	1	16

Table 4.3 Bit pattern for selection of solid state relays in the multiplexer IC.

The ports interfaced with the relays via a 50-way male header and ribbon cable. The pin assignments of this cable are shown in Figure 4.13. Pin 49 of the header was used to input 5 V to a 5–20 V converter and this provided the 20 V supply needed by the HI506 multiplexer IC. The 5 lines needed to operate the multiplexer were connected to the pins labelled PBO to PB4. Pins PBO to PB4 made up the four control lines and an enable line which were used to switch in each channel as shown in Table 4.2. The 16 channel multiplexer interfaced with 16 devices. Any number of the 16 devices were switched into circuit by applying the appropriate code or bit pattern to these control lines as outlined in Table 4.3. Control circuitry for the multiplexer is shown in Figure 4.14. The multiplexer, its power supply unit, LED status indicators and drivers, the solid state relays and voltmeter and ammeter BNC connections were housed in a separate switch box shown diagrammatically below in Figure 4.15. A 25 ribbon connector links the solid state relays to the devices in the temperature controlled chamber.

The supply was applied to all the devices at once and the connection to ground through the ammeter was switched to each device in turn.

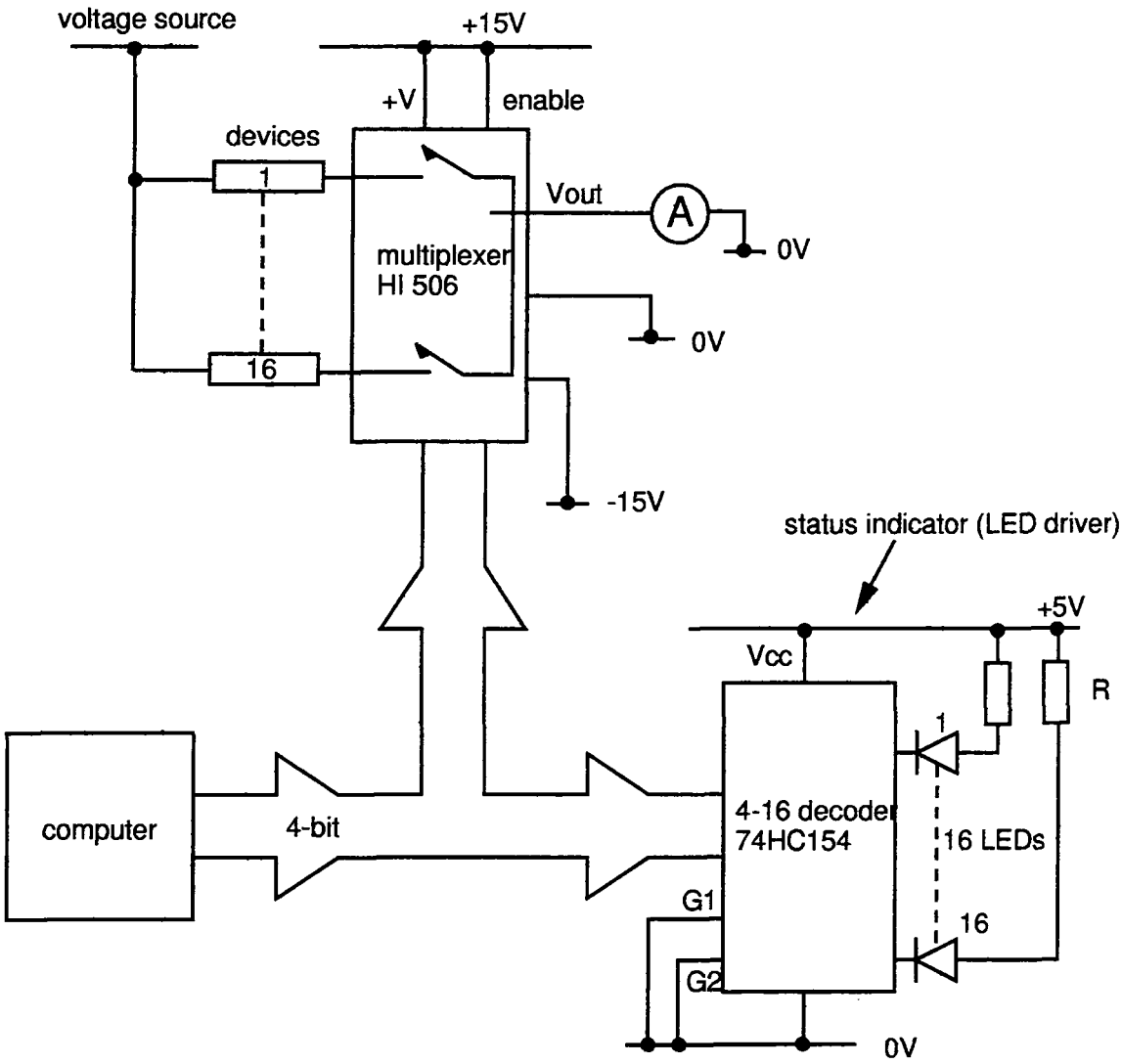

Figure 4.13 Multiplexer control and status indicator circuitry.

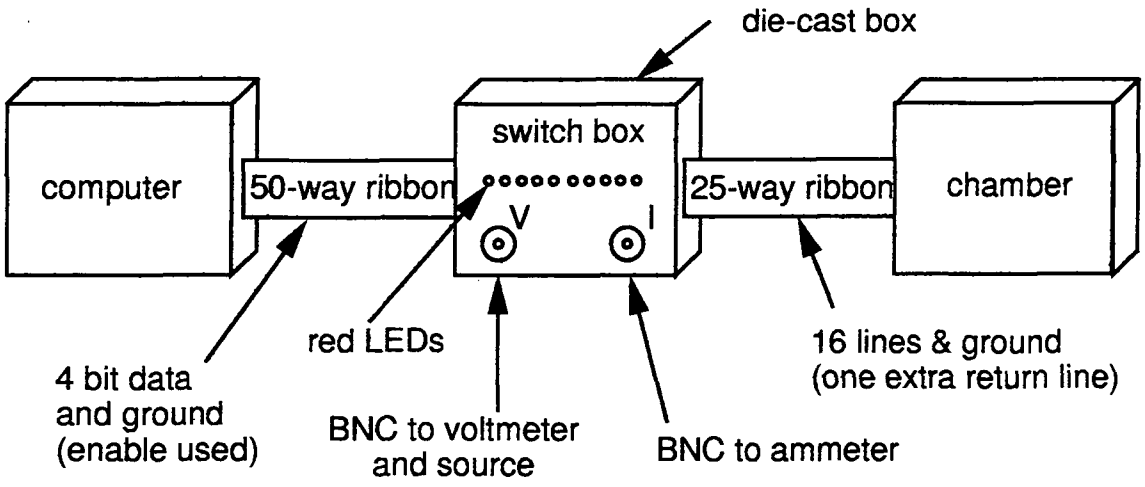

Figure 4.14 Physical arrangements for device selection.

4.6 Compositional analysis

4.6.1 Glow discharge optical emission spectroscopy

I am indebted to Mr. Dharmadasa of the Materials Research Institute of Sheffield Hallam University for allowing me access to this exciting new semiconductor technique. The equipment is described below. A LECO GDS-750 QDP glow discharge spectrometer was used for this study and the main features are shown in Figure 4.16.

The sample was held in position with an o-ring seal and forms the base of the plasma source and also acts as the cathode for the plasma source. A rotary vacuum pump evacuated the 4 mm diameter cylindrical chamber to approximately 1 Pa. The walls of this metal chamber act as the anode. A constant flow of argon gas towards the sample was maintained at a pressure of 100 Pa throughout the experiment. Water circulated around the glow discharge area and kept the temperature at approximately 30 °C. A stable voltage of around 693 V (power 18 W) was applied to the cathode and this combined with a controlled argon pressure across the sample surface produced a stable excitation source. Continuous removal of materials from the surface produced a very flat, uniform sputter area. This was aided by the fact that the etch products were continuously pumped away through a gap between the sample and the anode during plasma etching. Surface atoms removed by the sputtering process diffused into the plasma where excitation and emission occurs. The intensity of the emitted light from a particular element was directly proportional to its concentration in the plasma and therefore also to its concentration in the sample surface. Figure 4.17 shows the

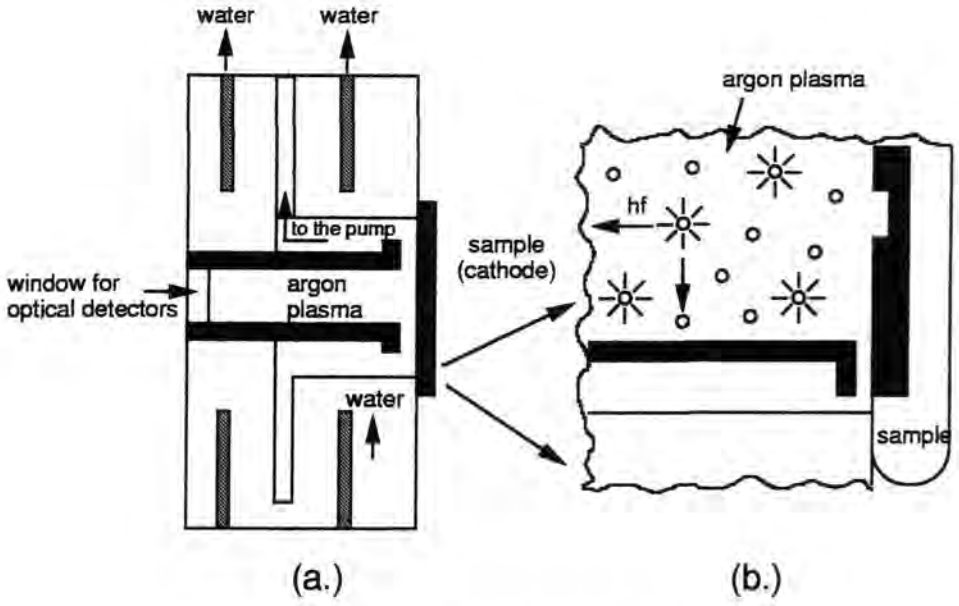

Figure 4.15 Plasma source for GDS.

lens, grating and photodetector arrangement used. The SRO film samples proved to be suitable samples for the Glow discharge optical emission spectroscopy (GDS) technique. The results of GDS analysis are described and discussed in Chapter 5.

4.6.2 Secondary ion mass spectroscopy

I am grateful to Dr. Mike Petty of Loughborough University for the Secondary ion mass spectroscopy (SIMS) and Auger electron spectroscopy (AES) work done in testing the SRO films. SIMS is a technique which uses sputtering to determine bulk composition analysis. Sputtering is the process whereby fragments (individual atoms or clusters of atoms) are ejected from a sample surface by energetic inert gas ions, for example, He^+, Ne^+, Ar^+. The sputtered fragments may be mass analysed to provide compositional information of the film under examination. A Cameca IMS 3f secondary ion mass spectroscope has been used in this work to provide depth profiling on a typical SRO sample. The reason why SIMS is particularly well-suited to depth profiling is that the profiling beam provides the SIMS signal. A distinct disadvantage of SIMS, however, is that it is a destructive technique.

The basic information of a SIMS experiment is the secondary ion mass spectrum of either the positive or negative ion fragments. The relationship of the ion yield to the total sputtering yield (ion and neutral atoms) is sensitive to the incident ion species, their energy and the method of measurement of the mass spectrum. The mass

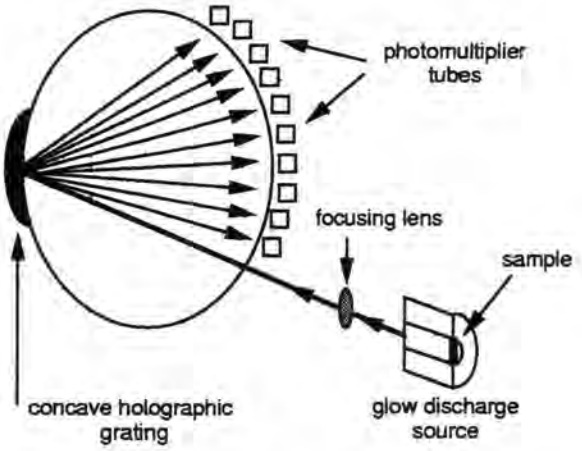

Figure 4.16 Optical detection system for GDS.

spectrometers used to analyse the ion spectrum are sensitive to the kinetic energies of the ions passing through them. For example, if a mass spectrometer is set to detect ions in the 0–5 eV energy range it will detect different yields of ions than when it is set to the 5–10 eV range. Preliminary investigations were required to set up the apparatus for each sample under test.

By far the most popular bombarding species is oxygen (O_2 partial pressure or O_2^+ ion bombardment). The oxygen atoms are thought to become embedded within the surface and subsequently to cause bonds to break, e.g. Si-O bonds which release Si^+ ions for mass spectroscopy. Oxygen is often used because it gives high sensitivities in SIMS studies of bulk composition, but of course, unlike some other bombarding species, this process severely disturbs the chemical state of the surface under examination.

The application of oxygen ions in the SIMS process revealed detail of the elemental composition of the SRO film deposited on test samples sent to Loughborough for analysis. The results are shown as plots of atomic percentage composition against film depth in Chapter 5.

4.6.3 Auger electron spectroscopy

Auger electron spectroscopy (AES) was used to identify the composition, distribution and bonding of the elements which make up the SRO film. The AES process is described below.

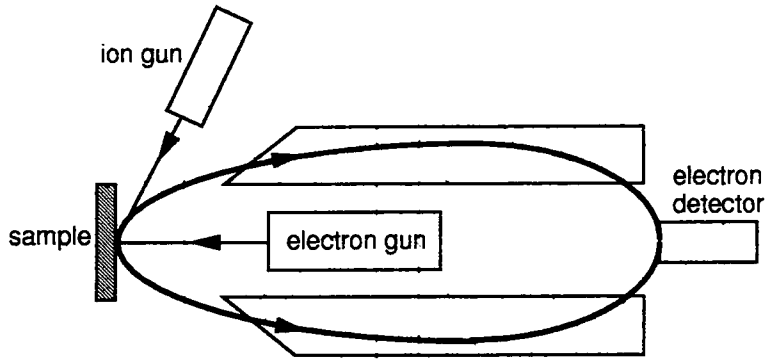

Figure 4.17 Block diagram for a typical AES system.

The process

A positively charged ion, within a solid, may lose some of its potential energy by accepting a low energy level electron and at the same time may emit energy. The emitted energy is often lost as a photon but in AES this energy is given to an outer shell electron as kinetic energy; this electron is subsequently emitted from the atom. Such electrons are characteristic of some combination of atomic energy levels and therefore can be used to identify the emitting atom. Auger electrons have relatively low kinetic energy and short mean free paths (1–3 nm) [8]. These factors mean that they provide a surface sensitive probe. Generally, the energy for initial ionisation, and therefore for Auger emission, comes from incident electron beams, which can be focused to a particular point on the sample under test. Varian manufactured the equipment used to perform the AES analysis and this is outlined below. A block diagram is shown in Figure 4.18. The electron gun operating at voltages up to 10 kV has a condenser system to allow the probe sizes to be varied between 50 nm and 5 μm. The electron energy analyser consists of either a cylindrical mirror analyser (CMA) or hemi-cylindrical analyser (HMA) with a collection efficiency for Auger electrons of as much as 10%. The electron detector is a scintillator-photomultiplier or electron multiplier with a variable aperture. The aperture size can be altered and this controls the energy resolution of the spectrometer, which can be varied between 1–40 eV. An initial scan with maximum energy range (typically 0–2 kV) is performed to determine which elements are present and to determine the actual energy range to be used. The ion gun is used to clean samples after the spectrometer is pumped down to a high vacuum of 10^{-10} mbar and also to remove the surface layers so that the underlying material can be investigated.

With an HSA arrangement, a wide angle lens is used to collect and focus the

Auger electrons onto the entrance slot of the analyser. This lens is typically 5–10 cm from the specimen allowing excellent access to the specimen. There are two modes of operation of the retarding lens:

(i) a two electrode lens which reduces the energy of collected electrons by a factor of 20. The lens system and analyser potential are ramped so that electrons of differing energies are collected with increasing resolution; or

(ii) the pass energy of the analyser is set at some pre-selected potential and the electrons collected by the lens are retarded to this preselected energy. This uses a three electrode lens where the middle electrode is scanned in a ramp

The first method is more useful for quantitative analysis since the lens only slows the electrons and does not affect the relative intensities of the electron leaving the material and entering the spectrometer.

With a CMA arrangement, a lens subtends a large angle at the specimen because it is close, typically 1 cm away. Samples must be only a fraction of a millimetre away from the focal point of the CMA if optimum resolution and electron energy accuracies are to be obtained. The analyser in a CMA consists of two concentric cylinders with entrance and exit apertures. Electrons are swept to the exit by ramping the potential between the cylinders.

The quantitative results of AES analysis appear as a series of plots of elemental composition against film depth. These results are shown in Chapter 5, where they are discussed and compared to the other depth profiling methods.

4.6.4 Rutherford backscattering spectroscopy

The Rutherford backscattering spectroscopy (RBS) analysis was performed in the Thomas J. Watson Research Centre, New York under the supervision of Dr. Douglas Buchanan. Two parameters can be determined from Rutherford backscattering spectroscopy (RBS), namely, film thickness and composition. This 'non-destructive' technique is a surface sensitive process which uses a monoenergetic stream of high energy alpha particles, i.e. $^{4}_{2}$He nuclei. Most of the beam passes straight through the test material with only a slight change in energy or direction. Some of the impinging nuclei, however, pass close to the nucleus of an atom in the film under examination and are scattered, changing their direction and energy. The signal 'reflected' back from the target has a 'range' or spectrum of energies, hence the name, backscattering spectroscopy.

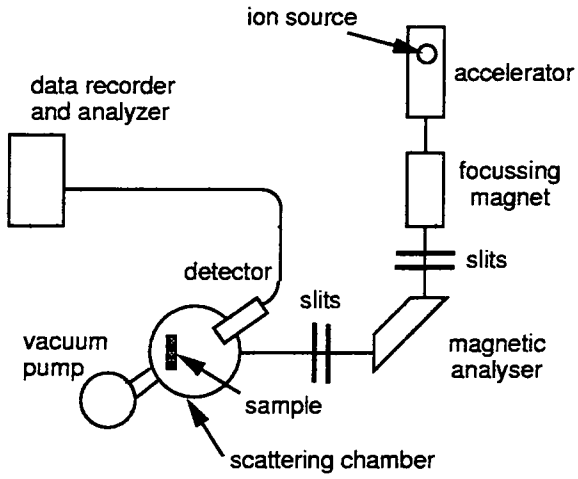

Figure 4.18 Diagram of a typical back-scattering spectroscopy system.

The beam is produced by an ion source and the α-particles are accelerated and focused onto the target which rests in an evacuated scattering chamber. The backscattered particles cause a signal to be generated at the detector. This electrical signal is then amplified and processed by a computer. The system is shown in Figure 4.19 The energy of the scattered particle is determined by:

(i) the element which caused its deflection and, in general, the larger the atomic mass of the target atom the greater the energy of the deflected particle; and

(ii) the position within the film where deflection occurred.

Those particles scattered from the front of the film have more energy than those scattered from the back (because the particles lose energy as they traverse a dense medium). This causes each element to produce a **range** of energies for the deflected particles. To analyse back-scattered signals, the energy spectra are compared with those for standard elements over known film thicknesses. Typical spectra are shown in Figure 4.20. The range of energies that results for one element over a certain film depth is called the 'energy thickness'. The lowest energy recorded for that element, i.e. the energy value at the leading edge of the spectrum, depends only upon the material, energy and type of the incident particle. These two properties, (leading energy value and energy thickness) are used to characterise the measured atomic spectra.

The RBS technique has been used to determine an average elemental composition for films deposited under exactly the same conditions for a range of deposition times. The resulting data for film composition and thickness are tabled in Chapter

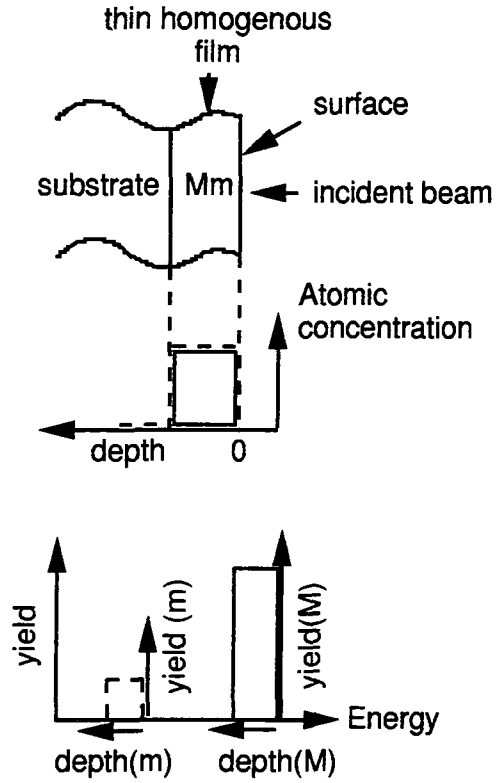

Figure 4.19 An example of electron yields against energy spectrum for a heavy element, M and a light element, m.

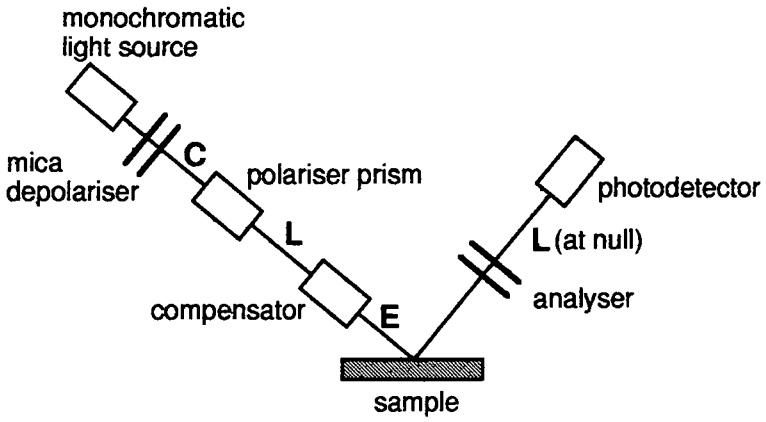

Figure 4.20 Block diagram for a basic ellipsometer.

5, where these results are cross-referenced to results obtained from other techniques, such as those obtained by ellipsometry. The ellipsometry apparatus is described in the following section.

4.7 Physical characterisation

4.7.1 Thickness measurements

Nulling ellipsometry

A purpose-built ellipsometer, mounted on an optical bench in the clean room, was dedicated to the immediate measurement of as-deposited SRO films. A schematic of the ellipsometer is shown in Figure 4.21. A mercury lamp together with a green filter provide quasi-monochromatic light of wavelength 546.1 nm. The light passes through a collimator to produce a parallel beam. A polariser which can be set to any angle in the range 0–360° polarises the light in one direction. A compensator, with fast and slow axes at 45° to the horizontal elliptically polarises the incident light. This elliptically polarised monochromatic beam then impinges on the sample at an angle of 69° to the sample normal. The sample is held in position by a vacuum chuck. Light passes through the film under test, is reflected from the upper surface of the silicon substrate and then passes through the film again and finally into the analyser. The analyser is a plane polarising filter identical to the polariser. Both are surrounded by a disc calibrated in degrees over the angle range 0–360°. An observer looks through a telescope and alters the analyser angle until a light intensity minimum is obtained. The polariser is then adjusted to obtain the best minimum of light intensity or 'null'.

When this can be improved no further, a photomultiplier tube is fitted and the best orientation of the analyser (a_1) and polariser (p_1) obtained.

The polariser is turned through a further 90° ($p_2 = p_1 + 90°$) and the intensity minimum found again after readjustment of the analyser to about 180° minus the first analyser angle ($a_2 = 180° - a_1$). The two parameters Δ and Ψ are defined in terms of the analyser and polariser angles according to the two equations below:

$$\Delta = p_1 + p_2 \qquad\qquad \Psi = \frac{a_1 + 180 - a_2}{2} \tag{4.6}$$

The sizes of Δ and Ψ are related to the degree to which the sample changes the elliptically polarised light.

The electric fields of the incident and reflected beams can be resolved into two linearly polarised components at right angles to each other: the p-component has its electric field vector parallel to the incident light and the s-component has its electric field vector normal to the plane of incidence. After reflection from a sample, the relative amplitudes and phases of the p and s-components change thus altering the size and orientation of the elliptically polarised light. The derivation of the equation of ellipsometry is beyond the scope of this thesis but it is suffice to say that it relates the changes in the p and s-components to Δ and Ψ. The basic equation of ellipsometry is [9]:

$$\rho = e^{i\Delta} \tan \Psi \tag{4.7}$$

where ρ is the ratio of the complex coefficient of the p-component to that of the s-component.

Since the mathematics is complicated, this relationship has been programmed in a computer. The computer compares the measured angles with the values of standard curves and the points of best fit are obtained. From these curves, the thickness and refractive index of the film can be obtained.

There are problems with this type of measurement. Mercury lamps are well-known for causing inconsistencies in the quasi-monochromatic light, which in turn will cause a drift in the observed 'null' angles. Also, since the amplitude and phase changes are cyclical with thickness, a series of values are obtained. The cyclic functions of film thickness arise from the fact that ellipsometry is based on an interference effect of the two reflected beams, one from the film surface and the other form the film-substrate interface. When the optical path length of the light traversing the film reaches an integral number of wavelengths the effect is the same as if there was no film present.

To be certain about the measurements, an alternative method would need to agree with those values obtained from the ellipsometer.

An improvement was to use a computerised ellipsometer, the Rudolph Research Auto EL-IV nulling ellipsometer, which operated at several wavelengths. This consisted of two parts: an optical system for measuring the values of the angles Δ and Ψ and a dedicated computer to convert these angles into physical film parameters.

This ellipsometer was situated in the Langmuir-Blodgett film laboratory, a class 10,000 cleanroom. Samples were placed in an evacuated chamber and measured at a later date. Both ellipsometers take a couple of hours to 'warm-up' to ensure that the lamps produce steady monochromatic beams. The Auto EL-IV produces monochromatic light at three different wavelengths: 632.8, 546.1 and 405 nm and the measurement is totally automated. Calibration is checked against standard SiO_2 samples before the test sample is placed onto the stage. The operator aligns the beam to the correct angle of incidence and focuses the beam on the film surface before measurements are taken. The machine is programmed with several options. Two different measuring wavelengths were used in this work. Due to the cyclical nature of the functions involved in ellipsometry, the angles Ψ and Δ, at a particular wavelength, determine a series of possible values for the film thickness each greater than the preceding one by the 'cycle' thickness. By performing the ellipsometric measurements at two different wavelengths, two series of results are obtained. Since the thickness of the film is independent of wavelength, there should be an approximate thickness 'match' between the two series. This value is the film thickness.

Values of film thickness are plotted against deposition time in Chapter 5. The resulting growth rate is then compared to the results obtained from RBS and Alpha step measurements on the same films. Ellipsometry also measures the refractive index of the samples, which can give an indication of the amount of silicon present. The refractive indices obtained from ellipsometry have been used to cross-reference the data with that obtained from AES studies to test for reasonable agreement of the results. This comparison is given in detail in Chapter 5.

4.8 Structural characterisation.

4.8.1 Scanning electron microscopy

Scanning electron microscopy, (SEM), has been used for structural analysis of materials for over sixty years [11]. In previous sections of this Chapter, techniques have

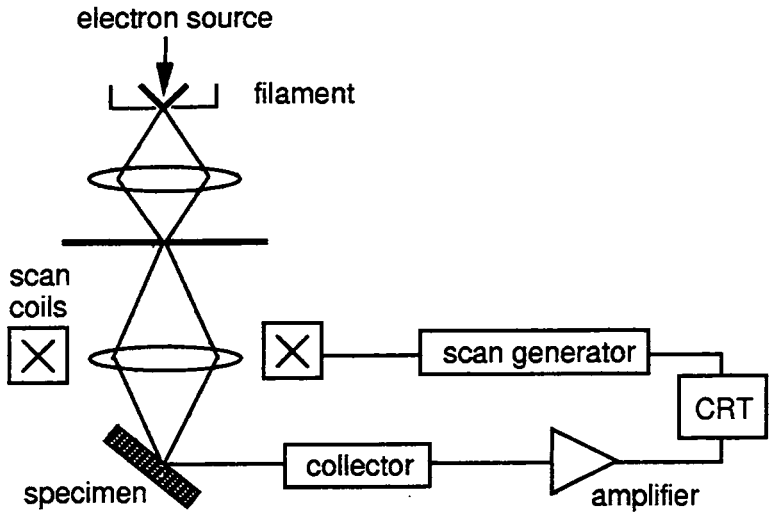

Figure 4.21 A typical arrangement for a scanning electron microscope.

been used that have supplied information on the elemental composition of the SRO film and also on its bonding. SEM was undertaken to investigate the film structure. It is not the aim of this work to provide a detailed account of such a well-established technique but since the other processes used have been described, a brief outline of this measurement technique is included for completeness.

SEM is used for the examination of thicker samples which are electron-opaque. An electron probe scans the surface of a specimen and electrons are either emitted or back-scattered from the sample to provide:

(i) topological information if the low energy secondary electrons are collected; or

(ii) atomic number or orientation information if the instrument is set up to collect the high energy or back-scattered electrons.

Initial experiments were performed with a Stereoscan 600 and later experiments with a JSM-IC848 scanning electron microscopes. Figure 4.22 shows a schematic diagram of the instruments. An electron gun produces a beam of electrons from a filament with an effective diameter of 50 μm. A series of lenses demagnify the beam and a final lens, often called the objective, focuses the beam onto the specimen. The beam scans across the specimen in a raster fashion similar to that used in a television picture.

A grid in front of the detector can be biased positively (as used in this study) to attract low energy secondary electrons or biased negatively to detect high energy reflected electrons. Behind the grid is a positively biased scintillator which is optically

coupled to a photomultiplier. The signals from the multiplier are amplified and then used to modulate the brightness of the cathode ray tubes (CRT). A three-dimensional image of the specimen results from the reflection and emission electrons from different parts of the sample.

A minimum of sample preparation is required for this technique. The SRO-covered wafers were cleaved by a mechanical stylus to fit the sample holder or stub. A layer of conductive silver paint was used to hold the specimen in place on the stub. The stub was mounted on a stage which could be moved in x, y and z directions. The sample chamber was evacuated and the magnification, brightness and filament voltage altered to obtain clear images of the film surface. Each instrument has at least two CRTs: one used for video display; and the other to record photographic evidence. Such photographs are included in Chapter 5, where they are discussed in detail and where a physical structure of the film is proposed.

4.8.2 Transmission electron microscopy

I am grateful to Dr. Douglas Buchanan, under whose supervision the transmission electron microscopy (TEM) analysis was performed in the Thomas J. Watson Research Centre, New York. Since this technique can only be applied to thin samples, only those films deposited in 0.5 minutes were used. Electrons must be able to pass through the films if this technique is to be successful. The transmitted electrons formed an image or a diffraction pattern of the specimen. An object aperture placed in front of the objective lens at its focal plane allows only one electron beam through. A bright field image is formed if the directly transmitted beam is selected. A dark field image is formed if the diffracted beam is selected. For high resolution electron microscopy (HREM), many diffracted beams together with elastically and inelastically scattered electrons must pass through the objective aperture if the periodicity of the sample and departures from periodicity are to be seen [8]

Plan view

A 3 mm diameter specimen was ground to a thickness of 100 μm using abrasive papers of 400 and 600 grit followed by polishing with 3 μm, 1 μm and 0.25 μm alumina and diamond polishing compound. The damaged region beneath the surface extends to a depth of three times the diameter of the grit used. Therefore, the next grit removes entirely all the damage from the previous grit. The process is repeated on the other surface of the wafer in order to produce discs with smooth surfaces and parallel sides.

The centre of the disc is dimpled by approximately 20–30 μm on each side with a dimpling apparatus.

The final thinning was by ion-beam milling. In this process a 2–6 kV ion beam impinges on the specimen at an angle of less than twelve degrees whilst the sample is rotated. Iodine ions are often used for semiconductors. Since the ion beam can generate crystalline defects in the specimen, it is preferable to start with the thinnest polished disc possible and to reduce the ion-milling time to a minimum. Often the temperatures are kept low during ion-beam milling.

Cross-section

Two samples may be glued together face-to-face with epoxy and then the composite is mounted in epoxy. The resultant sample is then sliced to form a 200–300 μm thick cross-section wafer which is then ground to a thickness of 100 μm with fine abrasive paper. After dimpling, the final thinning is again done with an ion-miller [10].

Photographic evidence of the cross-section of typical thin SRO samples are shown in Chapter 5. These photographs were compared to those produced by SEM and were found to confirm the initial proposal of the SRO film structure.

4.9 Summary

The equipment used and processes involved in the manufacture and testing of MIS devices have been described. Additional detail on the fabrication processes can be obtained from Appendix B. Problems encountered in making reliable electrical contact to the devices have been outlined. Gold wire bonding was adopted in favour of probing methods. Additional information on gold wire bonding can be obtained from Appendix C. The electrical measurements were made over a range of temperatures up to a maximum of 20 degrees Celsius. Each device was taken down to at least -50 degrees Celsius over a period of 5 hours. In the remaining part of 24 hours the devices warmed naturally to room temperature. The data collected, over 24 hour periods, were stored on disk. Data acquisition was software controlled. The hardware required and software package used have been described in section 4.5. Structural parameters such as film thickness were determined using electron microscopy, and ellipsometry. Compositional information was obtained using various types of spectroscopy, namely: glow discharge; optical emission; secondary ion mass; Auger electron; and Rutherford backscattering spectroscopy. A brief outline of the operation of each piece of

equipment and also details of sample preparation have been described.

The following Chapter describes the results of the spectroscopic, microscopic and ellipsometric studies.

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Chapter 5

Physical characterisation

5.1 Introduction

The aim of this work is to characterise the metal-SRO-semiconductor (MIS) structure, both electrically and physically, to understand how it functions as a semiconductor device. In particular, it is important to determine the film deposition factors that must be controlled to optimise the manufacture of reproducible MISS devices at Durham [1, 2]. Information concerning the SRO film thickness, composition and structure will help in the elucidation of the conduction mechanisms. The thickness of the film is an important parameter in determining the magnitude of the electric field developed across it. Since the electric field occurs in many conduction mechanism formulae, an accurate measure of thickness is essential when analysing current density versus electric field (J-E) data.

Knowledge of the composition of the film and how the constituent elements are distributed within it will help in explaining the physical processes that occur when current flows through the film. This will also be important in determining the structural link between the silicon and SRO. The interface region is thought to be very important in determining the observed non-symmetrical I-V or J-E characteristics. Various methods have been used to determine the elemental bonding, distribution and composition of the semi-insulator. These include Auger electron spectroscopy (AES), secondary ion mass spectroscopy (SIMS), glow discharge optical emission spectroscopy (GDS), scanning electron microscopy (SEM) and Rutherford back-scattering spectroscopy (RBS). Some of these experiments have also provided thickness information. In addition, several other techniques have been used to determine the film thickness. These include: transmission electron microscopy (TEM), Alpha-step and

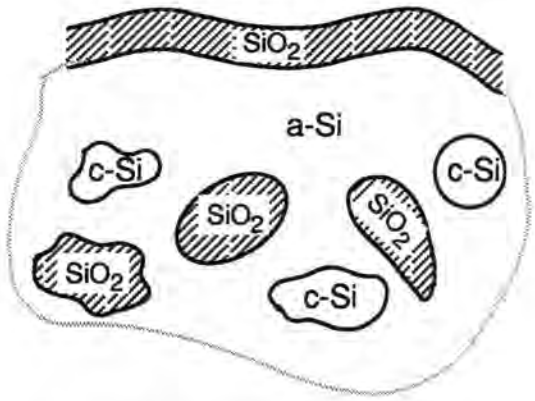

Figure 5.1 Mosaic model, c-Si is crystalline silicon and a-Si is amorphous silicon [5].

ellipsometry. Each of these was outlined in Chapter 4.

There has been much interest in the structure of silicon-rich oxides. Many research teams have been involved in the investigation of the way in which the silicon and oxygen atoms are arranged within the films. Silicon-rich oxide is thought to be diphasic at high or low concentrations [3]. If the atomic percentage of oxygen is low, Si-Si bonds are likely with Si-O as interstitial impurities. For higher atomic percentages of oxygen, the formation of Si-O bonds is more likely [4]. Several models have been developed to describe the way in which the silicon and oxygen atoms are arranged within silicon-rich oxides.

In this Chapter, experimental evidence is presented for the composition, structure and elemental bonding within silicon-rich oxide. These results are then compared with the prediction of theoretical models, described in the following section, and a model for the microstructure of SRO is proposed.

5.2 Models for silicon-rich oxide microstructure

Mosaic model

A mosaic structure of silicon nanocrystals and silicon dioxide regions dispersed in a matrix of amorphous silicon has been proposed [5], Figure 5.1. The size of the silicon crystals depends on both the deposition temperature and the oxygen concentration. However, there has been debate as to whether or not silicon nanocrystals of 1 nm or less exist in as-deposited films [6 to 9].

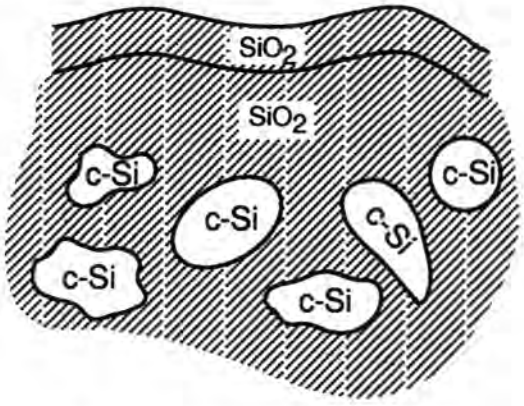

Figure 5.2 Shell model [10].

Shell model

This model, shown in Figure 5.2, consists of silicon grains surrounded by silicon dioxide and was suggested by Ni and Arnold [10]. Abeles *et al* [11] varied the oxygen content of SRO and studied the resultant conductivity. If the film was assumed to be 100% silicon a high conductivity was expected, since there would be a complete conduction path from the silicon substrate to the top contact metal. As the concentration of silicon dioxide increased there would be fewer silicon regions which formed a complete bridge between the substrate and top contact. The number of complete conduction paths would therefore decrease and the conductivity would be expected to decrease. With increased silicon dioxide concentration, the insulating silicon dioxide regions were expected to grow until eventually they interrupted every conduction path. At this concentration, the conductivity was expected to show a sudden decrease of several orders of magnitude. The point immediately before this drop in conductivity is called the percolation threshold [11]. Such a decrease has never been reported. The fact that the percolation threshold is not observed suggests that the silicon grains are surrounded by SiO_2 at all oxygen concentrations. DiMaria *et al* [12] support the shell model with a slight modification so that the silicon grains lie inside a SiO_x matrix.

The modified shell model

This model, shown in Figure 5.3, was proposed by Brüesch *et al* [8]. The structure of the silicon-rich oxide film depends on the amount of oxygen present. If $\gamma = 0$ (Chapter 4, section 4.2.7), columnar crystalline silicon growth results. For SiO_x and

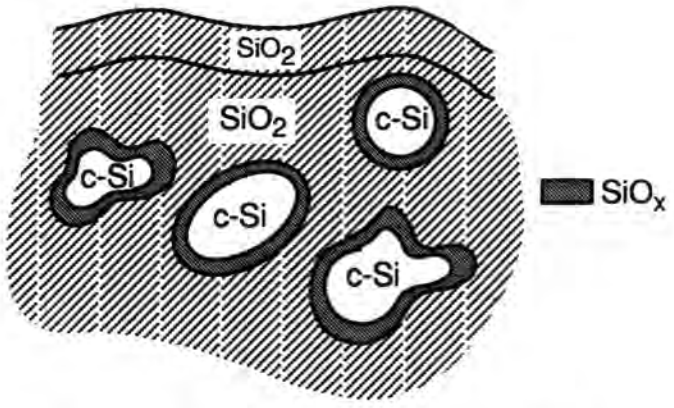

Figure 5.3 Modified shell model [8].

if x lies between 0.034–0.4, there is a transition from crystalline to amorphous silicon grains accompanied by a large reduction in grain size. If $x > 0.4$, the silicon grains are completely amorphous. The grains are surrounded by an inner shell of SiO_x and an outer shell of SiO_2 where SiO_x represents a range of transition oxides. For $x > 0.4$, the diagram is as shown in Figure 5.3 but all the Si grains are amorphous. Brüesch *et al* also mention two earlier models: the random mixture model (RMM) where the Si and SiO_2 are mixed at the level of several tetrahedral units; and the random bond model (RBM) which involves a complete mixing of Si-Si and Si-O bonds.

The continuous network model

This model was first described by Brunson *et al* [3] and postulates the silicon-rich oxide as existing in a continuous network. If the oxygen concentration is less than 26%, there is not enough oxygen to prevent a continuous silicon network. However, if the oxygen content is greater than 34%, there is not enough silicon to prevent a continuous oxygen network. Either silicon islands exist within SiO_2 or vice-versa. The continuous model is shown in Figure 5.4. A percolation threshold is expected at approximately 34–38% oxygen, but this has never been reported.

The three-dimensional network model

The three-dimensional network model was proposed by Shirley *et al* [13]. The data of Kwark and Swanson [14] revealed that a small decrease in the silicon phase produced a large increase in the optical absorption coefficients. Shirley concluded that the interface between the silicon and oxide phases was larger than that estimated by a separate grain model. Shirley proposed that each phase grows continuously in columns

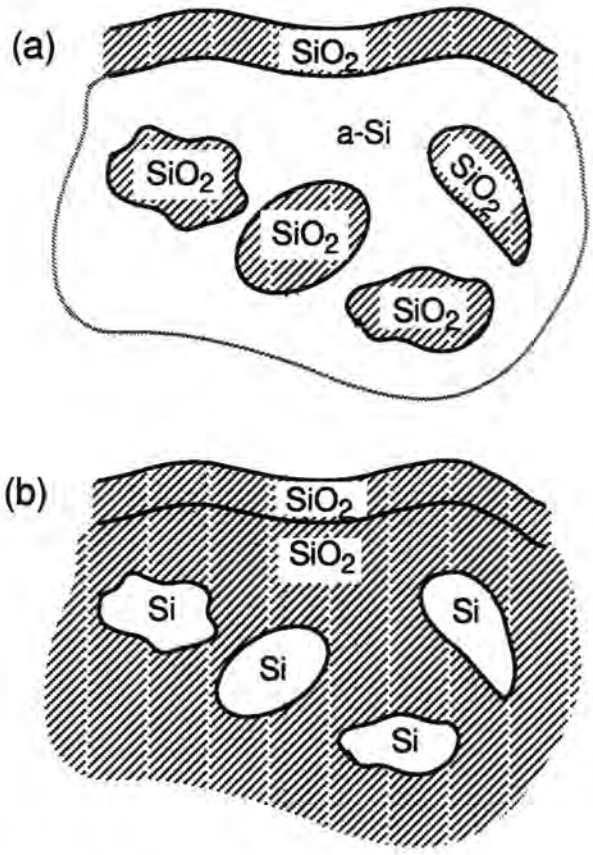

Figure 5.4 Continuous network model. Figure (a) shows a continuous network of amorphous silicon with embedded silicon dioxide islands. Figure (b) shows a continuous network of silicon dioxide with embedded silicon islands [3].

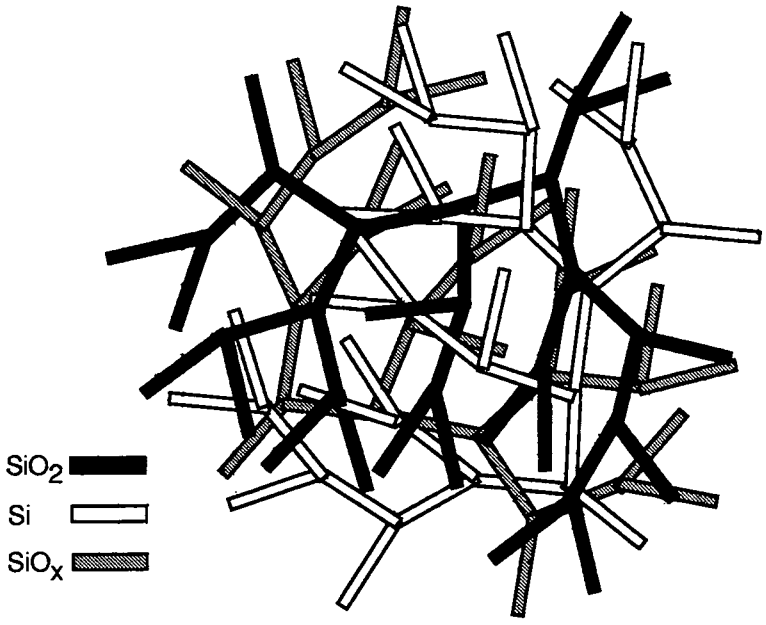

Figure 5.5 The three-dimensional network model [13].

or veins with branches due to fluctuations in surface temperatures and reactant gas flows. These branches intersect each other to produce a three-dimensional network with thinner and thicker parts to the mesh. A diagram for this model is shown in Figure 5.5. To assess which of the above models best describes the microstructure of SRO, evidence of film composition, elemental bonding and structure is needed. Film composition is the first parameter to be reviewed. Measurement techniques and results are discussed in the following sections.

5.3 Compositional analysis

5.3.1 Glow discharge optical emission spectroscopy

Glow Discharge Optical Emission Spectroscopy (GDS) was used for depth profiling. In this process, the sample acts as a cathode in a d.c. glow discharge system. Highly energetic positive ions of the working gas, argon, are focused onto the surface of the sample causing layers of atoms to be sputtered away. Atoms released from the exposed surface produce an individual characteristic radiation which is analysed by an optical spectrometer, by reference to standard samples. The process of sputtering has already been described in Chapter 4.

A major advantage of GDS over other profiling methods, such as AES or SIMS, is

that it takes only about 15 minutes from the initial mounting of the sample to analysis of the results. However, large sample areas are required. An estimate of the average composition of SRO films deposited in two minutes was obtained. The technique is still in its infancy and has not been fully investigated for all elements (at the time of writing). For the elements present in SRO films, however, the equipment at Sheffield is thought to be reliably calibrated [15]. The depth resolution has been called into question by some authors [16] but the GDS technique remains a good qualitative method.

Analysis of GDS results

The unsmoothed results of the sputtering of a typical SRO film (deposited on n-type silicon) are shown in Figure 5.6. The initial uncertainty in the signal is due to the setting up of the plasma. This can also be seen in Figure 5.7, which are the results of sputtering a typical silicon dioxide layer (grown as a gate oxide on n-type silicon). This gate oxide, grown in a dry-oxidation furnace at 1050 ° C, is included for comparison. The films are 200 nm – 300 nm thick. Both graphs show the presence of hydrogen and carbon within the films. The measurements are not absolute but have been scaled to show more clearly how the amount of each element alters with film depth. Hydrogen has been increased by a factor of two and carbon by a factor of four. GDS has been used in this study to indicate the way in which the elements are distributed in the SRO film. A comparison of Figures 5.6 and 5.7 shows that the pattern of distribution varies for these elements from film to film and therefore is unlikely to be a characteristic of the GDS process. The carbon in the SRO film was initially thought to have originated from the carbon susceptor of the CVD reactor but it seems that all silicon oxide films have some carbon present. This may have come from the chemical treatments applied to the wafer during cleaning and photolithography or may have originated from the walls of the deposition furnace. Since carbon and silicon are both group IV elements, it is likely that carbon could easily be assimilated into the silicon oxide layer. Hydrogen may have come from the water vapour present in the walls of the deposition furnace or from the subsequent chemical processing. However, the most likely source is silane. Both GDS plots show that the carbon and hydrogen concentrations follow that of oxygen. This suggests that carbon, hydrogen and oxygen are incorporated in the film as a C-H-O compound.

In interpreting the silicon and oxygen data, the graphs should be consulted from just after one second on the time axis. The SRO has been sputtered completely by 6.1 s

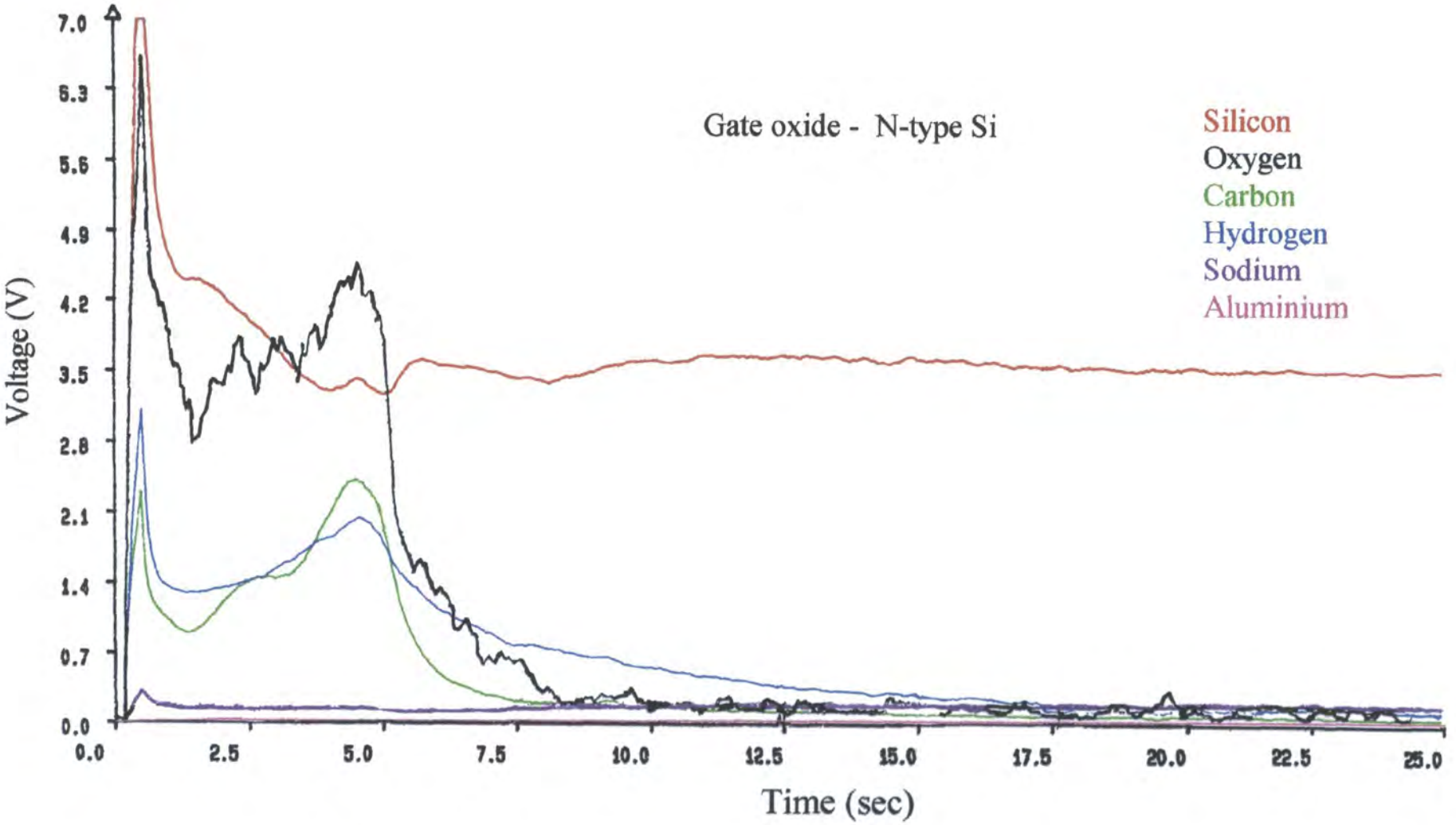

Figure 5.7 Elemental composition of a silicon dioxide gate oxide as a function of depth by GDS analysis.

and the gate oxide by 10 s. There is a marked difference in the way in which silicon and oxygen are distributed within the two films. Figure 5.6 shows that there is a very gradual interface between the silicon and silicon rich oxide. The oxygen increases from the wafer surface to a maximum at the surface of the film. Figure 5.7 shows a fairly abrupt junction between the silicon wafer and the silicon dioxide layer. The silicon increases towards the film surface whereas the oxygen decreases in concentration. This contrasts with the oxygen distribution in silicon-rich oxide. This gradual change from silicon to silicon-rich oxide is also confirmed from other studies as described in the following sections.

5.3.2 Secondary ion mass spectroscopy

Secondary Ion Mass Spectroscopy (SIMS) is a well-established technique used for bulk composition analysis. The system requires calibration but is then capable of qualitative analysis with good sensitivity to some species [17]. The SRO films provide suitable samples for this, another sputtering technique, which has been described in some detail in Chapter 4. Samples deposited in 1.5 minutes, under exactly the same conditions as those sent for GDS analysis, were sent for SIMS and AES processing.

Analysis of SIMS results

The results of the SIMS process are shown in the two spectra of Figures 5.8 and 5.9.

The spectra were recorded as a function of time, as the sample was sputtered. The origins of the spectra therefore represent the SRO film surface as the beam moves inwards towards the silicon wafer with time. Unfortunately, with SIMS it is not possible to calibrate for depth by reference to the rate of erosion of standard samples. Therefore, information concerning film thickness cannot be obtained from SIMS spectra but they do reveal some compositional detail of the SRO film under test.

The two plots show similar features but have been taken using different ion currents. Figure 5.8 displays different ion counts for silicon than those obtained in Figure 5.9. Ion yield is sensitive to the incident ion species, their energy and the method of measurement of the mass spectrum, as outlined in Chapter 4. Preliminary investigations were made to set up the apparatus for each sample. The two plots can be used to determine how the percentage composition of a particular element varied from substrate to air interface but do not present absolute comparisons of the atomic percentages of various elements at a particular point in the film.

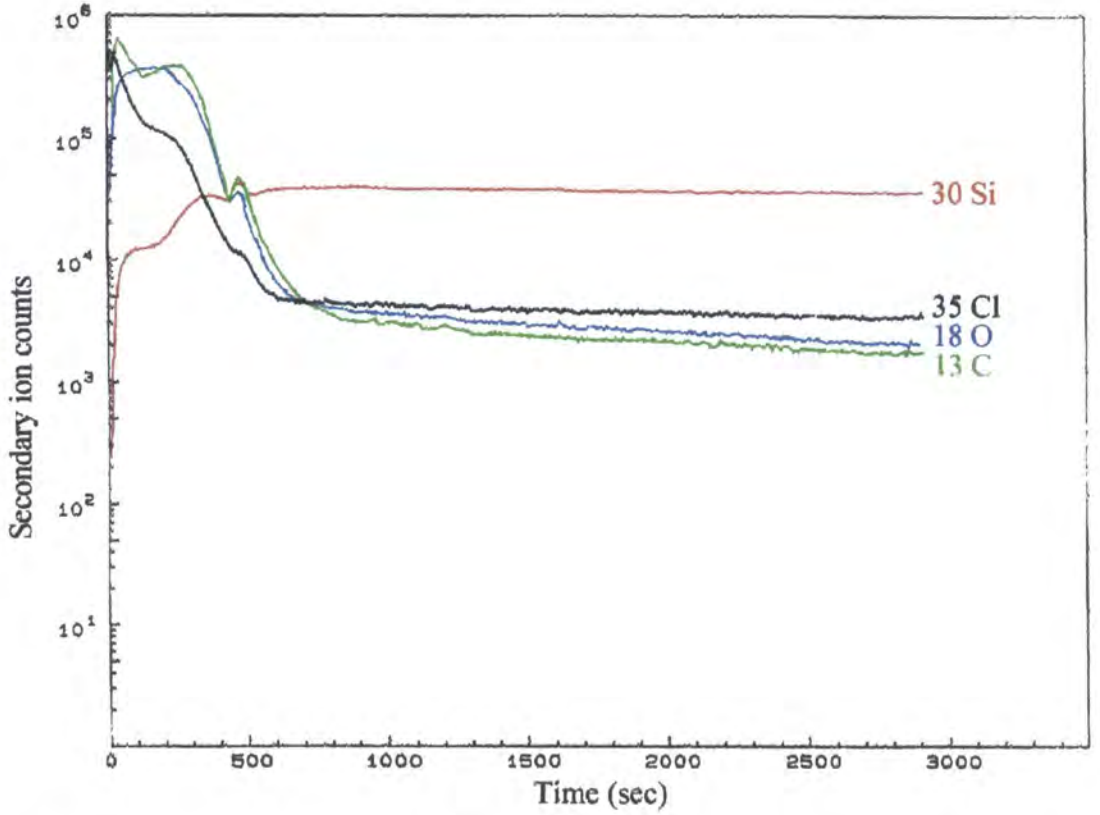

Figure 5.8 Elemental composition of SRO as a function of film depth by SIMS using high ion current values.

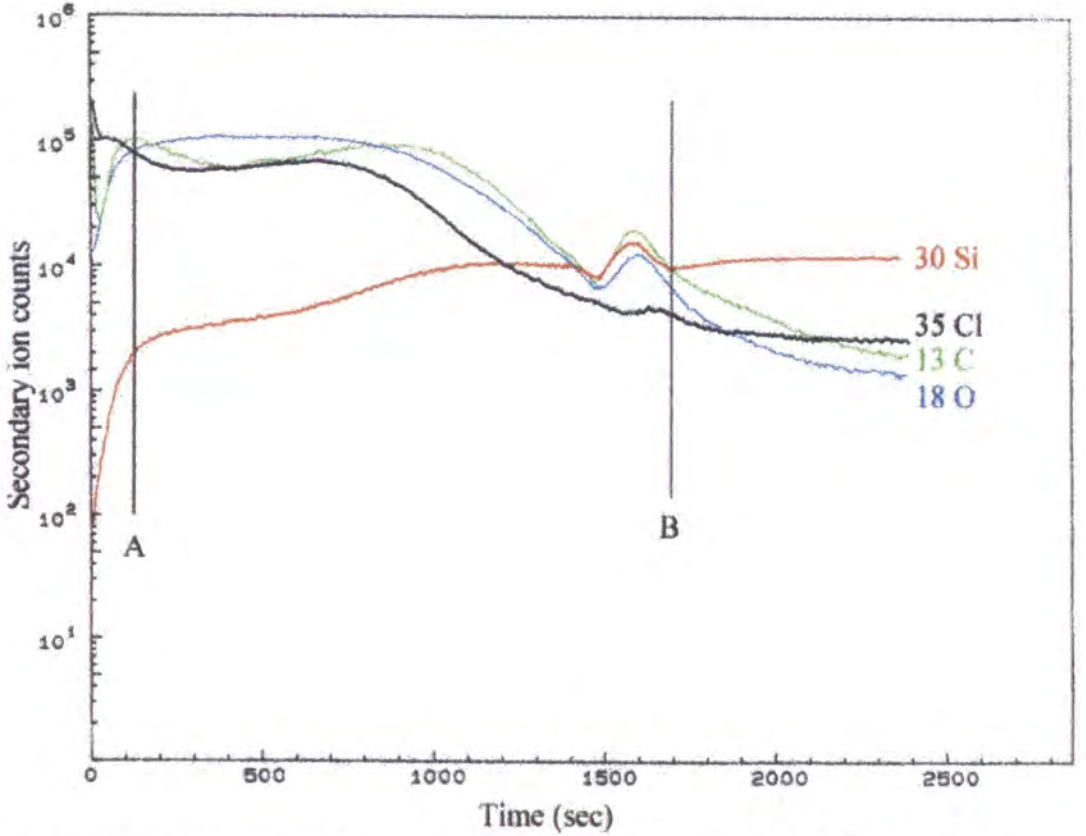

Figure 5.9 Elemental composition of SRO as a function of film depth by SIMS analysis using low ion current values.

Figure 5.9 shows that it takes longer to sputter to the same point in the film with the lower ion current than that used to produce the results shown in Figure 5.8. Since Figure 5.9 shows the signals spread out over a larger time interval, it reveals more detail and will be discussed further below.

Near the origin of the graph, the composition of the film appears to change abruptly, but this is assumed to be an artefact of the SIMS process itself rather than a property of the SRO film. The analysis of the film therefore should be considered between the two lines marked A and B. Like the GDS process, SIMS revealed that carbon was present throughout the film but, unlike GDS, the SIMS technique also showed that 1% of the film was chlorine. This contamination is most likely to have originated from the chemical treatments used on this test sample before it was sent for SIMS analysis.

The interesting spectra are those of the silicon and oxygen. Starting at the substrate, line B, there is some native silicon dioxide present, as shown by the feature at 1600 seconds. This is expected since, once cleaned, the wafer is immersed in ultrapure water, dried in nitrogen, transported to the susceptor in air and is bathed in air until the CVD reactor is flushed out with nitrogen. Inevitably a nascent oxide must form. The oxygen line shows the oxygen concentration increases significantly moving from the substrate to the surface of the film (note that the ordinate axis has a logarithmic scale). In contrast, the silicon concentration falls from substrate to the film surface.

In summary, the film appears to have three regions:

(i) the nascent oxide;

(ii) an oxide region 'rich' in silicon near the substrate; and

(iii) a region with a lower silicon content, therefore becoming nearer the stoichiometric silicon dioxide at the air/film interface.

It would seem logical to suggest that there may be a fourth region of silicon dioxide, as a final top layer of the film, with the normal 33% silicon and 67% proportions. This is expected since elemental silicon readily reacts with oxygen, when exposed to the air at room temperature. The SIMS process, however, did not show this layer.

Finally, reservations about analysing the film, on the grounds that oxide layers are insulating and this could cause charge accumulation which would hinder the SIMS analysis, proved to be unfounded. The SRO films did not store charge and did not show the insulating behaviour normally observed in silicon oxides. SRO is therefore more conductive than stoichiometric silicon dioxide.

AES analysis was subsequently performed on the same sample used in the SIMS analysis. This was to seek confirmation of the structure obtained from these sputtering techniques.

5.3.3 Electron spectroscopy

Introduction

The commercial equipment and theory of Auger Electron Spectroscopy (AES) has been described in detail in Chapter 4. AES has been used to identify the percentage composition, distribution and bonding of the elements which make up the SRO film. The results are discussed and compared with previous methods of compositional film analysis. First, the limitations of the technique are outlined in the following section.

Limitations

Collections of 'fingerprint' spectra for essentially every element exist for identification purposes [17]. Interpretation of AES results, however, is not as simple as comparing data with one standard set of spectral lines for each element. AES shows variations in energy shifts and line shapes due to local bonding arrangements. For example, the emission spectrum for carbon depends upon whether the carbon atom is involved in a single, double or triple bond. Of particular importance to this research is the fact that the spectral peaks from clean silicon wafers are shifted when compared with spectra from silicon bonded with silicon dioxide, from 92 eV to 70 eV [17].

Atoms capable of creating two holes for Auger emission have more complicated spectra with a multiplicity of lines. In theory the number of Auger electrons represents the number of atoms of a particular element in the test sample. Yields of Auger electrons may be too high due to an Auger electron decaying and releasing energy which produces a second Auger transition within the same atom. Back-scattered or secondary electrons can also cause a yield variation of at least a factor of two [17]. Maximum Auger electron yield results from primary electron energies of at least three times the binding energy of the deepest core levels of interest (normally 1–1.5 keV). This means that 3–5 keV are the primary incident energies used. Within this range, there is plenty of scope for inelastically scattered electrons to ionise core levels.

Diffraction of the incident electron beam varies with crystallographic direction. This causes marked variations in the penetration of the incident beam with direction. Fortunately, this effect induces comparable changes in both substrate and surface

adsorbants or contaminants so that normalisation of the Auger yields can minimise this error. The angle of incidence of the beam is also important since the larger the grazing angle, the greater the probability of ionisation as the path length of the incident beam increases.

Interpretation of the AES data is therefore very complicated. Corrections are made by performing a calibration experiment with the particular system of interest. The limitations listed above cause AES to be a relative rather than an absolute measuring technique. It is usual to show the derivative of electron yield against electron energy when identifying elements. The constant secondary background count is then suppressed but also the simple peak is changed to extended negative and positive peaks. It is the negative peak which is used in species identification. The results of this detailed analysis are discussed in the next section.

Auger analysis

The results of the Auger analysis are shown in Figure 5.10. The origin of the plot represents the top, outermost surface of the SRO film and the abscissa represents depth into the film, measured in nanometres. There are two ordinates. The left-hand scale is a measure of composition (as atomic percentage, 0–100%) and applies to all species except carbon. The right-hand side is atomic percentage (0–10%) and applies only to carbon. The Auger experiment was repeated twice on each sample and gave the same results.

Chlorine was not shown to be present in the SRO film using AES. Since AES cannot detect hydrogen, this element is not noted in Figure 5.10. Often carbon is found to be present in samples which have undergone Auger analysis This may be attributed to a characteristic of the process itself [18]. The AES technique has revealed that 1% of the film is carbon, increasing to a value of 2% midway through the film. Since GDS and SIMS also showed this element to be present, it must be concluded that carbon is a contaminant throughout the film. GDS and SIMS gave an indication of the amounts of carbon and oxygen in the film but Figure 5.10 gives a lower percentage of carbon than the GDS and SIMS spectra suggested. Unlike GDS, AES is a well-documented, tried and tested technique and unlike the SIMS technique repeat runs on similar samples revealed very similar atomic compositions. The AES results are therefore presented with most confidence.

There are surprising results to come from this analysis as well as some more expected findings. First, as previous techniques have shown, there is no sharp interface

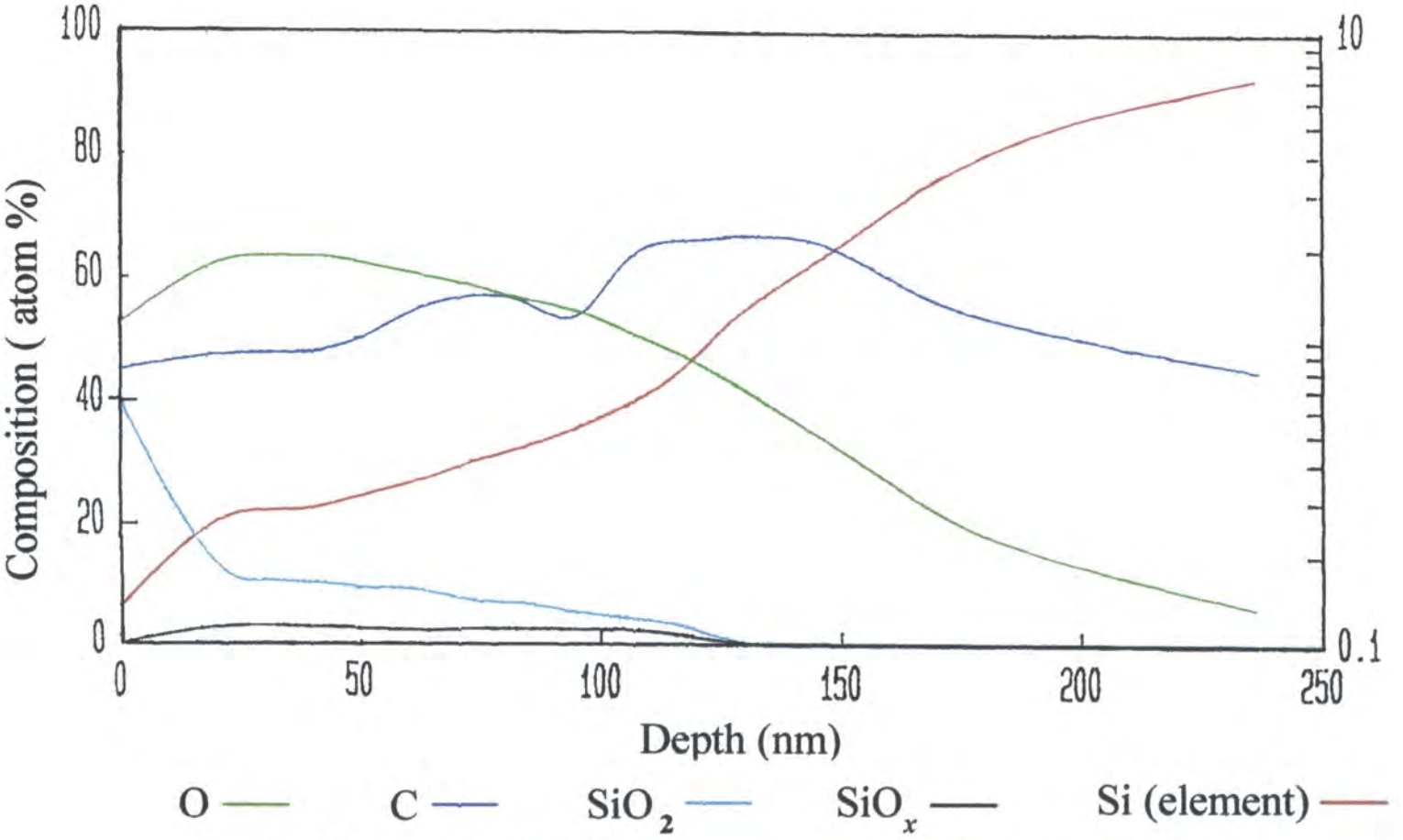

Figure 5.10 Elemental composition of SRO as a function of film depth by AES analysis.

between silicon and its oxide layer in these films. Unfortunately, the Auger experiment was not carried out for long enough to reach the absolute edge of the film where 100% elemental silicon would be expected. The plot shows that the elemental silicon line falls from about 95% at the substrate to 5% at the top surface of the film.

At a distance of only 10 nm from the top surface of the film, 20% of the film is composed of elemental silicon. This would account for the higher conductivity of the films and the lack of charging observed in the SIMS data. The sudden drop in percentage of elemental silicon coincides with the sudden increase in silicon dioxide throughout the top 10 nm of film. Any silicon with dangling bonds in the surface would inevitably become oxidised. Normally the width of this silicon dioxide layer is 1–2 nm [18]. Therefore the underlying 8 nm of silicon dioxide must be a property of the SRO film.

The distribution of silicon dioxide is unusual. Certainly a coating of silicon dioxide was expected on the outer surface of the film but a further oxidised layer was predicted at the silicon interface. This layer was shown to exist by SIMS. If the Auger process had run for longer, it may have revealed this other silicon dioxide layer. More interestingly, the film contains SiO and SiO_2 (both occur throughout the same region of the film), but these oxides only account for less than 15% of the film. A far larger percentage was expected, since most models for the microstructure of silicon-rich oxides suggest high concentrations of both SiO_2 and SiO. The unoxidised silicon may take the form of silicon islands embedded within the 'oxide' layer. This elemental silicon accounts for a large percentage (approximately 43%) midway through the film. At this point however, the data suggest that 43% of the film appears to be in the form of elemental oxygen! The idea of inclusions of elemental oxygen is difficult to reconcile with the reactivity of oxygen. Other elements, such as, iron or chromium were thought to be present as contaminants but these metal oxides should have shown up in the Auger spectra. Perhaps the oxygen could be bonded to the silicon as a hydroxide. The GDS experiment did reveal the presence of hydrogen in the SRO films. Referring to Figure 5.6, the hydrogen line follows the oxygen line but at a lower concentration.

The existence of silicon hydride (SiH) and silicon hydroxide or silanol (SiOH) groups in hydrated silicon has been inferred from infra-red absorption measurements [19] which detect the presence of the oxygen-hydrogen bond. Both water molecules and silanol groups have been shown to exist in hydrated oxides [20]. Water is thought to enter the silica as water molecules occupying interstitial sites. These molecules then react with a silicon-oxygen bridge to form a part of the silanol groups

according to the following scheme

$$H_2O + Si—O—Si \longrightarrow Si—OH + OH—Si \tag{5.1}$$

When the Si–O–Si bridge reacts with a water molecule to form a silanol pair another oxygen ion and two hydrogen ions must be inserted between them. This reaction can only occur if the imposed lattice strain is relieved by a shift of the ions in their immediate neighbourhood to decrease the void volume around them. Once formed, the silanol structure gives more order to the material. It is believed that the silanol pair is thermodynamically stable.

Over a period of time the reaction does reverse according to the equation

$$Si—OH + OH—Si \longrightarrow Si—O—Si + H_2O \tag{5.2}$$

but this reaction is much slower. It is possible therefore that there are a large number of silanol pairs and voids throughout the SRO.

The final method of compositional analysis used was that of Rutherford backscattering spectroscopy (RBS). This method, like AES, reveals details of composition and sample thickness.

5.3.4 Rutherford backscattering spectroscopy

Rutherford backscattering spectroscopy (RBS) has been used to determine film composition and thickness. This technique has been described in detail in Chapter 4. The back-scattered electrons are used to characterise the atoms which make up the sample under test. A major problem with the interpretation of backscattered signals for the thin SRO films is that the films are grown on a silicon substrate. Any signal produced by silicon within the film itself is swamped by the strong silicon signal from the substrate. The most common method of eliminating this problem is to channel the He^+ ions through the crystal of the substrate in a particular direction. By aligning the beam in a certain direction the probability of the substrate atoms causing a scattering event is much reduced.

The RBS studies were performed at IBM's Watson Research Centre in New York. Previous work at Durham [21] investigated the excess silicon content as a function of both the deposition temperature and the gas phase ratio, γ (section 4.2.7). The results are summarised in Figure 5.11. From Figure 5.11 the excess silicon expected in the films studied by the author is approximately 37% and therefore the total percentage

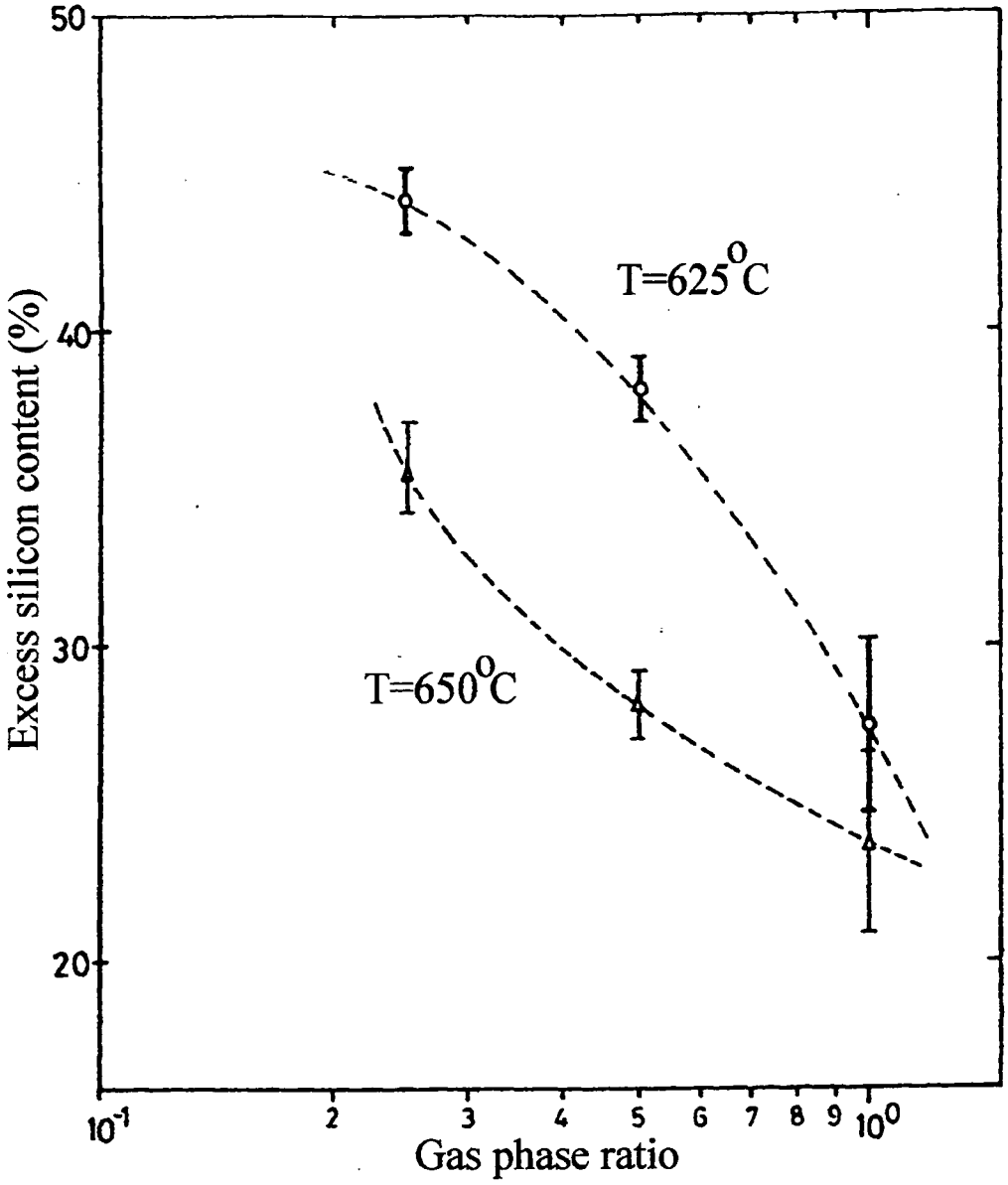

Figure 5.11 Excess silicon content (over stoichiometric silicon dioxide) as a function of the gas phase ratio, γ, for deposition temperatures of 625°C and 650°C by RBS analysis [22].

Deposition time (minutes)	Concentrations (x 10^{17} cm^{-3}) silicon	oxygen	% silicon	% excess silicon
1	1.94(23%)	0.54(25%)	77.2(4%)	44(4%)
1.5	8.50(21%)	4.37(2%)	64.6(8%)	31.3(17%)
2	4.44(0.2%)	1.56(15%)	74(4%)	41(4%)
4	3.63	13.15	-	OXYGEN RICH
8	-	-	-	OXYGEN RICH

Table 5.1 Measurement of excess Si using RBS. The table shows the average atomic percentage of each element and the standard error values.

of silicon in the films is about 70%. This figure assumes a homogeneous material of constant composition, which is independent of film thickness. Work covered in earlier sections of this Chapter show that these assumptions are inaccurate.

Further RBS analysis was performed on a series of SRO films of varying deposition times. Figure 5.12 shows a typical set of SRO RBS spectra. Each element corresponds to a certain energy range on the energy axis (x-axis) in this figure. The y-axis is the scattering yield. There are two peaks on each spectrum. The lower energy peak corresponds to the oxygen yield while the higher energy peak represents the silicon. A computer programme was used to integrate the areas under the graph. These areas represent the relative amounts of oxygen and silicon. The results are summarised in the Table 5.1.

These results agree with those obtained via GDS, SIMS and AES. In general the atomic percentage of oxygen increases with increasing film thickness. However, it is only at the lower deposition times that the excess silicon is in reasonable agreement with the average figure predicted by the earlier RBS analysis.

5.3.5 Thickness measurements

Approximate values for film thicknesses were obtained using RBS, AES, ellipsometry Transmission Electron Microscopy (TEM) and Alpha step measurements. TEM is described later in this Chapter and was used to determine the structure of the thinnest SRO films. However, a measurement of film thickness was obtained for films deposited in 0.5 minutes. Only the thickness measurement will be referred to in this section and a fuller discussion of the TEM analysis is given later.

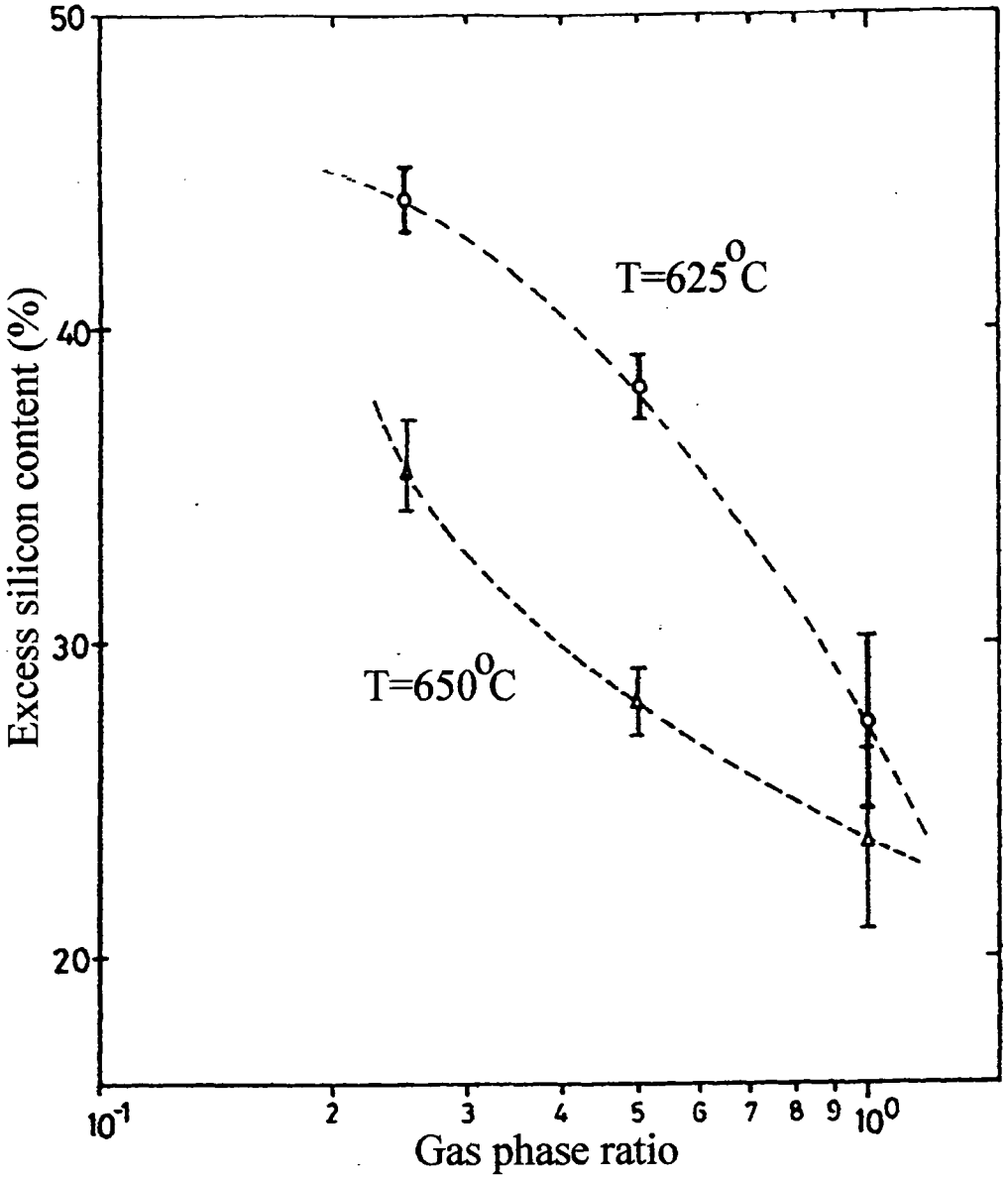

Figure 5.11 Excess silicon content (over stoichiometric silicon dioxide) as a function of the gas phase ratio, γ, for deposition temperatures of 625°C and 650°C by RBS analysis [22].

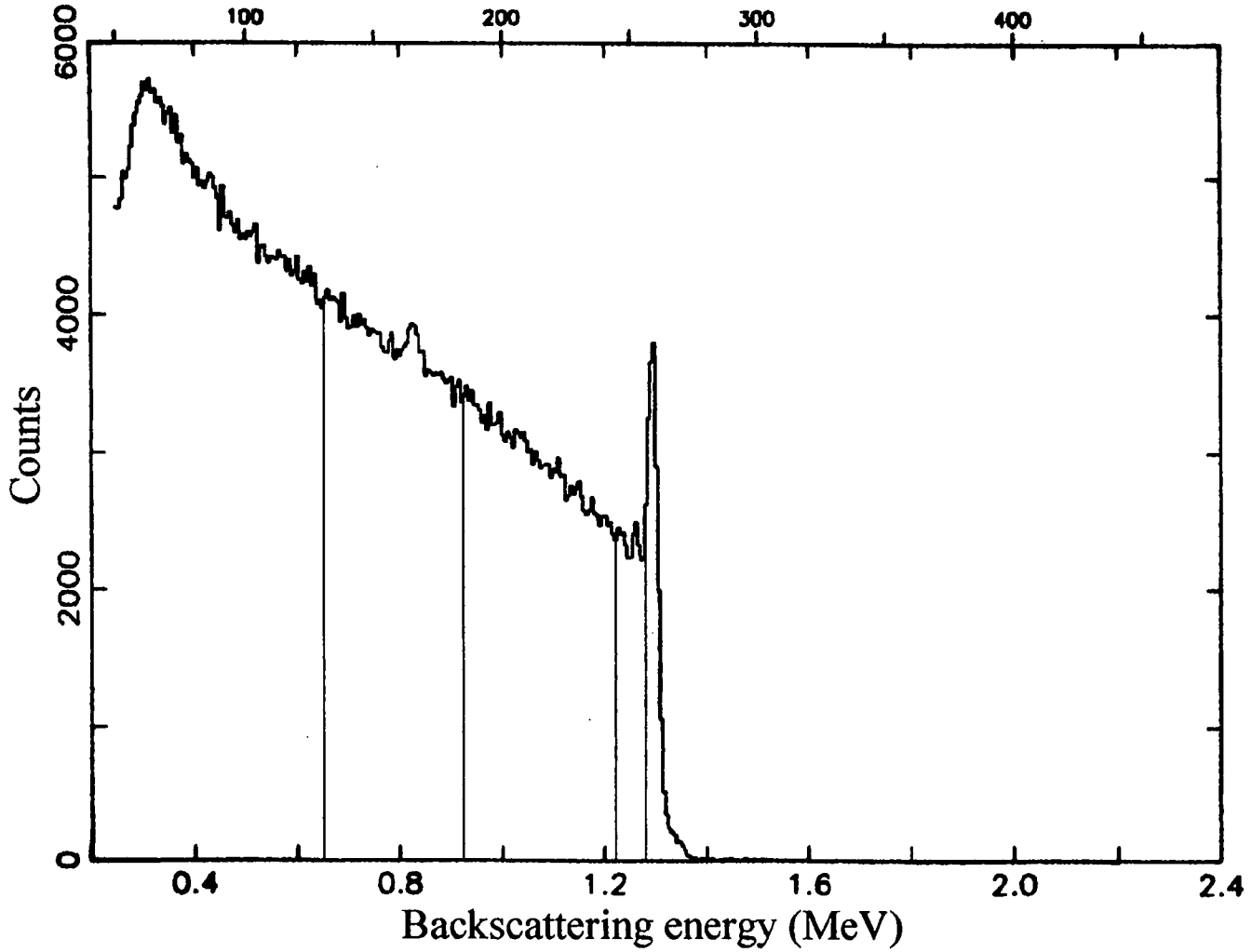

Figure 5.12a Typical RBS spectrum for the elemental analysis of SRO for a deposition time of 1 minute.

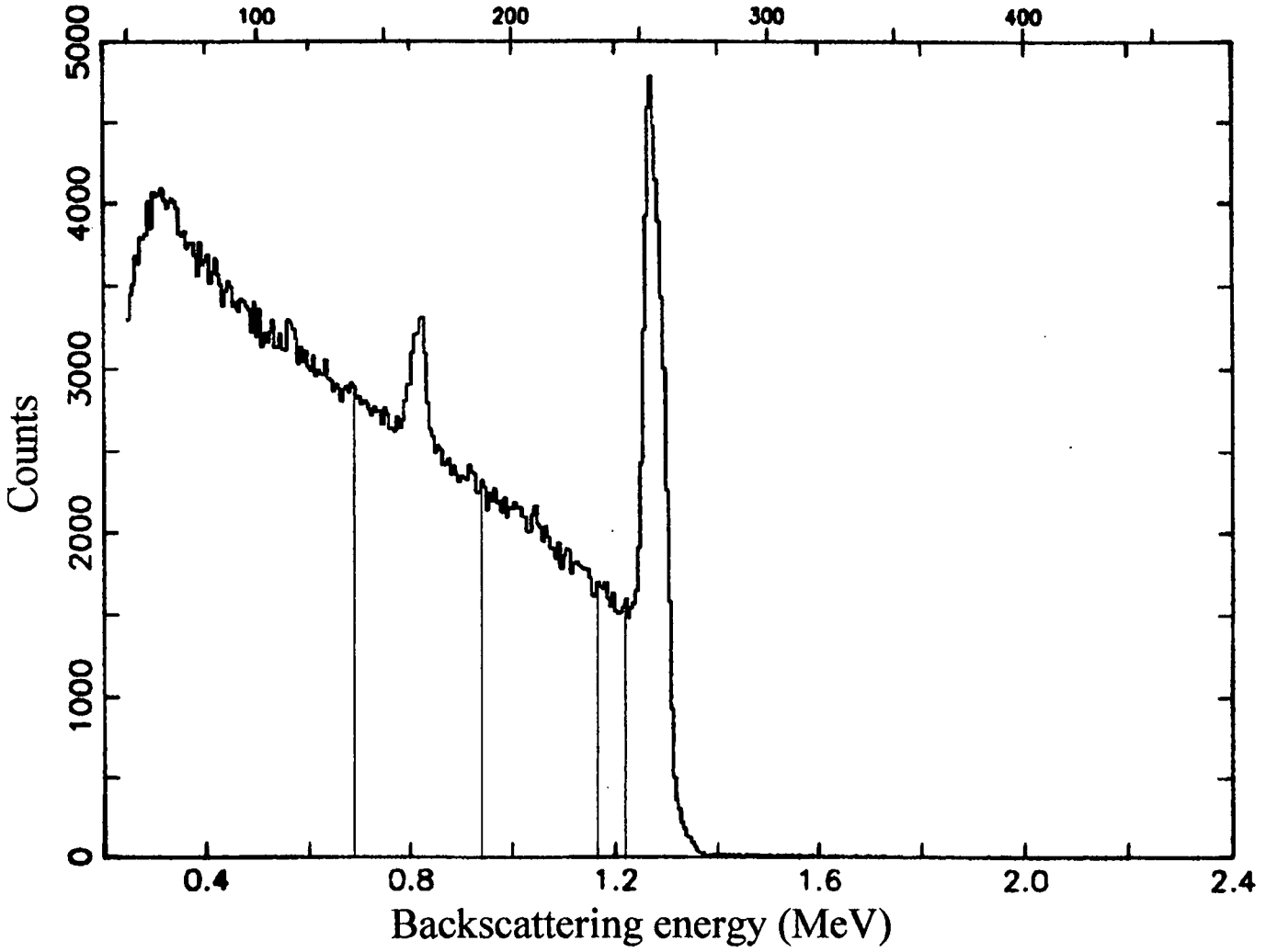

Figure 5.12b Typical RBS spectrum for the elemental analysis of SRO for a deposition time of 1.5 minutes.

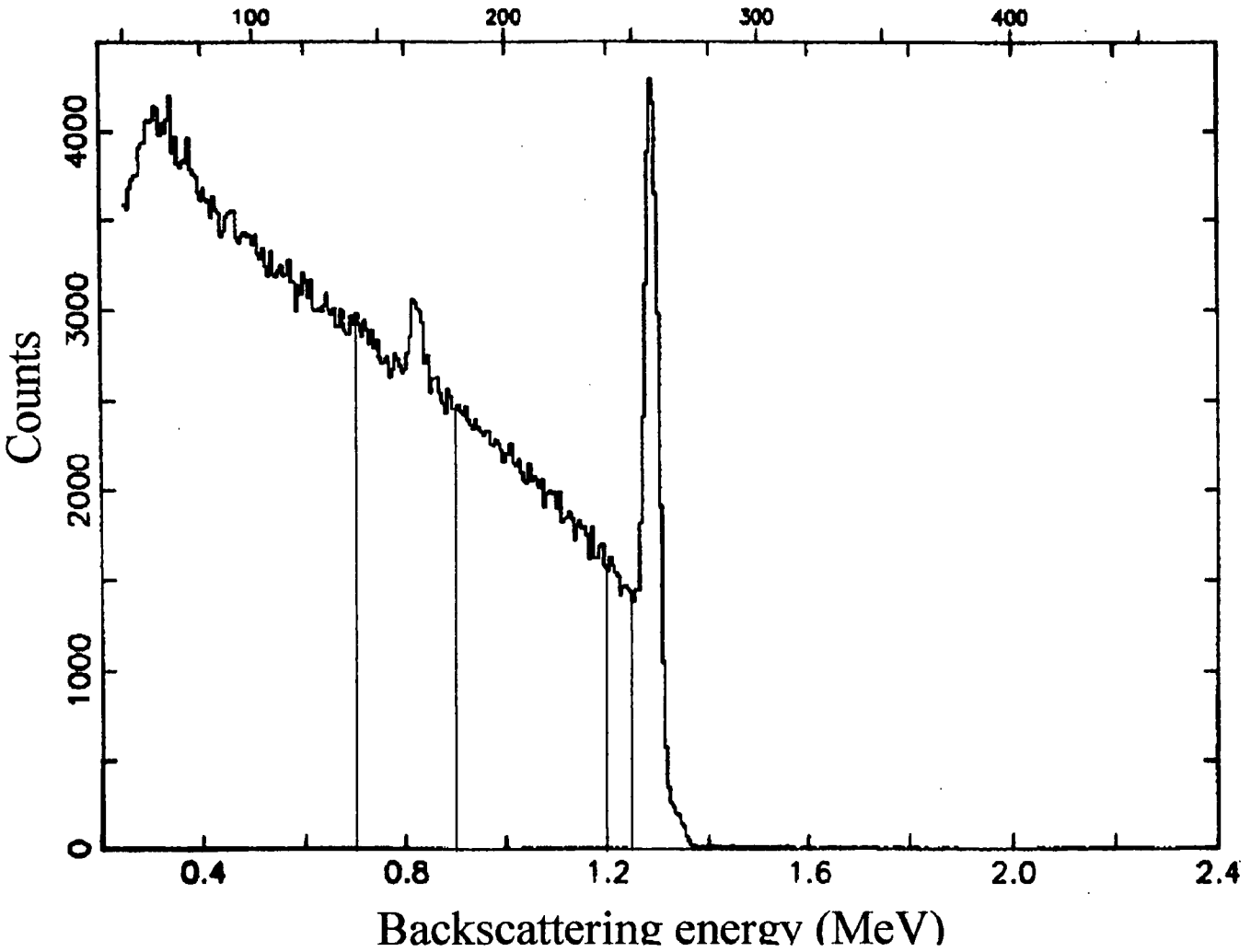

Figure 5.12c Typical RBS spectrum for the elemental deposition of SRO for a deposition time of 2 minutes.

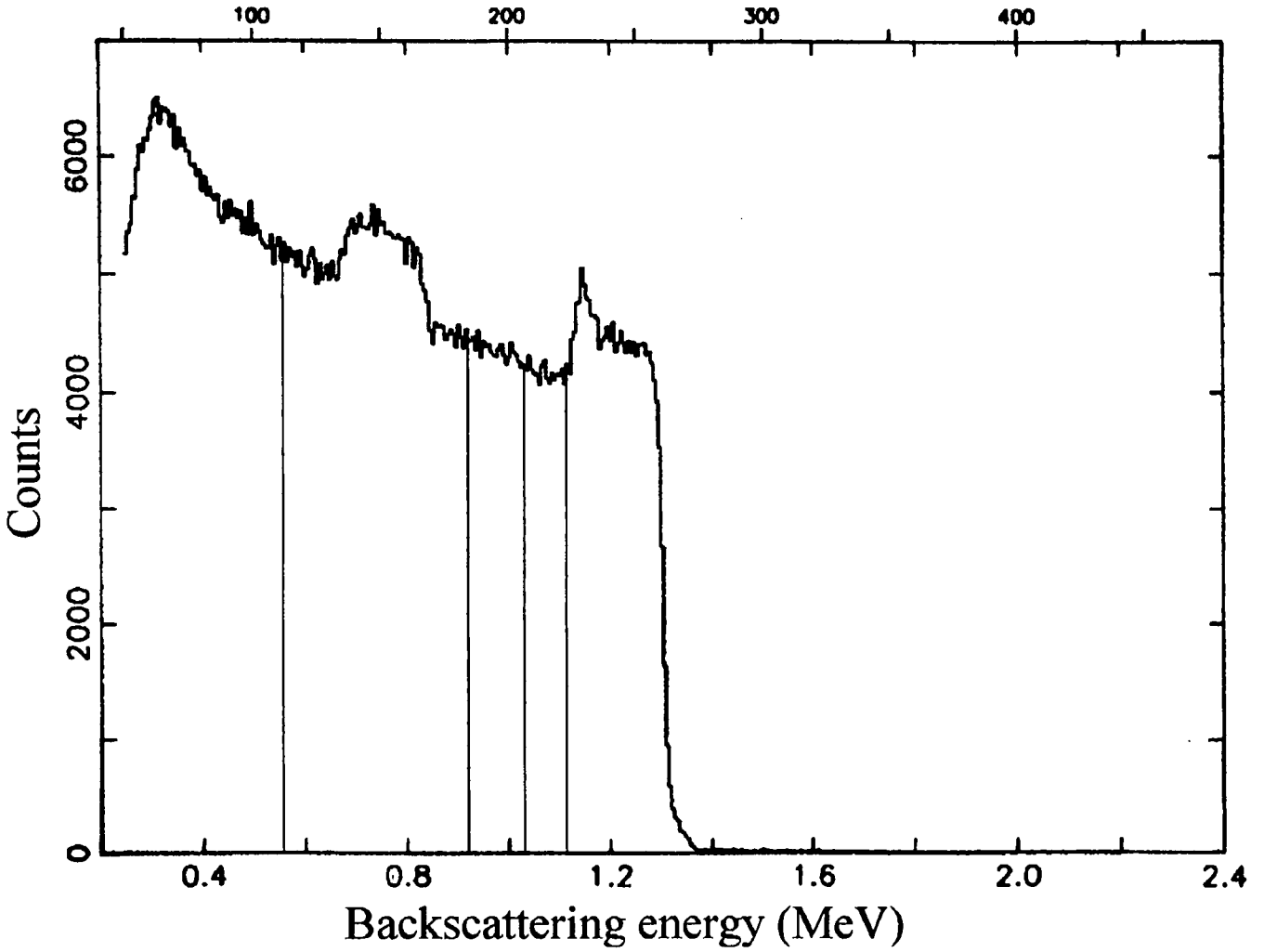

Figure 5.12d Typical RBS spectrum for the elemental analysis of SRO for a deposition time of 4 minutes.

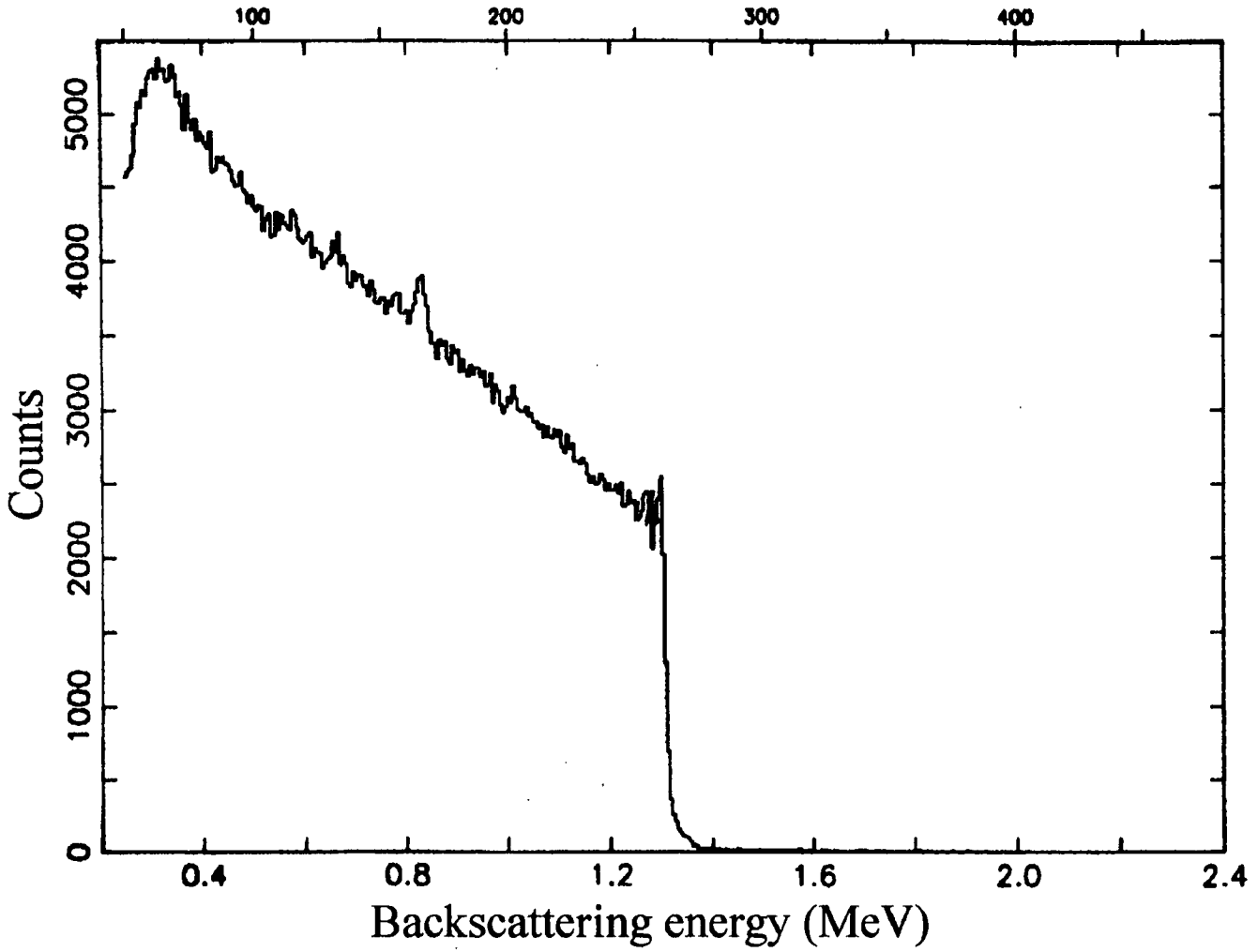

Figure 5.12e Typical RBS spectrum for the elemental analysis of SRO for a deposition time of 8 minutes.

Deposition time (minutes)	Average layer thickness (nm)	Standard error ($\pm$ nm)
1	88	10
1.5	158	30
2	273	30
4	728	240

Table 5.2 Measurement of thickness using RBS

RBS

An indication of film thickness can be obtained from RBS measurements and the results are shown in Table 5.2. The film thickness obtained from the RBS analysis gives an order of magnitude measure. Table 5.2 shows how the SRO film thickness varied with the deposition time. These estimates of film thickness were based upon standard atomic densities for oxygen and silicon. Samples containing a high concentration of silicon would have had atomic densities closest to the assumed values. As the oxygen concentration increased, the inaccuracy in the atomic density would have also increased. These results are later compared with those obtained by ellipsometry and by use of the Alpha step. There is some inaccuracy in the RBS results due to assumptions made about the atomic density and therefore spacing of the silicon and oxygen atoms.

Nulling ellipsometry

The process and apparatus for this measurement of thickness and refractive index have been described in detail in Chapter 4. The SRO samples proved to be non-ideal specimens for this system whose limitations are described below.

With some samples a 'null' could not be found and therefore no measurement was possible. This may be due to the refractive index being very different from that of the standard SiO_2 [22]. For the other samples, the nature of the SRO film itself could have caused inaccuracies since the analysis assumes a simple 2-layer model in which the layers are flat and homogeneous. It is thought that neither of these two conditions are true for SRO films deposited on silicon and therefore approximate values of film thickness have been obtained. The results of using ellipsometry to determine the film thickness for various deposition times are shown in Table 5.3.

The Alpha step was used in an attempt to confirm these results.

Deposition time (minutes)	Mean thickness (nm)	Standard error ± nm
0.5	25.8	0.24
1.0	63.9	0.06
1.5	196.5	9.0
2.0	427.1	0.8
2.5	567.1	2.5
4.0	633.9	8.0
8.0	653.8	8.5

Table 5.3 Film thickness for various deposition times determined with ellipsometry

Alpha step

An Alpha step measures relative height differences by moving a stylus across a sample. Test wafers used in the ellipsometry measurements were also used for Alpha step analysis. A mechanical mask covered the test wafers during SRO processing in the hope of providing a suitable step for film thickness measurements. The mechanical mask was necessary since other methods, e.g. photolithography, were thought to cause contamination of the film or CVD reactor. Unfortunately, the wafer had become concave during processing (apparently this is quite common and is caused by the SRO inducing stress in the silicon wafer) [23]. This stress is caused by the different rates of thermal expansion of the silicon wafer and the oxide layer. The concave shape coupled with the **gradual** rather than abrupt film profile made Alpha step measurements difficult on many samples.

An attempt was made to pattern the test wafers using standard photolithographic techniques. Buffered hydrofluoric acid was used as an etch, but since the films were very silicon-rich, the etches were generally unsuccessful. Some samples were etched in a solution 2:1:1:2 acetic acid:nitric acid:hydrofluoric acid:water. Both etches removed the silicon-rich oxide but also attacked silicon so that it was difficult to tell when the etch had finished and the etching of the substrate had started. Two typical step plots are shown in Figures 5.13 and 5.14. An approximate set of values for film thicknesses was obtained and these are tabulated in Table 5.4.

The above methods were used to obtain an order of magnitude for film thickness for a range of deposition times. For example, consider test samples which have an SRO layer deposited in 1.5 minutes. Referring to tables 5.2, 5.3 and 5.4, ellipsometry gave an average thickness of 196 nm, RBS gave an average of 273nm and Alpha step

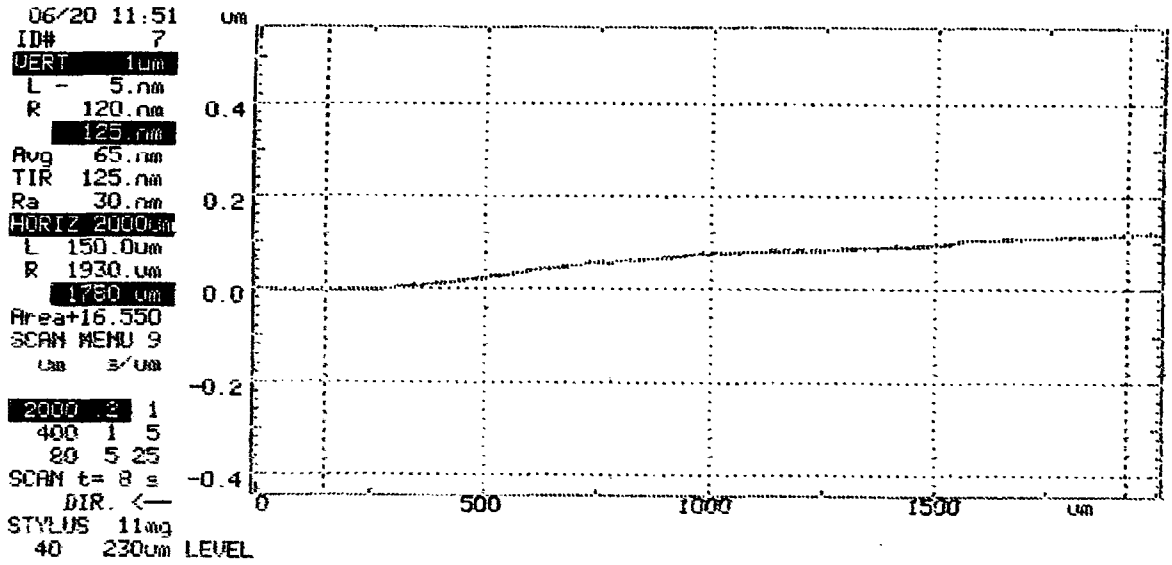

Figure 5.13 Alpha step measurement of SRO film thickness deposited in 1 minute at 650°C and $\gamma = 0.22$.

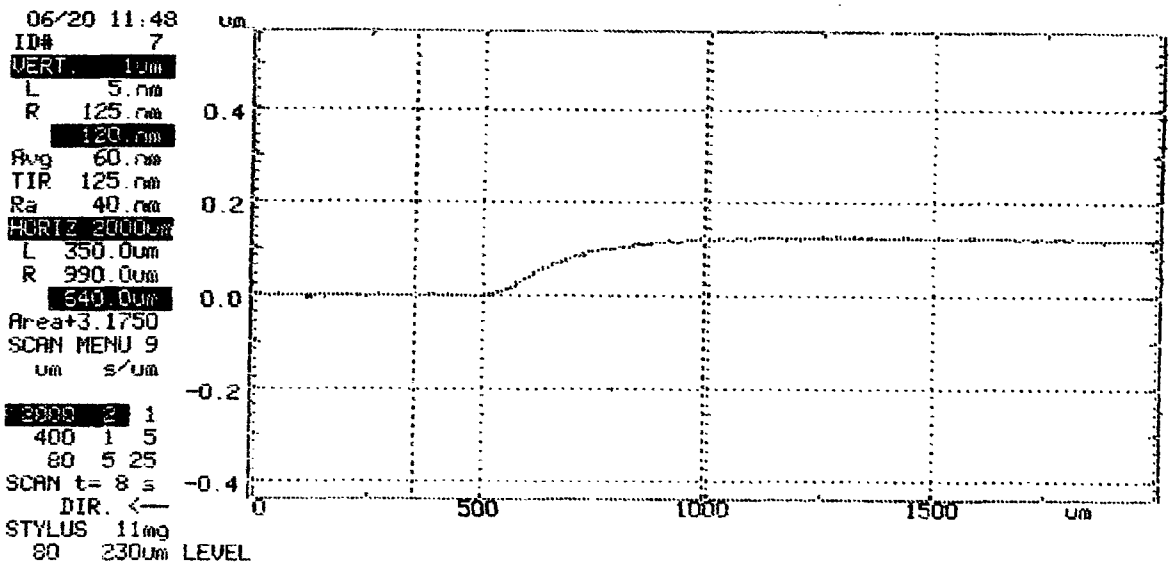

Figure 5.14 Alpha step measurement of SRO film thickness deposited in 1.5 minutes at 650°C and $\gamma = 0.22$

Deposition time (min)	Average thickness (nm)	Standard error (± nm)
0.5	58	7.5
1.0	141	70
1.5	164	84
2.0	177	35
2.5	200	19
4.0	173	45
8.0	275	63

Table 5.4 Film thickness for various deposition times as determined by the Alpha step

readings were averaged at 164nm for such films. AES studies indicated that these films were thicker, with a depth of at least 250 nm, perhaps as much as 300 nm. It should be noted that the AES measurements were performed much later. The lapse in time may have caused a growth of silicon dioxide to form on top of the SRO film but this is likely to be only 1–2 nm at room temperature [18]. TEM analysis was used to determine the thickness of the thinnest SRO films. Figure 5.21 shows that the film grew to a depth of 77 nm in 0.5 minutes. Again, this method yielded larger film depths than those obtained from ellipsometry. Water may be absorbed by SRO films as they age and this could account for the higher values of film thickness obtained from AES, TEM and RBS experiments [24]. In general, the thickness readings from the ellipsometry, AES and RBS methods are reasonably close but in contrast, the Alpha step measurements for the thickest films are too low. The average Alpha step measurement for the thinnest films was in good agreement with the TEM result. The TEM value is an absolute value which can be obtained from the photograph presented as Figure 5.21. Therefore it would appear that the film thickness is under estimated by ellipsometry. Each method of thickness measurement has limitations. However, ellipsometry gave the best estimate of the film thickness and refractive index, with the lowest values of standard error for the full range of SRO film thicknesses used. The film depths obtained must be used with care since AES, RBS and TEM measurements suggest that the values of film depth are underestimated for the SRO films deposited in 0.5 and 1.0 minute.

Figure 5.15 shows the plot of thickness, as measured using the ellipsometer, against deposition time. The thickness is more or less proportional to deposition time until the maximum is reached at 2.5 minutes. The growth rate then reduces with time. This growth rate is controlled by both the deposition temperature and the reactant

gas flow ratio, γ, described in Chapter 4, section 4.2.7.

Film growth kinetics

At Durham, the growth rate of SRO in the APCVD reactor has been found to increase with increasing γ for values in the range 0–1.5 [2]. In this work, the value of γ used was 0.22. Kragler *et al* [25] used γ in the range 0–0.2 and found, for their LPCVD reactor, as γ increased the deposition rate also increased. Hitchman and Kane [26] used values of γ in the range 0–0.6 and found that, unlike other systems, as γ increased the deposition rate decreased. The effect of γ on growth rate is obviously very specific to a particular reactor.

The reactant gas flow ratio (γ) is usually quoted to enable comparisons of different SRO growth conditions. However, γ is merely the ratio of the reactant gas flow rates and so care must be taken when comparing systems for SRO growth. For example, if the nitrogen flow rate is too high, so that the reactant gases are too diluted, or the silane flow rate is too low, silicon depletion may occur. This would decrease the deposition rate but would not be apparent from the gas flow ratio formula or the value quoted for γ. Silicon depletion may also occur if the wafers are placed too far away from the inlet. The gases may react near the inlet and therefore the concentration of silane decreases with distance along the reactor length.

Hitchman and Kane [26] attempted an explanation for the observed decrease in deposition rate for increasing γ. They proposed that the N_2O was adsorbed onto a disproportionate number of surface sites thus preventing the adsorption of the silicon atoms. Other silicon-rich oxide investigators also support this so-called 'N_2O depletion' model. Chao *et al* [27] found that for their LPCVD system, the growth rate increased initially for increasing γ. For γ values greater than 0.55 excessive N_2O near the wafer surface somehow inhibited silicon adsorption and resulted in low rates of film growth.

For each system there is obviously an optimum gas flow ratio which will maximise film growth. Maximum film growth, however, is not always a priority and could be sacrificed to obtain high quality, uniformly deposited layers. From figure 5.15, the maximum growth rate has been calculated to be approximately 6.7 nm s^{-1}. Assuming that the lattice constant for silicon of 5.43 Å can be used, this growth rate corresponds to approximately 12 monolayers per second. This is possibly an over-estimate but represents a typical value for APCVD reactors. Knolle *et al* [28] calculated that their APCVD reactor deposited 2.5 monolayers per second and compared this to

the deposition rate of 0.16 monolayers per second for their LPCVD reactor. The physical properties of a film are not only dependent upon the oxygen concentration but also on the deposition rate. Such a rapid deposition of atoms must mean that the random bonding applies in APCVD films whereas in films deposited by LPCVD, the bonding tends to create more SiO_2 molecules. The faster deposition rate in the Durham APCVD system might be expected to result in a more disordered film.

Knolle *et al* [28] also conclude that the growth rate, in both APCVD and LPCVD systems, was inversely proportional to the oxygen content. The growth rate for the APCVD reactor used in Durham was calculated from the ellipsometry measurements of film thickness. A plot of growth rate versus deposition time is shown in Figure 5.16. The deposition temperature and gas flows were maintained at constant values. Clearly a constant growth rate does not result. The growth rate increases to a maximum at 1.5 minutes and then reduces to zero at 4 minutes. This cannot be simply explained by considering the oxygen content of the films, as proposed by Knolle *et al* [28]. In this work, Auger analysis has shown that the oxygen concentration increased with distance from the silicon substrate. This would suggest that thinner films contain less oxygen and all wafers would have exhibited rapid growth initially. As the deposition time is increased, the growth rate should decrease. This is true up to a point but the growth mechanism appears to be a little more complex than this. A complicated growth mechanism involving the following reactions must be taking place

$$\mathrm{SiH_4(g)} \rightleftharpoons \mathrm{SiH_4(a)} \tag{5.3}$$

$$\mathrm{SiH_4(a)} \rightleftharpoons \mathrm{Si(a) + 2H_2(g)} \tag{5.4}$$

$$\mathrm{SiH_4(g)} \rightleftharpoons \mathrm{SiH_2(a) + H_2(g)} \tag{5.5}$$

$$\mathrm{H_2(g)} \rightleftharpoons \mathrm{H_2(a)} \tag{5.6}$$

$$\mathrm{N_2O(g)} \rightleftharpoons \mathrm{N_2O(a)} \tag{5.7}$$

$$\mathrm{N_2O(a)} \rightleftharpoons \mathrm{N_2(g) + O(a)} \tag{5.8}$$

$$\mathrm{Si(a) + }x\mathrm{N_2O(a)} \rightleftharpoons \mathrm{SiO}_x\mathrm{(a) + }x\mathrm{N_2(g)} \tag{5.9}$$

where (g) indicates the gaseous phase and (a) indicates adsorption on the film surface. These reactions compete for lattice sites on the wafer surface.

The AES studies support the idea of silicon and oxygen competing for lattice sites. Figure 5.17 shows the comparison between the percentage composition of oxygen and silicon. These two curves are a mirror image of each other, suggesting that there is a

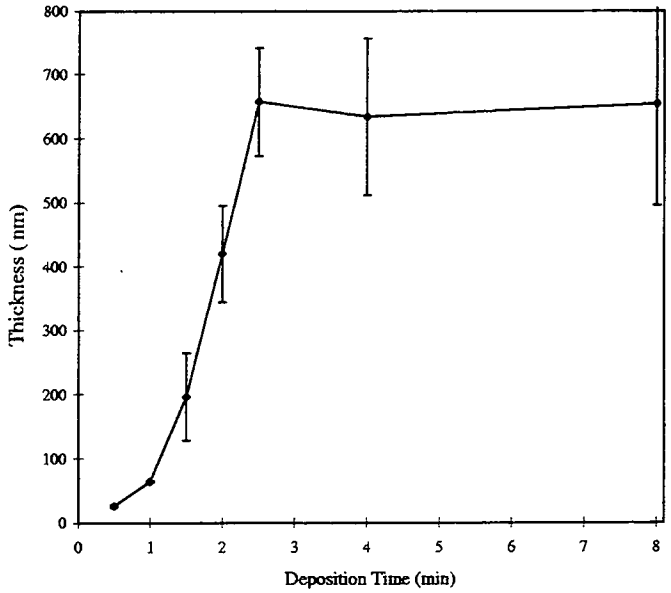

Figure 5.15 SRO Film thickness as function of deposition time for $\gamma = 0.22$ at 650 °C.

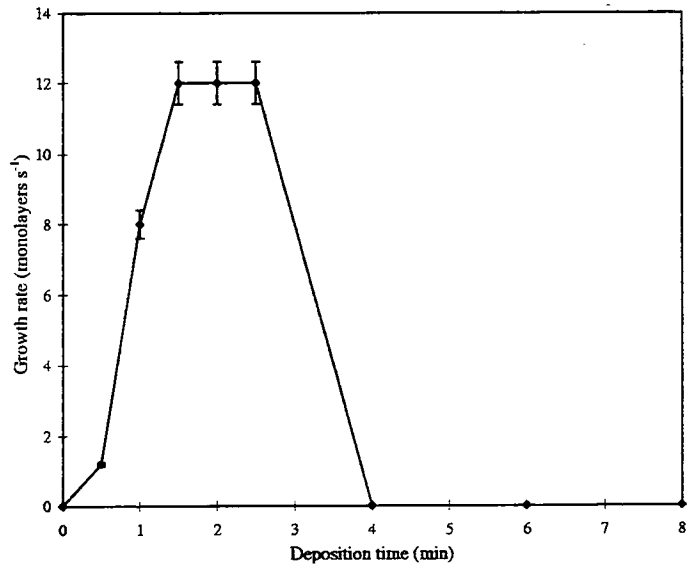

Figure 5.16 Growth rate of SRO as a function of deposition time for $\gamma = 0.22$ at 650 °C.

fixed number of sites available to the silicon and oxygen atoms.

The GDS, AES and SIMS spectroscopy methods show the highest concentration of silicon at the wafer surface and a decrease in silicon content as the SRO layer grows. This suggests that the APCVD reactor must initially favour silicon deposition and then oxygen deposition. The gases were switched from vent mode to the chamber simultaneously. The first gas to arrive at the wafer would have been N_2O. This was because of the construction of the reactor. N_2O oxidises silicon very slowly i.e. at a rate of $< 0.1\,\mathrm{nm\,min^{-1}}$ at the deposition temperature used for this work [18]. In less than a second, the nitrogen carrier gas and silane would have arrived. The wafer would have been at its hottest at this point. Perhaps the hotter temperature would have favoured reactions 5.1–5.3. Certainly, reactions 5.1–5.3 take place via pyrolysis. This would have caused a higher concentration of silicon to have been deposited.

The wafer was heated from below. As the film grew the surface would have become cooler due to the constant flow of cold gases. Most modern CVD reactors heat the gases prior to entry to the reaction chamber. The cooler surface temperature may have favoured the reactions 5.5, 5.6 and 5.7. This would have increased the oxygen content of the film with distance from the substrate. It should also be noted that Si–O bonds are more energetically favourable than Si–Si bonds at the temperatures involved and therefore are more likely to form [10]. As the deposition time increased, it is proposed that more and more sites become occupied by N_2O until the growth rate becomes minimal.

Refractive index

The ellipsometry results for refractive index, assuming a non-absorbing sample, are plotted in Figure 5.18 and tabulated in Table 5.5. Silicon has a high refractive index of 3.5 and silicon dioxide a lower value of 1.46. The refractive index of the SRO films was expected to follow the average percentage of silicon present in the films. GDS, AES and SIMS analyses predicted a high value for the refractive index of thinner SRO films since they are very silicon-rich and a lower value for thicker films since they contain more oxygen. This trend was not apparent from the ellipsometry results detailed in Table 5.5 and in Figure 5.18. As the deposition time increased the refractive index increased. This could have been explained by the fact that increased deposition time would have caused thicker films to be grown. Thicker films would be more absorbing and would affect the incident light more. However, the effect cannot only be due to film thickness since the plot shows an unexpected

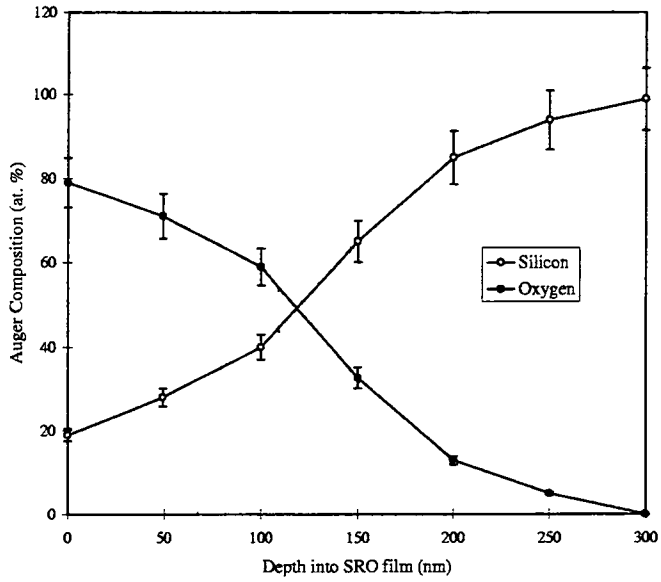

Figure 5.17 A comparison of the percentages of oxygen and silicon within an SRO film, as a function of depth

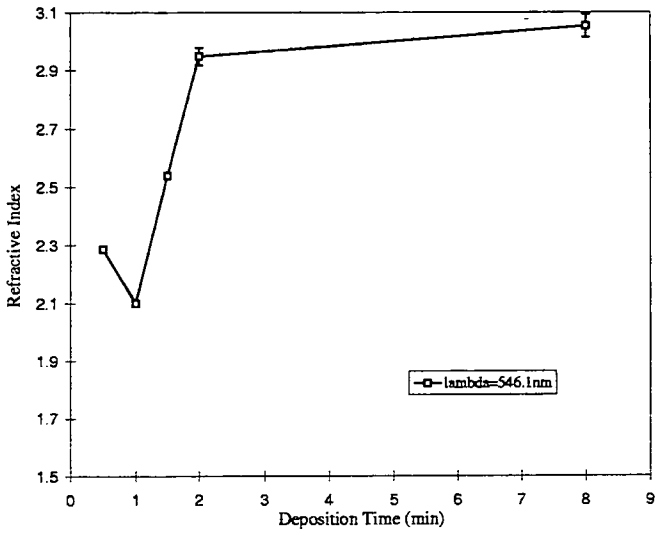

Figure 5.18 Refractive index as a function of deposition time for $\gamma = 0.22$ at 650 °C.

Deposition time	Refractive Index (standard error)		
(minutes)	λ=546.1 nm	λ=632.8 nm	λ=405.0 nm
0.5	2.286±0.01	2.308±0.18	2.716±0.004
1.0	2.1±0.01	2.00±0.02	2.849±0.01
1.5	2.54±0.01	2.254±0.035	3.13±0.12
2.0	2.949±0.03	2.633±0.026	3.545±0.035
2.5	2.16±0.01	2.285±0.03	2.98±0.02
4.0		2.69±0.03	3.34±0.015
8.0	3.053±0.035	2.685±0.027	3.31±0.155

Table 5.5 Film refractive indices at three wavelengths

dip in refractive index at a deposition time of 1.0 minute. For longer deposition times of 4–8 minutes, the refractive index is approximately constant. Ellipsometric analysis suggests that the average silicon content of the films increased to a maximum value at 2 minutes. A fairly constant film composition was then obtained which was independent of deposition time.

This trend does not agree with the three independent compositional analyses GDS, AES and SIMS. A comparison of Figures 5.17 and 5.18 highlight the discrepancy between the ellipsometry results and those of the other spectroscopic techniques. The problems associated with applying ellipsometry to an inhomogenous film, deposited on a concave substrate, very unlike the standard silicon dioxide in that the films may have contained so much silicon that they were too absorbing, could account for the discrepancy in the predicted and measured refractive index values. The GDS, AES and SIMS results were assumed to be accurate for compositional analysis and the refractive indices, obtained by ellipsometric measurements were averaged and used as an estimate of the refractive index for SRO.

The ellipsometry results were compared to the AES results using the films grown in 1.5 minutes. Ellipsometry gave an average refractive index of 2.586. The average atomic percentage of oxygen was estimated from the AES plots and was used to estimate the apparent dielectric constant of the silicon-rich oxide films. From this result the refractive index was calculated and compared with the result obtained from ellipsometry.

Hseih and Greve [6] used the Bruggeman effective medium approximation [29] to estimate the percentage of oxygen in their films. An annealed film with a volume

fraction x of SiO_2 has an apparent dielectric constant ϵ_a, which satisfies the equation

$$x\frac{\epsilon_{SiO_2}-\epsilon_a}{\epsilon_{SiO_2}+2\epsilon_a}+(1-x)\frac{\epsilon_{Si}-\epsilon_a}{\epsilon_{Si}+2\epsilon_a}=0 \tag{5.10}$$

where ϵ_{SiO_2} and ϵ_{Si} are the dielectric constants of silicon dioxide and silicon and have the values 3.9 and 11.9, respectively. The number of molecules of SiO_2 in the film is given by

$$x\frac{\rho_{SiO_2}}{W_{SiO_2}} \tag{5.11}$$

and the number of atoms of Si is given by

$$(1-x)\frac{\rho_{Si}}{W_{Si}} \tag{5.12}$$

where ρ_{SiO_2} and ρ_{Si} are the mass densities and W_{SiO_2} and W_{Si} are the atomic weights of silicon dioxide and silicon, respectively.

The atomic percentage of oxygen is related to the volume fraction x by

$$\begin{aligned}\%\text{ atomic oxygen} &= \frac{2x\frac{\rho_{SiO_2}}{W_{SiO_2}}}{3x\frac{\rho_{SiO_2}}{W_{SiO_2}}+(1-x)\frac{\rho_{Si}}{W_{Si}}} \\ &= \frac{2x}{3x+F(1-x)} \qquad (5.13)\end{aligned}$$

(5.14)

where $F=(\frac{\rho_{Si}}{W_{Si}})(\frac{W_{SiO_2}}{\rho_{SiO_2}})=2.26$.

In using this equation, Hseih and Greve assumed that their films consisted of only silicon and silicon dioxide. This assumption is justified since their films were annealed in nitrogen which changed the structure to a mixture of silicon microcrystals and silicon dioxide. This is not the case for the as-deposited films used in this work. However, this method is only used as rough guide to the accuracy of the ellipsometry results.

An estimate of the average atomic percentage of oxygen taken from the AES plot was found to be 37%. This was then used in equation (5.13) to obtain the volume fraction of silicon dioxide. A figure of 0.4844 was calculated and then used in equation(5.10) to obtain an apparent dielectric constant of 7.29. If it is assumed that the dielectric constant is equal to the refractive index squared then the refractive

index is 2.7. which compares favourably with the average of 2.586 obtained from the ellipsometry measurements. The dependence on ellipsometer wavelength was not investigated. Only the refractive index at a wavelength of 546.1 nm was considered. Many approximations were made in the determination of the two refractive indices. Therefore this analysis is only an indication that these independent methods give similar results. It was necessary to acquire independent confirmation of thickness and refractive index from additional techniques.

5.3.6 Structural analysis

Scanning electron microscopy

The Scanning Electron Microscopy (SEM) technique was described in Chapter 4. The results are presented in Figures 5.19 and 5.20. These photographs are of the thinnest films, i.e. those grown in a time of 0.5 minutes. It was not possible to obtain structural evidence for thicker films. Smooth featureless photographs were observed for all but the unannealed thinnest films.

Thin film deposition shows a mosaic pattern. There are large dark areas surrounded by a mottled lighter background. Some of these areas appear to have coalesced. Such photographs represent the initial deposition of SRO. The film may not be continuous and it is postulated that the dark areas are silicon islands or columns. Gas film nucleation causes deposition of $Si - Si_x$ [18] crystallites which could be of a similar size to those areas observed on the photographs [18]. Upon annealing, these islands disappear and a smooth featureless layer results. This could be due to the unwanted presence of oxygen in the nitrogen annealing furnaces which caused the oxidation of the silicon. Alternatively, it could be due to the coalescence of the grains at the elevated temperature of 1000 °C causing the layer to appear more even. The latter is more likely since these test wafers have been exposed to air and have not become even in appearance.

Dipping the film in hydrofluoric acid for 10 seconds revealed that the structure remained relatively unchanged reinforcing the idea that these larger areas were silicon. Also, it should be noted that the granular structure was observed at points of imperfection on the silicon surface and this is where film development is likely to begin.

Thicker films show no granular structure and present a uniform appearance from one minute deposition times upwards. This was probably due to the decrease in size of the silicon islands towards a more uniform Si-O matrix.

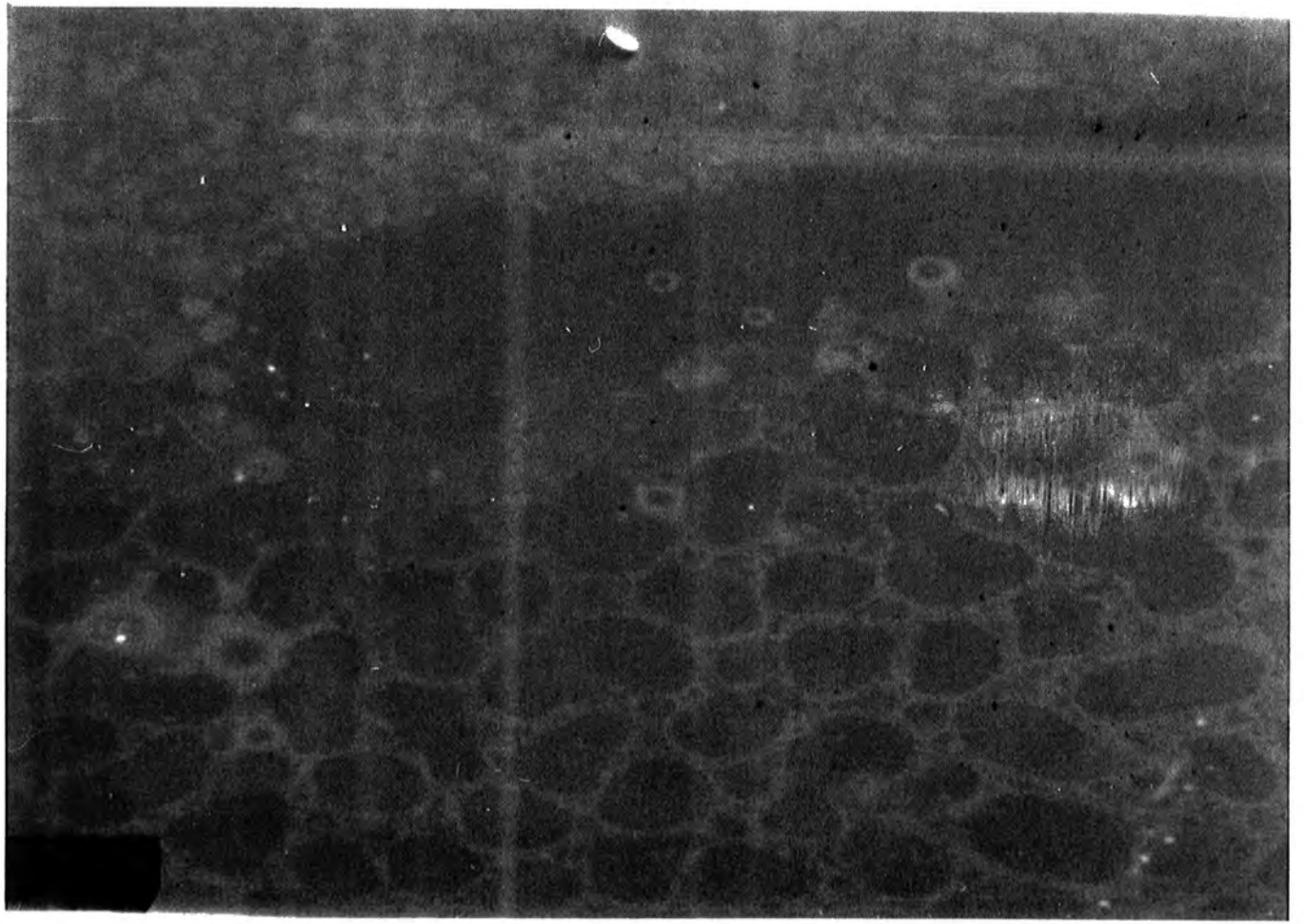

Figure 5.19 Scanning electron microscope (SEM) photograph of a thin SRO film of 0.5 min deposition time and $\gamma = 0.22$ at 650 °C.

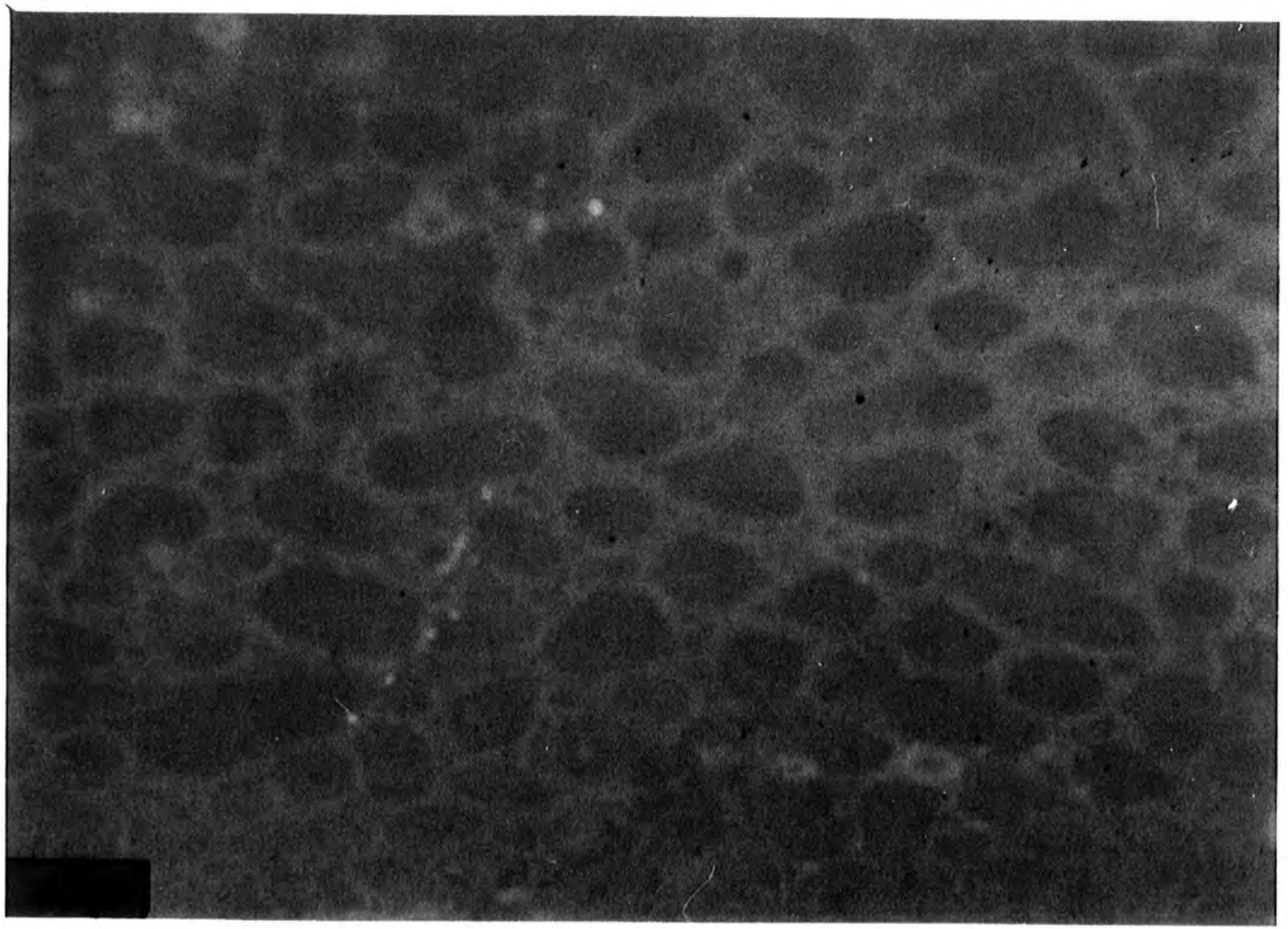

Figure 5.20 Scanning electron microscope (SEM) photograph of a thin SRO film of 0.5 min deposition time and $\gamma = 0.22$ at 650 °C.

Transmission electron microscopy

This technique and its sample preparation processes were described in Chapter 4. The results of Transmission Electron Microscopy (TEM) studies are shown in Figures 5.21 and 5.22. Again, TEM studies were limited to the thinnest samples only, i.e. those deposited in 0.5 minutes. This restriction is imposed by the TEM process. Referring to Figure 5.21, the paler layer is the SiO_x layer. The silicon substrate is the dark area underneath. Interestingly, Figure 5.21 shows an interfacial layer between the SRO film and the substrate. This could be a silicon oxide or silicon dioxide layer as postulated earlier. The columnar structure postulated from earlier SEM work was confirmed by TEM analysis, as shown by Figure 5.22. There are columns of what may be silicon growing up from the base of the SRO film. Unfortunately, the expected gradual decrease in width of these columns cannot be observed since thicker films were too opaque for TEM analysis. The mottled appearance of the surrounding matrix is thought to consist of silicon and silicon oxides.

5.3.7 Comparison of results for different techniques

Various research groups have made progress with the composition and structural characterisation of silicon-rich oxides. The growth conditions are critical in determining the exact nature of SRO films. Recent research has concentrated on low pressure chemical vapour deposition (LPCVD). Such reactors are said to produce better quality films, i.e. a better uniformity of film composition and thickness. This is achieved by the slower growth rates for the same gas flow rates and deposition temperatures as those used in an APCVD reactor. Early research indicated that APCVD films were very non-uniform across the wafer and even gave concentric rings of various colours. These resulted from film thickness variations. The films grown at Durham have shown a slight variation in film thickness across the wafer, typically, 5–6% [30] (from ellipsometry). All films produced at Durham had a smooth, even-coloured appearance. Uniformity would have been enhanced by the fact that the wafers were always placed in the reactor in the same position on the susceptor and this was at the point of minimum turbulence. This is not economical and early research, which showed non-uniform results, placed several wafers in quartz boats at right angles to the gas flow to gain commercial viability. LPCVD reactors overcame this problem. The lower growth rate not only caused more oxygen to be incorporated into the films [4] but also affected the way the oxygen bonded within the film [3, 31]. LPCVD films tend to have more SiO_2 whereas APCVD films contain more incomplete SiO_2

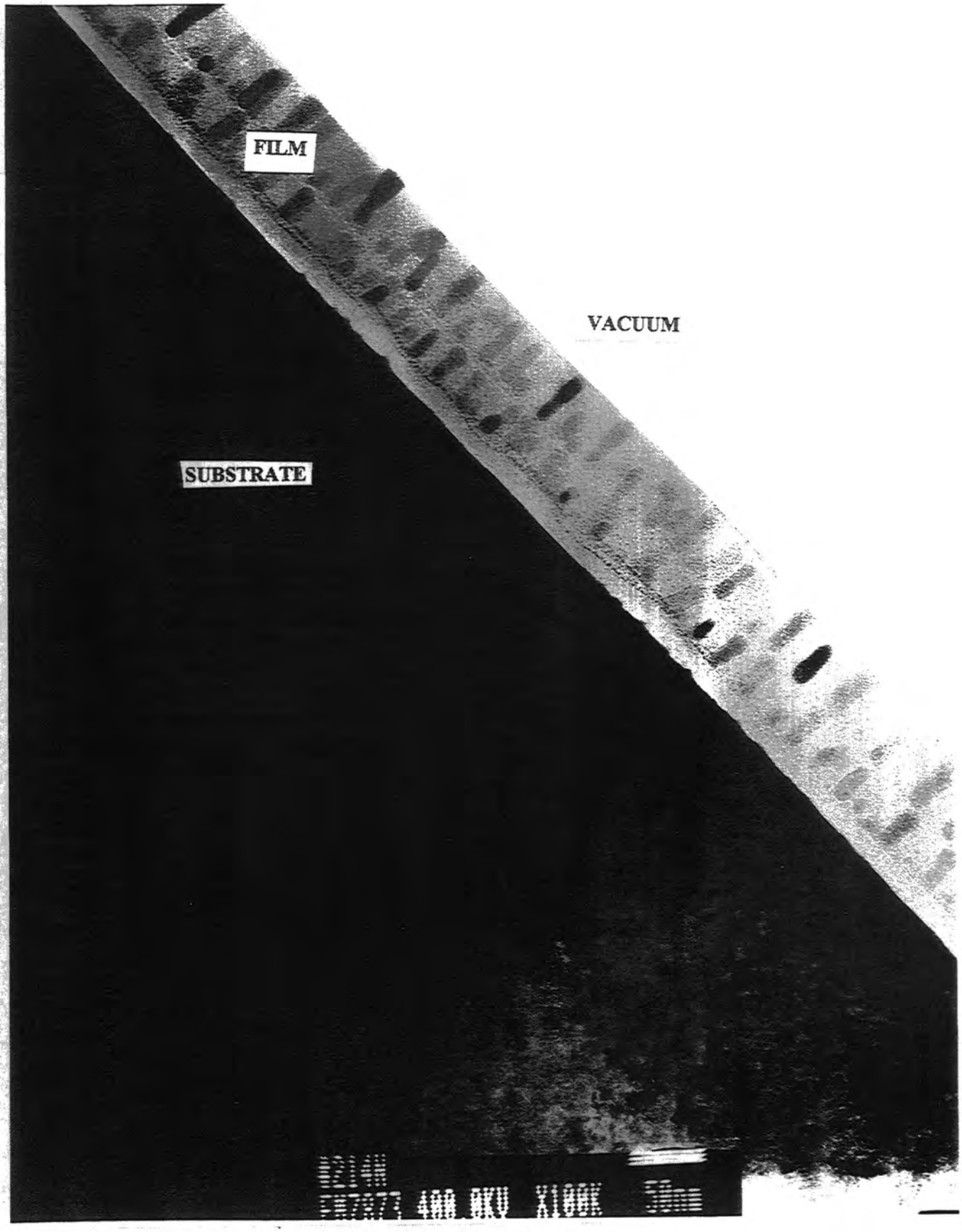

Figure 5.21 Transmission electron microscope (TEM) photograph of a thin SRO film of 0.5 min deposition time and $\gamma = 0.22$ at 650 °C. As for Figure 5.22 but greater magnification

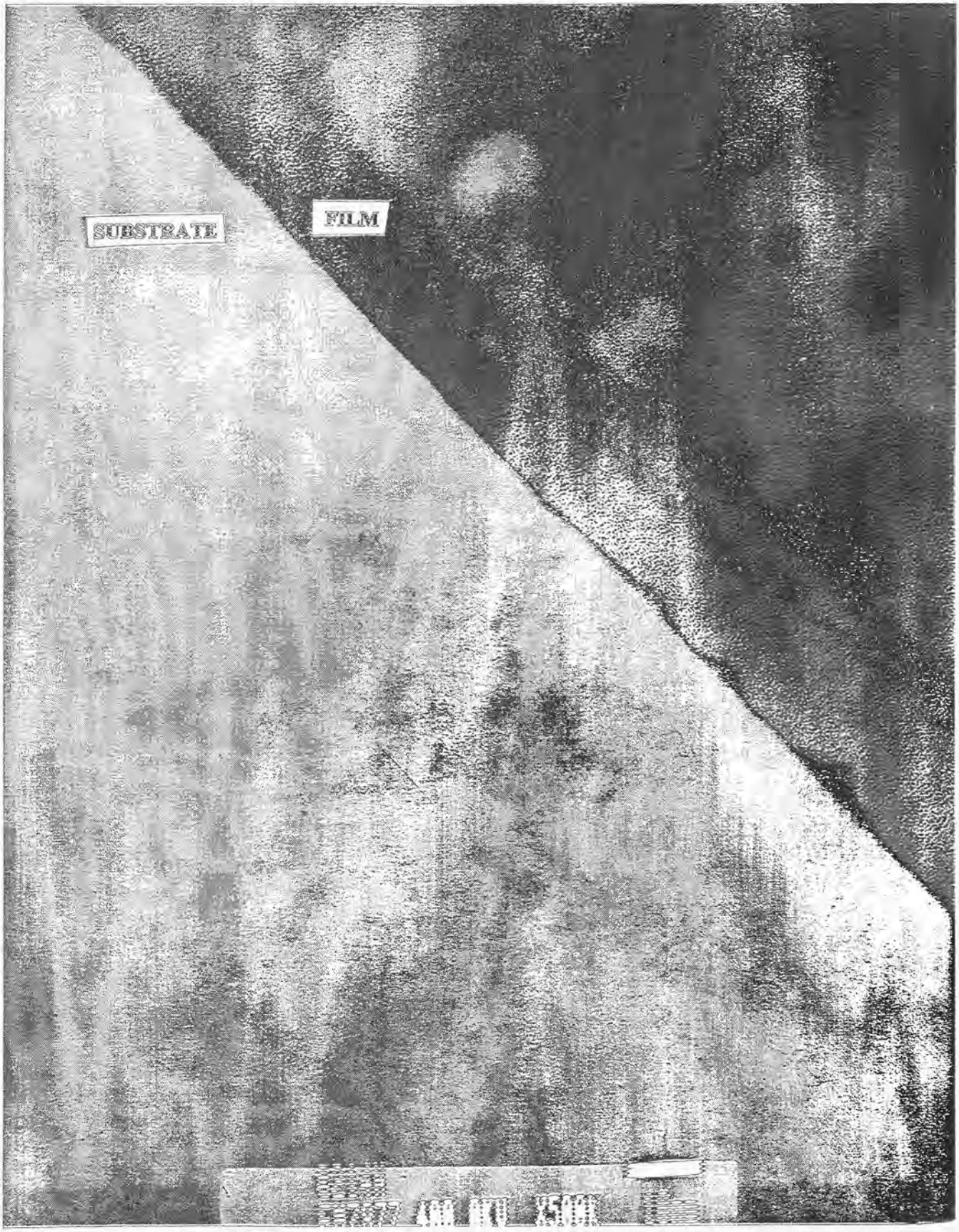

Figure 5.22 Transmission electron microscope (TEM) photograph of a thin SRO film of 0.5 min deposition time and $\gamma = 0.22$ at 650 °C. As for Figure 5.21 but greater magnification

tetrahedra. Plasma enhanced CVD (PECVD) reactors provide good uniformity of films at lower deposition temperatures than the other two methods. The lower temperature changes the growth kinetics and therefore the structure and composition of the films produced [32]. The different growth conditions make it difficult to transfer information learnt about SRO films in one system to another. Much information about the composition of the films grown in the APCVD reactor in Durham has been given by GDS, SIMS and AES analysis. All gave similar results. There was a gradual compositional change, a decreased silicon content and increased oxygen content towards the film-gas interface. The SIMS technique went a step further and sub-divided the film into three regions:

(i) a 'native oxide' layer;

(ii) a silicon-rich region near the substrate; and

(iii) an oxygen-rich region.

The AES studies gave more detail about the actual percentages of the film components at various depths. Figure 5.10 summarised the total atomic percentage of silicon and oxygen throughout the film. The relative percentages of silicon and oxygen are extremely important in determining the film structure. The macrostructure of the film is thought to have three main regions:

(i) an SiO_x layer at the film-substrate interface;

(ii) the SRO film of varying composition; and

(iii) a surface layer of silicon dioxide at the film-gas interface.

Each of these regions will be discussed below.

The film-gas interface

Hseih and Greve [6] observed the selected area diffraction (SAD) pattern using TEM for as deposited silicon-rich oxide and also for the same films annealed in dry oxygen at 1000 ° C. The SAD patterns for the as-deposited films were characteristic of amorphous solids. After the oxidation process, the SAD pattern was identical to that of silicon dioxide. Widmer and Hitchman [33] fully oxidised the silicon-rich oxide and used a differential thickness measurement to determine its oxygen content. The oxidation process breaks the Si-Si bonds and forms Si-O-Si bonds which was confirmed

by a decrease and an increase in the Auger line strength of the former and latter species, respectively [6].

These experiments suggest that the top layer of the SRO film is likely to be oxidised in air to form SiO_2. This will not be as thick as the 25 nm shown by the Auger process in Figure 5.10 because the test wafers used in this process were exposed to air for much longer than those wafers which were processed as devices.

The film-substrate interface

There has been much debate about the silicon substrate surface and whether or not the interface with its oxide or with silicon-rich oxide is abrupt. There are many workers who support the idea that a transition region of SiO_x exists linking the substrate to its oxide SiO_2 [34]. Harrington *et al* [35] reported the presence of excess silicon at this interface. Offerman *et al* [36] found evidence of a transition region but Feldman *et al* [37], using the same back scattering experiment, suggested that the interface was abrupt, as did DiStefano [38] and Blanc [39]. Catalano *et al* [9] support the theory that native oxides tend to be discontinuous in a nature. They presented TEM photographs that showed localised epitaxial growth of silicon extending from the substrate into the silicon-rich oxide films. These workers subsequently claimed that the silicon-rich oxide-silicon interface is chemically and structurally abrupt. However, Wong *et al* [40] have presented HRTEM photographs showing a definite interfacial layer (2.5–3 nm wide) between the substrate and the SRO film. The latest techniques now enable very thin, defect-free oxides to be grown with an abrupt interface with the silicon wafer [41].

Much depends on how fast the cleaned wafers are processed. In Durham, the cleaned wafers were placed in cold deionised water, dried with a nitrogen gun and placed on a warm susceptor in air. Within seconds the susceptor was returned to the reactor. The deposition chamber was flushed with nitrogen for 10 minutes before the heater was turned on. During this time some 'native oxide' could have been formed as indicated by the SIMS technique and shown in the TEM photographs. The exact nature of this layer is unknown but the literature suggests that it would be non-stoichiometric silicon oxide represented by the formula SiO_x, where $0 < x < 2$. Hollinger and Himpsel [42] discovered that the interface layer on <100> and <111> silicon surfaces was independent of orientation. This is fortunate since the p-type and n-type silicon wafers used in this work were of different orientations.

Composition of SRO

The Auger technique is incapable of detecting hydrogen but, as discussed earlier, it is possible that there is silicon hydride and silicon hydroxide or silanol present in the SRO films. Knolle and Maxwell [31] found that, in their APCVD films, the hydrogen concentration was proportional to the oxygen concentration. Their investigation suggested that the hydrogen was not bonded to oxygen but to silicon, as Si-H. GDS analysis shows a similar trait here. As the oxygen concentration increases, so does the hydrogen concentration. This suggests that the hydrogen is bonded to the oxygen. Silanol is not mentioned in connection with any silicon-rich oxide, in the literature. The SiOH model was put forward in an attempt to explain the high amount of elemental oxygen detected by AES. It is not meant to exclude the possibility of there being SiH in the films.

Many workers have evidence which suggests the presence of suboxides in their films [5, 7, 8, 43, 44]. The predominant oxide was found to be Si_2O_3 with Si_2O also present. There were no SiO or SiO_2 species present in these films. Knolle and Maxwell [28] predicted that less than 1% of silicon-rich oxide would be SiO_2 and that most of the film was amorphous SiO; they did not find any evidence for the presence of the oxides Si_2O_3 and Si_2O.

Catalano *et al* [9] found no evidence for Si_2O_3 and Si_2O but stated that silicon-rich oxide existed as a continuous solid solution of silicon and oxygen. The Auger analysis showed that there was very little ($<$ 10% SiO_2 and $<$ 3% SiO_x) throughout the SRO film. Si_2O_3 and Si_2O were not shown to be present by any of the spectroscopic techniques. SRO is likely to consist of variable quantities of silicon, oxygen and hydrogen in solid solution, similar to the composition proposed by Catalano et al.

5.4 The microstructure of SRO

All of the theoretical models assume a constant ratio of silicon to oxygen throughout the silicon-rich oxide. This is not the case for the SRO films shown here. The film is initially almost entirely silicon with very little oxygen. As the thickness increases, the percentage of oxygen increases. Columnar crystal growth of polycrystalline silicon is expected, similar to that described by Brüesch *et al* [8]. As the thickness of the film increases, the crystalline silicon becomes more amorphous and the columnar structure thins out as the oxygen concentration increases. This is because Si-O bonds are energetically more favourable than Si-Si bonds [4] and as the oxygen concentration

increases the disorder and defects become greater. There are also many voids present in the film [25]. Most research workers agree that as-deposited films are amorphous and that APCVD deposition is so rapid that there is no order to the deposition [44, 24]. Statistics governs the deposition and distribution of the Si-O bonds [28]. With rapid deposition, the atoms are laid down randomly. It should be noted that the excess silicon in the films presented in this work is much greater than most other SRO films reported in the literature. Therefore, the percentage of SiO and SiO_2 in the film is too small to support the theory that there is a matrix of SiO and SiO_2 around silicon grains. The Auger analysis suggests that SiO and SiO_2 are only present in the upper half of the film. There is not enough SiO_2 in the film to support the mosaic model [5] or the shell model [10]. The Brüesch *et al* [8] 'modified shell model' is a possibility but again there is not enough SiO_2 to fully support this structure or even the continuous network model [3]. The three-dimensional network model may apply in the initial growth stages of the film but is too ordered for a structure which is so rapidly deposited. The initial crystalline columnar structure gradually breaks up into grains of amorphous silicon as the oxygen concentration increases. These grains become smaller as the thickness of the film increases. There is no SiO_x or SiO_2 around these grains but instead a random network which contains silicon, oxygen and silanol. Gradually there is an increase in the SiO_2 concentration, which would be non-localised. Catalano's description [9] of a continuous solid solution of silicon and oxygen, a type of silicon dioxide alloy, with some hydrogen present is the closest description of the SRO in the Durham films. Finally, a possible structure for SRO is shown in Figure 5.23.

5.5 Conclusions

In this Chapter, experimental evidence was presented for the physical characterisation of silicon-rich oxide. Various spectroscopy techniques were employed and the typical film composition determined. The films were found to have three regions: some nascent oxide at the silicon interface; an oxide which is extremely silicon-rich at the substrate; and a region of variable composition, becoming nearer the stoichiometric silicon dioxide at the gas-film interface. A suggestion for the elemental bonding within the film was proposed and other film parameters such as film thickness and refractive index were obtained as a function of deposition time. These values were compared with those obtained from ellipsometry and Alpha step measurements. Film growth

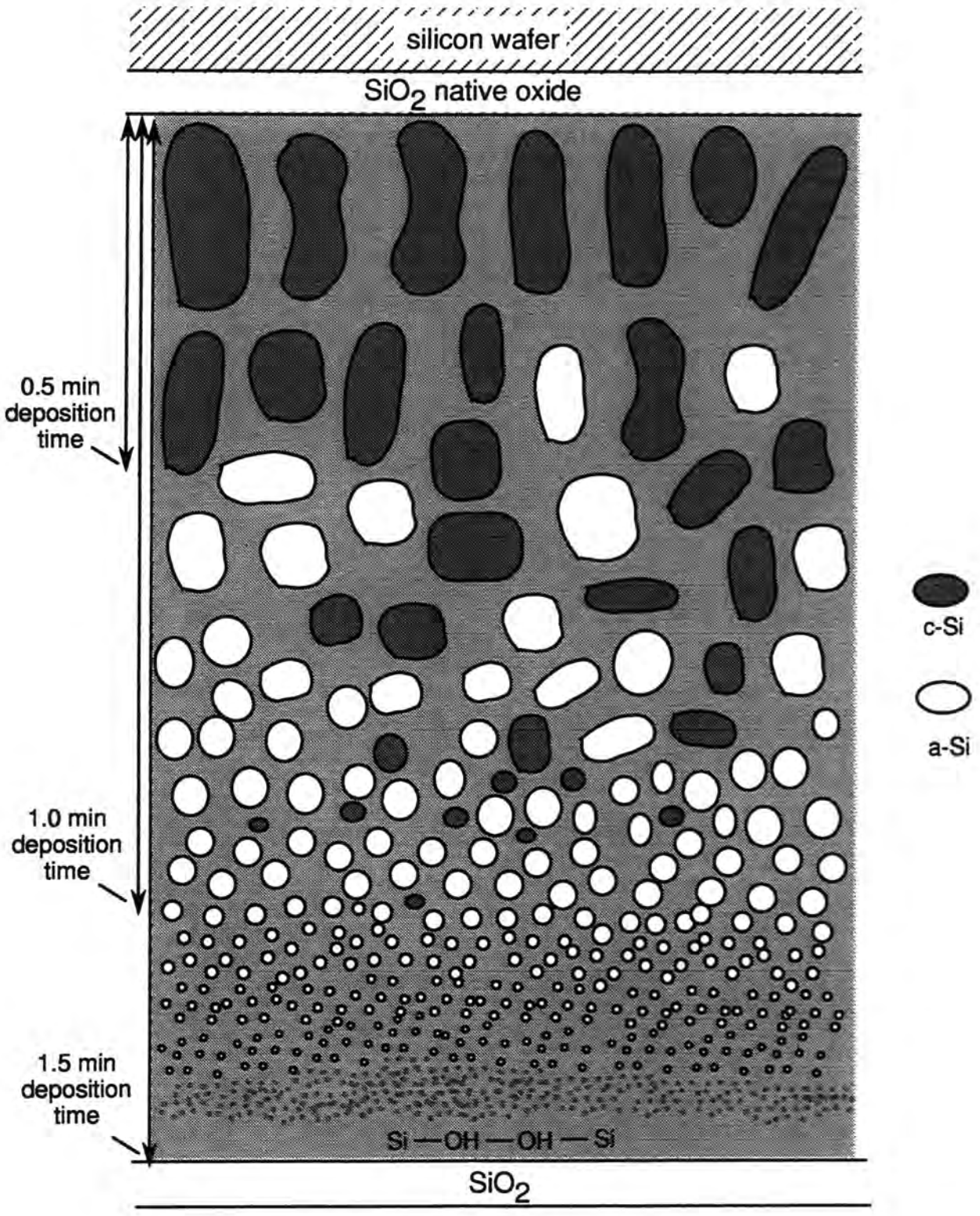

Figure 5.23 A possible structure for the SRO grown at Durham.

kinetics were discussed and an account was given of why the film composition varied with distance from the substrate. TEM and SEM provided additional evidence for the film structure and this information was presented as a series of photographs. Finally, the body of evidence was compared with theoretical models for the microstructure of silicon-rich oxide and a possible structure for the SRO films proposed.

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Chapter 6

Electrical Characterisation

6.1 Introduction

This Chapter concerns the electrical characterisation of the MIS devices. First, typical current-voltage (I-V) characteristics and capacitance-voltage (C-V) characteristics are discussed. Reproducibility was a problem. Before any changes in the device parameters were made, the reproducibility of samples with identical deposition and processing steps was assessed. Edge leakage is also discussed and shown to be negligible. Measurements were made to establish the time dependence of the currents and to determine any 'forming' effects. The results of changes in device parameters, such as film thickness, top contact metal and p- and n-type substrates, are then described. Breakdown voltages were determined for a range of devices. Comparisons were made between annealed and as-deposited samples. Finally, the effect of these variables on the performance of MISS devices is discussed.

6.2 Typical I-V characteristics

The structure of the MIS device investigated in this work is shown in Figure 6.1. For n-type devices in forward bias the top electrode was made positive with respect to the silicon substrate. P-type devices were in reverse bias with this applied voltage and were in forward bias when the metal electrode was made negative with respect to the silicon substrate. This polarity convention is used in the following data plots. The dark currents as a function of voltage characteristics for 'formed', identical SRO MIS devices are illustrated in Figures 6.2, 6.3 and 6.4. Figures 6.2 and 6.3 show the low field I-V curve at 280 K for a two minute SRO deposition on an n-type

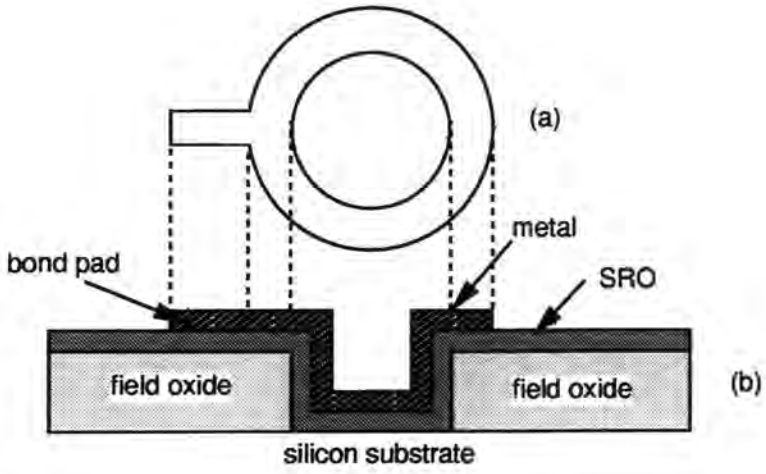


Figure 6.1 (a) Plan view of an MIS device. (b) Cross-sectional view.

and p-type substrate, respectively. The two wafers were processed in the APCVD chamber simultaneously. Every device displayed rectifying behaviour, i.e. the I-V characteristics were similar to those for a diode. N-type devices conducted current in the opposite direction to p-type devices. For comparison, Figure 6.4 shows the typical high field case for the same p-type device at 176 K. Eventually breakdown occurred. Similar plots were observed for either p- or n-type substrates over a range of thicknesses and temperatures.

The data were generated using a voltage change of 0.05 V steps with a delay of 10 s between readings. This allowed current transients associated with the voltage increments to die, to give a stable current measurement. The voltage ramp was then reversed at the same rate. Resulting current values were of the order of 10^{-6} to 10^{-3} A, depending on voltage size and polarity. In comparison with the current-voltage characteristics of other workers [1– 11], these readings tend to be an order of magnitude higher. The high percentages of excess silicon present in these SRO samples mean that low electric fields are required to induce charge transport across the device. There was no hysteresis observed in the readings, which indicates that there was no permanent charge trapping in the oxide or at its interfaces.

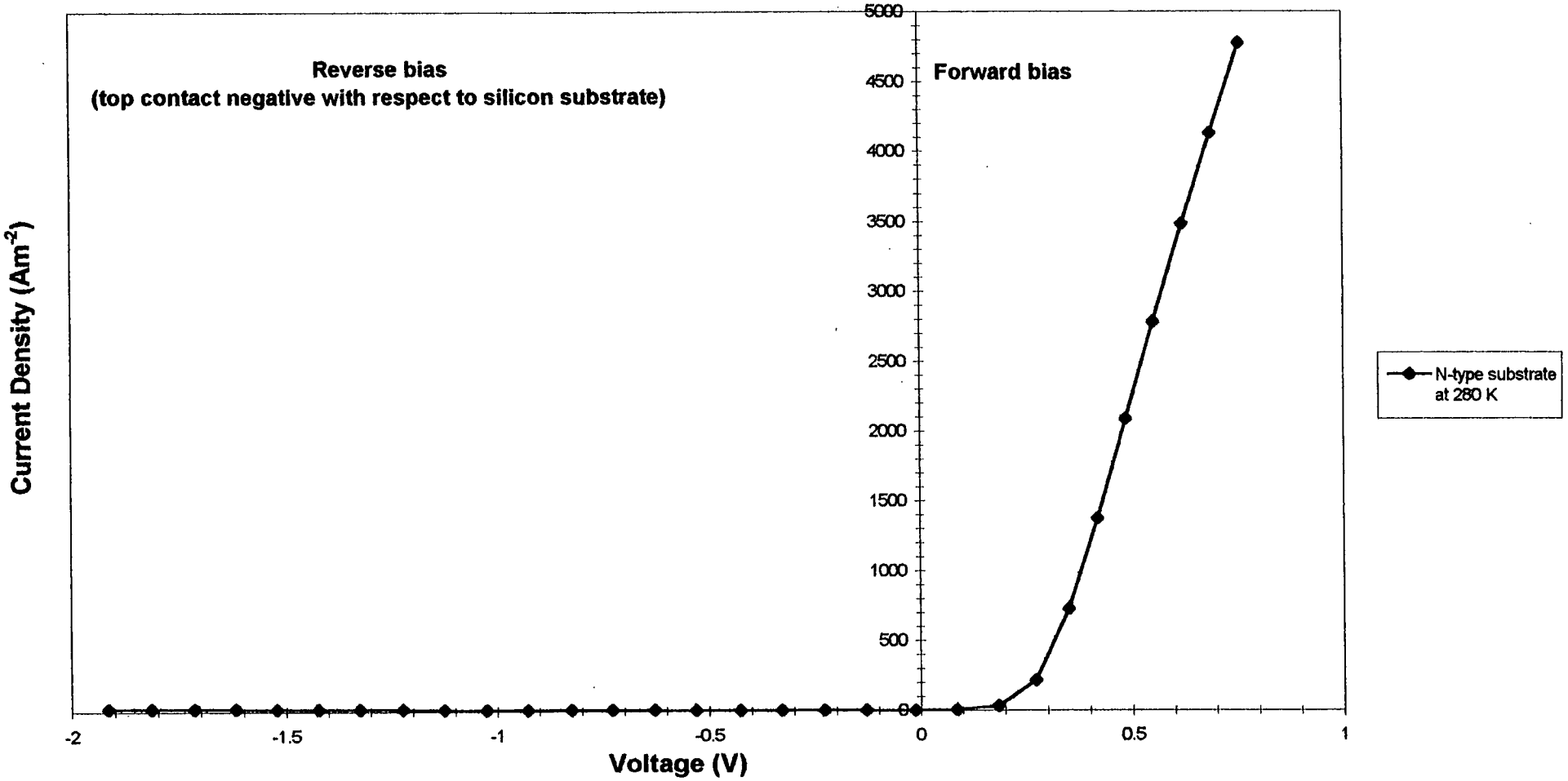


Figure 6.2 Low field dark current-voltage characteristics for a typical MIS device, with an n-type silicon substrate, at 280 K.

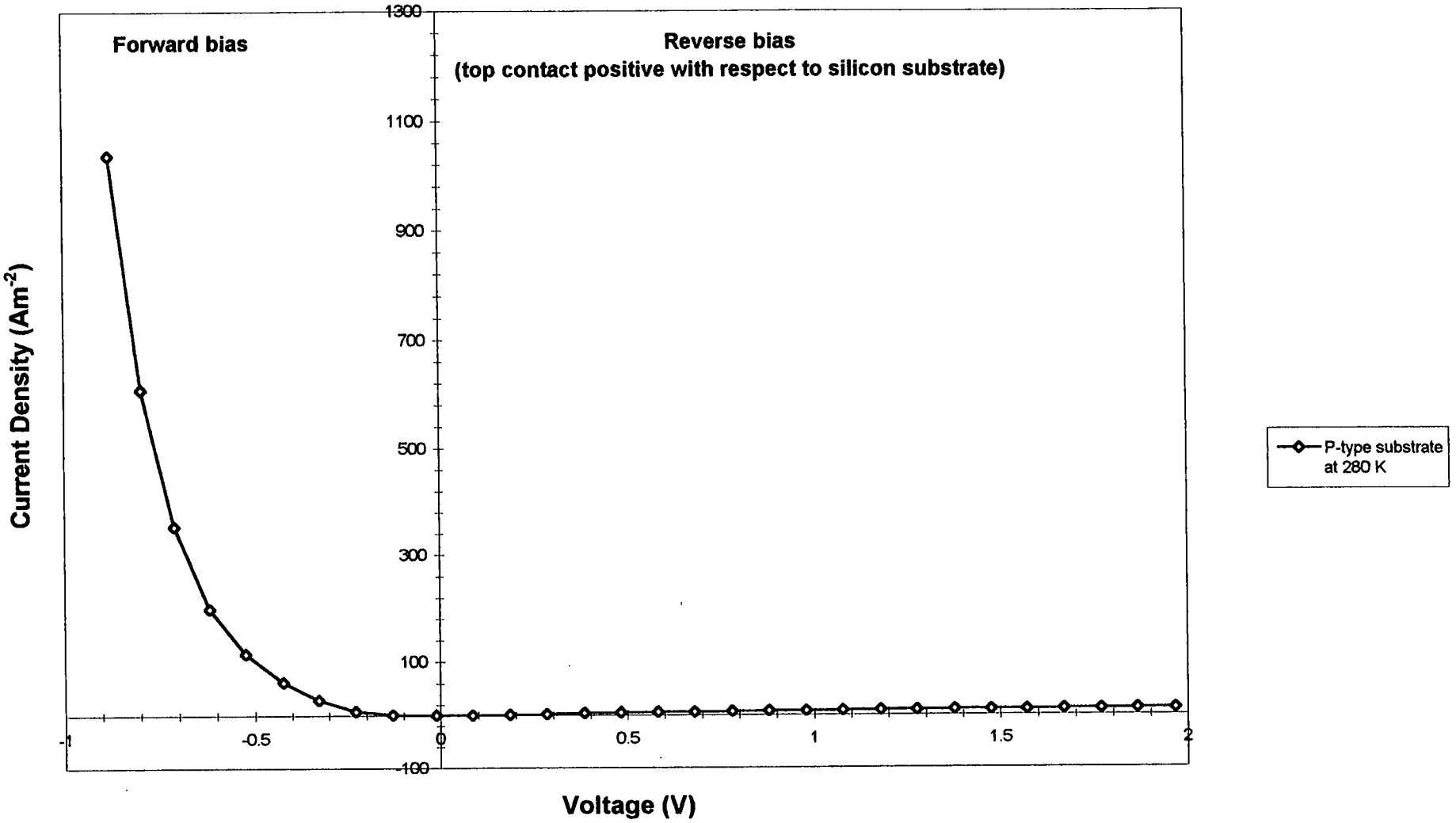


Figure 6.3 Low field dark current-voltage characteristics for a typical MIS device, with a p-type silicon substrate, at 280 K.

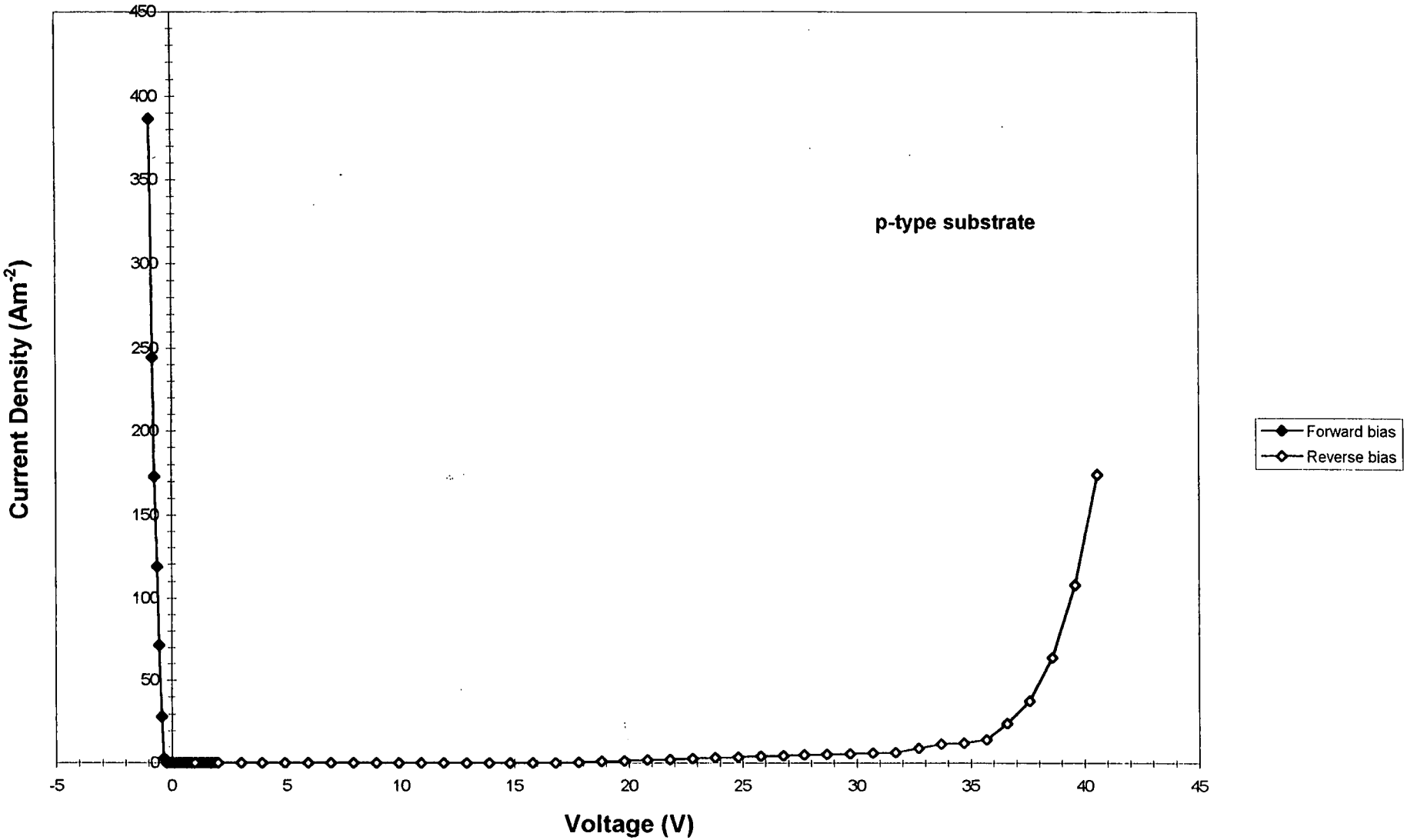


Figure 6.4 High field dark current-voltage characteristics for a typical MIS device, with a p-type silicon substrate, at 176 K.

6.3 Capacitance-voltage curves

6.3.1 Introduction

The current-voltage (I-V) characteristics of the MIS devices have shown that the oxide layer was conducting. The capacitance-voltage (C-V) curves have been plotted to aid further understanding concerning the effects of changing:

(i) the device area;

(ii) the top contact metal;

(iii) the oxide thickness; and

(iv) the substrate from n-type to p-type.

A typical Al-SRO-n-Si 1 MHz C-V curve is shown in Figure 6.5 and is described below.

6.3.2 A typical C-V characteristic

The C-V characteristics shown in Figure 6.5 were measured first in a light tight box and then in a well-lit laboratory. The two curves were coincident. Light stimulates electron-hole pair production. However, this increase in available charge is small in comparison with the accumulation charge and so has negligible effect on the accumulation capacitance. Minority carriers are too slow to respond to high frequency signals. Therefore light stimulation also has no effect on the reverse bias C-V characteristic.

Hysteresis was not observed for changes in the scan direction or repeated cycling from one polarity to the other and back. There was no shift to higher voltages on repeat runs. The C-V curves for each device always followed the same path. Therefore, like the I-V measurements, the C-V measurements showed no evidence of permanent charge trapping.

The inversion and depletion capacitances are as those described for the ideal MIS capacitor in Chapter 2. However, in accumulation, the characteristic is very different. Majority carriers are attracted to the interface but the build up of charge is only momentary. Electrons flow through the leaky oxide to the metal. The capacitance readings changed too rapidly to enable an accurate manual reading. A computerised system could have recorded the maxima for each capacitor, but these maxima were lower than the ideal case, due to unknown rates of charge leakage. Therefore, quantitative measurements were thought to be unreliable.

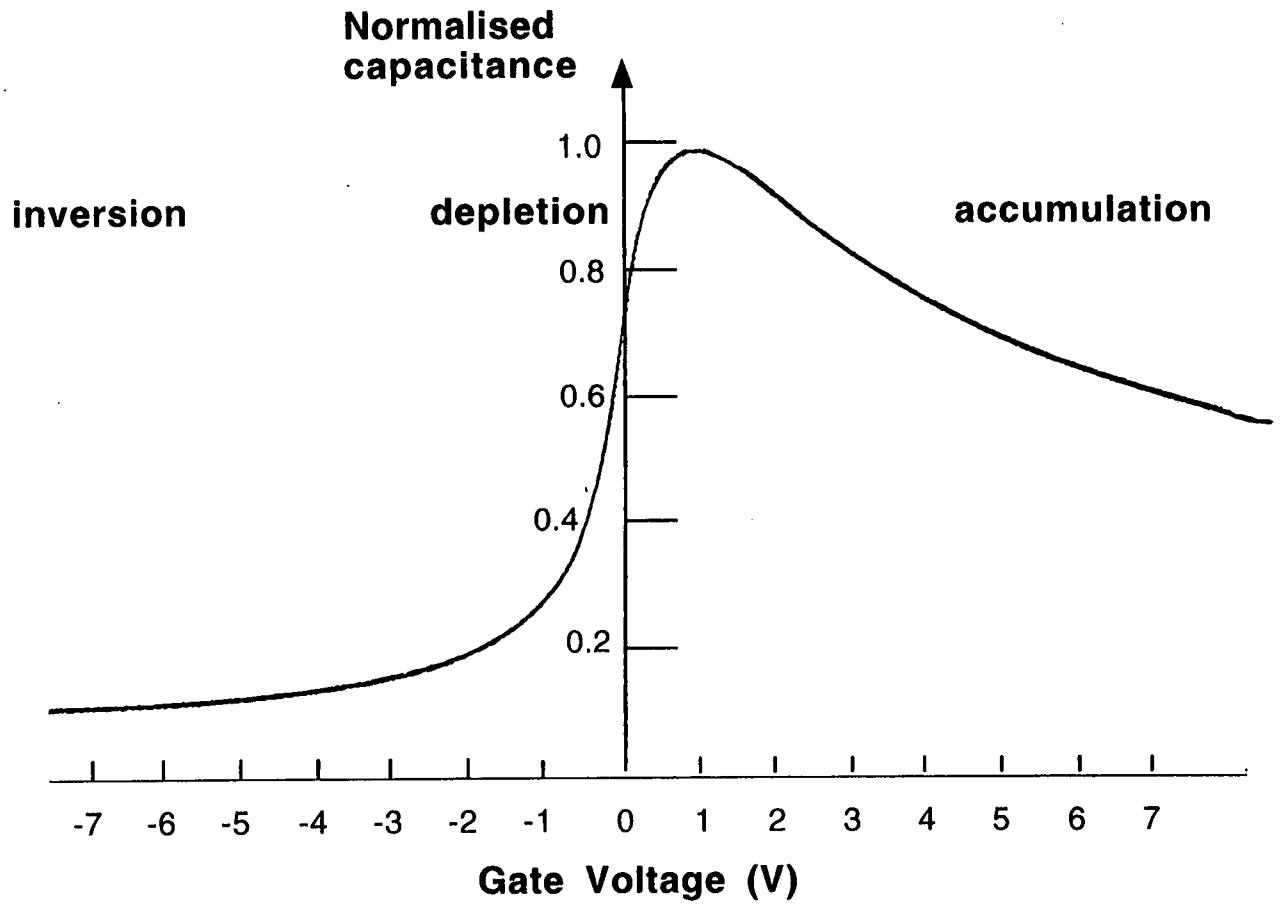


Figure 6.5 A high frequency (1 MHz) capacitance-voltage characteristic of an Al-SRO-n-Si device at 300 K. The SRO was grown in two minutes at 650° C, γ of 0.22 and a top contact of aluminium. Each C-V curve was scanned in 4s.

6.4 Reproducibility

6.4.1 Reproducibility of devices on the same wafer

To observe the significance of changing device parameters, the reproducibility of the I-V characteristics was first determined for identical devices. Each device was labelled A to J, with A representing the largest device area, 3×10^{-6} m^2 and J representing the smallest in the series of 10, of area 3.5×10^{-7} m^2. L and R in the device names represent the left and right sides of the wafer. For all of the reproducibility experiments, aluminium was used as the top contact. The SRO was deposited under the same growth conditions for all samples, i.e. using a reactant gas flow ratio, γ, of 0.22 at 650° C, as described in Chapter 4. The SRO deposition time was varied from 0.5 to 8 minutes.

First, the smallest devices (LJ and RJ), with the thinnest SRO layer (deposited in 0.5 minutes), on an n-type substrate, were compared. The currents were higher for the LJ devices at all voltages. The maximum difference in currents was 50% and so the average difference was $\pm 25\%$. The reproducibility of the smallest devices is, therefore, not ideal and must be taken into account when making comparisons between devices.

The comparison of I-V characteristics was then extended to cover larger device areas on the same wafer. Most comparisons between identical devices yielded an average difference of $\pm 10\%$ or below. Since most devices fell within this limit, the reproducibility was independent of device area. The $\pm 10\%$ differences in conductivity could be caused by the random nature of the SRO and also any errors in purportedly identical device manufacture and processing.

A similar range of current values were obtained for all film thicknesses, though in general the thicker the film the lower the reproducibility. This may be due to the increased oxygen content of the thicker films. As documented in Chapter 5, increased oxygen content increased the randomness of the SRO film structure. Ellipsometric measurements have shown that film thickness varied across the wafer by about $\pm 5\%$. SRO film thickness may be an important device parameter. This is discussed later.

The maximum range in the reproducibility of identical devices on p-type wafers was $\pm 25\%$. Again, an average difference of $\pm 10\%$ was more representative of most devices.

6.4.2 Reproducibility of wafers processed simultaneously

Simultaneous depositions of SRO were carried out for comparisons between n- and p-type substrates and to examine the effect of annealing. The n- and p-type wafers were always positioned in exactly the same place on the susceptor during SRO deposition. This was estimated to be the point of minimum gas turbulence and so produced the most even films. All p-type wafers were positioned to the left of the n-type wafers. Both were equidistant from the edges of the susceptor. The films on all wafers processed simultaneously were the same colour and therefore were covered in SRO to a similar depth. Thickness measurements, recorded in Chapter 5, confirmed this. The reproducibility was found to be independent of substrate material at around $\pm 10\%$. This poor reproducibility must be taken into account when comparing n- and p-type devices and also when estimating the difference caused by annealing the samples.

6.4.3 Reproducibility of wafers processed in different APCVD runs

Initial reproducibility measurements were poor, with an average difference in the current per Volt of $\pm 40\%$. This figure was the worst case room temperature percentage difference observed in the I-V characteristics for identical devices with a 2 minute deposition of SRO. The installation of the mass flow controllers increased reproducibility. This suggests that the gas flows to the chamber must be precisely controlled. SRO composition is therefore an important parameter which determines the exact I-V relation. Although the resistivity of the film alters with each run it should be noted that the curves followed the same relation but were shifted to higher or lower voltages. Since the shape of the curves were constant, a common conduction mechanism is implied.

Once mass flow controllers were installed, the current at a particular voltage differed by a maximum of 32%, for 7 separate but identical APCVD runs. The relative percentage difference was therefore, reduced to $\pm 16\%$. Although the reproducibility was improved the difference was high and means that whenever comparisons are made on wafers processed in separate CVD runs the differences observed must be significantly greater than $\pm 16\%$. This is important for comparing the effect of film thickness, which can only be investigated using several CVD depositions.

In summary, for comparisons made between wafers with different top contact metals, the effect of annealing and p-type versus n-type substrates the range in con-

ductivity is typically $\pm 10\%$. Film thickness comparisons should be made using a difference of $\pm 16\%$. This average value is much lower than the possible $\pm 25\%$ sometimes observed.

6.4.4 Reproducibility and C-V measurements

Evidence from I-V curves has shown that reproducibility of the samples was a problem. C-V curves were also used to assess reproducibility of the device manufacturing processes. A comparison of same sized devices were made at different points on test wafers. Two examples of this are shown in Figure 6.6. Each C-V curve has a flat portion (shoulder) in the characteristic. This is thought to be caused by interface states and the precise C-V relation is discussed in Section 6.9.6. Several cycles of negative and positive voltage scans have been drawn for each of four devices in Figure 6.6. Each curve displayed no hysteresis in the C-V measurements. This was true of all devices on all wafers. Device LJ and RJ are the smallest devices at the left and right hand sides of the wafer, as described in section 6.4.1. A comparison of devices LH and RH is also made in Figure 6.6. Invariably, the two curves for each pair of identical devices did not align. This suggested that the SRO film thickness varied across the wafer surface. The differences were as high as those recorded in the I-V data.

Figure 6.6 shows that the C-V characteristics vary by different amounts for different electrode sizes. The larger the electrode area, the greater the effect of SRO thickness. This is expected since

$$C = \epsilon \frac{A}{d} \tag{6.1}$$

$$C_1 - C_2 = \epsilon A \left(\frac{1}{d_1} - \frac{1}{d_2} \right) \tag{6.2}$$

Reproducibility was also tested from one CVD deposition to the next. Most runs varied by about the same amount as that observed across the wafers. Occasionally poor reproducibility was observed. In general, the C-V curves showed a smaller variation than that observed in the I-V curves, which suggests that the previous figures quoted are worst case values.

6.4.5 Reproducibility on temperature cycling

Reproducibility was also affected by cycling the temperature between 20° C and −55° C. During the measurement process all devices were cooled to at least −55° C

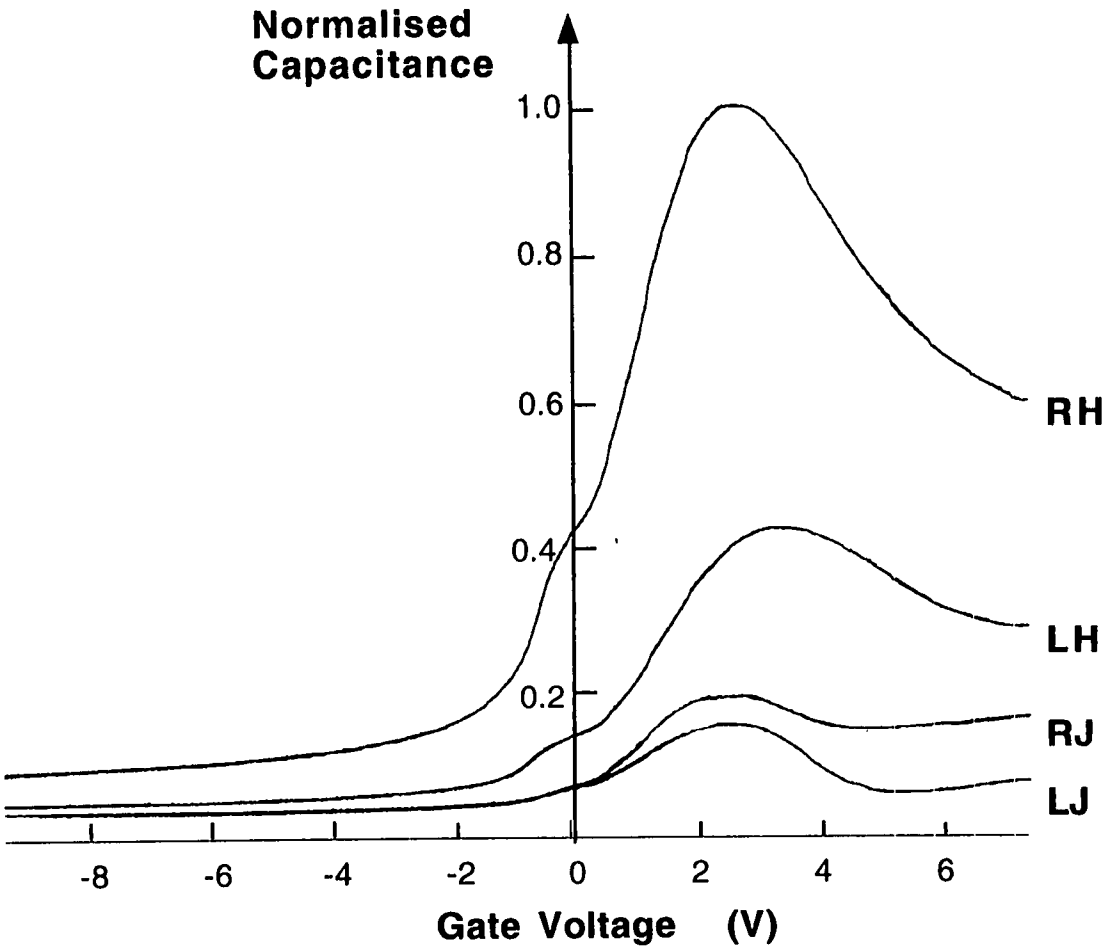


Figure 6.6 A comparison of the capacitance-voltage (C-V) curves, using a 1 MHz signal, for devices of the same area on different parts of the wafer. Devices LH and RH have an area of H = 7.27 $\times, 10^{-7}$ m^2 and devices LJ and RJ have an area of J = 3.66 $\times$ 10^{-7} m^2. The SRO was grown in two minutes at 650° C, γ of 0.22 and a top contact of aluminium. Each C-V curve was scanned in 4s.

and allowed back to room temperature several times. Temperature cycling in this way is unlikely to occur in the use of SRO as the semi-insulator in MISS devices. However, since all devices were subjected to this temperature cycling, its effect should be evaluated.

A constant voltage was applied to the devices and the temperature cycled several times. The current increased with each successive temperature cycle but was constant within each cycle. After 5 to 7 temperature cycles the current became constant. For example, a wafer with a 2 minute deposition of SRO was found to have a worst case variation for device LA of $\pm 7\%$. Typical differences for device LJ were $\pm 10\%$ over all forward biases. In reverse bias the reproducibility was better at $\pm 7\%$. The relative percentage difference increased for the smaller devices, probably due to the use of a more sensitive scale.

The change in current due to temperature cycling may be caused by a structural change at the wafer-film interface. The stresses induced on the wafer by the SRO film were described in Chapter 5. Temperature cycling may cause a lowering of the number and/or occupancy of traps at the substrate-SRO film interface. This may then account for the increased current observed per Volt when the temperature is cycled.

In summary, temperature cycling adds a further reproducibility factor on top of that caused by device manufacture. In an attempt to minimise this, all wafers were subjected to five temperature cycles before any I-V or C-V measurements were recorded. The overall difference was therefore taken to be $\pm 12\%$ for simultaneous depositions and $\pm 18\%$ for individual depositions. This would be an over estimate for most samples.

The random nature of the SRO film may be responsible for the poor reproducibility of the samples or it may be that even tighter controls need to be applied during device manufacture. Pre-warming the gases, before entry into the CVD chamber, would create a more reproducible film and one which would most probably be more constant in composition. However, such an improvement may produce films which would behave differently to those films used in the Durham SRO MISS devices. This type of temperature cycling treatment can be thought of as a 'forming' treatment. Forming is described in more detail below.

6.5 Forming

When a voltage is first applied to a sample the resultant current flow is thought to cause structural changes. These changes cause the current to vary each time the same voltage is applied. Once the device structure settles down the current becomes steady and reproducible. This process is known as forming.

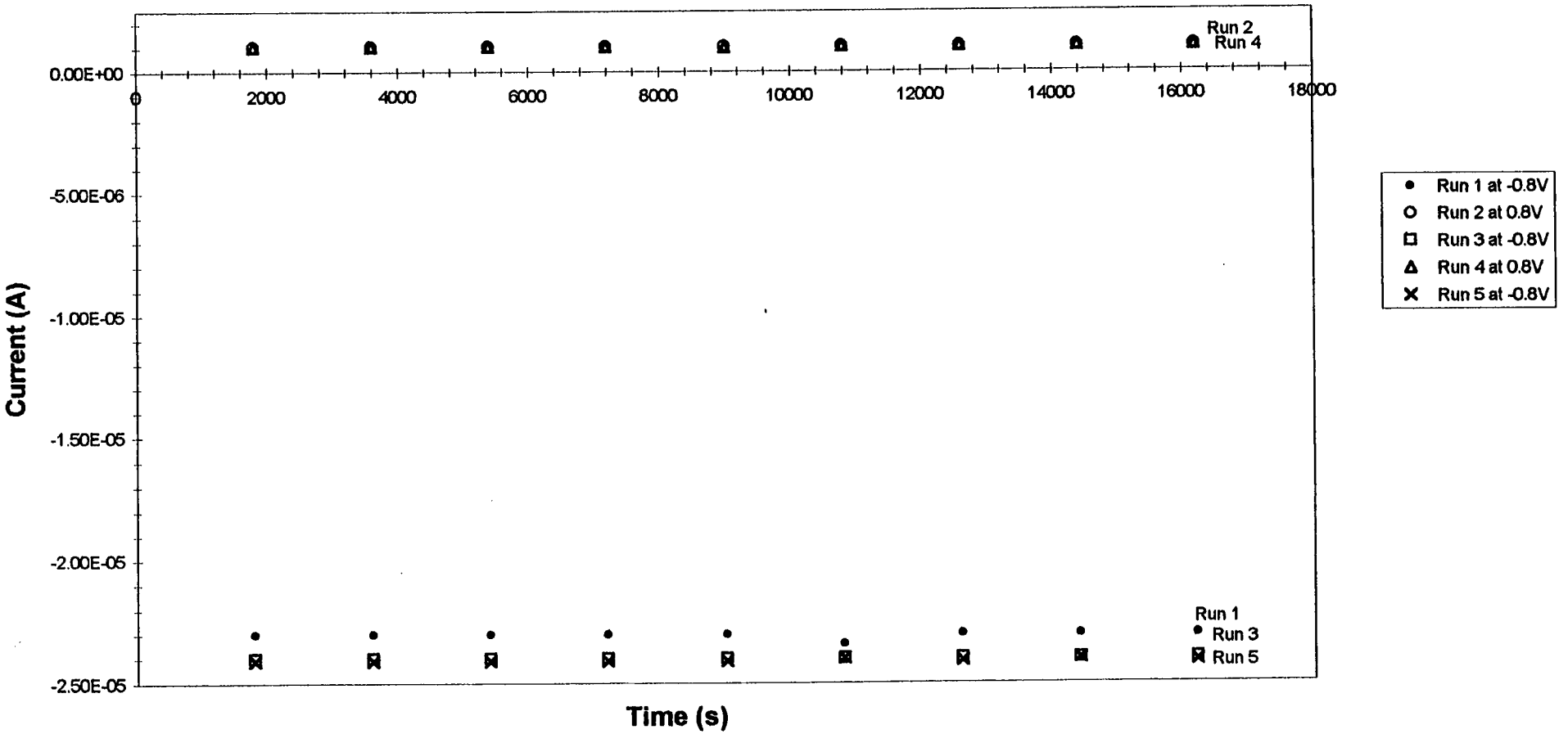
The current-time characteristics were obtained by holding the voltage constant at 0.8 V, in forward bias, and measuring the current at fixed time intervals. The time intervals were varied from a few seconds to 30 minutes. In all cases a flat current-time characteristic was obtained. When the voltage source was reset to 0 V and then the forward bias re-applied, the current-time characteristic remained flat but was shifted to a slightly higher current level. A forming process was thus identified. An example of this is shown in Figure 6.7. To generate these data a forward bias of -0.8 V was applied to device LJ on an n-type substrate for five minutes. The polarity of the voltage was reversed and applied to the device several times. Figure 6.7 shows the lower initial forward biased current, measured for run 1 and the increased current for subsequent runs in forward bias. Reverse bias currents were constant during the forming process. The forming effect was small but present in all of the samples tested.

The lowest temperature the ethanol system was capable of was $-55°$ C. This was the only temperature that could be sustained and so all forming investigations were made at $-55°$ C. A voltage of -0.8 V, i.e. close to the maximum voltage which causes overload, were applied to the device and the current noted at 30 minute intervals. The current measurements were repeated when the voltage was switched to 0.8 V and then returned to -0.8 V.

Figure 6.8 shows the resultant formed dark currents as a function of time for a range of devices, on a wafer with a 2 minute deposition of SRO, in forward bias. In general, the larger the device area the larger the current. Device LA had an area of 3×10^{-6} m^2 and the smallest device, LJ, had an area of 3.5×10^{-7} m^2. These currents are very stable. Formed samples remained stable when remeasured several days later. There were no transients associated with charge trapping.

The forming effect in the SRO samples was small, at less than 5%, but all samples were voltage-formed before a temperature-forming process. Forming may be caused by permanent electron trapping into deep sites. Once these traps are filled current flow was higher and stable. Reproducible I-V characteristics were obtained for all formed devices.

Figure 6.7 Plots of dark current against time showing the forming effect for device LJ at 217 K. The device was manufactured with an SRO layer grown in one minute at 650° C, γ of 0.22 on an n-type substrate and a top contact of aluminium.



6.6 Edge effects

A further consideration must be taken into account before comparisons between different devices can be made. This is the dependence of current density, J, as a function of average electric field, $\mathcal{E}$, on device area and perimeter. The areas were varied from $2.69 \times 10^{-7}\,m^2$ to $1.42 \times 10^{-7}\,m^2$ which resulted in a change in perimeters from $1.33 \times 10^{-3}\,m^2$ to $5.81 \times 10^{-3}\,m^2$. Figure 6.1 shows the structure of an MIS device and illustrates the relation between the device area and the metal area. The device area is the area of the hole etched into the field oxide, ready for SRO deposition. SRO was deposited across the whole of the wafer surface and then the metal evaporated onto the device areas. The electrodes encircle the device areas and overlap the surrounding field oxide. A bonding pad is evaporated simultaneously onto the field oxide and is part of the top contact area. The metal area therefore is larger than the device area.

Figures 6.9 and 6.10 show the same linear relation between the current and the device area, A, and the metal area, respectively. The current was proportional to device area. This pattern was common for all devices. Figure 6.11 shows a square law relation for the current and the device perimeter. Since the current is proportional to device area, it follows that the current will be proportional to the square of the perimeter. There was no dependence of J versus $\mathcal{E}$ on A, P or A/P for all thicknesses or for either gate polarity. This implies that the dark currents in SRO MIS devices are macroscopically controlled and are not associated with oxide defects or edges of contacting electrodes.

6.7 Device area

Figures 6.8, 6.9, 6.10 and 6.11 also show that the current is approximately proportional to device area. In accumulation, the device capacitance was expected to be directly proportional to the top contact area. Figure 6.12 shows that the larger the area the larger the capacitance at all voltages. The figure in brackets, shown beside each C-V curve, represents the highest capacitance observed. A linear relation between capacitance and area was not evident for any voltage value.

In an ideal capacitor the oxide layer is insulating and the charge is maintained on the positive and negative electrodes. In these SRO devices the oxide is very leaky and charge flows through the semi-insulating layer. When the semiconductor is accumulated or inverted the charge does not reach its theoretical maximum due to an unknown rate of charge leakage across the oxide (discussed earlier). At a particular

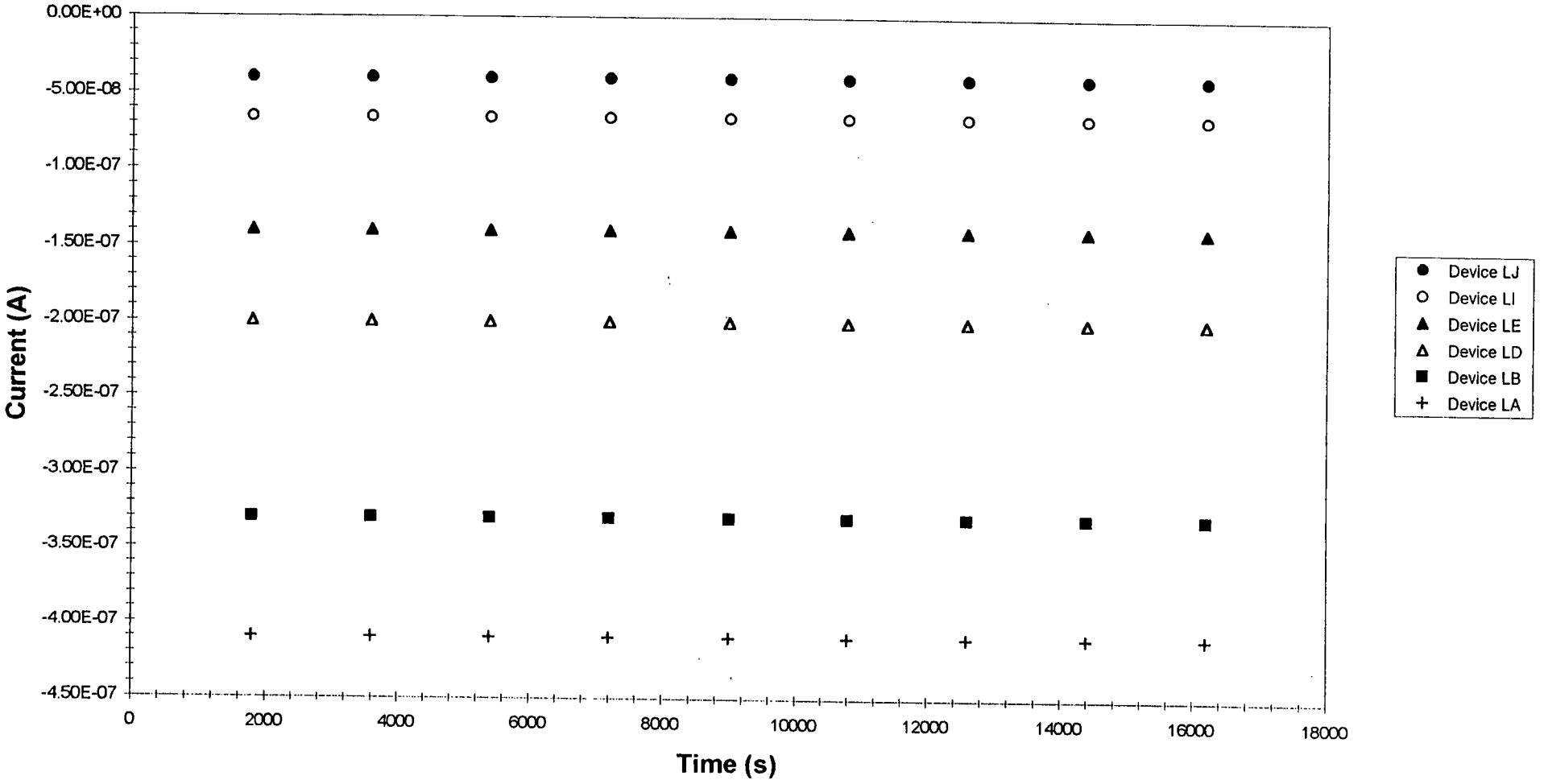


Figure 6.8 Formed dark current against time, at a constant voltage of -0.8 V, for a range of device sizes on the same wafer, at 217 K. The SRO was grown in two minutes at 650° C, γ of 0.22 and a top contact of aluminium.

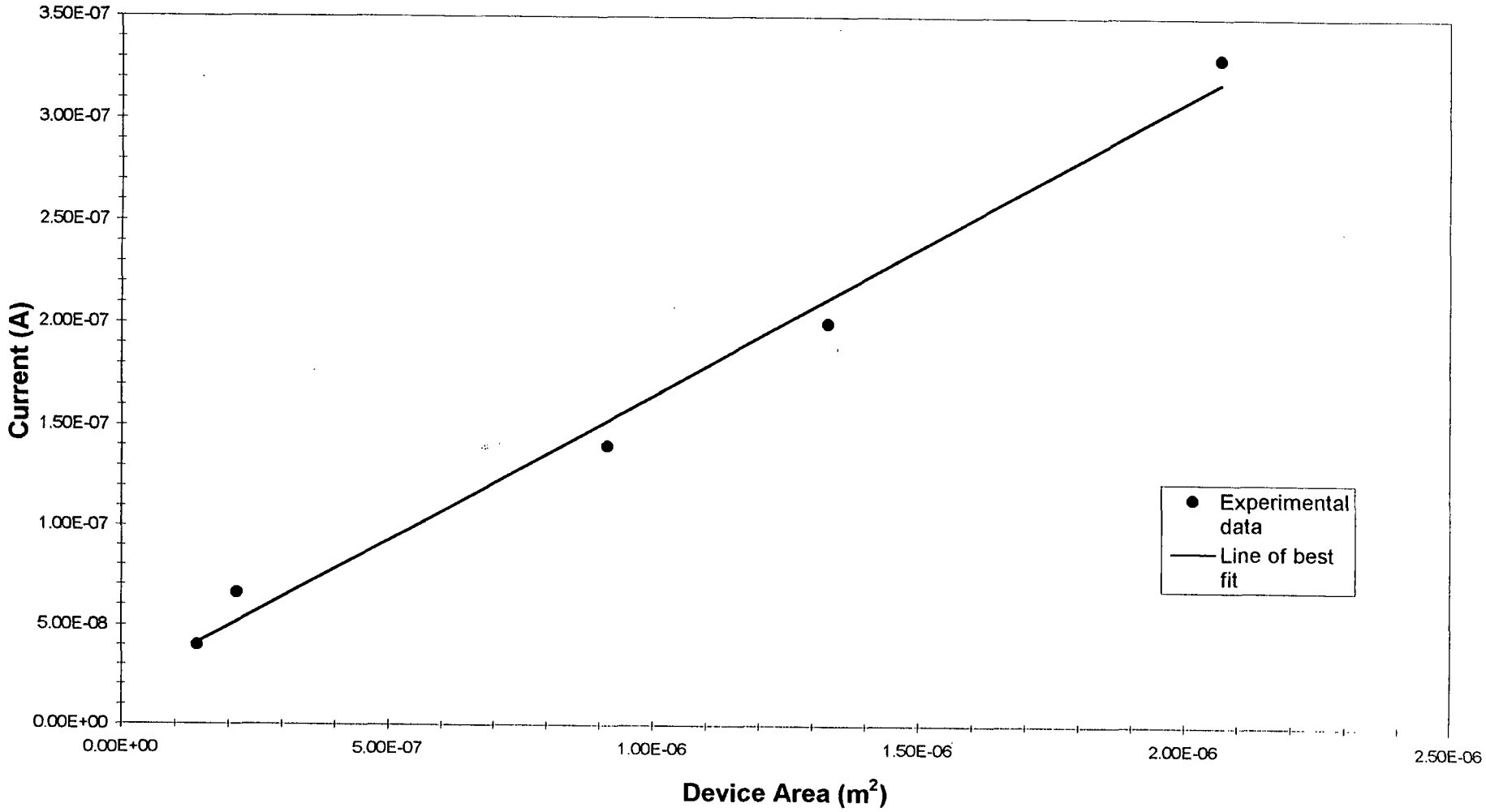


Figure 6.9 A plot of dark current against device area at a voltage of -0.8 V and a temperature of 217 K and the line of best fit. The top contact was aluminium, the SRO was grown in two minutes at 650° C, γ of 0.22 on an n-type substrate.

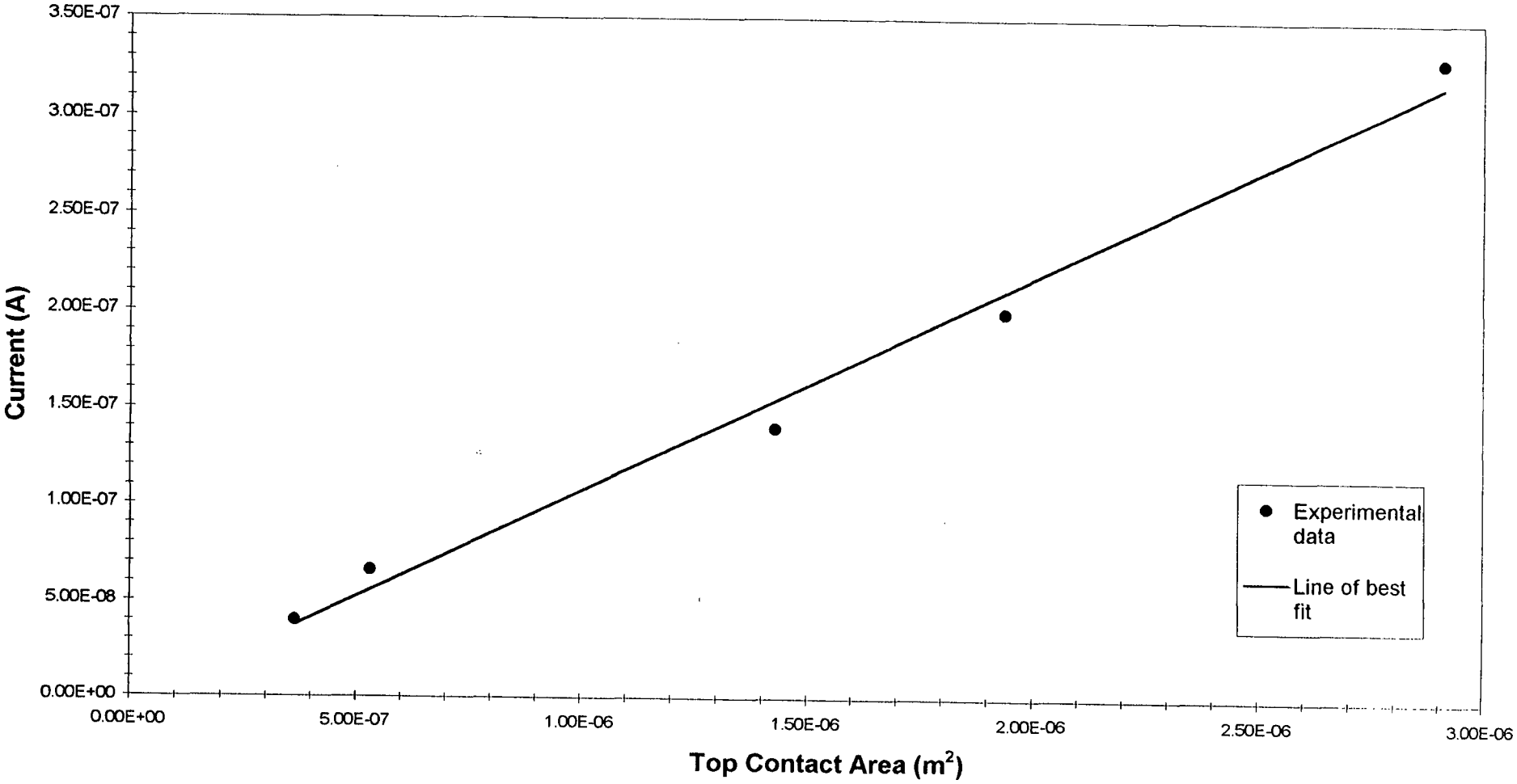


Figure 6.10 A plot of dark current against metal area at a voltage of -0.8 V and a temperature of 217 K and the line of best fit. The top contact was aluminium, the SRO was grown in two minutes at 650° C, γ of 0.22 on an n-type substrate.

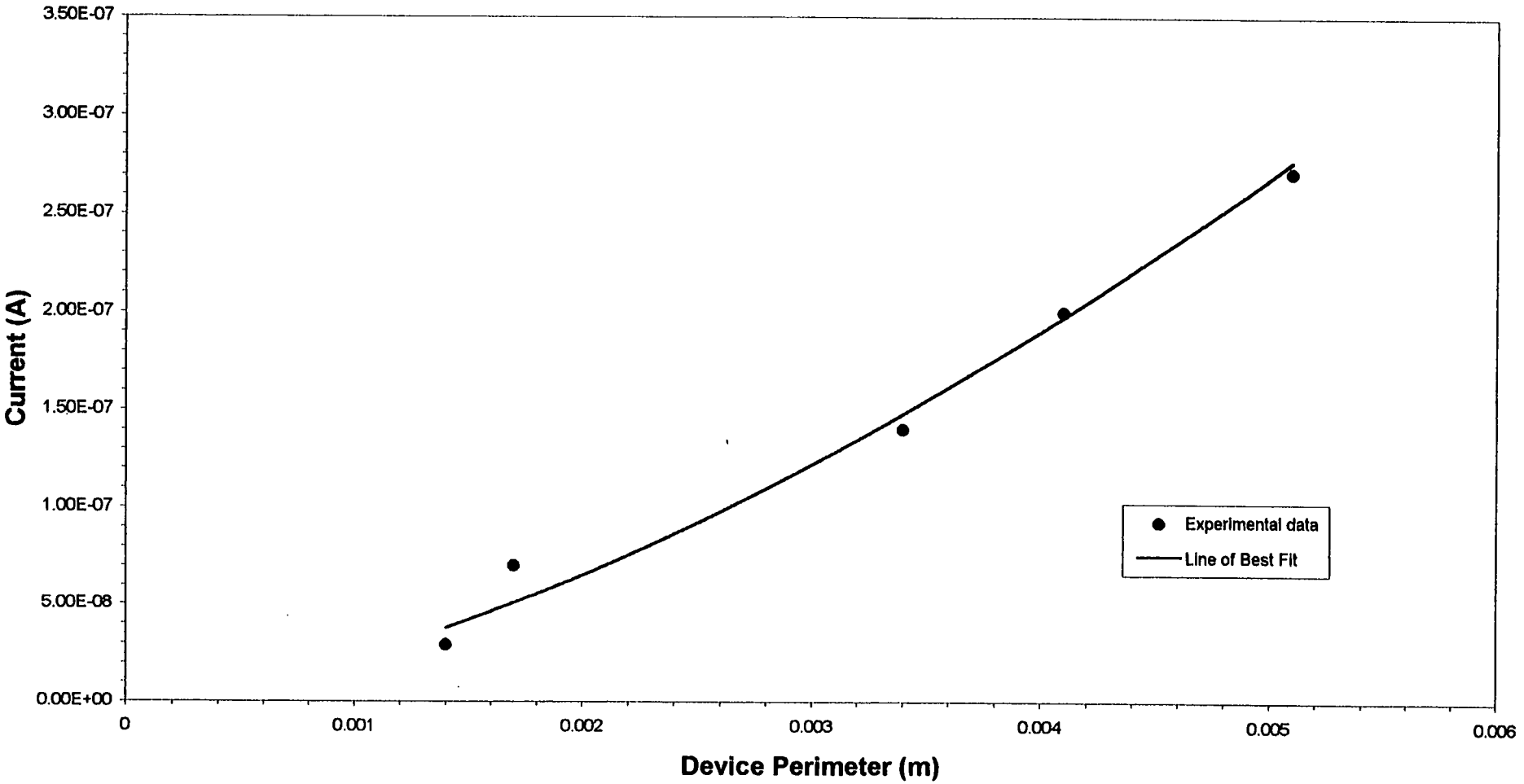


Figure 6.11 A plot of dark current against device perimeter at a voltage of -0.8 V and a temperature of 217 K and the line of best fit. The top contact was aluminium, the SRO was grown in two minutes at 650° C, γ of 0.22 on an n-type substrate.

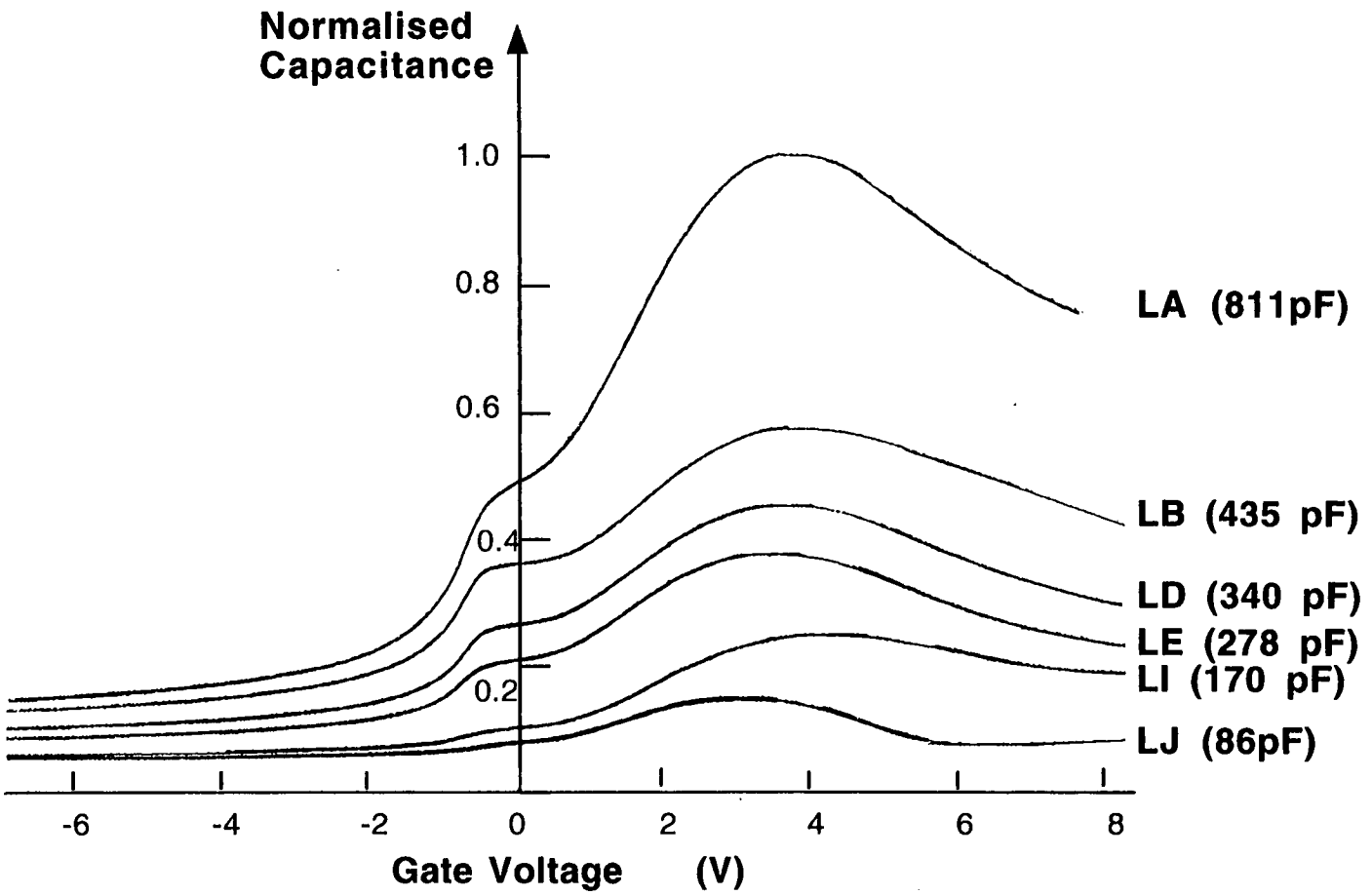


Figure 6.12 Room temperature capacitance-voltage characteristics of Metal-SRO-n-Si devices of different areas at 300 K. RA is the largest device area and RI the smallest. The SRO was grown in two minutes at 650° C, γ of 0.22 and a top contact of aluminium. Each C-V curve was scanned in 4s using a 1 MHz signal.

applied voltage, the rate of flow of charge through the oxide is partly determined by the top contact area and partly determined by the properties of the SRO film which is independent of area. There is a trend for increased capacitance with increased device area but the capacitance-area relation is not linear.

6.8 Thickness comparisons

6.8.1 C-V evidence

C-V curves for identical SRO growth conditions were plotted at 300 K for 4 wafers. Each C-V curve was scanned in 4s. All curves were scanned several times and there was no hysteresis in any of the measurements. The wafers were processed with deposition times, ranging from 0.5 to 8.0 minutes. Device LE is shown in Figure 6.13. Samples deposited in 0.5 and 1.0 minute showed similar characteristics. Once the deposition time exceeded this, in general, the capacitance became more stable. This was expected since thicker SRO layers were expected to contain higher amounts of SiO_2. Therefore, thicker layers are more insulating and so the charge was expected to leak away more slowly. Figure 6.13 shows the thinner the SRO film, the higher the capacitance. The slope of the depletion C-V curve is highest for the thinner SRO layers. Under reverse bias the majority carriers are easily repelled by the close proximity of the gate voltage. As the majority carriers move away from the interface the capacitance rapidly falls. As the oxide layer becomes thicker more voltage is lost across the oxide and a higher voltage is needed to deplete the silicon. The gradient of the resulting C-V curve is therefore lower. Similarly, in accumulation more voltage is required to achieve the same level of charge in thicker samples. All devices show the same level of capacitance in inversion. This has been described earlier and is due to the inability of minority carriers to respond to the high frequency signal used to obtain the C-V curves.

6.8.2 I-V evidence

The effect of film thickness on typical dark currents as a function of voltage is shown in Figure 6.14 for n-type samples. A similar pattern was observed for p-type devices. Even allowing for large differences in reproducibility, increasing the film thickness significantly reduces the current in both n- and p-type MIS devices.

Typical plots of dark currents versus film thickness are shown in Figures 6.15

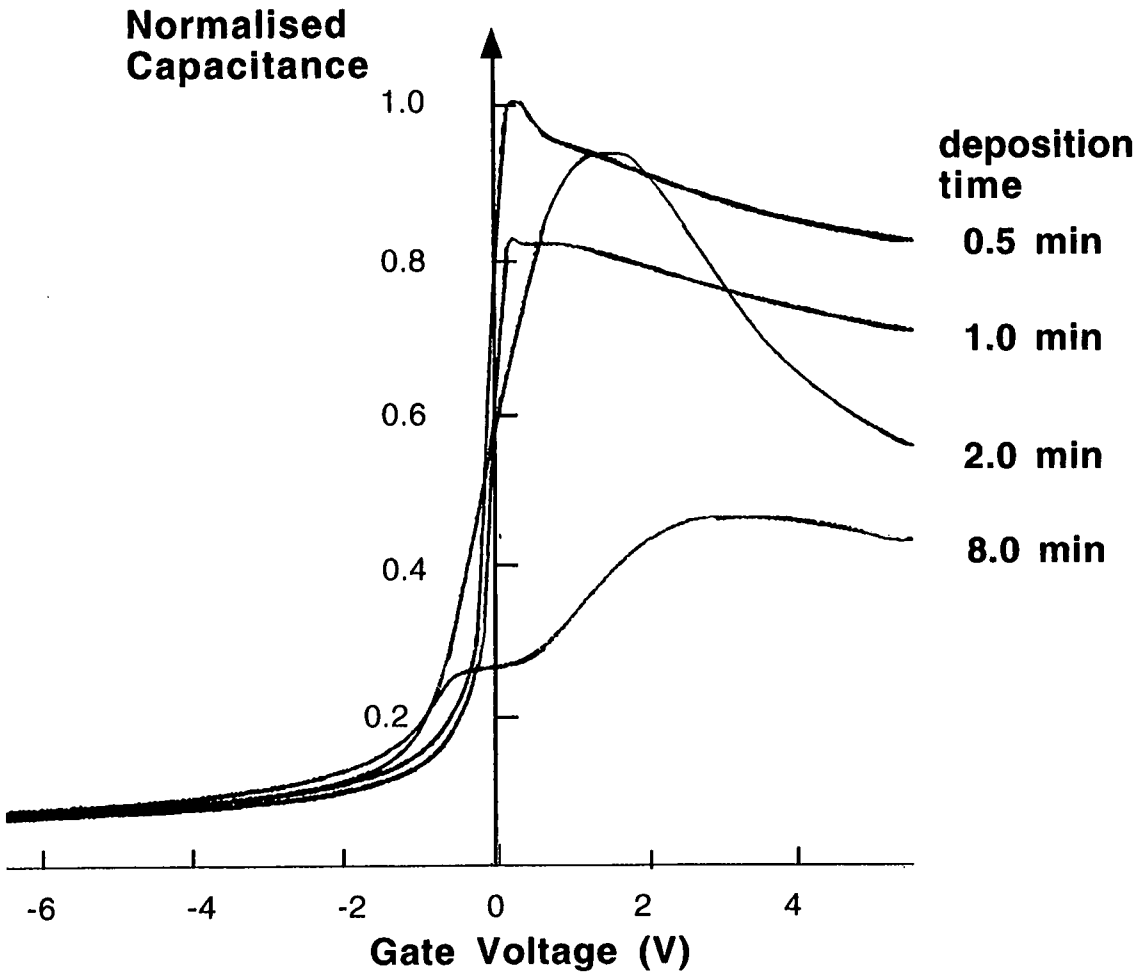


Figure 6.13 Room temperature C-V curves for device LE for a range of deposition times 0.5 to 8 minutes. Each C-V curve was scanned in 4s using a 1 MHz signal.

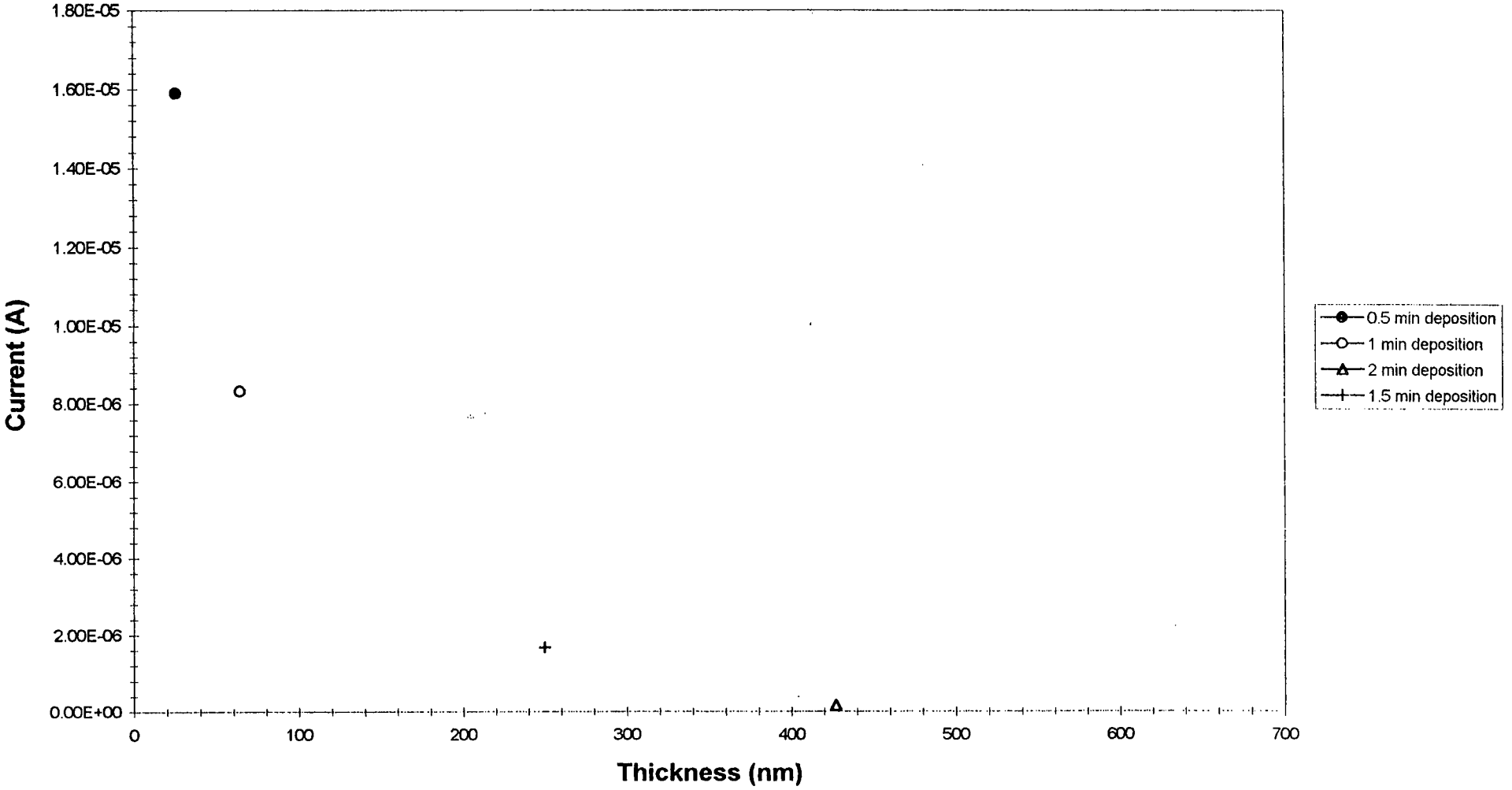


Figure 6.15 Room temperature dark current versus SRO film thickness at a constant voltage of 0.8 V in reverse bias. The SRO was deposited in 0.5 - 2 minutes at 650° C, γ of 0.22, on an n-type substrate and a top contact of aluminium.

and 6.16. These graphs show that there is no polarity dependence of film thickness, i.e. both polarities are affected equally by changes in film thickness. SRO gradually becomes closer to the insulator, SiO_2, with increasing film depth. The increased current path length and increase in oxygen concentration caused only a **moderate** dependence of current on film thickness.

6.8.3 The effect of film thickness on MISS devices

The oxide film depth provides a means of controlling the size of the turn on voltage for MISS devices. MISS devices with thinner oxides have higher switching voltages. This is because minority carriers are attracted to the silicon-oxide interface by the gate voltage. As outlined in Chapter 1, these carriers then traverse the SRO to the gate. There is little build up of minority carriers. High voltages must be applied to cause an imbalance between the number of carriers arriving at the interface to the number of carriers leaving through the oxide. Thicker oxide layers have higher resistivities which limit the leakage currents. Therefore, inversion occurs at lower voltages. The inversion state coincides with the device switching on. Thicker film devices, therefore, switch on at lower applied biases. The SRO film thickness can be controlled by altering the deposition time and so MISS devices can be manufactured with specific switch on voltages.

6.9 Top contact metal

6.9.1 Introduction

Several depositions of SRO were made to investigate the effect of top contact metal on the conductivity of the MIS devices. The deposition time was fixed at 2 minutes. Quarter wafers were processed in the reactor separately with identical SRO growth conditions ($\gamma = 0.22$ at 650° C). Four new quarter wafers were also placed in the reactor simultaneously and the same temperature, gas flow rates and deposition times repeated as for the individually processed samples. Once deposition was complete an attempt was made to process the wafers in precisely the same way until the evaporation of the top contact metal. The simultaneous depositions were compared with those deposited separately. Film thickness varies with the position of the wafer on the susceptor of the APCVD reactor. Alternatively, film composition alters with each deposition. As discussed in the section on reproducibility, those samples processed

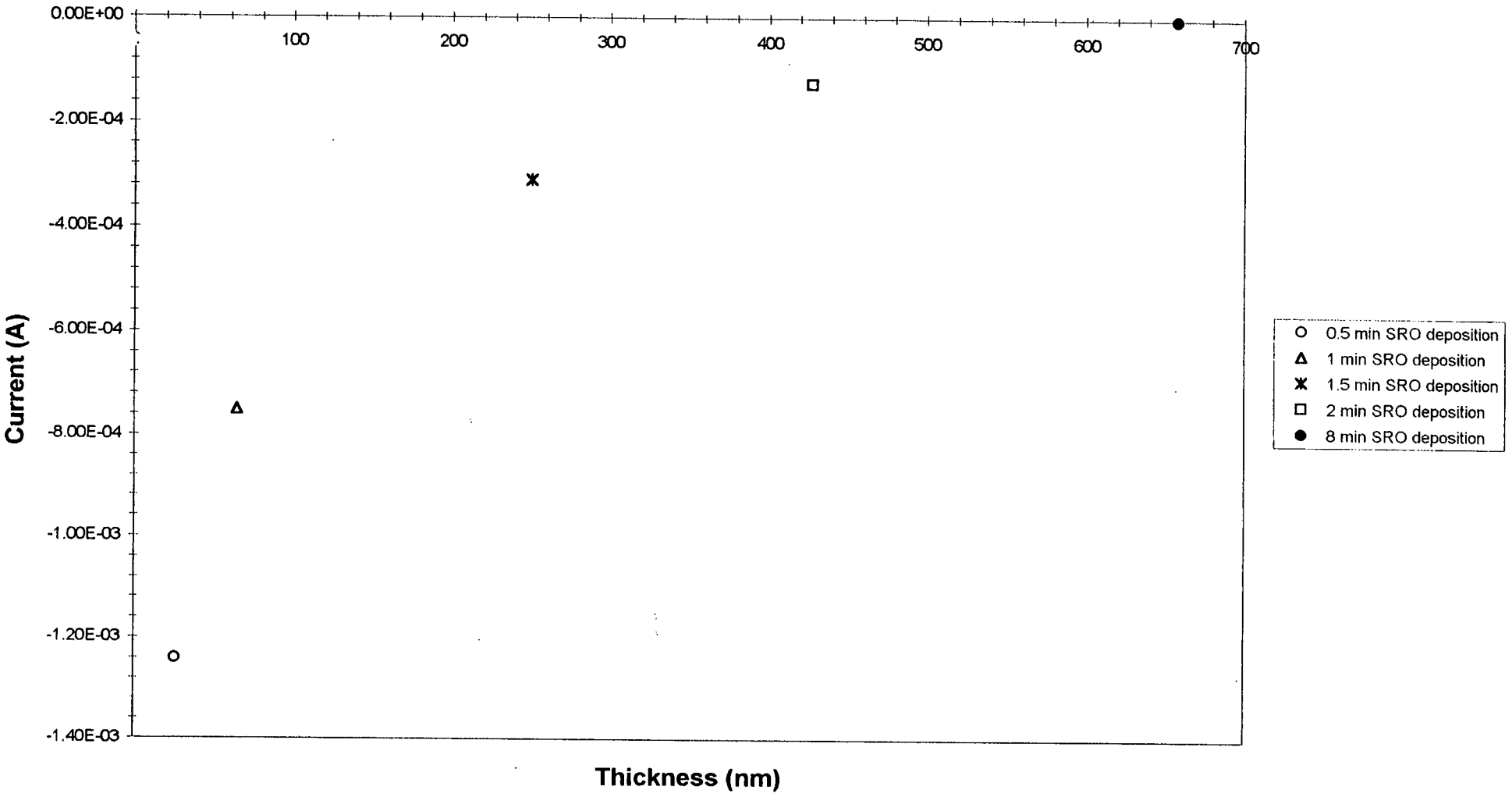


Figure 6.16 Room temperature dark current versus SRO film thickness at a constant voltage of 0.8 V in forward bias. The SRO was deposited in 0.5 - 8 minutes at 650° C, γ of 0.22, on an n-type substrate and a top contact of aluminium.

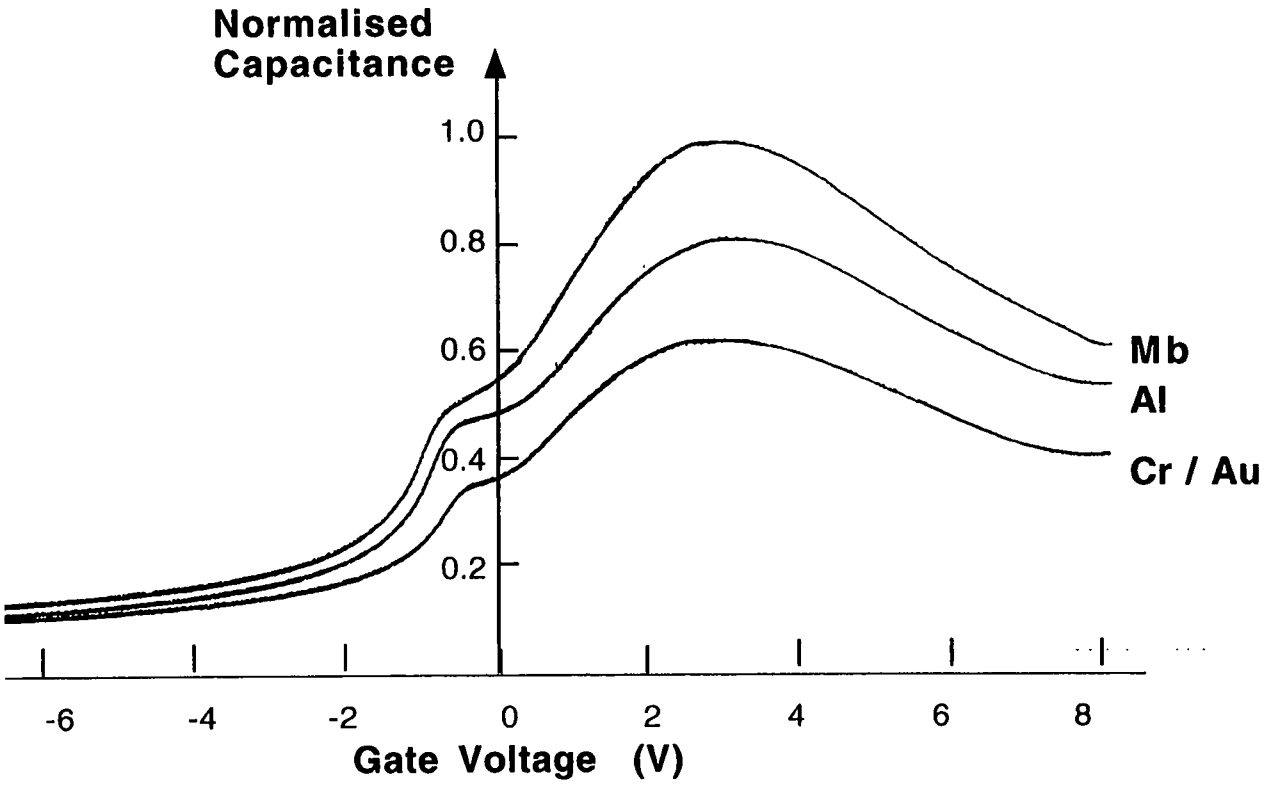


Figure 6.18 C-V curves for three top contact metals, evaporated on SRO deposited in 2 minutes with $\gamma = 0.22$ at 650° C. Each C-V curve was scanned in 4s using a 1 MHz signal.

easily be controlled in MISS devices is the size of the electrode area.

The metal itself is relatively unimportant in device performance. The C-V curves have shown that it is the interface charges at the metal-oxide interface which makes conduction in SRO devices independent of electrode material. Aluminium forms a good bond with the SRO and with the gold wires used in gold ball bonding. The molybdenum posed problems because it is harder than aluminium and therefore more difficult to use with bonding machines. Gold does not stick to SRO and is removed during wet etching processes. A mechanical mask is required to deposit gold so that no etching is necessary. Chromium requires a gold top layer to act as a mask for etching. Since, the top contact material is not critical, aluminium is recommended for MISS device manufacture.

6.10 Substrate doping

6.10.1 I-V evidence

Identical devices were fabricated simultaneously on p- and n-type substrates. For all thicknesses, the n-type MIS devices showed a higher current per Volt, at low fields, than the p-type devices. Saturation occurred at a higher voltage for the p-type devices than for the n-type equivalents. This pattern was observed consistently in all comparisons made between n- and p-type devices and, even allowing for the $\pm 10\%$ differences in reproducibility, is thought to be a significant effect.

The difference between n- and p-type substrates was difficult to assess because of the limited number of wafers investigated. The n-type wafers were orientated in the <100> direction and the p-type wafers in the <111> direction. In addition, the p-type wafers had a lower resistivity than the n-type substrates, but had a lower doping level, as described in Chapter 4. Usually, a higher doping level is coincident with a higher conductivity in all semiconductor devices. Substrate resistivity is important in MISS devices [13, 14]. To assess this effect more accurately a range of n- and p-type substrates with varying substrate resistivities (and doping levels) would need to be investigated. Even the relative position on the susceptor should be exchanged in any further investigations. However, both types of MIS device were affected slightly differently by bias. This may be due to the different substrate resistivities, dopant concentrations or may be due to the different charge carriers. It is could be due to the different crystal orientations but the silicon-silicon oxide interfaces for [111] and [100] silicon surfaces are similar [15]. The silicon-silicon dioxide barrier is independent

of silicon orientation to within 0.1V [16]. When the silicon orientation **and** I-V reproducibility are taken into account, the observed difference in the p and n-type devices is insignificant. However, in all cases the p-type devices turned on at a higher voltage than the n-type equivalents.

The p-type samples have a higher barrier to overcome. Once this barrier is overcome the current climbs at a higher rate per Volt than in the n-type samples. Carrier flow, therefore, appears to be easier for holes, once the initial barrier is overcome. This implies a Schottky type of effect or it may be that there are space charges which inhibit hole flow at low voltages.

The I-V characteristics for thicker SRO films show that in reverse biased n-type devices, the currents are higher than in forward biased p-type devices for low values of electric fields. This means that the barrier seen by forward biased p-type devices is absent or reduced in reverse biased n-type devices and suggests that it is space charges and not potential barriers within the bulk of the SRO that control the current. If this barrier were caused by a layer of positive charge at the silicon-oxide interface the electrons in the n-type silicon could partially counteract this. In the p-type substrate the holes see the uncompensated positive charge. A higher potential is required to attract holes to the interface and to pull them through the barrier. This I-V evidence, therefore, suggests a positive charge layer at the silicon-oxide interface.

6.10.2 C-V evidence

The C-V curves for identical n- and p-type MIS devices were also compared. Since the measured capacitance is dependent on the speed of accumulation of charge, it must also be dependent on the doping density (as discussed in Chapter 2). Therefore, the n-type wafers were expected to show higher capacitance values. Aluminium was used as the top contact metal and in theory, for n-type silicon, the surface would be accumulated at zero applied voltage (as described in Chapter 2). At this voltage the p-type silicon surface would be depleted. Fermi level pinning has been shown to occur at the silicon-oxide interface and so these interface states may cause a different silicon surface charge to the theoretical values. Figure 6.19 compares p- and n-MIS devices made with a 0.5 minute deposition of SRO. Reproducibility for 0.5 minute samples was poor, values of current per Volt sometimes varied by $\pm 25\%$. This makes the difference observed in the C-V curves of Figure 6.19 insignificant. However, similar comparisons were made for other SRO deposition times. In all cases the accumulation capacitance was higher for the p-type devices. These results are summarised in Figure 6.20.

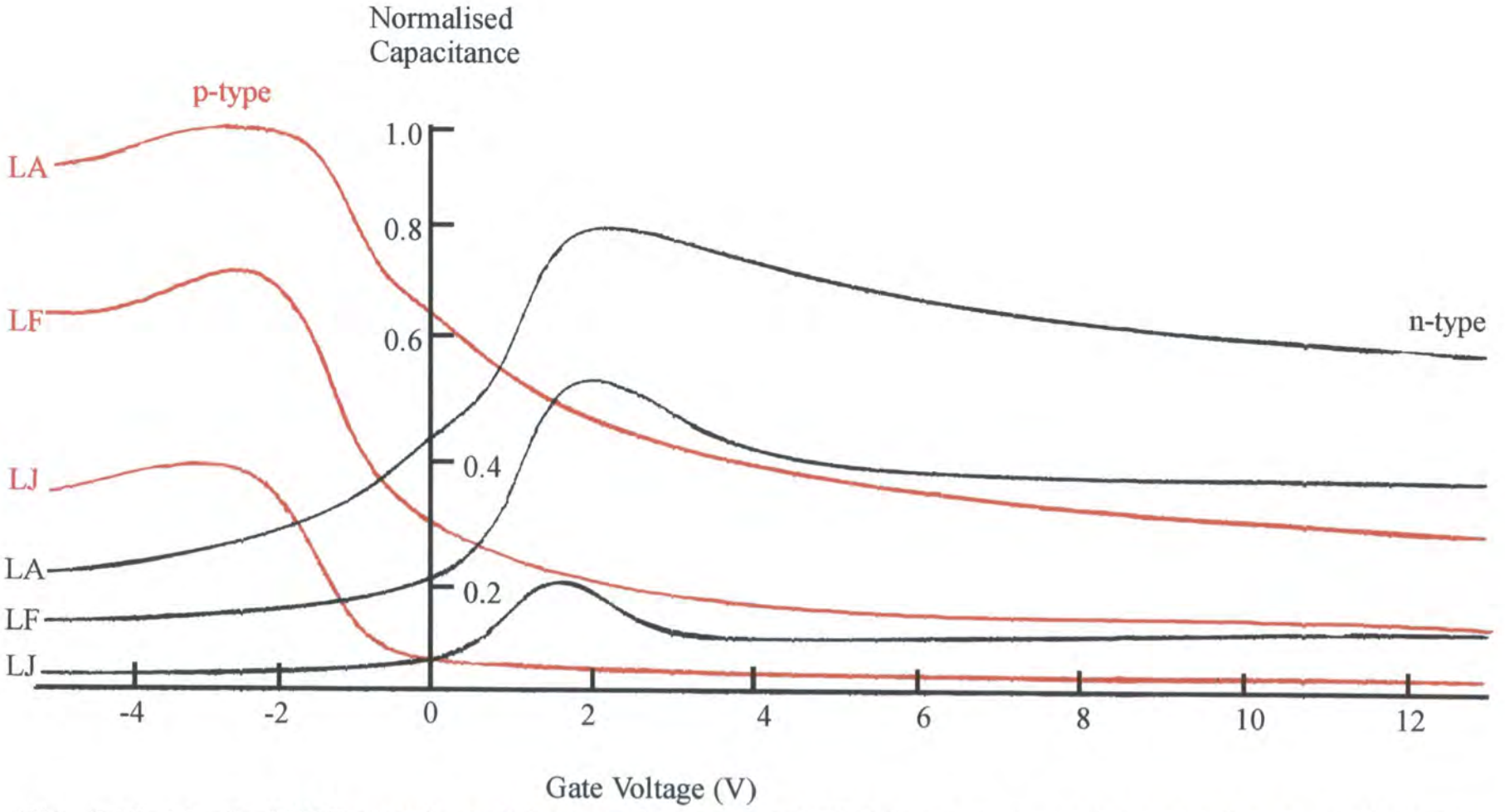


Fig 6.19 Identical SRO growth conditions used to produce MIS devices on n – and p-type substrates with aluminum as the gate electrode. The SRO growth conditions were γ of 0.22, at 650°C in 0.5 minutes. Each C-V curve was scanned in 4s using a 1 MHz signal.

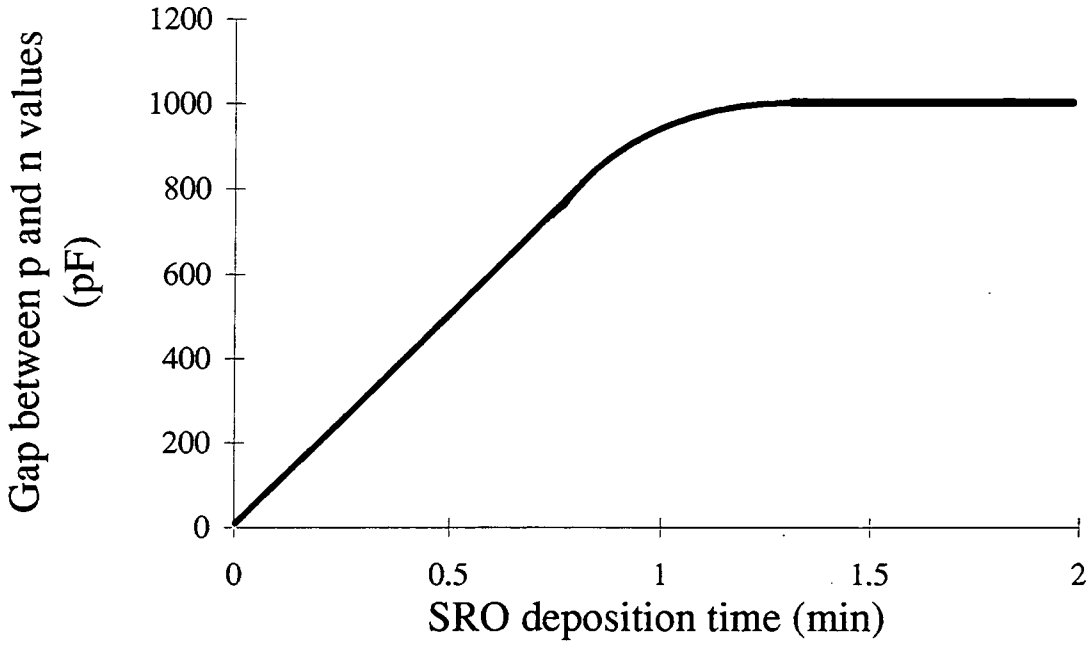


Figure 6.20 A plot of the gap between the p- and n-type accumulation capacitance values versus SRO deposition time.

Comparisons showed that the difference in capacitance values was smallest for an SRO deposition of 0.5 minutes. Beyond one minute the difference was constant. This suggests that the silicon-oxide interface has negligible effect on the capacitance values.

Films grown in one minute or more possess some property which enables the p-type devices to store more charge than the n-type devices. This property could be caused by fixed oxide charges. The structure of the SRO film was described in Chapter 5. Thin SRO layers, grown in 0.5 minutes, are very silicon rich, in places, columns or dendrites of silicon traverse the SRO film. As deposition time increases the silicon breaks up into smaller and smaller areas. Eventually the silicon is nanocrystalline. There may be two interfaces to consider for this type of film: the first at the wafer-native oxide interface; and the second at the crystalline silicon-silicon oxide interface. Once the columnar silicon breaks up, dangling bonds and traps are present. Samples deposited in more than 0.5 minutes would have a higher number of traps. Extending this argument to thicker samples, the number of traps increases with oxide thickness. However, the results in Figure 6.20 show that the gap between p- and n- accumulation capacitances does not increase with increasing oxide thickness. Only those traps within 10 to 15 nm of the columnar silicon have an effect on the accumulation charge layer [17].

The oxide charge causes a shift along the voltage axis of a high frequency C-V curve [16]. This voltage shift is measured with respect to an ideal C-V curve. For both n- and p-type substrates a positive charge within the oxide shifts the C-V curve to more negative values of gate bias whereas a negative oxide charge shifts the C-V curve to more positive voltage values. Ideal curves were computed from the standard formulae listed in Table 6.1. Figure 6.21 shows a comparison between the ideal C-V curve and the experimental curve for device LA with a top contact of aluminium and an SRO layer of 427 nm deposited in two minutes on a p-type silicon substrate. The difference in the shapes of the two characteristics shows the non-ideality of the SRO devices. At all biases the capacitance of the device is below that of the ideal curve. This is due to the SRO layer allowing charge to leak through it, as discussed in previous sections of this Chapter. In most plots it was difficult to determine any flatband shift [16] because of the relative differences in the magnitudes of the real and ideal capacitance values. Figure 6.21 shows a shift to more negative biases and therefore suggests a positive oxide charge. This positive oxide charge could repel holes and so cause the higher turn on voltage observed for p-type devices. This may also impede hole flow across the SRO and so cause the higher accumulation capacitances

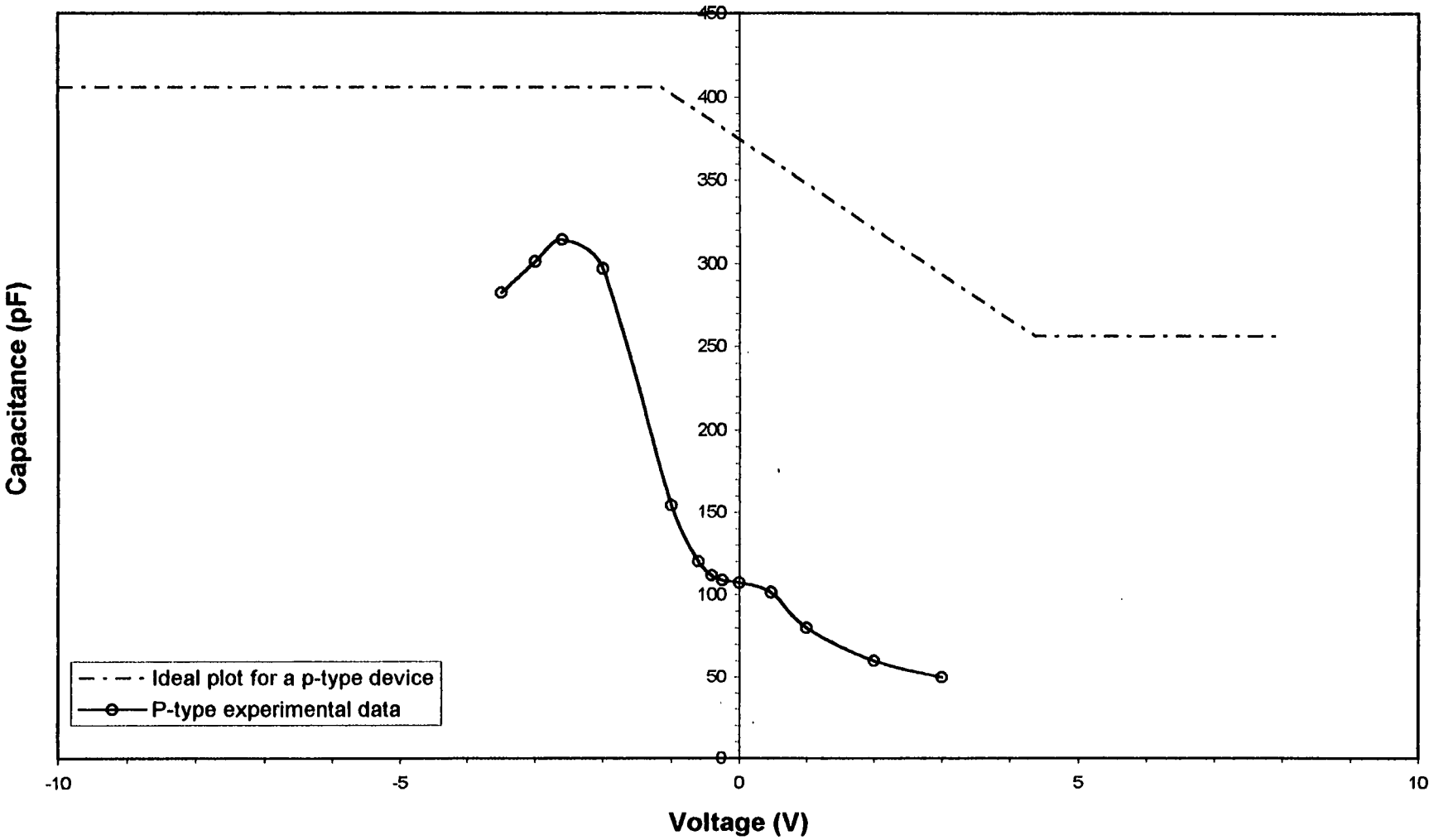


Figure 6.21 Plots of the ideal and experimental C-V curves for device LA on a p-type substrate with aluminum as the gate electrode. The SRO growth conditions were γ of 0.22, at 650° C in 2.0 minutes.

Parameter	Formula
Maximum depletion width	$w = \sqrt{\frac{4\epsilon_s kT \ln(N_A/n_i)}{q^2 N_A}}$
Minimum capacitance	$C_{min} = \frac{\epsilon_{ox}}{d_{ox} + (\epsilon_{ox}/\epsilon_s)w}$
Accumulation capacitance	$C_{ox} = \frac{\epsilon_{ox} A_{ox}}{d_{ox}}$
Capacitance at flatband	$C_{FB} = \frac{\epsilon_{ox}}{d_{ox} + (\epsilon_{ox}/\epsilon_s)\sqrt{kT\epsilon_s/q^2 N_A}}$
Threshold voltage	$V_T = \frac{\sqrt{2\epsilon_s q N_A (2\phi_B)}}{C_{ox}} + 2\phi_B$

Table 6.1 Standard formulae used to compute the ideal C-V curves [16]. k is Boltzmann's constant, T is temperature, q is the electronic charge, ϵ_s and ϵ_{ox} are the permittivities of silicon and SRO, respectively, d_{ox} is the thickness of the SRO film, A_{ox} represents the area of the device, N_A is the doping density, n_i is the intrinsic carrier concentration and ϕ_b is the potential within the bulk of the silicon.

observed in p-type devices.

6.11 Effect of temperature on I-V characteristics

The temperature dependence of the ramped I-V curves for SRO was investigated in the range $< -55°$ C to 20° C. Typical I-V characteristics for SRO MIS devices are shown in Figure 6.22. This graph shows the I-V characteristics at 10° C, 5° C, 0° C, −5° C, and −45° C. As temperature increases both forward and reverse currents increase. The higher the temperature the more marked the difference in conductivity. This behaviour was observed for all devices on all wafers.

In reverse bias, the higher the temperature, the lower the voltage which causes the saturation current level. For example, at 10° C the reverse current for samples deposited in 1 minute is more or less constant at −0.25 V, whereas at −45° C even at −2.5 V saturation current has not been achieved. Saturation is therefore a current-limited rather than a voltage-limited phenomenon. This change in the reverse bias conductivity with temperature has implications for the SRO MISS device. It would

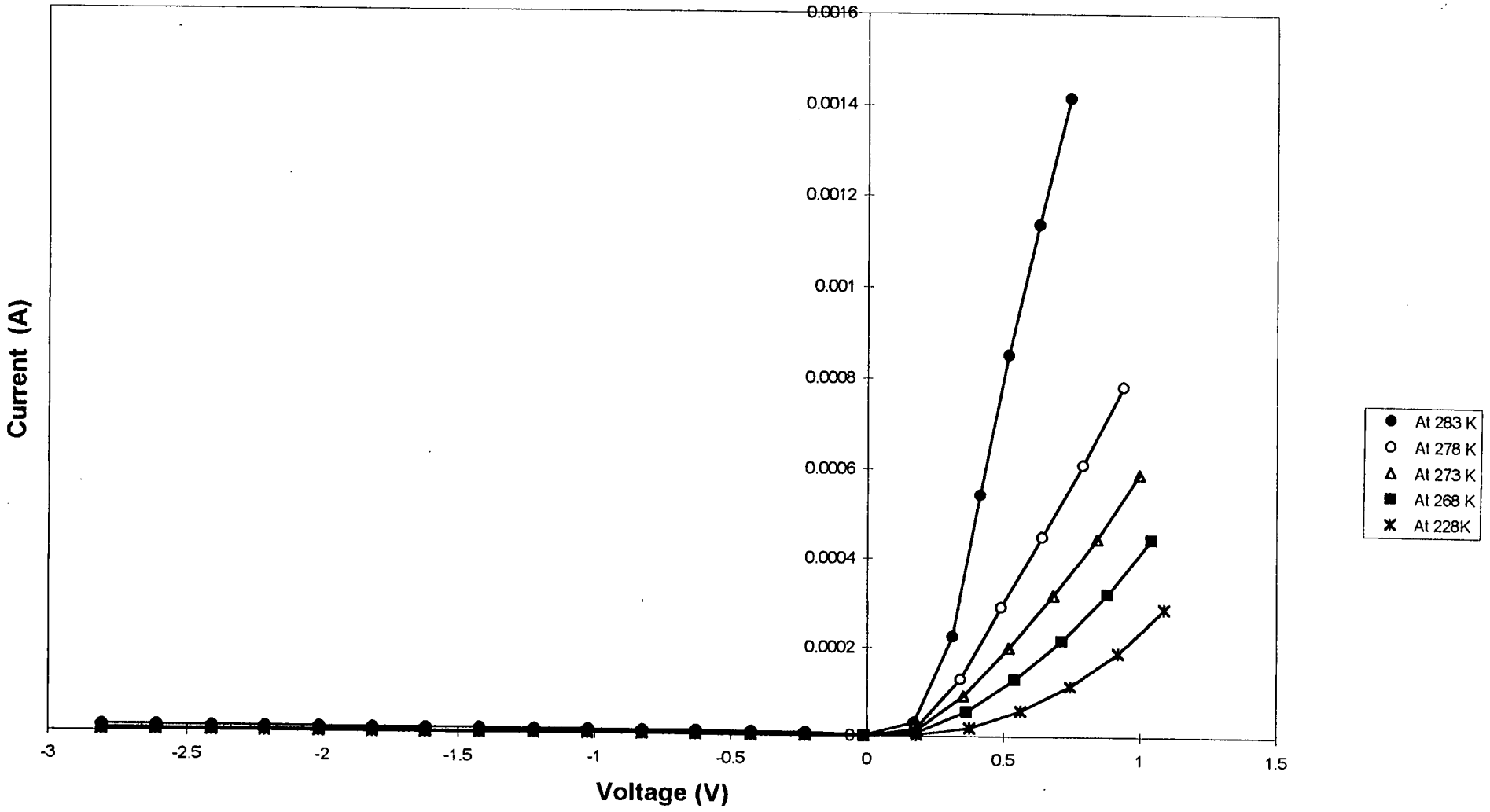


Figure 6.22 Plots of current versus voltage at various temperatures for device LA on an n-type substrate with aluminum as the gate electrode. The SRO growth conditions were γ of 0.22, at 650° C in 1.0 minute.

prove to be unstable if operated over a wide range of temperatures.

An MISS switch consists of a metal, an insulator, a semiconductor (the S_1 layer) and finally another semiconductor (the S_2 layer). The off-state of the MISS has been found to correspond to deep depletion of the S_1 semiconductor layer. The on-state has been found to correspond to inversion of the S_1 layer. As temperature increases more electron-hole pairs would be generated in the silicon. The increased current causes more voltage to be dropped across the oxide and pn junction, which in turn causes more current to flow. When the rate of hole flow to the SRO-Si interface is higher than that through the oxide the conductivity is oxide-limited rather than semiconductor-limited and this is the low impedance state. With increased temperature the switching point would occur at different voltage values.

If the MISS device were used at 10° C the reverse bias MIS current is more or less constant for all voltages higher than -0.25 V. If the MISS device were used at -45° C the reverse bias MIS current is lower and climbs over two orders of magnitude between 0 and -3 V. A higher negative voltage would be needed to cause the current to be oxide-limited. This would mean a change in the switching voltage. The lower the temperature the more negative the switching point.

The I-V curves tend to be parallel but shifted to higher levels of conduction with increased temperature. There is no dependence of the temperature variation of the conductivity with electric field, i.e. the temperature shifts the current to higher levels at all electric fields. There is also no pronounced dependence on film thickness, i.e. all thicknesses are affected equally by temperature changes. The I-V characteristics showed that there was no strong dependence of the temperature variation of conductivity with metal electrode. There was no strong dependence on substrate resistivity or dopant species.

Figure 6.23 shows two identical p-type devices at 0.5 V in forward bias. The temperature was increased by 100° C and the dark current increased by six orders of magnitude. This effect is at least 3.5 times greater than most other reported results [6, 7, 8, 9, 10, 12], probably due to the higher excess silicon in the Durham films. The dark currents show an exponential temperature dependence (i.e. $\ln I \propto T$), as shown in Figure 6.23. There are two straight lines. This could mean that two activation energies for two different conduction mechanisms could be involved. Temperature effects are useful for the separation of similar conduction models and so will be discussed in more detail in Chapter 7.

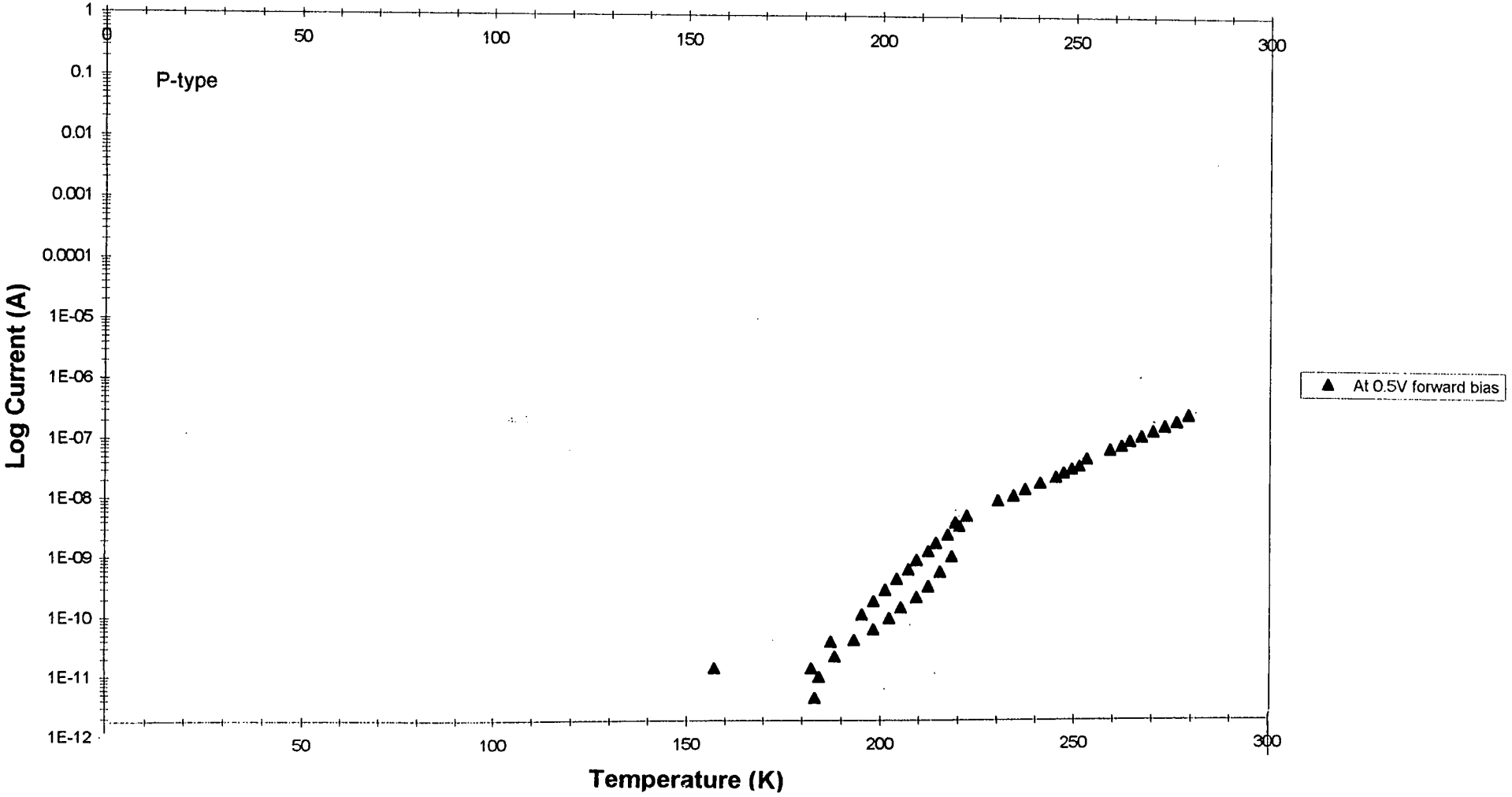


Figure 6.23 The effect of increasing temperature on the dark current for a constant forward bias of 0.5 V, for device LA with an aluminium top contact, on a p-type substrate, with a 4.0 minute deposition of SRO at 650° C and γ of 0.22

6.12 Device breakdown

MIS breakdown strengths are typically $100\,\mathrm{MV\,m^{-1}}$ ($1\,\mathrm{MV\,cm^{-1}}$). Some MIS structures have been found to withstand $10\,\mathrm{MV\,cm^{-1}}$. These SRO films must be relatively defect-free, since it is usually through defects that breakdown occurs. Most reported films conduct lower currents, are more resistive and have higher percentages of oxygen than the films grown here. Increased oxygen content is usually associated with increased disorder and therefore defects, but much depends on the method of film deposition. Increased resistivity means that higher fields are required to reach the critical current limit required for breakdown.

Typical forward breakdown fields are $2 \times 10^6\,\mathrm{V\,m^{-1}}$ or $2 \times 10^4\,\mathrm{V\,cm^{-1}}$. In reverse bias fields of the order of $100\,\mathrm{MV\,m^{-1}}$ or $1\,\mathrm{MV\,cm^{-1}}$ are typical. The field in forward bias is most accurate since, as discussed in Chapter 2, most of the applied voltage is dropped across the oxide layer. In reverse bias, part of the applied voltage is dropped across the depletion width of the semiconductor. In both cases the field is only the average value and is much lower than the actual value. If the silicon particles in the SRO are assumed to drop negligible voltage, then the voltage is dropped across the intervening oxide layer. The breakdown voltage is lowest for thinner SRO films, the breakdown field strength decreases with film thickness and the relationship between film thickness and breakdown voltage is not linear. This is expected because there is an increase in oxygen concentration with film thickness and therefore an increase in the number of defects and a decrease in the silicon crystallite size [10].

Breakdown occurs at lower field strengths for higher temperatures. This suggests that breakdown is a current-controlled phenomenon. The current-voltage breakdown characteristics are parallel but are shifted to higher levels of current per Volt with increasing temperature. Often breakdown in MIS devices is accompanied by self-healing. The power generated by the high breakdown currents is sufficient to melt the aluminium. Evaporation may occur leaving a hole in the metal surface. This process removes the path of least resistance and causes a lower current to flow per Volt on the next I-V cycle. A higher breakdown field is, therefore, required. Figure 6.24 is a sketch of the resultant I-V characteristics. Higher temperatures decrease the breakdown voltage and successive breakdowns increase the breakdown voltage. Figure 6.25 shows these two opposing phenomena for an MIS device with n-type substrate, the SRO layer was deposited in 2 minutes and an aluminium electrode evaporated on the top.

For breakdown strengths to be compared between samples only the first breakdown at one temperature can be used. This temperature was chosen to be $-100\,^\circ$ C and was

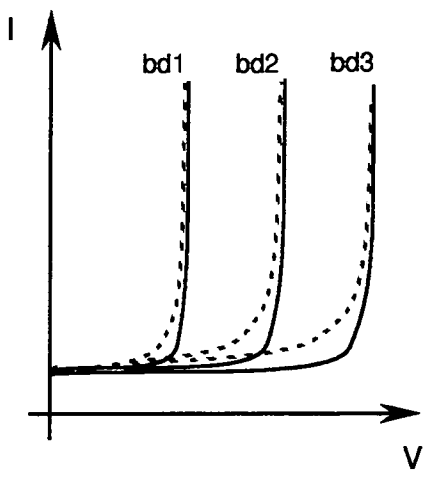


Figure 6.24 A sketch of typical breakdown hysteresis.

obtained by pouring liquid nitrogen into the coolant container and allowing the device chamber to warm to $-100\,^{\circ}$ C. To measure the breakdown strength, the ramped I-V characteristics were obtained, for a range of devices, of various SRO film thicknesses, on p- and n-type substrates. The maximum current flow was limited to 2 mA, by the ammeter and by the software. When the current reached this value, the voltage was immediately reduced and ramped down to zero volts. The observed hysteresis suggests that breakdown had occurred. This may also be accompanied by permanent charge trapping within the oxide.

The p-type devices were in general less conductive than the n-type devices and therefore higher breakdown fields were required. In Chapter 2, the theoretical maximum depletion width was calculated for each substrate. P-type devices were estimated to have a 33% larger depletion width. Since the depletion width was smaller in n-type devices, the electric field was higher and therefore, a lower breakdown voltage was required.

The breakdown requirements of the SRO layer can be tailored to meet the specifications required by the MISS device. Higher breakdown strengths can be achieved by manufacturing the MISS device with the p-type layer next to the SRO film. The bias for the low impedance state of the MISS devices is limited by the oxide breakdown strength. SRO film thickness and therefore the deposition time are important factors.

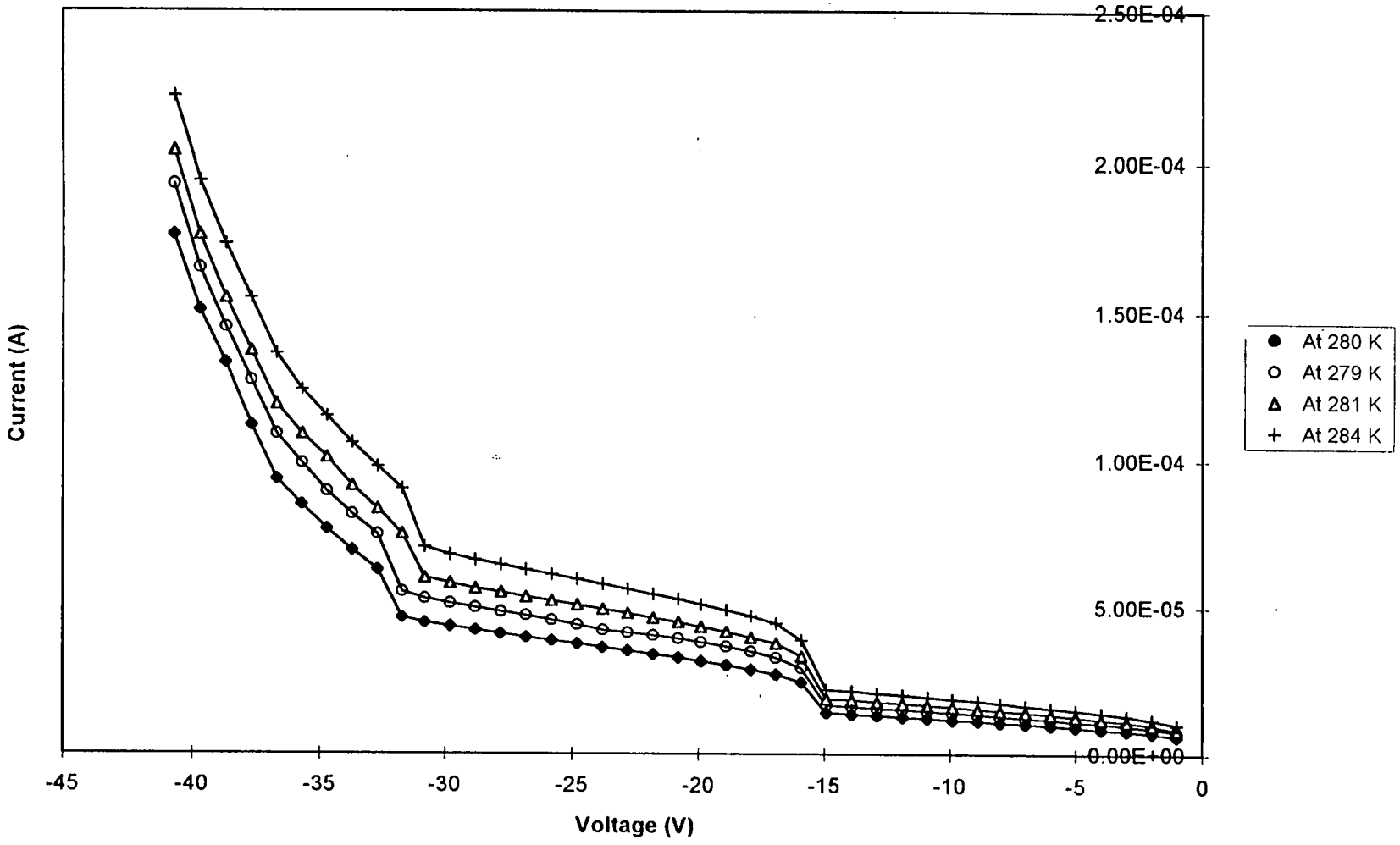


Figure 6.25 Reverse breakdown cycled I-V characteristics for device LA at various temperatures. The device was manufactured with an aluminium evaporated onto 2 minute deposition of SRO on an n-type substrate

6.13 The effect of annealing

6.13.1 Introduction

The purpose of this section is to make comparisons between the electrical properties of the as-deposited SRO samples with those of the annealed samples. A summary of the electrical characteristics and how they change when the material is annealed is given. This may shed light on the importance of the precise structure of the film. However, the process of annealing may cause a number of counter-acting changes, discussed in more detail later, which make the result of the anneal more difficult to predict.

The precise details for the annealing process were given in Chapter 4. All samples were grown on n-type wafers, which were cleaved into quarters, cleaned, and placed in the APCVD reactor simultaneously. SRO deposition was carried out at 650° C, with the reactant gas flow ratio, γ, fixed at 0.22, in 2 minutes. Of the four quarters, one was used for thickness and composition analysis, one was processed normally and two underwent the extra step in the nitrogen annealing furnace for two or four hours before the evaporation of the top contact.

Hamasaki *et al* discovered that the annealing process involved two stages. In the first stage the tiny microcrystals of silicon melted. This happened within the first 5 minutes and for this stage temperature was very important. In the second stage the microcrystals migrated towards each other. A gradual rate of crystal growth was observed. Therefore time was important for the second stage. The crystal growth in SRO is therefore diffusion controlled and the intergranular oxide has been found to dominate the self-diffusion of silicon during the annealing process. Higher oxygen concentrations must either inhibit the diffusion of the silicon atoms and/or increase the diffusion path length required for crystal formation. Recently, researchers have gained evidence which suggests that silicon crystals precipitate out until the remaining matrix reaches SiO_2 [21, 22]. The resulting SRO is more dense [23] and therefore the thickness of SRO reduces. This could be due to the formation of SiO_2 but could also be caused by the reduction of voids within the film.

There is a minimum temperature and excess silicon content, necessary for crystallisation of the silicon clusters [21, 24]. Where the oxygen concentration exceeds the silicon concentration, Nesbit [24] discovered that a minimum temperature of 950° C is needed to form silicon clusters. For films with a silicon to oxygen ratio greater than 1, the minimum temperature required was 800° C. Where these conditions are

not met silicon clusters may still grow, but are thought to be amorphous. Crystal size has been found to be very strongly dependent on the temperature of the anneal and only weakly dependent on the anneal time [19].

Crystal size is unique to the SRO film composition and to the annealing conditions. For this work Nesbit's criteria were met since the samples were annealed at 1000° C for two or four hours.

6.13.2 Forming investigations for annealed SRO MIS devices

All samples were 'formed' at 0.8 V as described earlier in this Chapter. The formed dark current-time characteristics were very flat and stable with time, whether the samples were annealed or not. Formed dark currents were higher for annealed samples in forward bias at -0.8 V. There was no consistent difference for samples annealed for two as opposed to four hours.

6.13.3 I-V characteristics

Like the as-deposited SRO MIS devices, the annealed film devices showed negligible edge effects. Therefore, there was no dependence of J versus $\mathcal{E}$ on area, perimeter or A/P for either gate polarity. In general, at low fields the unannealed samples required smaller gate voltages for the same current flow, in both forward and reverse bias. The precise curve varied from device to device on the annealed wafers but there was a consistent reduced polarity dependence, as shown in Figure 6.26. Figure 6.26 shows the current-voltage comparisons for device RH on a wafer annealed for 4 hours with an unannealed wafer. As can be seen in Figure 6.26, annealed samples sometimes conducted more than unannealed samples, and sometimes conducted less, depending on the size of the voltage in forward bias, but always showed a less curved, more linear characteristic, especially in reverse bias. In general, at low fields annealed samples conducted less than the as-deposited samples and at high fields the turn on was more sudden. The interpretation of the changes introduced in the I-V characteristics by annealing is complex. Annealing has been found to cause structural and electrical changes in SRO. All published research into the annealing of SRO, in inert gases such as argon or nitrogen, reports the production of nanocrystals of silicon within the SRO . These silicon clusters or microcrystallites are described in the literature as the dominant factor for the electrical characteristics of SRO films.

As-deposited CVD films have been found to contain silicon clusters with a diame-

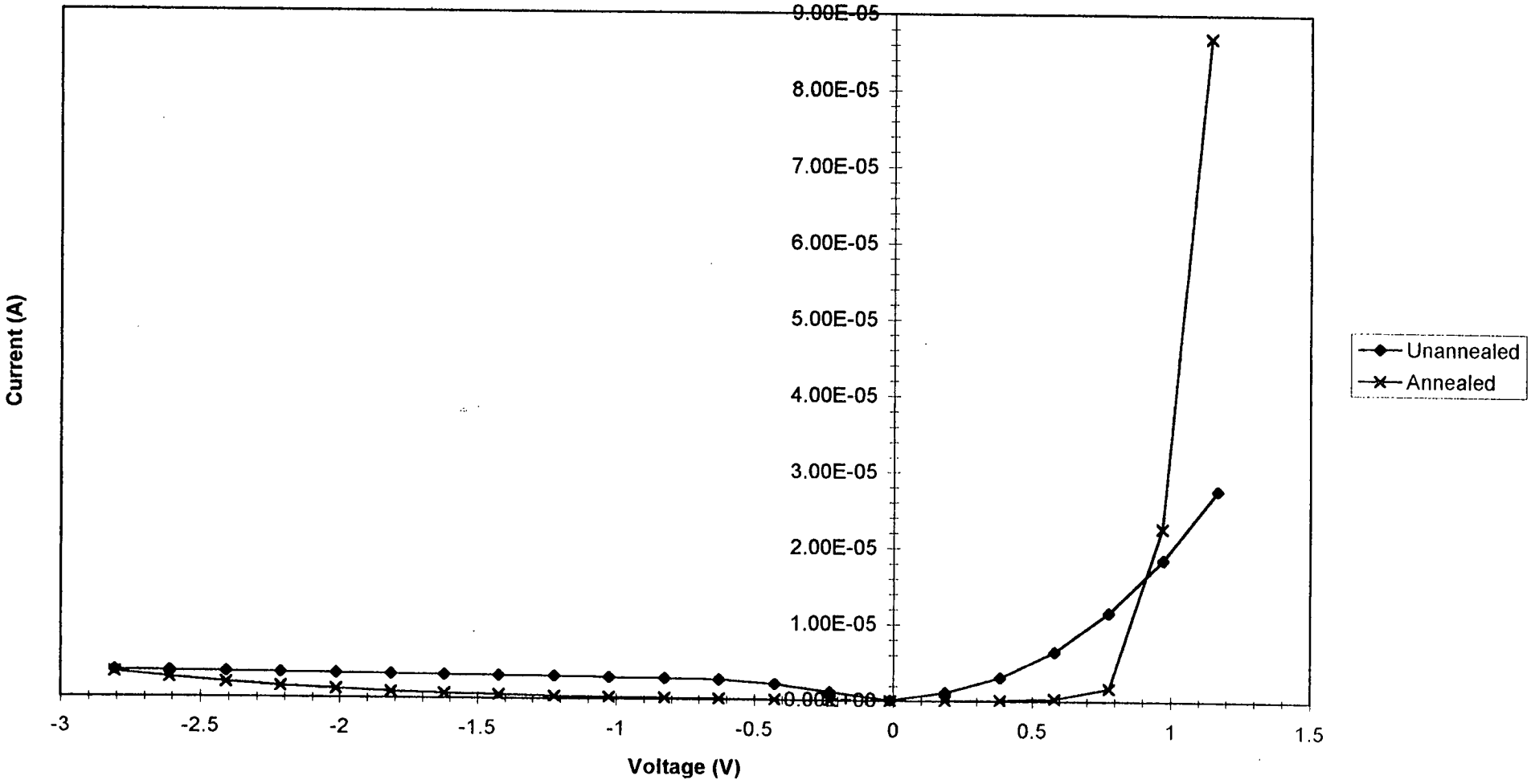


Figure 6.26 A comparison of the I-V characteristics for annealed and as-deposited SRO MIS devices. The SRO was deposited on each wafer in the same APCVD run in 2.0 minutes at 650° C and γ of 0.22.

ter of 1 nm [24]. Electron diffraction patterns do not show the presence of these clusters but instead show a series of diffuse rings, typical of amorphous structures [24, 25]. In general, annealing causes the microcrystals to increase in size. Films grown in the Durham CVD reactor have been shown to exhibit increased order after a nitrogen anneal [25].

Annealing was therefore expected to increase the average size of the silicon grains within the SRO. However, the structural changes brought about by the annealing process may not increase conductivity of the MIS device. If the crystallites are small and closely spaced, tunnel currents may flow through the intervening oxide. These small clusters would have a higher perimeter to area ratio than larger more widely-spaced clusters. The interface between the crystal and the oxide is disordered and contains traps. Therefore smaller crystallites mean increased numbers of traps within the film. Larger more widely spaced clusters contain less traps but are surrounded by a longer oxide path length. Smaller fields are expected to be dropped across the larger silicon crystals and therefore higher fields should be developed across the oxide. Increased fields across the oxide and reduced numbers of electron traps should enhance current flow but increased oxide path length may counteract this effect by reducing tunnel currents.

The SRO grown here is a composite material. The as-deposited microstructure, described in Chapter 5, consists of silicon which gradually changes to an amorphous mixture of elemental silicon, silicon oxides and silanol. Increased oxygen concentration has been found to decrease silicon grain size [26]. The oxygen content of the film increases with distance away from the substrate surface. Therefore this variable composition means that the silicon crystals vary in size. Those near the silicon substrate are much larger than those near the top contact metal. The large crystals at the silicon surface may serve to increase the effective substrate depth and it may be that the more resistive microcrystalline section of the SRO film, dominates the conduction.

Annealing may also cause other changes. Many authors have found that annealing inadvertently caused oxidation of the SRO film [27]. This resulted in a more resistive layer. Annealing may also cause changes at the SRO interfaces between the film and electrode or the silicon substrate and this also makes the effect of annealing difficult to predict. The work of Burte and Schulze [28] showed that annealing caused a decrease in the effective interface charge density at the silicon-SRO interface and caused a change in the sign of the charge up to 700° C. An increase in the effective positive charge resulted when the identical aluminium-SRO-silicon samples were annealed at

900° C.

In summary, annealing increases silicon grain size which may or may not increase conduction, may cause oxidation of the film which decreases conduction, reduces voids which increases conduction and may cause changes in the SRO-electrodes interface charge layers.

The annealing furnace has been found to inadvertently cause oxidation of the SRO films [27] and also to cause increased order [25], thought to be associated with the growth of silicon crystallites. The random structure of SRO is thought to contain many voids. Void reduction has not been investigated but is likely to occur during the anneal. Figure 6.26 shows a reduced conductivity in both forward and reverse biases. This suggests that the SRO film has become more resistive and therefore it may be that oxidation of the film dominates over the other phenomena. The device switches on more suddenly after the anneal. This could be caused by a reduced negative interface charge. Such an effect has been observed by Burte and Schultz [28]. A lowering of the interface charge and increased resistance of the SRO causes more potential to be dropped across the SRO film and hence a more ohmic characteristic may result.

Reverse breakdown

In reverse bias annealing showed a marked difference in the I-V characteristics. This is shown in Figure 6.27. Figure 6.27 shows that the device RH does not begin to turn on, in reverse bias, until the applied voltage exceeds 20 V. Both the annealed and unannealed devices have this voltage in common and therefore both have the same potential barrier to overcome. Once this barrier is overcome the annealed devices quickly reach saturation and breakdown occurs. The as-deposited devices, however show an ohmic response to increasing voltages. This linear relation continues beyond 40 V, which is double the breakdown voltage of the annealed sample.

A possible explanation for the difference in the characteristics comes from the work of Burte and Schultze [28]. Annealing altered the balance of positive and negative interface charges in their SRO samples. Annealed samples show a lower breakdown strength. If the negative charge increased, or the positive charge decreased, more holes would be attracted to the interface, the depletion width would reduce and the effective field would increase. Less of the applied voltage is dropped across the silicon depletion width and more is dropped across the SRO film. This increases the conductivity of the device.

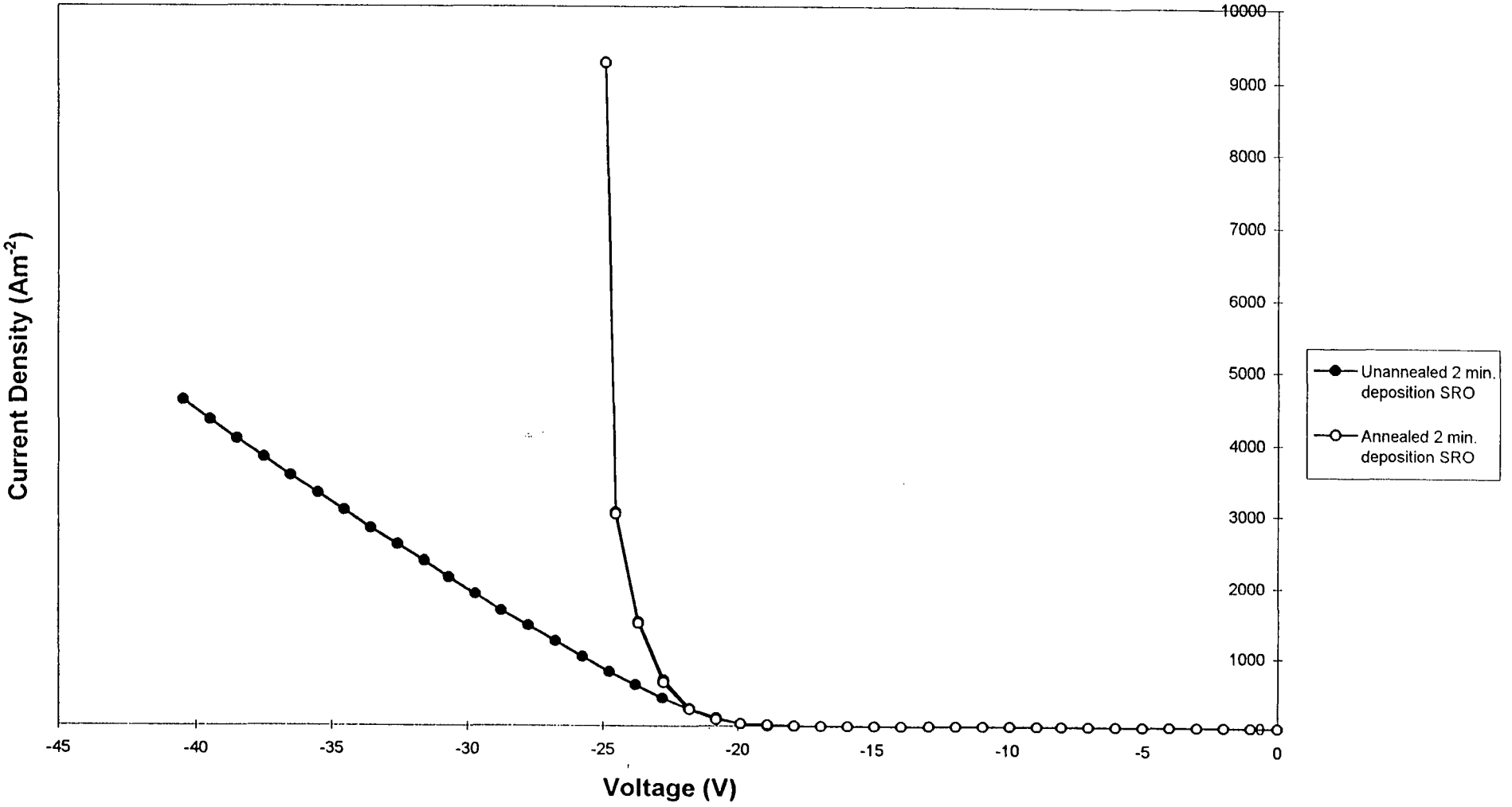


Figure 6.27 A comparison of the reverse bias I-V characteristics, at 207 K, for annealed and as-deposited SRO MIS devices. The SRO was deposited on each wafer in the same APCVD run in 2.0 minutes at 650° C and γ of 0.22.

The ohmic region displayed by the as-deposited samples in Figure 6.27 could mean that the breakdown is oxide limited. Once the initial barrier is overcome, increased voltage appears across the film, more barriers are lowered and the current increases. The origin of the initial barrier could come from the charges at the interfaces. Any extra voltage causes the breakdown of potential barriers in the oxide layers between silicon crystallites.

6.14 Recommendations for MISS devices

A forming treatment is recommended for MISS devices with SRO as the semi-insulator. One of the factors that can easily be controlled in MISS devices is the size of the electrode area. This controls the current magnitude. Interface states at the silicon-oxide interface outweigh the effect of changing the top electrode. Aluminium was found to be the best contact in MIS device manufacture and is recommended for MISS device manufacture. This limited study suggests that substrate resistivity should have little effect on MISS device parameters. This contrasts with published research [13, 14], which has shown that as doping density increases the switching voltage, switching current and holding current are reported to decrease. The effect of substrate resistivity is thought to be relatively unimportant in the MIS devices manufactured at Durham because of the high number of interface states at the silicon-oxide interface. These outweigh the effect of changing substrate resistivity. The change in the reverse bias conductivity with temperature, for the SRO MISS device, would make it unstable, if operated over a wide range of temperatures. Wide temperature changes would alter the switching voltage. The lower the temperature the more negative the switching point.

MISS devices with thinner oxides have higher switching voltages. The SRO film thickness can be controlled by altering the deposition time and so devices can be manufactured with specific switch on voltages. The bias for the low impedance state of the MISS devices is limited by the oxide breakdown strength. This is also related to film thickness. Higher breakdown strengths can be achieved by manufacturing the MISS device with the p-type layer next to the SRO film.

Annealed MIS devices have lower breakdown voltages. This suggests that it is better not to anneal the SRO films. Annealed devices switch more suddenly than the as-deposited devices and therefore it may be advantageous in some applications. Most published work concerns annealed films. The anneal is carried out to increase

stability of the electrical characteristics of the MISS devices. The films grown at Durham have proved to be stable without the anneal. MISS devices have been grown at Durham which switch without the annealing step in their manufacture [27]. It is recommended, therefore, that the anneal not be carried out.

6.15 Summary

This Chapter provided an estimate for the reproducibility of the MIS devices manufactured at Durham. Edge leakage effects have been shown to be negligible. Current flow was found to increase with device area. Forming effects were measured and an explanation offered, in terms of permanent charge trapping, for the slight increase in current, observed with repeated applications of a constant d.c. voltage. Although a temperature forming process was found to be necessary for these test devices, this stage would probably not be required in MISS devices, in normal use. Measurements were made to establish the time dependence of the currents, to observe any long term transients associated with the capture or release of electrons from traps. Currents were found to be steady. Once the device had been formed the currents were repeatable.

Typical current-voltage (I-V) characteristics and capacitance-voltage (C-V) characteristics have been given for a range of device parameters. Conduction in thin films of SRO was found to depend on film thickness. The top contact metal was found to be relatively unimportant. Fermi level pinning is thought to occur at the silicon-oxide interface. Although, aluminium showed no electrical advantage it did have some physical and chemical properties which made it a good electrode for the Durham SRO MIS/MISS devices.

MIS devices with p- and n-type substrates were investigated. Substrate resistivity was not found to be a significant factor in determining the conductivity of the MIS devices. The p-type devices were in general less conductive than the n-type devices and therefore higher breakdown fields were required. The I-V curves suggest that p-type devices have a higher barrier to overcome in forward bias. Once this barrier is overcome the device turns on quickly and conducts like the n-type devices. The C-V curves show that p-type devices are more accumulated than n-type devices. The higher barrier to conduction in p-type devices could have caused the charge to leak away more slowly. The surface would then be more accumulated. This is thought to be caused by a positive oxide charge. The lack of a strong current dependence on

SRO film thickness, electrode material, or substrate resistivity suggests that interface charges could be the dominant factor in determining conduction in SRO.

There is no dependence of the temperature variation of the conductivity with electric field. There is also no pronounced dependence on film thickness, i.e. all thicknesses are affected equally by temperature changes. The I-V characteristics showed that there was no strong dependence of the temperature variation of conductivity with metal electrode. The dark currents show an exponential temperature dependence. Most current versus temperature plots show two straight lines. This could mean that two activation energies dominate conduction in SRO. The two activation energies could be associated with two different conduction mechanisms, which operate over different temperatures. Temperature response is discussed further in Chapter 7 and is used to determine likely conduction models. Finally, recommendations for the important factors in MISS device manufacture have been identified.

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Chapter 7

Device Modelling

7.1 Introduction

In this Chapter, a Schottky barrier at the silicon-SRO interface is proposed to explain the rectifying behaviour observed in all devices. The current-voltage (I-V) characteristics are linked to the data obtained from structural and compositional analyses and a possible energy band structure for the SRO MIS device is suggested. An estimate of the voltage needed to overcome the Schottky barrier is made and the measured data are corrected, to allow analysis of the current flow through the remainder of the SRO film. Once the Schottky barrier is overcome conduction occurs by a Poole-Frenkel mechanism at low temperatures and by Thermionic emission at high temperatures.

7.2 Electrical measurements

The starting point for the modelling of the conduction processes was the I-V curves, detailed in Chapter 6. The forward and reverse bias currents were similar in value for low voltages. At higher fields, in reverse bias the current saturated at low levels and was thought to be semiconductor limited. In forward bias the currents increased exponentially to much higher levels. In this, the Durham devices were atypical. Other workers [1– 2] report symmetrical characteristics for a wide range of voltages in both biases. This is probably because annealed films were investigated. Most of the work, reported here, concerns as-deposited samples. The rectifying behaviour, observed for the Durham devices, was relatively independent of film thickness, electrode material and substrate dopant species. Therefore, the evidence suggested that the semiconductor-SRO interface dominated conduction in these MIS devices.

Figures 7.1 and 7.2 show the current density, on a log scale, versus voltage (log J-V) plots for devices LJ, manufactured in the same SRO reactor run, one deposited on n-type and the other on p-type silicon. The curves are similar for the two devices. In reverse bias, the plots show a slight increase in the log J values with increased bias. In forward bias, the curves incline steeply at low bias and then more gradually at higher bias. The precise shape of these plots varied from device to device. These examples show straight line regions over a limited voltage range. For other samples, more curved plots were obtained but, basically, the example plots show the pattern of the log J-V response for all the MIS diodes. Rectifying behaviour is clearly apparent. Such plots are often observed in Schottky diodes. At low forward bias, the steeper part of the curve is thought to represent the effect of the Schottky barrier. At higher forward biases the Schottky barrier is overcome and conduction is then limited by the neutral region of the silicon, the SRO film and the metal-SRO interface. The polarity of the log J-V response was substrate dependent. Therefore, it is proposed that two different Schottky barriers were formed. The SRO - n-type silicon formed a Schottky barrier rectifying current in the opposite direction to the SRO - p-type silicon.

A theoretical energy band structure for the SRO Schottky diode is postulated. This model is based on the chemical composition and structural analyses and on the rectifying behaviour observed for all electrical measurements. The MIS data were then further studied to ascertain how closely the Schottky barrier model fitted the observed current-voltage behaviour.

7.3 The Proposed SIS Energy band structure

The energy band structures for Schottky barriers were described in Chapter 2. These are now discussed further, with reference to the MIS structure. This device is dominated by the silicon-oxide interface. At this interface there is a thin oxide layer at one side is the silicon substrate and at the other side is the SRO. SRO is thought to consist of grains of intrinsic silicon, surrounded by traps. Initial SRO deposition has been shown to be in the form of large columns of silicon in an amorphous matrix. The silicon columns are thought to be intrinsic silicon and therefore the substrate-SRO interface is possibly made up of doped silicon, a thin oxide layer and intrinsic silicon. For simplicity, abrupt junctions between the silicon substrates and intrinsic silicon are considered first. Figure 7.3 shows how the the energy bands bend in the intrinsic silicon and in the n- and p-type substrates. Figure 7.4 shows the energy

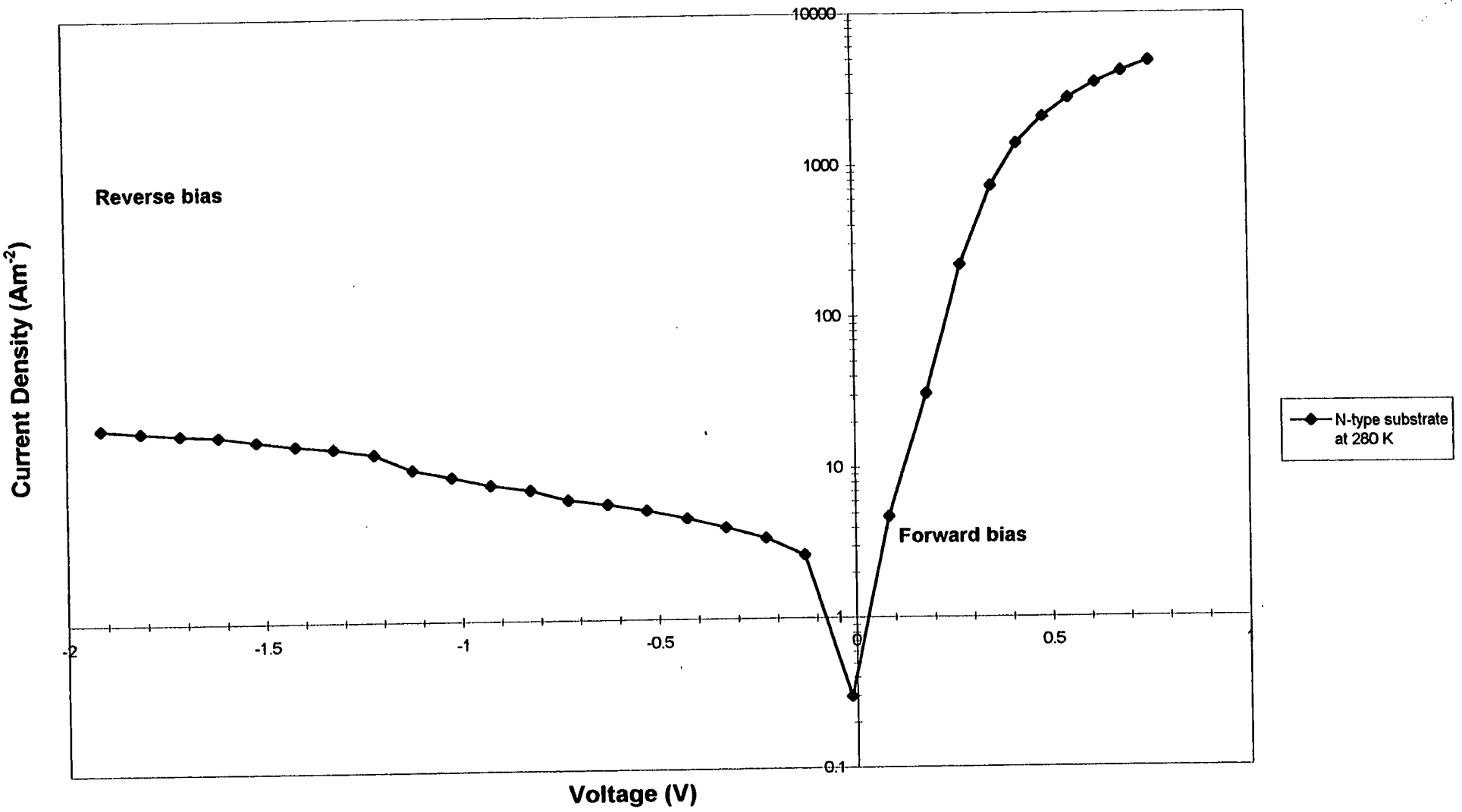

Figure 7.1 A plot of natural logarithm Current Density versus voltage for device LJ with an aluminium top contact, an SRO deposition of 1 minute and an n-type silicon substrate

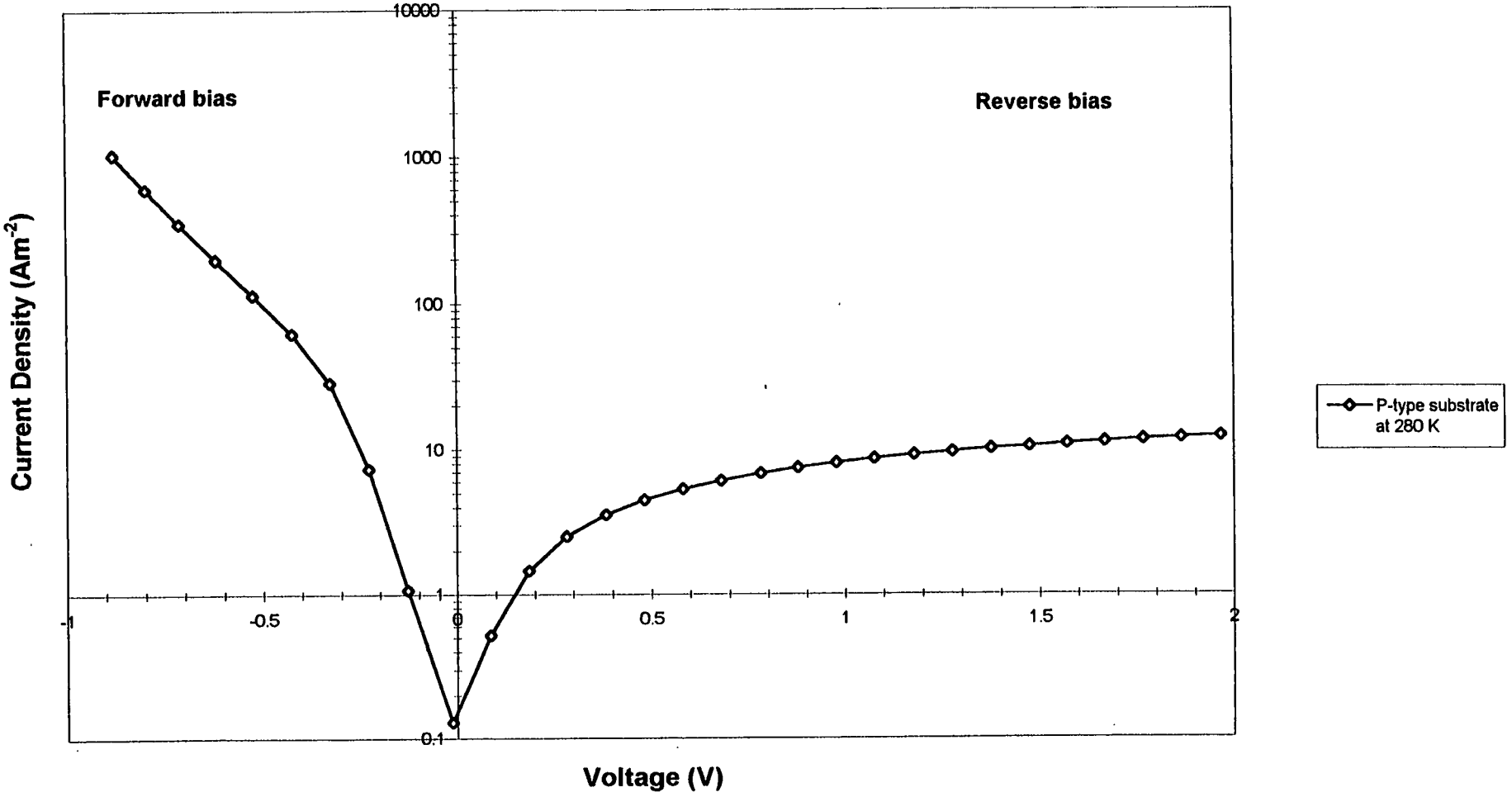

Figure 7.2 A plot of natural logarithm Current Density versus voltage for device LJ with an aluminium top contact, an SRO deposition of 1 minute and a p-type silicon substrate

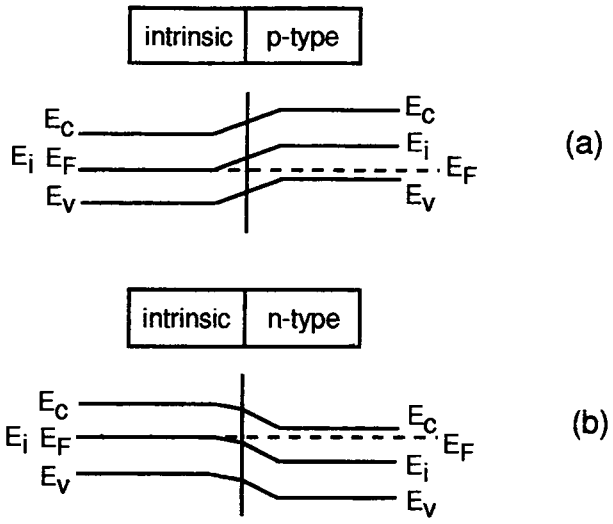

Figure 7.3 The energy band diagrams for intrinsic silicon in close contact with (a) p-type and (b) n-type substrates.

band diagrams for an SIS structure. Once an interfacial layer of oxide is present the band bending in the silicon on either side of the junction reduces. Any applied bias appears across the intrinsic silicon layer, across the oxide and across the substrate. Figure 7.4a shows the silicon-SRO interface structure for an n-type substrate before equilibrium is established. For n-type silicon $q\phi_{si} > q\phi_{sn}$ and for p-type $q\phi_{si} < q\phi_{sp}$. As described in Chapter 2, such differences in work functions produce a Schottky barrier in both n- and p-type devices. Since it is this silicon-SRO interface which is so important in these devices, they may be termed silicon-insulator-silicon or SIS devices. Figure 7.4b shows the silicon-SRO interface structure for an n-type substrate once equilibrium is established. With zero gate voltage, the Fermi levels in the two types of silicon align and band bending occurs throughout the structure. The n-type silicon is depleted. Figures 7.4c and 7.4d shows the silicon-SRO interface structure for an n-type substrate at equilibrium under forward and reverse bias, respectively. The Schottky effect can be seen. In forward bias, the barrier to electron flow from silicon to SRO is reduced, the substrate is accumulated. In reverse bias, the barrier to electron flow is reduced for the intrinsic silicon but the barrier is increased at the substrate. In theory, in forward or reverse bias the barrier from one side of the device to the other is of a similar size but intrinsic silicon has so few carriers that current flow is reduced. The reverse current is, therefore, semiconductor limited. This theory also applies to the intrinsic silicon-nascent oxide layer- p-type silicon devices.

The rectifying nature of all n-type and p-type devices can therefore be explained

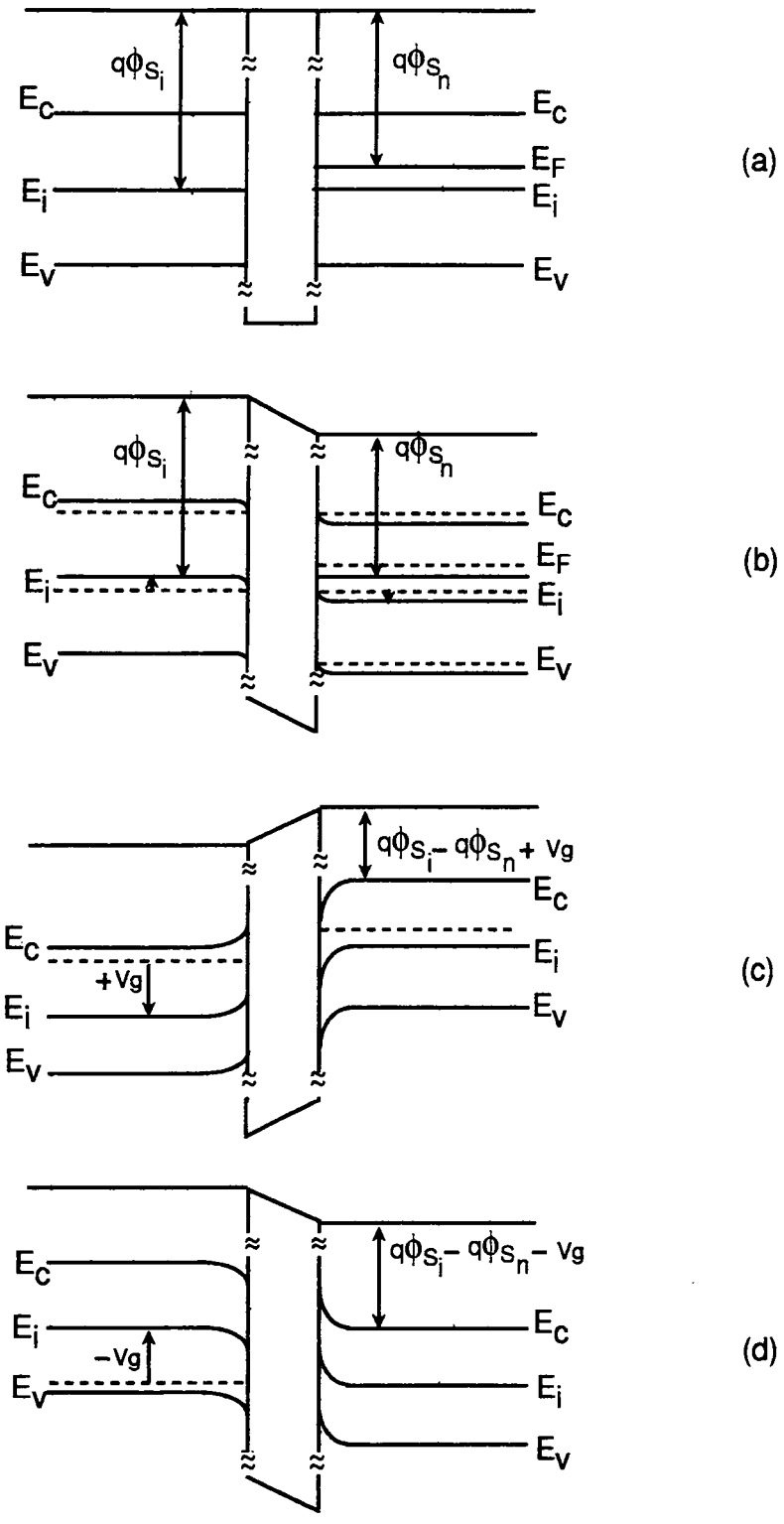

Figure 7.4 The energy band diagrams for an SIS structure consisting of intrinsic silicon, a thin nascent oxide and n-type silicon; (a) before equilibrium is established with zero gate voltage, (b) after equilibrium is established with zero gate voltage (c) in forward bias and (d) in reverse bias.

by a Schottky barrier formed by the close contact of the n- and p-type wafers with the intrinsic silicon, deposited in the early stages of SRO film growth. This model links the structural information obtained in Chapter 5 with the electrical measurements recorded in Chapter 6.

Figure 7.5 pulls together the results of Chapters 5 and 6 and summarises the most dominant conduction mechanism in the SRO devices. The Schottky barrier model is indicated at the substrate-SRO interface.

This structure could explain the rectifying behaviour, observed in all devices, regardless of film thickness, electrode material and substrate type. The current-voltage behaviour was analysed in more detail to assess how closely the Schottky barrier model fitted the experimental data.

7.4 The SIS Schottky barrier properties

7.4.1 Theory

Current flowing across the Schottky diode must cross the depletion region of the semiconductor, a process controlled by drift and diffusion. The electrons are then emitted into the metal by thermionic field emission. In high mobility semiconductors such as silicon, thermionic emission theory is thought to adequately describe conduction in metal-semiconductor diodes [3]. The current density for ideal Schottky diodes is given by [3]

$$J = A^* T^2 \exp\left(\frac{-q\phi_b}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{7.1}$$

where ϕ_b is the barrier height, V is the voltage across the diode and the other symbols have their usual meanings. For $V > 3kT/q$ the last term in the bracket is negligible, and the current density should be proportional to $\exp(qV/kT)$. This ideal behaviour is not observed in practice, but instead the current is usually found to vary as $\exp(qV/nkT)$. The equation for Schottky diodes becomes

$$J = J_0 \exp\left(\frac{qV}{nkT}\right) \tag{7.2}$$

The factor J_0 contains the Richardson's constant, the temperature and the barrier height terms. The factor n represents a measure of how close the ln J-V behaviour is to the theoretical curves. This is often referred to as the ideality factor and is obtained from the gradient of a graph of ln J against V. These data can be used for

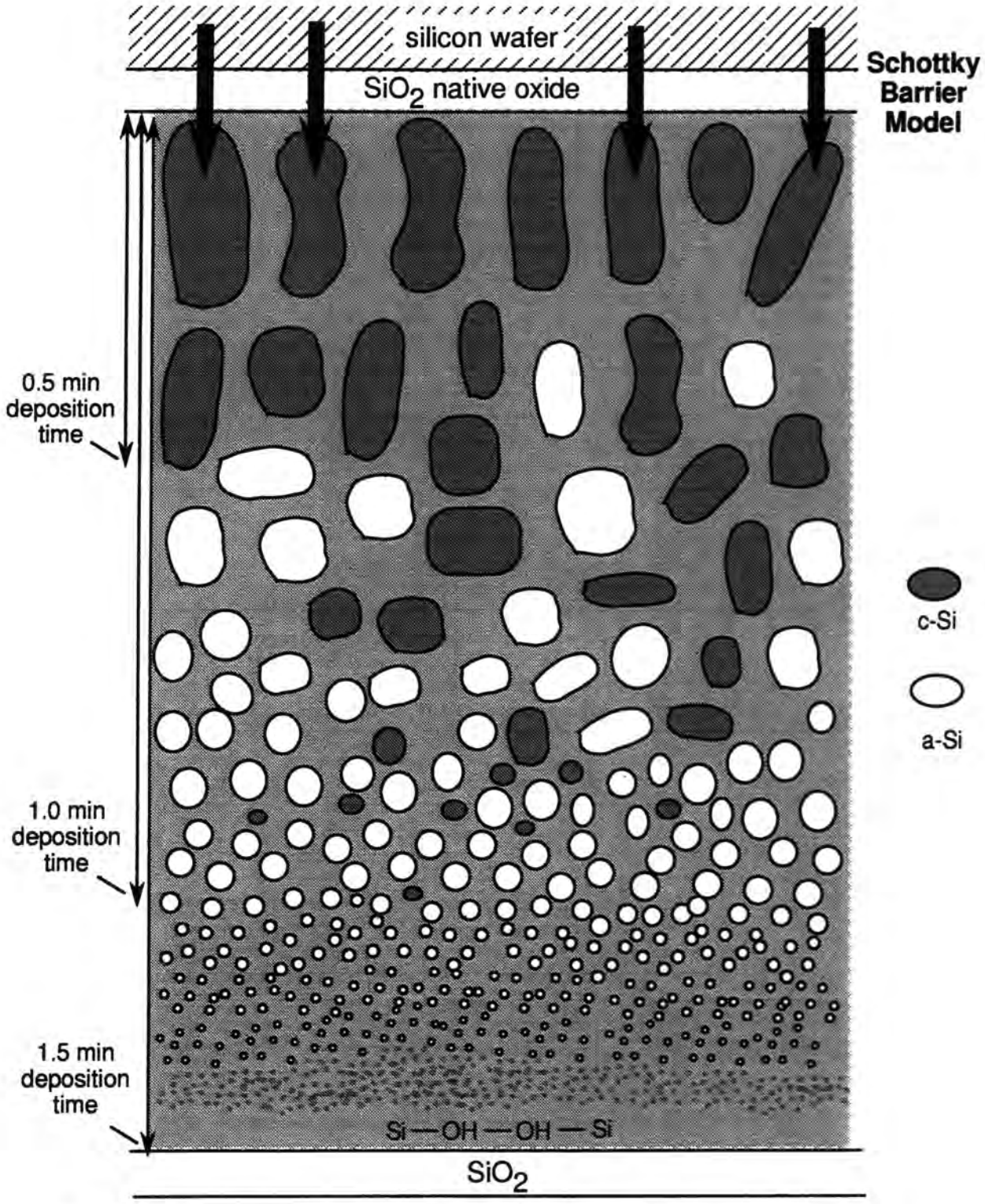

Figure 7.5 The structure of the MIS device and how this links to the Schottky barrier theory for the SIS interface.

barrier height determination, provided that the ideality factor is close to unity.

Rhoderick [3] obtained an expression for the ideality factor of Schottky diodes with thin nascent oxide layers between the semiconductor and metal. The insulating layer had three effects:

(i) The height from the bottom of the conduction band in the semiconductor to the Fermi level in the metal was reduced at zero bias because of the potential drop in the layer. This means that the zero bias barrier height is lower than it would be in an ideal diode.

(ii) The electrons have to tunnel through the barrier presented by the interfacial layer and so the current for a given bias is reduced.

(iii) When a bias is applied, part of the voltage is dropped across the insulating layer so that the barrier height is a function of voltage.

These factors cause the n-value to increase with increasing oxide thickness and the ideality factor was given by

$$n = 1 + \left(\frac{d_{ox}\epsilon_s}{w(d_{ox}qD_s + \epsilon_{ox})} \right) \tag{7.3}$$

where d_{ox} represents the interfacial layer thickness, ϵ_{ox} is the permittivity of the oxide, ϵ_s is the permittivity of the semiconductor, w is the width of the depletion region, D_s is the density of surface states and q represents electronic charge.

7.4.2 Ideality factor

Many ln J-V curves were analysed for n- and p-type devices with various SRO film thicknesses, over a wide range of temperatures. The ideality factors were calculated for the initial, (straight) part of the forward ln J-V characteristics. Some of the data are given in Figures 7.6 and 7.7, which show how the ideality factor varies with temperature for device LJ, with SRO film thicknesses of 25 nm and 200 nm, respectively. In general, the p-type samples had a higher ideality factor than the n-type equivalents. The gap between the two is greatest for the thinnest SRO film devices. As the SRO film thickness increased, the ideality factor changed. For film thicknesses of 200 nm or more the ideality factor values were similar for n- and p-type devices and are summarised in Table 7.1. All of the n-values suggested that the diodes were far from ideal. The ideality factors varied between 3 and 8, with the

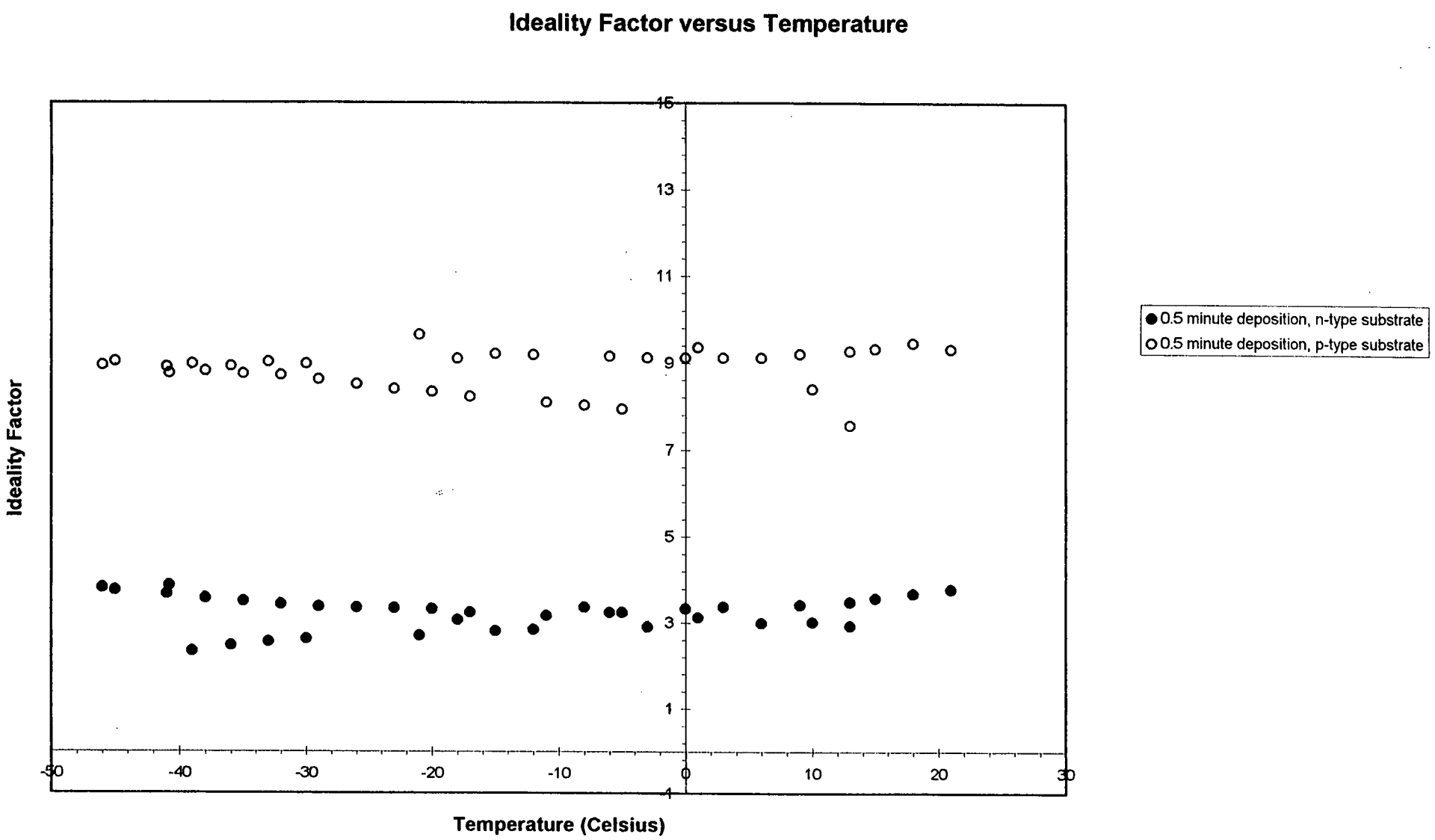

Figure 7.6 A plot of the ideality factor versus temperature for two LJ devices which are identical except for the substrate dopant species. The devices were manufactured with an SRO film thickness of 25 nm and aluminium top contact.

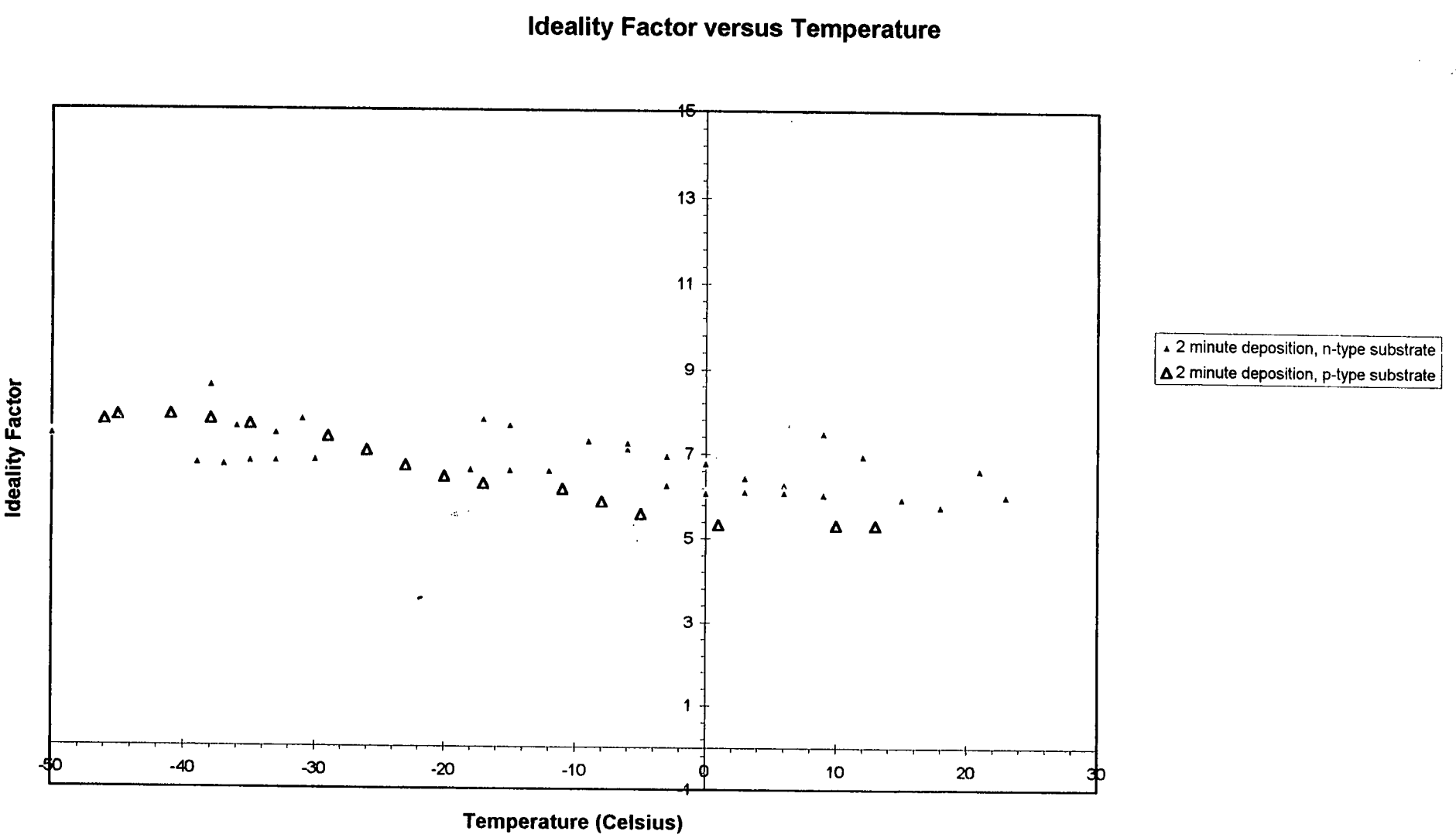

Figure 7.7 A plot of the ideality factor versus temperature for two LJ devices which are identical except for the substrate dopant species. The devices were manufactured with an SRO film thickness of 200 nm and aluminium top contact.

Deposition Time (minutes)	Film thickness (nm)	Substrate	Average Ideality Factor
0.5	25	n-type	3.0 ± 25%
0.5	25	p-type	8.5 ± 13%
1.0	64	n-type	2.5 ± 8%
1.0	64	p-type	6.0 ± 23%
2.0	200	n-type	7.0 ± 11%
2.0	200	p-type	7.0 ± 16%

Table 7.1 Average ideality factors for a sample of SRO MIS devices.

Deposition Time (minutes)	Film thickness (nm)	Substrate	Theoretical Ideality Factor (± 43%)
0.5	25	n-type	1.10
0.5	25	p-type	1.08
1.0	64	n-type	1.10
1.0	64	p-type	1.08
2.0	200	n-type	1.10
2.0	200	p-type	1.08

Table 7.2 Theoretical ideality factors for a range of SRO MIS devices.

thinnest n-type devices showing the most ideal behaviour and the thinnest p-type devices showing the least ideal behaviour. This may be due to the presence of a positive charge within the interface states.

Table 7.1 shows that for each device there was a spread of values for the ideality factor but there is good agreement between all of the p-type ideality factors. The ideality factors for the n-type devices were found to be independent of device area but were affected by SRO film thickness. As the SRO film thickness increases it becomes disproportionately more insulating. It is therefore reasonable that as film thickness increases the SIS interface should become less dominant and therefore the ln J-V curves reflect this change.

The formula developed by Rhoderick [3] which accounted for the presence of an interfacial layer was applied using the depletion widths calculated in Chapter 2, the nascent oxide thickness from Figure 5.21 and permittivity from Chapter 5 and the density of surface states from Chapter 6. The resulting ideality factors are summarised in Table 7.2. The measured values did not correspond to the those calculated in Table 7.2. This is probably caused by the presence of interface states and the effect

of the remainder of the SRO layer.

Non-ideality is to be expected since the theoretical concepts of Schottky barriers are based on a metal in close proximity to the semiconductor. Metals are so electron-rich that there is no field developed across the electrode. In SIS devices band bending occurs in the intrinsic silicon and a field is developed across it.

Figures 7.6 and 7.7 show that for each device there was a slight temperature dependency. The lower the temperature the less ideal the diode. Below 210 K the thermionic emission theory was not applicable, since the ideality factors became very high. For a wide range of temperatures, $-55°$ C to room temperature, the ideality factor was independent of temperature. This suggests that the departure from unity was due to image force lowering and interface charge effects [3]. The reverse characteristics also support this idea.

7.4.3 Reverse characteristic

In reverse bias, the drift and diffusion theory predicts that the reverse current does not saturate but for large values of reverse current increases in proportion to $V^{1/2}$. This was not found to be the case for the SIS devices. The thermionic emission theory fitted the experimental data better. This predicts that the reverse current density of an ideal silicon Schottky diode should saturate at at the value J_0 [3].

$$J_0 = A^* T^2 \exp(-q\phi_b/kT) \tag{7.4}$$

The reverse current densities show saturation, particularly when compared with the forward characteristic.

There is a slight increase in reverse current with bias. This may be due to a field dependency of the barrier height (ϕ_b). The maximum field strength within the barrier ($\mathcal{E}_{max}$) increases with reverse bias and may decrease ϕ_b by image force lowering [3].

$$\Delta\phi_b = 2(q\mathcal{E}_{max}/16\pi\epsilon_s)^{1/2} \tag{7.5}$$

ϵ_s is the permittivity of the silicon. In addition, the presence of a nascent oxide on the substrate surface causes the effective barrier height to decrease with increasing bias. If there is no interfacial layer, the barrier height is independent of the electric field which may exist in the substrate. However, the electric field in the semiconductor

changes the potential across the interfacial layer and so modifies the barrier height [3].

$$\Delta\phi_b = \alpha\mathcal{E}_{max} \tag{7.6}$$

where

$$\alpha = \delta\epsilon_s/\epsilon_i + qD_s \tag{7.7}$$

and ϵ_i is the permittivity of the nascent oxide, δ is the width of the interfacial layer and D_s is the density of interface states. Tunnelling through the interfacial barrier may become significant in reverse bias because the voltages involved are much greater. These factors cause the slight increase in the ln J values with increased reverse bias displayed in Figures 7.1 and 7.2,

Although there are discrepancies between the Schottky barrier model and the experimental data, these may be accounted for by the possible changes in the barrier height, the nascent oxide, the presence of electric fields across both electrodes and the presence of interface charges. Overall, this model explains the rectifying behaviour of all devices at all temperatures reasonably well. In forward bias at high fields, once the SIS barrier has broken down, then other mechanisms act in series with the Schottky barrier and may control the flow of current across the remainder of the device.

7.4.4 Barrier height estimation

Estimates of the barrier heights may be obtained from

$$\begin{aligned} n &= n_i \exp\left(\frac{E_F - E_i}{kT}\right) \\ (E_F - E_i) &= kT \ln\left(\frac{N_D}{n_i}\right) = q(\phi_{si} - \phi_{sn}) = \phi_b \\ (E_i - E_F) &= kT \ln\left(\frac{N_A}{n_i}\right) = q(\phi_{si} - \phi_{sp}) = \phi_b \end{aligned} \tag{7.8}$$

Assuming a carrier concentration of $n_i = 1.45 \times 10^{10}\,cm^{-3}$ for intrinsic silicon, and $n = 1.00 \times 10^{16}\,cm^{-3}$ for n-type and $p = 5.00 \times 10^{15}\,cm^{-3}$ for p-type, the barrier $\phi_{si} - \phi_{sn} \approx 0.34V$ and the barrier $\phi_{si} - \phi_{sp} \approx 0.32V$. These theoretical calculations suggest that the p-type devices would conduct at lower biases than the n-type devices. The results presented in Chapter 6 show that this is not the case. However, ideal barrier height calculations do not take into account any interface or bulk oxide charge.

7.4.5 The barrier voltage determination

An MIS device is a multi-layered structure. The applied voltage is dropped across each of the following regions:

(i) top electrode;

(ii) metal-SRO interface;

(iii) bulk SRO;

(iv) Schottky barrier;

(v) bulk silicon;

(vi) silicon-back contact interface; and

(vii) the back metal.

Regions (i) and (vii) are assumed to drop negligible voltage, since the type of metal used as the top contact has been shown, in Chapter 6, to have little effect. The voltage associated with region (ii) was also assumed to be unimportant. The back contact metals were selected to provide symmetrical I-V characteristics of low resistance and therefore voltage (vi) was ignored. Region (v) was assumed to be ohmic. Any applied voltage would therefore make up a constant component of a similar value for each device on the same type of substrate and a variable component which is determined by the SRO film thickness.

Plots of voltage at particular current values were plotted against film thickness for a range of temperatures. The plots were extrapolated to zero film thickness to obtain a very approximate average value for the Schottky barrier voltage. Two examples of such plots are shown in Figures 7.8 and 7.9.

Figures 7.8 and 7.9 showed that the intercept increased with increasing current and that it was temperature dependent. The resultant barrier voltage was calculated from an average of many such plots and was taken to be $0.26\,V \pm 28\%$. This method provided a primitive estimate which was then deducted from the voltages recorded for the forward bias I-V characteristics. The barrier voltage value is in agreement with the theoretical estimate obtained in the previous section. This adds further impetus to the accuracy of using the Schottky barrier model to explain the observed rectifying behaviour which dominates these MIS devices.

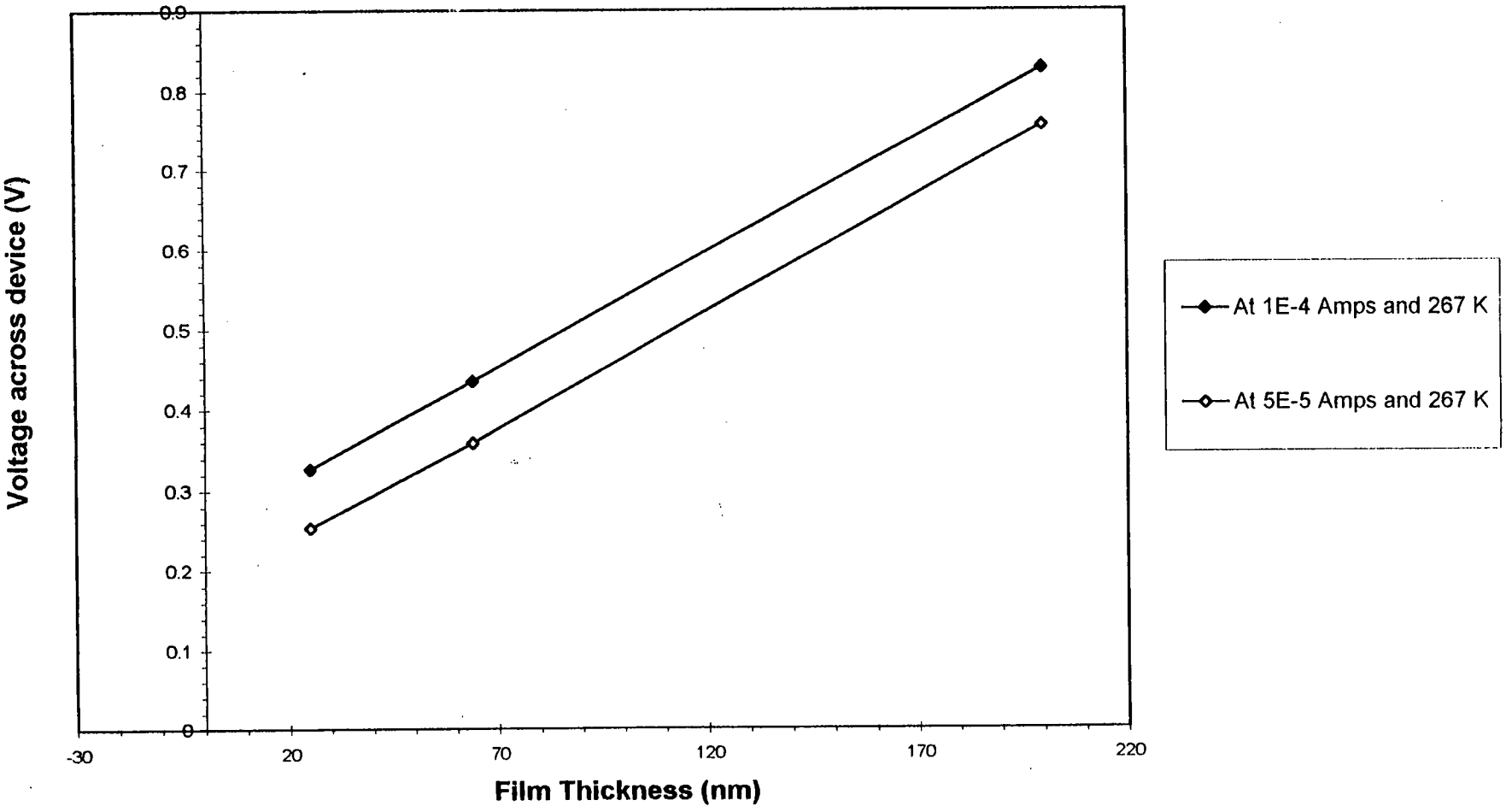

Figure 7.8 Plots of voltage at two stated current values against film thickness at 267 K. The intercept provides the SIS barrier voltage.

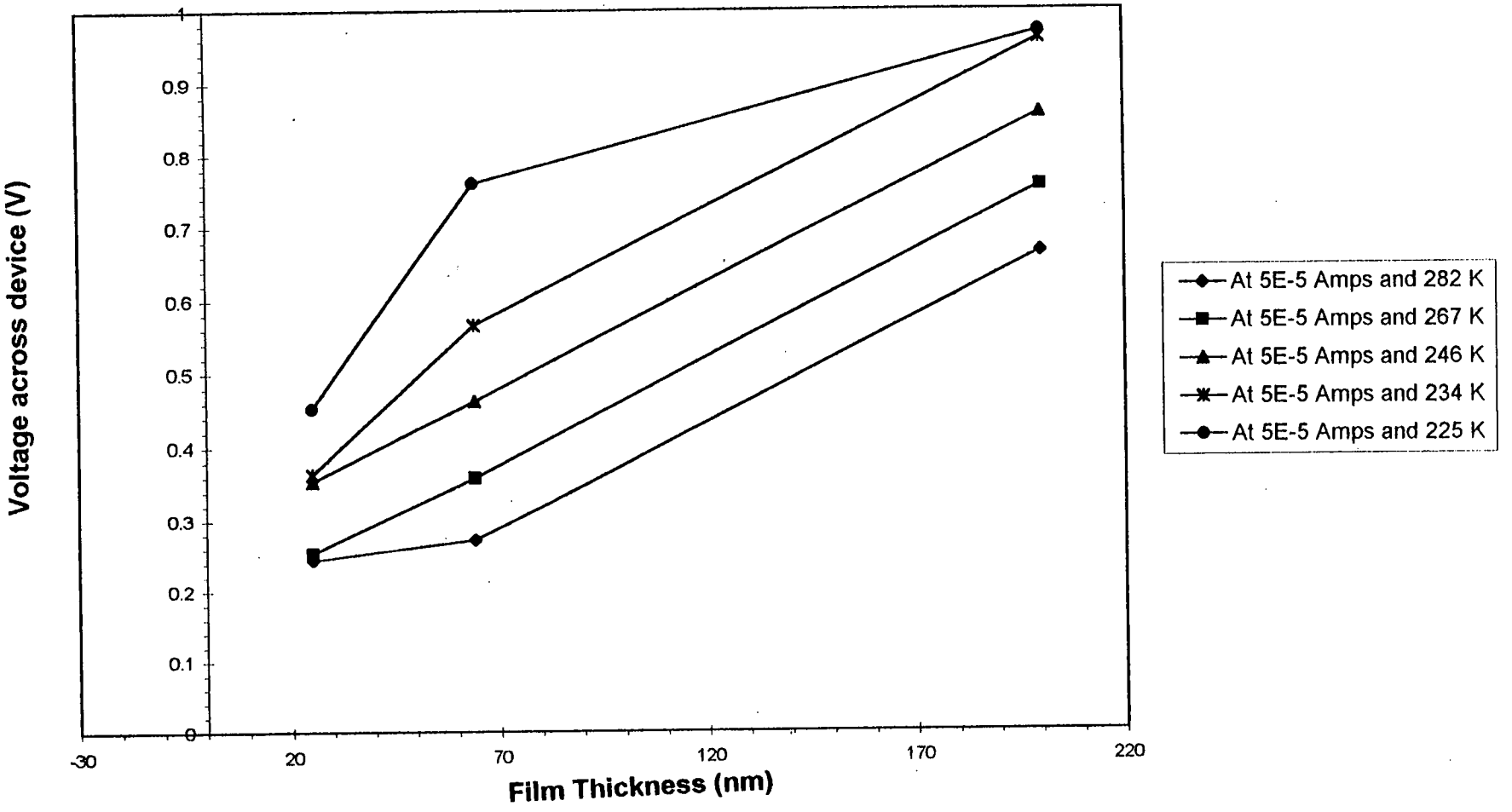

Figure 7.9 Plots of voltage at a particular current value against film thickness for a range of temperatures. The intercept provides the SIS barrier voltage at each temperature.

Substrate	ϕ_b (V)	A*(A m^{-2} K^{-2})	Ideality factor (n)
n-type	0.347	120	3
p-type	0.320	10	7

Table 7.3 Parameter values used in the Schottky equation to generate the theoretical curves for comparison with experimental data.

7.4.6 Comparison of theoretical and experimental curves

The current density for ideal Schottky diodes is given by [3]

$$J = A^* T^2 \exp\left(\frac{-q\phi_b}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{7.9}$$

as outlined in Section 7.4.1. The theoretical and measured parameters of barrier heights and ideality factors (as outlined in Table 7.3) were inserted into this equation and the experimental and theoretical curves for both n- and p-type SRO MIS devices were compared. Richardson's constant was used as a fit parameter. The values are stated in Table 7.3. Richardson's constant varies with temperature and applied electric fields and depends on whether the substrate is n- or p-type silicon. The values are low but such non-ideality is to be expected in this SIS diode. Figures 7.10 and 7.11 are typical of theoretical and experimental comparisons. A good fit was obtained between theory and experiment across the full range of SRO thicknesses for all reverse biases and for low forward biases. The turn on voltages are close to their theoretical values. Once the diode becomes conducting the fit fails. The theoretical currents rise much more steeply than the measured MIS currents. This is expected because in SRO devices once the Schottky barrier at the silicon-SRO interface is overcome the current must traverse the rest of the SRO film.

Further analysis was carried out to determine the dominant conduction mechanism once the Schottky barrier was overcome. Within each data file only the last few points, which safely represented the behaviour of the device when turned on, were considered. This limited the study and can, therefore, only provide an overview of the possible models for conduction in the remainder of the SRO film, once the Schottky barrier is conducting. A more detailed analysis on more reproducible devices is required.

The following sections describe how well various models for conduction in the remainder of the SRO film fit the experimental data obtained, once the Schottky barrier was overcome and the MIS device was conducting relatively large currents.

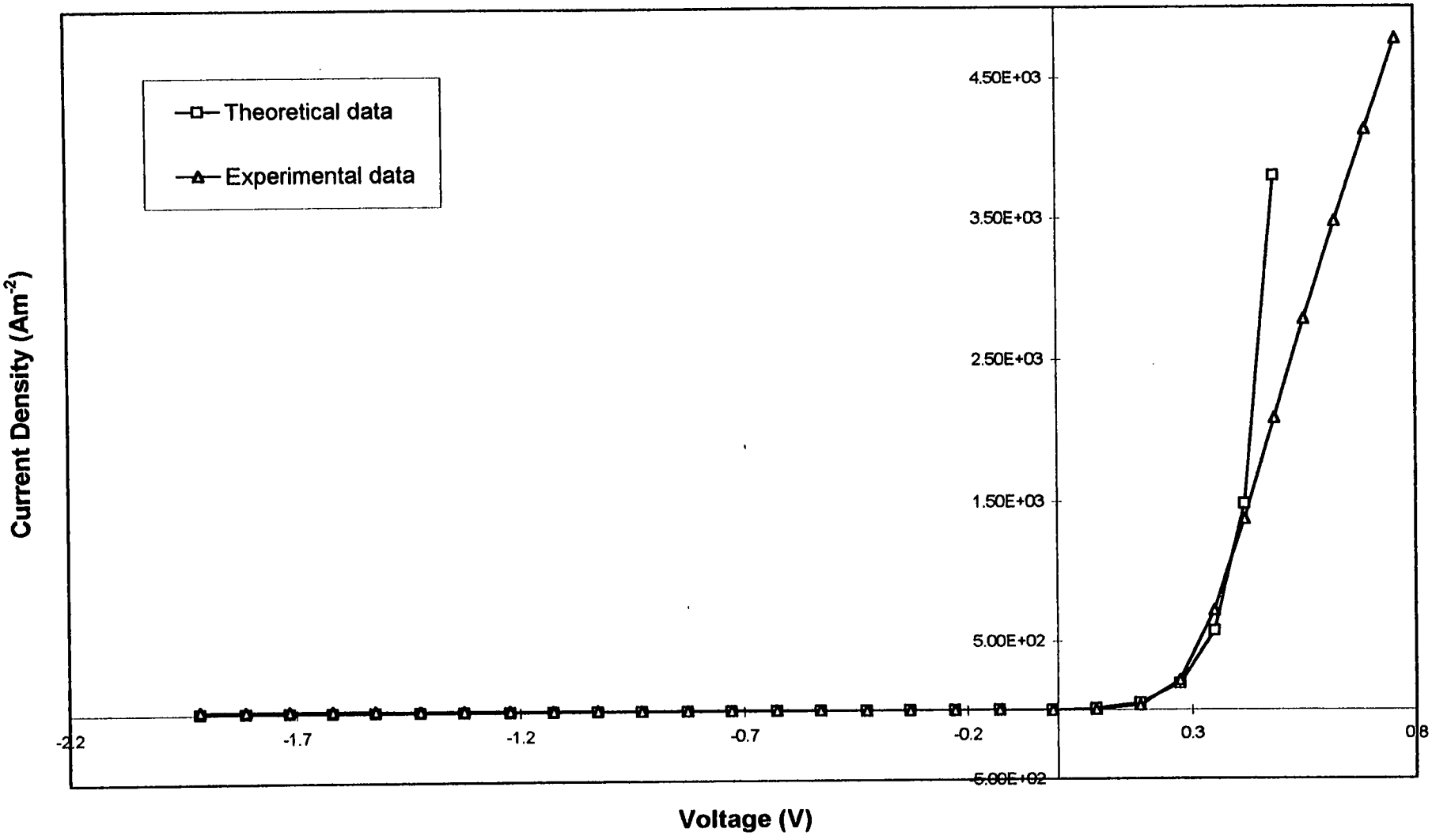

Figure 7.10 A comparison between Schottky theory and experimental data for device LJ with and aluminium top contact, an SRO deposition of 1 minute and an n-type silicon substrate.

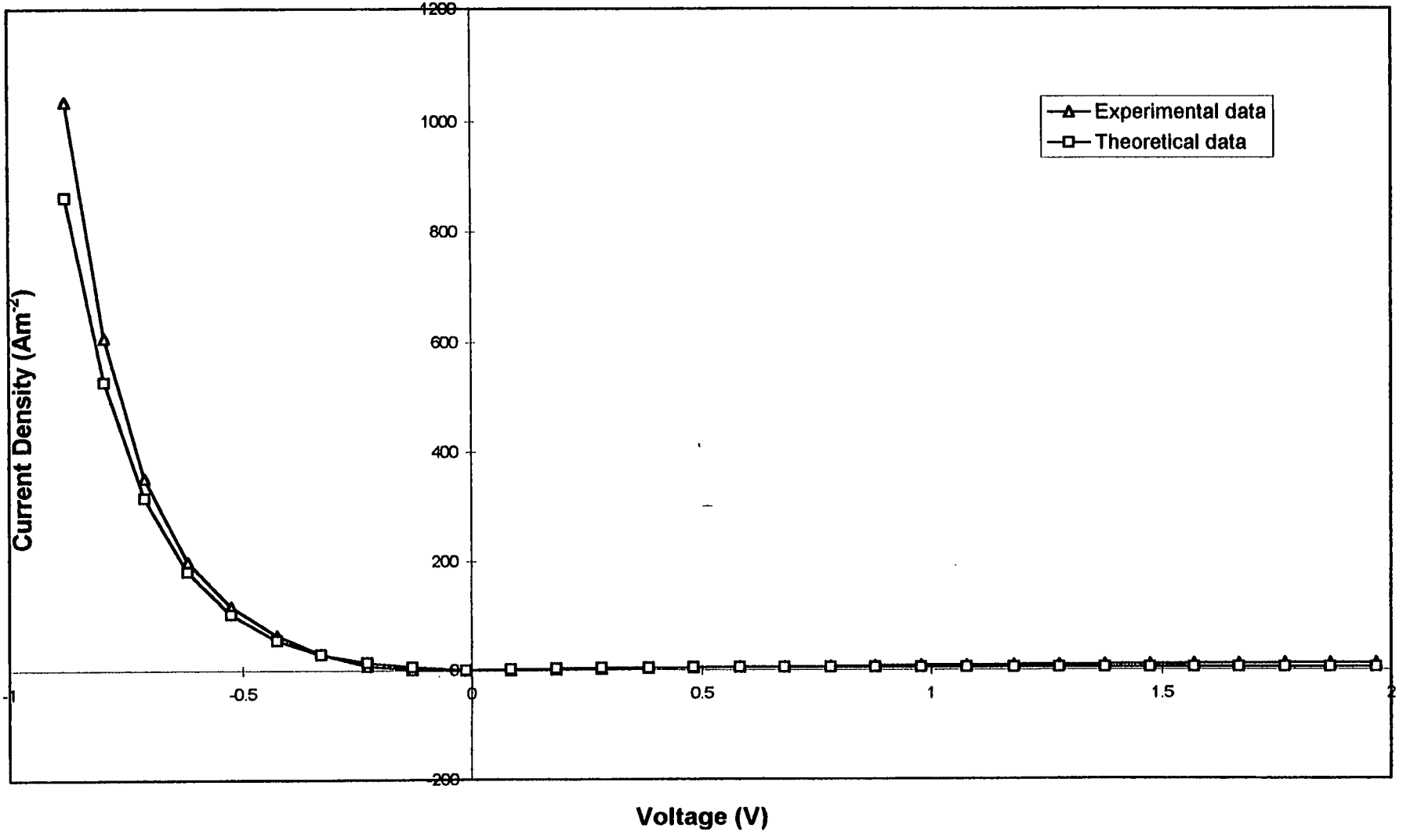

Figure 7.11 A comparison between Schottky theory and experimental data for device LJ with and aluminium top contact, an SRO deposition of 1 minute and an p-type silicon substrate.

SRO thickness (nm)	ϕ (eV)	A*(A m^{-2} K^{-2})
25	1.17	0.01
64	1.24	0.10
196	1.40	1.96
654	1.55	458.26

Table 7.4 Average values of ϕ from thermionic emission theory for a range of SRO film thicknesses on devices LJ at an applied voltage of 1.2 V.

7.5 Conduction in the bulk of the SRO film

Models for conduction in thin films were described in Chapter 3. The Schottky barrier is assumed to describe the low current and voltage regions of the forward and reverse bias I-V characteristics. The other theories are compared to I-V characteristics at high forward bias to model the high current regime.

7.5.1 Ohmic conduction

The thinnest SRO devices showed ohmic behaviour for all but the lowest temperatures. This was probably because, as reported in Chapter 5, in these samples silicon dendrites traversed the SRO film. The currents were temperature-dependent and were probably determined largely by the resistivities of the intrinsic silicon within the SRO and the silicon substrate. There is little evidence to suggest that ohmic conduction is the dominant mechanism in the remainder of the SRO, once the SIS interface is conducting. Ohmic conduction is therefore ruled out.

7.5.2 Thermionic emission

Thermionic emission of electrons is governed by the equation

$$\frac{\ln(J/T^2)}{1/T} = \ln A^* - 1 + \frac{qV}{k} - \frac{q\phi}{k} \tag{7.10}$$

The intercept of the graph is a measure of the Richardson's constant, A^* and the gradient is $q(V-\phi)/k$, where V is the applied voltage and ϕ is the barrier height. As shown by Figure 7.12 the gradient was independent of voltage and should have been proportional to V. ϕ varied from 1.1 to 1.5 eV, increasing with increased film thickness, as shown in Table 7.4. Each value has an error within $\pm 5\%$. The values for

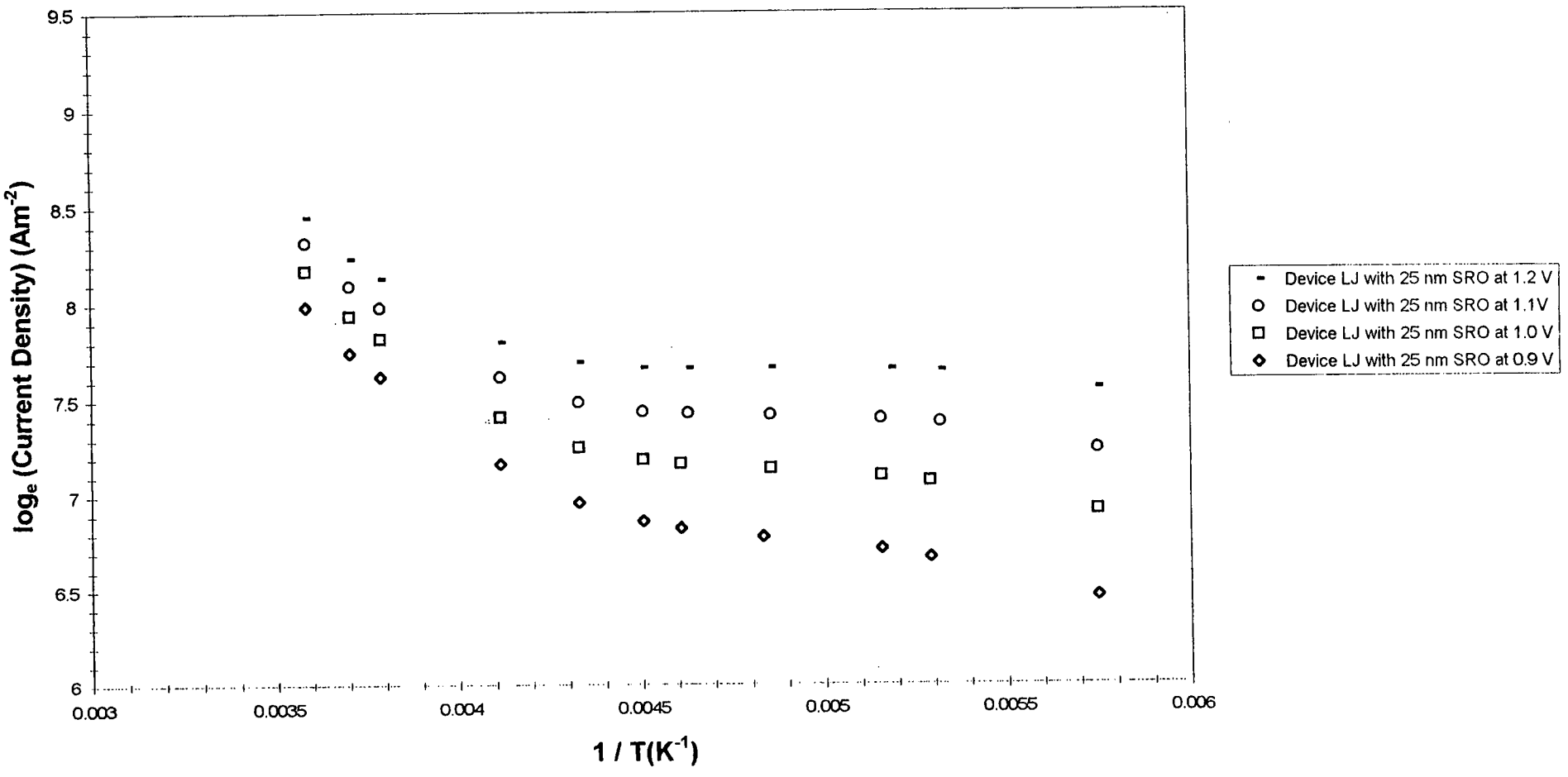

Figure 7.12 Thermionic emission theory plots of ln current density versus the reciprocal of temperature at various voltages for a typical MIS device on an n-type substrate.

ϕ are high whereas those for A*, shown in Table 7.4 are ridiculously low. Figure 7.12 shows that the temperature dependency of J increases at around 270 K. At 270 K there appears to be an exponential increase in the current, this would make intercept calculations much more difficult. Although the numerical parameters were inaccurate, this analysis suggests that thermionic emission is important at temperatures above 270 K and that another mechanism is predominant below this.

7.5.3 The Abeles model

Many workers, as described in Chapter 3, suggest that there are two mechanisms operating in SRO films. Abeles [4] modelled carrier transport in cermets.The conductivity was controlled by direct tunnelling from metal grain to metal grain. Fowler-Nordheim tunnelling between metal particles was found to predominate at high fields. The low field region was governed by the relation

$$J \propto \exp\left(-2\sqrt{\frac{c}{kT}}\right) \tag{7.11}$$

where c was a constant. Plots of ln J versus $\sqrt{T}$ showed two regions, (as shown by Figure 7.13). The change in mechanism occurred at around 260 K but Abeles' cermet model provided a poor fit to the data. This model is therefore discounted.

7.5.4 Fowler-Nordheim tunnelling

At the lower limit of the temperatures investigated and at high fields, there was a negative slope to the $\ln J/\mathcal{E}^2$ versus $1/\mathcal{E}$ characteristic and straight line regions were present. This suggested that a Fowler-Nordheim tunnelling process may be in operation. The currents were too low for the $\mathcal{E}^2$ term to be representative of a space charge limited flow. At the higher temperatures Fowler-Nordheim tunnelling was evident only for the 25 nm films. The typical equation used for plotting data is

$$\ln\left(\frac{J}{\mathcal{E}^2}\right) = \ln\left(\frac{K_1}{\phi}\right) - \frac{K_2\phi^{3/2}}{\mathcal{E}} \tag{7.12}$$

K_1 has the value $5.41 \times 10^{-25}\ \mathrm{C^3\,J^{-1}\,s^{-1}}$. K_2 has the value $1.08 \times 10^{38}\ \mathrm{kg^{1/2}\,J^{-1}\,s^{-1}C^{-1}}$. A plot of $\ln(J/\mathcal{E}^2)$ versus $1/\mathcal{E}$ should yield straight lines with an intercept given by $\ln K_1/\phi$ and gradient $-K_2\phi^{3/2}$. As shown in Figure 7.14 the gradients for the Durham films were negative. The barrier height (ϕ) values were obtained from the intercept,

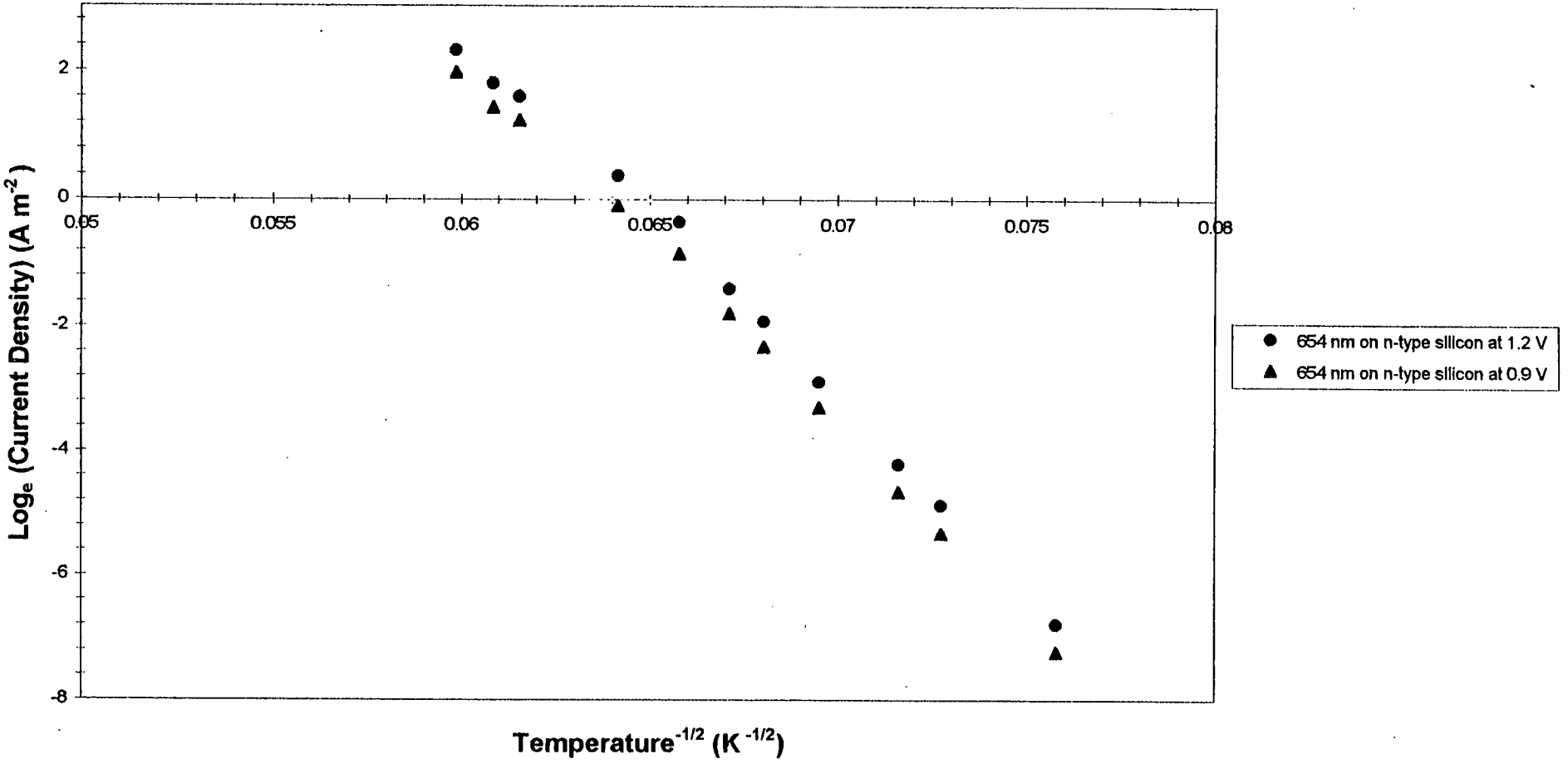

Figure 7.13 The Abeles model. Plots of ln current density versus the square root of temperature for a typical SRO MIS device at two voltages.

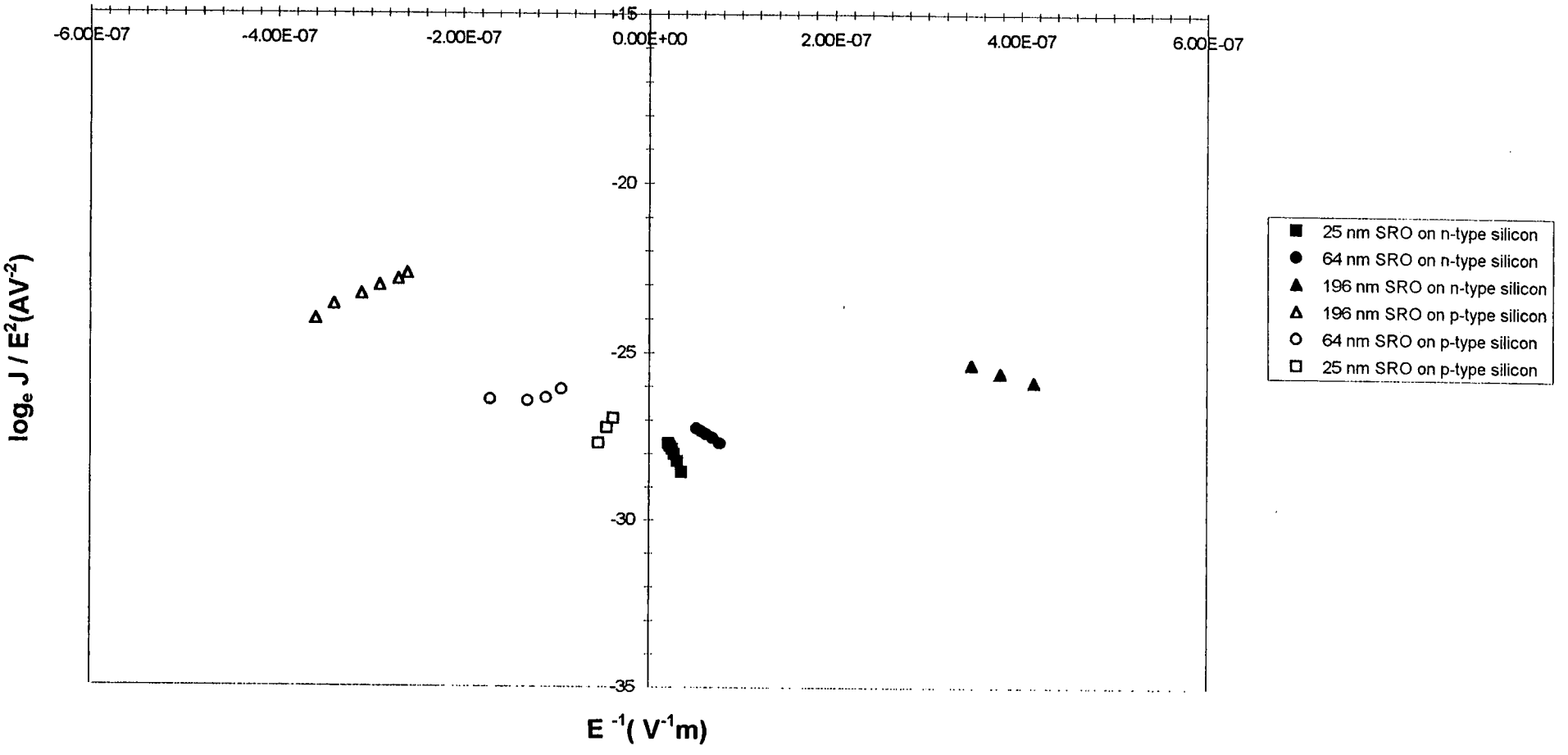

Figure 7.14 Fowler-Nordheim plots at 174 K for device LJ with SRO film depths of 25 to 654 nm on n- and p-type substrates.

by extrapolation of the Fowler-Nordheim plots. ϕ was also obtained from the gradient. In theory, the two barriers should have been close in value, but this was not the case. The inaccuracies introduced by the extrapolation may account for this but both methods yielded unrealistically low values for ϕ.

Since the barrier heights are too low and the plots shown in Figure 7.11 are very diverse and different from the conventional Fowler-Nordheim plots this mechanism is ruled out for SRO. The poor response to a purely field operated mechanism also rules out those tunnelling mechanisms suggested by Di Maria [1] and by Tarng [2], for SRO. In addition, Di Maria *et al* [1] suggested that conduction in SRO was mainly by electrons due to the higher energy gap between the valence bands within the oxide and silicon. In the Durham SRO films this does not seem to apply. N- and p-type equivalent devices have a similar current flow when made and tested using identical conditions. This provides further evidence for the dismissal of these field operated tunnelling mechanisms.

7.5.5 The Hamasaki model

Hamasaki *et al* [5] also found that conduction in their SRO films involved two distinct mechanisms, one mechanism dominated at high temperature and the other at temperatures below room temperature. The behaviour was governed by

$$\sigma = \sigma_0 \exp\left(\frac{-E_0}{kT}\right) + \sigma_1 \exp\left(\frac{-E_1}{kT}\right) \tag{7.13}$$

σ_0 and E_0 are the conductivity and activation energies above room temperature and σ_1 and E_1 are the same quantities below room temperature. The higher the temperature, the higher the gradient and the higher the activation energy. Ln $J/\mathcal{E}$ versus 1/T plots showed two conduction regimes: one associated with high temperatures; and the other with low temperatures. This pattern of behaviour can be seen in Figure 7.15.

In contrast to the Hamasaki model, the higher activation energy was associated with the lower temperature range. This was also in contrast to a similar model produced independently by England and Simmons [6]. The experimental data fitted both models inconsistently across the various SRO film thicknesses and substrate types and therefore, these mechanisms were discounted.

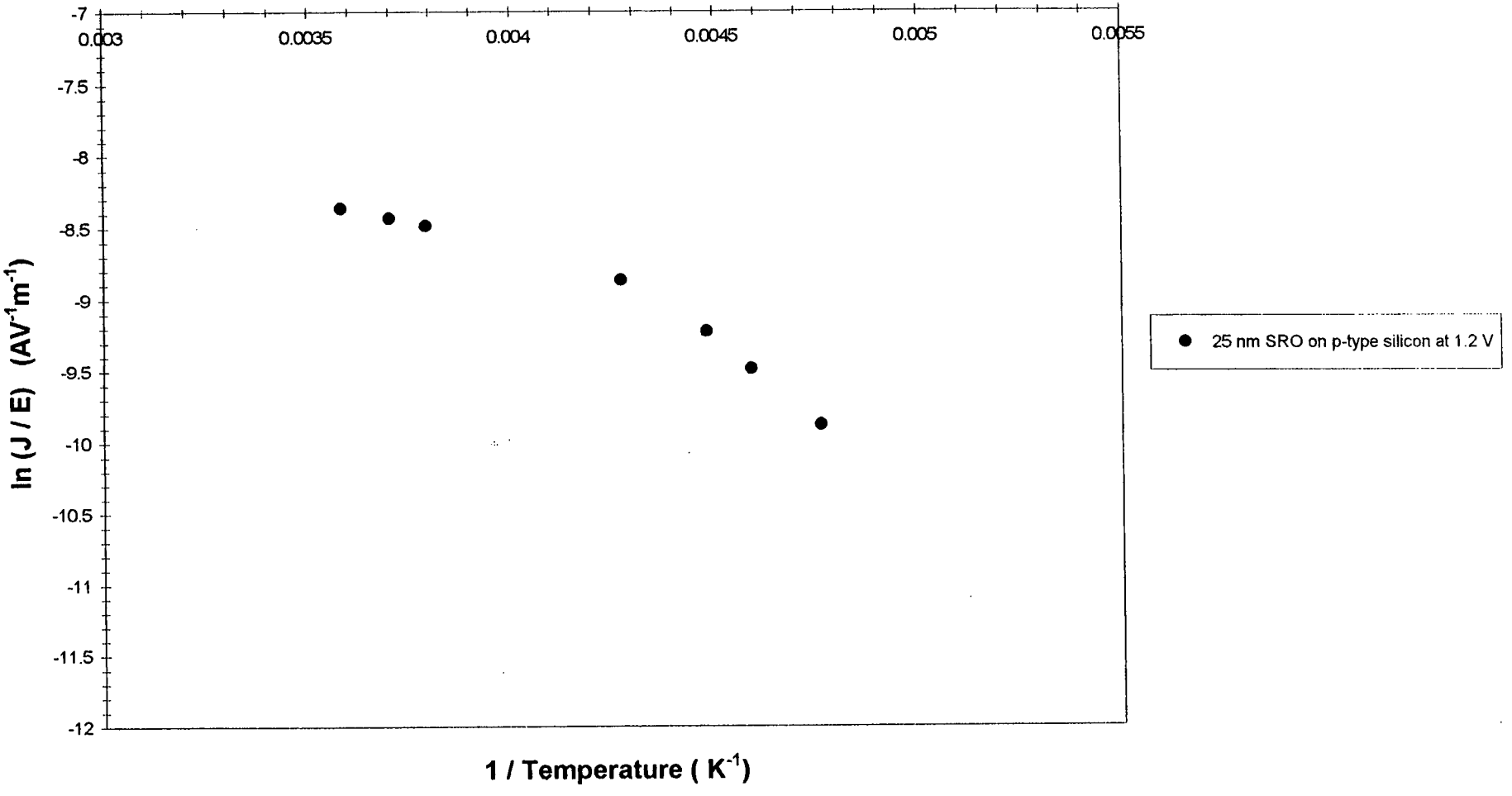

Figure 7.15 Plots of ln $J/\mathcal{E}$ versus the reciprocal of temperature for device LJ discount the Hamasaki and the England and Simmons models for conduction in the Durham SRO films.

7.5.6 Percolation theory

In this model the SiO_x film is considered to contain a random arrangement of barriers separated by an average distance, l [7].

$$J = J_0 \exp\left(\frac{\alpha \mathcal{E}^{1/2}}{kT}\right) \tag{7.14}$$

α is related to the degree of disorder. N-type devices were annealed, as described in Chapters 4 and 6. Annealed films have been found to be more ordered and therefore should have a smaller value for alpha. Plots of ln J versus $\mathcal{E}^{1/2}$ were analysed for annealed and identical as-deposited samples. Straight line regions were observed, which suggested that this could be a possible model for the SRO diodes. The as-deposited devices actually had lower gradients and α values than the annealed samples and therefore, percolation cannot describe conduction in SRO.

Fowler-Nordheim plots showed that tunnelling was more likely to occur in annealed films. The increased crystallite sizes may cause more voltage to be dropped across the intervening oxide in the annealed films. This reduces the barrier between crystallite and oxide conduction bands enough to allow Fowler-Nordheim tunnelling to occur. The observed increase in tunnel currents was small.

The anneal produced a more symmetrical plot and therefore, must have changed the silicon-oxide interface in some way. The barrier was reduced in reverse bias. Annealing has been shown to alter the number and sign of the interface charges [8]. Once again, the SIS interface was found to play an important part in the conduction of SRO MIS devices. More detail on the structural and chemical effects of annealing are needed before the electrical characteristics can be explained. A limited study was conducted here and further experiments are suggested in the final Chapter but percolation is ruled out as a conduction mechanism for the SRO film once the SIS interface is conducting.

7.5.7 The Ni and Arnold model

Ni and Arnold [9] developed a theory to explain one of the two conduction regimes displayed by their SRO I-V measurements. Conduction was thought to be by thermally generated carriers tunnelling through the oxide layers separating adjacent sili-

con grains. At the higher temperature range the current density followed the relation

$$J = K_1 \mathcal{E}(d + l_{ox}) \exp\left(\frac{-E_a}{2kT}\right) \exp(-2K_2 l_{ox} \phi^{1/2}) \tag{7.15}$$

where

$$K_1 = \frac{4\pi q^2 m_1 kT}{h^3} \tag{7.16}$$

and

$$K_2 = \left(\frac{8\pi^2 m_2}{h^2}\right)^{1/2} \tag{7.17}$$

m_2 is assumed to be $0.42\,m_o$, m_1 is assumed to be $0.98\,m_o$ [9] and m_o is the rest mass of an electron. d is the average silicon grain width and l_{ox} is the average intervening oxide width. The functional form of the above equations is

$$\ln\left(\frac{J}{\mathcal{E}}\right) = \ln\left(K_1[d + l_{ox}]\right) - \frac{E_a}{2kT} - 2K_2 l_{ox} \phi^{1/2} \tag{7.18}$$

A plot of $\ln(J/\mathcal{E})$ versus $1/T$ produces an intercept of $\ln(K_1[d + l_{ox}]) - 2K_2\phi^{1/2}l_{ox}$ and a gradient given by $-E_a/2k$. Ni and Arnold [9] estimated the average grain size and intervening oxide thickness and substituted these values into their equation for the intercept to obtain the barrier height. The barrier height was found to be 3 eV. This agreed with the theoretical barrier height between the conduction bands of Si and SiO_2.

The Ni and Arnold equations were used to determine typical average values of silicon grain size and oxide length for the Durham SRO films. For an average composition of oxygen of 29% it can be shown that l_{ox} and d are related by $l_{ox} = 0.165d$. The values for l_{ox} and d were calculated to be 1.01 nm and 6.12 nm, respectively, and are reasonable for the structure of SRO grown here. The average grain size is larger than that of other workers [9] due to the high silicon content and due to the presence of the columnar growths of silicon, observed in the electron microscope photographs.

These approximate values for grain size and intervening oxide widths were applied to different device areas. The barrier height was independent of device area. The results of typical Ni and Arnold plots for some of the Durham SRO devices are summarised in Tables 7.5 and 7.6.

In the Ni and Arnold model the silicon crystals, within SRO, are thought to be intrinsic in nature with traps at the edges which pin the Fermi level near mid-gap. The activation energies Ni and Arnold calculated were around half the band gap of silicon at 300 K, i.e. 0.56 eV. In the Durham devices, only the thickest SRO films, as

SRO film thickness (nm)	Activation energy (eV)	ϕ (eV)
25	0.28 $\pm$5%	3.93 $\pm$4%
64	0.37 $\pm$6%	2.43 $\pm$10%
196	0.38 $\pm$6%	2.48 $\pm$16%
654	0.63 $\pm$4%	1.82 $\pm$15%

Table 7.5 Measured energy gap values for device LJ with various depositions of SRO on an n-type substrate at temperatures above $-20°C$

SRO film thickness (nm)	Activation energy (eV)	ϕ (eV)
25	0.08 $\pm$10%	7.2 $\pm$10%
64	0.23 $\pm$5%	4.1 $\pm$4%
196	0.39 $\pm$20%	3.0 $\pm$25%
654	0.74 $\pm$3%	1.0 $\pm$2%

Table 7.6 Measured energy gap values for device LJ with various depositions of SRO on an n-type substrate at temperatures below $-20°C$

shown in Table 7.5, have similar activation energies. The activation energies increase with SRO film thickness. This is logical, since the increasing film thickness contained an increasing amount of oxygen. The activation energy and ϕ values decreased with increasing bias, which suggested an image force lowering effect. For the high temperature regime, it may be that the Schottky emission or Poole-Frenkel models may better describe the data.

At the lower temperatures investigated the activation energies and barrier heights are summarised in Table 7.6. The activation energies are smaller for the thinner films. This agrees with the Ni and Arnold model. However, the barrier heights are large and are closer to the value for SiO_2 than for silicon. Again, the barrier height decreased with increased SRO film thickness. The converse was true for p-type materials. Measurements of ϕ, for example, were approximately 4, 6 and 8 eV for 25, 64 and 196 nm, respectively. As the barrier to electron flow decreased with SRO film thickness, the barrier to hole flow increased. This suggests that there was a change in the Fermi level as the SRO film grew and that the Fermi level was not pinned to mid gap.

The Ni and Arnold model goes some way towards describing the current flow in the SRO MIS devices but there were some problems. Since the logarithm of the K_1 term in the intercept equation is used in the intercept calculation, the result of the first

term is fairly insensitive to changes in T, d and l_{ox}. Also, $[d+l_{ox}]$ in this term is likely to remain fairly constant, since if d increases l_{ox} decreases. Ni and Arnold have made conclusions based on a model which contains a mathematical error. They included the K_2 term in the gradient instead of the intercept. The K_1 and K_2 terms make the model fairly insensitive to changes in grain size, etc. This makes it impossible to make conclusions about relative barrier sizes in the various n- and p-type devices with confidence. This data analysis suggested that the Schottky or Poole-Frenkel model may be more effective in describing SRO conduction.

7.5.8 The Schottky and Poole-Frenkel mechanisms

Details of Schottky and Poole-Frenkel models were given in Chapter 3. Schottky plots of the data were made using the equations outlined below.

$$J = A^* T^2 \exp\left(\frac{-q\phi}{kT}\right) \exp\left(\frac{q^{3/2}\mathcal{E}^{1/2}}{2\pi kT\epsilon^{1/2}}\right) \tag{7.19}$$

$$\ln\left(\frac{J}{T^2}\right) = \ln A^* - \frac{q\phi}{kT} + \frac{\beta\mathcal{E}^{1/2}}{kT} \tag{7.20}$$

It is usual to plot

$$\ln\left(\frac{J}{T^2}\right) \quad \text{versus} \quad \mathcal{E}^{1/2} \tag{7.21}$$

Regions of linearity were observed in the Schottky plots for several film thicknesses, over a wide range of temperatures. Figure 7.16 is a particularly good example. In fact, the thicker the film the straighter the lines on these graphs. The intercept is given by the expression

$$\ln|A^*| - \frac{q\phi}{kT} \tag{7.22}$$

and the gradient by

$$\frac{\beta}{kT} \tag{7.23}$$

where

$$\beta = \frac{q^{3/2}}{2\pi\epsilon^{1/2}} \tag{7.24}$$

A similar set of equations was described in Chapter 3 for the Poole-Frenkel model, with the exception that $\beta_{PF} = 2\beta_s$.

Many data files were analysed for all film thicknesses, substrate type and for all temperatures. The model fitted the data badly for temperatures above $-20°$ C. For the temperature range $-27°$ C to $-96°$ C the fit was variable depending on the

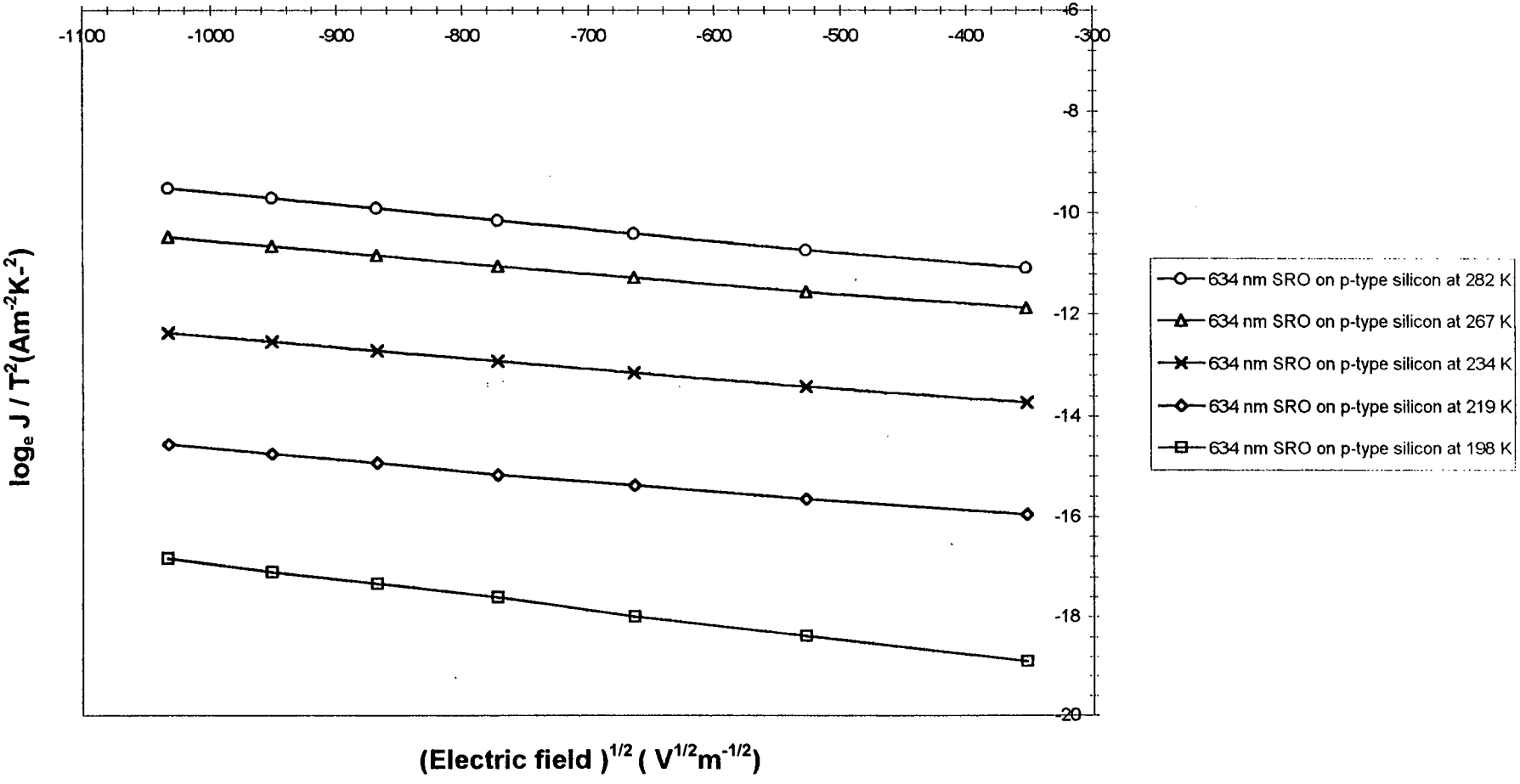

Figure 7.16 Example Schottky plots, over a range of temperatures, for device LJ manufactured on a p-type substrate with 634 nm of SRO.

Temperature (K)	Permittivity of the oxide $\times 10^{-11}\,\mathrm{Fm}^{-1}$ (Schottky)	Permittivity of the oxide $(\times 10^{-11}\,\mathrm{Fm}^{-1}$ (Poole-Frenkel)
231	1.84	7.38
222	1.54	6.15
217	1.74	6.96
207	1.61	6.45
195	1.81	7.24
189	1.77	7.09
174	1.89	7.54

Table 7.7 Permittivity measurements for device LJ with a 25 nm film of SRO deposited on an n-type substrate over a range of temperatures.

particular conditions of temperature and SRO film thickness. The evidence showed that the data fit was independent of substrate material. Even though the plots sometimes looked slightly curved for the thinner films, a correlation factor of above 0.99 was obtained for all $\ln\left(\frac{J}{T^2}\right)$ versus $\mathcal{E}^{1/2}$ data below $-27°$ C.

Some of the results of the Schottky data analysis are shown in Table 7.7 for a one minute deposition of SRO on an n-type substrate, from $-27°$ C to $-99°$ C. First, the gradients were obtained and the permittivity of the oxide calculated, using both the Schottky and Poole-Frenkel β values. The results presented in Table 7.7 compared favourably with those obtained from the ellipsometry measurements. The refractive index, n, obtained from the ellipsometry measurements was 2.586 and since $\epsilon_r = n^2 = 6.687$ a value of 5.92×10^{-11} was calculated for ϵ_{ox}. Since the values of ϵ_r for silicon and SiO_2 are 11.9 and 3.9, respectively, the value for ϵ_r obtained from ellipsometry is reasonable. Of the two models, in general, the Poole-Frenkel mechanism produced the closest fit to the ellipsometry results. Table 7.7 shows that there is some doubt in the way in which the permittivity values change with temperature for the 25 nm SRO films. This was true of all film thicknesses, but the trend was for decreasing temperature the permittivity increased.

Table 7.8 summarises some of the results of the Schottky/Poole-Frenkel data analysis for various film thicknesses. The uncertainty in the permittivity values make it difficult to make precise conclusions. Reasonable data fits were found for all but the thickest SRO film. Table 7.8 shows that the Poole-Frenkel mechanism appears to be the most likely of the two models. Strangely, the thickest films produced the best straight line plots for the $\ln\left(\frac{J}{T^2}\right)$ versus $\mathcal{E}^{1/2}$ relation and yet also produced ridiculously low permittivity values.

Film thickness (nm)	Substrate type	Permittivity of the oxide $\times 10^{-11}\,\mathrm{Fm}^{-1}$ (Schottky)	Permittivity of the oxide $\times 10^{-11}\,\mathrm{Fm}^{-1}$ (Poole-Frenkel)
25	p-type	1.28	5.14
25	n-type	2.78	11.1
64	p-type	1.24	4.95
64	n-type	1.61	6.45
634	p-type	8.67	3.47
654	n-type	0.155	0.622

Table 7.8 Permittivity measurements for SRO for various SRO film thicknesses at around 210 K.

The Schottky equation, can be rearranged to produce a different set of graphs.

$$\ln\left(\frac{J}{T^2}\right) = \ln A^* - \frac{\phi}{kT} + \frac{\beta\mathcal{E}^{1/2}}{kT} \tag{7.25}$$

$\ln(J/T^2)$ versus $1/T$ plots have a gradient given by

$$\text{gradient} = \frac{\phi_m - \beta\mathcal{E}^{1/2}}{k} \tag{7.26}$$

and an intercept given by $\ln A^*$. A^* is the Richardson constant. Again, the best linear plots were obtained for the thicker samples. Examples of the $\ln(J/T^2)$ versus $1/T$ plots for various SRO film thicknesses on otherwise identical devices at 1.2 V are shown in Figure 7.17.

If the value for ϵ_{ox}, obtained from ellipsometry or from the previous plots is inserted into the equation for the gradient the barrier height can be determined. This was expected to be near half of the band gap for silicon. The results were very low. 0.175 eV was the highest value recorded. The intercepts were used to determine the $\ln A^*$ and therefore the value of A^*. Ridiculously low values were obtained.

The simple analysis used to calculate the value of A^* is unreliable. A line of best fit may not give a true intercept value. The Richardson constant, A^* is usually quoted as $120\,\mathrm{A\,cm^{-2}\,K^{-2}}$. This value applies to free electrons at room temperature. A^* is given by

$$A^* = \frac{4\pi q m k^2}{h^3} \tag{7.27}$$

Electrons in n- and p-type silicon have an effective mass which differs from that of the electron rest mass. This causes A^* to change by a factor of 2.1 and 0.66 for n-type

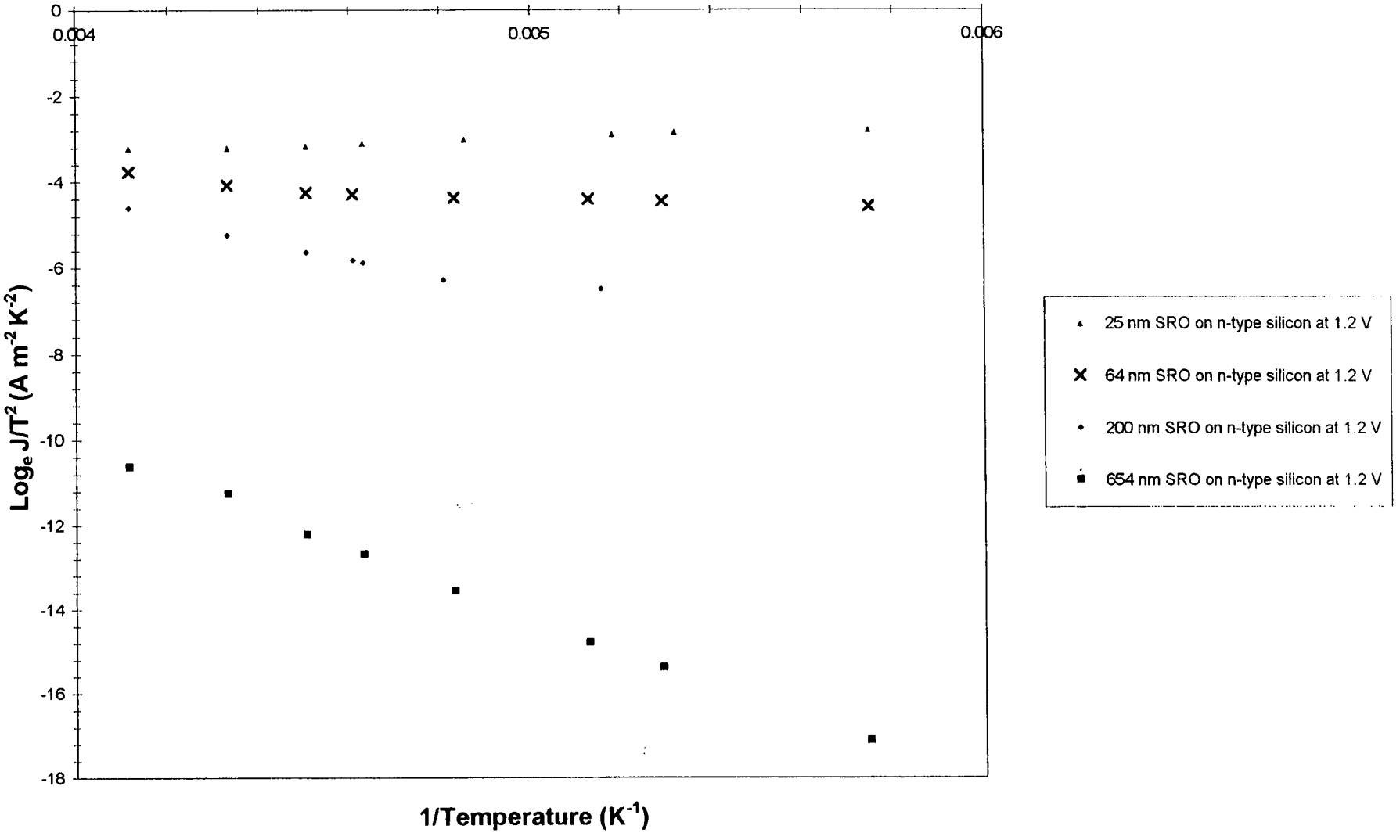

Figure 7.17 Schottky and Poole-Frenkel plots of $\ln(J/T^2)$ versus $1/T$ for various SRO film thicknesses on otherwise identical devices at 1.2 V

and p-type silicon, respectively [10]. A^* is also affected by applied electric field and temperature. At room temperature and electric fields in the region of $10^5\,\mathrm{Vm^{-1}}$. A^* has been found to have values of $110\,\mathrm{A\,cm^{-2}\,K^{-2}}$ and $30\,\mathrm{A\,cm^{-2}\,K^{-2}}$ for n- and p-type silicon, respectively [10]. For fields in the region of $10^6\,\mathrm{V\,m^{-1}}$, used in this study, higher values above $1.20 \times 10^4\,\mathrm{A\,m^{-2}\,K^{-2}}$ are expected. As temperature increases, since

$$A^* \propto T^{-2} \tag{7.28}$$

A^* should fall in value. It is therefore, difficult to predict the precise value for A^*. Even allowing for this, some of the values recorded for the thinner films are less than $1\,\mathrm{A\,m^{-2}\,K^{-2}}$ and are exactly as calculated in Table 7.4. The thickest films produced values in the region of $500\,\mathrm{A\,m^{-2}\,K^{-2}}$ but this is still too low.

The values for the potential barrier, ϕ, have been found to increase as the temperature falls. Even so, extremely low barrier heights have been recorded. This is thought to be caused by the presence of interface states at both SRO film interfaces and due to the large number of traps which surround each silicon grain, within the SRO. The band gap is made smaller and narrower by the presence of extended states and intermediate trap levels help to bridge the forbidden gap, as shown in Figure 7.18.

As the SRO film grows more oxide is present, the film is more disordered and the silicon crystallites decrease in size. A large number of intermediate energy levels are introduced within the forbidden energy gap of the oxide. These intermediate levels are thought to be randomly arranged in both space and energy. The number of these levels, therefore, vary with distance into the SRO film. The smaller the silicon crystal, the higher the number of interface states present. The band diagram alters and is represented by Figure 7.19. Conduction takes place via the path of least resistance. The lowest band gap may be represented by the trend shown in Figure 7.19, which links the SRO structure with the decreasing barrier heights.

The lowered energy barriers are consistent with those values obtained using the Poole-Frenkel model. Conduction in amorphous materials has often been described by a Poole-Frenkel process. Poole-Frenkel emission could be occurring, via a hopping mechanism between defect centres and silicon crystallites within the SRO. In conclusion, the Poole-Frenkel model best describes conduction in the n- and p-type devices which contain SRO layers between 25 and 600 nm in thickness, across a temperature range of $-27°$ C to $-99°$ C.

Figure 7.20 pulls together the results of Chapters 5 and 6 and summarises the most

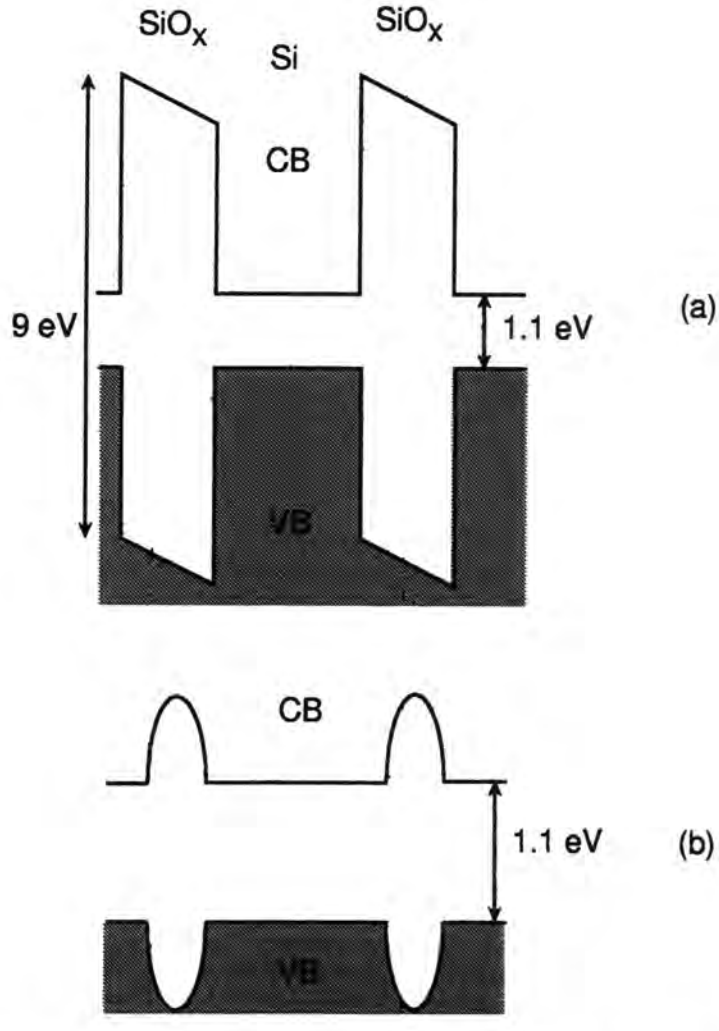

Figure 7.18 The energy bands between two adjacent silicon crystallites. (a) The ideal case and (b) the real case.

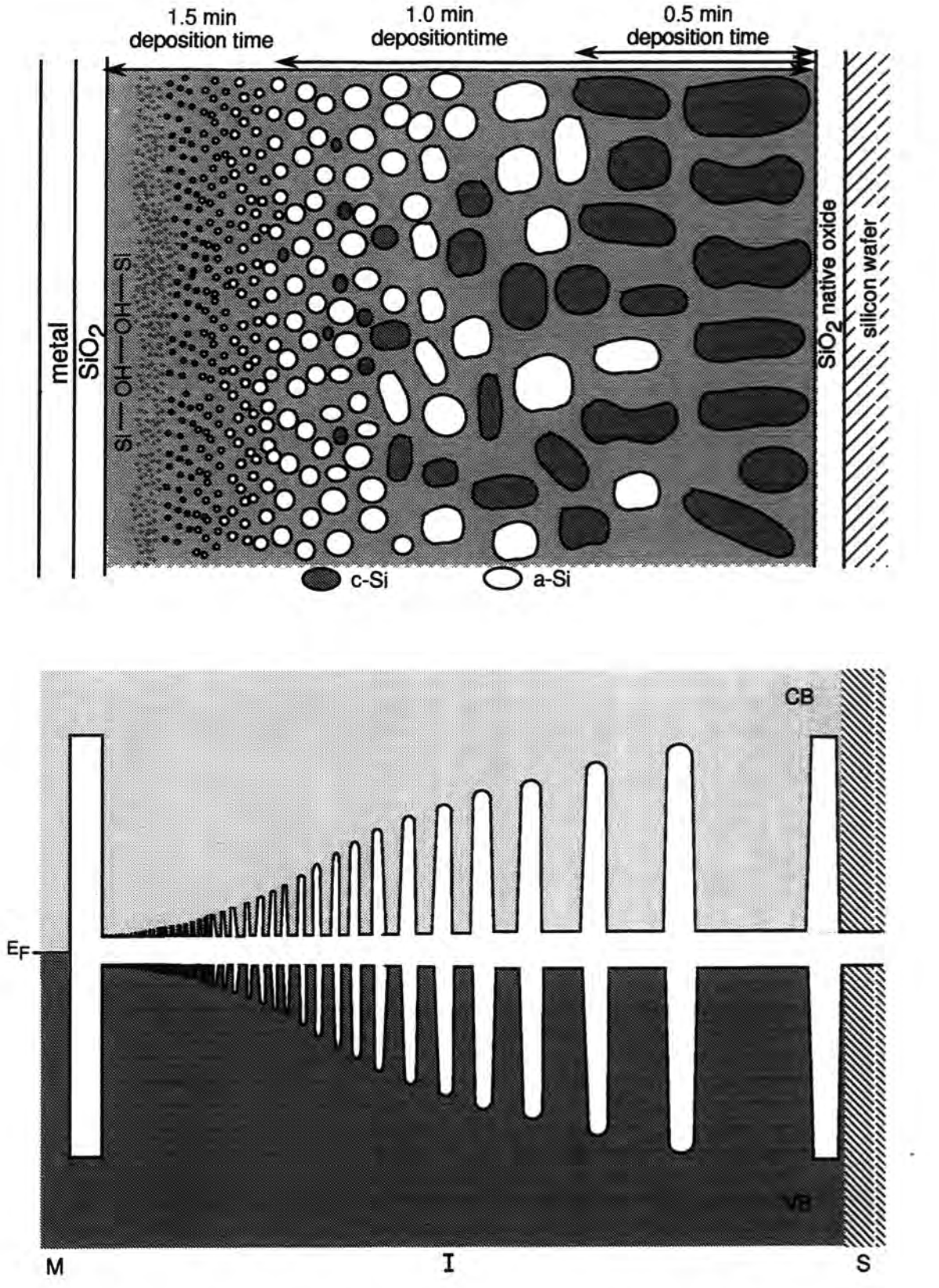

Figure 7.19 SRO film structure and corresponding energy band diagram.

dominant conduction mechanisms in the SRO devices. The Schottky barrier model is indicated at the substrate-SRO interface. Once the Schottky barrier is overcome conduction in the remainder of the SRO film is dominated by a Poole-Frenkel process at low temperatures and by thermionic emission at high temperatures.

7.6 Summary

The complex nature of the SRO MIS device makes it difficult to characterise precisely. Semi-continuous films, consisting of randomly arranged islands and traps probably conduct via several mechanisms, simultaneously. Various standard models for conduction have been compared with the electrical data obtained for a range of MIS structures. Some data have been linked to possible conduction models and to a band structure for the silicon-oxide interface and the SRO interior. Since, real devices rarely behave as predicted by theoretical models few of the physical parameters can be reliably extracted from the data. However, theoretical and experimental behaviour compare closely enough to imply that conduction in SRO is thought to be dominated by Schottky emission across the SRO-substrate interface. Once this Schottky barrier is conducting, at suitably high biases, conduction across the remainder of the device is thought to be by thermionic emission at high temperatures and by a Poole-Frenkel process at low temperatures. The Poole-Frenkel process occurs by carriers hopping between defect centres surrounding silicon crystallites within the SRO. The measured barrier heights are lower than theoretical predictions because of the presence of energy states within the forbidden gap surrounding the silicon crystallites in the SRO. At high temperatures thermionic emission probably would occur by conduction in the band tails.

This was an exploratory piece of work and there are many questions as yet unanswered. Further device characterisation with films of improved reproducibility is required. Suggestions for further work have been made in the following Chapter.

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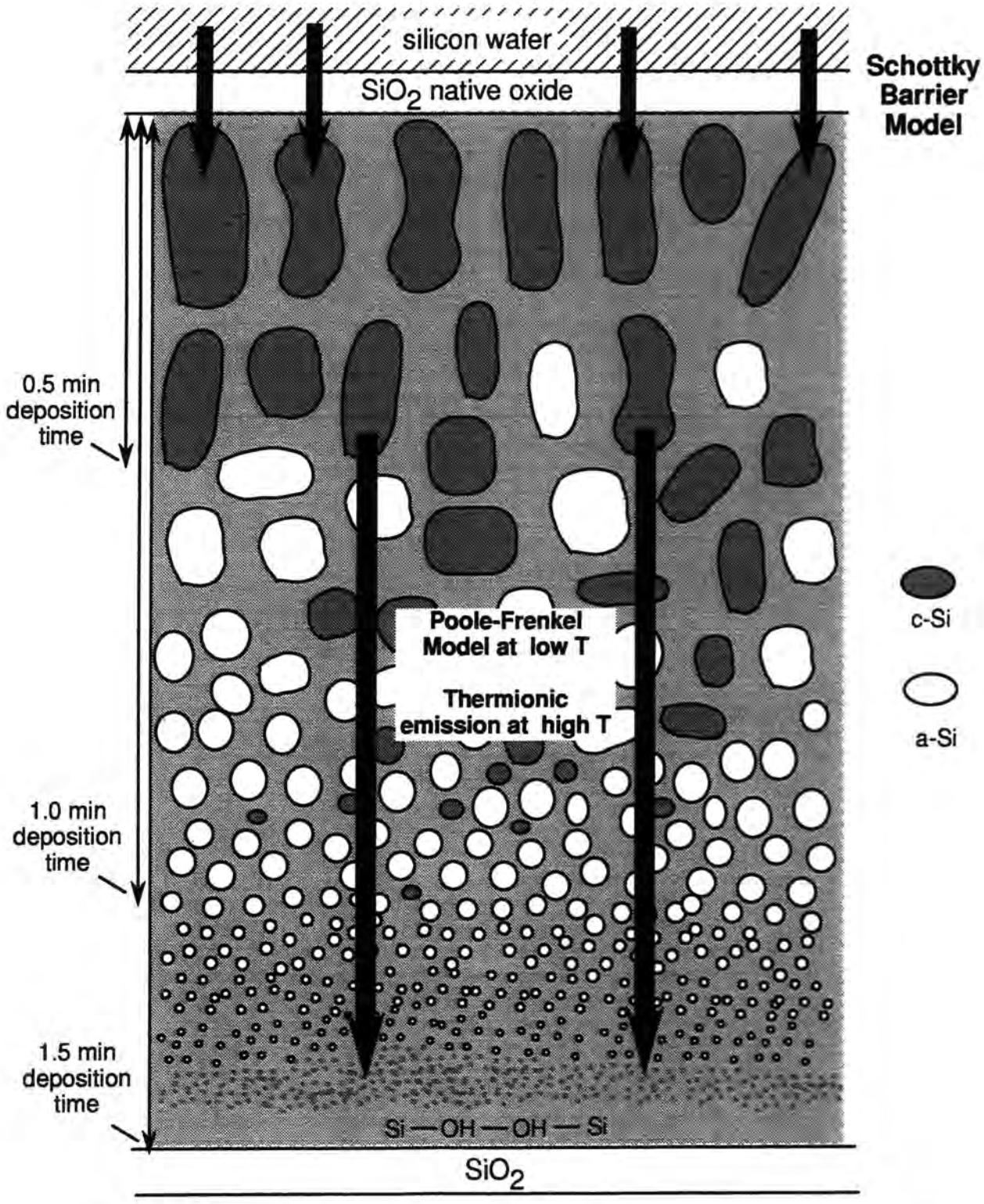

Figure 7.20 The structure of the MIS device and the conduction mechanisms associated with each part of the SRO film.

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Chapter 8

Conclusions and suggestions for further work

8.1 Introduction

This Chapter summarises the results obtained from Chapters 5, 6 and 7 and also makes suggestions for further work.

8.2 Summary of results

8.2.1 Structural properties

The SRO films deposited in the Durham APCVD reactor have three regions: some nascent oxide at the silicon interface; an oxide which is extremely silicon-rich; and a region of variable composition, becoming nearer the stoichiometric silicon dioxide at the gas-film interface. A model for the microstructure of silicon-rich oxide has been proposed. All films of SRO, grown at 650° C and a γ of 0.22, have a layer of columnar silicon. Each column is separated from the next by a silicon-rich oxide. These columns break down into islands as the oxygen content of the film increases. As the deposition time increases, the percentage of oxygen in the film increases and the average size of the silicon grains decreases. There is no SiO_x or SiO_2 around these grains but, instead, a random network which contains silicon, oxygen and silanol, (Si-OH-Si). Catalano's model [1] of a continuous solid solution of silicon and oxygen, a type of silicon dioxide alloy with some hydrogen present, is the closest description of the SRO films.

Since the film composition was found to vary with distance from the substrate and therefore with deposition time, the APCVD reactor must initially favour silicon deposition and then oxygen deposition. The growth rate was not linear. These two observations were explained in terms of the SRO film growth kinetics. Film growth kinetics are controlled by the type of reactor, the gas flow rates and the temperature of deposition. The wafer was heated from below. A change in wafer surface temperature was caused by the constant flow of cold gases. The cooler surface temperature must favour reactions that increase the oxygen content of the film. Si–O bonds are more energetically favourable than Si–Si bonds at the temperatures involved and therefore are more likely to form [2]. As the deposition time increased, more sites became occupied by N_2O until the growth rate became minimal.

The interface structures and gradual change in SRO composition have an effect on the electrical properties of the SRO MIS devices.

8.2.2 Electrical properties

Reproducibility of SRO MIS devices was maximised using voltage and temperature forming processes. The high percentages of excess silicon meant that low electric fields were required to induce charge transport across the device. There was no hysteresis observed in the readings for 'formed' MIS devices and so there was no permanent charge trapping in the oxide. Dark current values were of the order of 10^{-6} to 10^{-3} A, depending on voltage size and polarity (1 V in forward bias and 40 V in reverse bias). All devices displayed rectifying characteristics.

The time dependence of the dark currents, for formed devices, was found to be very stable in both forward and reverse bias. The current was approximately proportional to device area and edge leakage effects were shown to be negligible. Film thickness showed an equal effect in both forward and reverse bias and, therefore, could not account for the observed polarity dependence of the I-V characteristics. I-V results suggested that the influence of silicon surface contamination, insulator charges and metal-oxide interface traps and charges were far greater than the electrode material. C-V evidence indicated that Fermi level pinning occurred at the metal-oxide interface and made the device fairly immune to changes of ϕ_{ms}.

I-V data show that p-type devices required higher turn on voltages in forward bias. C-V evidence demonstrated that p-type devices had higher accumulation capacitances. Since, the oxide thickness and permittivity were similar for samples prepared in the same reactor run, the increase in capacitance was assumed to be caused by

an increase in the amount of charge at the silicon-SRO interface. This was probably caused by a higher potential barrier for holes. The p-type devices were in general less conductive than the n-type devices and, therefore, higher breakdown fields were required. This was probably due to the wider depletion width in p-type devices. At any applied voltage, lower electric fields and, therefore, higher breakdown strengths resulted.

8.2.3 Device modelling

Since the top contact metal and substrate material appeared to have little effect on the MIS device characteristics, the SRO film was assumed to be the dominant material. However, only a moderate dependence of conductivity on SRO film thickness was observed. This suggested that the silicon-SRO interface determined conduction in these MIS devices. A model was proposed for the energy bands at this interface and within the SRO film and various conduction models were applied to these structures. The rectifying behaviour, which dominated the I-V measurements, was caused by a Schottky barrier at the silicon-SRO interface. The effect of this barrier, in forward and reverse bias, was increased by the unequal number of charge carriers within the doped silicon substrate, compared with the intrinsic silicon laid down in SRO deposition. Measurements of the ideality factors for the Schottky barriers at the SRO-substrate interface showed the barriers to be far from ideal.

In forward bias, once carriers surmounted the Schottky barrier conduction across the device was probably governed by several mechanisms. Once this Schottky barrier is conducting, at suitably high biases, current flow across the remainder of the device is thought to be dominated by thermionic emission at high temperatures and by a Poole-Frenkel process at low temperatures. Parameter extraction from the Poole-Frenkel mechanism was close to that obtained from the ellipsometry measurements and gave some confidence in using this model, though the barrier height within the SRO was found to be very low. This could be caused by intermediate energy levels introduced by defects etc. within the band gap. Parameter extraction from the thermionic emission model yielded very low values for the constant A^*, as did all of the models. Thermionic emission gave the closest fit to the experimental data at high temperatures. There is a need for further investigation of the I-V behaviour of the SRO devices at temperatures above room temperature.

8.3 Suggestions for further work

8.3.1 Conduction models

There is a need for the development of mathematical models which can be applied to amorphous films, which are discontinuous in structure. Semi-continuous films, consisting of randomly arranged islands and traps, probably conduct via several mechanisms, simultaneously. Most models make assumptions which cannot be applied faithfully to real systems.

8.3.2 Temperature range

I-V measurements have shown that there appears to be several conduction regimes in the SRO films. Most published research has been carried out above room temperature and for comparison it would be worthwhile investigating the SRO grown at Durham in the temperature range 300 - 400 K.

8.3.3 Electrode material

This research suggested that the top contact metal had little influence on the I-V characteristics but the electrode material was only changed for one value of SRO film thickness. The charge in the contact-oxide interface was presumed to totally screen the effect of metal work function. Metal work functions should be further investigated for films deposited in less than two minutes. Two minute depositions were selected because it was SRO deposited in this time that were used in the successful MISS devices. Thinner films may show the effect of changing the electrode material. This is because the space charge layer, near the electrode-oxide interface, may not be wide enough to screen the effect of the metal work function. Depositions could be as low as 0.1 minutes. Should an effect be observed, then a wide range of metals could be investigated.

The effect of p- and n-type substrates could then be further investigated. It may be that one contact is able to supply more of one type of carrier than another. Again, the thinner depositions are likely to be most sensitive. Substrate resistivity has been shown to have little effect on the MIS device characteristics. MISS devices are sensitive to changes in dopant concentration. To assess this effect more accurately a range of n- and p-type substrates with varying substrate resistivities (and doping levels) would need to be investigated. Even the relative position of the two wafers, on

the APCVD reactor susceptor should be exchanged to minimise or account for errors in film depth reproducibility.

A charge layer is thought to form at the silicon-oxide interface. This space charge may change with substrate material. It would be interesting to investigate MIS characteristics for substrates other than silicon.

8.3.4 Breakdown

MIS devices with an aluminium top contact could be broken down by current flow in excess of the 2 mA used in this work. An electron microscope would reveal any structural changes that occurred, in particular the presence of any microscopic holes in the aluminium top contact.

8.3.5 Annealing

Annealing changed the I-V characteristics of the SRO MIS devices. It would be worthwhile to investigate fully the effect of annealing on the structure of the film. Annealing should be performed at sequentially higher temperatures with the anneal time held steady at two hours to determine the critical temperature, should one exist for the Durham films. This critical temperature should become apparent from the I-V characteristics. Each anneal temperature should be investigated from one minute to several hours. Capacitance-Voltage (C-V) curves should be obtained to observe the flatband shift. C-V curves should be measured at high and low frequencies for annealed films at various temperatures and for a range of SRO deposition times.

Electrical measurements alone cannot identify the chemical reactions that occur during the annealing of interface traps and fixed oxide charges. Structural and compositional analysis techniques should be used to determine whether annealing increases crystal size, produces SiO_2, reduces voids and reduces film thickness. Crystal size depends on the time taken for the silicon to diffuse through the oxide. If crystal size dominates conduction, then the longer the anneal time, the greater the effect on the I-V characteristics [3]. If the silicon crystallites drop negligible voltage, then if they grow in size, more of the applied voltage must be dropped across the oxide portion of the film. The distribution of the electric field would change. Again, this should be apparent from I-V measurements. The thickness of the film should be determined immediately before and after the anneal. A reduced film thickness may be due to a reduction in the number of voids [4]. The increased order observed in the RHEED

analysis photographs [5] could be related to void reduction and may therefore have little to do with the silicon crystal size. Fewer voids may also increase conduction in these films.

Details of the microscopic electric fields between the tiny silicon islands in SRO and how these fields are influenced by size, shape and density of the islands is clearly beyond the scope of this study. If SRO films could be manufactured that were equal in all aspects, except for these parameters, then interface states could be ignored and the importance of the silicon islands determined.

If the average silicon island size were determined then photoconductivity measurements could be carried out to determine whether there was a Coulombic attraction between the silicon sites which may reduce the potential barriers between silicon islands [6].

8.3.6 Structural analysis

In addition to the structural analysis suggested in the above section, Transmission Electron Microscopy (TEM) could be used on films deposited from 0.1 to 1 minute. This may reveal the point at which the columnar silicon breaks up into islands. Comparisons between these thin films may provide insight into the effects of interface charge. For SRO depositions of less than 0.5 minutes, there may be short circuits due to these growths of columnar silicon. If the structures observed at the silicon-SRO interface are not columnar silicon then short circuits are less likely to occur. Scanning Electron Microscopy (SEM) on films deposited in 0.1 to 1 minute may also give an indication of when these columns start to thin and break up into islands. Electrical measurements could then be linked to the interface structure. Very thin samples may be expected to behave as ideal Schottky diodes. This work would determine whether the silicon-oxide interface is all-important in controlling current flow or whether fixed oxide charges within the SRO play an important role.

8.3.7 Equipment

Some workers have reported that when annealing samples, oxidation inadvertently took place. It would be advantageous to determine whether oxidation of samples occurs in the nitrogen annealing furnace at Durham. This would aid characterisation of the MIS devices. The installation of the mass flow controllers aided reproducibility of device manufacture. Warming the gases before entry to the APCVD reactor

chamber should be investigated. This may further aid reproducibility. It may change the structure of the film to a more uniform composition and so alter the electrical characteristics. A thorough compositional analysis of the film could then be linked to any changes in the electrical properties. Reproducibility of the MIS devices has been shown to be poor. More reproducible films may be obtained by using a Low Pressure Chemical Vapour Deposition Reactor LPCVD or a Plasma Enhanced Chemical Vapour Deposition reactor PECVD.

This research has been a first attempt at characterising the Durham SRO films and therefore has been exploratory in nature. In particular, it is hoped that future workers will use this as a starting point for further development of the elucidation of the conduction mechanisms associated with SRO films.

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Appendix A

Image Force Lowering

A.1 The metal-vacuum system

An electron in the vicinity of a metal surface induces a positive charge on the metal surface. The charges then attract each other with a force equivalent to that force between a negative and positive charge at equal and opposite distances from the surface. The likeness to a mirror image can be seen in Figure A.1. This force is called the image force and is given by $F_{i(x)}$

$$F_{i(x)} = \frac{-q^2}{4\pi\epsilon_0(2x)^2} \tag{A.1}$$

where q is the electronic charge, ϵ_0 the permittivity in a vacuum and x is the distance of each charge from the metal surface.

If there were no forces present the energy an electron would have when completely free from the influence of the metal is called the force-free vacuum level, E_0. This is a reference for electron energy levels and is usually taken to be zero. If forces are present then the energy an electron would have at rest, outside of the metal is the local vacuum level, E_l. The electrostatic energy, E, associated with the image force is the work done in moving the electron from point x to the vacuum level.

$$E = \int_x^\infty F\,dx = \int_x^\infty \frac{-q^2}{16\pi\epsilon_0 x^2} \tag{A.2}$$

$$E = \frac{-q^2}{16\pi\epsilon_0 x} \tag{A.3}$$

When an external applied field, $\mathcal{E}$, is applied the total potential energy as a function

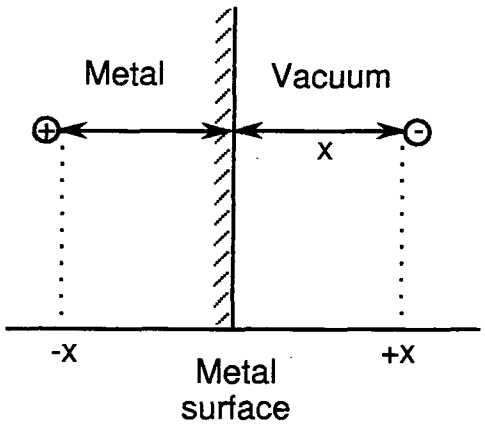

Figure A.1 Diagram showing the image force charge induced by an electron near a metal surface.

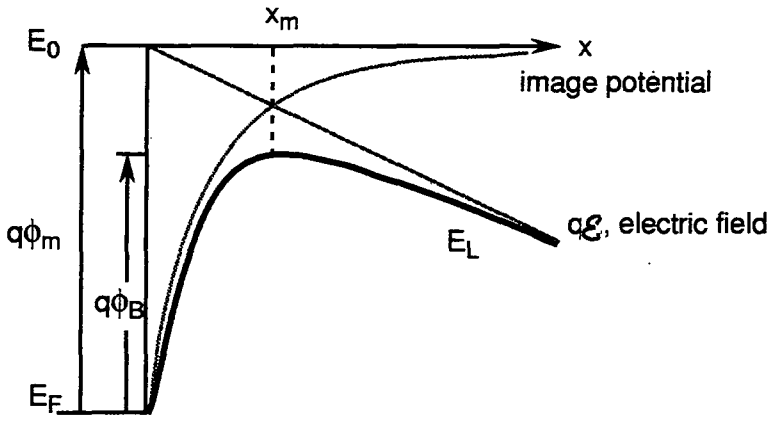

Figure A.2 Image force barrier lowering.

of distance (measured downward from the x axis) is given by the sum

$$E_l = \frac{q^2}{16\pi\epsilon_0 x} + q\mathcal{E}x \tag{A.4}$$

The image force lowers the potential energy for charge carrier emission. For high fields the barrier is considerably lowered and the effective metal work function for thermionic emission is reduced, from $q\phi_m$ to $q\phi_B$ as shown in Figure A.2. The position of maximum barrier is no longer at $x = 0$ but is now at a new position $x = x_m$. The value of x_m can be found by equating $dE_l/dx = 0$ and using equation A.4 for E_l this gives

$$\frac{d}{dx}\left(\frac{-q^2}{16\pi\epsilon_0 x} - q\mathcal{E}x\right)_{x=x_m} = 0 \tag{A.5}$$

Solving for x_m leads to

$$x_m = \sqrt{\frac{q}{16\pi\epsilon_0\mathcal{E}}} \tag{A.6}$$

$\Delta\phi_B$ is the barrier lowering and is given by evaluating the potential at $x = x_m$. The equation for the potential is the equation for the total potential energy (equation A.4 divided by the electronic charge, q, and is

$$\Delta\phi_B = \frac{q}{16\pi\epsilon_0 x_m} + \mathcal{E}x_m \tag{A.7}$$

Dividing throughout by x_m and substituting on the right-hand side for x_m from equation A.6 gives

$$\frac{\Delta\phi_B}{x_m} = \frac{q}{16\pi\epsilon_0}\left(\frac{16\pi\epsilon_0\mathcal{E}}{q}\right) + \mathcal{E} \tag{A.8}$$

$$\Delta\phi_B = 2\mathcal{E}x_m \tag{A.9}$$

Substituting for x_m

$$\Delta\phi_B = 2\mathcal{E}\sqrt{\frac{q}{16\pi\epsilon_0\mathcal{E}}} = \sqrt{\frac{q\mathcal{E}}{4\pi\epsilon_0}} \tag{A.10}$$

A.2 The metal-semiconductor system

The image force lowering may be approximated in the metal-semiconductor system by [1]

$$\Delta\phi_B = \left(\frac{q\mathcal{E}}{4\pi\epsilon_s}\right)^{1/2} \tag{A.11}$$

where ϵ_s is the permittivity of the semiconductor. Since ϵ_s is approximately 12 times the value of ϵ_0, $\Delta\phi_B$ is not as great with the semiconductor as with the metal alone. However, at high fields the barrier lowering or Schottky effect is significant. Figure A.3 shows the band bending in the semiconductor. The Schottky effect for different biasing conditions is shown in Chapter 2. The lower the metal potential the lower the barrier. There are two components which make up the local vacuum energy level in the semiconductor. The first is the electrostatic energy associated with the image force $E_{l(i)}$,

$$E_{l(i)} = \frac{-q^2}{16\pi\epsilon_0 x} \tag{A.12}$$

The second component is due to the space charge $E_{l(s)}$. Consider Poisson's equation

$$\frac{d^2\psi}{dx^2} = -\frac{\rho(x)}{\epsilon} \tag{A.13}$$

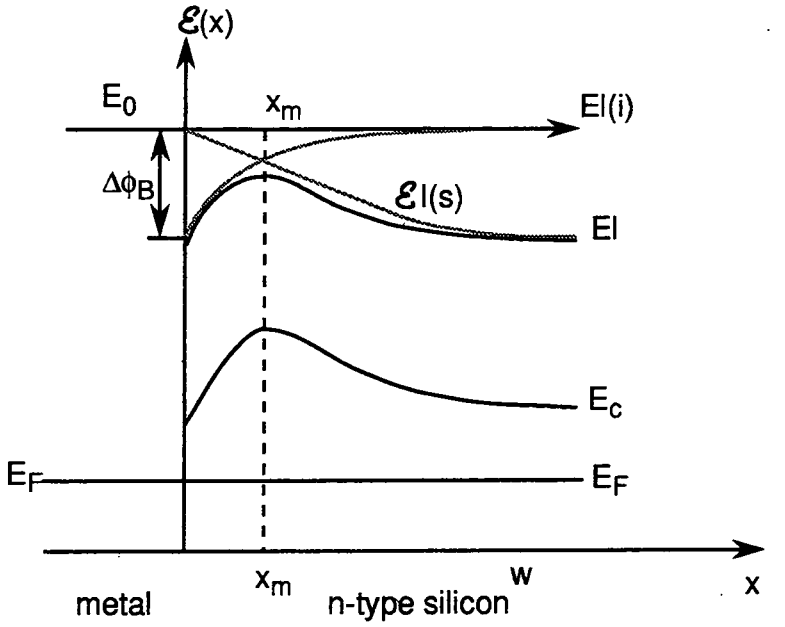

Figure A.3 Image force lowering and semiconductor band bending.

Let $\rho(x) = qN_D$ where N_D is the doping density.

$$\frac{d^2\psi}{dx^2} = -\frac{qN_D}{\epsilon} \tag{A.14}$$

Integrating the above gives

$$\mathcal{E} = -\frac{d\psi}{dx} = \frac{qN_D x}{\epsilon} + c \tag{A.15}$$

Let w be some width in the semiconductor so that when $x = w$, $\mathcal{E} = 0$. At w, $c = -qN_D w/\epsilon$

$$\mathcal{E} = \frac{qN_D x}{\epsilon} - \frac{qN_D w}{\epsilon} \tag{A.16}$$

Since the definition of electric field intensity is force per unit charge then $F = q\mathcal{E}$. The electrostatic energy associated with the space charge is

$$E_{l(s)} = \int_x^\infty F\,dx = \int_x^\infty q\mathcal{E}\,dx \tag{A.17}$$

and substituting for $\mathcal{E}$ from equation A.16

$$\frac{q^2 N_D}{\epsilon}\left(\frac{x^2}{2} - wx\right) \tag{A.18}$$

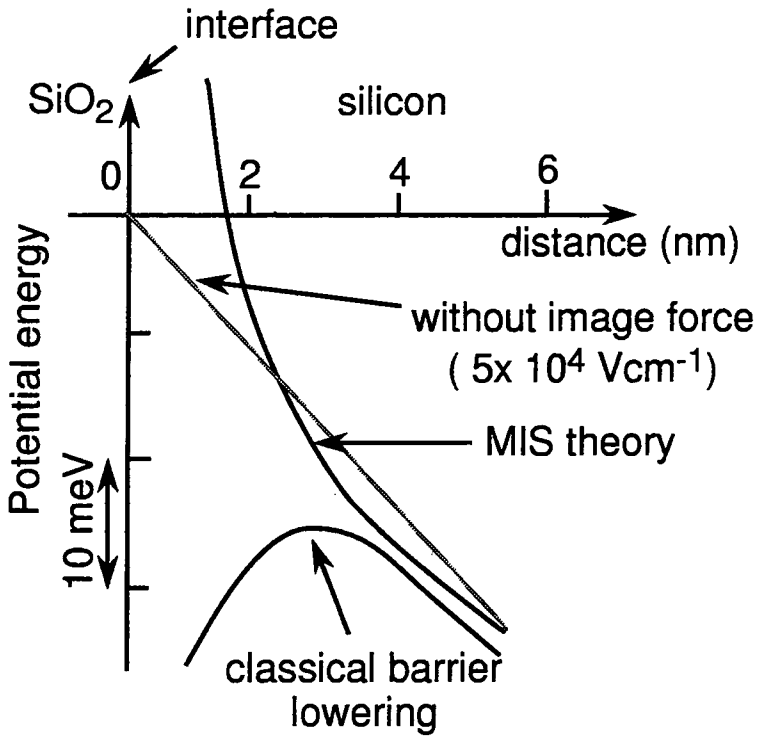

Figure A.4 A summary for the local electric field patterns for classical image force lowering, zero image force lowering and image force heightening of the metal-insulator barrier.

and therefore

$$E_{l(s)} \propto \left(\frac{x^2}{2} - wx\right) \tag{A.19}$$

If $w \gg x$ the term in brackets tends to have negative values.

The two components added together produce the resultant local vacuum level.

$$E_l = E_{l(s)} + E_{l(i)} = \frac{-q^2 N_D}{\epsilon}\left(wx - \frac{x^2}{2} + \frac{1}{16\pi N_D x}\right) \tag{A.20}$$

The form of E_l is shown in Figure A.4. Since all levels follow the vacuum level the barrier in the conduction band is also lowered by the image force. At $x = x_m$, $dE/dx = 0$. Therefore

$$\frac{-q^2 N_D}{\epsilon}\frac{d}{dx}\left[(wx - \frac{x^2}{2}) + \frac{1}{16\pi N_D x}\right] = 0 \tag{A.21}$$

and

$$w - x = \frac{1}{16\pi N_D {x_m}^2} \tag{A.22}$$

If $x \ll w$

$$x_m = \left(\frac{1}{16\pi N_D w}\right)^{1/2} \tag{A.23}$$

By a similar method to that shown in the metal-vacuum case it can be shown that

$$\Delta\phi_B \approx \frac{q}{\epsilon}\sqrt{\frac{wN_D}{4\pi}} \tag{A.24}$$

Image force lowering, therefore, occurs in reverse bias and depends upon the permittivity of the material on top of the metal and on the doping density and the size of the electric field applied.

A.3 The MIS system

The situation for an MIS system is not so clear cut. The image charge, q' is given by [2]

$$q' = \frac{-q(\epsilon_s - \epsilon_i)}{\epsilon_s + \epsilon_i} = -q\beta \tag{A.25}$$

Rearranging for β

$$\beta = \frac{\epsilon_s - \epsilon_i}{\epsilon_s + \epsilon_i} \tag{A.26}$$

Usually $\epsilon_i < \epsilon_s$ and therefore $\beta > 0$ and this makes q' negative. The image force repels the electron rather than attracting it. The barrier to electron flow increases in the semiconductor rather than becomes lower.

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Appendix B

Fabrication Techniques

This appendix describes the processes involved in device fabrication in more detail.

B.1 Wafer cleaning

The slice was placed in a jig and boiled for 5 minutes in 1,1,1 trichloroethane and then repeated in with fresh solution. Acetone could have been used instead of 1,1,1 trichloroethane since it is more environmentally friendly. The beaker was placed in the ultrasonic bath for 2 minutes Propan-2-ol was used to rinse the slice and it was given a final rinse in deionised water. A 'bomb' was prepared by adding 1 part (by volume) concentrated sulphuric acid to 1 part (100-volume) hydrogen peroxide (always add the sulphuric acid to the hydrogen peroxide and never vice-versa) in a glass beaker. The sample (suspended in a jig), was immersed in the 'bomb' and heated via a water bath for 30 minutes. It was then rinsed in deionised water. The bomb oxidises the silicon surface and trapped impurities within the oxide layer. These impurities were then removed along with the oxide using a 10% HF solution. This solution consisted of 1 part 49% HF to 9 parts deionised water.

The wafer was dipped in this solution for 2 minutes and then dipped in deionised water. When clean, the silicon slice was hydrophobic. The wafer was then thoroughly rinsed in deionised water and placed in the recirculator for an hour or until the measured resistivity of the water was in excess of $10^7\,\Omega\,\mathrm{cm}$.

B.2 Growing the field oxide

The samples were placed in the mouth of the furnace (in a quartz boat) for 10 minutes in nitrogen. This allowed them to dry and prevented thermal shock. They were then slowly pushed to the centre of the furnace. After 10 minutes, which allowed them to reach maximum temperature, the nitrogen was turned off and dry oxygen passed over the wafers. After a further 10 minutes a low carrier gas of nitrogen was applied with wet oxygen, the gas having passed through deionised water. The oxidation ran over a 24 hour period and at the end of this period dry oxygen was again applied. The boat was pulled to the furnace mouth and left there in nitrogen until the wafers were required.

B.3 Photolithography

B.3.1 Mask making

The masks were first designed on graph paper and then the design copied onto sheets of Rubylith. One sheet of Rubylith, (20 cm x 20 cm), was used for each mask. The Rubylith was held fast on a lightbox to which was attached a sharp cutter mounted on a manoeuverable arm. The cutter was moved to a precise location and the Rubylith scored without damaging the clear plastic sheet underneath. Once the design was complete the opaque red material was peeled from its clear plastic backing. Any mistakes could be rectified by placing ruby-coloured adhesive tape over places where the material was wrongly cut away. The Rubylith original was then mounted on a lightbox and was photographed in a clean, dark, vibration-free environment. The camera and light screen were precisely positioned so that the image was centered and in focus at the back of the camera. High resolution photographic (HRP) plates were loaded into the backslide in the darkroom and the backslide loaded into the camera. The HRP plates were exposed for 6 minutes at f22. The backslide was then inverted and the next mask exposed. Once exposed the plates were developed using the following solutions:

(i) Clearing bath (1 part to 3 parts water);

(ii) Developer (1 part to 4 parts water);

(iii) Fixer (250 cm^3 solution A; 28 cm^3 solution B; 750 cm^3 water).

Temperature (°C)	Time (min-sec)
18	6
20	5
22	4–20
24	3–30
26	3
28	2–30
30	2

Table B.1 Mask developing times for various solution temperatures

The clearing bath was poured into a small developing tank and the fluid agitated for 30 seconds, before being discarded. This process was repeated twice with water. The developer was added to the tank and the solution agitated occasionally throughout the developing time, which varied with temperature as in Table B.1 below:

At the end of this time interval the developer was removed and the fixer added for 1 minute. The plates were then rinsed in water twice as above. The developed plates were placed in the ultrasonic bath, in water, for 1 minute and finally dried in the laminar flow cabinet. The area reduction was 1:134 and a negative image was produced on glass slides, which were then mounted in the aligning machines when required for wafer processing.

B.3.2 Wafer processing

The sample was removed from the furnace and placed immediately onto a vacuum spinner. Eight drops of photoresist (Microposite S1813) were applied and the sample spun for 30 seconds. The evenly coated wafer was then removed and placed on the hot plate at at temperature of 80 °C for 15 minutes. The mask was loaded into the mask aligner, emulsion face down. Once soft-baked the sample was placed onto the vacuum chuck and was aligned with the mask. When correctly aligned the mask and wafer were brought into contact and the automatic timing sequence for exposure started. The UV light impinged onto the positive working photoresist through the device mask for 20 seconds. After exposure the wafer was automatically ejected. The pattern was then developed in photographic developer, Microposite MF312 for 60 seconds and then the sample was thoroughly rinsed 5 times in deionised water. After drying with a hot air blower, excess photoresist was removed from the back of the sample, which

was then hard baked at 120 °C for 30 minutes The samples were not removed from the hot plate until they were to be etched, otherwise the photoresist has been found to deteriorate.

B.4 Etching the field oxide

1 part 49% hyrdofluoric acid and 4 parts 40% ammonium fluoride made up the buffered HF used to etch the field oxides. This process took several minutes for deep field oxides and the wafers were immersed until, upon dipping in deionised water they were hydrophobic. Buffered HF was removed from the sample by rinsing 5 times in deionised water and the remaining photoresist was removed in 'remover', Microposite Remover 1112A. The sample was placed in remover in the ultrasonic bath for 30 seconds and then in acetone in the ultrasonic bath for a further 30 seconds. Fresh acetone was then used again if necessary. The field oxide samples were then placed in recirculating deionised water until the resistivity of the return flow of water was $10^7\,\Omega\,\mathrm{cm}$. This usually took one hour.

B.5 Cleaning

The samples were cleaned in a bomb as outlined above for 20 minutes prior to being placed in the CVD. The wafers were etched in 10% HF for 10 seconds. The samples were thoroughly rinsed in deionised water as above and were placed in the recirculator. Once the return flow meter read $10^7\,\Omega\,\mathrm{cm}$ each sample was removed, dried in nitrogen and placed on the CVD susceptor as quickly as possible.

B.6 Chemical vapour deposition (CVD)

The CVD reactor was purged with nitrogen, for 10 minutes in vent mode, before and after after the heater was switched on and allowed to reach its set point of 650°C. This ensures that the air was removed to allow minimum surface oxidation of the wafer. The nitrogen carrier gas, silane and nitrous oxide were all set to pre-set values using the mass-flow controllers (N_2O – 13ml/min; SiH_4 – 61.3ml/min; N_2 – 35l/min) The gases were allowed to flow for 3 minutes in vent mode and were then applied to the reaction chamber for the required deposition time.

After completion of the film deposition the valves were closed and the sample purged in nitrogen for 20 minutes as it cooled. Each step in the sequence was precisely timed to ensure that each device was subjected to precisely the same process.

B.7 Evaporation of aluminium

The samples were held under vacuum until the top contact was to be applied. Aluminium deposition was carried out in the Varian High Vacuum system at a pressure of 10^{-7} mbar. An emission current of 400 mA was used in six second pulses with a period of ten minutes between each pulse until the desired thickness of aluminium was built up.

B.8 Etching aluminium

Photoresist was applied and the sample was soft baked at 80°C. The aluminium could not be hard baked at 120°C because acetone cannot remove hard-baked photoresist from the back of the wafer and proprietary remover also dissolved aluminium. UV light patterned the photoresist, which was developed as described earlier. The aluminium was etched in 90 parts concentrated orthophosphoric acid: 6 parts concentrated nitric acid and 10 parts deionised water for one to two minutes and then the sample was thoroughly rinsed and returned to the circulator for one hour. The remaining photoresist was removed in acetone, applied twice in the ultrasonic bath for 30 seconds. After being blow dryed in nitrogen the samples were placed in an evacuated dessicator until needed for the back contact preparation.

B.9 Lapping the back of the wafer

The wafer was placed face-down on a large piece of PTFE tape. A small quantity of diamond paste was placed on the back of the slice together with a drop of lapping fluid. A PTFE rod was used to polish the slice for 10 minutes. The slice was then cleaned in acetone twice and then rinsed in isopropyl alcohol in the ultrasonic bath for 30 seconds. After drying with a hot air blower, a drop of 10% HF was carefully painted onto the back of the wafer to remove any oxide and the wafer was immediately placed in the gold evaporator.

B.10 Gold evaporation

Gold evaporation was carried out at a pressure of 10^{-5} to 10^{-6} mbar. A current of 30 A was used over two minutes and the process was repeated after the pressure recovers. The back contacts were checked to see how ohmic they were and also that the resistance was reasonably low, of the order of 200 Ω.

B.11 Molybdenum evaporation

Molybdenum was evaporated under exactly the same conditions as for aluminium as an alternative top contact. The aluminium etch was also used to etch molybdenum.

B.12 Chromium evaporation

Chromium was evaporated under inferior pressure conditions, i.e. at 10^{-6} mbar. Gold was immediately deposited on top of the chromium in the same evaporator. The top contact was then patterned using the photolithography techniques described earlier and the gold etched with iodine in potassium iodide. The gold was then used as a protective layer and the underlying chromium etched with potassium ferricyanide (K_3FeCN_6).

Appendix C

Gold Wire Bonding

C.1 Cratering

The shear test reveals weak bonds and is also a measure of damage to the layers under the bond pad. This damage is termed cratering, because in extreme cases overbonding causes a crater under the bond and a divot appears attached to the wire. More frequently, the defects are less severe and although there is no visible damage, the devices are degraded. Marginal cratering is thought to cause leakage between underlying layers. Winchell [1] found that cratering is prevalent in very thin metallisations ($< 0.6\,\mu$m). He found that for 1–3 μm the surface damage is undetectable provided that the correct machine set-ups are used. Hardness of bond pad metals have shown ambiguous results but hard interfacial layers of titanium and tungsten help to prevent cratering [2]. Excessive ultrasonic energy and also one ball bond on top of another was found to increase cratering. This has been reported by other workers [3]. The performance of the gold ball bonder should be optimised to ensure that the ultrasonic power applied is minimised and the static bonding force used is neither too high nor too low. These machine parameters are largely responsible for efficient energy transfer, which, in turn, makes the total energy requirements of the bond as low as possible and, therefore, minimises the risk of cratering.

C.2 Cleaning pads

Optimum bonds result if there are no impurities at the interface between pad and wire. Plasma cleaning can be used to improve bondability. The samples, aluminium pads or gold plated pcbs were placed in an evacuated chamber and oxygen and/or argon

introduced for 10 minutes at 0.1 mbar. The mechanism is thought to be that oxygen molecules become separated and/or ionised. They react with hydrocarbons to form water and carbon dioxide and are pumped out with the gaseous plasma. Sputtering of other contaminants also occurs. Since argon has twice the atomic weight of oxygen, the cleaning process is, in general, twice as long if argon is used. RF powers should be limited to below 300 W [4].

Problems can occur when using plasma cleaning, for example, when using oxygen plasma on silver, the metallisation becomes blackened and bondability reduces. Argon, introduced at the end of the oxygen cleaning process, restores this [5]. Some CMOS devices show an increased threshold voltage after plasma cleaning, however 200 to 300 °C for 20 minutes has been found to restore this voltage [6]. This problem is thought to be caused by gaseous ions impinging on the device insulators, causing electron-hole pair generation. The holes drift to the silicon interface and are trapped. An interface charge develops and shifts the operating point of the device.

Once a device has been cleaned it becomes recontaminated during storage. A period up to 2 hours is acceptable before bonding [7]. If stored for longer the device should be recleaned.

C.3 Intermetallic compounds

Good bonds may become weak with time. This is sometimes caused by the presence of intermetallic compounds. Gold-aluminium bond failures tend to be impurity driven or corrosion reactions. The much documented purple plague ($AuAl_2$) occurs if the temperature-time product is large enough [8, 9, 10] and so a few monolayers form, even at room temperature. There are several phases of gold-aluminium namely: $AuAl_2$, Au_2Al, Au_5Al_2, AuAl and Au_4Al. The presence of these compounds does not mean bond failure since they are mechanically strong, though brittle, and are electrically conductive. They are, however as stated above, susceptible to degradation by impurities and corrosion. Kirkendall voids form around the periphery of the bonds and so limit the available conduction paths. These voids are caused by one of the metals of the bond diffusing out of one region, faster than it can diffuse in from the other side. Kirkendall voiding is limited by restricting the availability of one of the metals and therefore thin films are thought to make more reliable bonding pads. Horsting [11] discovered that impurity particles accelerated AuAl bond failures by acting as vacancy sinks and so cause Kirkendall voids. Thin films contain less grain

boundaries, impurities etc. and so this could be another reason for keeping bonding pad metallization thin. The fact that, the intermetallic compounds are brittle means that fracture can occur with thermal-cycle induced flexure.

C.4 Bonding wire loop height

Tests have revealed that the bond pull force is related to the ratio between loop height to bond spacing [6]. Higher loops, therefore, mean stronger bonds. Wire bonds have been found to suffer from a flexure fatigue due to thermal or power cycling. High loops reduce bond failure caused by such cycling and a minimum height to bond length ratio is recommended at 4:1 [3].

C.5 Pcb metallisation

Copper-aluminium intermetallic compounds can form. The Al_2Cu phase tends to lead to corrosion of the bond pad if moisture and traces of halogen are present. When such corrosion occurs the metal becomes brown or black and the device should be disused. Copper causes aluminium pads to be harder to bond and the extra ultrasonic energy needed increases the possibility of cratering.

Thallium, lead and arsenic are commonly added to gold-plating solutions as grain refiners to speed up the plating process. Arsenic increases bond strengths but thallium and lead have been found to cause bond failures [12]. Hydrogen has also been found to cause problems [11]. The following reduces hydrogen content in gold plating:

(i) keep the current density low;

(ii) agitate the solution;

(iii) keep the gold concentration up;

(iv) keep the bath temperature low;

(v) low plating rates give better results and if hydrogen is observed at the cathode the rate should be reduced.

Pcbs can be annealed at 350 °C to remove hydrogen. Joshi and Stanwald [13] produced a time schedule for this as shown in Table C.1 below.

Temperature (°C)	Annealing time (hours)
150	50
175	29
200	18
250	8
300	4
350	2.25
390	1.5

Table C.1 The hydrogen anneal times for pcbs at various temperatures

Ideal gold films should be soft and nodular, not shiny in appearance, with less than 50 ppm total of Ni, Cu or Pb impurities. It is not possible to bond onto gold films which contain Chromium, this is removed using ferric ammonium nitrate [14]. Titanium oxidises and reduces the bondability of gold films. This is removed with a 10:1 dilute solution of HF, HNO_3 etch [15]. It is possible to bond onto pure copper but the copper oxide is thought to act as a lubricant at the bond interface and therefore must be removed first.

C.6 Metal systems

Mono-metal pads and wires appear to be reliable. Gold-gold systems improve with time. Aluminium-aluminium systems are also extremely reliable and improve with time but weaken at high temperatures. Gold-silver bonds are reliable over long times at high temperatures.

When choosing new metallization systems the following should be taken into consideration:

(i) check the welding handbook to ensure it can be welded ultrasonically;

(ii) the presence of a soft oxide prevents bonding and so this must be removed. Nickel and copper can be bonded by gold but their soft oxide reduces bondability;

(iii) since gold is a soft wire cratering is minimised;

(iv) intermetallic compounds should have a melting point greater than 1000 °C, if less than 500 °C bondability is likely to be poor;

(v) the electrochemical series should be checked to ensure that one metal is not very electro-positive and the other negative since corrosion would then occur.

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