Effect of wearout processes on the critical timing parameters and reliability of CMOS bistable circuits

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Abstract

The objective of the research presented in this thesis was to investigate the effects of wearout processes on the performance and reliability of CMOS bistable circuits. The main wearout process affecting reliability of submicron MOS devices was identified as hot-carrier stress (and the resulting degradation in circuit performance). The effect of hot-carrier degradation on the resolving time leading to metastability of the bistable circuits also have been investigated.

Hot-carrier degradation was identified as a major reliability concern for CMOS bistable circuits designed using submicron technologies. The major hot-carrier effects are the impact ionisation of hot-carriers in the channel of a MOS device and the resulting substrate current and gate current generation. The substrate current has been used as the monitor for the hot-carrier stress and have developed a substrate current model based on existing models that have been extended to incorporate additional effects for submicron devices. The optimisation of the substrate current model led to the development of degradation and life-time models. These are presented in the thesis.

A number of bistable circuits designed using 0.7 micron CMOS technology design rules were selected for the substrate current model analysis. The circuits were simulated using a set of optimised SPICE model parameters and the stress factors on each device was evaluated using the substrate current model implemented as a post processor to the SPICE simulation.

Model parameters for each device in the bistable were degraded according to the stress experienced and simulated again to determine the degradation in characteristic timing parameters for a predetermined stress period. A comparative study of the effect of degradation on characteristic timing parameters for a number of latch circuits was carried out. The life-times of the bistables were determined using the life-time model. The bistable circuits were found to enter a metastable state under critical timing conditions. The effect of hot-carrier stress induced degradation on the metastable state operation of the bistables were analysed.

Based on the analysis of the hot-carrier degradation effects on the latch circuits, techniques are suggested to reduce hot-carrier stress and to improve circuit life-time. Modifications for improving hot-carrier reliability were incorporated into all the bistable circuits which were re-simulated to determine the improvement in life-time and reliability of the circuits under hot-carrier stress. The improved circuits were degraded based on the new stress factors and the degradation effects on the critical timing parameters evaluated and these were compared with those before the modifications. The improvements in the life-time and the reliability of the selected bistable circuits were quantified. It has been demonstrated that the hot-carrier reliability for all the selected bistable circuits can be improved by design techniques to reduce the stress on identified critically stressed devices.

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Declaration

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Chapter 1

INTRODUCTION

As integrated circuit processing has advanced in recent years, the reliability of sub micron Complementary Metal Oxide Semiconductor (CMOS) bistables has been critically affected. One cause of this is timing errors introduced by wearout processes as a result of process tolerances and device degradation during normal operational life of the circuit. Increased semiconductor complexity and reduced feature sizes for devices have emphasised the need for greater understanding of the physical processes affecting the reliability of Very Large Scale Integrated (VLSI) circuits. For sub-micron devices, variations in their parameters due to fabrication tolerances and limited process control become larger on a percentage basis [1.1]

The two major failure classifications affecting the reliability of VLSI circuits are catastrophic failures and wearout failures. Catastrophic failures such as junction breakdowns, oxide breakdown and electrostatic discharge initiated breakdowns have been thoroughly investigated by many researchers. Wearout failures due to hot-carrier effects have become a major issue for submicron devices. Research has been going on for many years and have gained a very good understanding of the physical processes leading to the generation of hot-carriers in a MOS device and the damaging effects it can cause. But the degradation effects of hot-carriers on the various characteristic timing parameters of digital VLSI circuits have not been fully understood mainly because of the cumulative effects of time dependant degradation on individual devices in a large integrated circuit are difficult to assess. Furthermore, in comparison with combinational circuits, bistable circuits have been relatively neglected by many researchers. This may be due to the effects of positive feedback which can compensate for defects in many cases making the circuit less susceptible and preventing fault detection. The scaling of MOS transistors to submicron dimensions has caused degradation mechanisms to become a significant problem which needs to be addressed as a matter of priority.

CMOS has emerged as the dominant technology for VLSI digital circuits. In VLSI and ULSI systems, the low power and high packing density afforded by advanced CMOS process is vital. The increased circuit complexity was made possible by shrinking device geometry using scaled down MOS devices. Because the operating voltage is not scaled down proportional to the device geometry reduction, the electric fields in the channel of the devices have increased dis-proportionately. The high fields in the channel of MOS devices led to the phenomenon of hot-carriers giving rise to a number of problems in the channel, oxide layers and the depletion regions. Hot carriers can cause degradation in device characteristics and the overall reliability

of the circuit is affected. Hot-carrier degradation occurs in the field and so it is not very easy to assess the impact on reliability of the VLSI circuits at the design and testing phase unless field testing data is made available. In this context, it is important to consider the hot-carrier induced changes in electrical variables and the effects of these on the timing parameters of important VLSI circuit elements such as bistables. This information can be used to design a reliable bistable which when incorporated into a VLSI circuit will enhance the overall reliability of the circuit.

1.1 Objectives of the research

The main objective of the research was to establish the effects of CMOS wearout processes (not catastrophic failures) on the reliability of representative bistable circuits. One of the main factors affecting the reliability which is metastability in the bistables and the conditions which cause changes in the metastable behaviour of the bistable and hence eventual failure of the circuit have been investigated. Solutions to the problems caused by wearout have also been investigated. Device design techniques for reducing the effects of wearout processes on the timing performance of bistables have been proposed at the end of the thesis.

In this thesis we describe the hot carrier induced damage mechanisms and how to model the effects of degradation on MOS devices on the characteristic timing performance of bistable circuits designed using standard CMOS technology. All the identified known degradation effects due to hot-carriers have been incorporated into the hot-carrier degradation model which is based on a substrate current model to monitor stress levels on all the devices in a bistable circuit. Available data from other researchers have been used to characterise the degradation effects on the electrical parameters of the devices. AC degradation models were generated from dynamic stress simulations of the bistables and by processing the time varying current and voltage wave forms employing quasi-static analysis. Identified SPICE device model parameters have been used to incorporate the degradation effects and subsequent circuit simulations using degraded SPICE models were used to establish the timing performance degradation in the bistable circuits. Comparison of various forms of bistables simulated under identical conditions led to the identification of circuit forms which are less susceptible to hot carrier effects. Effects of hot carrier degradation on metastability behaviour has been investigated and bistable circuits which have better resistance to metastability have been identified. An understanding of the circuit configurations and stress levels leading to hot-carrier degradations led to proposals for circuit designs with improved reliability. The detailed analysis of the selected circuits simulated using the proposed design improvements have been used to quantify the reliability improvements in the cases under analysis.

1.2 The need for the research

The development of submicron CMOS technology has introduced a number of new factors into the reliability equation. The intrinsic wearout failure mechanisms such as hot carrier degradations are becoming an important factor in VLSI circuits. Wearout processes occur in all CMOS circuits although the time to failure may vary greatly. Manufacture of VLSI circuits now is based upon accurate simulation and estimation of the reliability of the circuit. Hence we need an accurate model to predict the stress levels on the various devices in a circuit under normal operating conditions.

Unfortunately for sub micron VLSI circuits, the reliability implications due to wearout processes such as hot carrier effects and electromigration have not been fully investigated and assessed before manufacture. Much time and cost could be saved if one is able to make a prediction of the reliability of the VLSI at the design phase. Reliability simulation offers an opportunity to uncover potential reliability hazards present in designs. The effectiveness of the reliability simulator is determined by the quality of the models employed and the time required for the simulations. It is possible to use accelerated testing or time steps to reduce the time for simulation for the wearout processes to progress provided that the acceleration factors are known and that the increased stress conditions are not going to introduce any other wearout mechanisms that are not present during normal operating conditions. The wearout processes leading to the eventual failure of bistable circuits have not been fully investigated yet and so it was necessary to develop a simulation model for the analysis of degradation effects on critical timing parameters of various forms of bistables. Unlike catastrophic failures, wearout degradations generate timing errors and an eventual failure of the bistable. Bistable elements are one of the basic building blocks of VLSI circuits and so the reliability of bistables are very important.

1.3 Outline of this Thesis

Following this introduction, a review of wearout processes in bistable circuits designed using CMOS technology is presented in chapter 2. The common terms used in reliability engineering and failure analysis have been defined. The basic distinction between the two major failure mechanisms, catastrophic and wearout faults, are discussed and the parametric faults to be investigated are identified.

In chapter three, we review the hot carrier generation and the degradation mechanisms in MOS devices. A new substrate current model has been developed which will be used to

monitor stress levels on MOS devices in a circuit. Using the substrate current model and employing characterisation techniques, a static degradation model has been proposed to monitor the effects of hot carrier stress.

Chapter four deals with the analysis and optimisation of a range of CMOS bistable circuits. The timing parameters are analysed using fault-free simulations and an optimisation procedure is used to select the most appropriate circuits for further analysis. The selected bistable circuits were redesigned using 1 micron and 0.7 micron device technologies and simulated to determine the fault-free delays.

In chapter five, hot-carrier degradation in bistable circuits is addressed. Using the static substrate current model and employing dynamic simulations, we have developed a dynamic stress model for the bistable. The modelling of the stress and the effects of hot-carrier degradation led to the evaluation of timing degradation in the selected bistable circuits. A comparative study of the hot carrier degradation effects on the selected bistable circuits is presented and the circuits having best performance identified.

Metastabe behaviour and its impact on the reliability of bistable circuits are considered in chapter six. Metastability simulations of the selected bistable circuits revealed the susceptibility to this condition and the metastable resistance as well as metastable window are defined and described. The effects of parametric variations including hot-carrier degradations on critical timing parameters leading to metastability on the bistable circuits are also addressed.

Design techniques for reducing stress and the effects of the degradation considered in chapter five and six are discussed in chapter seven. Improvements in the life-time of the bistables as a result of the design improvements are also considered. The characteristic timing parameters for the latch circuits are evaluated after the design modifications. The changes in metastability resolving time due to hot-carrier degradation was evaluated and analysed.

A qualitative analysis of the simulation results and the reliability improvements in the selected bistables has been considered in chapter eight. Improvements in reliable operating lifetime of the circuits have been analysed, compared and quantified. The overall effect of design improvements on the characteristic timing parameters have been assessed. Chapter nine deals with the conclusions and some suggestions on future direction for research work. A few design rules for reducing the hot-carrier degradations and hence how to improve the reliability of the bistable circuits have been suggested.

Chapter 2

Wearout Processes in CMOS and Reliability of VLSI Circuits

Reliability standards for VLSI are becoming more stringent with a required failure rate of one failure per 10^8 devices per hour [2.1]. The improvement in reliability can only be achieved by the interaction of the design engineer and the process engineer in order to remove process and design related problems. It has been reported in the literature [2.1]-[2.4] that the key failure mechanisms in VLSI circuits are related to hot-carrier damage, electromigration, radiation effects, electrostatic discharge and time-dependent dielectric breakdown and in many cases the failure arises because of manufacturing defects.

The observed failure rate of electronic components in VLSI circuits can be considered to be made up of intrinsic and extrinsic failure rates. According to Campbell [2.5], the intrinsic failure rate is dependant on the physical processes inherent within the device. This leads to wearout during normal operation which has long time scales and so does not contribute significantly to the failure rate during the useful life of a component. Takeda [2.1] has reported that increased VLSI reliability has been achieved by improving device and circuit structures for overcoming hot-carrier effects, dielectric breakdown and stress effects and will require close control of every process condition including gas purification and contamination of impurities in the wafer. The damaging effects of degradations no longer can be predicted by fault analysis based on the simple fault models developed by many researchers. Common fault models are the stuck-at, stuck-closed and the stuck-open fault models and the reader may refer to any of the following references [2.6]-[2.11].

Technological evolution and reliability engineering influence each other. Reliability engineering is a branch of human knowledge that has the aim of describing, predicting and improving the behaviour over time of components and systems. Failure analysis is the study of each individual anomaly with the aim of determining the dynamics of the physiochemical mechanism responsible for it and locating the cause, outside or inside the component [2.12]. The techniques of investigation applied to failure analysis have been applied to the study of new devices with the aim both of knowing the process and trying to identify eventual weak points present in the new device; and extracting information that will improve the reliability. Failure analysis carried out intensively, implemented with its methodology of observation and analysis and the development of a new branch of physics have exercised a decisive role in the evolution of the semiconductor failure technology.

In this thesis, it is postulated that all the devices in a VLSI circuit do not receive the same amount of electrical and environmental stress. For submicron devices in a VLSI circuit, the major concerns are wearout mechanisms, which lead to degradation in the circuit performance due to overstress in critical devices, and eventual failure. The effects of such over-stress and the gradual degradation of circuit delays have not been fully investigated in the case of latches and flip-flops in CMOS VLSI circuits. Bistables are critical circuits and hot-carriers are a major reliability hazard and can give rise to reduced performance of the IC. The proposed method to investigate this problem is to evaluate the extent of stress and to determine the eventual degradation of key circuit parameters on critical devices in a range of bistable circuits. Once this is established, methods to reduce the stress and hence to improve the reliability of the VLSI circuit will be identified.

2.1 Terminology

Some of the common terms used in this thesis are defined below, based on a survey of literature [2.12]-[2.16]:

Wearout: gradual degradation or deterioration of the specified characteristics of the main population of non defective devices which may lead to an eventual failure which ideally will occur a considerable time after manufacture. Doyle [2.16] defines wearout as the process of attrition that results in an increase of hazard rate with increasing age.

Hazard rate: The rate of change of the number of items that have failed at a particular time divided by the number surviving.

Degradation: deterioration in the characteristic parameter(s) of a device or circuit.

Reliability: is a characteristic of a device or circuit expressed by the probability that the item will perform its required function under specified conditions for a stated interval of time.

Reliability, $R(t) = \exp(-t / \tau)$ --- (2.1)

where τ is the life-time of the device.

Fault: unacceptable discrepancy between actual performance and its expected performance.

Failure: termination of the ability to perform a required function due to presence of a fault.

1 FIT: 1 failure per 10^9 device hour.

Failure Mechanism: is the physical, chemical or other process that result in failure.

Failure mode: the effect by which a failure is observed.

Stress: Any influence to which an item is exposed to at a certain instant.

Life-Time (τ): is the expected (reliable) operating period of the device.

Mean time between failure (MTBF): is the mean of all time periods over an infinite length of time for which the device has functioned correctly before failing.

Failure rate: the probability of failure in unit time of a component which is still working satisfactorily.

$$\text{Failure rate, } Z(t) = \frac{\text{Number failing per unit time at instant t}}{\text{Number surviving at instant t}} \quad \text{--- (2.2)}$$

For a constant failure rate, $Z(t) = \lambda$, and so the constant failure rate is the number failing per unit time.

If we assume that the reliability to be 100% at t = 0, then R(0) = 1 and R(t) = $\exp(-\lambda t)$

For a system consisting of two sub systems in series as shown, the failure rate for the system [2.20],

$$\lambda_{system} = \lambda_a + \lambda_b \qquad \text{--- (2.3)}$$

and the system reliability is,

$$R_{system} = \exp\left[-(\lambda_a + \lambda_b)\, t\right] \qquad \text{--- (2.4)}$$

For a system made up of two identical sub systems in parallel, the reliability for the sub systems are,

$$R_a = R_b = \exp(-\lambda\, t) \qquad \text{--- (2.5)}$$

and the system reliability (for a parallel system) is [2.20],

$$R_{system} = 1 - (1 - R_a)(1 - R_b) \qquad \text{--- (2.6)}$$

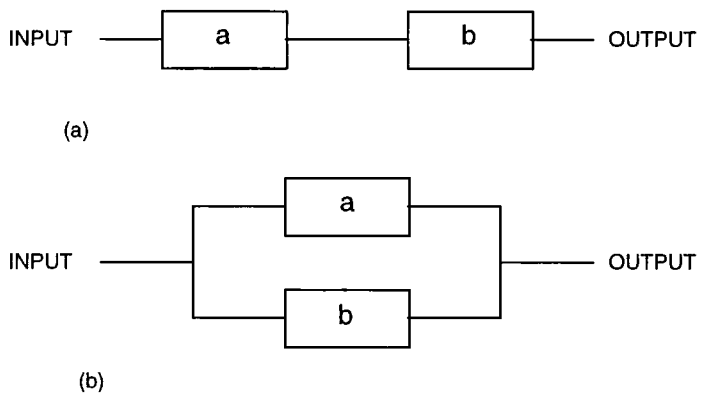


Figure 2.1 (a) Series and (b) parallel models for reliability evaluation

Substituting equation 2.5 into equation 2.6 for the identical sub systems,

$$R_{system} = 2\exp(-\lambda\, t) - \exp(-2\lambda\, t) \qquad \text{--- (2.7)}$$

A common graphical interpretation of the failure rate known as the bathtub curve [2.13], [2.16] is shown in figure 2.2. The overall life characteristic curve (thick line) is a plot of failure rate versus time and can be divided into three regions, the infant mortality region, useful life and wearout phase. This curve can be further defined by the three failure components as shown in the bottom part of the figure. Stress related failure shown as a thin horizontal line is a constant failure rate and the wearout phase only starts later in life and starts to increase with age.

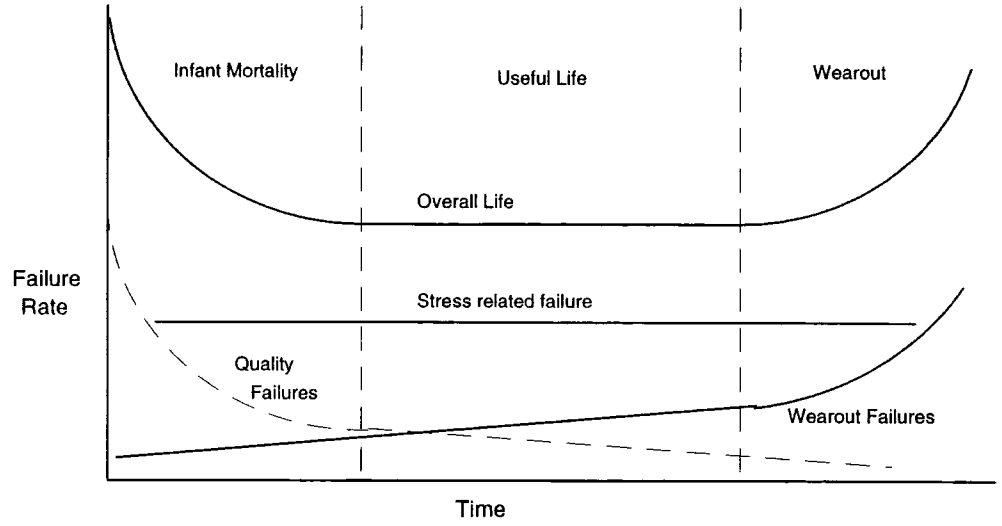


Figure 2.2 The bathtub curve

Accelerated Tests: The principle is to apply stress to a limited quantity of devices, under bias or environmental conditions above the normal ratings, to speed up the failure mechanisms that would occur in actual operating conditions and then extrapolate the behaviour observed on one lot to an entire population.

Screening: The principle of screening is to submit the entire population to low intensity stress with the aim of inducing failure only in the devices that are already weak and without damaging those that are strong.

Screening or burn-in testing has greatly reduced the failure rate in the field, since it identifies and allows elimination of early failures.

Arrhenius' Law: Temperature is one of the environmental stress that most often accelerates the degradation in semiconductor devices. A mathematical model of failure rate at raised temperature is,

$$\lambda(T) = \lambda(T_0) \exp\left[\frac{E_a}{k}\left(\frac{1}{T_0} - \frac{1}{T}\right)\right] \qquad \text{---- (2.8)}$$

where T: temperature in Kelvin, T_0: reference temperature in Kelvin, $\lambda(T)$: failure rate at temperature T, E_a: activation energy for failure mechanism in electron-volt and k: Boltzmann's constant. The activation energy is often used to characterise a failure mechanism.

2.2 A Review of Wearout Processes

As opposed to catastrophic failures, wearout processes in VLSI circuits are very difficult to predict and, therefore more difficult to model. The physical mechanism of the wearout processes can vary from one process technology to another as well as from device/design technology point of view. MOS devices designed using sub micron technology design rules are expected to wearout faster because of factors such as increased current density and raised operating temperature.

Wearout mechanisms in VLSI circuits can be classified as operational if they require the external application of a voltage to the chip and as environmental if they do not. Examples of environmental wearout are corrosion, surface ionic inversion and diffusion, while examples of operational wearout are electromigration, hot-carrier degradation and charge injection. Not all wearout processes may lead to failure of the circuit. Failure mechanisms in MOS VLSI circuits are either process-related or time-related. Some devices wearout faster when operated normally due to defects introduced during processing [2.4]. Burn-in tests can identify most of the weak devices due to this type of wearout mechanism. Takeda [2.1] has reported that wearout processes such as hot-carrier degradation, dielectric breakdown and degradation in the aluminium used as interconnect are responsible for time-dependant failures which are shown to affect the reliability of sub-micron VLSI circuits. According to another researcher [2.14], time-dependant wearout mechanisms leading to failure may give rise to abnormally high and low ohmic resistance in the interconnect layers, high resistance contact windows, excessive drain/source-substrate reverse leakage currents, large threshold voltage shifts, transconductance degradations, gate-oxide breakdowns, excessive sub-threshold leakage currents and device width and length variations.

Reviewing the literature in the field [2.3], [2.12]-[2.18] suggests the following list of wearout processes which may lead to an eventual failure:

(a) Electromigration: Electromigration is a clear example of a wearout mechanism which can lead to failure. If the current density is sufficiently high in the aluminium tracks on the semiconductor surface, the continuous impact of electrons on the Al grains cause the grains to move in the direction of electron flow [2.3]. A void is created at one end of the track while metal accumulates at the other end. Failure can occur due to an open circuit of the track at a thin region or due to short circuit with another track where the Al grains pile up.

(b) Hot-carrier degradation: The current sub micron MOS transistors used in VLSI circuits are susceptible to damage due to hot-carrier degradation. MOS transistors have two main characteristics, threshold voltage and transconductance. Any small change in one of these parameters can alter the performance of a circuit. If charge carriers are introduced into the gate dielectric then the threshold voltage will be changed and the transconductance will be degraded. Electrons may be injected into the gate oxide of an NMOS transistor when a hot electron in the channel collides with the crystal lattice generating electron-hole pairs which are attracted to the interface due to the lateral electric field. The electrons must have higher energy to surmount the silicon-silicon dioxide barrier. As device feature sizes are reduced, a corresponding reduction in thickness of the oxide dielectric layers are also made, which increases electric field strengths significantly. Hot electrons are injected from the channel into the oxide layer mainly in the avalanche plasma region near the drain [2.1]-[2.4].

(c) Oxide breakdown: Oxide breakdown is another wearout process which can lead to a gradual increase in gate to channel leakage current and an eventual short circuit from gate to channel. If an electron injected into the gate oxide has sufficient energy, it will produce electron-hole pairs by impact ionisation. The electrons created are collected by the gate and give rise to a small gate current in the case of an NMOS transistor. The holes are trapped in the gate oxide making it more positive and so encouraging more impact ionisation of hot electrons from the channel and an eventual breakdown of the oxide layer [2.1].

(d) Corrosion: Another metalisation related problem is that of aluminium corrosion due to galvanic or electrolytic action [2.1]. Galvanic corrosion may occur due to the bonding of gold wires to aluminium pads producing corrosion at the junction. The inter-metallic compounds formed between the gold and aluminium can produce bond embrittlement or voiding, leading to bond breakages and open circuits. Electrolytic decay occurs due to impurities in the overglass used to protect the IC surface from contamination. If chlorine is present with a small amount of moisture then the aluminium can be attacked, forming aluminium hydroxide and eventually producing an open circuit. This effect is increased by high electric field between conductors.

Failure mode	Definition	Effect
Internal short	Short from metal to metal or diffusion region or polysilicon	Circuit malfunction or failure
Internal open	Open circuit in the metal or wire bond or contact	Circuit malfunction or failure
Parametric shift	Variation of gain or other electrical parameter	Marginal performance or temperature sensitivity
Junction leakage	Leakage current across p-n junctions	Malfunction and increased current
Threshold shift	Shift in turn-on voltage	Increased propagation delay, random logic malfunction
Oxide damage	Charges and traps in oxide and interface	increased propagation delay
Seal integrity	Ingress of ambient air, moisture and/or contaminants	Effects ranging from degradation to complete malfunction

Table 2.1 Failure modes in semiconductor devices.

A summary of principal failure modes for semiconductor devices is given in table 2.1 [2.16].

2.3 Distinction between catastrophic and parametric faults

Catastrophic faults are those leading to a complete and sudden or obvious malfunction of the device or circuit. Examples of catastrophic failures are those due to electrostatic discharge, short circuits and open circuits due to process induced faults and many of the stresses (voltage and mechanical) induced failures, leading to complete destruction of a semiconductor junction or a metal track. Gross defects such as missing bond, large mask misalignment, wrong ion implantation dose etc. produces catastrophic failures [2.14]. The effect of catastrophic faults on a circuit can be normally detected at the outputs using a few simple tests and so these are well researched and understood even though new types of failure mechanisms may arise as device dimensions are further scaled or when new process technologies are implemented.

Parametric faults are quite different from catastrophic faults in that they may not give rise to a hard failure of the device or circuit and may take a relatively long period of time to manifest even though the mechanisms responsible for the fault already exist. Such a fault may have to be detected indirectly because the present fault detecting algorithms are unable to detect it directly since it lies dormant in a device and can only develop into a fault after a period of time in field use. A literature survey [2.14], [2.17] shows that a number of wearout mechanisms in CMOS may not cause hard failures of a device. These are:

(i) gradual increase in resistance of a metal track due to electromigration,

(ii) a change in the dielectric properties of gate oxide due to charges injected into it,

(iii) threshold voltage shift,

(iv) transconductance degradation,

(v) excessive subthreshold leakage current,

(vi) excessive drain/source-substrate reverse leakage current and

(vii) Device width and length variation due to inter diffusion or corrosion.

These are classified as wearout mechanisms leading to parametric faults. Functional level and logic level simulators do not have the models necessary to specify the above set of faults [2.14]. Faults resulting from process induced or intrinsic defect induced wearout [2.4] are easily detected using accelerated tests therefore are not classified as parametric faults. Parametric faults can be detected by the potential of a device to develop the fault when it is operated in a circuit under certain conditions such as increased stress during active life of the device. Hence tests must be devised to detect increased stress on a device in a circuit environment. Electrical, mechanical or environmental overstress can give rise to prolonged wearout leading to parametric faults. An increase in the time it takes for a specific sequence of tests to propagate through a defective circuit is a parametric fault called *delay fault* [2.8]. Hot-carrier degradation and electromigration are two examples of parametric degradation mechanisms.

2.4 Parametric faults identified for investigation

Not all parametric faults in CMOS circuits lead to catastrophic failures. There is a significant amount of literature dealing with fault analysis in CMOS for catastrophic faults. Wearout was not considered as a problem for semiconductor devices until submicron devices became the standard in VLSI and ULSI circuits in the 1990s. It was reported by Christiansen [2.15] that since semiconductor devices have no wearout mechanism, the late-life end of the *bathtub* in the life characteristic curve is missing! Doyle [2.16] also stated that wearout failures are not a factor with semiconductors whose life characteristic curves tend to be flat after the early failure period. But these suggestions are incorrect for submicron devices as these devices degrade faster and have wearout mechanisms not encountered in normal devices of larger dimensions. Takeda [3.21] stated that the influence of scaling down device dimensions on hot-carrier generation can be fatal for submicron devices. Researchers [3.7-3.10] also found evidence of wearout mechanisms for MOS logic circuits designed using submicron devices that are not normally found in 2- and 3- micron device technologies.

Hot-carrier degradations have been investigated for several decades by many researchers and have become a major constraint on submicron MOS devices as the degradation effects set in at a much faster rate. The degradations in device parameters are more or less understood. The effects of hot-carrier degradations on combinational circuits under normal static operation also have been investigated. But the research into the degradation effects due to hot-carriers on the timing and propagation through sequential circuits has not been fully investigated yet.

The parametric faults which are identified for investigation in this thesis are the **hot-carrier** induced degradation effects and the effect of the degradation on the **metastability** of the CMOS bistable circuits. Modelling of hot-carrier degradation will be discussed in the next chapter. Hot-carrier degradation simulations will be presented in chapter 5 and metastability simulations will be considered in chapter 6. Improvements in circuit designs to reduce hot-carrier degradations are considered in chapters 7 and 8.

2.5 Chapter summary

The wearout processes affecting the reliability of VLSI circuits have been reviewed. Reliability in VLSI circuits has been increasing with improved processing technology and due to the fact that there exists a greater understanding of the physical mechanisms responsible for the failures. Failure physics has been applied for the identification of mechanisms responsible for wearout processes leading to circuit failure and hence affecting the reliability of VLSI circuits. The common terms used in reliability engineering and failure analysis have been defined. For submicron devices, hot-carrier degradations were identified as a major reliability problem that needs to be addressed as a matter of priority.

Chapter 3

Modelling hot-carrier degradation effects

The wearout processes affecting the reliability of VLSI circuits have been considered in chapter 2. The dominant degradation mechanisms in submicron devices have been identified as hot-carrier degradations and the effect of degradation on metastability of CMOS bistables.

Reliability research involves the following sequence of steps:

(i) characterising the effect contributing to reliability problems,
(ii) mathematical modelling of the effects,
(iii) incorporating the model into a CAD package and
(iv) using these tools to optimise the design.

Understanding the physical principles of various degradation mechanisms and their effect on circuit behaviour is essential for successful modelling of the effects and hence improving the reliability through the optimisation procedure. Many of the degradation effects in CMOS VLSI circuits cannot be successfully modelled by the gate-level stuck-at, stuck-closed or stuck-open models. Degradation effects due to hot-carriers and metastability behaviour in CMOS circuits fall into this category.

In this chapter, we will review the present understanding of the physical mechanisms leading to hot-carrier generation and the effect of these on MOS device model parameters. We will also examine some of the existing mathematical models used for simulating hot-carrier degradation effects on MOS devices. We will present an improved model which takes into consideration additional effects which have been ignored by previous models. As the degradations in devices progress in a circuit environment, the main difficulty in quantifying the degradations was to identify a parameter which can be used as a monitor. Many researchers have suggested different

techniques for this and have defined *device lifetime* using the shift in this parameter as a guideline. We have made use of a modified model based on substrate current as a monitor to predict the lifetime of the device.

3.1 Hot-carriers: a review

Research into hot-carrier generation and degradation in CMOS devices has been carried out by many researchers. The investigation of hot electrons in solids was initiated by Landau and collaborators in the mid-nineteen-thirties [3.1]. Experimental understanding of electron transport and acceleration in vacuum tubes led to similar studies in solids under the action of electric and magnetic fields. Frohlich introduced the idea of field-dependent electron temperature and the concept of a hot-electron in 1947 [3.2]. In 1951 Shockley postulated [3.3] that the characteristic temperature (average energy) of electrons in a solid is proportional to the electric field strength based on his early work on electron conduction in germanium and silicon. According to the *Lucky electron model*, electrons acquiring a kinetic energy greater than 1.5 eV may initiate ionisation by collision with lattice atoms in the solid [3.4]. At a typical field strength of 105 V/cm the electrons will gain sufficient energy for impact-ionisation giving rise to carrier pairs and phonon emission.

3.1.1 Generation of hot-carriers and substrate current

A MOSFET is a voltage controlled device. The current through the device can be expressed as a function of the MOSFET terminal voltages and the device (geometrical) parameters using the Gradual Channel Approximation (GCA). In GCA it is assumed that the transverse electric field (gate to channel field) is much greater than the longitudinal field (along drain to source) [3.5]. The current in a MOSFET is intended to flow between the source and the drain. Currents to the substrate and the gate, and from one device to another, are prevented by potential barriers between different regions of the device. As device dimensions shrink, it becomes harder to maintain large potential barriers between adjacent regions and tunnelling currents may flow as the barrier decreases. The decreasing barriers give rise to reduced radii of curvature of depletion regions and localised regions of very high field are formed. For sub-micron devices, the GCA is not valid since the longitudinal field is now comparable to the transverse field. The two-dimensional potential results in degradation

of the sub threshold behaviour, dependence of the threshold voltage on channel length and biasing voltages and failure of current saturation due to punch-through.

As the longitudinal field is increased, the channel mobility becomes field-dependent and eventually velocity saturation of the carriers occurs. When the field is increased further, carrier multiplication near the drain occurs, leading to substrate current and parasitic bipolar action. The generation of substrate current will be discussed in more detail in the next section. The high field also causes *hot-carrier* injection into the oxide leading to oxide charging and subsequent threshold voltage shift and transconductance degradation [3.5]. Hot-carriers are electrons or holes in the channel and pinch-off regions of a short channel MOSFET which have gained sufficient energy from the high lateral electric fields in the channel to cause their energy distribution to greatly exceed that which would be expected if they were in equilibrium with the lattice [3.6]. The generation of these hot-carriers can be the cause of reliability problems and there are a number of factors which can influence the generation of hot-carriers. Many effects not encompassed in the simple theory of FETs are collectively known as *short channel effects* and these limit the scaling of FETs.

The research into hot-carrier degradation has been gaining momentum during the last fifteen years and much understanding has been gained in recent years. However there is still some controversy and debate about the nature of degradation and the physical processes involved, mainly because of the limitations in the conventional techniques used to monitor carrier injection and device degradation. We will now take a closer look at the physical processes which bring about the degradation and their effects on the device parameters. This will help us to model the hot-carrier degradations for circuit simulation studies.

3.2 Hot-carrier degradation mechanisms

The degradation mechanisms and the overall effect on the device parameters will now be discussed in detail. The reliability and the life-time of the devices are estimated using characterisation of the hot-carrier mechanisms and simulations of the degradation effects. In the case of an nMOS transistor, with a positive voltage on the gate, inversion of the p-region between the drain and the source occurs, forming an n-type conduction channel extending from drain n^+ region to source n^+ region. A potential

applied on the drain with respect to the source sets up a longitudinal field along the channel causing the electrons to be swept across from the source to the drain. The longitudinal field has a pronounced peak in the vicinity of the substrate-drain junction at the Si-SiO_2 interface [3.6-3.8]. The electrons in the channel absorb energy and can become *heated* because of the interaction between them. Some of the hot electrons with energies higher than 1.5 eV generate electron-hole pairs by impact ionisation. The electrons generated contribute to added current (I_D) and the holes travel towards the source. Some of these holes are repelled away from the interface and they are attracted by the low substrate potential [3.31]. This causes a substrate current of the order of micro amperes at a value of V_{DS} of 5 V or more. The substrate current generated can be used as a monitor for hot-carrier generation in the transistor [3.8].

If the drain voltage is higher than 5 V, some electrons can gain energy of 3 eV or more so that they can overcome the energy barrier of 3.1 eV between silicon and oxide and may be trapped or form interface states, generally damaging the dielectric properties of the oxide [3.6], [3.8]. For even higher fields, holes generated due to impact ionisation can overcome their barrier of 4.8 eV into the valence band of the SiO_2 and be injected into the oxide. Holes can cause greater damage inside the oxide than the electrons although, fortunately, there are fewer high energy holes than hot electrons so that the degradation is relatively insignificant at normal operating voltages.

In order to understand the physical mechanism of the hot-carrier degradation in MOS devices, several MOSFET parameters have been commonly used as a measure of the damage. These are $\Delta I_{DS}/I_{DS}$, $\Delta g_m/g_m$, ΔI_{DS}-V_{GS} curves, the change of sub threshold slope S, ΔV_T with V_T defined at a constant current level etc. Variations in V_T, μ, g_m etc. can be characterised using these curves. Many experimental techniques such as *charge pumping* (CP) and *floating gate* (FG) were employed by many researchers [3.6], [3.32],[3.42] to characterise the hot-carrier effects.

3.2.1 Multiplication and oxide charging

As the injection of hot-carriers into the gate oxide is the driving force of the degradation in MOSFETs, the process of generation of hot-carriers will be examined in detail. In a long-channel MOS transistor, when the drain voltage becomes sufficiently high, a weak avalanche occurs within the pinch-off region. From the avalanche plasma,

the generated electrons enter the drain and the generated holes are collected by the substrate terminal and constitute a substrate current. A schematic diagram [3.9] showing the generation of substrate current in an nMOS transistor is shown in figure 3.1. The substrate current I_{SUB} plotted as a function of the gate voltage using equation (3.1) for a long-channel transistor is shown in figure 3.2. The drain current for the device is also shown and it covers the region from sub-threshold to linear and then to saturation. The substrate current increases first with V_{GS}, reaches a maximum, then decreases.

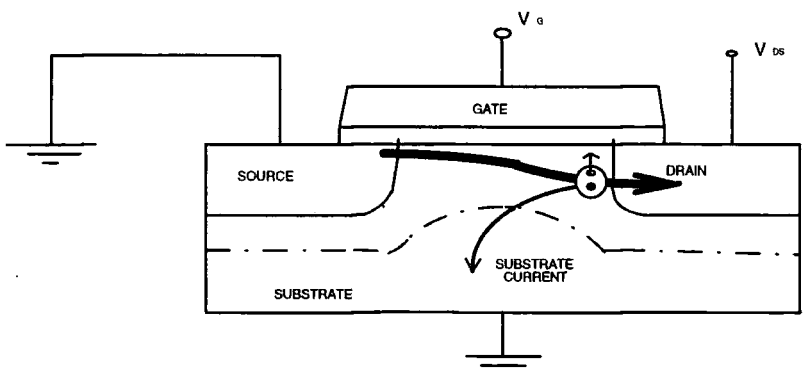


Figure 3.1 Cross section of an nMOS transistor showing substrate current generation

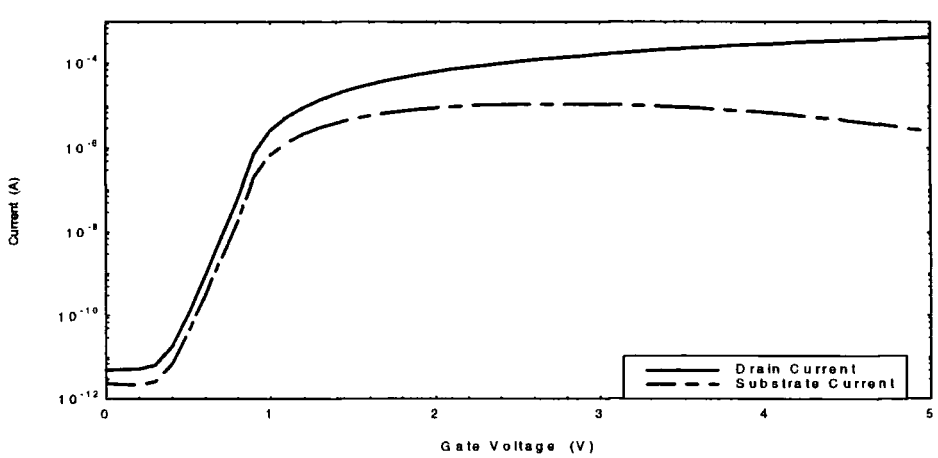


Figure 3.2 Drain current and substrate current versus gate voltage for an nMOS transistor (W=1 μm, L=0.8 μm, V_{DS} = 5 V, Process: EC/3 (see appendix D))

The maximum in I_{SUB} characteristic can be explained as follows. Assuming that the impact ionisation occurs uniformly in the pinch-off region, the substrate current can be written as, [3.5]

$$I_{SUB} = I_D \cdot \gamma \cdot \Delta L \qquad \text{--- (3.1)}$$

where γ is the ionisation coefficient, the number of electron-hole pairs generated per unit distance; and ΔL is the length of the pinch-off region. For a given V_{DS}, as V_{GS} increases, both I_D and $V_{DS.SAT}$ increase. When $V_{DS.SAT}$ increases, the lateral field $(V_{DS} - V_{DS.SAT})/L$ decreases, causing a reduction of γ. Thus we have two conflicting factors. The initial increase of I_{SUB} is caused by the increase of drain current with V_{GS}, and at larger V_{GS} the decrease of I_{SUB} is due to the decrease of γ. Maximum I_{SUB} occurs where the two factors balance.

For short-channel devices, the additional effect is caused by the avalanche-generated hole current. As the source-drain separation is reduced, some hole current can flow to the source. If the drain voltage is low, most of the hole current flows out at the substrate terminal; the substrate current behaves similarly to that shown in fig. 3.2. However when the drain voltage is large, a substantial hole current can flow to the source and the product of the current and substrate resistance can become large enough (> 0.6V) to forward-bias the source-substrate junction, causing electron injection into the substrate. This injection leads to a parasitic n-p-n (source-substrate-drain) bipolar transistor action [3.5]

As the field along the channel becomes high, it is possible for some hot-carriers in the inversion layer to gain sufficient energy to surmount the $Si\text{-}SiO_2$ energy barrier (3.1 eV) and be injected into the gate oxide. Hot electrons can therefore be injected from the avalanche plasma formed near the drain region. Thermally generated carriers can also be injected into the oxide due to a large transverse field in the bulk semiconductor. The effects of the injected hot electrons on the I_{DS} - V_{DS} characteristics are shown in figure 3.3. Note the reduction in drain current after stress. The transconductance becomes smaller because of reduced channel mobility [3.5] and the sub threshold current becomes larger because of the increased interface trap density. An increase in threshold voltage also can be observed on a I_D - V_{GS} curves for the device.

Long-term operation of the device is seriously affected by oxide charging,

because the charging continues to increase with time during device operation. As a result of this cumulative degradation, oxide charging limits the maximum voltage levels that can be applied for a device to have a specified lifetime [3.10], [3.11]. As the channel length is reduced, different mechanisms limit the maximum drain voltage.

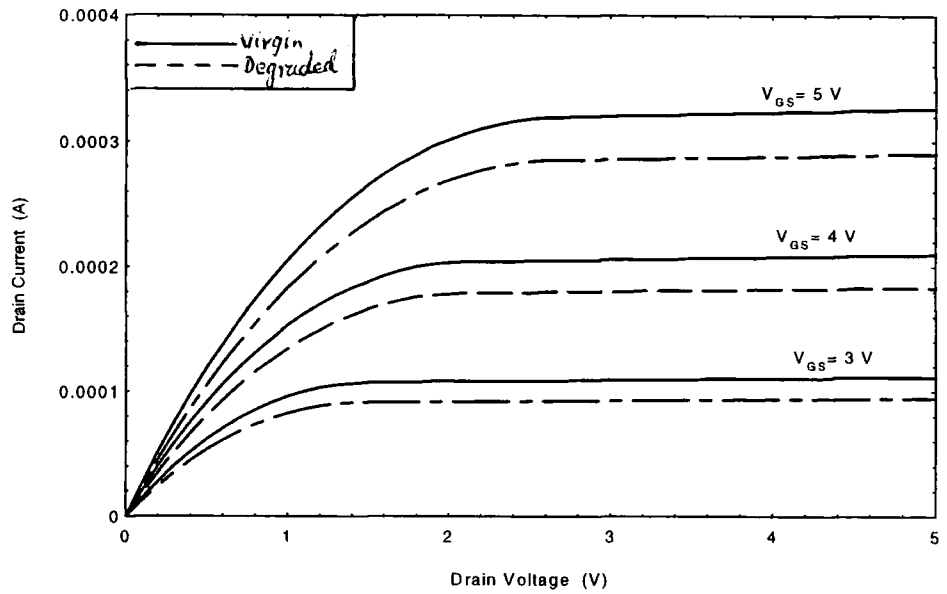


Figure 3.3 Degradation in drain current due to hot-carrier stress (Device: N 4/3 (see appendix: E) Process: EM/3)

3.2.2 Carrier temperature and mobility degradation

At low electric fields the drift velocity in a semiconductor is proportional to the electric field and the proportionality constant is called the mobility μ, which is independent of the electric field. When the fields are sufficiently large, non-linearities in mobility and saturation of drift velocity are observed. At still larger fields, impact ionisation occurs.

As the electric field increases, the average energy of the carriers also increases and they acquire more energy than they have at thermal equilibrium. The effective temperature T_e at high field is higher than the lattice temperature T and is given by [3.5],

$$\frac{T_e}{T} = \frac{1}{2}\left\{1+\left[1+\frac{3}{8}\pi\left(\frac{\mu_0\varepsilon}{C_s}\right)^{1/2}\right]\right\} \qquad \text{--- (3.2)}$$

and the drift velocity is given by,

$$v_d = \mu_0\,\varepsilon\sqrt{T/T_e} \qquad \text{--- (3.3)}$$

where μ_o is the low field mobility, ε is the electric field and C_s is the velocity of sound in the semiconductor. When $\mu_o\varepsilon$ is comparable to C_s (low fields),

$$T_e \approx T\left[1+\frac{3\pi}{32}\left(\frac{\mu_0\varepsilon}{C_s}\right)^2\right] \qquad \text{--- (3.4)}$$

and $$v_d \approx \mu_0\varepsilon\left[1+\frac{3\pi}{64}\left(\frac{\mu_0\varepsilon}{C_s}\right)^2\right] \qquad \text{--- (3.5)}$$

When the field increases to $\mu_0\varepsilon \approx \frac{8}{3}C_s$, the carrier temperature T_e is double that for low field and the mobility drops by 30% [3.5]. Finally at sufficiently high fields, the drift velocity approaches a saturation velocity,

$$v_s = \sqrt{\frac{8E_p}{3\pi m_0}} \sim 107 \text{ cm/s} \qquad \text{--- (3.6)}$$

where Ep is the optical-phonon energy. At very high fields, the carriers gain enough energy so that they can excite electron-hole pairs by impact ionisation. The electron-hole pair generation rate G is [3.5],

$$G = \gamma_n.n.v_n + \gamma_p.p.v_p \qquad \text{--- (3.7)}$$

where γ_n and γ_p are electron and hole ionisation coefficients respectively.
The ionisation rate is given by,

$$\gamma(\varepsilon) = \frac{q\varepsilon}{E_I}\exp\left[-\frac{\varepsilon_I}{\left[\left(1+\frac{\varepsilon}{\varepsilon_p}\right)+\varepsilon_{kt}\right]}\right] \qquad \text{--- (3.8)}$$

where E_I is high field effective ionisation energy, ε_{kt}, ε_p & ε_I are threshold fields for carriers to overcome the deceleration effects of thermal, optical phonon and ionisation scattering respectively. For Si the value of E_I is 3.6 eV for electrons and 5.0 eV for holes. The impact ionisation is temperature dependent.

3.2.3 Gate current generation

A small gate current is generated due to channel hot-carriers, either channel electrons or avalanch generated holes, that possess sufficient energy to surmount the Si-

SiO_2 barrier [3.12]. The barriers for electrons and holes emitted to the gate are 3.1 eV and 4.1 eV, respectively. The two common models for gate current are the *lucky-electron model* [3.4] and the *electron-temperature model* [3.5]. In the lucky-electron model, the probability of an electron suffering a collision would determine the energy distribution of carriers generated. The *lucky-electrons* simply escape energy loss events and gains energy from the applied fields; while the electron-temperature model applies the theory of thermionic emission of *hot* electrons into the oxide from the channel if the electron temperature T_e is not in equilibrium with the lattice. For the present technology devices, the gate current generated is insignificant and may not produce excessive leakage current. The gate current generation will not be considered in detail in this thesis and the reader is requested to refer any one of the many authors [3.6], [3.12] on this topic.

The discussions in the last sections have shown that the main hot-carrier damage mechanisms are interface state generation and the trapping of charges in the oxide and the interface. The mobility degradation due to carrier multiplication also has been discussed. In order to understand the physical mechanism of the hot-carrier degradation in MOS devices, several MOSFET parameters are commonly used as a measure of the damage. These are $\Delta I_{DS}/I_{DS}$, $\Delta g_m/g_m$, ΔI_{DS}-V_{GS} curves, the change of subthreshold slope S, and ΔV_T. These identified damage mechanisms will be modelled as device parameter degradations for SPICE circuit simulations as discussed in the next section. The degradation process is monitored using the substrate current and the modelling of substrate current is discussed next.

3.3 Substrate current modelling

The channel hot electrons (Lucky electron model) [3.13] are not responsible for degradation or the generation of substrate current in MOS devices. For submicron devices the increased peak in the lateral electric field close to the drain junction accelerates the electrons to such an extent that it generates photons by Bremsstragging. The photons have been observed near the drain junction by many researchers [3.14], [3.15]. The photons scatter in all directions and collide with lattice atoms near the drain junction close to the interface between the silicon channel and the gate oxide and generate electron/hole pairs. The high energy electrons generated during this process partly are collected by the drain and the rest are injected into the

interface and into the gate oxide. A few electrons may be accelerated by the gate field and get collected as gate current. Except for a few recombinations, almost all the holes are collected by the substrate if the substrate is biased negative with respect to the drain junction, which is normally the case.

It has been reported [3.16] that the degradation rate of nMOS transistors during dynamic operation is larger than the degradation rate during static operation. The enhanced degradation has been attributed to the alternating hot-electron and hot-hole injections into the gate oxide during dynamic stress and the generation of interface states [3.17]. Gate current generated can be used as a monitor of the degradation in MOS devices. As the gate current is of the order of a few pica amperes and substrate currents are in the range of micro amperes, substrate currents are generally used for monitoring degradation. During static operation of a MOS transistor, substrate current has three components:

(i) reverse saturation leakage current from drain to substrate (reverse biased junction)
(ii) leakage current from channel area and perimeters to substrate
(iii) impact ionisation current generated at the high lateral field near the drain junction.

For submicron devices the first two components are insignificant compared to impact ionisation current and so the substrate current can be used as a reasonably accurate monitor for stress generated degradation. During dynamic operation, the substrate current has an additional component: charging and discharging currents of the reverse biased substrate to channel (and drain) capacitors. During fast rising and falling edges of voltage wave forms, this component could be significantly large. Only the substrate current due to impact ionisation is required here and so the capacitor currents can actually offset this current.

The fraction of the drain current I_{ds} that contributes to the impact ionisation current is a function of:

(a) (V_{ds} - $V_{pinch\text{-}off}$) : impact ionisation current increases with increasing (V_{ds} - $V_{pinch\text{-}off}$) as this increases the accelerating field near the drain.
(b) V_{gs} : the impact ionisation current decreases with increasing V_{ds} the peak

occurring when $V_{gs} \approx \frac{1}{2}V_{ds}$.

(c) L : impact ionisation current increases with decreasing L while keeping supply voltage constant.

Fortunately the magnitude of the impact ionisation current peak is large at maximum stress conditions compared to substrate capacitor currents for submicron devices and so the peak value of the substrate current can also be used as a monitor for maximum stress during dynamic operation.

3.3.1 Existing substrate current models

Even though substrate current has been recognised as the ideal monitor for hot-carrier degradation in MOS devices, SPICE models do not generally include substrate current equations. A commercial version of SPICE produced by *Meta-Soft* [3.43] and called HSPICE does have impact ionisation model equations incorporated into device models. Many researchers [3.13], [3.15], [3.18-3.23] have recognised the importance of monitoring of substrate current for hot-carrier degradation and have incorporated their models into the simulation process. Most of these use the substrate current model as a post processor, making use of the SPICE simulation results as input data to the processor. The Philips MOS Model:9 [3.44] has the substrate current models incorporated where it is referred to as a *weak-avalanche current*. Some existing substrate current models are discussed below and a new optimised model created by the author for use as a post processor in SPICE simulations is also presented.

3.3.1.1 Sakurai model for substrate current

The substrate current model suggested by Sakurai [3.23] is a combination of two different models modified to include substrate bias effects. This model uses an empirical expression for 0.8- μm poly-gate-length conventional devices with oxide thickness of 16 nm and is given as:

$$I_{sub} = I_{ds} a (V_{ds} - V_{dsat})^{b} \qquad \text{--- (3.9)}$$

where $a = 2.24 \text{ x } 10^{-5} - 0.10 \text{ x } 10^{-5} V_{ds}$

and $b = 6.4$

$$V_{dsat} = \frac{(V_{gsth} L_{eff} E_{sat})}{(V_{gsth} + L_{eff} E_{sat})} \qquad \text{--- (3.10)}$$

$$V_{gsth} = V_{gs} - V_{th} - 0.13V_{bs} - 0.25V_{gs} \quad \text{--- (3.11)}$$

$$E_{sat} = 1.10 \text{ x } 10^7 + 0.25 \text{ x } 10^7 V_{gs} \quad \text{--- (3.12)}$$

where I_{sub} is the substrate current, I_{ds} the drain-source current, V_{ds} drain-source voltage, V_{gs} gate-source voltage, V_{bs} bulk-source voltage, V_{dsat} drain saturation voltage, L_{eff} effective channel length in meters and E_{sat} velocity saturation field in volt per meter. The drain current was modelled using SPICE level 3 and the empirical parameters given above were the best fit parameters. The model was implemented as a SPICE post processor. The substrate current plotted using this model is given in figure 3.4.

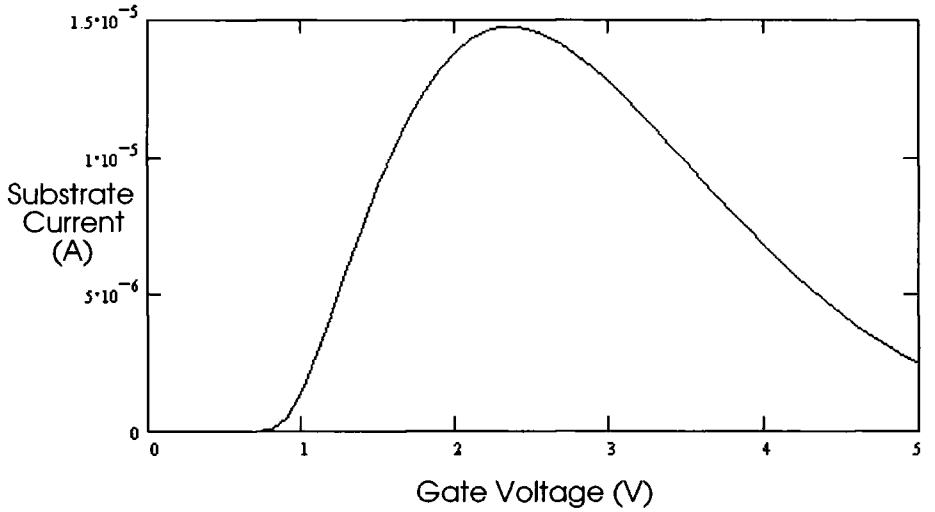


Figure 3.4 Substrate current plotted using Sakurai model
(Device: N 1/0.8, Process: EC/3)

3.3.1.2 Hu model for substrate current

This model [3.15] is also a modification of previous models by the inclusion of an exponential term for modelling the exponential dependence of the impact ionisation coefficient on 1/E as suggested by S.Sze [3.5]. It is a very simple model and is given by:

$$I_{sub} = C I_{ds} \exp\left(-\frac{\beta}{E_m}\right) \quad \text{--- (3.13)}$$

where I_{ds} is the drain current, β is the impact ionisation coefficient, E_m the maximum channel electric field which occurs at the drain end and C is an empirical fitting

parameter. These values are dependent on the processing technology and the device dimensions used and are given as: C ≈ 2, β = 1.7 x 10^6 , $E_m = \frac{V_{ds} - V_{dsat}}{l_c}$ where l_C is the effective channel depth and is given by:

$$l_c = \sqrt{3T_{ox}\, X_j} \qquad \text{--- (3.14)}$$

which was approximated as,

$$l_c = 0.2\,(T_{ox})^{1/3}\,(X_j)^{1/2} \qquad \text{--- (3.15)}$$

where X_j is the junction depth. For submicron devices, the saturation voltage decreases with decreasing L and is given by:

$$V_{dsat} = \frac{(V_{gs} - V_T) LE_{sat}}{(V_{gs} - V_T) + LE_{sat}} \qquad \text{--- (3.16)}$$

where E_{sat} is the critical field for velocity saturation and is about 5x10^4 V/cm.

3.3.1.3 HSPICE substrate current model

Meta-Soft has released a recent version of HSPICE (version H92) [3.43] which has an impact ionisation model included. The impact ionisation current is available for all model levels and the controlling parameters are ALPHA, VCR and IIRAT. The parameter IIRAT sets the fraction of the impact ionisation current that goes to the source.

$$I_{ds} = I_{ds}(\text{normal}) + \text{IIRAT} \times I_{impact} \qquad \text{--- (3.17)}$$

$$I_{db} = I_{db}(\text{diode}) + (1 - \text{IIRAT}) \times I_{impact} \qquad \text{--- (3.18)}$$

IIRAT defaults to zero, which sends all impact ionisation current to bulk and is consistent with all versions. The length and width sensitivity parameters LALPHA, WALPHA, LVCR and WVCR can be ignored for simplified models. The impact ionisation current is calculated as follows:

$$I_{impact} = I_{ds} ALPHA_{eff} (V_{ds} - V_{dsat}) \exp\left(-\frac{\text{VCR}_{\text{eff}}}{V_{ds} - V_{dsat}}\right) \qquad \text{--- (3.19)}$$

where $ALPHA_{eff}$ is the effective impact ionisation coefficient and VCR_{eff} is the critical voltage.

3.3.1.4 BSIM substrate current model

A parametric substrate current model is implemented into the Berkeley Short-Channel IGFET Model (BSIM). The substrate current model used in BSIM is based on work done by El Mansy and Ko [3.18]. El Mansy derived an exponential relationship of the channel electric field in the saturation region using quasi-dimensional concepts and later Ko improved the model by including the effects of junction depth and channel doping.

The impact ionisation coefficient $\alpha_i = A_i \exp\left(-\frac{B_i}{E_s}\right)$ is integrated over the limits of the velocity saturation region to obtain the equation for substrate current as,

$$I_{sub} = I_{ds} A_i \int \exp\left(-\frac{B_i}{E_s}\right) dy \qquad \text{--- (3.20)}$$

where E_s is the electric field in the channel and is given by:

$$E_s(y) = E_{crit} \cosh\left(\frac{y}{l_c}\right) \qquad \text{--- (3.21)}$$

E_{crit} is the critical field for velocity saturation and l_c is the effective conduction depth of mobile carriers. The electric field has a maximum peak at the drain end of the channel and by using approximations, the critical electric field at the drain end is given by,

$$E_d \approx \frac{(V_{ds} - V_{dsat})}{l_c} \qquad \text{--- (3.22)}$$

After integrating over the limits and substituting the critical drain field equation, the final expression for substrate current is given by,

$$I_{sub} = \frac{A_i}{B_i} I_{ds} (V_{ds} - V_{dsat}) \exp - \frac{B_i l_c}{(V_{ds} - V_{dsat})} \qquad \text{--- (3.23)}$$

The commonly used values for A_i and B_i are: $A_i = 2 \times 10^6$ cm^{-1} , $B_i = 1.7 \times 10^6$ V/cm. The value of l_c must be determined empirically. For short-channel devices, V_{dsat} departs from the well-known relationship $V_{dsat} = V_{gs} - V_{th}$ for long-channel devices because electrons in the channel region become velocity-saturated before V_{ds} reaches $V_{gs} - V_{th}$. The model used in BSIM to account for this behaviour was derived by Sodini and Ko [3.25] as,

$$V_{dsat} = \frac{E_{crit} L (V_{gs} - V_{th})}{E_{crit} L + (V_{gs} - V_{th})} \qquad \text{--- (3.24)}$$

where L is the channel length and E_{crit} is extracted as a parameter from measured V_{dsat} values. Parameter extraction tools are used to extract the empirical parameters not defined in the model.

3.3.1.5 Philips substrate current model

Philips (Philips Electronics, Netherlands) MOS Model:9 was released in January 1994 and it includes substrate current equations embedded into the model [3.26]. This has the advantage that there is no need to have a post processor to establish the substrate currents in each device and hence any reliability problems associated with substrate current generation could be addressed at the circuit simulation stage itself. The substrate current model is referred to as *weak avalanche model* and it can be applied to short-channel devices of channel length 1.2 μm and smaller. At large V_{ds} values, the effect of avalanche generated substrate current is shown to be quite high. The avalanche current is given by:

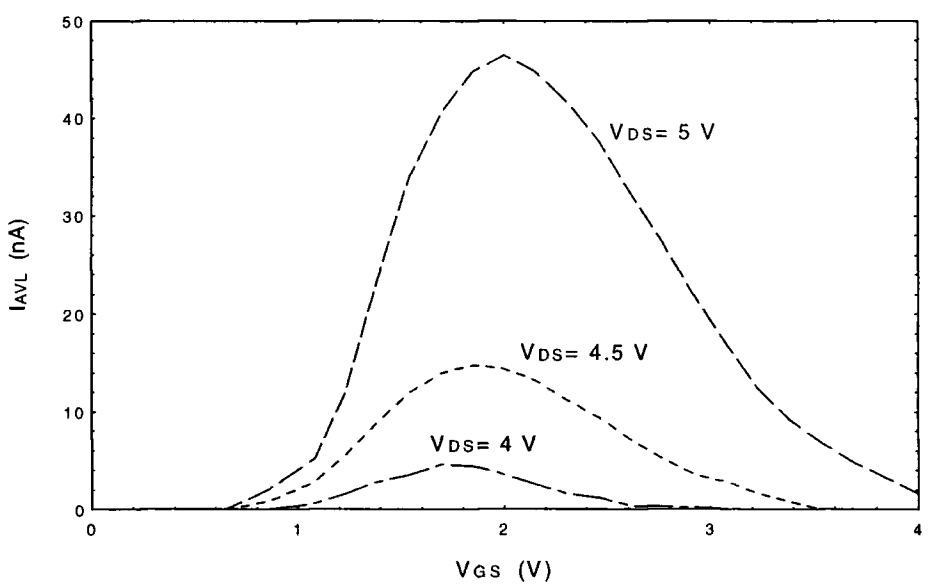


Figure 3.5 Substrate currents plotted using Philips model (Device: N 1/0.8, Process: EC/3)

$$I_{avl} = \begin{cases} 0 & \text{for } V_{DS} \leq V_{Dsat} \\ I_D \,.a_1 \exp - \dfrac{a_2}{(V_{DS} - V_{Dsat}.a_3)} & \text{for } V_{DS} > V_{Dsat} \end{cases} \quad \text{--- (3.25)}$$

where a_1 is the factor of the weak-avalanche current, a_2 the exponent of the weak-avalanche current and a_3 the factor of the drain-source voltage above which weak-avalanche occurs. The empirical model parameter values for MOS Model 9 is given as,

$a_1 = 15.888$

$a_2 = 31.900$

$a_3 = 0.760$

The substrate current plotted using this model is given in figure 3.5.

3.3.2 Optimised substrate current model

The substrate current models presented above have been modified over the years in order to include additional effects introduced by submicron devices and improvements in the processing technology. Most of the models were designed around a process or technology and so it was an extremely difficult procedure to select one model suitable for the 0.7 micron *process: EC/3* which has been used for this research work.The extracted empirical parameters used in these models were not in a suitable form for incorporation into the model for simulation. The impact ionisation model parameters were not available for the SPICE and HSPICE models currently used for the designs. Hence it was not possible to incorporate the substrate current model directly into the SPICE or HSPICE simulations. As a starting point, it was decided to select a simple model from the above list and to implement it as a post processor, making use of the output of the HSPICE simulations of the circuits as input. It was necessary to adjust some of the empirical parameters specified in the model such that it will give a reasonably accurate substrate current value in spite of differences in technology.

It is generally accepted that for CMOS devices, pMOS transistors forming the load are much more rugged than nMOS transistors and so produce much less substrate current. It has been reported [3.27-3.29] that pMOS transistors are much less susceptible to hot-carrier effects due to the lower impact ionisation rate for holes. Another researcher [3.30] has shown that in a CMOS circuit environment, the degradation of pMOSFETs contributed approximately 5 percent to the speed

degradation due to hot-carrier stress. The pMOSFET lifetime factor was found to be much larger than that for nMOSFET. Hence we have assumed that the stress and the subsequent substrate current generated in pMOS load transistors is negligible and may be ignored. This is true for the transistors fabricated using present technology conforming to 0.7 micron design rules. Hence the simulation and optimisation procedure was undertaken for nMOS transistors in the latch circuit.

3.3.2.1 The Optimisation Procedure

Since the Sakurai Model [3.24] has all the empirical parameters specified and was modelled around a 0.8 micron poly-gate-length conventional device technology, we decided to use this model as a starting point. The first step was to generate an output file by HSPICE Level:6 simulations for one of the latch circuits. The output parameters needed were drain current, drain voltage gate-source voltage and threshold voltage. The MATHCAD package running on a PC was used as the post processor to evaluate and graph the substrate current.

The output of the post processor was used to generate a plot of substrate current vs time. The plot obtained was analysed using I_D vs Time as well as V_{DS} & V_{GS} plots for the same latch circuit. It was observed that substrate current had a peak at the instant when the gate voltage is nearly half the drain voltage as theoretically predicted, under static operation. In order to obtain a conclusive agreement that the magnitude of the peak substrate current plotted is correct, an additional simulation of the circuit was carried out using HSPICE and the substrate current and drain current were plotted. The substrate current plotted using HSPICE has two components, I_{impact} and I_{cap}. At the peak of the substrate current, I_{impact} is sufficiently large and so I_{cap} has very little effect and so can be ignored. The peak values of the two plots were in agreement. Published results also gave a substrate current value of about 10% of the drain current at the most severe stress conditions in the case of an nMOS device of comparable dimensions [3.41].

The Hu model was now implemented using the post processor and a plot of I_{sub} vs Time was generated. The comparison with Sakurai model was not acceptably accurate and the magnitude of the peak substrate current was inaccurate. The failure of the model could be attributed to the dependence of the model on the empirical parameters.

The HSPICE impact ionisation model was implemented and plots showed reasonable agreement with the Sakurai model even though the peak current was under estimated by about 20%. The following options were used in the model: IIRAT = 0, ALPHA = 1 and VCR = 15. The Philips model was implemented and plotted using MATHCAD and the plot indicated that the currents were under estimated by more than 200%. The parameter a_2 had to be adjusted so that this anomaly was rectified. The BSIM model also was implemented using the following parameter options as described in the previous section. The value of saturation current from HSPICE output was used and the value of l_c was evaluated using the formula,

$$l_c = 0.2\,(T_{ox})^{1/3}\,(X_j)^{1/2} \qquad \text{--- (3.26)}$$

which is an approximated value of equation (3.15) as suggested in section 3.3.1.2. T_{ox} and X_j values from the HSPICE Level 6 model which was used for the circuit simulations were made use of for the evaluation. By specifying the units for all the empirical parameters correctly, the substrate current plotted was found have the correct range. The magnitude of the substrate current was adjusted slightly by modifying the model parameters and the evaluated value of l_c was 5.76×10^{-7} m. A block diagram representing the optimisation steps is given in figure 3.6.

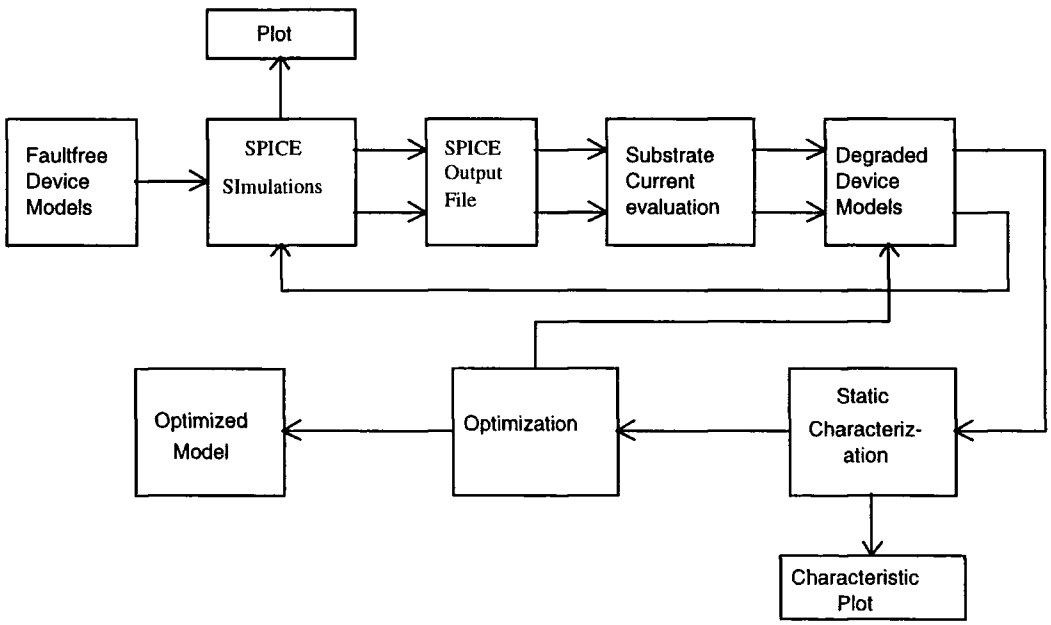


Figure 3.6 Optimisation steps: Substrate current model

3.3.2.2 Optimised final model

All the models described in the previous section have been found to be dependent on the device dimensions and the process and so the empirical parameters had to be re-evaluated. The need was for a substrate current model accurate enough for submicron devices and less dependent on the process. Since the Hu model was developed around short channel MOS devices (BSIM1) [3.32], it was decided to use this model with the necessary modifications to account for the effect of the variation of substrate current with V_{Dsat} variation for submicron devices. The effect of gate bias on substrate current is modelled by using a bias term (V_{DS} - V_{Dsat}) multiplying I_d as well as the exponential terms. The model also must contain a term which accounts for the effect of change in the conduction depth of mobile charge carriers under the action of the lateral and gate fields. This was achieved by using the l_c term (derived from T_{ox} and X_j) within the exponential. The optimisation steps described before and shown in figure 3.6 has been employed which resulted in a robust model for submicron nMOS devices. All the empirical parameters have been evaluated by a sequence of SPICE simulations, substrate current evaluation, generation of degraded SPICE models, static characterisation and comparison using published experimental values of substrate currents for devices having similar dimensions.

The final model is given by:

$$I_{sub} = C_i \, I_{ds}(V_{ds} - V_{dsat}) \, \exp\left(-\frac{\beta l_c}{(V_{ds} - V_{dsat})}\right) \qquad \text{--- (3.27)}$$

where $C_i = 0.9875$, $\beta_i = 6.07 \times 10^7$, and $l_c = 0.2 \, (T_{ox})^{1/3} \, (X_j)^{1/2}$. The values for T_{ox} and X_j for the technology are 15 nm and 0.25 μm respectively. This model has the following features compared to the other models:

1. does not depend on extracted parameters based on process technology; this has been verified by circuit simulations using a number of process technologies.
2. dependence on device dimensions and channel doping is built into the model (T_{ox} and X_j) and can be easily obtained from SPICE or HSPICE model parameters
3. the variation of substrate current with gate bias is incorporated into the model
4. the exponential dependence of electric field on impact ionisation is included

5. any small discrepancy between simulation and experimental values can be adjusted by just one parameter C_i.
6. channel length and channel width dependencies of substrate current are built into the model by using the output values for I_d, V_{ds} and V_{dsat} from SPICE simulations as input to the post processor.

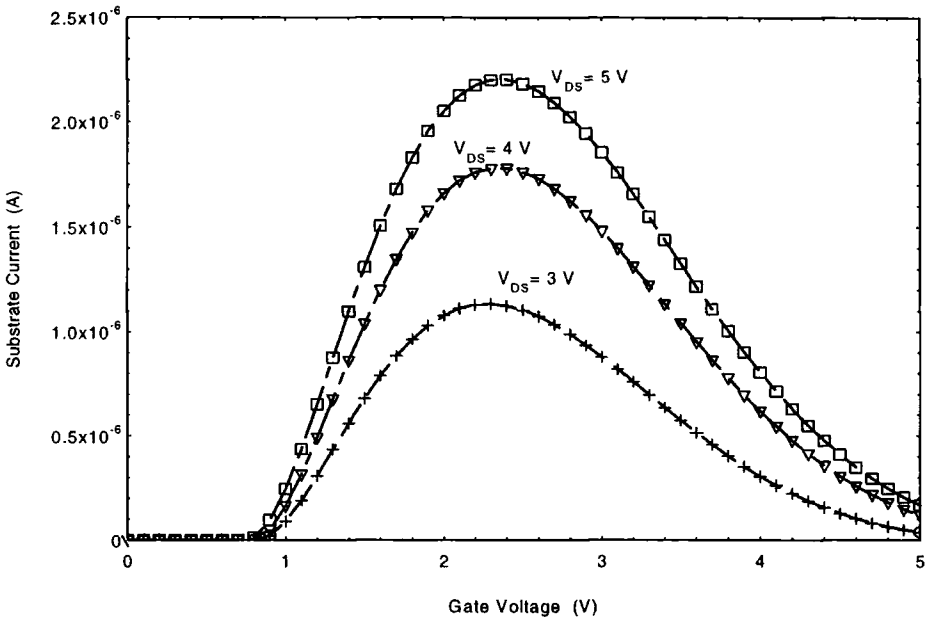


Figure 3.7 Substrate current plotted using the optimised model (Device: N 1/0.8, Process: EC/3)

The model was used to plot substrate current for the 0.7 micron nMOS transistor and is given in figure 3.7.

3.4 Degradation modelling

When a transistor in a circuit is subject to electrical stress, its output characteristics degrade with time. The degradation is due to the shift in the transistor parameters. It is possible to predict device degradation and lifetime from the substrate current because all hot-carrier effects are driven by the channel electric field which has a maximum at the drain end giving rise to maximum degradation at the drain end. It has been proved convincingly by Hu [3.15] that the generation of interface traps is the dominant cause of MOSFET degradation. The parameters commonly used to quantify

the amount of device degradation that has occurred are the drain current degradation $\Delta I_D/I_{D0}$, transconductance degradation $\Delta g_m/g_{m0}$ and threshold voltage shift ΔV_{Th} [3.32]. Drain current and transconductance are normally measured at V_{GS} = 5 V and V_{DS} = 50 mV or 100 mV, while V_{Th} is usually measured at a pre-determined drain current level at the same drain biases. Changes in all three parameters are related to the substrate current that is generated by the device. By measuring the substrate current generated by a device in a circuit, the degradation of the device parameters can be calculated and the lifetime predicted.

The modelling of the substrate current has already been discussed in the last section of this chapter; the modelling of hot-carrier induced stress and the simulation of the degradation of device parameters under static conditions are now discussed. The degradation models extracted from this analysis will be used to predict reliability of the device and to investigate the device lifetime under stress conditions.

3.4.1 Parametric degradation

The shift of a general parameter P_i during an interval of time 0 to T can be expressed as [3.33],

$$\Delta P_i = \int_0^T D_i[S(t)]dt \qquad \text{--- (3.28)}$$

where D_i is the degradation function associated with parameter P_i and S(t) is the stress function. The stress function is evaluated at each instant of time and the parameter change due to the stress at that instant is represented by the degradation function. When considering measurements at discrete time intervals, the integration can be replaced by a numerical summation as given below,

$$\Delta P_i = \sum_{i=1}^{n} D_i (S_j) \Delta t_j \qquad \text{---(3.29)}$$

where t_0= 0, Δt_j= t_{j-1} and t_n= T. For hot-carrier effects, S(t) is usually taken as the normalised substrate current (I_{sub}/W). Using substrate current as a parameter, the degradation model is,

$$\Delta P_i = A_i \left[\frac{I_{SUB}}{W}\right]^m t^n \qquad \text{--- (3.30)}$$

where A_i, m and n are empirical degradation parameters dependent on the process technology. With the aid of the substrate current model and using degradation simulations, it is possible to predict the reliability of a device in a circuit. Two

approaches are generally used: (i) the one-cycle simulation scheme and (ii) the repetitive simulation scheme. Both schemes of simulations will be employed in our model.

In the one-cycle simulation scheme, the stress information for a relatively short period is available based on one conventional circuit simulation run. This information is used for quick identification of weak devices. The long term IC reliability is predicted using a large extrapolation factor. In this model, the wave form of the stress is assumed to be unchanged throughout the life time of the circuit. Prediction of device lifetime is made by calculating the time taken to reach a user-specified maximum tolerable device parameter change. The impact of transistor degradation on circuit performance is then determined based on a single update of the parameter set affected by the stress.

The repetitive simulation scheme [3.16], [3.33], where multiple simulation cycles are utilised is more reliable than one-cycle method. This method can closely mimic real circuit operation in which bias conditions of a circuit are changing as wearout proceeds in the devices. The device parameter values are updated according to accumulative device degradation at the end of each time interval. Long term circuit performance can be predicted reliably using this simulation scheme.

Simulation results from either scheme can be used to analyse the circuit-level dynamics of the degradation mechanism and can also be used as a design aid for improving the long-term reliability through design modifications. It has been reported [3.16] that degradation rate of nMOS transistors during dynamic operation is larger than that during DC operation. Kuo [3.34] also reported that under AC or pulsed stress, enhanced degradation is observed when fast V_{GS} transients occur in the presence of high V_{DS}. Even though Mistry & Doyle [3.35] dispute the reasons for enhanced degradation under fast transients, they also found enhanced degradation under AC stress and attribute this to all the three different degradation mechanisms (discussed before) present during an AC cycle. The existing degradation models are discussed in the next section and our degradation model will be introduced.

3.4.2 Existing degradation models

A number of Degradation models have been proposed by various researchers. Almost all of them make use of substrate current as a parameter for monitoring the stress on a device as well as the progress of degradation with time. A few of the existing models are discussed briefly.

3.4.2.1 BERT degradation model

The *BErkley Reliability Tools* (BERT) incorporate the hot-carrier degradation model, the Circuit Ageing Simulator (CAS), the Circuit Oxide Reliability Simulator (CORS), Electromigration (EM) and the Bipolar Circuit Ageing Simulator (BiCAS) [3.32], [3.36-3.38]. We will only discuss the hot-carrier degradation model incorporated in the reliability tool. In this degradation model, device degradation is typically measured by the amount of threshold voltage shift (ΔV_T) that occurs during a simulation period. Other parameters such as $\Delta I_{DS}/I_{DS0}$ may be used to characterise device degradation. In that case, ΔV_T in the equation should be replaced by the corresponding variable. Under DC static stress conditions, the amount of degradation as a function of time is given by,

$$\Delta D = A.t^n \qquad \text{--- (3.31)}$$

and

$$\Delta D_f = A.\tau^n \qquad \text{--- (3.32)}$$

The device lifetime τ is defined as the time for the degradation of the device parameter to progress to a pre-determined value D_f and is,

$$\tau = W\,B\,(I_{SUB})^{-m}\,(I_{ds})^{m-1} \qquad \text{--- (3.33)}$$

where the constants, $m = \phi_{it}/\phi_i$, and $B = H\,(\Delta D_f)^{1/n}$. The values of n, m and H are determined from stress experiments and H is dependent on device processing technology. ΔD_f is the amount of shift in the parameter value defined at device failure, t is the stressing time and ϕ_i and ϕ_{it} are the critical energies required for impact ionisation and the creation of interface traps respectively.

Using quasi-static (an equivalent DC stress was calculated from the applied AC stress using the duty cycle of the AC signal) analysis and solving for A in the above equation, the equations are simplified as,

$$A = \left[\frac{I_{ds}}{WH}\left(\frac{I_{SUB}}{I_{ds}}\right)^m\right]^n \qquad \text{--- (3.34)}$$

Substituting A into the equation, the degradation is modelled as,

$$\Delta D = \left[\frac{I_{ds}}{WH} \left(\frac{I_{SUB}}{I_{ds}} \right)^{m} \right]^{n} t^{n} \qquad \text{--- (3.35)}$$

or $$(\Delta D)^{1/n} = (WH)^{-1} (I_{SUB})^{m} (I_{ds})^{1-m} t \qquad \text{--- (3.36)}$$

and the degradation at failure is,

$$\Delta D_f = A \tau^{n} = \left[\frac{I_{ds}}{WH} \left(\frac{I_{SUB}}{I_{ds}} \right)^{m} \right]^{n} \tau^{n} \qquad \text{--- (3.37)}$$

Since $(\Delta D)^{1/n}$ is a linear function of time, this quantity can simply be summed over the time period of the SPICE analysis. If $t_0 \ldots t_p$ are the individual time points of SPICE, then

$$[\Delta D_{(tot)}]^{1/n} = [\Delta D(t_1 - t_0)]^{1/n} + \ldots + [\Delta D(t_p - t_{p-1})]^{1/n} \qquad \text{--- (3.38)}$$

To find the device lifetime assuming a periodic signal, a simple linear extrapolation in terms of $\Delta D^{1/n}$ is all that is necessary. The number of time intervals of the SPICE analysis needed so that $\Delta D = \Delta D_f$ is simply,

$$N = \left[\frac{\Delta D_f}{\Delta D_{(tot)}} \right]^{1/n} \qquad \text{--- (3.39)}$$

Thus if the length of the SPICE analysis is $t_p = T$ and is equal to the period of the signal, the lifetime is found from

$$\tau = NT \qquad \text{--- (3.40)}$$

$$= T \left[\frac{\Delta D_f}{\Delta D_{(tot)}} \right]^{1/n} \qquad \text{--- (3.41)}$$

or $$\tau = \frac{T W H (\Delta D_f)^{1/n}}{\sum_{h=1}^{p} [I_{SUB}(t_h)]^{m} [I_{ds}(t_h)]^{1-m} (t_h - t_{h-1})} \qquad \text{--- (3.42)}$$

Using the above expression, degradations in threshold voltage, transconductance degradation and current degradation can be determined at any time point. Usually the lifetime of a device is defined as the time for 10% degradation in the device parameter, the lifetime is estimated by inserting $\Delta D_f = 0.10$ in the equation.

There have been reports [3.16, 3.31, 3.34, 3.35] of enhanced hot-carrier

degradation from stressing using AC wave forms. This has been attributed to capacitively coupled spikes appearing in the drain voltage during stress. BERT model has not incorporated the enhanced degradation due to AC stress, but it will warn the users when it detects wave forms that could cause enhanced hot-carrier degradation.

3.4.2.2 Leblebici model

The recognition of the significant difficulty in circuit level simulation of hot-carrier effects due to the very slow rate at which device degradation progresses led to the Leblebici degradation model [3.16]. In this approach, the degradation models are applied to predict the hot-carrier induced device degradation accurately within a time interval of length T_1. Then the amounts of device and circuit degradation are predicted for the operation time interval $T_2 = kT_1$, where $k > 1$. The period of the input wave form is $T_0 << T_1\ T_2$. The simulation procedure is as follows:

1. Simulate the circuit for one period (T_0) and determine the stress conditions (terminal voltage wave forms) associated with each nMOS transistor.
2. Using the hot-carrier degradation models, determine the amount of degradation that each transistor will experience at the end of time interval T_1.
3. Update the damage parameters of each transistor to specify the hot-carrier degradation sustained at the end of T_1.
4. Return to step (1) and repeat the procedure k times such that $T_2 = kT_1$.

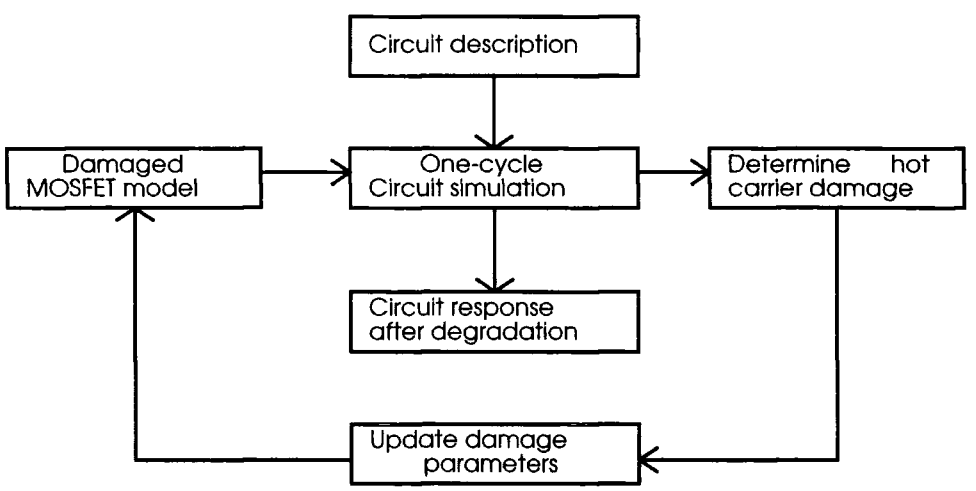


Fig. 3.8 Reliability simulation steps: Leblebici model

The major steps involved in this model is shown in figure 3.8.

The results of each circuit simulation cycle for one period T_0 are used to estimate the amount of hot-carrier induced damage each transistor will experience during a time interval T_1. The reliability tool will automatically carry out this procedure and the circuit response after degradation can be analysed.

3.4.2.3 HOTRON model

HOTRON is another hot-electron effect simulator used for predicting reliability at circuit level [3.38]. Hot electron measurements are carried out under DC stress conditions using substrate current as a monitor. Stress experiments are normally performed under accelerated conditions in order to observe the degradation results in a reasonable length of time. The device lifetime is predicted as,

$$\tau = C\left(\frac{I_{SUB}}{W}\right)^{n} \qquad \text{--- (3.43)}$$

where C and n are empirical parameters dependent on the fabrication process. A more realistic approach is used to determine device degradation and to predict lifetime by measuring 10% degradation of the delay time of the circuit under test. This degradation has to be measured under the real-life circuit operating condition. In a circuit environment, the substrate current is a time-dependent wave form and must be converted to an equivalent DC value via integration. This value can then be used to estimate the amount of device degradation that will occur for a particular MOSFET by comparison to DC stress characterisation data. This individual device degradation then has to be converted to the circuit performance degradation via circuit simulation.

3.4.2.3.1 AC to DC transformation

To determine the stress on each MOSFET in a circuit operation, a circuit simulation is performed. The substrate current for each device is then calculated and then converted to an equivalent AC stress from empirical DC stress degradation with respect to substrate current. When the substrate current is a function of time, the degradation model is of the form,

$$[\Delta p(t)]^{1/n} = C^{1/n} I^{m/n}(t)\, t \qquad \text{--- (3.44)}$$

where $I = I_{sub}/W$. With a linear time dependence, we can integrate to a time T:

$$[\Delta p(T)]^{1/n} = C^{1/n} \int_0^T I^{m/n}(t)\, dt \qquad \text{--- (3.45)}$$

and $T = N\, t_p$, where t_p is the period and N the number of cycles. The amount of stress is represented by an equivalent DC stress and is given by:

$$\Delta S = \frac{T}{t_p} \int_0^{t_p} \frac{[I(t)]^{m/n}}{[I(ref)]^{m/n}} dt \qquad \text{--- (3.46)}$$

where I(ref) = ($I_{SUB,DC}/W$) under specified DC stress conditions. In practice the integration is over a short time period representing one cycle and then multiplied by the number of cycles required to obtain a longer operational time. Actual device degradation can then be quantified from ΔS by interpolating into a table of SPICE model parameters. This table has been obtained by stressing a MOSFET at some fixed $I_{sub,DC}$ for an interval of time and then characterising that MOSFET for SPICE model parameters.

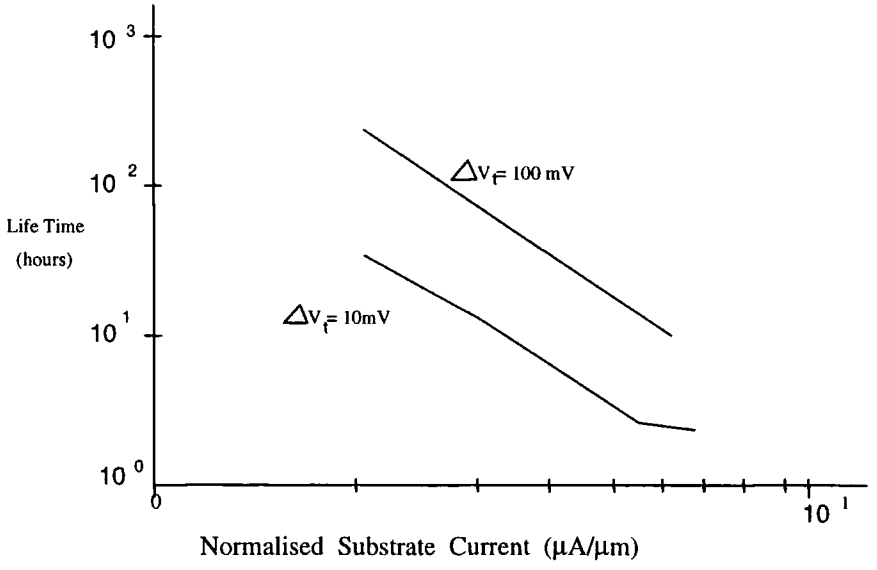


Figure 3.9 Lifetime vs normalised substrate current: HOTRON model

3.4.2.4 RELY degradation model

The RELY Circuit Reliability simulator [3.33], [3.39] consists of several software modules including pre-processing modules, core circuit simulator, stress

monitor modules, degradation prediction modules and post-processing modules. The pre-processing module of RELY translates the user's input file into a format compatible with the circuit simulator and stores the reliability information in the database. The core circuit simulator (SPICE) is used for detailed analysis of small circuits. Stress monitor modules determine the corresponding electrical stresses according to various physical failure mechanisms such as hot-carrier damages. Based on the level of stress on each device, the corresponding degradation is determined in the degradation module. The post processor now evaluates the circuit performance degradation.

The reliability simulator assumes that the stress level changes slowly with time as a result of gradual degradation of the transistors. During the normal operating conditions of a VLSI circuit, the inputs and outputs consist of constantly changing wave forms. This results in constantly changing AC stress wave forms on the individual transistors in the circuit and so the degradations progress relative to the stress on each device. The transistor parameter shifts are correlated with the magnitude of the stress using degradation parameters obtained directly from DC stress experiments. During actual operation, circuits are stressed using AC wave forms and so the degradations under AC stress are evaluated using DC stress degradation data. Transistors subjected to the AC stress are usually found to have excessive degradation when compared to DC stress.

3.4.2.5 PRESS degradation model

The *Philips REliability Simulation Software* (PRESS) is based on Philips' proprietary circuit simulator *Pstar* [3.40]. The reliability model which is called *Press* (Philips Reliability Simulation Shell) and is implemented in the input language of the simulator. The approach taken is different from those previously described and supersedes the costly degradation updating scheme. The degradation can be calculated at every transient time-step due to the fact that the reliability model is specified in the Pstar input language. Degradation by AC signals is calculated based on a DC degradation model and duty cycle effects.

PRESS also allows the user to choose between a so called *indicator* mode and a *full-fledged simulator* mode. Using the indicator allows for *degradation flagging*,

i.e. warning the user for device degrading beyond a specified level. Although the results in this model are less accurate, the indicator mode is useful for a quick check on potential reliability hazards with respect to hot-carrier degradation. The full fledged model allows the user to simulate the degradation of a circuit in more detail. The lifetime is given as,

$$\tau = K\left(\frac{I_{SUB}}{I_{ds}}\right)^{-m}\left(\frac{W}{I_{ds}}\right) \qquad \text{--- (3.47)}$$

and the parameter degradation is modelled as,

$$\Delta Par(t) = C\ \{\ln(1+D.t)\}^{E} \qquad \text{--- (3.48)}$$

where K, C, m, D and E are fitting parameters dependent on the processing technology.

3.4.3 Optimised degradation model

The degradation model has been developed using substrate current as a monitor and was modelled using BERT degradation model. Since the substrate current model has been modified based on the 0.7 micron process technology and the SPICE model parameters used to model the degradation effects, it was necessary to optimise the degradation model and the optimisation procedure is discussed below:

The optimised substrate current model and a set of validated HSPICE or SPICE MOS model parameters were used for the degradation model. The model described below has been adapted from the previous models in such a way that known degradation effects are incorporated in the simulations by using characterisation techniques described later in this chapter. This way the degraded SPICE models can be used for simulation of the whole circuit and hence the timing degradations on the circuit can be evaluated. The procedure for the optimisation is shown below in figure 3.10 using a block diagram.

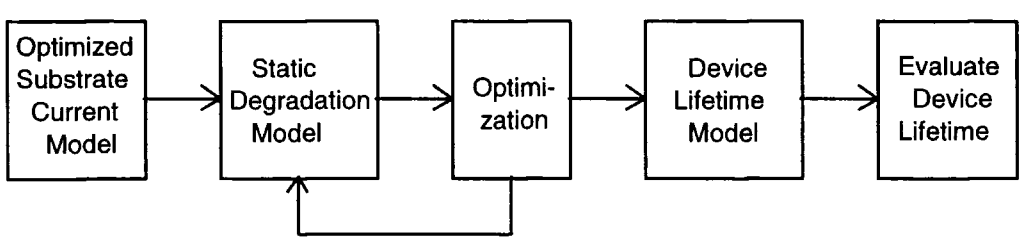


Figure 3.10 Optimisation of Degradation model

The degradation and the lifetime of a number of devices having minimum dimensions, two and three times the standard width were determined using the degradation model. Using a set of validated HSPICE model parameters, the device simulations were carried out and the normal (undegraded) channel and substrate currents were determined. Using the substrate current as a monitor, the stress on each of the devices was evaluated using the post processor. The degradation was evaluated for a ten hour stress period using the optimised model. It was assumed that the stress and hence the degradation was linear during this period. Based on this information, a degraded HSPICE model is generated.

The following *four* HSPICE level 6 parameters are used to model the degradation effect:

(i) NFS (number of fast interface states): At low gate voltages (below half drain voltage) the hot hole effect is dominant and will generate a large number of additional interface states all along the conducting channel and this is modelled as an increase in NFS.

(ii) UO: Mobility degradation; this is mainly due to the scattering of electrons in the channel as a result of electron traps generated by hot holes at low to medium gate voltages.

(iii) VTO: Shift in threshold voltage is due to trapped electrons at the interface (close to the drain) and that trapped in the gate-oxide. Normally this will give rise to an increased applied gate voltage before the channel is inverted and is modelled as increased threshold voltage for the nMOS transistor.

(iv) RSH: Source and drain sheet resistance; the impact ionisations at the high field damage the silicon lattice close to the drain and reduce the conductance of silicon. This effect is modelled as an increase in RSH.

It has been reported by Mistry & Doyle [3.35] that the enhanced hot-carrier stress damage observed under AC stress conditions is due to three different damage mechanisms namely, that occurring during low to medium gate voltages, medium gate voltage and that at medium to high gate voltages. All three modes are necessary to

explain the enhanced degradation during dynamic stress and so the three degradation mechanisms are included in this degraded model. The trapping of electrons at the interface is modelled as a threshold voltage shift, the scattering of electrons at low to medium gate voltages is modelled as mobility degradation and the change in the sub threshold slope is modelled using the NFS parameter. The device degradation is thus given by:

$$\Delta D = \left[\frac{I_{ds}}{WH} \left(\frac{I_{SUB}}{I_{ds}} \right)^{m} \right]^{n} t^{n} \qquad \text{--- (3.49)}$$

where the fitting parameters were determined by comparing various published values and using simulation results. These parameters are given by, H = 10^6, m = 2.9, n = 0.5 and t is the effective duration of stress. For AC simulations, the effective stress time must be estimated from the duty cycle for all the devices in the circuit. The degradation as a function of the substrate current evaluated using this model is given below in figure 3.11.

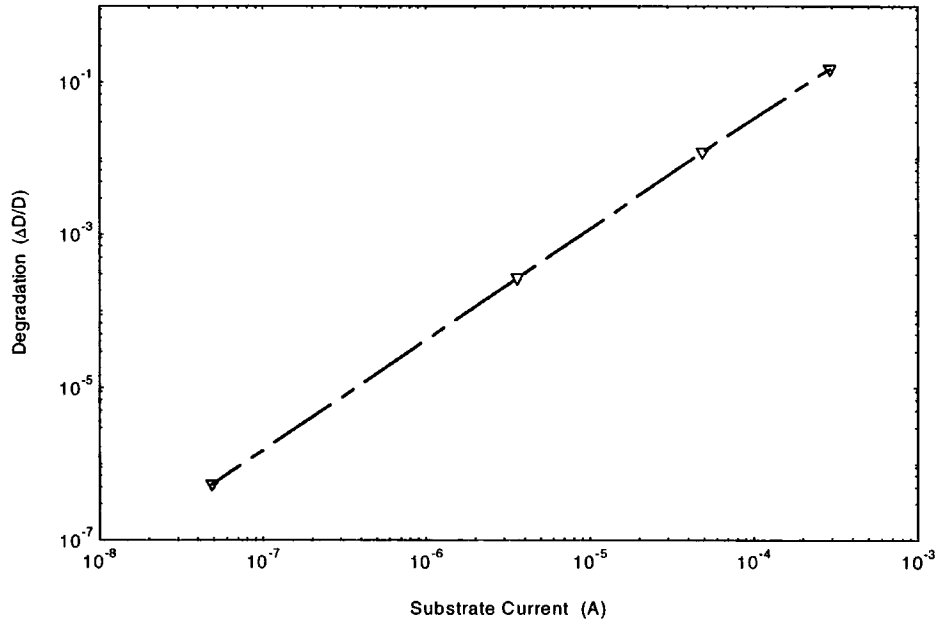


Figure 3.11 Device degradation as a function of Substrate current plotted using the optimised model (Device: N 1/0.8, Process: EC/3)

using BERT lifetime model [3.32] by replacing the constants H, m and n from our optimised substrate current model and is given by,

$$\tau = \frac{W H \left(\Delta D_f\right)^{1/n} \left(I_{ds}\right)^{m-1}}{\left(I_{SUB}\right)^{m}} \qquad \text{--- (3.50)}$$

The lifetime is normally defined as the time for degradation in any of the main device model parameter to change by 10 percent of the original undegraded value. Using this definition, the lifetime was evaluated for the 0.7 micron minimum dimension nMOS transistor as a function of substrate current. The devices were simulated by sweeping the gate voltage from 0 V to 5 V while using fixed drain biases at 2 V, 3 V, 4 V and 5 V respectively. The substrate and drain currents were calculated and the lifetime determined using equation (3.50) by substituting ΔD_f equal to 0.1. The graph of lifetime vs substrate current is given in figure 3.12.

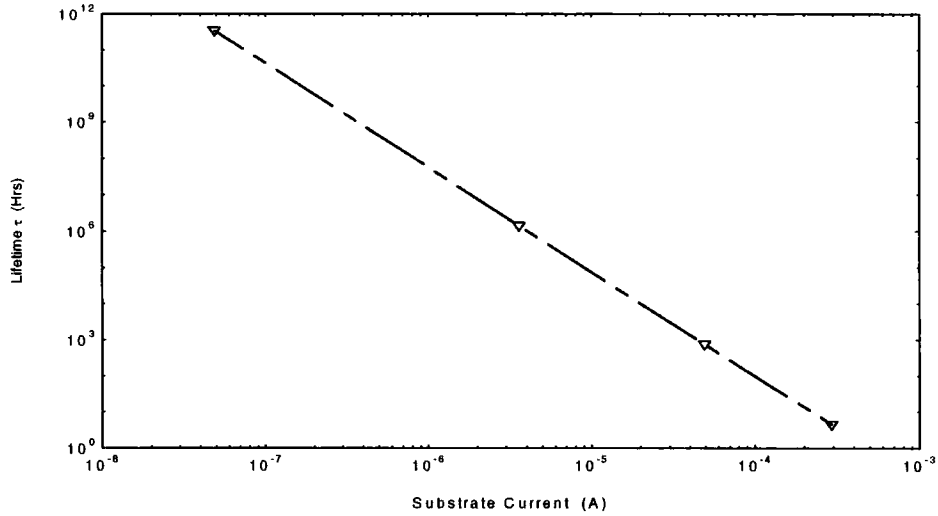


Figure 3.12 Lifetime vs Substrate current: Optimised model (Device: N 1/0.8, Process: EC/3)

3.5 Characterisation of degradation effects

The model developed must be validated using experimental results. In this section it will be shown that the optimised degradation model developed can accurately predict nMOSFET degradation. The hot-carrier sensitive MOSFET parameters were incorporated into the SPICE simulator and the characteristic curves were plotted with and without degradation. The simulation results were compared

with experimental results from many researchers and was shown to predict the static characteristics of a degraded device. The characterisation of the degradation effects by comparing results from other researchers are discussed below.

Lunenborg [3.41] has verified from experimental measurements and by simulations that the drain saturation current of an nMOS device will degrade by 170 μA after stressing it at maximum stress conditions for 10^6 seconds when the device dimensions were W=10 μm and L=0.55 μm. The simulations performed using the same device dimensions as Lunenborg's work produced a drain saturation current degradation of 370 μA (at a saturation current of 4.61 mA) when the device SPICE parameters were degraded by 10% and 190 μA for a device degradation of 5%. A characterisation plot showing the degradation in drain current for Lunenborg's work at 10% device degradation is shown in figure 3.13 and the SPICE device parameter values used for the modelling of the degradation are given in table 3.1.

UO	VTO	NFS	RSH
467	0.832	4E11	213

Table 3.1 SPICE parameter values used for degradation modelling (Process EC/3)

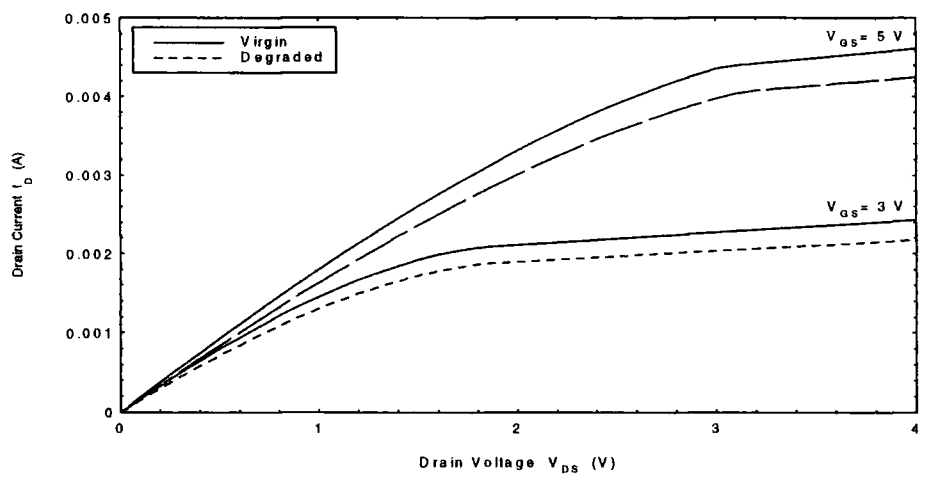


Figure 3.13 Characterisation of degradation effects: I_D vs V_{DS} plotted for a virgin device and for a device with SPICE parameters degraded by 10% (Device: N:10/0.55, Process: EC/3) Lunenborg [3.41].

The devices used in the simulations were all designed using minimum size dimensions according to technology EC/3 and it was necessary to establish a correlation between the stress time and the SPICE model parameter degradation to produce the same drain current degradation. The output characteristic curves were plotted for a minimum size nMOS virgin transistor and with 5% and 10% degradations. Using standard characterisation techniques, a relationship between stress time and degradation of device parameters under standard conditions was established. The plot shown below is the output curves for the standardised device with and without degradation.

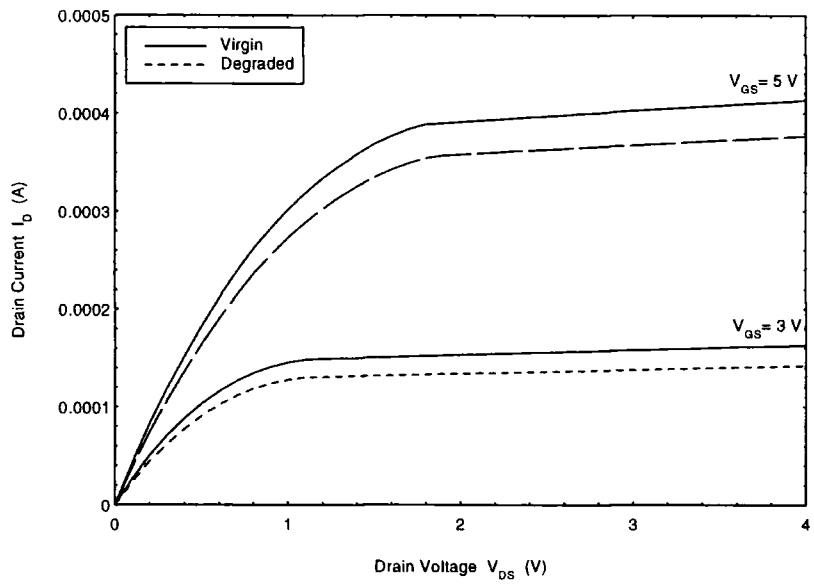


Figure 3.14 Degradation characterisation under normalised conditions: SPICE parameters degraded by 10% (Device N:1/0.8, Process EC/3)

It is also necessary to verify that the degraded SPICE models will produce drain current degradations in the linear region comparable to that produced by Lunenborg experiment. A set of simulations were performed in the linear region of the characteristic curve and the plots were compared with that for the experimental model. A transfer curve plotted for characterisation in the linear region is shown in figure 3.15.

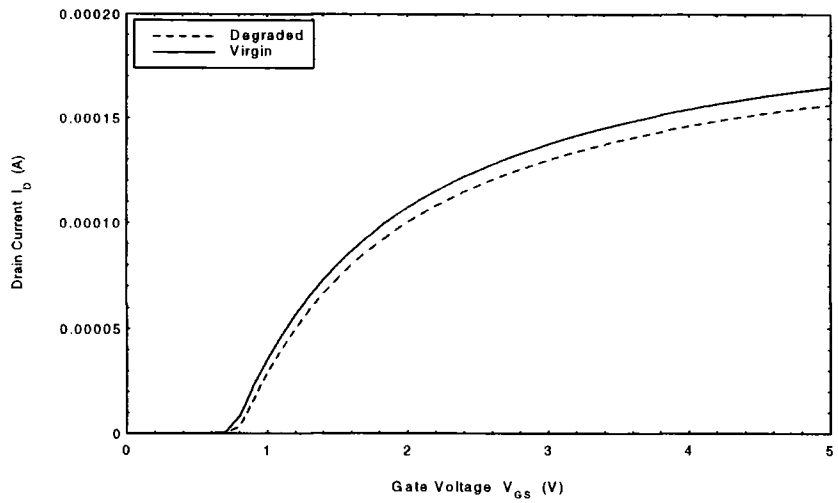


Figure 3.15 Characterisation of degradation of Drain Current in the linear region: I_D - V_{GS} plotted at V_{DS} = 0.1 V for virgin and 5% degraded device (Device: N:10/0.8, Process:EC/3)

3.5.1 Characterisation simulation results

Saturation region: A decrease in saturation drain current of 18 μA for a device degradation of 5% at a drain current of 413 μA.. This is equivalent to a stress time of 10^6 seconds at maximum substrate current level.
Linear region: A decrease in linear drain current of 2 μA for every 5% degradation in device parameter for the same stress time period.

3.6 Chapter summary

Hot-carrier degradation mechanisms have been reviewed in this chapter. A clear understanding (from the present CMOS technology point of view) of the physical mechanisms responsible for the generation of hot-carriers and the degradation of the device parameters due to hot-carriers has been achieved. Using existing models, a new substrate current model was proposed. The optimisation steps for the development of the model has been explained. The substrate model has been used to monitor the generation of hot-carrier induced substrate current and was used as a monitor for stress on MOS devices.

The stress level monitored using the substrate current was employed to model the device degradation model under static conditions. Utilising the degradation model, a lifetime model has been proposed. The characterisation of various degradation effects were carried out and has led to the validation of the model. The substrate current and the degradation models will be used for dynamic stress simulations of CMOS bistable circuits in the next chapters. The design and simulation of CMOS bistable circuits are discussed in the next chapter.

Chapter 4

The Analysis of CMOS Bistable Circuits

Many of the wearout processes affecting the reliability problems in CMOS VLSI circuits have been identified in chapter two. Hot-carrier degradation in submicron CMOS devices and its effect on device parameters have been modelled in chapter 3. Hot-carrier degradations are a major reliability concern for submicron VLSI circuits. Before one can investigate the effects of hot-carrier degradations on bistable circuits and a solution to these critical problems can be found, a thorough understanding of various forms of bistable circuits and their operational characteristics as well as timing parameters must be ascertained. This chapter is concerned with the design and testing of basic D-latch circuits. Consideration is given to the specifications of the circuit and to simulate the standard conditions at which these specifications are measured. It was decided to use CMOS technology for the design of the D-latch circuits for incorporation into VLSI systems and it is very important to understand the performance characteristics of the circuits designed using devices having small geometry. Special attention is given in the design of minimum size inverters, transmission gates and other logic elements so as to maintain the symmetric pull-up and pull-down wave shapes at the outputs of the latches under normal loading conditions.

The *SPICE* (Simulation Program with Integrated Circuit Emphasis) [4.1] circuit simulation program is used for the simulation and evaluation of the circuit parameters. SPICE was originally developed at the University of California at Berkeley and there are many commercial versions now available for IC design and simulation. SPICE is a very powerful circuit simulation package which contains built-in mathematical models for integrated circuit transistors, allowing for many physical effects that are ignored in first-order device equations. It contains many features, but in digital IC design it is used largely to simulate the transient response when circuit inputs change state. SPICE level 3 commercial process parameter values were used for the circuit simulations since this produced simulated response which was very close to the actual circuit behaviour compared to level 1 and level 2 simulations. *HSPICE* simulations were carried out for the selected latch circuits for determining their timing parameters. HSPICE is a commercial version of the original SPICE2, released by *Meta-soft* [4.2] and has many enhanced features such as accurate models for commercial integrated circuit processes.

Chapter four starts with a discussion of the various forms of the family of bistables. A few of the circuits must be selected for analysis and simulations. The parameters to be analysed are defined and the inputs and outputs standardised. The selection and standardisation of the SPICE device model parameters is also discussed. The final section of this chapter is devoted to the simulations and analysis of the results of the simulations for the selection of the best circuits for further simulations.

4.1 Bistable Circuits: Terminology

Two basic categories of bistables are the latch and the flip-flop. Bistable devices have two stable states called *SET* (logic 1) and *RESET* (logic 0), they can retain either of these states indefinitely, making them useful as storage devices. The basic difference between the latch and the flip-flop is the method used for changing from one state to the other. [4.3-4.5]

Latch: Latches are bistables that can reside in either of the two stable logic states by virtue of a positive feedback. Outputs Q and Q' are always complements of each other and, in its simplest form, are controlled by two inputs called *SET* and *RESET* inputs for obvious reasons.

Gated Latch: A gated latch requires an additional input called *ENABLE (EN)* before SET and RESET can be activated.

Gated D-latch: The gated D-latch has only one input called the *D (Data)* input in addition to EN. When the D input is HIGH and the EN is *active* (EN can be active HIGH or LOW depending on the design), the latch will SET; when D is low and EN is active, the latch will RESET. Since the output responds to the D input as long as EN is active, the circuit is called a *transparent D latch.*

Edge-Triggered Flip-flops: Flip-flops are bistables in which the outputs change state only at a specified point on a triggering input called the *CLOCK.*
Latches, bistables and flip-flops are used interchangeably in many technical books, but we will use D-latch to represent the transparent D-type latch through out this thesis. A description and the characteristic timing parameters for the transparent latch are given in the next sections.

4.2 Design of Transparent Latches

The D-type Latch is the simplest data storage circuit in the family of bistables. It is the basic element in most CMOS flip-flop circuits and can be used to design edge triggered and Master-slave (M/S) flip-flops. The logic symbol of a simple D-type latch is given in figure 4.0 [4.5]. It has two inputs D (Data or Delay) and EN (Enable or Clock) and it has two outputs Q and its complement Q'. The latch is called transparent because data passes straight to the output (allowing for a small delay) as long as the EN input is active. When EN goes inactive, the current value of Q is latched and further changes in D are ignored. The EN input can be active high or low.

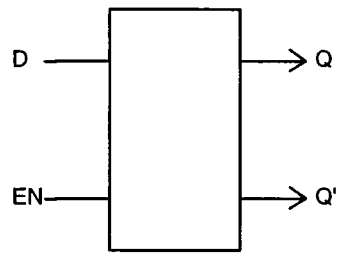


Figure 4.0 D-latch logic symbol

4.2.1 Design of D-type Latch with Reset

The designs of D-latch circuits using CMOS technology used a number of configurations of MOS transistors, transmission gates, tristate devices and other basic logic gates to obtain simple and dependable latch circuits which can be incorporated into VLSI systems as standard elements. A *RESET* input was added to the design so that the outputs can be brought to a predictable logic state which will ease the testing process. The D-latch circuits are shown in figure 4.1 [4.3-4.7, 4.11]

The circuits in figure 4.1 (a), (b) and (d) uses transmission gates as multiplexers connected between input and the feed-back path and have inverters, NOR gates or NAND gates (or a combination of these) in the signal path. Circuit in (c) uses two tri-state devices as a multiplexer and circuit (e) uses a weak inverter (with long channel and reduced gain) in the feed-back path. Circuit (f) uses NAND gates and (g) is a mixed-gate version of the typical latch circuit. The ninth latch designed using NAND gates is identical to the one shown in figure 4.1 (f) but has an additional reset input connected to the NAND gate with the DATA input using a 3-input NAND gate. The latch circuit shown in figure 4.1(h) uses a pass transistor in place of the transmission gate found in other designs (see circuit (e) for example). Since the pass transistor

introduces a threshold voltage drop to the D- input, the input inverter must be specially designed to have a transition voltage equal to $\frac{1}{2}(V_{DD} - V_{Tn})$.

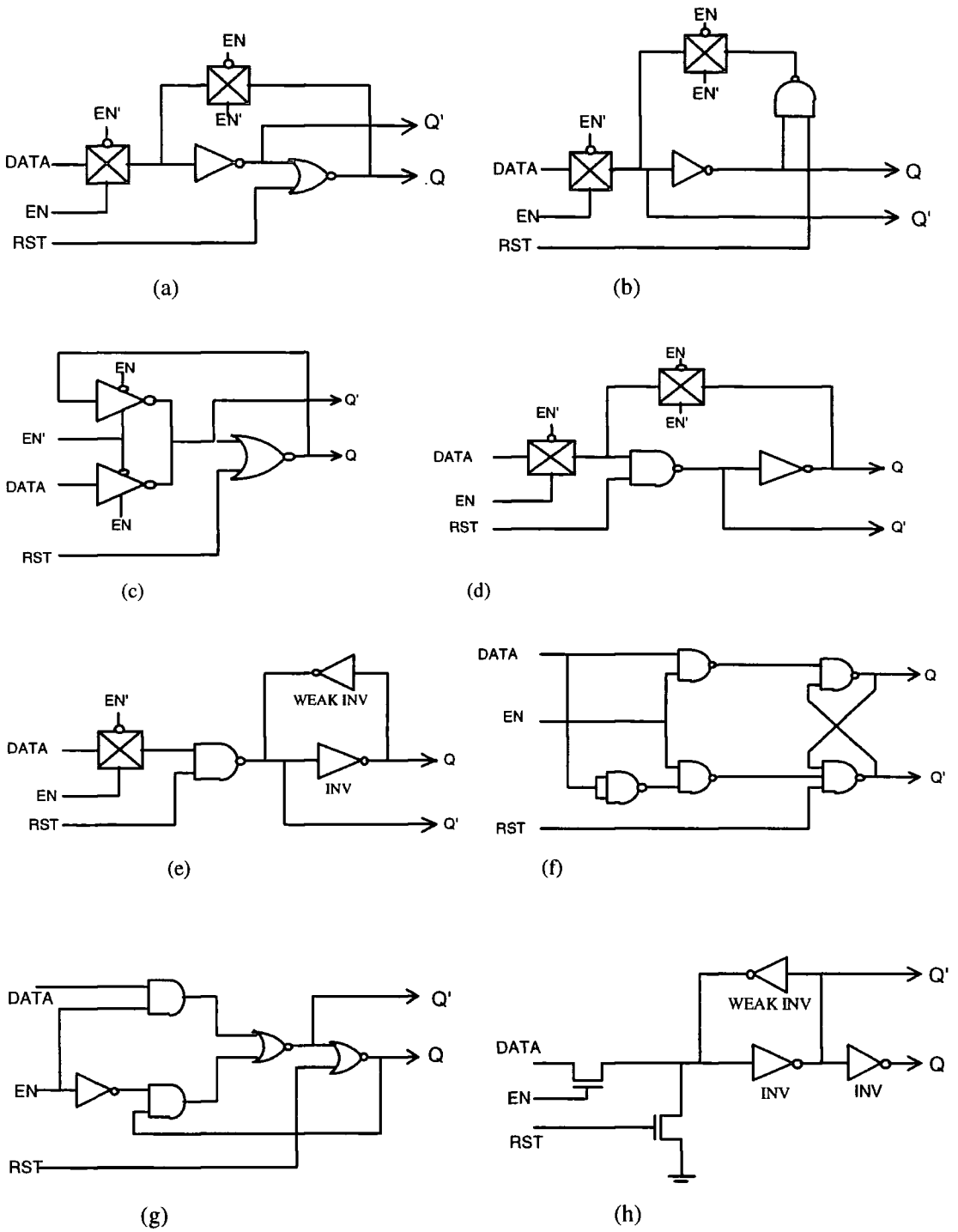


Figure 4.1 D-latch circuits

The devices used in the latch circuits were designed to optimise the circuit

performance. The optimisation of the devices used in the latch circuits are discussed next.

4.2.2 Optimised CMOS D-latch Design

The nine latch circuits designed using CMOS technology design rules as discussed above have been improved to minimise the delays and enhance performance. These improvements are discussed below.

(a) Inverter Design for a Transition Voltage of 2.05 V

The threshold voltages for the nMOS and pMOS transistors in the process used for this work were 0.902 V and -0.504 V respectively. The transition voltage is given by [4.3],

$$V_t = \frac{V_{Tn} + \sqrt{\beta_p / \beta_n}\,(V_{DD} - |V_{Tp}|)}{1 + \sqrt{\beta_p / \beta_n}} \qquad \text{--- (4.1)}$$

$$\text{but} \quad V_t = \frac{(V_{DD} - V_{Tn})}{2} \qquad \text{--- (4.2)}$$

$$= \frac{(5V - 0.902)}{2} \quad = 2.05 \text{ V}$$

The gain factor of a transistor is given by,

$$\beta = \frac{\mu \varepsilon W}{t_{ox} L} \qquad \text{--- (4.3)}$$

where μ is the mobility of charge carriers, ε is the permitivity of the gate oxide, W width of the transistor channel, L length of the transistor and t_{ox} is the thin-oxide thickness. Therefore,

$$\frac{\beta_n}{\beta_p} = \frac{\mu_n W_n L_p}{\mu_p W_p L_n} \qquad \text{--- (4.4)}$$

and

$$W_n = W_p \frac{\beta_n}{\beta_p} \frac{\mu_p}{\mu_n} \qquad \text{--- (4.5)}$$

For a transition voltage of 2.05 V, the nearest ratio for β_n/β_p was calculated using equation (4.1) and was found to be = 4.5. For a normal inverter, the width of the p-transistor channel was designed to be 2.88 μm for a drawn width of 5 μm and the ratio of the mobilities calculated using CMOS 3 micron (Process EM/3) parameter values

was found to be equal to 1.733. Substituting the above evaluated value of the gain factor ratio in equation (4.5), the widths for n- and p- transistors were calculated.

The final design is :- $W_p = 2.88\ \mu m$, $L_p = 3.00\ \mu m$,
$W_n = 7.73\ \mu m$ and $L_n = 3.00\ \mu m$
and has a transition voltage of 2.05 V.

In order to confirm the design, the inverter circuit was coded and simulated using SPICE and the transfer curve was plotted. The transfer curve indicated a transition voltage of 2.09 V for the threshold adjusted inverter.

(b) Optimised CMOS Inverter Design

It is desirable to have the same peak drive current in the n- and p-channel MOS transistors so as to have symmetrical rise and fall times for the inverter. First order theory of MOST gives the saturated drive current as:

$$I_D = \frac{\beta}{2}(V_{GS} - V_T)^2 \qquad \text{--- (4.6)}$$

For the same drive current in n- and p-channel transistors: [4.3]

$$\frac{W_p}{W_n} = \frac{L_p}{L_n}\frac{\mu_n}{\mu_p}\left[\frac{V_{GS} - V_{Tn}}{V_{GS} - |V_{Tp}|}\right]^2 \qquad \text{--- (4.7)}$$

For $L_p = L_n$ and for the special case when $V_{Tn} = |V_{Tp}|$

$$\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p} \qquad \text{--- (4.8)}$$

Equation (4.7) or (4.8) can be used to determine transistor sizes in the design. In Level 3, although μ_n and μ_p are given, these are low-field values. It is better to use the actual drive current, assumed to be given by an equation of the form of (4.6). By using the drive current provided by the manufacturer for drawn L = W = 3 μm and denoting them as I_{Dn}, I_{Dp} for n- and p- transistors,

$$\left(\frac{I_{Dn}}{I_{Dp}}\right)_3 = \left(\frac{W_{n(eff)}}{W_{p(eff)}}\right)_3 \left(\frac{L_{p(eff)}}{L_{n(eff)}}\right)_3 \left(\frac{V_{GS} - V_{Tn}}{V_{GS} - |V_{Tp}|}\right)^2 K \qquad \text{--- (4.9)}$$

where K is a measure of the relative drive capabilities of the n- and p-MOSTs. K should be $\frac{\mu_n}{\mu_p}$ in Level 1, but in Level 3 we can calculate it. From (4.9),

$$K = \left(\frac{I_{Dn}}{I_{Dp}}\right)_3 \left(\frac{W_{p(eff)}}{W_{n(eff)}}\right)_3 \left(\frac{L_{n(eff)}}{L_{p(eff)}}\right)_3 \left(\frac{V_{GS} - |V_{Tp}|}{V_{GS} - V_{Tn}}\right)^2 \qquad \text{--- (4.10)}$$

and can be evaluated from the data provided. W_{eff} and L_{eff} values will be those for 3 x 3 μm drawn devices. Applying this to a minimum size n-channel MOST used in an inverter, we can find the width of the pMOST. The minimum drawn size for nMOST was W_n = 4 μm and L_n = 3 μm. The drive current in this transistor should be the same as in the p-channel transistor with W_p to be determined and was labelled as $[W_{p(eff)}]_4$.

Using values of dimensions for W_n = 4 μm, equation (4.9) gives,

$$\left(\frac{W_{p(eff)}}{W_{n(eff)}}\right)_4 = \left(\frac{I_{Dp}}{I_{Dn}}\right)_4 \left(\frac{L_{p(eff)}}{L_{n(eff)}}\right)_4 \left(\frac{V_{GS} - V_{Tn}}{V_{GS} - |V_{Tp}|}\right)^2 K \qquad \text{--- (4.11)}$$

where $\left(\frac{I_{Dp}}{I_{Dn}}\right)_4 = 1$ for this design of the inverter.

Equation (4.11) was evaluated to find W_p(drawn) for *high, typical and low* drive conditions.

Substituting (4.10) into (4.11),

$$\left(\frac{W_{p(eff)}}{W_{n(eff)}}\right)_4 = \left(\frac{L_{p(eff)}}{L_{n(eff)}}\right)_4 \left(\frac{I_{Dn}}{I_{Dp}}\right)_3 \left(\frac{W_{p(eff)}}{W_{n(eff)}}\right)_3 \left(\frac{L_{n(eff)}}{L_{p(eff)}}\right)_3 \qquad \text{--- (4.12)}$$

But channel lengths are the same in the 3 micron test MOSTs and so equation (3.12) simplifies to,

$$\left(\frac{W_{p(eff)}}{W_{n(eff)}}\right)_4 = \left(\frac{I_{Dn}}{I_{Dp}}\right)_3 \left(\frac{W_{p(eff)}}{W_{n(eff)}}\right)_3 \qquad \text{--- (4.13)}$$

and the effective width of the p- transistor is given by,

$$\left(W_{p(eff)}\right)_4 = \left(W_{n(eff)}\right)_4 \left(\frac{I_{Dn}}{I_{Dp}}\right)_3 \left(\frac{W_{p(eff)}}{W_{n(eff)}}\right)_3 \qquad \text{--- (4.14)}$$

The effective widths are calculated by subtracting two times the SPICE parameter WD (width reduction due to diffusion) from the drawn values. Hence equation (4.14) becomes,

$$\left(W_{p(drn)}\right)_4 - 2WD_p = \left[\left(W_{n(drn)}\right)_4 - 2\,WD_n\right]\left[\left(\frac{I_{Dn}}{I_{Dp}}\right)_3 \left(\frac{\left(W_{p(drn)}\right)_3 - 2\,WD_p}{\left(W_{n(drn)}\right)_3 - 2\,WD_n}\right)\right] \qquad \text{--- (4.15)}$$

For drawn dimensions $(W_p)_3$ = 3 μm, $(W_n)_3$ = 3 μm and $(W_n)_4$ = 4 μm, the drawn width for the pMOST is given by,

$$\left(W_{p(drn)}\right)_4 = \left[(4\mu m - 2\,WD_n)\left(\frac{I_{Dn}}{I_{Dp}}\right)_3 \left(\frac{3\mu m - 2\,WD_p}{3\mu m - 2\,WD_n}\right)\right] + 2\,WD_p \qquad \text{--- (4.16)}$$

Using this expression the drawn p-channel widths were close to 5 microns for high-drive, low-drive and typical-drive. The resulting inverter was almost geometrically symmetrical due to the difference in the threshold voltages. This had the advantage that the inverter input capacitance was considerably less than that for a more normal design, about 11 fF compared with 26 fF for the normal one. This could almost double the speed of the circuit but at the expense of a reduced noise margin. The transistor dimensions calculated for all the devices to be used in the D-latch designs are given in appendix A.

(c) Delay Optimisation of Scaled Devices

The propagation delay of a CMOS logic gate chain can be minimised by selecting the proper size for the n- and p- devices. Usually the propagation delay is the sum of the pull-up and pull-down delays of successive stages is found to be a minimum when the pull-up time and pull-down time are equal. As a general rule, when very large fanout ratio is necessary, or when a very complex gate is used, the pFET/nFET size ratio should be chosen so that the gate pulls up and pulls down with approximately equal delay [4.6]. For normal devices driving other normal devices, the size ratio should be chosen smaller than the ratio for delay symmetry. In this case the pullup-pulldown asymmetry of individual gates are compensated by the asymmetries of neighboring gates and the delay asymmetry does not accumulate.

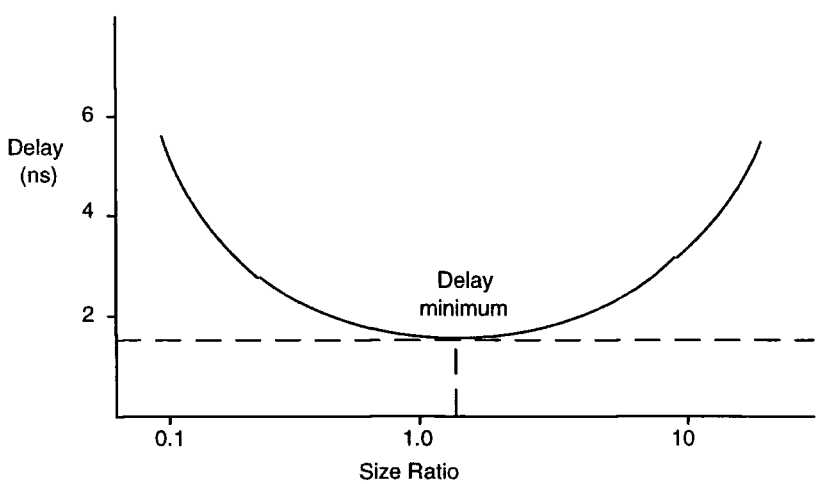


Figure 4.2 Delay of a CMOS inverter versus size ratio of p- and n- devices

As the device dimensions are reduced by scaling, the delays are also reduced and it is observed that the size ratio also falls. For submicron devices, it is found that

the delay minimum is reached when the size ratio is slightly greater than one as shown in graph of figure 4.5 [4.6]. In order to make the design simpler and to keep layout symmetry, it is common to select a size ratio of one for simple structures designed using submicron design rules. It has been reported by Shoji [4.6] that the optimisation of FET size for symmetric delays without assuming any constraints on FET sizes can be a very complex process and so the sizing is often carried out by software. For the latch circuits designed using 0.7 micron design rules, we have opted for layout symmetry and the device size ratio was selected as 1 for simple structures.

4.3 Standardisation of Inputs and Outputs for Simulation

A standard set of input wave forms must be used to simulate D-latches. Also the inputs must be realistic, i.e. it must have similar wave shape, rise time and fall time as encountered in real world integrated circuit devices. Output load and fanout also must be standard so that any variation from standard performance can be compared by monitoring the output wave shape.

4.3.1 Parameters

It was decided that the following parameters would be selected to characterise the D- latches in this analysis:

Propagation delay t_{pd} from input to output can be of two types:

t_{pLH} - propagation delay (output) LOW to HIGH;

t_{pHL} - propagation delay (output) HIGH to LOW.

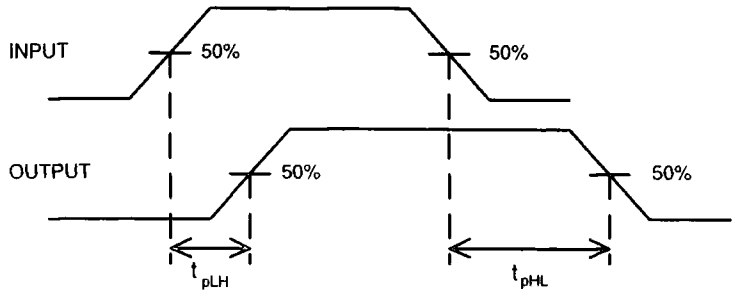
The propagation delays are measured from 50% point on the input wave to the 50% point on the output wave as shown in figure 4.3 (a).

Output transition time t_t relative to input can be of two types:

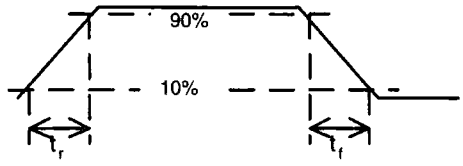
t_r - rise time: is the interval between the 10% point to the 90% point on the rising edge of the output wave.

t_f - fall time: is the interval between the 90% point to the 10% point on the falling edge of the output wave.

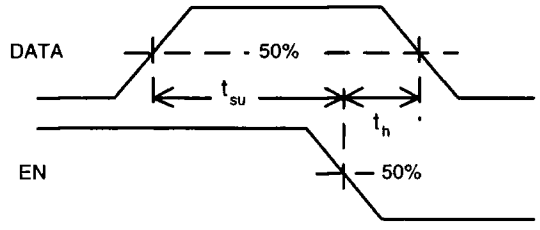
The set-up time t_{su} is defined as the minimum time Data must be set-up prior to edge of EN HIGH to LOW in order to transfer Data reliably to the output.



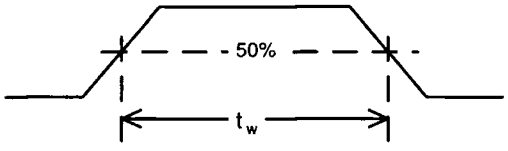
(a) Propagation Delays



(b) Rise and Fall times



(c) Set-up and Hold times



(d) Pulse duration

Figure 4.3 Time Delays

The hold time t_h is defined as the minimum time Data must be held after EN going HIGH to LOW for reliable latching.

Pulse duration (pulse width) t_w is the minimum pulse duration of the input data for reliable operation of the D-latch; a 50% duty cycle is assumed. The maximum operating frequency of the D-latch is decided by t_w. $T_{min} = 2\ t_w$ and $f_{max} = 1/T_{min}$.

Critical Window for metastability t_c is the region of critical triggering for metastable

state operation. Usually it can be defined as the sum of set-up time and hold time.

4.3.2 Standard Conditions for Inputs and Outputs

The testing of the circuit must be carried out with standard input wave forms as well as standard input and output loading. It was decided to use minimum size transistors as the standard with an aspect ratio of W_n:W_p = 1:3 = 4 μm:12 μm while keeping $L_n = L_p$ = 3 μm. This will make the input load (gate capacitance) the same for all circuit simulations. Using the layout of the CMOS inverter, the approximate value of load capacitance driven by the circuit under test was calculated. This load will be taken as a standard for all simulations.

In order to establish a standard wave form for the inputs of the circuit, simulations were carried out with a pulse having 3 ns rise (fall) time applied to an inverter chain consisting of six inverters. Since simulations of long chain of inverters are tedious and can take up a lot of computer time, simpler circuits of one and two inverters are simulated for comparison. Various circuits and set ups used for the simulations, and the results will be discussed in section 4.4. Output loads were also simulated under different conditions. The main aim of this test was to establish a standardised load. Simulation results are discussed in the next section.

4.3.3 Types of Circuits

Nine different D-latch circuits were designed using CMOS technology. The layout of the circuits were generated using design rules from a commercial CMOS process EM/3 and the drain and source area and perimeter values of the transistors were calculated. These were included in the SPICE input file for circuit simulations so as to have the parasitic capacitances and its effect on rise and fall times for the devices to be evaluated by the simulator. A design layout for one of the CMOS D-latch circuit is shown in figure 4.4.

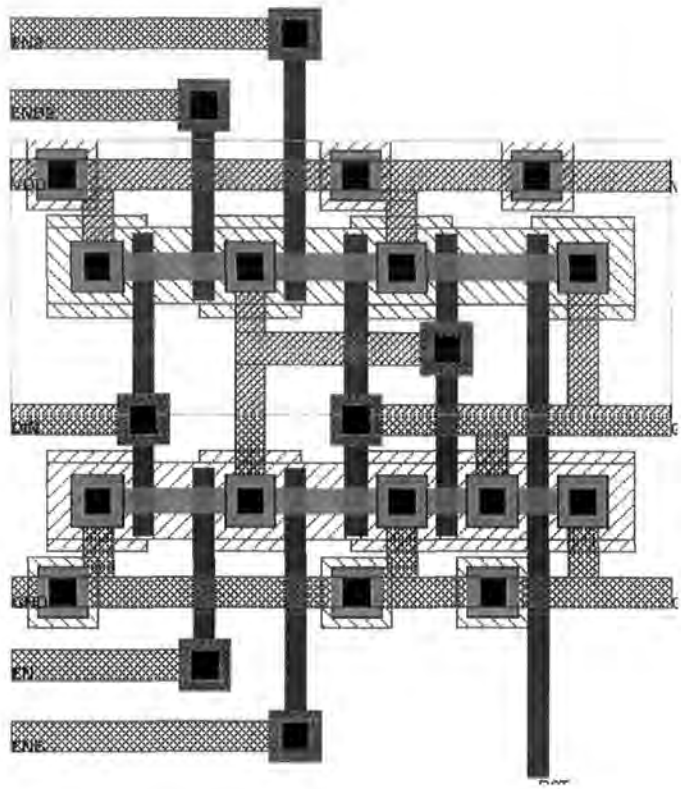


Figure 4.4 Design Layout for latch circuit DL1(Technology EC/3, Device N/P: W/L = 1/0.8)

Three of the selected circuits were redesigned using 1 micron design rules from process EC/13 and were simulated using HSPICE. The circuits were later redesigned using 0.7 micron design rules and simulated using device parameters from process: EC/6 and process: EC/3 as the work progressed. The SPICE.2G device parameters used for circuit simulations in level 1, level 2 and level 3 as well as the HSPICE commercial device parameters which were used for the circuit simulations in level 6 and level 13 are discussed in the next section.

4.4 Standardisation of SPICE Parameters for MOS Devices

Simulations for MOS transistors with SPICE.2G can be carried out using Level 1, Level 2 or Level 3 models. Some commercial versions of SPICE have MOS transistor models going up to level 26 but the three models discussed below are the ones commonly used for research. PSPICE, the PC version of SPICE also has three models for MOS transistors and the parameters as well as the algorithm used are the same in both.

4.4.1 MOS Level 1 Model

The level 1 model is a basic model based on theory presented by *Schichman-Hodges* [4.8]. This model uses the first-order equations based on the GCA (Gradual Channel Approximation) for the MOST and the parameter LAMBDA (channel-length modulation factor) to allow for the lack of saturation of the drain current [4.5]. The five essential parameters for this model are listed in table 4.1.

Parameter	Description
VTO	Threshold voltage for long channel device with zero substrate bias
KP	Gain factor $C_{ox}'\mu$. The same as β if W=L, otherwise $\beta = (KP)\frac{W}{L}$.
GAMMA	Body-effect coefficient
PHI	Surface potential in strong inversion = $2\phi_F$
LAMBDA	Reciprocal of the Early Voltage, determined experimentally.

Table 4.1 Essential SPICE parameters for Level 1 Model

If the above parameters are not given in the level 1 model file, three of these can be calculated using the following values: TOX: Oxide thickness in meters, UO: Low-field mobility for carriers in the channel in $cm^2.V^{-1}.s^{-1}$, NSUB: Substrate or well doping specified in cm^{-3}. In terms of these variables the parameter equations are:-

$$KP = UO\frac{\varepsilon_{OX}}{TOX} \qquad \text{--- (4.17)}$$

$$GAMMA = (2q\,\varepsilon_{si}\,NSUB)^{\frac{1}{2}}\,\frac{TOX}{\varepsilon_{ox}} \qquad \text{--- (4.18)}$$

$$PHI = \frac{2kT}{q}\ln\left(\frac{NSUB}{n_i}\right) \qquad \text{--- (4.19)}$$

VTO also can be calculated theoretically in level 1 but it is better to provide the experimental value which avoids having to give values for the metal-semiconductor work function and surface mobility. The equation for current in the linear region is,

$$I_D = KP\frac{W}{L-2X_{jl}}\left(V_{GS}-V_{Th}-\frac{V_{DS}}{2}\right)^2 V_{DS}(1+\lambda V_{DS}) \qquad \text{--- (4.20)}$$

where X_{jl} is the lateral diffusion and,

$$V_{Th} = V_{TO} + \gamma(\sqrt{2\phi_p - V_{BS}} - \sqrt{2\phi_p}) \qquad \text{--- (4.21)}$$

The current in the saturation region is,

$$I_{D(sat)} = \frac{KP}{2} \frac{W}{L - 2X_{jl}} (V_{GS} - V_{Th})^2 (1 + \lambda V_{DS}) \qquad \text{--- (4.22)}$$

A set of level 1 parameter values for a commercial CMOS process (EM/3) is listed in appendix B.

4.4.2 MOS Level 2 Model

The level 2 model [4.8, 4.12] is an analytic model and it includes many second order effects such as channel length modulation, short channel effects, reduction in the mobility of carriers due to high field strengths and carrier velocity saturation. The first set of parameters are VTO, TOX, UO and NSUB. These are required for various calculations and they are also used to evaluate KP, GAMMA and PHI which need not be supplied in level 2. The next set of parameters are listed in table 4.2.

Parameter	Description
LD	Channel shortening by lateral diffusion from source and drain and the effective channel length L_{eff} = L - 2 x LD,
WD	Channel width reduction due to encroachment of channel sides by field oxide and the effective channel width W_{eff} = W - 2.WD,
XJ	Depth of source and drain junctions,
DELTA	A factor used in modelling the change of V_T at small channel widths.
UCRIT	Critical field parameter
UEXP	Exponential coefficient for mobility
UTRA	Transverse field coefficient
VMAX	Maximum carrier velocity
NEFF	Total channel charge coefficient
LAMBDA	λ is the channel length modulation
NFS	Surface fast state density; this parameter is used for the calculation of sub-threshold currents.

Table 4.2 Device parameters for SPICE level 2 model

UCRIT, UEXP and UTRA are SPICE input parameters used to characterise the degradation of surface mobility μ_o (UO). In the level 2 model, it is necessary to include the source and drain capacitances. These are the voltage dependent depletion layer capacitances of the p-n junction. They have components at the bottom of the implanted layers, proportional to the areas, and at the sides, proportional to the periphery of the source and drain junctions. The model parameters for capacitances are listed in table 4.3.

CJ	Zero-bias bulk capacitance per square meter,
CJSW	Zero-bias perimeter capacitance per meter,
MJ	Bulk-junction grading coefficient,
MJSW	Perimeter capacitance grading coefficient,
CGSO	Gate-source overlap capacitance per meter,
CGDO	Gate-drain overlap capacitance per meter.

Table 4.3 Capacitance parameters for SPICE level 2 model

With oxide isolation, the sides of the source and drain come out into oxide so that the sidewall capacitance is only present on one of the four edges. The capacitance models will only be included if the source and drain areas (AS and AD in m^2) and the perimeter of the source and drain regions (PS and PD in meter) are given in the circuit description for the particular transistor. As the level 2 equations for current and nodal voltages can be very complicated, the reader is requested to refer to Vladimirescu [4.1] or Antognetti [4.8] for further details. The SPICE level 2 parameters for a commercial CMOS process (EM/3) are listed in appendix B.

4.4.3 MOS Level 3 Model

The level 3 model [4.8] is a semi- empirical model and it can be used for very accurate simulations if all the process parameters are available from the manufacturer. The equations for the level 3 model are formulated in the same way as for level 2 model; however, a simplification of the current equation in the linear region has been obtained with a Taylor series expansion. This approximation allows the development of more manageable basic equations than level 2. The short channel effects are included in the calculation of threshold voltage and mobility.

The values of all the parameters are determined experimentally in level 3 through a long sequence of measurements on transistors of various sizes. Computer programs are used to determine the best-fit parameters from the measurements. The resulting values do not necessarily bear much resemblance to those expected from device physics. The overall model accuracy depends on the ability of the engineer to match the characteristics of the device with the parameters of the model. The purpose is both to improve the precision of the model and to limit the complexity of the calculations and the resulting time needed to carry out the program. The empirical model can be used even if the parameters based on measured data is not available, by calculating the parameters from process data. When enough parameters are not supplied, the simulator uses default values which will, at least, provide a computable model. The basic equations are very simple. The current in the linear region is, [4.8]

$$I_{D(sat)} = \beta(V_{GS} - V_{Th} - \frac{1+F_B}{2} V_{DS})V_{DS} \qquad \text{--- (4.23)}$$

where $F_B = \frac{\gamma F_s}{2\sqrt{2\phi_p - V_{BS}}} + F_n$ --- (4.24)

The effects of the short channel influence the parameters V_{Th}, F_s, and β, while the narrow-channel effects influence the term F_n . The dependence of mobility on the gate electric field is simulated with a simple equation than that used for the level 2 model, without any appreciable loss in precision. Thus mobility,

$$\mu_s = \frac{\mu_0}{1 + \theta(V_{GS} - V_{Th})} \qquad \text{--- (4.25)}$$

It is very important to note that the following parameters are meaningless for level 3 model : LAMBDA, UCRIT, UEXP, UTRA and NEFF. The four parameters specific to level 3 model are listed in table 4.4.

Parameter	Description
ETA	Static feedback parameter
DELTA	Channel width factor
THETA	Empirical mobility modulation parameter
KAPPA	Field correlation factor.

Table 4.4 SPICE device parameters specific to level 3

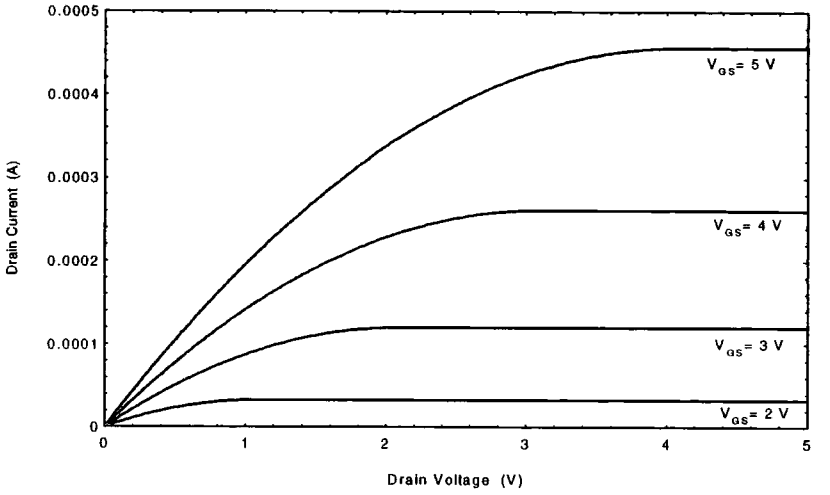
It is also worth noting that for all MOS models (levels 1 to 3) both electrical (e.g. VTO, GAMMA etc.) and processing (e.g. NSUB, TOX etc.) parameters can be entered, but the electrical data will always override the value computed from processing data if also specified. The level 3 model parameters used for the simulations are listed in appendix B.

4.4.4 Optimisation of Model Parameters

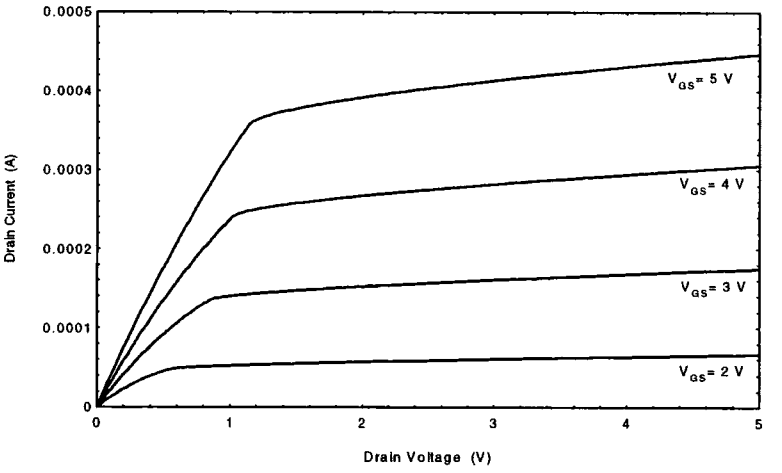
The model parameters given above were used to plot transistor characteristic curves. The plots were used for comparison and optimisation of the device parameters for the three models. It was found that the level 1 model is the easiest one for simulations and it shall be used for a quick and rough estimate of circuit performances. A sample curve of the output characteristics in level 1 using technology EM/3 is shown in figure 4.5(a).

The level 2 model is precise and complex and can be used for long channel and short channel transistors. Because of the complexity of the model equations, it takes much longer to simulate and it often causes convergence problems. The simulations of the short channel transistors show an unacceptable kink at the transition between the linear and saturation regions of each of the output curve [4.8, 4.13]. Figure 4.5(b) is an example of the short channel device effects plotted in level 2 which may lead to non-convergence at the transition region.

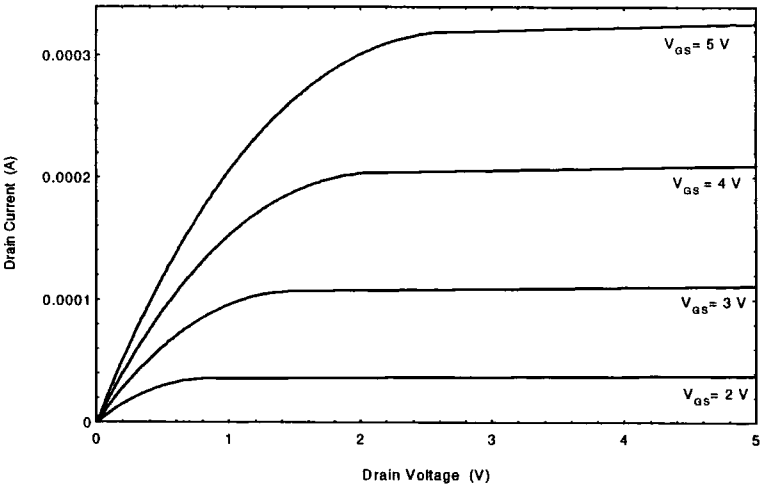
The level 3 model, even though more complex than level 1, is manageable and gives very good results consistent with measured values. The transistor curves plotted using level 3 parameters gave the best results even for short channel transistors. Even though some of the simulations for the D-Latch carried out in level 2 are included in this thesis, it was decided to use the level 3 model for further SPICE simulations. HSPICE simulations using level 6 device parameters were also made for the selected latch circuits. A sample plot in level 3 is given in figure 4.5(c). The circuit digram and the input file used for plotting transistor (output) curves are shown in appendix C.



(a) Level 1 Output curves (Process: EM/3, Device: N 3/4)



(b) Output curves in Level 2: Short channel effects (Process: EM/3, Device: N 2/4)



(c) Output curves, Level 3 (Process: EM/3, Device: N 3/4)

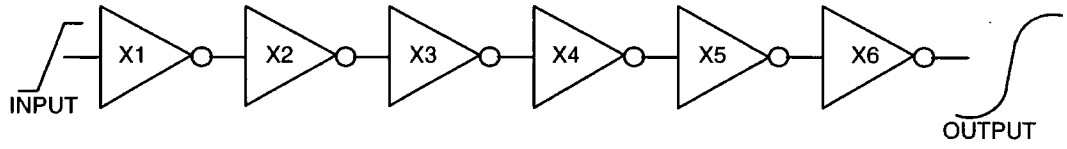
Figure 4.5 Transistor Characteristic Curves plotted using SPICE Levels 1, 2 and 3 device parameters

4.5 Simulations of Latch Circuits

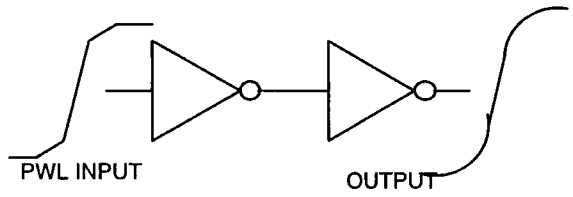
SPICE simulations were carried out to establish the standard input and output environment. The level 3 parameters given in previous section were used for these simulations.

4.5.1 Simulation Environment

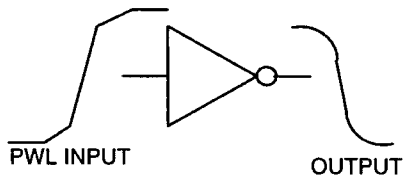
As discussed in section 4.3, a standard simulation environment must be selected so that the latch circuits experience the same loading at the inputs and outputs similar to that found in a VLSI circuits. A circuit consisting of a chain of six inverters was used to condition the input signal. The input signal to this circuit was a pulse with a rise time of 3 ns. The expected output was a smooth curve. The input conditioning circuit and the wave forms used are shown schematically in figure 4.6(a). Since the simulation of the long inverter chain was tedious and needed more simulation time, two simple circuits consisting of two inverters and a single inverter were also simulated with *piece-wise-linear* (PWL) inputs for comparison with the output of the inverter chain. The input conditioning circuits used for the simulations are shown in figure 4.6 (b) and (c).



(a) Six Inverter Chain



(b) Two Inverter and



(c) One Inverter Test Circuits

Figure 4.6 Input conditioning test circuits and the wave forms used for simulations

The simulation results plotted were compared and it was found from the output wave shape that the long inverter chain circuit can be replaced by the simple two inverter circuit. The single inverter circuit was found unsuitable since the wave shapes do not compare favourably.

Simulations were also carried out with the latch circuit driving a range of output loads for estimating a standard output loading. It was found from the simulation results that a simplified equivalent load capacitance C = 0.05 pF can be used in place of the gate loading representing the device driven by the latch.

4.5.2 Fault-free Simulations of D-Latches

Simulations of the D-latch circuits were carried out to determine their timing parameters. The latch and its simulation environment is shown in figure 4.7. It consists of two inverters and two transmission gates forming the latch and the inverters at the inputs are used for conditioning the PWL inputs at DATA and EN input terminals. An additional inverter was used to obtain EN' input for the latch. The D-latch circuits were simulated to determine the fault free timing parameters.

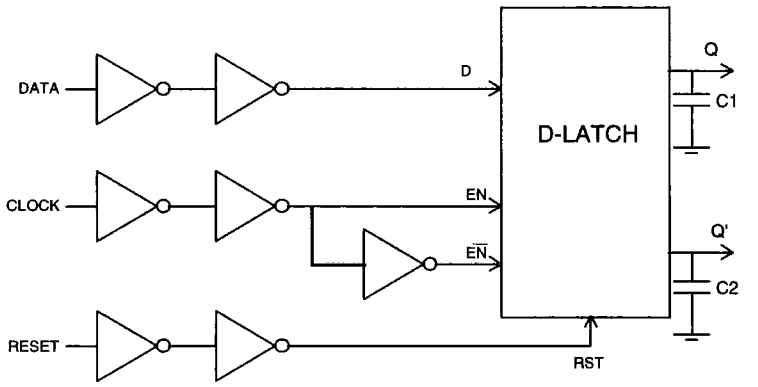


Figure 4.7 Simulation environment for the Latch

In this section, we discuss the characteristic timing parameters determined for one of the latch circuits (TX-NOR) using standardised SPICE parameters (technology EM/3):

(a) Determination of Rise and Fall Times

The rise and fall times at the output of the latch circuit were measured from circuit simulations.

Rise time, t_r = 5 ns
Fall time, t_f = 5 ns.

(b) Determination of Propagation Delays

t_{pLH} (D↑ Q↑) = 6 ns (EN=HIGH).
t_{pHL} (D↓ Q↓) = 6 ns (EN=HIGH).
t_{pLH} (EN↑ Q↑) = 6 ns (D=HIGH).
t_{pHL} (EN↑ Q↓) = 7 ns (D=LOW).

(c) Set-up Time Simulations

Set-up simulations were carried out for time intervals of 6.5 ns, 7.5 ns and 8.5 ns between Data edge and EN edge as shown in the plot and all the results were traced on a single graph with a uniform scale. The family of curves plotted is shown in figure 4.8.

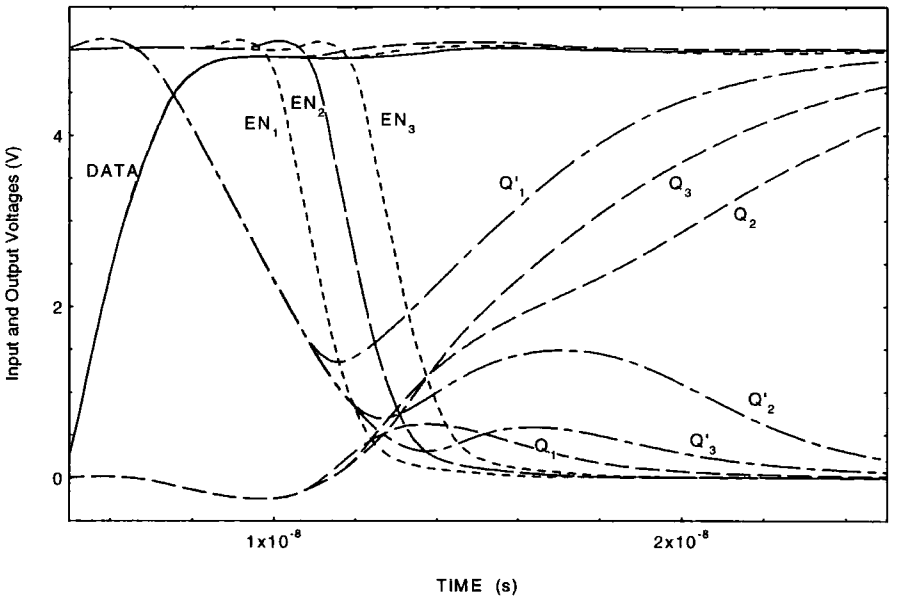


Figure 4.8 Family of curves: Set-up time simulations (Process: EC/3, Device: N/P 4/8)

The family of curves plotted in figure 4.7 reveals many interesting features. The Data D=1 is latched at the output for 7.5 ns, 8.5 ns and all time intervals greater than 8.5 ns; but it completely fails to latch at 6.5 ns prior to edge of clock (input EN_1 and output Q_1 as indicated in the graph). At 7.5 ns, the outputs Q_2 and Q'_2 have excessive time delays and it displays *metastable* operation [4.9]. At 8.5 ns the output Q_3 rises sharply to $\frac{1}{2}V_{DD}$ and has unacceptably long rise time between $\frac{1}{2}V_{DD}$ and V_{DD}. The correct latching takes place at a minimum time of 9 ns.

Set-up time, t_{su} = +9 ns.

Metastable state of the latch was simulated by adjusting the set-up time interval between 6.5 and 8.5 nano seconds. Metastability simulations are discussed in detail in chapter 6.

(d) Hold Time Simulations

The family of curves plotted for hold time simulations is given in figure 4.9. The minimum time at which data = 1 is latched with acceptable rise and fall times at the output nodes.

Hold time, t_h = +6 ns.

In this case we get a positive value for the hold time which means that the data must be held for this duration from the edge of the clock for reliable latching. It is also possible to have a negative hold time in some circuits. In many other latches and flip-flops, a positive hold time of 10 ns and above are common.

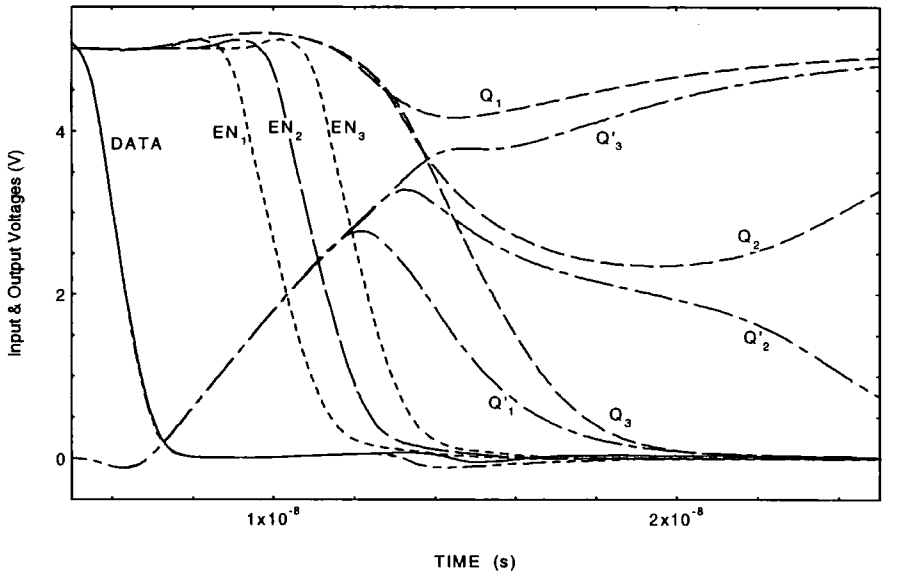


Figure 4.9 Family of curves: Hold time simulations (Process: EC/3, Device: N/P:4/8)

The plot for the hold time shown in figure 4.9 also displays metastable state of the latch due to hold time violations. Much longer rise and fall times for Q and Q' outputs are observed at the metastable state and this situation must be avoided for reliable operation

of the latch.

(e) Determination Pulse Duration

The pulse duration t_w for reliable operation of the latch was determined using a 50% duty cycle.

Pulse duration, $t_w = 9$ ns

$T_{min} = 2\ t_w = 18$ ns

$f_{max} = 1/T_{min} = 1/18$ ns

$= 55.5$ MHz.

4.6 Simulation Results and Selection of 3 Latch Circuits

D-Latch Circuits *										
Parameter	1 (a)	2 (b)	3 (d)	4 (c)	5 (f)	6 (i)	7 (e)	8 (g)	9 (h)	unit
t_r	5	6	4.5	5	4.8	5	5.2	5.3	4.9	ns
t_f	5	6	4.5	5	4.4	4.4	5	5	4.4	ns
t_{pLH}	6	6	5.5	5	3.4	3.8	8.1	5.5	6.4	ns
t_{pHL}	6.5	6.8	5.5	6.5	6.9	7	8.2	7.8	7.5	ns
t_{pRST}	6	7	5	5.5	6	6	8	5.5	7.2	ns
t_{su} [Q=1]	5	8	5	5	5	5	5	6	6	ns
t_{su} [Q=0]	5	8	5	5	6	6	5	6	6	ns
t_h [Q=1]	-1	-1	-0.5	0	-2	-2	-1	0	-1	ns
[Q=0]	-1	-1	-0.5	-0.5	-1	-1	-1	0	-1	ns
t_w	9	11.6	9	9	11	11	10	10	10	ns
f_{max}	55.5	43.1	55.5	55.5	45.5	45.5	50	50	50	MHz
t_c	4	7	4.5	4.8	4	4	4	6	5	ns
Transistors	10	12	10	12	20	22	9	12	8	
Contacts	37	38	40	32	49	51	40	34	36	
Silicon area	6650	6650	5950	5120	8550	8550	7150	5120	5950	μm

Table 4.5 Timing Parameters measured for the 9 D-Latch Circuits (Technology: EM/3, Device: N/P: 1/2.5) (* Key: D-Latch Circuits, 1: TX-NOR, 2: TX-NAND(V1), 3: TX-NAND(V2), 4: TRI-NOR, 5: NAND-N3(V1), 6: NAND-N3(V2), 7: INVL-TX, 8: MX-GATE, and 9: INVL-NPAS.

The Q and Q' outputs of the D-latch under normal operating conditions has similar rise and fall times of 5 ns each. This was achieved by designing the n- and p-transistor widths so that they have similar drive current irrespective of differences in other parameters such as mobility of carriers and threshold voltage. Since t_r and t_f are equal, we have achieved one of our design objectives for using CMOS, namely electrical symmetry.

The propagation delays are within acceptable limits or even better compared to similar devices available commercially. The output responds to the input signal without any glitch when EN is HIGH. The functionality test shows that the latch remains transparent to Data input when EN is HIGH and the Data can be latched at the output reliably if a valid Data is available before the edge of the clock. Data=1 as well as Data=0 can be latched at the output reliably. Set-up and hold times are also better than that specified for similar devices.

The latch going into metastable state was simulated and the Q and Q' outputs of the latch remain floating midway between the two logic states for an indefinite period. By understanding the conditions at which the latch enters its metastable state, we can incorporate improved designs by which this problem can be reduced or even eliminated. The circuit lay outs of each of the latches were also carried out using *CHIPWISE* VLSI design tools. The lay outs were used to estimate the number of transistors used, the total number of contacts per design and the net silicon area used for the design.

Additional simulations were carried out for each circuit and the metastable hardness of the circuits were determined (these are discussed further in chapter 6). The critical window within which the latch entered the metastable state was also determined. A comparative study of all the performance characteristics were carried out and are tabulated in table 4.5.

4.6.1 Analysis of the Simulation Results

The designs of D-latch circuits using commercial CMOS technology rules have been successfully completed. The simulations of the latches using standardised input and output loads were carried out and the results were plotted. The designs were found to be reliable and the performance characteristics measured using simulation results were found to be comparable to or even better than that for latch circuits made using gate array technology.

The rise and fall times for each of the latch circuits designed using technology EM/3 was found to be same and this was one of the design objective. The rise and fall times varied between 4.5 ns to 6 ns. The propagation delays, set-up and hold times and the maximum operating frequency were found to differ for the nine latch circuits. It will be shown in the next section that the circuit delays can be reduced for submicron designs by using minimum size devices and by selecting layout symmetry as opposed to signal symmetry.

All the nine latch circuits were simulated for metastable hardness and the critical window for each was determined. The comparative performance study carried out using identical test conditions allowed us to select the ones with better parameters and utilising less silicon area. We have retained 3 of the circuits (circuits c, d and f shown in figure 4.1) for further simulations and are carried out in the next section using 1 micron and 0.7 micron design rules. These selected circuits had relatively better performance and were unique designs.

4.6.2 Fault Free Simulations of Submicron Latch Circuits

At this stage, 1 micron design rules using technology EC/13 were made available for simulations of the latch circuits. Three of the selected latch circuits were simulated using an optimised set of device parameters and a comparative study of the performance characteristics measured for the three latches was carried out. The table 4.6 summarises the simulation results.

Parameter	TRI-NOR	NAND-N3	TX-NAND	UNIT
t_r	1.37	1.30	1.22	ns
t_f	0.98	0.86	0.92	ns
t_{pLH}	1.5	1.25	1.75	ns
t_{pHL}	1.75	1.75	2.0	ns
t_{su}	1.25	1.25	1.5	ns
t_h	0.0	0.5	0.25	ns
T_{min}	5	5.0	6.0	ns
f_{max}	200	200	167	MHz
t_c	1.75	1.75	1.75	ns

Table 4.6 Timing parameters measured for the 1 micron design (Technology: EC/13, Device: N/P:1/2)

The t_{pLH} and t_{pHL} values tabulated are the average values obtained for Data and EN inputs. From the table it is clear that the latch circuits designed using 1 micron devices are much faster than the 3 micron designs.

4.6.3 Simulation results for 0.7 Micron Design

The three selected latch circuits were also simulated using 0.7 micron device technology (EC/6 & EC/3) and the simulation results were used to determine t_r, t_f, t_{su} and t_h; t_{pd} is the average of the two propagation delays. These are tabulated below in table 4.7.

Parameter	TRI-NOR	NAND-N3	TX-NAND	UNIT
t_r	2.21	1.18	1.25	ns
t_f	0.94	0.80	0.67	ns
t_{pd}	1.88	1.32	1.54	ns
t_{su}	1.19	1.62	0.92	ns
t_h	0.0	-0.50	0.0	ns
T_{min}	5.5	4.5	4.0	ns
f_{max}	182	222	250	MHz
t_c	1.19	1.12	0.92	ns

Table 4.7 Timing parameters measured for the 0.7 micron design (Technology: EC/3, Device: N/P:1/1, minimum size devices used in all gates)

4.7 Chapter Summary

We have discussed the design and selection of the latch circuits for studying the degradation effects which will be discussed in the next chapter. The logic devices used in the circuits were optimised for peak performance under normal conditions. The timing parameters for the transparent latch circuits were identified for further analysis. The input and output loading effects were analysed and standardised for emulating a VLSI environment. The SPICE device model parameters used for the simulations were optimised using characterisation techniques. The optimised SPICE model parameters

were used to analyse the simulation results and have selected best three circuits for degradation simulations. The 1 micron and the 0.7 micron devices were found to be faster and it is expected that these submicron devices will degrade faster and hence will have a larger effect on the wearout processes discussed in chapter 2. All degradation simulations will be carried out using the optimised SPICE device parameters discussed in this chapter.

In the next chapter, stress simulations will be carried out for the selected latch circuits. The latch circuits will be simulated with device parameters degraded based on stress levels measured using a stress model and the corresponding timing degradations of the latch measured and compared with that measured for the fault free simulations. Metastability simulations and hot-carrier degradation simulations on the selected transparent latch circuits are discussed in the next two chapters to prove that the timing parameters will be adversely affected by these wearout processes giving rise to increased resolving time and circuit failure.

Chapter 5

Hot-Carrier Degradation Simulations of CMOS Bistable Circuits

Hot-carriers have been identified as a significant problem in the operation of CMOS bistable circuits. Dynamic operation of a bistable circuit will give rise to varying stress levels on the transistors leading to non-uniform degradation levels. The modelling of the substrate current in CMOS devices as a monitor of device degradation has been discussed in chapter 3 and we discussed the design and optimisation of the CMOS bistable circuits selected for hot-carrier degradation analysis in chapter 4.

In this chapter we describe the techniques which we have used to evaluate the relative and absolute stress levels experienced by the transistors in a number of bistable circuits. The stress on each device is translated into parametric shift in transistors and from this the effect on circuit timing parameters has been evaluated. The degradation of device parameters is used to predict device life-time and hence the projected life expectancy of the bistable circuits. It has been reported [5.1] that the degradation rate of nMOS transistors during dynamic operation was found to be more severe than the degradation rate during static operation. The enhanced degradation has been attributed to the alternating hot-electron and hot-hole injections into the gate oxide during dynamic stress and the generation of interface states [5.2], [5.3]. Consequently we have investigated the dynamic stress experienced by devices under normal operating conditions. The three latch circuits selected based on fault free simulations performed as discussed in chapter 4 will be used for degradation simulations in this chapter.

The method used to evaluate the stress on each transistor involves calculating the substrate current for each device in the latch circuit. This is generally accepted as a reliable means of monitoring hot-carrier stress in transistors and is preferred to gate current monitoring due to the magnitudes of the currents involved. The substrate current model developed in chapter 2 was used as a direct monitor of stress on each of the devices in the circuit. The stress on each device was translated into device parameter shifts using a degradation model which is described in chapter 3. Parameter shifts were then incorporated into device models for subsequent resimulation of the bistable circuits

and the effect of transistor degradation on circuit performance is discussed in this chapter.

5.1 Modelling degradation effects in bistables

The three D-type latch circuits selected for degradation simulations were re-designed using a 0.7 μm technology so that all the devices used in the circuits conformed to the technology design rules and had the minimum dimensions allowed. In this design, we have opted for geometric symmetry as opposed to signal (pull-up and pull-down delays) symmetry. As we are using submicron devices in the design, we expect the mobilities of charge carriers in nMOS and pMOS devices to be comparable due to velocity saturation [5.4].

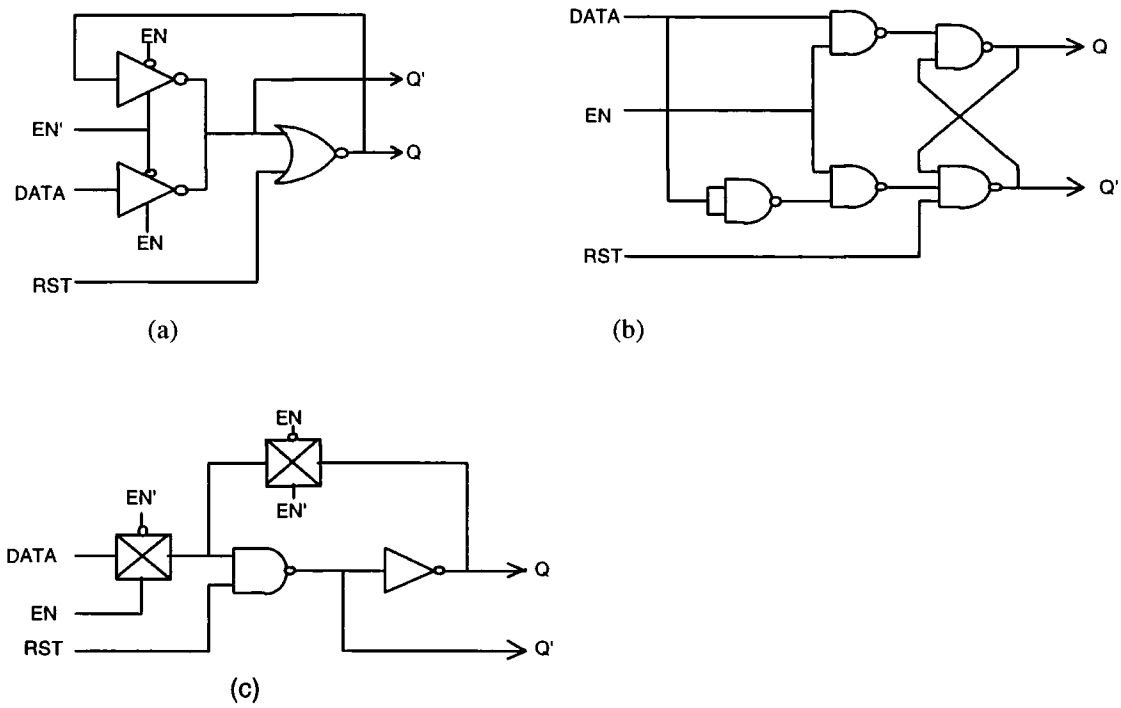
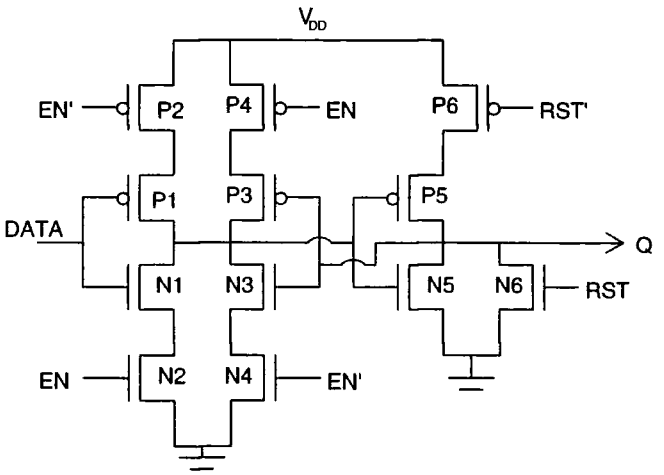
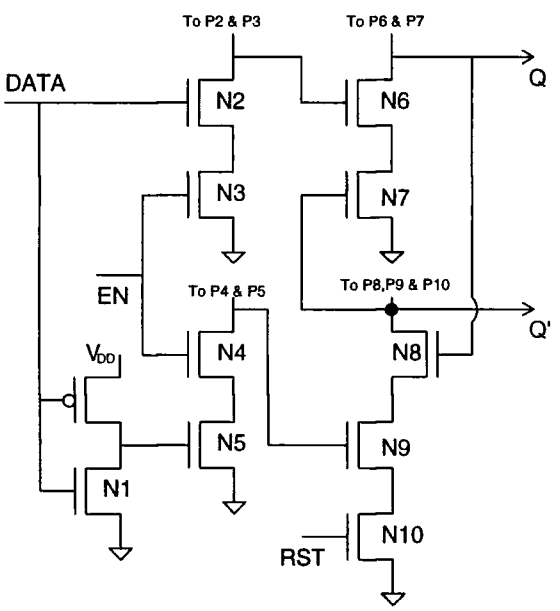


Figure 5.1 The three bistable circuits selected for stress simulations

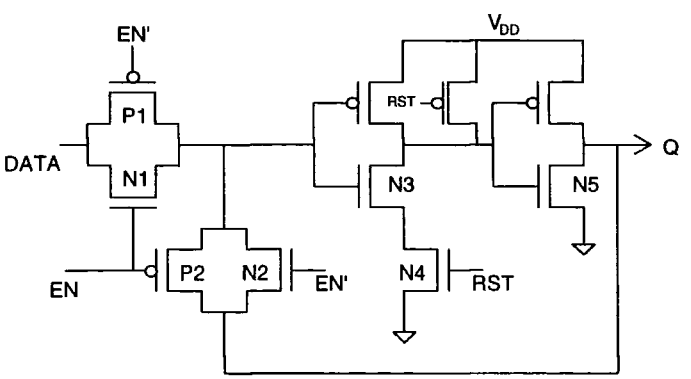
Minimum sized devices permitted by the design are used and so the device width and length are approximately same. This provides an added advantage of reduced nodal capacitances and hence faster rise and fall times. Gate level and transistor level circuits for the latch circuits are given in figures 5.1 and 5.2 respectively. A list of all device dimensions used in the circuit designs are given in appendix E. Unlike the stress models developed for devices operated under steady state conditions, the stress on each device in a latch circuit will be depedant on the circuit complexity, changing voltage and current and the duty cycle.



(a)



(b)



(c)

Figure 5.2 Transistor level circuits for the three bistable circuits

The procedure devised to evaluate the stress effects on the circuits is as follows:- The wave- form used to simulate the stress effects must represent a realistic cycle of operation which will stress all the devices in the circuit for varying periods. Hence the degradation levels on each device must be based on the stress levels of this simulation period. Average stress levels for each of the devices were then evaluated over the whole simulation period. All the characteristic timing parameters for the latch were measured from SPICE simulations as defined in chapter 4. The average stress values were translated into device parameter shifts using the degradation model. The parameter shifts were then incorporated into device models used for SPICE simulations and the circuits were resimulated using the same simulation cycle as used for the fault free simulations. A new set of stress values were established for this period and the corresponding circuit timing parameters were measured and were compared with that determined for fault free simulations. A block diagram representing the degradation simulation cycle for the latch circuits is given in figure 5.3.

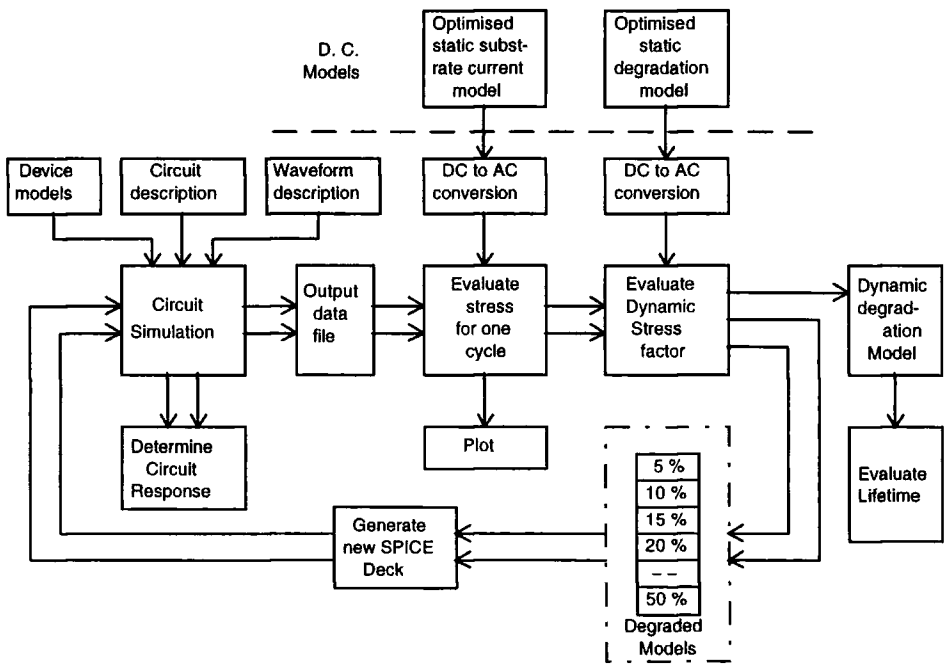


Fig 5.3 Hot-carrier degradation simulation cycle for bistable circuits

Once the average stress and degradation levels have been evaluated, these are used to establish the predicted life time of the circuit. Life time of the circuit will be predicted by two techniques (i) using the the average stress values on all the devices in a circuit and (ii) stressing just one or two of the identified critical devices and then measuring the degradation in circuit performance. We may also consider only the

average stress on the devices having a preselected threshold value of stress known to generate degradation levels within a realistic life time of the whole circuit. Techniques employed to improve life-time are discussed in chapter 7.

5.2 Relative effects of stress on each device in the latch circuits

In order to determine the relative effects of stress on each device in a latch circuit, the devices were degraded equally and the timing parameters were determined by circuit simulation. This step was necessary to characterise the effects of degradation of the devices on the overall timing parameters of the latches. Once we have established the degradation effects on the latch circuit for uniform degradation, the circuits were simulated again by degrading the device parameters proportional to stress levels which was determined from fault-free simulations performed as discussed in chapter 4. Using a standard stimulus, the first circuit DL1 was simulated with a set of optimised SPICE device models and output data was generated. This stored data file contained the drain current I_D, drain-source voltage V_{DS} and gate-source voltage V_{GS} for the whole cycle, arranged in a structured array form for input to a MATHCAD post processor. Using the optimised static substrate current model and employing quasi-static analysis, the substrate currents and the stress factors for each of the data points were calculated for the devices using the post processor. Quasi-static analysis was employed to convert dynamic stress levels into equivalent static values by sampling the nodal voltages and currents at regular intervals and converting this to stress factor using the post processor, which was then summed over the whole cycle. The stress factors and the life-times calculated for all devices in the three latch circuits over one simulation cycle are tabulated in table 5.1. A listing of the MATHCAD program for modelling the substrate current and evaluating life-time is given in appendix F.

It can be seen from table 5.1 that the stress levels on the devices in the three latch circuits have a wide range, device N2 of circuit DL1 has a very low stress where as the device N5 and N6 have the highest stress. The currents through devices N1 and N2 (identical transistors connected in series) in circuit DL1 are the same but the stress levels calculated over the simulation cycle are quite different. Similar results are obtained for devices N3 and N4 in circuit DL1, N2 and N3, N4 and N5, N6 and N7 as well as N8 and N10 in circuit DL2 and also for N3 and N4 in circuit DL3. This shows that the stress on devices in a complex circuit depend also on nodal voltages which are continuously changing under dynamic operation and can differ substantially.

	Stress Factor (A/m)			Life-Time (Hours)		
DEVICE	DL1	DL2	DL3	DL1	DL2	DL3
N1	5.4	7.7	5.5	1.7×10^5	5.2×10^3	3.8×10^4
N2	0.1	6.5	1.5	1.0×10^{10}	1.8×10^4	2.6×10^5
N3	9.9	0.7	8.7	1.2×10^3	1.3×10^7	3.1×10^4
N4	0.4	7.2	0.5	1.4×10^7	1.4×10^4	1.9×10^8
N5	21.1	0.8	10.6	2.1×10^3	8.4×10^6	5.5×10^3
N6	21.1	6.0		2.1×10^3	9.1×10^4	
N7		0.4			2.5×10^8	
N8		13.0			1.4×10^4	
N9		1.1			1.7×10^7	
N10		0.7			8.5×10^7	

Table 5.1 Stress factors and Life-time for all nMOS devices in the three latch circuits.

A graphical output was generated for each of the devices with substrate current plotted over the period of the simulation. A cross check of the graphic output was made with that for drain current plotted by the MATHCAD processor and that plotted by the PSPICE *PROBE* plot. This is necessary to confirm that the substrate current generated is in accordance with the model developed and that the peak of the substrate current coincides with the point when the gate current is approximately half the drain voltage for that part of the simulation. We analyse the effect of stress on devices in each of the three latch circuits next.

5.2.1 Effect of stress on Latch DL1

Figure 5.4 shows the drain current and the substrate current plotted using the substrate current model as a function of simulation period for one of the device in the circuit. From the evaluated stress for one cycle and using the optimised static degradation models, the average dynamic stress factor for each of the devices in the circuit was evaluated. A histogram representing the stress factors for each of the devices in the latch circuit DL1 is shown in figure 5.5.

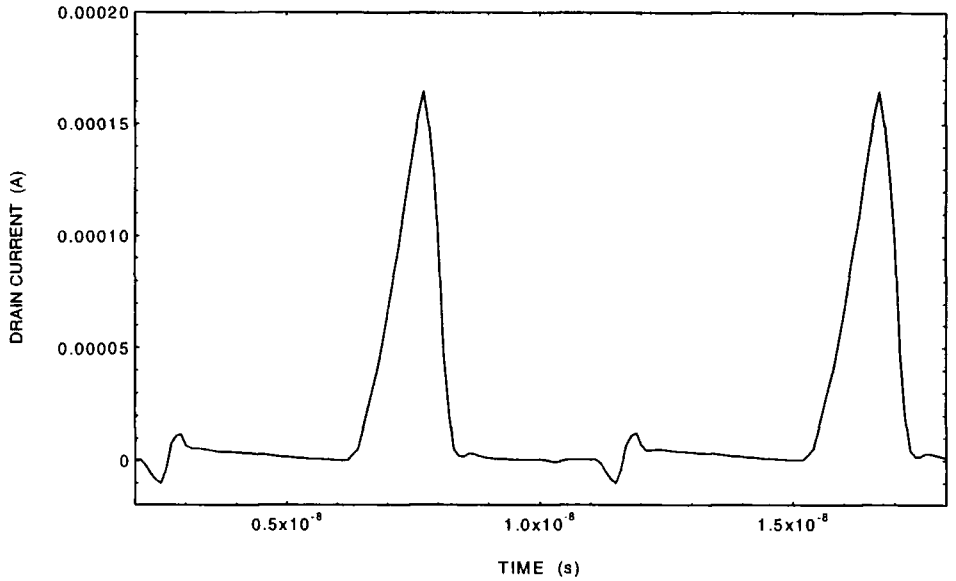


Figure 5.4 (a) Drain current for devive N5 of DL1 during the simulation cycle (Process EC/3, Device 1/0.8)

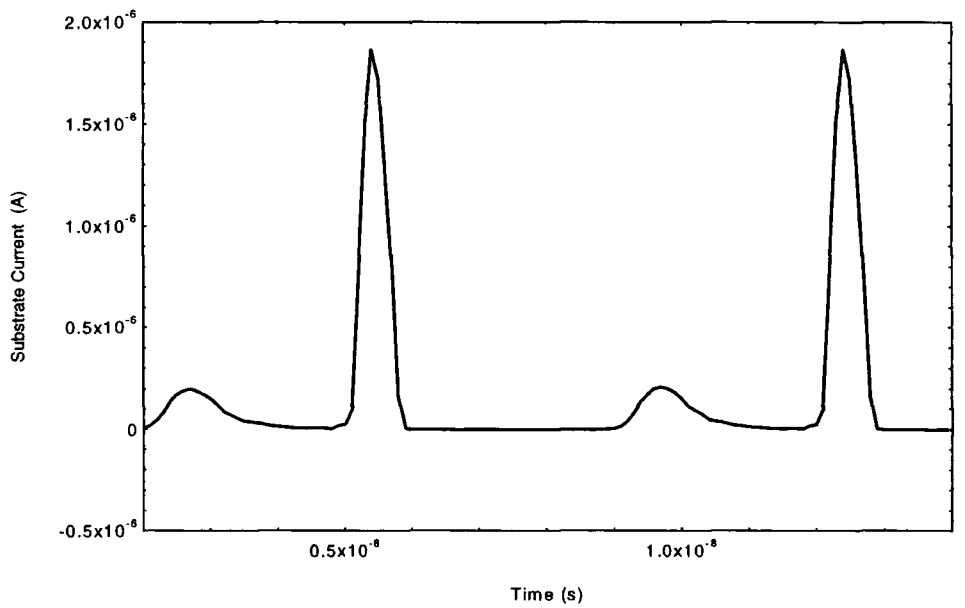


Figure 5.4(b) Substrate Current for N5 of DL1 during the same simulation period plotted using the Substrate Current Model (Process EC/3, Device 1/0.8)

It can be seen from the histogram in figure 5.5 that the devices N5 and N6 suffer the highest stress during one typical cycle of operation of the latch and the devices N2 and N4 has the least stress. This information will be made use of when considering steps to reduce the stress on critical devices in a latch circuit. The substrate current model has

been employed successfully to show that the stress levels are not the same on all devices in a latch and has revealed those having higher stress than normal. The next step will be to evaluate how the stress levels in devices translates into timing degradations in the latch circuits.

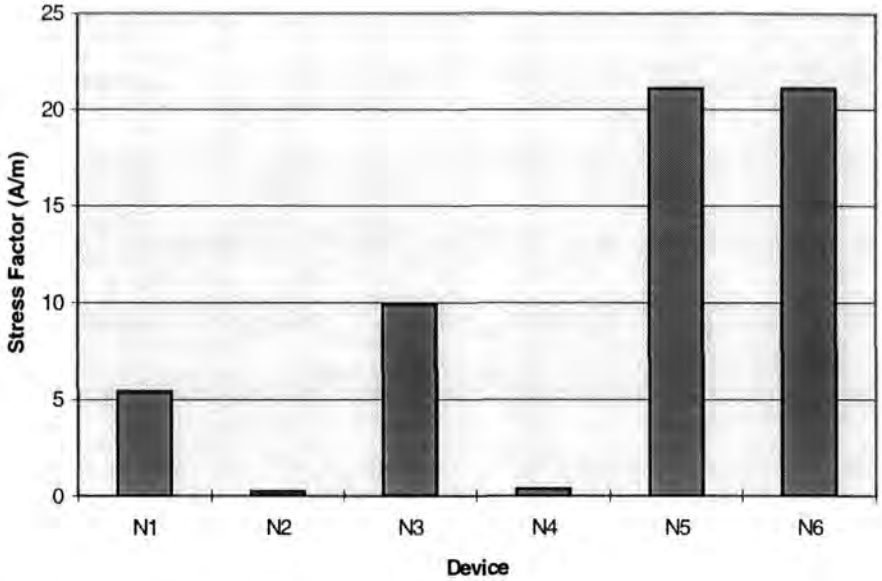


Figure 5.5 Histogram showing the stress on each device of DL1

5.2.2 Effect of stress on Latch DL2

The transistor level circuit for DL2 shown in figure 5.2(b) illustrates the positions of the nMOS devices having higher stress than average. Stress levels are measured using normalised substrate currents evaluated over the simulation period and we have used a sliding scale for converting stress levels into degradation in device parameters which will be fully explained in the next section. A stress factor (over one cycle) of 7.5 A/m is taken as a normal stress on a device. The average stress level of 7.5 A/m was calculated by taking the average stress on all devices in the latch circuits. A device having a stress factor less than this will be ideally stressed and a factor more than 10 A/m will be considered to be highly stressed. Using the same sliding scale, we can define severely stressed devices also. The stress levels for all nMOS devices in latch DL2 are shown in figure 5.6.

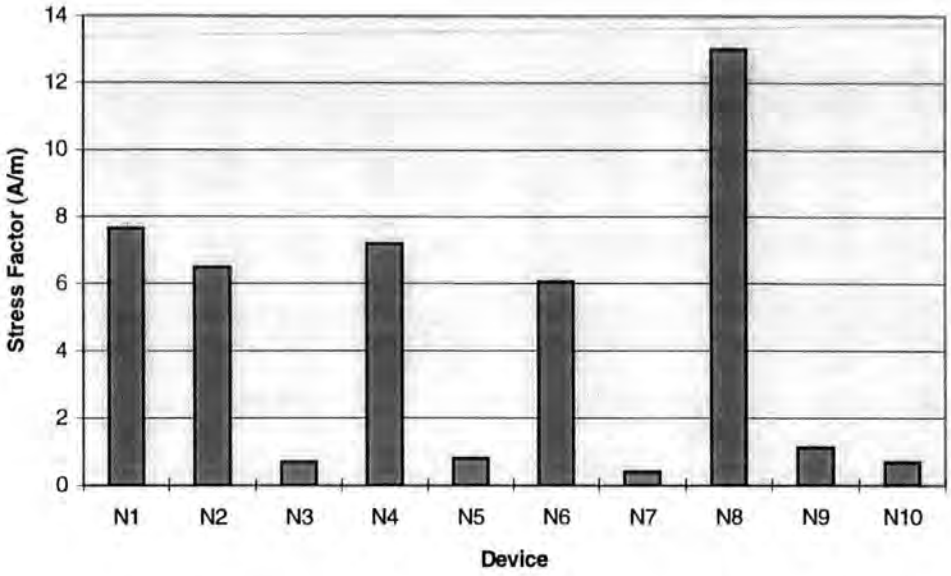


Figure 5.6 The stress levels on the n- devices in latch DL2.

It can be seen from figure 5.6 that we have an almost ideal latch with stress levels well below the normal value for all the devices except for one which has a stress value more than normal. The average stress level for the latch was found to be 4.8 A/m. If we can reduce the stress on the device N8 to an acceptable value, this latch can be a typical latch design having improved reliability. We have noticed from the bar graph in figure 5.6 that devices N1, N2, N4 and N6 have close to normal stress and the device N8 has higher stress level. All these devices are at the top of the ladder forming series connected nMOS devices and the drains of all these devices are connected to the output node of the respective NAND gates. N3, N5, N7, N9 and N10 have stress levels very much less than normal and we notice that these are the devices forming the lower positions in the ladder net work of nMOS devices. It is clear that the position of a device and the connection of the drain, source and gate nodes have an important bearing on the stress levels and hence how these devices generate hot-carriers and degrade. We will apply this findings in chapter 7 for reducing the stress on some of the devices and hence improve the reliability of the latch.

5.2.3 Effect of stress on Latch DL3

The third latch circuit contains the smallest number of devices and the stress simulation results are shown in figure 5.7. The device N5 has a higher value of stress compared to other devices in the circuit and the average stress value for the circuit is 6.6. As the N5 drain is connected to one of the outputs and is also a node connected to

the feed back loop, it is much more critical than other devices. This device also has its source connected to ground and so will have the full voltage swing occurring across its drain-source terminals during switch ON/OFF giving rise to all the hot-carrier degradation modes.

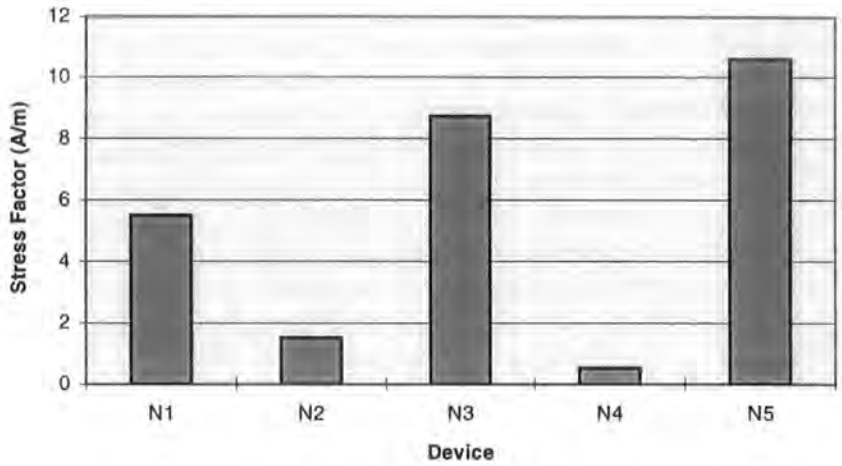


Figure 5.7 The stress levels on the devices in DL3.

The average stress value for this circuit is less than that for DL1 and we expect the latch to degrade less than DL1. The device N3 also has a higher stress level and we notice that its drain is connected to the output node of the NAND gate and is the output node Q' for the latch. Device N4 has the least stress as it forms the lower end of the ladder. The techniques to reduce the stress levels on N5 and N3 will be considered in chapter 7 so as to improve the reliability of this circuit.

5.3 Degradation Simulations

At this stage it is possible to determine the dynamic degradation over a cycle of operation and the projected life time of the devices using the substrate current model as all known hot-carrier effects are accounted for in this model. Degraded SPICE device models were generated based on the dynamic stress factors and these degraded models were used to re simulate the circuit. The degraded circuit response was measured and compared with the circuit response without degradation. Additional plots were generated from the simulations showing the degradation effects on circuit currents and nodal voltages. Using these plots, the effects of degradation on timing parameters for the latch circuits were determined.

5.3.1 AC. Degradation Model

The dynamic simulation results were used to determine the dynamic stress factor by employing the static degradation model. The substrate current generated was summed over the whole cycle and normalised to obtain the ac. stress factor. The simulation period was converted into an equivalent dc. stress time by quasi-static analysis. The stress factor is evaluated using the following equations:

AC. Stress Factor, $S_{ac} = \frac{\Sigma I_{sub}}{W}$ --- (5.1)

Normalised ac. Stress Factor, $S'_{ac} = \frac{\Sigma I_{sub}}{\Sigma I_D W}$ --- (5.2)

Simulation period = 20 ns

Effective ac. cycle period (assume 50% duty cycle) = 10 ns

Using quasi-static analysis, the effective stress period for each device was evaluated as 5 ns, which is 25% of the simulation period. This was an approximation, but it was found to be an acceptable value by estimating the *on time* for the nMOS devices using the drain current plotted in figure 5.3. Some of the devices may remain *on* for longer and some others for a shorter period. The simulation steps selected were such that all devices go through a similar sequence of *on* and *off* periods in order to keep the summation as simple as possible. Any slight variation from this fixed period will not adversely affect the overall results of the analysis.

5.3.2 Characterisation of Degradation Effects under AC. Stress

When a latch is operated under dynamic conditions, the devices are under stress for only 25% of the simulation time. A CMOS inverter with minimum size n- and p-devices was simulated using standard device parameters and also with degraded device parameters. The peak drain currents for the two simulations were measured. As the devices are in saturation, the saturation drain current degradation was evaluated at the peak level.

Peak saturation drain current for standard simulation = 312 μA
Peak saturation drain current for 20% degraded device = 269 μA
Degradation in drain current for 20% degraded device = 43 μA
Percentage degradation in drain current for 20% device degradation = 14%

It was established from static degradation characterisation simulation and experiments,

[5.5] discussed in chapter 3, that a 20% degradation in device parameter is equivalent to a static stress period of 1110 hours under peak stress conditions. Under dynamic stress conditions, this translates into 4440 hours of ac. stress and will produce a 14% degradation in drain current.

The life time of a device is defined using a 10% degradation level in saturation drain current and the dynamic stress time for this event was evaluated as 3000 hours. We expect that the first latch DL1 having highest stress levels on devices will degrade and fail if we define end of life as 10% degradation in drain current. This stress period will be kept constant for all latch circuits and the effects of degradation on timing parameters for the latches will be measured in the next section.

The normalised ac. stress factors were used to degrade each of the devices to its equivalent degradation as shown in the degradation simulation cycle in figure 5.3. The average stress factor $S = \sum I_{sub}/W$ was evaluated for a simulation period where the width W for all the devices were 1 micro meter. The average stress factors calculated for the three latch circuits were 7.38 A/m, 4.80 A/m and 6.59 A/m respectively and are shown in the bar chart of figure 5.8.

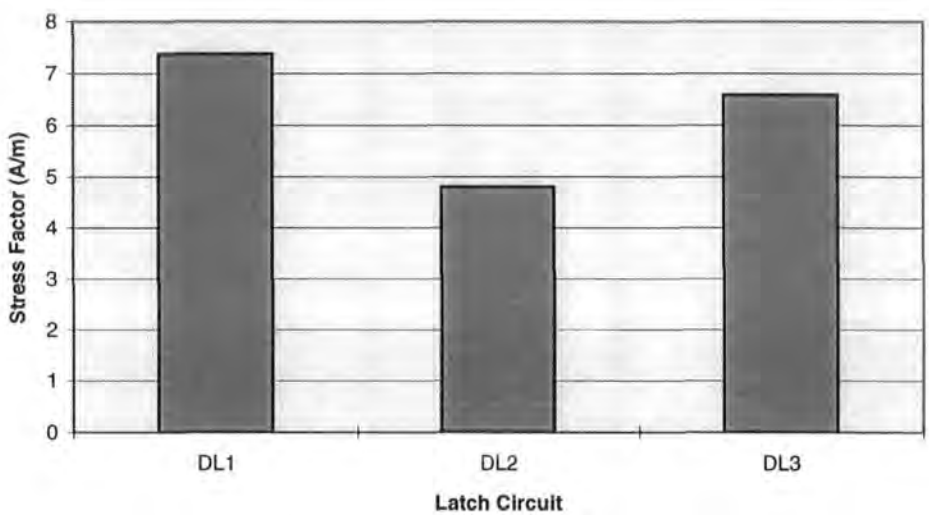


Figure 5.8 Average Stress factor S for the three latches over one simulation period

Using a sliding scale, shown in table 5.2, the stress factors for each device in the latch circuits were converted to device degradation. Degraded device SPICE parameters were generated for each of the devices from the stress factors given in table 5.1.

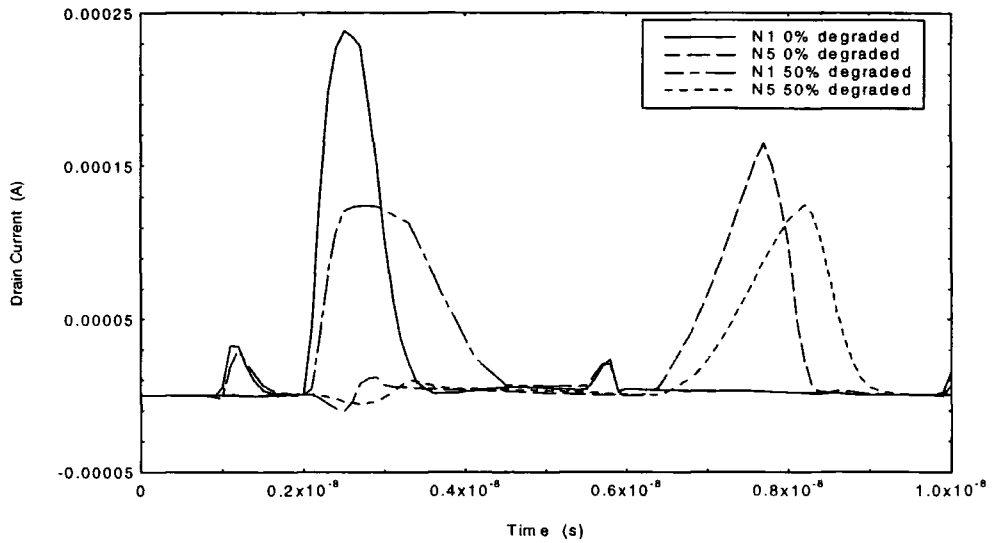
Stress Factor (A/m)	Device Degradation (%)
0 - 0.5	0
0.5 - 2.5	5
2.5 - 5	10
5 - 10	20
10 - 15	30
15 - 20	40
20 - 25	50

Table 5.2 Conversion scale for Stress factor to Degradation

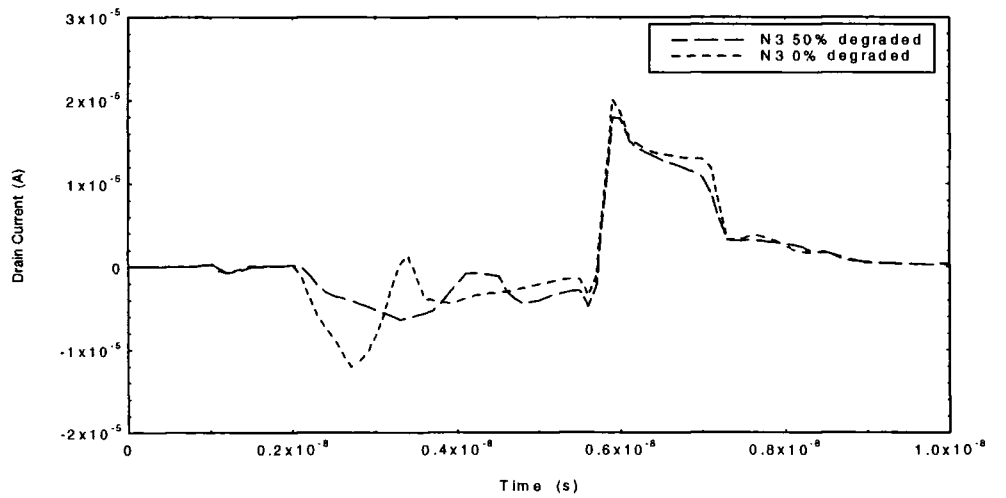
The effects of degradation for the three latch circuits were determined using more simulations with the degraded SPICE models which are now discussed.

5.3.3 Effects of Uniform Degradation of all Devices in the Latch

The effects of degradations on the latch circuits were characterised by simulating each circuit with uniform degradations (all devices degraded by the same level) of 10%, 20%, 30%, 40% and 50% degradations respectively. We have used identified device SPICE model parameters to model the degradation effects as discussed in chapter 3. The simulation results were studied with that for the virgin circuits. This procedure will provide us vital information on the susceptibility to degradation of each device in a latch. The most noticeable effect of degradation is in the drain current of a device and so plots were generated for the drain currents of each of the devices in the latch. Figure 5.9(a) is a graph showing the drain current plotted for devices N1 and N5 and figure 5.9(b) is that for device N3 of the latch DL1 before and after degradation.



(a)



(b)

Figure 5.9 Drain currents with and without degradation in latch DL1 for (a) Devices N1 and N5 and for (b) Device N3 (Process EC/3, Device 1/0.8).

The stress factors measured using the substrate current model indicated that devices N2 and N4 had stress levels very much less than the normal stress level and so these will degrade at a much slower rate than other devices. Since N2 is in series with N1 and N4 is in series with N3, the drain currents are the same as plotted in figure 5.9 for devices N1 and N3 respectively. The drain current for N6 will be the same as that for N5. The deterioration in drain currents for N1 and N5 are clearly visible in the plots, but for N3 we have very little change in the drain current. This indicates that even though N3 has a higher stress level than the average stress value, it will not have a marked effect on the timing parameters for this latch since it is along the feedback path. The

peak current for N1 has dropped by 50% and that for N5 has dropped by 25% as a result of degradation in device parameters due to hot-carriers. We also notice that the position of the peak currents have been shifted along the time axis indicating an increased propagation delay which is markedly more for N5. The spreading of the drain current means that the devices remain switched on for a longer period giving rise to an overall increase in power dissipation, even though the peak current has been reduced due to the degradation effect.

A similar analysis has been carried out for the other latch circuits and the effects are summarised at the end of this chapter.

5.3.4 Effect of degradation on rise and fall time

The rise time and fall time of the latch were measured at the output node Q with the help of a rising and falling impulse at the inputs. As discussed in chapter 3, we are only considering the degradation in the rise and fall times as a result of device parameter deterioration of the nMOS transistors due to hot-carriers and have not included any of the hot-carrier effects on the pMOS transistors. As the pMOS load transistors are responsible for the rise time, we did not expect any appreciable deterioration in this parameter. Two types of degradation measurements were taken, first by uniform degradation of all devices in a latch for characterisation of the degradation effect and then by degrading the devices proportional to stress.

(a) Uniform degradation of all devices in the circuit

The simulations were carried out using uniform degradations of 10%, 20%, --, 50% and the corresponding timing degradations were measured. The plot of rise time versus percentage degradation in device parameter shown in figure 5.8 indicates that the increase in rise time is very small and may be attributed to the propagation of a small delayed response from the previous stage due to an increase in fall time and the corresponding propagation delays. The rise times increased by 4.5%, 2.5% and 12% for the latch circuits DL1, DL2 and DL3 respectively for a degradation of 50%. The larger than normal increase in rise time for the circuit DL3 shown in figure 5.10 is due to a higher stress level for the nMOS device N3 transmitting this delay to the gate of the out put device. In the other two circuits, the devices responsible for propagating the signal to the gate of the output devices are not excessively stressed. Latch DL2 has the smallest increase in rise time.

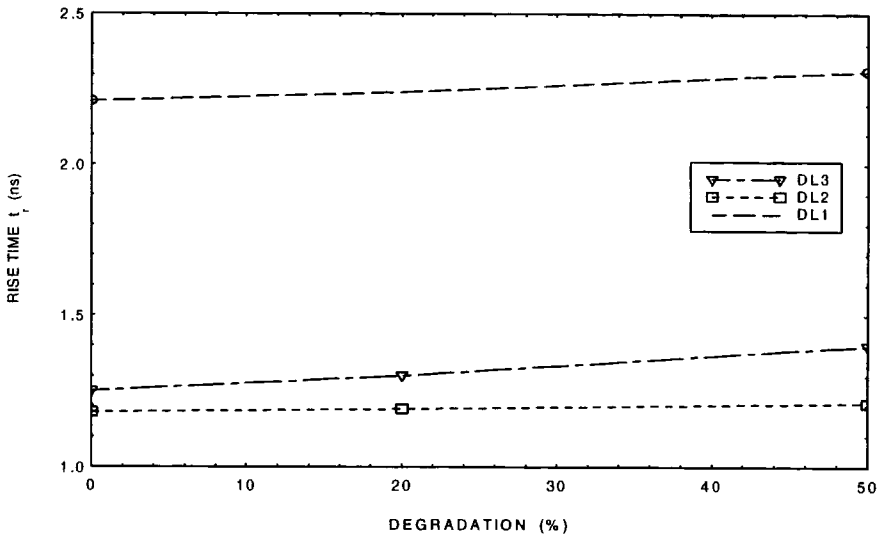


Figure 5.10 Rise Time as a function of Degradation for the three latch circuits
(Process EC/3, Device 1/0.8)

The fall time is due to the nMOS devices pulling the output low and the deterioration in device parameters due to hot-carriers has a marked effect on this timing parameter. A plot of the fall time versus degradation of device parameters for the three latch circuits are shown in figure 5.10. It is clear that the fall times have been affected to varying degrees for the three circuits, 25.5%, 63.8% and 34.3% for DL1, DL2 and DL3 respectively. The steeper increase in fall time for DL2, shown in figure 5.9, is due to the nMOS devices connected in series for the NAND gates at the outputs affecting the fall time twice as much as that for the other circuits.

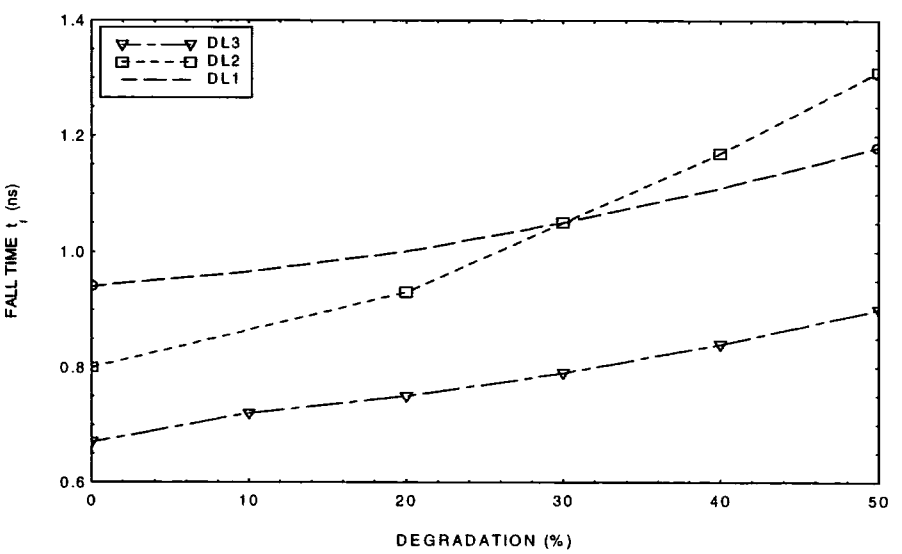


Figure 5.10 Fall Time as a function of Degradation for the three latch circuits
(Process: EC/3, Device: 1/0.8)

(b) Effects of degradation proportional to stress on each device

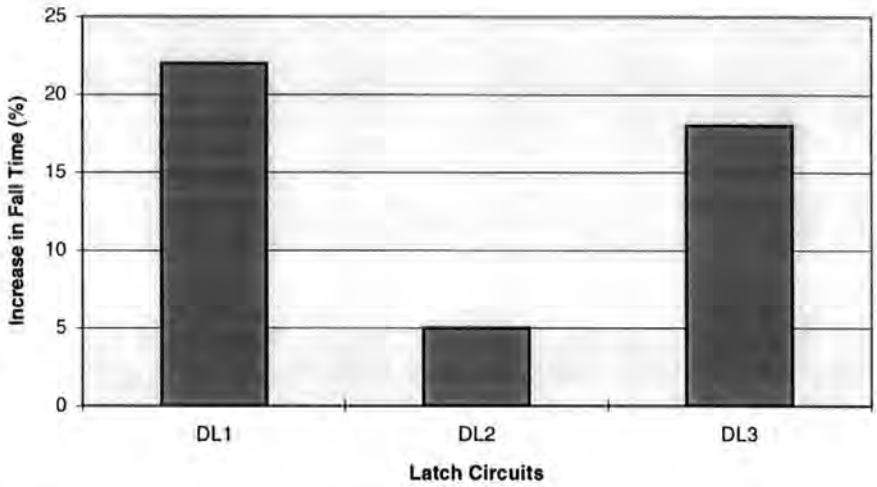


Figure 5.11 Increase in Fall Time for the three latch circuits

We have used substrate current as a monitor for stress and was shown in chapter 3 that the degradation rate is proportional to stress. The stress period for all the bistable circuits were fixed as 3000 hours and the circuits were now simulated with device degradations introduced proportional to the stress levels measured from the fault free simulations. The rise time and the fall time for the three circuits were once again measured and compared with that measured for degradation free and that for the uniform degradation. The changes in the rise times for the three circuits were negligible as expected; 1% for DL1, 0% for DL2 and 1.6% for DL3. The fall times have been increased due to the degradations and the increase in fall times for the three circuits are shown in the bar graph of figure 5.11.

The increase in the fall time for DL1 is found to be more than that for other two and DL2 had the least. The fall times for the three circuits have been increased by 22%, 5% and 18% respectively during the same degradation period. The bistable circuit DL2 had the least stress level and hence had least degradation, which resulted in a small increase in fall time compared to the other circuits.

5.3.5 Effects of degradation on propagation delays

The propagation delays from D(ata) input to Q output measured were the low to high propagation delay t_{pLH} and the high to low propagation delay t_{pHL}. The propagation

delays were determined by simulating the circuits with uniform degradation and with degradation proportional to stress. The two propagation delays are affected by the degradation in rise and fall times of the devices in the latch circuits and so we have evaluated the degradation in the average propagation delay.

(a) Effects of propagation delay with uniform degradation

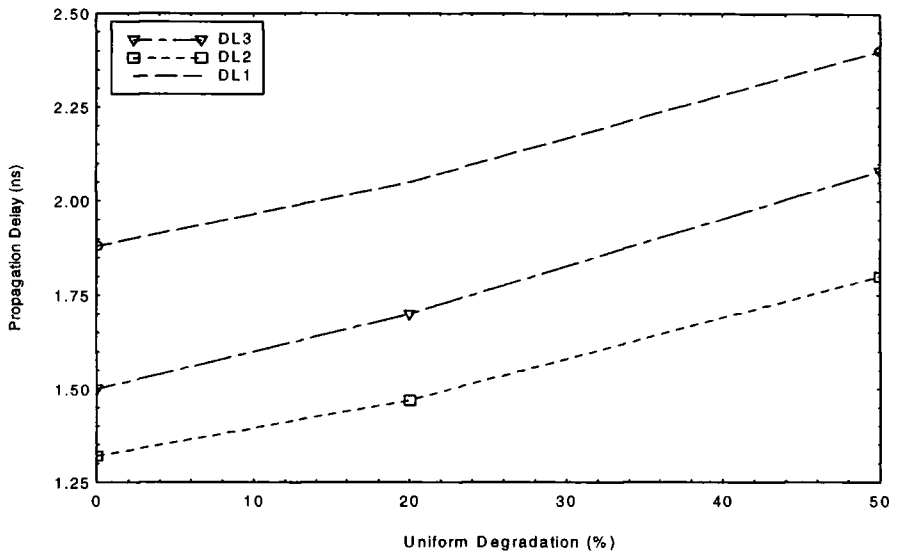


Figure 5.12 Propagation Delay Vs Degradation for the latch circuits
(Process: EC/3, Device: 1/0.8).

Since the average propagation delay t_{pd} for the latch circuits are plotted against the percent degradation in figure 5.12 for the three circuits with uniform degradation. The average increase in propagation time was found to be about 7% for every 10% degradation in device parameters for all the three circuits. No abnormal increase in t_{pLH} or t_{pHL} was found for any one of the circuits.

(b) Effects of degradation proportional to stress

The three circuits responded differently when subjected to degradation proportional to the stress. From the bar chart in figure 5.13, it can be seen that DL1 has the highest increase in propagation delay as it had experienced maximum stress level. The stress levels on the devices in the latch circuit DL1 was the highest and so it has the maximum increase in propagation delay; the devices in circuit DL2 experienced lowest stress compared to other circuits and has the least increase in propagation delay as shown in figure 5.13.

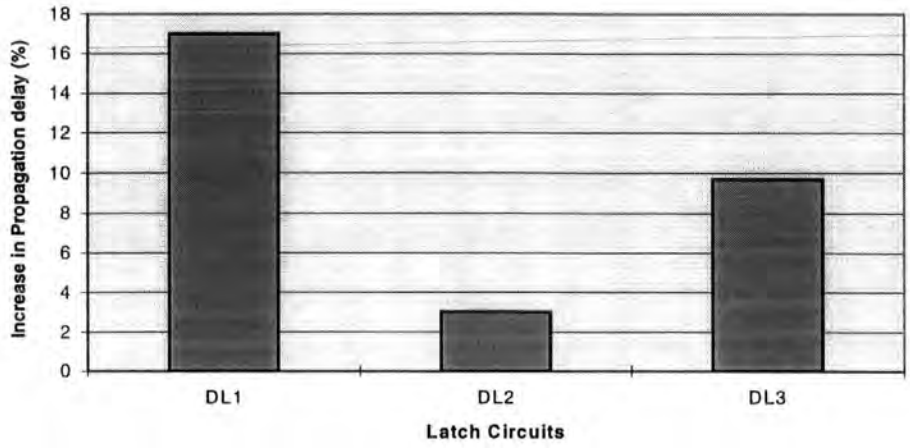


Figure 5.13 Increase in propagation delay for the three circuits

5.3.6 Effects of degradation on set-up and hold times

The set-up time of the latch circuits were affected in varying degrees as the degradations progress. At 10% degradation of the device parameters, no measurable change in set-up or hold time was observed. The increase in set-up time was much more for DL1 with further increase in degradation as shown in the chart of figure 5.14. It shows that this circuit has an average stress greater than all the other circuits giving rise to an increased degradation rate.

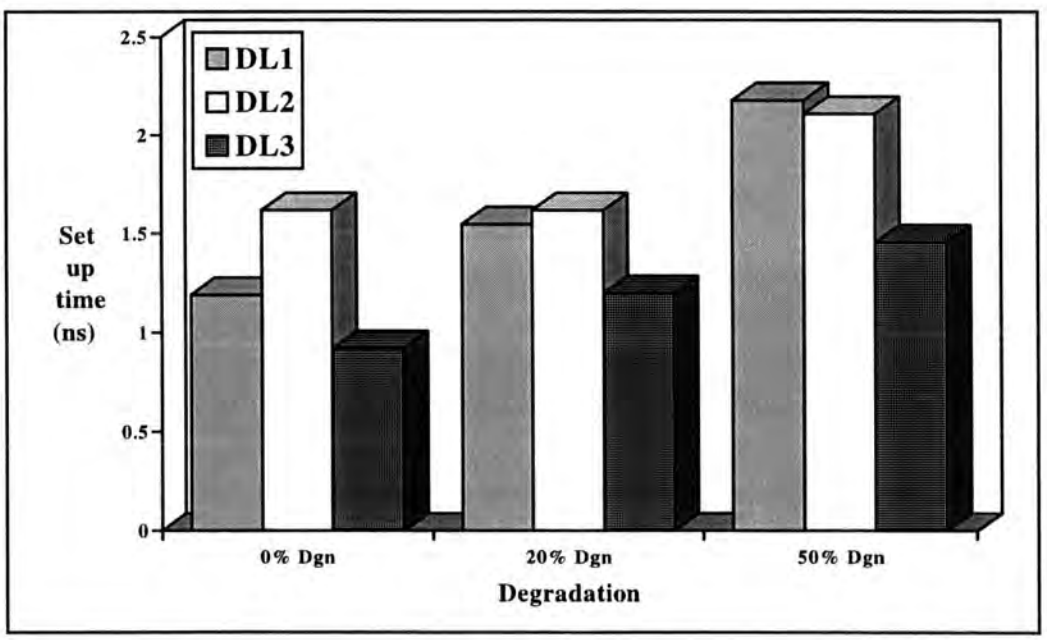


Figure 5.14 Increase in set up time for the three latch circuits

The hold time t_h for all the three latches did not increase with increase in degradation; it remained at the value measured for the virgin latch. The hot-carrier degradations have no effect on the hold time, but has increased the set-up time and hence an increase in the critical window for metastability. The effect of hot-carrier degradations on the metastability state behaviour of the bistable circuits are discussed in the next chapter.

5.3.7 Effect of degradation on minimum pulse width and maximum frequency of operation

When the D- latch circuits are used as ring counters or as shift registers, the maximum operating speed is decided by the time for data transfer from the D- input to the Q output. The maximum operating frequency for the latch circuits were measured by simulating the circuits with an impulse of 50% duty cycle. The minimum pulse width at the DATA input node was determined for correct operation of the latch while keeping the CLOCK signal HIGH. The criterion used for the correct operation was to allow a maximum of ±5% variation or drop in output voltage at Q. At higher frequencies, the circuits failed because the output nodes did not reach the logic levels within the tolerance as set above.

(a) Uniform degradation of all devices in the circuit

Since the degradation effects were not measurable at 10% degradation, it was only measured at higher degradations. The increase in minimum pulse width and the decrease in maximum operating frequency were 2.5%, 8.4% and 5% for every 10% increase in hot-carrier degradation for DL1, DL2 and DL3 respectively when the circuits were degraded uniformly. This shows that if the stress conditions are similar, circuit DL2 will have the highest rate of erosion of operating frequency. The table 5.3 shows the degradation effects on minimum pulse width (T_{min}) for the three latch circuits and figure 5.15 is a graph of maximum frequency of operation versus uniform degradation.

Degradation	DL1	DL2	DL3
0 %	5.5 ns	4.5 ns	4.0 ns
20 %	5.7 ns	5.0 ns	4.25 ns
50 %	6.2 ns	6.4 ns	5.0 ns

Table 5.3 Minimum pulse width with uniform degradation

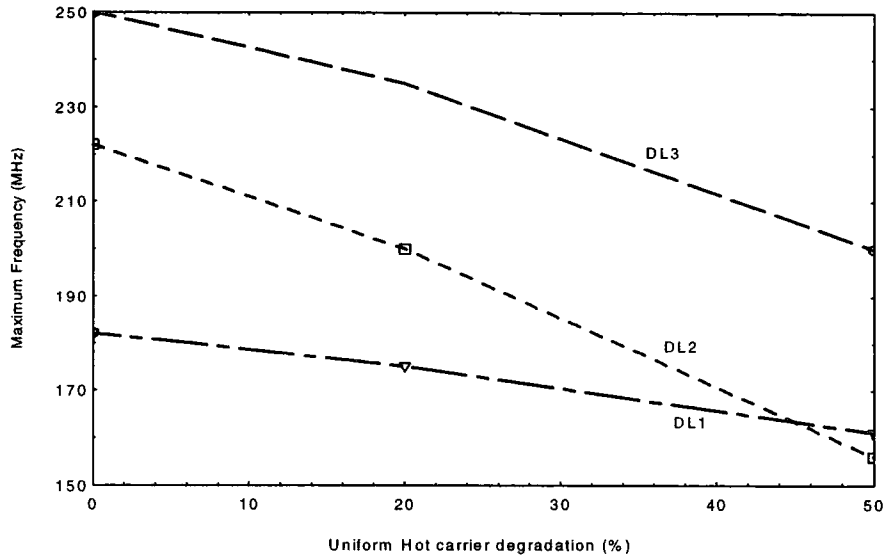


Figure 5.15 Max. frequency Vs uniform degradation plotted for the latch circuits (Process: EC/3, Device: 1/0.8)

(b) Effect of degradation proportional to stress

The degradation effects were noticeable only for DL1 during the simulation period with degradations of all devices proportional to stress. During this period, T_{min} has deteriorated by 4.5% for DL1 and so the maximum operating frequency has also been affected by the same amount. DL1 has shown larger degradation compared to the other two circuits which have negligible decay in maximum operating frequency during the same period. The maximum operating frequency of DL1 has fallen to 174 MHz from 182 MHz.

5.4 Relative susceptibility of different bistables to degradation

From the hot-carrier degradation simulations with uniform stress on all devices, the rise time, fall time, propagation delays, maximum frequency of operation and set-up and hold times have been shown to degrade for the three latch circuits. In actual circuit operation, all devices are not stressed uniformly and so do not degrade at the same rate. We have made use of the substrate current model to assess the stress factors on each device of the latch circuit and the average stress factor for the D-latch circuits were evaluated over one cycle using a typical operating cycle. It was found that circuit DL1 has the highest stress factor while DL2 has the lowest. It can be seen from the analysis of section 5.3 that the delays have increased with degradation but the degradation rate is

not the same for all the circuits simulated.

During dynamic operation of a latch, all the devices go through a stress cycle in which the gate voltages pass through three phases, low to medium, medium and medium to high. The corresponding stress levels and the substrate current generated during the three phases have been modelled using the substrate current model discussed in chapter 3 and the degradation effects during a typical simulation cycle has been modelled using identified SPICE device parameters. It was found from our degradation simulations that the degradation effects do not always translate into characteristic timing parameters in the latch circuits. The position of a device having higher than the average stress level is seen to contribute to the degradation effect leading to a decay in the timing parameters. In the first latch DL1, the highly stressed devices are found at the output nodes and are much more susceptible to increased degradation effect. The degradation effects due to stressed devices at the output nodes for the latch circuits DL1 and DL3 translated into increase in fall time and propagation delays. The second latch DL2 was found to have less than average stress on the device at the output node and hence it degrades at a much slower rate. The stress on the device at the input node of the latch circuit DL2 is higher than the average and the overall effect of this was found in the increased set-up time of the latch. Relative effects of stress on life-time of the circuits will be considered now.

Using the dynamic stress factors and employing the degradation model, we can evaluate the life-time of the circuits. Life-time of a circuit was defined as the stress time over which one or more of the characteristic parameters of the latch degrade by 10% of the original value. Average stress factors and the evaluated life-time for the three latch circuits are listed in table 5.4.

Circuit	Stress Factor (A/m)	Life-time (Hours)
DL1	9.7	1.4×10^4
DL2	4.4	1.5×10^5
DL3	5.4	5.9×10^4

Table 5.4 Stress factor and Life-time for the latch circuits evaluated using the average stress on all devices in the circuits (Technology: EC/3, Device: 1/0.8)

The degradation of the device parameters for all devices in a circuit do not

progress uniformly and so life-time calculated using the average stress was found to be more optimistic than the real life-time. Hence we have evaluated the life-time using the stress and the degradation rate for one of the critically stressed device in each of the three latch circuits. It was found that the stress level and the degradation rate of the device at the output node of the latch circuits affected the characteristic timing parameters more that for other devices and so we have evaluated the life-time using the stress level of this device and is listed in table 5.5.

Circuit	Critical Device	Stress Factor (A/m)	Life-time (Hours)
DL1	N5	21.1	2.1×10^3
DL2	N8	13	1.4×10^4
DL3	N5	10.6	5.5×10^3

Table 5.5 Stress factor and Life-time for the latch circuits evaluated using the stress level on critical device in the circuits (Technology: EC/3, Device: 1/0.8)

A comparative study of three of the D-latch circuits simulated using our degradation model showed that the most severe degradation is experienced by the circuit which used Tri-state devices and NOR gate. The minimum stress and degradations were experienced by the circuit which used NAND gates. The stress and the subsequent degradations were moderate for the D-latch circuit which used Transmission gates and inverting devices.

5.5 Chapter Summary

Our investigations have shown that all the devices in a VLSI circuit do not receive the same amount of electrical and environmental stress. The level of electrical stress received by each device is a complex function of the transistor location, terminal voltage, current magnitude and duty cycle. A circuit may become inoperative due to the failure of some critical devices. It is possible to improve the circuit reliability by reducing the stress applied to these potentially weak devices through circuit-level reliability enhancement techniques and by process parameter adjustments (i.e. fine tuning of process parameters which are critical to circuit performance such as threshold voltage).

Using substrate current as a monitor, the hot-carrier stress experienced by the

devices in the latch circuits has been modelled. The corresponding degradation in device parameters have been established using circuit level simulations and the shift in circuit delays leading to metastability in the D-latch circuits analysed. The effects of degradations on the three latch circuits were compared and analysed.

In all the three circuits simulated, it is possible to reduce the stress on highly stressed devices which can be identified by using the model developed. A number of techniques can be employed to reduce the stress on these critical devices and thereby improving the overall reliability of the circuit and these will be discussed in the next chapter.

D-latch circuits which used NAND gates in place of NOR gates and Tri-state devices must be employed for high reliability circuits in order to reduce hot-carrier degradation problems.

Chapter 6

Metastability Behaviour and Reliability of Bistable Circuits

Metastable operation of latches and flip-flops is recognised as a potential cause of timing errors in digital systems. These timing errors are due to the unusually long delay in logic decision time due to the metastable state which is a state between the two stable logic states where a circuit output may remain for an indefinite time before resolving into one of the stable states. Many research papers [6.1-6.19] have been published on this subject and many have suggested ways for minimising the errors caused in digital systems due to synchroniser malfunction. However the problem of metastability in latches and flip-flops still remain unresolved even though better understanding of the metastable operation of these elements are at hand.

In this chapter, the reliability problems of bistable circuits operated in the metastable region are addressed. It was shown in chapter four that D-type latch circuits when operated under marginal triggering conditions may enter the metastable state. In chapter five, it was demonstrated that the D-type latch can become unreliable after hot-carrier degradations due to metastable state operation. A clear understanding of the conditions under which the D latch will enter the metastable state and the effects of hot-carrier degradations on metastability will help us to design reliable latch circuits for incorporation into VLSI circuits.

6.1 What is Metastability?

Metastable is a Greek word meaning *between stability* and it is a state between the logic HIGH and logic LOW states in a digital system [6.22]. Metastability is a condition which can occur in any latch or flip-flop if the minimum set-up or hold times are violated. In most cases, the flip-flop will either react to the input and switch to a new stable state or remain in the current stable state. The normal operation of a flip-flop can be disrupted if the data input changes during the set-up or hold time interval preceding the clock pulse. Under these circumstances, there is a chance that the input has changed at a critical time, causing the output of the flip-flop to hover at the logic threshold literally for microseconds or even worse, go towards one logic state and before settling at this state switch back to the other state! In most flip-flops and other synchronising circuits, the metastable state may last for only a short period of time, but theoretically this state can persist indefinitely. When the output of a device goes into metastable state the clock to out delay will be grossly affected. This may affect the system's worst case propagation delay and potentially lead to a system failure.

A functional definition of metastability applied to cross-coupled circuits is the occurrence under undriven conditions of an output voltage in a range around V_t (transition voltage) that cannot reliably be interpreted as either high or low [6.20]. As discussed in section 3, static latch circuits are made by cross coupling two inverting devices. When plotting static transfer curves for the two cascaded inverters, (as shown in figure 6.1) the resulting three intersections indicate three points of equilibrium [6.17].

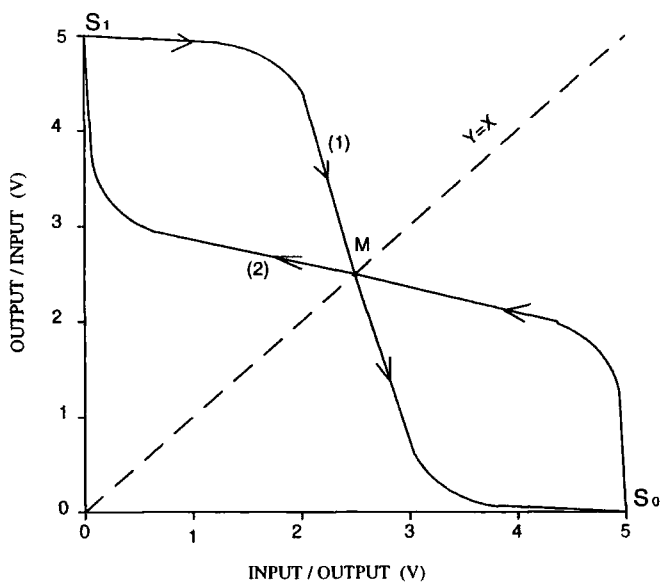


Figure 6.1 Bistable State transfer Curve

A latch or a flip-flop in a fault free self-contained synchronous system never has the opportunity to reach a metastable condition since satisfaction of the timing constraints assures that the output is driven to a voltage outside of a metastable range [6.20]. But if asynchronous inputs are applied to a latch, the data and the clock inputs may change simultaneously producing a metastable state at the outputs of the latch. If this condition persists for more than a clock period, an illegal or incorrect logic value may be transmitted to the next stage of the digital system. A further possible cause of metastability is timing errors which may be introduced by incorrect design or device parametric shift. We have shown in chapter five that parametric shift can be introduced by hot-carrier degradation and the effect of this on metastability in cross coupled circuits will be discussed in this chapter.

The reliability of bistables have been influenced by timing errors introduced by the *metastable state* operation which may occur in any device having two stable states. If the bistable outputs linger half way between the logic *high and low* states longer than the normal logic decision time, an erroneous output may be generated. For reliable operation of flip-flops, it is vital to recognise this problem and to prevent it by means of improved design methods. Parametric variations introduced during processing as well as during normal operation are usually responsible for these timing errors and so it is very important to include the metastable state simulations during the design stage so as to study the effects on critical parameters and to devise design improvements to reduce this problem.

6.2 A review of metastability in bistables

Metastability has been recognised as a problem as early as 1966 and many papers have been published on this subject. Interest in this field has been increasing for the last seven or eight years and this can be seen from the number of papers published recently. The interest in this field has been revived probably due to the increase in speed of digital devices due to scaling and the reduction in set-up and hold times of fast synchronisers. Metastability effects are potentially very important for submicron devices because of the parametric degradations introduced by hot-carriers.

One of the first paper published on this subject was by Ivor Catt [6.1] in February 1966 and his encounter with this problem was through the semiconductor industry (Motorola Inc., Phoenix, Ariz.). He has coined the word *metastable state* to

represent the operation of the output of a digital system at half the supply voltage for an extended period of time. In his paper, he has discussed the time loss through gateing of asynchronous logic signal pulses and suggested that the problem can be solved by using a circuit element having very high gain and to this day this has been the best and most simple solution.

Researchers T. Chaney and C. Molnar [6.2] (1973), W. Fleischhammer and O. Dortok [6.7] and L. Reyneri, D. Corso and B. Sacco [6.18] (1990) have considered oscillatory behaviour in the metastability region and suggested design techniques to improve metastable state resolving for TTL flip-flops. H. Veendrick [6.8] proposed a method for predicting the failure rate by a graphical extrapolation technique and indicated that the probability of failure can be decreased by optimising W/L ratios of the driver and load transistors.

Theoretical approach for the metastable state problem was put forward by G. Couranz and D. Wann [6.3] (1975) as well as L. Mariano [6.9] (1981) and have claimed that the theory can be applied to digital as well as non-digital systems without any restriction and have used a standard cross coupled NAND gate latch as the model to develop the theory. F. Rosenberger and T. Chaney [6.10] (1982) presented techniques for measurement of resolving time parameters for latches operated in the metastable region. The measurements were based on R-S flip-flops formed from NOR gates using nMOS technology but did not offer any solution to the metastable state problem.

P. Stoll [6.11] of Intel Corporation in his paper defined a "failure window" for a synchroniser in terms of propagation delay and resolution time constant of the circuit. Another parameter of great importance, the "mean time before failure" (MTBF) was introduced as a function of the timing parameters.

The first published work on metastability in CMOS flip-flops was by S. Flannagan [6.13] in 1985. He has used numerical analysis and phase-plane trajectories for analysing metastable behaviour of CMOS flip-flops. Error rate was determined as a function of delay parameter and the gain band width (GB) product estimated. It is implied that by increasing the GB of the flip-flop, the error probability can be minimised and this can be done by optimising the design of the circuit. It was also stated that GB is maximum when $W_n = W_p$, even when the n- and p-transistors have unequal carrier mobilities or unequal threshold magnitudes. L. Kleeman and A. Cantoni [6.14] suggested a number of ways by which the performance of the synchroniser can be

improved and were of the opinion that extended decision time is the best technique for lowering the probability of synchronisation failure.

The metastable operation of CMOS R-S flip-flops was presented by T. Kacprzak and A. Albicki [6.15] (1987) making use of R-S flip-flops having two cross coupled NOR gates implemented using CMOS technology. They also made use of the small signal linear amplifier model biased around the metastable region and evaluated the resolving time constant in terms of the transistor sizes and fabrication process parameters. They have suggested that the failure rate can be improved by minimising the resolving time constant and optimising circuit parameters.

T. Sakurai [6.16] (1988) used cross coupled NAND gates for metastability simulations and suggested optimum size to improve metastable state resolving. J. Horstmann, H. Eichel and R. Coates [6.17] also used R-S flip-flops to study metastable state operation and the analysis was carried out using a number of graphical illustrations of state-space trajectories of flip-flops triggered between two stable states.

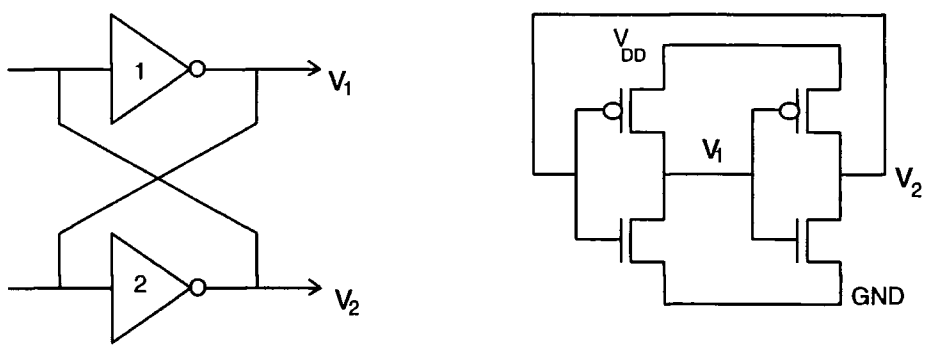
A well written paper on metastability of CMOS latch/flip-flop is by L. Kim and R. Dutton [6.19] (1990). They have investigated various aspects of the design and timing parameters for improving the metastable resolution of the devices. The influence of fabrication parameters such as threshold voltage, gate oxide thickness, substrate doping etc., on metastability was investigated. It was found that by lowering the threshold voltage, it is possible to improve the metastable resolving capability of the flip-flop. They have suggested the optimal device size, aspect ratio and circuit configurations for the metastable hardened design. Two recent papers [6.25] and [6.26] are also based on metastability simulations of CMOS latches.

Researchers [6.1]-[6.4],[6.6],[6.7],[6.9],[6.10],[6.14] and [6.18] mainly concentrated on gate level models and were of theoretical nature and researchers [6.5],[6.8] and [6.12] have included nMOS circuits in the investigation on metastability. Most of the recent papers were based on circuit simulations on CMOS latch and flip-flop circuits [6.13],[6.15]-[6.17],[6.19]. Since CMOS is the most popular and the most mature technology available today, researchers and semiconductor manufacturers are interested in all the aspects of metastability in CMOS devices so as to improve the reliability of the synchronisers by design improvements and by optimisation of process

parameters. We have control over design parameters such as device size, aspect ratio, circuit configurations etc., and process parameters such as threshold voltage, substrate doping, gate oxide thickness etc., and these parameters can be adjusted for the best possible metastable hardened design. More research is needed so that we can have a better understanding of the various parameters and their effect on metastability in latch and flip-flop circuits.

6.3 Metastability Resolving Time

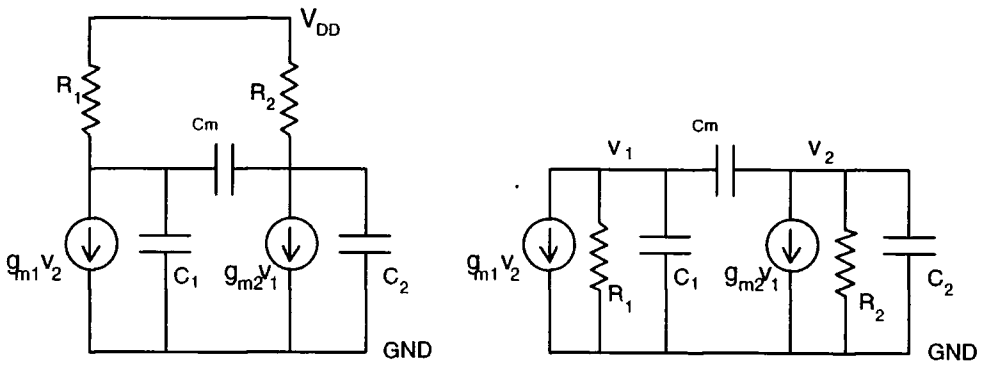
A simple latch is basically two inverting devices cross coupled as shown in figure 6.2(a). It is possible to realise this circuit using two NAND gates, two NOR gates or two inverters. When the latch is in a metastable state, the voltages at the two output nodes will be exactly the voltage known as the transition voltage V_t and in this thesis it will be called the metastable voltage V_m . A transistor level circuit for the latch using CMOS logic is given in figure 6.2 (b).



(a) Gate level circuit (b) Transistor level circuit

Figure 6.2 A simple latch

In the metastable state, both n- and p-transistors are biased in the saturation region and have large gains. Hence it is possible to replace the circuit by its small signal model given in figure 6.3 [6.19]. The p-transistors are replaced by their equivalent ON resistances R_1 and R_2 respectively in the saturation region and the n-transistors are replaced by its transconductances g_{m1} and g_{m2} respectively, multiplied by the nodal voltages as shown. C_1 and C_2 are the nodal capacitances at the two output nodes respectively and C_m is the coupling capacitance between the gate and the drain of the transistors. An ac small signal equivalent circuit of the latch in the metastable region is shown in figure 6.3(b) and the voltage evolution at the two output nodes are plotted in figure 6.4.



(a) d.c. equivalent circuit (b) a.c. equivalent circuit

Figure 6.3 Small signal models for the latch operated in the metastable region

Using small signal analysis, the circuit equations for the latch operated at the metastable region are [6.25],

$$g_{m1} v_2 + \frac{v_1}{R_1} + C_1 \frac{dv_1}{dt} + C_m \frac{d(v_1 - v_2)}{dt} = 0 \qquad \text{--- (6.1)}$$

and

$$g_{m2} v_1 + \frac{v_2}{R_2} + C_2 \frac{dv_2}{dt} + C_m \frac{d(v_2 - v_1)}{dt} = 0 \qquad \text{--- (6.2)}$$

Solving equations (6.1) and (6.2) for v_1 and v_2, we obtain,

$$\Delta V = \Delta V_0 \, e^{t/\tau} \qquad \text{--- (6.3)}$$

where $\Delta V = (v_2 - v_1)$ is the voltage evolution at the output nodes with time, ΔV_0 is the value of ΔV at time $t = 0$ and τ is the resolving time constant and is given by,

$$\tau = \sqrt{\frac{C_1 C_2}{g_{m1} g_{m2}}} \qquad \text{--- (6.4)}$$

When a CMOS inverting device is operated at the metastability region, both the nMOS and the pMOS transistors are in the saturation region and the currents through them are the same, i.e. $I_{Dn} = I_{Dp}$. Equating the current equations for n- and p- MOS transistors in the saturation region, we have, [6.27]

$$\frac{\mu_n}{2} C_{ox} \frac{W_n}{L_n} (V_m - V_{Tn})^2 = \frac{\mu_p}{2} C_{ox} \frac{W_p}{L_p} (V_{DD} - V_m - |V_{Tp}|)^2 \qquad \text{--- (6.5)}$$

Assuming that $L_n = L_p$ and C_{ox} is the same for the two devices, the metastability voltage V_m for an inverting device is given by [6.19],

$$V_m = \frac{V_{DD} - |V_{Tp}| + V_{Tn}\, b}{1 + b} \qquad \text{--- (6.6)}$$

$$\text{where } b = \sqrt{\frac{W_n}{W_p}\frac{\mu_n}{\mu_p}} \qquad \text{--- (6.7)}$$

The gain g_m of the NMOS transistor at the metastable region is defined as the slope of the transfer curves at V_m and is given by,

$$g_m = \frac{d(I_{Dn})}{dV_m} \qquad \text{--- (6.8)}$$

$$= \frac{d\left(\frac{\mu_n}{2} C_{ox} \frac{W_n}{L_n}(V_m - V_{Tn})^2\right)}{dV_m} \qquad \text{--- (6.9)}$$

$$= \mu_n \frac{W_n}{L_n} C_{ox}(V_m - V_{Tn}) \qquad \text{--- (6.10)}$$

Substituting equation (6.6) in (6.10), we have,

$$g_m = \mu_n \frac{W_n}{L} C_{ox} \frac{V_{DD} - |V_{Tp}| - V_{Tn}}{1+b} \qquad \text{--- (6.11)}$$

The value of C_m has very little effect on resolving time but it affects the bandwidth (BW) of the latch. The gain band width product (GB) of the latch is given by [6.13],

$$GB = \frac{(V_{DD} - |V_{Tp}| - V_{Tn})\sqrt{\mu_n \mu_p}}{L\,a} \frac{\sqrt{R}}{R+1} \qquad \text{--- (6.12)}$$

$$\text{where } R = \frac{W_n}{W_p} \text{ and } a = \frac{C_t}{(W_n + W_p) L C_{ox}} \qquad \text{--- (6.13)}$$

The total effective capacitance at the output nodes C_t is given by,

$$C_t = \mathrm{K} C_{ox}(W_n + W_p) L \qquad \text{--- (6.14)}$$

where K is the ratio of output capacitance to input capacitance. The resolving time constant can be evaluated from the circuit parameters using [6.24],

$$\tau = \frac{\mathrm{K} L^2 (W_n + W_p)}{(V_{DD} - V_{Tn} - |V_{Tp}|)\sqrt{\mu_n W_n}\sqrt{\mu_p W_p}} \qquad \text{--- (6.15)}$$

Using equations (6.12) and (6.15) we can calculate the GB and τ for a number of latch circuits for comparison. By selecting a latch having a higher GB and lower τ, it is possible to improve metastability resolving and hence the reliability of the latch. The resolving time can be evaluated by circuit simulations and is discussed in the next section.

Using equation (6.3) for evaluating the resolving time, we can define the mean time between failure for the latch as [6.14],

$$MTBF = \frac{e^{t'/\tau}}{f_D f_c T_0} \qquad \text{--- (6.16)}$$

where t' is the resolving time, f_c the clock frequency, f_D is the average frequency of the data and T_0 is a constant related to the set-up time of the latch. By reducing the resolving time t', we can improve the MTBF of the latch.

If the inverting devices used in a latch have the same gain and input and output loads, the circuit is called a matched latch. For a matched latch, if we assume that b = 1 and $|V_{Tp}| = V_{Tn}$ then we have, $V_m = ½ V_{DD}$ for the two inverting devices and we have a balanced latch. In such cases it is possible to force the latch into a metastable state by setting the inputs of the latch to $½ V_{DD}$ at t = 0 and removing this restriction for t > 0. A plot of the metastable operation of a nearly matched latch is shown in figure 6.4 and it displays an exponential evolution of the output nodal voltages as expressed in equation (6.3)

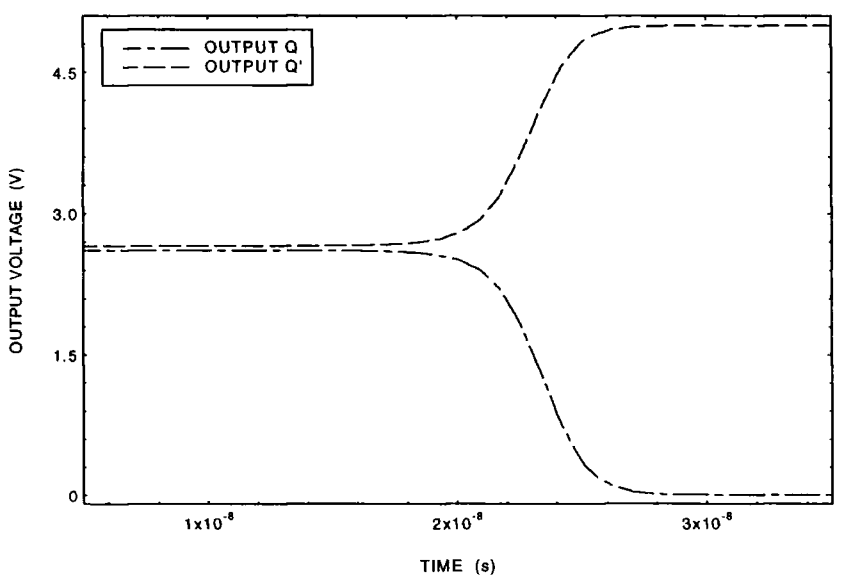


Fig 6.4 Voltage evolution at the outputs of a nearly matched latch operated in the metastable region (Process: EM/3, Device: 4/3)

When the inverters are not matched, V_{m1} and V_{m2} for the two inverters must be calculated using equations (6.6) and (6.7). By setting the input nodes to the predetermined values, the latch can be operated in the metastable region.

Similar techniques have been used by many researchers to force a latch into metastable operation. Kacprzak and Albicki [6.15] used an RS flip-flop and the metastable operation was achieved by forcing both R and S inputs to the active mode which will bring both Q and Q' outputs to logic zero and the time evolution is studied. Horstmann [6.17] also used a similar technique to study metastability in latch circuits. Another researcher [6.16] used a *dummy* MOSFET to short circuit the two output nodes for a short period allowing the cross coupled NAND latch to enter a metastable state. An experimental set up involving the latch under test, an oscilloscope and two pulse generators were used by a researcher [6.24]. We found that the method by which the input and output nodes are set to the pre-evaluated metastable state is the simplest and valid method for evaluating the resolving time.

We have assumed that the small signal model is valid for analysing the metastable region. Using the acceptable logic state values at the input of a CMOS logic gate, we can show that this assumption is valid for evaluating the resolving time and is discussed now.

For CMOS inverters, the metastability region is between V_{IL} and V_{IH} and can be calculated from the threshold voltages and the dimensions of the n- and p- transistors [6.23, 6.27]. The input low voltage occurs when the nMOS transistor is saturated while the pMOS device is non saturated. Equating the currents for the two transistors gives,

$$\frac{\beta_n}{2}(V_{IL}-V_{Tn})^2=\frac{\beta_p}{2}[2(V_{DD}-V_{IL}-|V_{Tp}|)(V_{DD}-V_{out})-(V_{DD}-V_{out})^2] \qquad \text{--- (6.17)}$$

where V_{in} and V_{out} are the input and output voltages for the CMOS inverting device. Since I_{Dn} is a function of V_{in} and I_{Dp} is a function of V_{in} and V_{out}, the unity-slope point where $(dV_{out}/dV_{in}) = -1$ is determined by,

$$\frac{dV_{out}}{dV_{in}}=\frac{(dI_{Dn}/dV_{in})-(\partial I_{Dp}/\partial V_{in})}{\partial I_{Dp}/\partial V_{out}}=-1 \qquad \text{--- (6.18)}$$

Evaluating the derivatives and substituting in (6.18) gives,

$$V_{IL}(1+\frac{\beta_n}{\beta_p}) = 2V_{out} + \frac{\beta_n}{\beta_p}V_{Tn} - V_{DD} - |V_{Tp}| \qquad \text{--- (6.19)}$$

Equations (6.17) and (6.19) must be solved simultaneously which yield a quadratic for V_{IL}. These can be reduced by substituting the numerical values for the parameters and can be solved for V_{IL}. For the special case when $(\beta_n / \beta_p) = 1$, the equations can be simplified as, [6.23]

$$V_{IL} = \frac{3V_{DD} - 3|V_{Tp}| + 5V_{Tn}}{8} \qquad \text{--- (6.20)}$$

V_{IH} can be evaluated by noting from the voltage transfer curve of a CMOS inverter that, when $V_{in} = V_{IH}$, the nMOS transistor is non saturated and the pMOS transistor is saturated. Equating the currents in the two devices, we get,

$$\frac{\beta_n}{2}[2(V_{IH} - V_{Tn})V_{out} - V_{out}^2] = \frac{\beta_p}{2}(V_{DD} - V_{IH} - |V_{Tp}|)^2 \qquad \text{--- (6.21)}$$

Since $I_{Dn}(V_{in}, V_{out}) = I_{Dp}(V_{in})$, the derivative for the transfer curve is,

$$\frac{dV_{out}}{dV_{in}} = \frac{(dI_{Dp} / dV_{in}) - (\partial I_{Dn} / \partial V_{in})}{\partial I_{Dn} / \partial V_{out}} = -1 \qquad \text{--- (6.22)}$$

and can be solved to give,

$$V_{IH}(1+\frac{\beta_p}{\beta_n}) = 2V_{out} + V_{Tn} + \frac{\beta_p}{\beta_n}(V_{DD} - |V_{Tp}|) \qquad \text{--- (6.23)}$$

Equations (6.21) and (6.23) can be solved for V_{IH} using standard techniques. For the special case when $(\beta_n / \beta_p) = 1$, we can obtain a simplified equation for V_{IH} ,

$$V_{IH} = \frac{5V_{DD} - 5|V_{Tp}| + 3V_{Tn}}{8} \qquad \text{--- (6.24)}$$

The evaluation of the equations (6.20) and (6.24) for the given circuit parameters gave us, ΔV (for metastability resolving) = V_{IH} - V_{IL} = 0.90 V.

These are approximate values for $(\beta_n / \beta_p) = 1$, $V_{Tn} = 0.9$ V and $V_{Tp} = -0.5$ V. Using these values ΔV is approximately 0.90 V in the metastable region and we are justified in using the small signal model for the analysis given above.

6.4 Metastability Simulations

The operation of the latch as it enters the metastable state and the time evolution of the two outputs Q and Q' to the termination of metastability is of paramount importance in the design of synchronisers. A better understanding of the operation of the latch at the metastable state will help us to design a latch which is reliable and hardened against metastable operation.

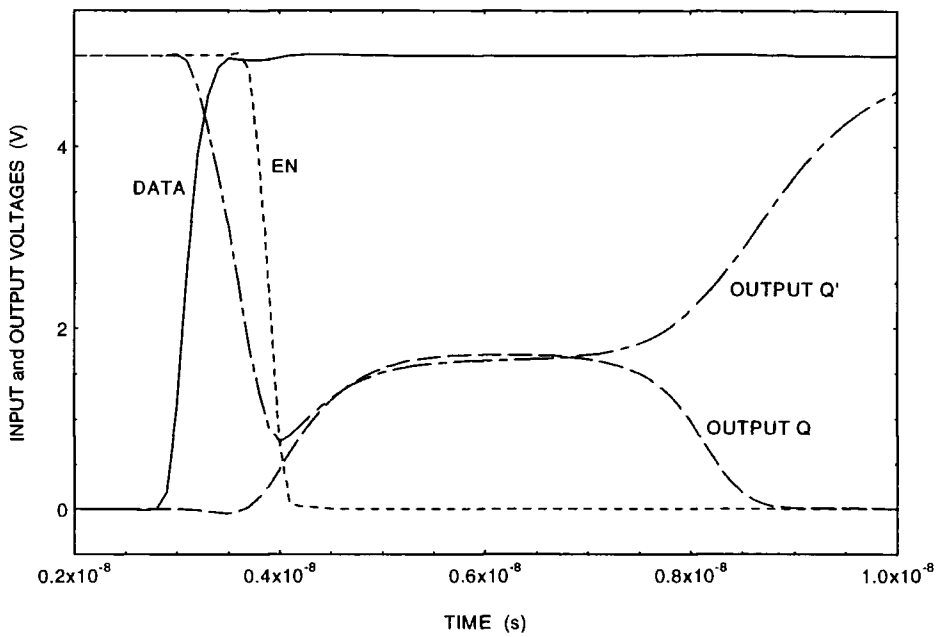


Figure 6.5 Metastable simulation for DL1 by adjusting clock edge to 0.61035 ns (Process: EC/3, Device: 1/0.8)

The nine D-type latch circuits discussed earlier in this thesis were tested for metastability. The circuits were coded using SPICE taking care to include the area and perimeter dimensions of the drain and source for SPICE to evaluate the capacitances at these nodes and simulated using optimised MOS SPICE model parameters. Since the latch is made up of inverting devices as discussed in chapter 4, parametric imbalance in the transconductances, conductances, parasitic capacitances, threshold voltage of the devices and any change in the output or input load capacitances can result in an undesirable effect and the latch may settle in the wrong state. Hence all these parameters must be standardised for optimum operation of the latch under fault free conditions. The standardisation and optimisation of the latch designs were discussed in chapter 4. Repeated simulations were carried out by adjusting the edge of the input DATA with respect to the clock (EN) edge to force the latch into a metastable state. Figure 6.5 shows the operation of the latch DL1 in the metastable region.

The inputs, DATA and EN, and the outputs Q and Q' are shown in the figure. When the DATA edge was adjusted to 0.61035 ns with respect to the EN edge, the output Q' fell much below the transition voltage of the NOR gate pulling the output node Q towards V_{DD}. At the point of intersection of the Q and Q' outputs at about 4 ns, the edge of EN has fallen sufficiently cutting off the inverting device controlling the DATA input into Q'. At this point the feed-back path from Q to Q' has been switched on assisting the rising Q to aid Q' to be pulled low. Due to the slow rise time of the relatively slow pMOS devices (we have two pMOS devices in series for the NOR gate) and the propagation delays, the output Q rose very slowly and both outputs now entered a metastable state. Both output voltages were now at the transition voltage, $V_{IN} = V_{OUT}$ and have remained in the metastability state for about 4 ns. How the latch will resolve itself from the metastable state will be decided by the relative gains of the n- and p-devices and the load capacitances, which must be charged or discharged, connected at the two output nodes. At the Q output the n- transistor is stronger and it pulled Q low and the feed back effect pulled Q' high terminating the metastable state.

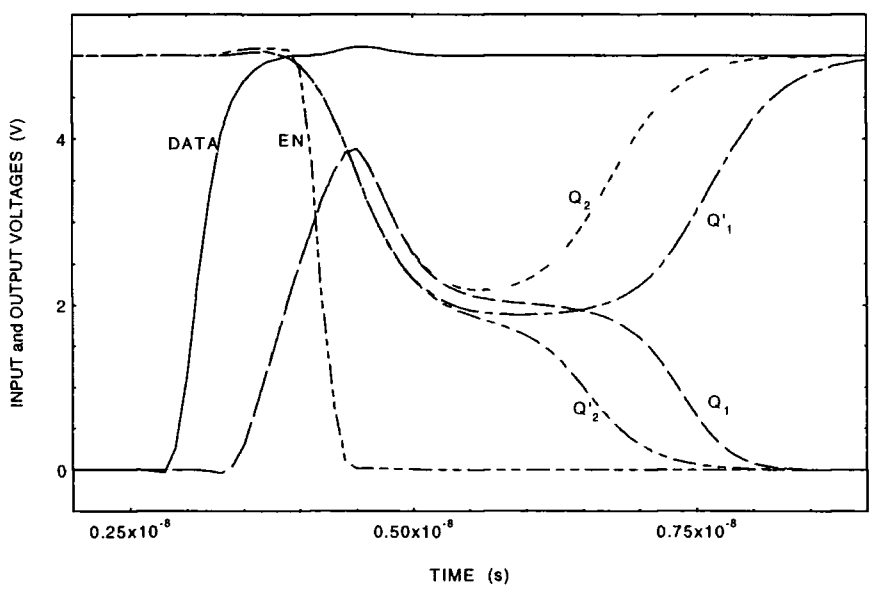


Figure 6.6 Metastability resolving for latch DL2 at clock edge of 0.92329685 ns (Q_1 & Q_1') and 0.92329688 ns (Q_2 and Q_2'). (Process: EC/3, Device: 1/0.8)

At this point it is worth pointing out that the events may not always follow exactly as given above allowing the termination of the metastability in which Q is pulled low by the stronger n- device. In the metastable state, we have an exactly balanced pair of cross coupled inverting devices and any small variation in the input conditions or the output load will produce the opposite effect. This can be seen in the plots shown in

figure 6.6, in which the first set of output wave forms are shown to be exactly opposite to the second set, both differing by just a fraction of a femto second. This type of simulations in the metastable region need a lot of patience and can be very time consuming. If we try to go any lower than this interval of time, many of the error tolerances of the SPICE algorithm and convergence problems may result in a non-repeatable result which can be of very little value to us.

The metastability simulations shown in figure 6.7 is that for latch DL3 and displays a metastable region of more than 3 ns (measured at a clock edge time of 0.7139798 ns). We can also notice a number of features typical of this latch design. At the intersection of the EN edge with DATA, the rising edge of DATA is distorted as the transmission gate gain is reduced due to the sharply falling gate voltage. The internal node (8) did not have sufficient time to settle to the DATA high value and during this period, the second transmission gate is switched on connecting the positive feed-back path between Q and node (8).

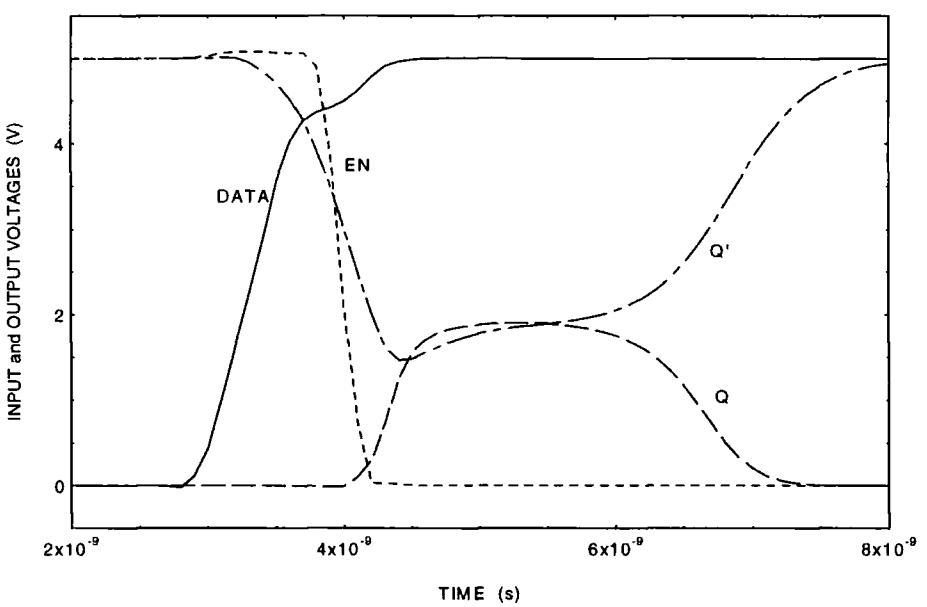


Figure 6.7 Metastabilty simulation for latch DL3 at a clock edge of 0.7139798 ns.
(Process: EC/3, Device: 1/0.8)

Transmission gates are pass elements and can pass the signal voltages in both directions without much drop in signal levels. As the feed-back path is opened, the output nodes reach a common voltage, and in this case it happened to be the transition voltage we referred to as the metastable voltage. After a delay of more than 3 ns, the output nodes respond to the gains of the devices connected to the nodes and the circuit resolves out of this condition. The nMOS transistor at the output node has a higher gain

at this stage and is able to pull the output Q low and Q' responds to the feed-back effect reaching the supply rail voltage. The data input failed to latch at the output node in this instance, but at a slightly increased time delay the outputs will respond with an opposite effect.

In many of the latch circuits designed using 3 micron CMOS design rules, it was observed that the metastability can last for 10 ns and longer. The 0.7 micron design rules used for the design of the latch circuits DL1, DL2 and DL3 in the simulations shown, made the circuits much faster and have higher gains in the metastable region. This has the overall effect of reducing the metastability region of the latches; but with hot-carrier degradations, these devices are expected to be more susceptible to failure due to metastability. A plot showing the comparatively large resolving time (>15 ns) is given in figure 6.8. It displays excessively large rise and fall times for the output voltages Q and Q' compared to DATA and EN inputs at the metastable region.

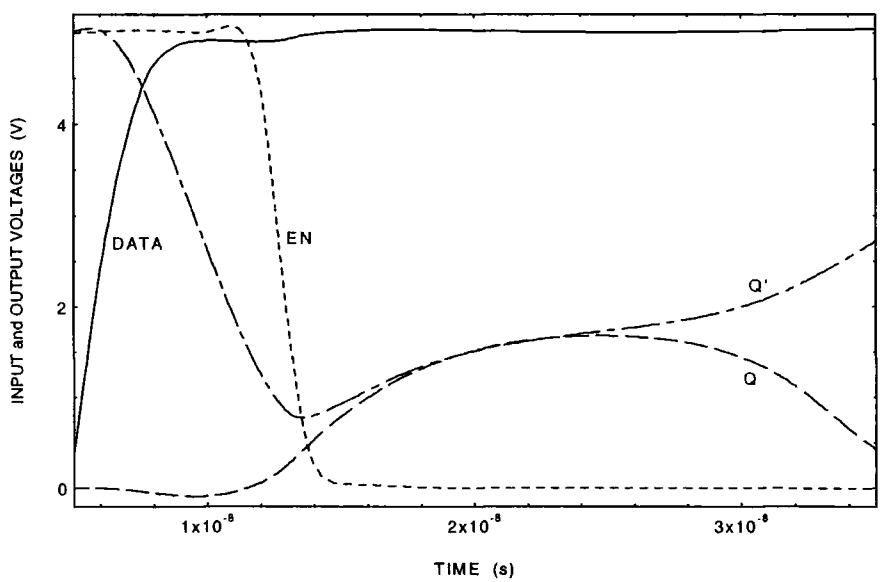


Figure 6.8 Metastable state simulation for a latch designed using 3 micron technology. (Process: EC/3, Device: 4/3)

All the metastabilty simulations plotted in figures 6.5 to 6.8 were for metastability simulations due to set-up or hold time violations. The time interval between clock and data must be adjusted precisely close to a fraction of a femto second or smaller to force the latch into the metastable state with both outputs floating at half supply voltage. Since this was found to be a very time consuming method, a second method suggested in section 6.3 by which the input nodes were preset to the metastable voltage calculated from device parameters was employed successfully. This forced the

latch into metastable state and the time evolution of the output node voltages were studied. The plots shown in figures 6.9 to 6.11 are the metastable resolving simulations for the three latch circuits respectively.

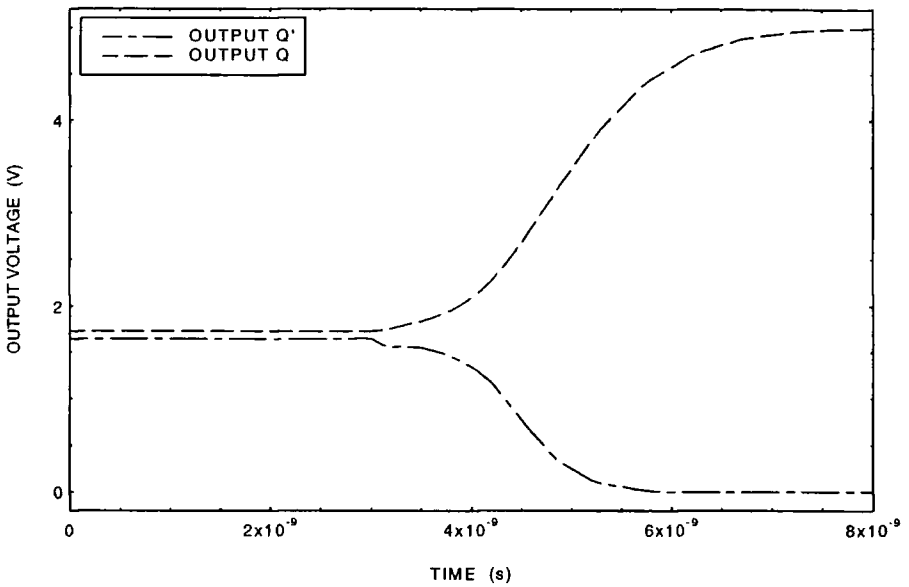


Figure 6.9 Metastable state resolving simulation for DL1. (Process: EC/3, Device: 1/0.8)

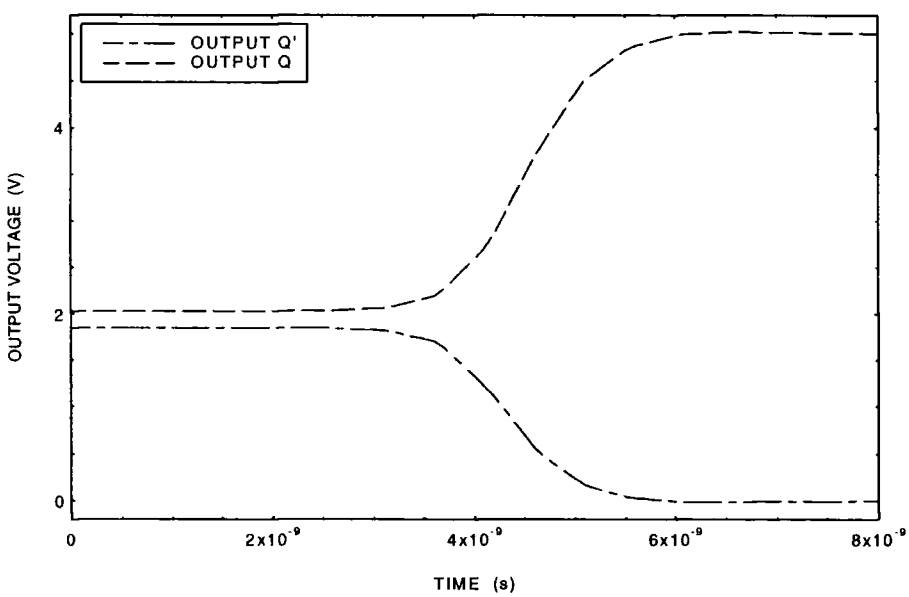


Figure 6.10 Metastable state resolving for DL2. (Process: EC/3, Device: 1/0.8)

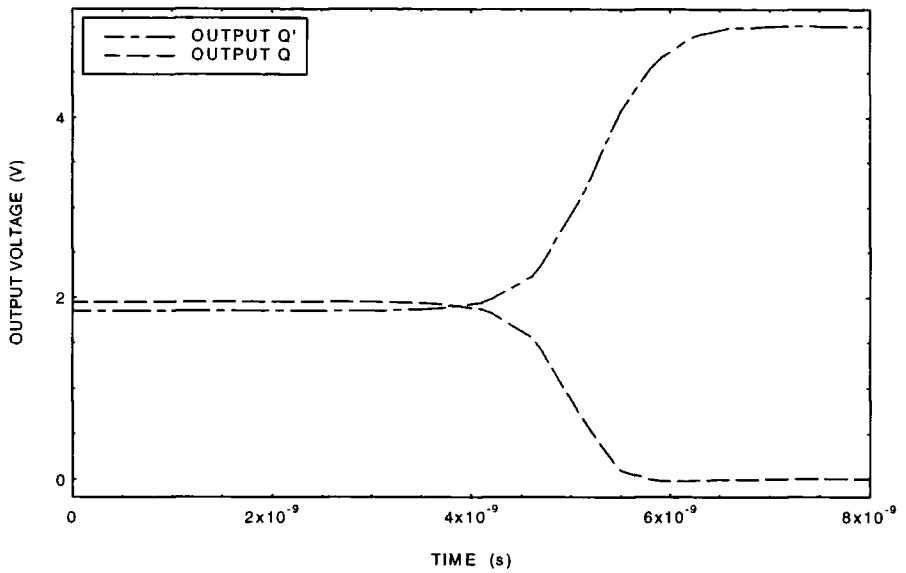


Figure 6.11 Metastable state resolving simulation: DL3. (Process EC/3, Device: 1/0.8)

This method has the advantage of measuring the resolving time very accurately and can save the time taken for repeated simulations necessary for the metastable simulation method by adjusting the clock edge. The resolving times measured using this method are tabulated in table 6.1.

OUTPUT LEVEL	DL1	DL2	DL3
$\Delta V = 1$ V	4.12 ns	3.87 ns	4.70 ns
$V_{OH} \geq 3$ V & $V_{OL} \leq 2$ V	4.70 ns	4.27 ns	5.05 ns

Table 6.1 Resolving times measured for the three latches for the two output level conditions.

Two output level conditions are used to determine the point at which the output nodes come out of metastability. Using equations (6.20) and (6.24), we can calculate the minimum value of V_{OH} and maximum value of V_{OL} for the latch outputs which will be detected as V_{IH} and V_{IL} for the logic connected to the outputs of the latches. The values of ΔV calculated had a range of 0.95 to 0.70 volt, and for convenience it was selected as 1 V for all the latches taking into account a small noise margin. The second value of resolving time was calculated considering that the latch circuits did not produce a symmetric output. Hence the first occurrence of a voltage ≥ 3 V and ≤ 2 V on the output nodes will be detected as the termination of metastability. The latch DL2

was found to have the minimum value of resolving time and so it is expected to be more reliable.

6.5 Effects of hot-carrier degradation on metastability

It was shown in chapter 5 that hot-carriers degrade the characteristic timing parameters of the latch circuits. In this section, we will analyse the effect of hot-carrier degradations on the metastability behaviour of the latches.

We have used four SPICE device parameters to model the degradation effects due to hot-carriers. These parameters are NFS, UO, VTO and RSH; the modelling of the degradation effects was discussed in chapter 3. The characterisation of the degradation effects were carried out by degrading the above SPICE parameters by 10%, 20% etc. and the corresponding effect on metastable state operation of the latch circuits were determined by circuit simulations.

The stress factors were determined for all the devices in the latch and the selected SPICE parameters were degraded based on the degradation model discussed in chapter 3. Metastability simulations were carried out using the degraded device models and the effect of resolving times were determined and compared. The critical window for metastability was defined in chapter four as the period during which the output of a latch remained in the region between V_{IL} and V_{IH}. This region is found to be the sum of the set-up time and the hold time for the latch. The critical window for metastability for the latch circuits evaluated using degradation simulations are listed in table 6.2 and this result was compared with that for the virgin circuit. The simulation results show that the critical window for metastability for the latch circuits increased with hot-carrier degradation and the effect is much more for circuit DL1 compared to DL2 and DL3 when all the devices in the circuits were degraded uniformly.

Degradation	DL1	DL2	DL3
0 %	1.2 ns	1.1 ns	1.0 ns
20 %	1.6 ns	1.1 ns	1.2 ns
50 %	2.2 ns	1.6 ns	1.5 ns

Table 6.2 Critical window for metastability for the 3 latches measured as a function of degradation

The three latch circuits were now degraded proportional to the stress (determined by stress simulations) and the time evolution of the circuits were studied using metastability simulations. The plot in figure 6.11 shows the evolution of the output voltages after degradation, superimposed on the plot obtained for the virgin latch circuit DL1. The degraded latch has an increased resolving time compared to the virgin circuit and we also notice the increase in rise and fall times.

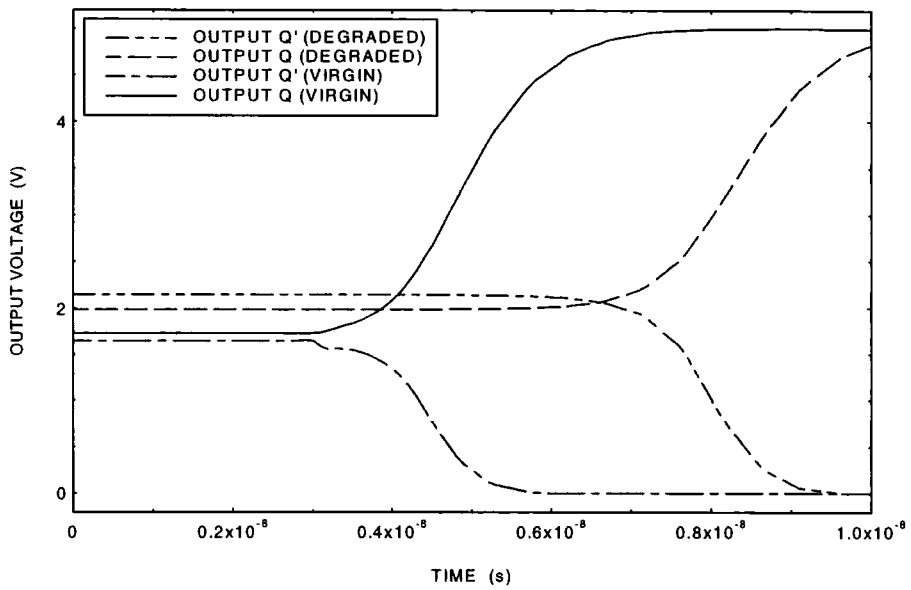


Figure 6.11 Resolving time simulations with and without degradation for DL1. (Process: EC/3, Device: 1/0.8)

The resolving times measured for the three latch circuits after hot-carrier degradation are tabulated below:

OUTPUT LEVEL	DL1	DL2	DL3
$\Delta V = 1$ V	7.67 ns	5.58 ns	13.0 ns
$V_{OH} \geq 3$ V & $V_{OL} \leq 2$ V	8.00 ns	5.83 ns	13.3 ns

Table 6.3 Resolving times measured for the three latches after hot-carrier degradation for the two output level conditions.

The results tabulated in table 6.3 indicate that the increase in resolving time for DL2 is very small where as the increase is substantially more for DL1 as expected, since this circuit had the highest stress. But we have a surprising result showing a disproportionate increase in resolving time for DL3, a 176.6% increase. The resolving times before and after the degradation for the three latches are plotted in the bar graph of figure 6.12.

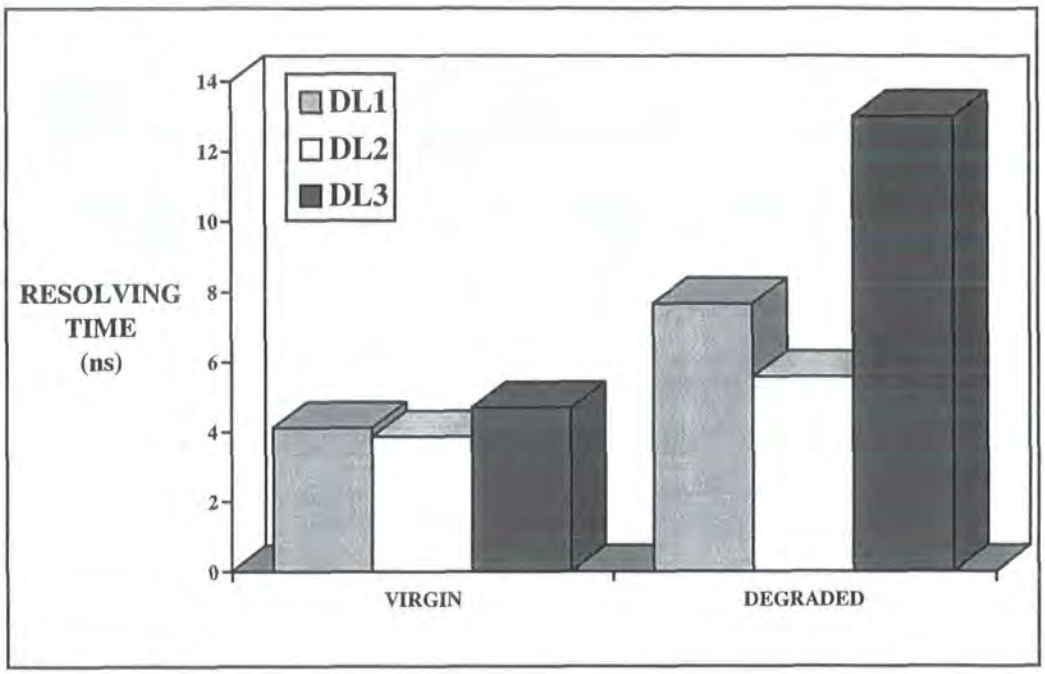


Figure 6.12 Resolving times with and without degradation for the three latches.

6.5.1 Variation of resolving time with SPICE parameter ABSTOL.

A number of simulations were carried out for determining the resolving time of the latch after forcing it into metastability. It was noted that for the older versions of PSPICE, when the value of ABSTOL option in the SPICE input file was varied or if the transient time step was varied (using .TRAN statement), the resolving times plotted were found to differ substantially. ABSTOL determines the *best accuracy of currents* and has a default value of 1 pA. This problem was due to the algorithm used by the SPICE program to force the nodal voltages to converge; a smaller error tolerance or smaller time step producing a different current and voltage convergence since the nodal voltages are very sensitive at the metastable state. The variations were found to be much more when the latch was forced into a metastable state by setting nodes to the metastable voltage at time t=0 and it was less sensitive when simulated with set-up time violations. The latest version of PSPICE which was used for most of our simulations for

the three selected latches, had the algorithm corrected and we have not experienced any change in the resolution of the time measured. We have also used the same values (ABSTOL = 1 pA and time step = 0.1 ns) for all the simulations. Assuming that the algorithm used by SPICE is reliable and it is sensitive enough to evaluate the nodal voltages and currents at the metastable region without causing any convergence problems, we expect to get consistent results for all the circuits simulated. The simulations were repeated using SPICE2G and HSPICE and in all the simulations, we obtained results which were comparable with our main simulations using PSPICE Version 6.2j [6.28].

6.5.2 Effects of threshold voltage variation on metastability

The metastability voltage V_m is dependent on the threshold voltages of the n- and p- transistors in the latch. It is possible that these parameters may also affect the metastability resolving of the latch circuits. A number of simulations were carried out with a range of threshold voltage values for the n- and p- devices. It was observed that the metastability voltage is shifted as expected from equation 6.6. But the relative effect of variation in resolving time was less than 3 % for a variation in V_{Tn} from 0.832 V to 0.50 V and 1.50 V and less than 2 % for a variation of V_{Tp} from -1.04 V to -0.50V and -1.50V. The best possible improvement in resolving time was obtained when the threshold voltages were set at 0.55 V and -0.55 V for the n- and p- MOS transistors respectively.

It was found from these simulations that a threshold voltage shift alone is not going to improve the metastability behaviour of the latch but in fact it may destabilise the latch by shifting the transition voltage too much from the mid point between V_{DD} and ground. Other parameters such as gain and capacitive loading must be adjusted in order to have an optimised latch circuit which can have a better metastable resolving capability. These findings will be further investigated in the next chapters.

6.6 Chapter summary

A flip-flop operated in the metastable region is found to be unreliable due to unusually long decision time encountered in fast submicron CMOS digital systems. The conditions under which the flip-flop tends to enter a metastable state has been

investigated. A number of bistable circuits were designed and simulations were carried out within the metastable window in order to determine the circuits which are more susceptible to metastable operation.

Using small signal analysis and employing analytical methods, it is possible to calculate the metastable voltage of cross coupled CMOS inverting devices. By pre-setting the inputs of these latches to the calculated metastable voltages, the latches were forced into metastable operation. Repeated simulations using this technique led to the determination of the metastable resolving time. The circuit design improvements to reduce the resolving time and hence improve the reliability of the circuits will be considered in chapter 7.

It was established from metastable state simulations for the designed latch circuits that threshold voltage for the MOS transistors affect the metastable region. By adjusting the threshold voltages for the n- and p- transistors it is possible to improve metastability resolving for the latch circuits simulated, even though these improvements were offset by the shift in the transition voltages of the latch circuits. Other design constraints such as noise margins must be also taken into account when adjusting the threshold voltages for the devices. The effects of improvements in the gain and the capacitive loading effects will be discussed in the next chapter as part of a general design improvement to reduce the metastability resolving time.

Chapter 7

Design Techniques for Reducing the Effects of Degradations and Improve Life-time

Hot-carrier degradation simulations performed on the three latch circuits in chapter five have revealed that the first latch DL1 has a higher average stress level compared to the other two latch circuits simulated. The transistors in this circuit experienced the most severe degradation during the simulation period resulting in the deterioration of the performance of the circuit. Metastability simulations in chapter six have shown that the resolving times of the circuits are affected by the hot-carrier degradation.

The stress levels for all the devices in the latch circuits have been measured and the average stress for a typical operating cycle determined. The devices having higher stress levels have been identified. It is possible to reduce the stress levels on identified highly stressed devices by design improvements and hence improve the life-time and these issues will now be addressed. The effect of metastability resolving of the improved designs will be also assessed.

7.1 Techniques for reducing the stress on circuit DL1

The highly stressed devices were identified as N5 and N6 having a stress level of 21.1 A/m each. Device N3 also has a higher than normal stress (9.9 A/m) and N1 has a normal stress level of 5.4 A/m. Devices N2 and N4 have negligibly small stress levels. It can be seen from the circuit diagram for DL1 shown in figure 7.1 that these transistors having high levels of stress are at the output node of the latch.

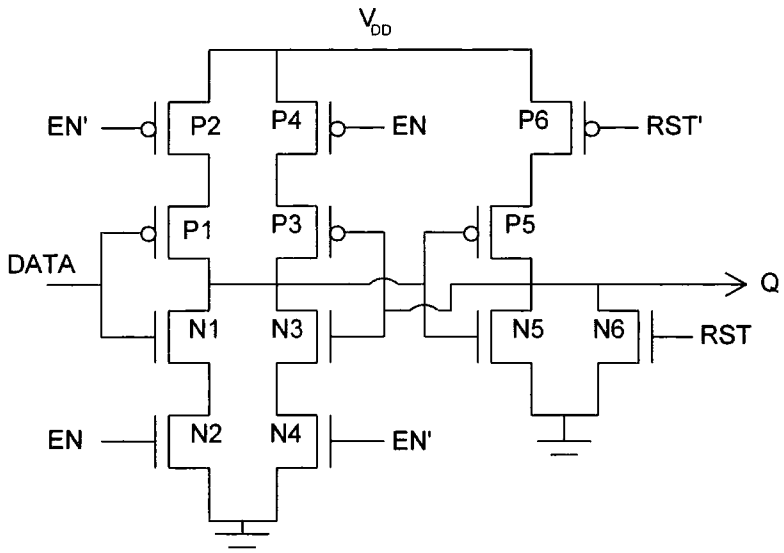


Figure 7.1 Circuit diagram for DL1. The transistors N3, N5 and N6 have higher levels of stress. (Technology EC/3, device N: 1/0.8)

It has been shown in chapter 3 that hot carriers are generated close to the drain of the nMOS device as the channel electric field has a pronounced peak in this region. While the drain voltage is *high* and the gate voltage is ramped *high*, hot electrons are generated in the channel due to impact ionisation. If we can reduce the peak of the channel electric field and move the peak away from the drain, the stress level and the hot carrier generation can be reduced. The devices N2 and N4 have very much reduced stress levels even though the drain currents are the same as that for N1 and N3 respectively since N1 is in series with N2 and N3 is in series with N4. The devices N2 and N4 are at the lower ends of the ladders and the *ON* resistance for N1 and N3 act as load at the drain end of these devices which has the effect of reducing the stress on these devices. Similar observations were also made for the other two latch circuits. The *ON* resistance of the upper device acts as a load spreading the electric field and hence diverting the peak away from the drain of the device for which the gate voltage is ramped.

7.1.1 Stress Reduction for N1 and N3

Since the stress level on N2 is very much lower than the normal stress, it is possible to reduce the stress on N1 simply by interchanging N1 with N2. A similar technique was used to reduce the stress on N3 by swapping N4 with N3 such that the *ON*

resistance of the upper device acts as a load for the device having higher stress level there by reducing the stress level.

It must be stressed that it is not always possible to reduce the stress on devices simply by swapping the devices; improvements are possible only when one of the devices has an inherent reduced stress level and happens to be at the lower end of the ladder of the series connected nMOS devices before the swapping. Since the devices are in series, the drain currents are the same for the devices; but the device for which the gate voltage is ramped will have the highest stress. A two-input NAND gate and a three-input NAND gate also will have similar stress levels as shown for the tri-state devices used in this circuit, but the order of the devices is irrelevant in this circuit as the logical inputs are equivalent.

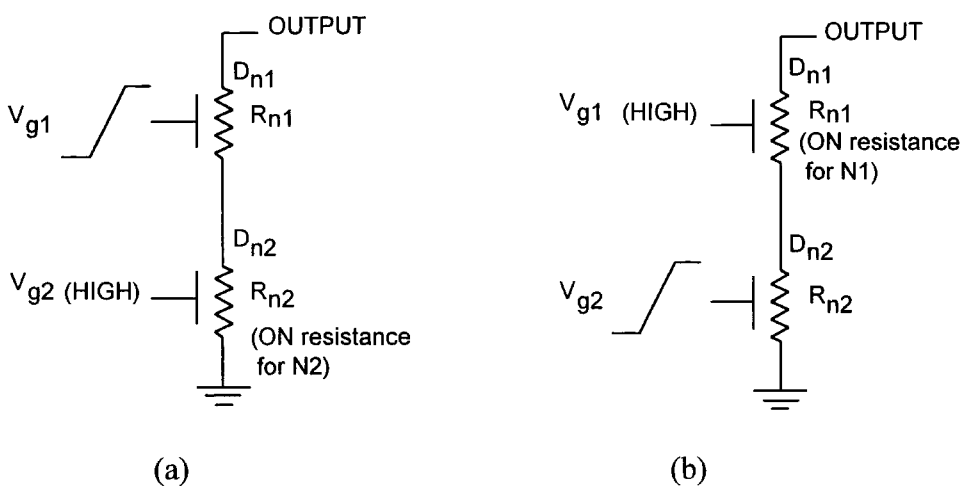


Figure 7.2 The tri-state devices used in the latch circuit (a) the series connected nMOS transistors before swapping and (b) after swapping.

For the tri-state circuit, the nMOS devices are in series as shown in figure 7.2(a) before the transistors are swapped. When V_{g2} is *high* the channel resistance R_{N2} is the *ON* resistance of N_2 and if V_{g1} is *low*, device N1 is *OFF* and has a very large channel resistance; V_{OUT} is *high* and V_{DN2} is approximately at ground potential and the full output voltage is dropped across R_{N1}. When V_{g1} is now ramped *high*, the peak of the field is at the drain end of N1 and will generate drain current and substrate current at high stress levels during a typical operation of the transparent D-type latch.

By exchanging V_{g1} and V_{g2}, we have the *ON* resistance R_{N1} as load to R_{N2} as shown in figure 7.2(b). When V_{g2} is ramped while V_{g1} is *high*, the *ON* resistance R_{N1} acts as a load for N2 which reduces the peak of the electric field near the drain of N2 and hence reduces the stress and the substrate current for N2.

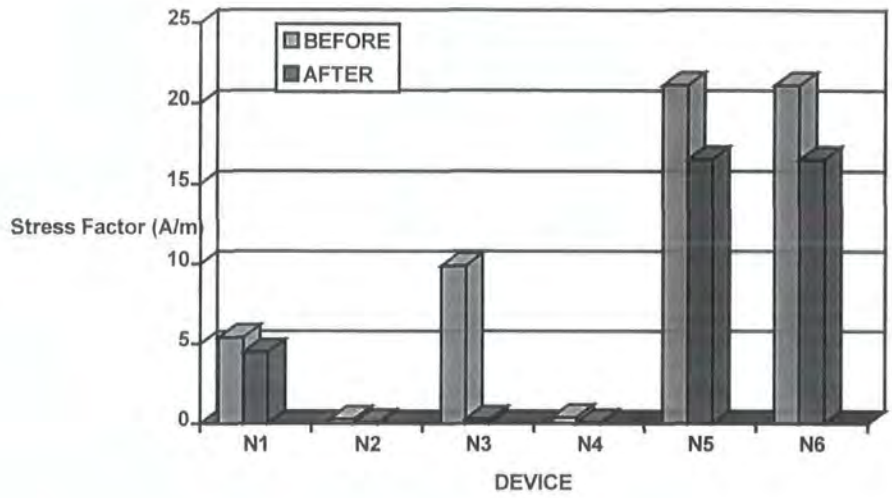


Figure 7.3 Bar graph showing the stress levels on all the devices in DL1 before after swapping of N1 with N2 and N3 with n4. (Technology: EC/3, Device N: 1/0.8)

It is also possible to reduce the stress on N3 in the second tri-state device by exchanging transistors N3 and N4. The circuit simulations have shown that this is an effective method for reducing the stress. The stress levels measured over a typical simulation cycle for all the devices in DL1 before and after the exchange of N1 with N2 and N3 with N4 are shown in a bar chart of figure 7.3.

Figure 7.3 shows that the stress levels on N1 and N3 have been lowered to 4.5 A/m from 5.4 A/m and to 0.3 A/m from 9.9 A/m respectively. It can also be noted that the reduction in stress levels in the previous stages due to the exchange of the devices have indirectly caused a reduction in the stress levels for N5 and N6.

7.1.2 Stress reduction for N5 and N6

Devices N5 and N6 are in parallel and it is not possible to reduce the stress on these devices using the technique described above as the output voltage is appearing across the drain and source of these devices. When we use the minimum dimensions allowed by the technology design rules, we have a very narrow channel, 1 micron width, for the transistors between the drain and the source making the current density and the electric field magnitudes very high. When the width of the devices N5 and N6 were doubled, the field lines get spread over a wider width and hence the impact ionisation per unit area of cross-section of the channel is reduced. The increase in width will give rise to an increase in peak saturation current for the device and the substrate current also is increased. But the substrate current generation is not increased proportionately as the electron temperature is lower in a wider device [3.4, 3.5] and hence the normalised substrate current generated also is reduced.

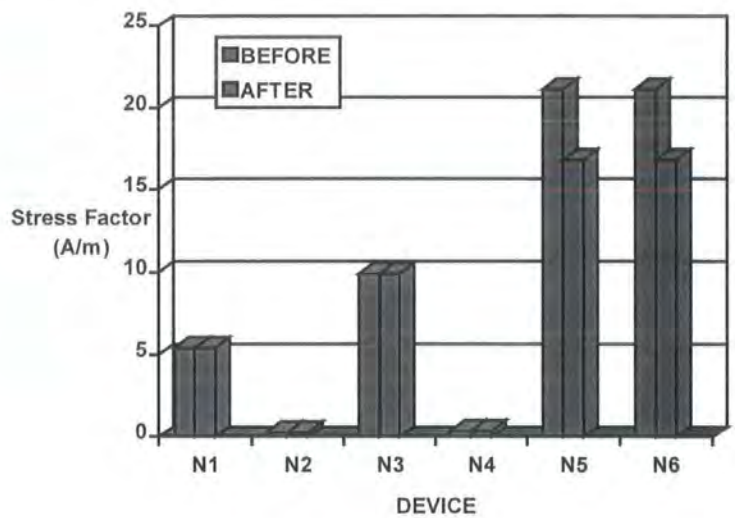


Figure 7.4 Stress levels for devices in DL1 before and after doubling of the channel widths for N5 and N6. (Technology: EC/3, New device dimensions are: N1, N2, N3, N4: W/L = 1/0.8 and N5,N6: W/L = 2/0.8)

The stress levels measured over a cycle before and after the doubling of the devices (N5 and N6) are shown in figure 7.4. It can be seen from figure 7.4 that the stress levels for N5 and N6 have been reduced to 16.8 A/m from 21.1 A/m by increasing the

channel width. The stress levels on these devices are still higher than the normal stress levels required for reliable operation of the latch over an acceptable life-time. Further stress reduction is possible for these two devices by increasing the channel length. An increase in channel length has the disadvantage of reducing the speed and this is a price we have to pay for improved reliability.

The channel lengths of the devices N5 and N6 were increased to 1.5 μm and the circuit was simulated to measure the stress over a cycle. The increase in channel length of the two devices may not affect the overall response of the latch adversely as we have already doubled the channel width for these devices while all other devices in the circuit have normal widths. The improvements in the stress levels for the devices have been determined using circuit simulations and was found that the stress levels have been reduced to 11.5 A/m from 16.8 A/m due to the increase in length.

7.1.3 Final improved design for DL1

All the techniques discussed above have been incorporated into the new design and the stress levels for all the devices in the circuits have been measured over a typical operating cycle. The device N1 was swapped with N2 and the device N3 was swapped with N4; devices N5 and N6 have been redesigned using double widths and increased channel lengths. Improvements in stress levels have been plotted in figure 7.5 and Table 7.1 shows the stress factors and the life-time for DL1 before and after the design modifications.

The life-time for each of the transistors was calculated using the life-time model developed in chapter 3 and for AC stress simulations, it is given by equation (3.50),

$$\tau = H(\Delta D / D)_f \frac{\Delta D}{D})_f W(\Sigma I_{SUB})^{-m}(\Sigma I_{DS})^{m-1}$$

where the degradation $(\Delta D/D)_f = 0.1$ or 10% for failure, the drain current (ΣI_{DS}) and the substrate current (ΣI_{SUB}) are summed over one AC cycle. The results tabulated in table 7.1 show that this circuit has very high stress levels contributing to reduced life for the devices. The transistors N5 and N6 at the output nodes are affected most and the design

improvements were concentrated in reducing the stress on these devices. Even though we have achieved a stress reduction of about 50% for these devices, the stress levels remain unacceptably high leading to an early failure of these devices.

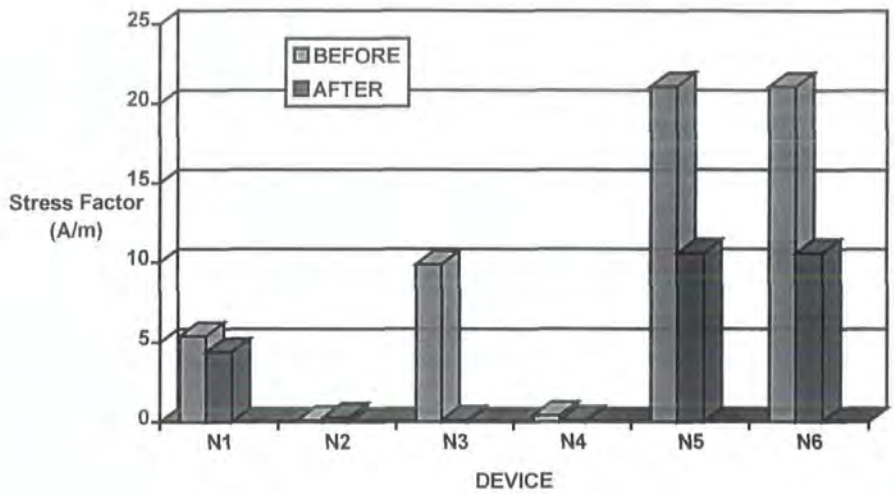


Figure 7.5 Stress factors for devices in DL1 before and after all the improvements in the design. (Technology: EC/3, New device dimensions are: N1, N2, N3, N4: W/L = 1/0.8 and N5,N6: W/L = 2/1.5)

	Stress factors (A/m)		Life-time (Hours)	
Device	Before	After	Before	After
N1	5.4	4.4	1.7×10^{5}	3.9×10^{5}
N2	0.1	0.3	1.0×10^{10}	6.4×10^{8}
N3	9.9	0.1	1.2×10^{3}	9.6×10^{8}
N4	0.4	0.1	1.4×10^{7}	9.8×10^{8}
N5	21.1	10.6	2.1×10^{3}	5.5×10^{3}
N6	21.1	10.6	2.1×10^{3}	5.5×10^{3}

Table 7.1 Stress factors and life-time for DL1 before and after design modifications. (Technology: EC/3, Device size has been adjusted to reduce stress)

Based on the stress levels on the devices, the device parameters were degraded and the circuit re-simulated to determine the deterioration in the timing and propagation delays for the circuit. Quantitative analysis of the improvements in timing parameters will be discussed in the next chapter.

7.2 Techniques for reducing the stress on DL2

The devices in the latch circuit DL2 were found to have relatively lower stress levels and the average stress on DL2 also is the lowest of the circuits examined. However it is possible to reduce the stress levels on the devices further and hence to improve the circuit life-time. Circuit simulations using the substrate current model has identified the devices having higher stress and the improvements in the circuit design are discussed below:

7.2.1 Stress reduction for N1

Stress level on N1 was higher than normal at 7.7 A/m and the stress on this device can be reduced by inserting a single n-channel transistor between the output rail and the drain of the n-channel transistor of the inverter with the gate of the upper n- transistor permanently connected to the positive rail of the power supply and the input connected to the gate of the lower transistor. The widths of the n- and p- transistors were doubled and the lengths of the n- transistors were increased to 1.5 μm. Simulations have shown that the stress level for the device has been lowered to 0.1 A/m from 7.7 A/m.

7.2.2 Improvements for devices N2 and N3

Transistors N2 and N3 are the series connected devices for the two input NAND gate and it was observed that N2 had a higher stress level (6.5 A/m) while N3 had very low stress (0.7 A/m). Even though, the stress on N2 is at an acceptable level, it can still be improved because of the inherent lower stress on N3 simply by exchanging N2 and N3.

The device having higher stress was brought to the lower end of the series ladder and the *ON* resistance for the device with lower stress was used as extra load on the drain to reduce hot-carrier generation. The widths of the transistors N2 and N3 were doubled and the lengths were increased to 1.5 μm, further reducing the stress levels to 3.2 A/m and 0.3 A/m respectively.

7.2.3 Improvements for N4 and N5

The stress on N4 was found to be 7.2 A/m and that for N5 was only 0.8 A/m. It is also noted that the gate voltage for N4 is ramped while that for N5 is *high*. The stress level on N4 has been reduced by exchanging N4 with N5 without affecting the stress on N5. Further reduction in stress was achieved by doubling the widths of the transistors and increasing the lengths of N4 and N5 to 1.5 μm. The improved stress levels on N4 and N5 are found to be 2.2 A/m and 0.4 A/m respectively.

7.2.4 Improved designs for N6 and N7

The transistor N6 has a higher stress level compared to N7, but the gate voltages for both devices are ramped during the normal operation of the latch. Hence the exchange of N6 with N7 will not improve the stress levels. A simulation with the exchanged devices showed an increase in stress for the upper device. The best solution to reduce the stress was to insert a single n- channel transistor between the output node and the drain of the upper n- transistor of the NAND gate; the gate of this transistor was permanently connected to the positive supply rail. This extra load on the drain of the highly stressed device effectively lowered the stress. Further stress reductions were achieved by doubling the widths of both transistors and increasing the lengths of the n- transistors to 1.5 μm. The stress level for N6 has been lowered to 0.1 A/m and that for N7 has been increased by a small amount to 0.7 A/m.

7.2.5 Improvements for N8

The device N8 was found at the upper end of the series connected n- devices and has the highest stress (13 A/m); N9 and N10 have very low stress levels. The stress on N8 can be lowered by exchanging it with N10 which is at the lower end of the series ladder. The gate input to N10 is held high during normal operation of the latch and hence will not increase the stress on this device by moving it to the upper end of the ladder. The device widths and lengths were also increased to 2 μm and 1.5 μm respectively, achieving further reduction in stress levels. The improved stress level for N8 was found to be 1.8 A/m, a substantial stress reduction and that for N9 and N10 were 0.1 and 0.6 respectively.

7.2.6 Evaluation of the improvements

The final design for DL2 was simulated with all the improvements and the stress levels for each device was measured. The results were plotted and compared with the stress levels plotted for the latch before the improvements and is given in figure 7.6.

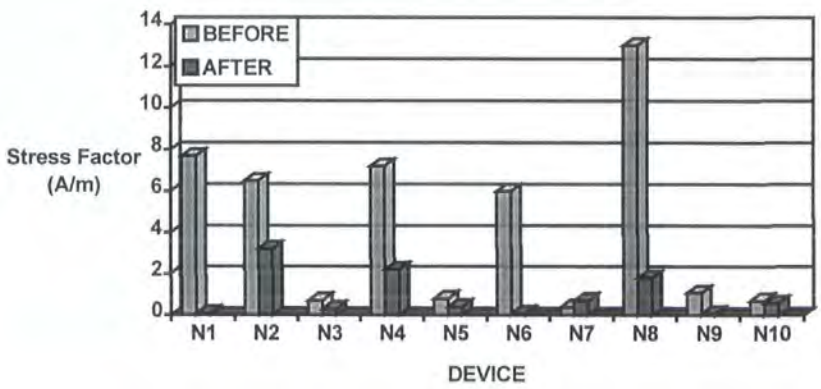


Figure 7.6 Stress factors for DL2 before and after design changes.

(Technology: EC/3, Device size has been adjusted to reduce stress)

It can be seen from the bar-graph and the simulation results shown in table 7.2 that the transistor N8 had the highest stress level (13 A/m) before design improvement. Since this device is at the output node of the latch circuit, it will suffer maximum degradation and can lead to circuit failure. With the design improvements, we have reduced the stress on this device to 1.8 A/m and the life-time also has been improved by a factor of 100. The overall improvement in the life-time of the circuit will be evaluated in the next section of this chapter.

	Stress factors (A/m)		Life-time (Hours)	
Device	Before	After	Before	After
N1	7.7	0.1	5.2×10^{3}	4.1×10^{10}
N2	6.5	3.2	1.8×10^{4}	1.4×10^{5}
N3	0.7	0.3	1.3×10^{7}	2.0×10^{8}
N4	7.2	2.2	1.4×10^{4}	4.5×10^{5}
N5	0.8	0.4	8.4×10^{6}	7.8×10^{7}
N6	6.0	0.1	9.1×10^{4}	3.1×10^{9}
N7	0.4	0.7	2.5×10^{8}	1.8×10^{7}
N8	13	1.8	1.4×10^{4}	1.1×10^{6}
N9	1.1	0.1	1.7×10^{7}	2.4×10^{9}
N10	0.7	0.6	8.5×10^{7}	2.3×10^{7}

Table 7.2 Stress factors and life-time for DL2 before and after design modifications. (Technology: EC/3, Device size has been adjusted to reduce stress; New device dimensions are: N1:2/0.8 N2, N3, N4, N5: 2/1.5 N6, N7, N8, N9, N10: 3/1.5)

7.3 Improvements for Latch Circuit DL3

The stress simulations have shown that the devices N3 and N5 have higher stress levels of 8.7 A/m and 10.6 A/m respectively. The stress levels on these devices must be reduced by design improvements in order to improve the reliability of the circuit. Reducing the stress on these devices will also reduce the average stress on the latch and hence improve the life-time of the latch. We can also try to reduce the stress on device N1 from 5.5 A/m to improve the overall performance of the circuit. The stress levels on N2 and N4 are very low and so no improvements are needed for these devices.

7.3.1 Stress reduction for N3

The devices N3 and N4 are the series connected n- transistors for the two-input NAND gate. Since N4 has a negligibly small stress and the gate voltage is held *high* during normal operation, it is possible to reduce the stress on N3 by interchanging its position with N4. The *ON* resistance for the upper device acts as a load for the device having higher stress thereby reducing the stress. Further stress reduction was achieved by doubling the widths of the devices in the NAND gate and increasing the channel length to 1.5 μm.

7.3.2 Improvements for N5

The device N5 is the n- transistor for the inverter at the output of the latch and has high stress level. The stress level on this device was reduced by doubling the device widths and by increasing the channel length to 1.5 μm. The stress simulations have shown that the stress has been reduced to 7.3 A/m. The stress level on N5 can be reduced further by inserting a single *ON* n-channel transistor in series with the existing n- transistor at the drain end.

7.3.3 Improvements for N1

The transistor N1 is at the *DATA* input of the latch and experiences high stress level of 5.5 A/m. This stress was reduced by doubling the width and increasing the length to 1.5 μm and the stress level has been reduced to 3.3 A/m and the corresponding improvement in life-time is 66600 hours from 37600 hours, an improvement of 77%.

7.3.4 Simulation of improved design

The final design was simulated and the stress levels determined. The stress levels before and after the design improvements are shown in figure 7.7 and the improvements in life-time for the devices in the circuit are given in table 7.3.

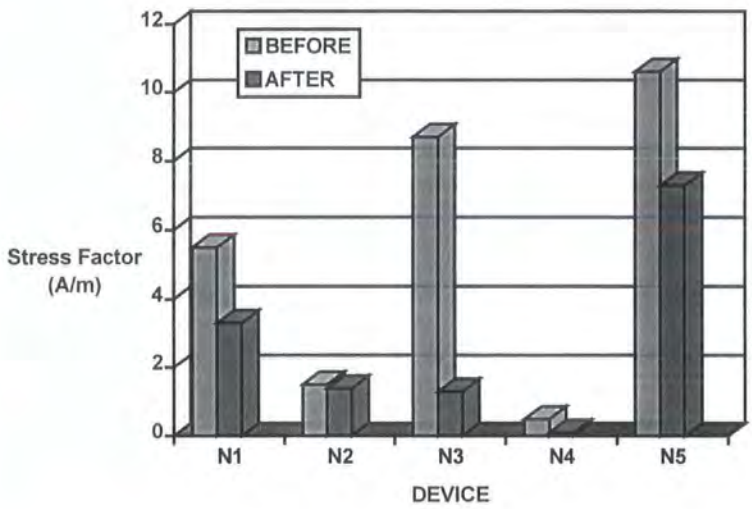


Figure 7.7 Stress factors for DL3 before and after design changes

(Technology: EC/3, Device size has been adjusted to reduce stress)

It can be seen from table 7.3 that the highest stress is experienced by the transistor N5 which is at the output node of the latch. Our design improvements were aimed at improving the stress on this device as well as that on N3. We have reduced the stress on N3 to 1.3 A/m and the stress on N5 has been lowered to 7.3 A/m. We have not achieved

the level of improvement in the life-time for this device by reducing the stress and so this device is critical for failure of the circuit.

	Stress factor (A/m)		Life-time (Hours)	
Device	Before	After	Before	After
N1	5.5	3.3	3.8×10^{4}	6.7×10^{4}
N2	1.5	1.4	2.6×10^{5}	4.9×10^{5}
N3	8.7	1.3	3.1×10^{4}	1.1×10^{6}
N4	0.5	0.1	1.9×10^{8}	3.1×10^{10}
N5	10.6	7.3	5.5×10^{3}	1.8×10^{4}

Table 7.3 Stress factors and life-time for DL3 before and after design modifications. (Technology: EC/3, Device size has been adjusted to reduce stress)

7.4 Life-time and timing parameters for the Latches

	Average Stress factor (A/m)		Life-time (Hours)	
Circuit	Before	After	Before	After
DL1	9.7	4.4	1.4×10^{4}	1.7×10^{5}
DL2	4.4	0.9	1.5×10^{5}	3.8×10^{7}
DL3	5.4	2.7	5.9×10^{4}	8.4×10^{5}

Table 7.4 Stress factors and life-time for the latch circuits before and after design modifications. (Technology: EC/3, Device size has been adjusted to reduce stress)

The stress factors for the devices in the three latch circuits were determined using stress simulations over a typical AC cycle. The average stress factor for each of the circuit

was determined by averaging of the stress levels on all devices in the circuit. The life-time for each of the latch circuits was calculated using the average values of drain currents and substrate currents over an AC cycle for all devices in the latch. These values are tabulated in table 7.4.

When a circuit is operated normally, the end of life may be due to a critical, highly-stressed device for which the timing parameters have been degraded due to hot carrier effects. The stress level and the relative position of the device in the circuit can be critical for such circuits. If the device under stress is at the output node of the latch circuit, the *rise* and *fall* times and the propagation delays are affected adversely; if the device is at the *data* input path, the propagation delays are also affected. The stress on the identified critical devices and the corresponding life-times for the circuits are given in table 7.5.

		Max. Stress factor (A/m)		Life-time (Hours)	
Circuit	Critical Device	Before	After	Before	After
DL1	N5	21.1	10.6	2.1×10^3	5.5×10^3
DL2	N8	13	1.8	1.4×10^4	1.1×10^6
DL3	N5	10.6	7.3	5.5×10^3	1.8×10^4

Table 7.5 Maximum Stress factor on the critical device and life-time for the latch circuits before and after design modifications. (Technology: EC/3, Device size has been adjusted to reduce stress)

A comparison of the life-times shown in table 7.4 and 7.5 for the latch circuits, it is clear that the life-time evaluated using the stress on the critical device in a latch is much shorter than that calculated using the averaged stress value. This result shows that the eventual failure of the circuit may occur relatively earlier if the critical device in the circuit degrades faster than the average degradation rate. Hence it is very important to assess the stress levels on identified critical device and to address special techniques to reduce the stress for this device.

7.4.1 Determination of timing parameters for the modified latches

The modified latch circuits were simulated to determine the propagation delays and other timing parameters and are tabulated in table 7.6.

Parameter	TRI-NOR (DL1)	NAND-N3 (DL2)	TX-NAND (DL3)	UNIT
t_r	1.23	0.96	0.69	ns
t_f	0.98	1.03	0.71	ns
t_{pd}	1.86	1.46	1.20	ns
t_{su}	1.60	1.60	0.75	ns
t_h	0.0	-0.50	0.0	ns
T_{min}	7.0	4.5	5.0	ns
f_{max}	143	222	200	MHz
t_c	1.60	1.10	0.75	ns

Table 7.6 Timing parameters measured for the 0.7 micron *modified* design (Technology: EC/3, Device size has been adjusted to reduce stress)

Table 7.6 must be compared with the results of simulation for the latch circuits before design modification tabulated as table 4.7 in chapter 4. The tabulated results show an improvement in rise-time for all three circuits. This is due to an increase in device width for the p- channel transistors at the output nodes in order to maintain layout symmetry as we have increased the width of the n- transistors; there is a small decay in the fall-time which is due to *on* resistance of the n- transistor at the drain of the device and the increase in channel length. Propagation delay has increased for the circuits and a fall in circuit speed also is experienced. These changes in circuit timing parameters are expected for the modified circuits which are not significant for the reliability of the circuit. The

degradations in circuit characteristic timing parameters with time and the reliability of the circuits before and after design improvements will be compared and analysed in the next chapter.

7.4.2 Improvements in Resolving time

The changes in metastability resolving for the three latch circuits were estimated by further resolving time simulations as discussed in chapter six. The results of a comparative study of the resolving times determined for the latch circuits before and after the design modifications are tabulated in table 7.7.

Circuit	Resolving time (before) (ns)	Resolving time (after) (ns)
DL1	4.1	4.2
DL2	3.9	4.6
DL3	4.7	3.3

Table 7.7 Resolving times for the three latch circuits before and after design improvements.

It can be seen from the table that DL1 shows no significant improvement in the resolving time while DL2 shows an increased resolving time after the design changes. The increase in resolving time for DL2 is due to the increase in the parasitic capacitance at the circuit nodes as a result of increase in device dimensions introduced to reduce hot-carrier stress. These nodal capacitance must be charged or discharged during AC operation giving rise to increased resolving time. The hot-carrier reliability of the circuit has been improved but it may affect the metastability resolving of the latch if the circuit is operated within a fast VLSI circuit. The resolving time for DL3 has improved to 3.3 ns from 4.7 ns; hence this circuit can be designed as part of a fast VLSI circuit if the circuit application can tolerate the degradation in fall-time and propagation delays due to hot-carrier stress for prolonged periods.

7.5 Chapter Summary

The substrate current model and the AC. degradation model have been effectively employed for identifying the devices having higher stress levels. It was revealed that the position of the device in a latch circuit and the sequence at which the devices are operated have a major influence on the generation of substrate current and hence the degradation. A number of techniques have been employed to reduce the stress and degradation of the identified highly stressed devices in the circuits. It has been shown that it is possible to reduce the average stress on all three latch circuits and hence improve the life-time.

The improved designs of the latch circuits were simulated to determine the propagation delays and timing parameters. The fall times and propagation delays were adversely affected by the design changes to improve hot carrier stress on the devices. A small increase in propagation delays and a decrease in circuit speed are the price we have to pay for improving the reliability of the latch circuits. The results of the stress reduction and the improvements in hot carrier reliability will be quantified in the next chapter.

Chapter 8

Quantitative Analysis of the Results and the Reliability Improvements in the selected Bistables

A number of techniques have been employed in chapter 7 for reducing the stress on devices in the three latch circuits. The simulations of the improved designs of the circuits show an improvement in the life-time of the devices used in the circuits. Average stress level on the devices in each circuit was used to evaluate the life-time of the circuits.

The end of an operational life of a circuit may be due to the failure of the circuit to meet the characteristic timing parameters of the circuit as a result of the degradation of one or more of the highly stressed critical device. A device is considered critical if it is in the signal path of the circuit which can give rise to increased propagation delays and transition times. Our simulations have shown that the *most critical device* in a bistable can be found at the output node of the latch circuit. There are two main reasons for this: when the bistable is operated under dynamic conditions, the gate of the output device experiences a constantly changing voltage and the drain-to-source voltage of this device is also changing, giving rise to the condition necessary for peak substrate current generation as discussed in chapter 3 and we have shown in chapter 5 using

characterisation of degradation effects that the rise and fall times of a bistable circuit are affected to a maximum degree when the device at the output degrades faster than other devices in the circuit. Hence the circuit life-time for the three latch circuits were also evaluated using the stress factor on the most critical device in that circuit.

The effect of circuit performance degradation due to hot-carrier stress has been evaluated for the latch circuits. The suggested improvements in the latch circuits to reduce hot-carrier stress may have reduced the speed and performance of the virgin circuits before hot-carrier stress, but the life-time and the hot-carrier reliability of the circuits have been improved.

In this chapter we will evaluate the reduction in stress factors for the devices and the average stress for each circuit with the design improvements. We will evaluate quantitatively the effects on performance for the three virgin latch circuits with all the design improvements to reduce the hot-carrier stress. We will also evaluate the degradation in performance when the improved circuits are operated normally and compare this to performance degradation prior to circuit modification. Improvements in reliability and life-time are also assessed. The effects on metastable state resolving times for the improved designs are also evaluated.

8.1 Reduction in Stress Factor

The improvement in the life-time and the reliability of the bistables were assessed by evaluating the reduction in average stress levels as a result of design improvements. The average stress factors for the three latch circuits before design improvements are 9.7 A/m, 4.4 A/m and 5.4 A/m respectively. The relatively higher stress level on DL1 has resulted in a higher rate of degradation and hence a shorter life-time for this circuit. The design techniques suggested have reduced the stress levels on all three circuits; even then the average stress on DL1 remain relatively at a higher level.

The second latch circuit, DL2, has the lowest stress level compared to the other two circuits. Further improvement in the stress levels were achieved by design

improvements and the stress factor has been lowered to 0.9 A/m. The stress level for the third latch circuit was also lowered to an acceptable value (2.7 A/m) and the improvement in the reliability will be assessed in this chapter. The improvements in stress factors are quantified below:

Reduction in stress factor for DL1 = 55%
Reduction in stress factor for DL2 = 80%
Reduction in stress factor for DL3 = 50%

As we have stated before, the failure of a latch may be due to a critical device having higher stress degrading at a faster rate than others. We have identified the critical device in the latch circuits and using characterisation of degradation effects discussed in section 5.3 (Chapter 5), it is possible to evaluate the failure of the critical device leading to circuit failure. The reliability calculated using the average stress factors for all devices in a circuit may give a rather optimistic value of the reliability which may be misleading. The stress level and the life-time of the circuit evaluated based on the critical device in each of the latch circuit was used to quantify the improvements and to give us a more realistic value for the reliability and are listed below:

Reduction in stress factor for DL1 (critical device: N5) = 50%
Reduction in stress factor for DL2 (critical device: N8) = 86%
Reduction in stress factor for DL3 (critical device: N5) = 31%

We have achieved significant improvement in the stress factors for the critical devices in the three circuits. These improvements will be reflected as life-time and reliability improvements for the circuits and are discussed next.

8.2 Improvements in Life-Time

We have discussed in chapters five and seven, how we evaluated the life-time of all the devices in the three selected latch circuits using the life-time model developed in chapter three. The normal operating life-time of each of the latch circuits was also evaluated using expression (3.50) and for this evaluation we have used the average stress

factors for all the devices in the latch circuit summed over a dynamic operating cycle. The life-times for the circuits evaluated are shown in table 7.4. This table also shows the average stress factors for the circuits after design modification and the corresponding life-times. The improvements in the life-times for the latch circuits after the design modifications are listed below:

Improvement in life-time for DL1 = 1100%
Improvement in life-time for DL2 = 2500%
Improvement in life-time for DL3 = 1300%

As can be seen from the bar charts in figures 7.5 to 7.7, the magnitudes of the stress levels for some of the devices in the circuits are at least a hundred times lower than that for the devices at the output nodes, the averaging of the stress levels for all the devices may give rise to an unrealistically optimistic value for the life-times calculated. Hence we have also determined the life-times of the circuits using a second method; by evaluating the life-time of the critically stressed device in each circuit which can lead to the eventual failure of the circuit and are given in table 7.5. The improvement in life-times were now evaluated based on these results which could give us a more realistic value and these are listed below:

Improvement in life-time for DL1 (critical device: N5) = 162 %
Improvement in life-time for DL2 (critical device: N8) = 7800 %
Improvement in life-time for DL3 (critical device: N5) = 227 %

Improvements of 162% and 227% in the expected life-time of the two circuits DL1 and DL3 respectively are practically achievable as these devices are experiencing higher levels of stress before design modifications and hence had relatively short life-times. An improvement in life-time of 7800% for DL2 needs to be accepted with caution and in the final analysis, we may have to evaluate the life-time for DL2 using an average value of stress for a number of devices having higher levels of stress. Hence we have used a series model for the evaluation of the reliability of the latch circuits and is discussed in the next section.

8.3 Reliability Improvements

The reliability of a circuit having constant failure rate has been defined as (2.1),

$$R(t) = \exp(-t/\tau)$$

where τ is the life-time of the circuit. The reliability of the circuits are evaluated using the life-times calculated in chapter 7. The normal time-to-fail was defined on the basis of a deterioration in drain current by 10% and for the latch circuits, this was determined as 3000 hours of operation at maximum stress levels (defined in chapter three as the peak of the substrate current model). The reliability of each of the latch circuits was evaluated based on the failure of the critically stressed device in each circuit tabulated in table 7.5.

Reliability R(t) evaluated at the end of 3000 hours of operation for the three latch circuits before and after the design improvements to reduce the hot-carrier stress are listed below:

Reliability for DL1 (before modification) [t=3000 hours] = 24%
Reliability for DL1 (after modification) [t=3000 hours] = 58%

The life-time of the device was only 2100 hours before the design modifications and so the circuit would have failed before 3000 hours. With the design improvements to reduce the hot-carrier stress, we have achieved a reliability improvement of 34% for this circuit at the end of 3000 hours of operation. The reliability for the other two circuits are 81% and 58% before and 99% and 85% after the design modifications respectively.

The reliability of the circuits were also evaluated based on the average stress factors and the corresponding life-times evaluated in chapter seven (table 7.4). The

average life-times for the circuits were found to be close to 5 years and so the reliability was evaluated at t = 5 years for all the circuits and are tabulated in table 8.1.

	Reliability (t = 5 years) (%)	
Circuit	Before modification	After modification
DL1	4	77
DL2	75	99
DL3	47	95

Table 8.1 Reliability for the three circuits before and after design improvements.

It can be seen from the table that the reliability of DL1 is lowest (4%) and it would have failed before the 5 year period. After the design modifications, the reliability has improved dramatically by 73%. The reliability for DL2 and DL3 are much higher even before the design modifications; it was further improved by 24% and 48% respectively by design modifications to reduce hot-carrier stress.

8.3.1 Reliability Analysis using Series Reliability Model

The two methods described in the last section for the evaluation of the reliability for the latch circuits may give unrealistically low (for the first method) or high (for the second method) values. These two methods can be useful as a first order analysis to compare the life-times and the reliability of two or more circuits. A more realistic approach is by determining the reliability at the lowest level (transistor level) for all the devices in the signal path and proceeding through intermediate levels until an estimate of the system reliability is obtained at the (system (circuit) level. The reliability of the circuits were evaluated using series/ parallel model discussed in chapter 2. The signal path for the latch includes a number of nMOS devices in series or parallel. By analysing the reliability of individual devices and then evaluating the reliability of the latch circuits using equation (2.7) [8.1, 8.2], we have a better model for the reliability of the circuit

when operated under hot-carrier stress. We have assumed that any early failure has been eliminated using burn-in. Hence the degradation rate during useful life-time is considered to be constant leading to device failure as shown in the bath tub curve.

At the lowest level, the forward signal path for DL1 can be considered as a number of nMOS devices in series as shown in figure 8.1. Using the life-times for the devices N1, N2 and N5, the reliability of the circuit was evaluated using the series reliability model.

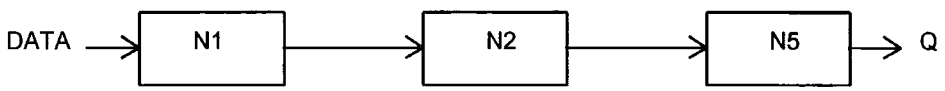


Fig 8.1 Series reliability model for latch DL1

Reliability for DL1 (before modification) [t=3000 hours] = 23%
Reliability for DL1 (after modification) [t=3000 hours] = 58%

The reliability for DL2 and DL3 were calculated using the series models shown in figures 8.2 and 8.3 respectively.

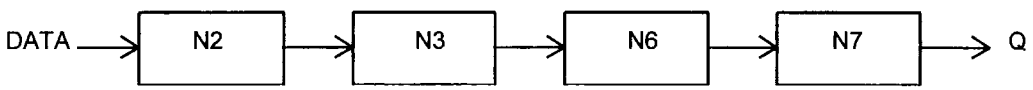


Fig 8.2 Series reliability model for latch DL2

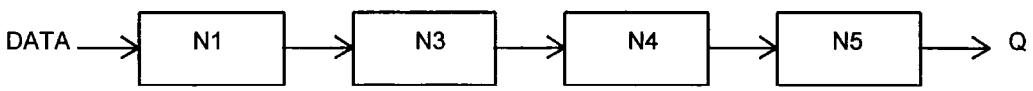


Fig 8.3 Series reliability model for latch DL3

Reliability for DL2 (before modification) [t=3000 hours] = 82%
Reliability for DL2 (after modification) [t=3000 hours] = 98%
Reliability for DL3 (before modification) [t=3000 hours] = 49%
Reliability for DL3 (after modification) [t=3000 hours] = 81%

These results calculated using the series reliability model are within 10% of the results obtained in the first method. Hence we can use the first method as a fast first order approximation to evaluate and compare the reliability of a number of circuits.

8.4 Effect on performance of the latch circuits

The performance of the latch circuits were determined before and after hot-carrier stress for a pre-determined period. We have found that the first latch having higher than normal stress failed before 3000 hours of operation and so this period of stress was taken as standard for all the circuits.

Parameter	TRI-NOR (DL1)		NAND-N3 (DL2)		TX-NAND (DL3)		UNIT
	Virgin	Stressed	Virgin	Stressed	Virgin	Stressed	
t_r	1.23	1.24	0.96	0.96	0.69	0.71	ns
t_f	0.98	1.10	1.03	1.05	0.71	0.78	ns
t_{pd}	1.86	2.02	1.46	1.49	1.20	1.30	ns
t_{su}	1.6	1.7	1.6	1.6	0.8	0.8	ns
t_h	0.0	0.0	-0.5	-0.5	0.0	0.0	ns
T_{min}	7.0	7.5	5.0	5.0	4.5	5.0	ns
f_{max}	143	133	200	200	222	200	MHz
t_c	1.6	1.7	1.1	1.1	0.8	0.8	ns

Table 8.2 Timing parameters measured for the 0.7 micron *improved* design before and after hot-carrier stress (Technology: EC/3, Device size adjusted to reduce stress)

The degradation in circuit performance was determined for each circuit after the stress period. The results were compared with those set of data from the re-designed circuits with reduced stress levels. The data shown in table 8.2 indicate that the effect of degradation on the improved circuits are very much less compared to that for the circuits before modifications shown in table 5.2 (chapter 5).

A detailed comparative study of the degradation effects on the circuit performance and the characteristic timing parameters have been carried out for the three latch circuits designed using 0.7 micron CMOS technology (EC/3) design rules using the simulation results tabulated in table 8.2 after the design modifications with that in table 5.2 (chapter 5) before design modifications. Our findings are discussed below:

8.4.1 Transition times

The deterioration in rise and fall times for the latch circuits were compared before and after design improvements to reduce hot-carrier stress. It is expected that the degradation in transition times for the improved circuits will be less than that before the modifications.

The degradation in *rise time* with hot-carrier stress has been very small for the circuits before and after the design modifications, only less than 1% in both cases. This result is not surprising as we have considered the degradation in the device parameters for the n- devices and the rise time is controlled by the p- devices for which the hot-carrier stress is negligible for the current technology. The degradation in fall time has been affected for all the circuits due to the deterioration of the n- devices and we quantify these findings:

The degradation in *fall time* before design modification for DL1 = 22%
The degradation in *fall time* after design modifications for DL1 = 12%

We have achieved an improvement in the fall time of 10% after the design modifications for DL1 when the circuit is operated normally for 3000 hours.

The degradation in *fall time* before design modification for DL2 = 5%
The degradation in *fall time* after design modification for DL2 = 2%

The second latch has the least degradation in fall time over a 3000 hours of operating time and we have reduced the stress further and hence the fall time has improved by 3%.

The degradation in *fall time* before design modification for DL3 = 18%
The degradation in *fall time* after design modification for DL3 = 10%

An improvement of 8% has been achieved for the third latch for the same operating period.

8.4.2 Propagation Delay

The propagation delay for all three latch circuits were affected by the hot-carrier stress and the decay in propagation delay before and after design modifications are listed below:
The degradation in *propagation delay* before design modification for DL1 = 17%
The degradation in *propagation delay* after design modification for DL1 = 9%

An improvement in propagation delay of 8% has been achieved for the first latch circuit by improving the design to counter hot-carrier degradation effects. The improvements in propagation delay for latch circuits DL2 and DL3 are 1% and 2% respectively. The improvements are relatively small for DL2 and DL3 as these circuits have lower levels of average stress and hence the improvements are also small.

8.4.3 Operating Speed

Even though there is a drop in the maximum operating frequency for each of the improved designs of the bistables, it is demonstrated that the improved designs have reduced hot-carrier stress and hence the degradation with operating time of the circuit speed has been minimised. The degradation in circuit speed for an operating life of 3000 hours for DL1 is found to be 13% before design changes, where as we have brought down this to 7% for the improved circuit; a gain of 6%!

The corresponding improvements in operating speed degradation for DL2 and DL3 are 11% and 10% respectively for an operational period of 3000 hours.

8.4.4 Critical Window for Metastability

The critical window for metastability is an important parameter for the latch and we now investigate the effect of design improvements on this parameter. The degradation in critical window for DL1 is 17% before the design improvements and 6% after; an improvement of 11%. The corresponding improvements for DL2 and DL3 are 0% and 33% respectively. We have noted that the stress level on DL2 was the minimum and the design improvements have managed to reduce the stress further but failed to register any appreciable improvement in this parameter, while DL3 has the best improvement. By reducing the critical window for metastability, we have reduced the interval during which the output logic state of the circuit may not be well defined leading to a circuit failure and hence the reliability of the circuit has been improved.

8.5 Conclusions and Chapter Summary

We have assessed the reduction in stress levels for the selected bistables as a result of the design improvements in order to reduce hot-carrier degradations. The improvement in life-time of the circuits as a result of stress reduction has also been evaluated. The improvement in life-time is used to assess the reliability improvements for the latch circuits.

The performance of the improved designs were evaluated by measuring the characteristic timing parameters for the bistables and comparing the parameters measured after hot-carrier stress on these circuits. The effects of hot-carrier degradations for the improved designs were now compared with that for the circuits before improvements were made. The bistable circuits were also analysed for improvement in resolving time which was assessed after stress over a fixed period.

The average stress levels on each of the selected three bistable circuits had a wide range of values during a typical operating cycle. The first bistable DL1 had the highest

stress level and the design improvements have shown to reduce the stress and improve the life-time for this circuit more than the other two. The reliability improvement for this circuit is better than the others, an improvement of 73% over a five year period. The second bistable had the minimum stress and hence higher reliability before improvements. We have improved the reliability of this bistable over a five year period of operation to 99% from 75% before improvement. For the third bistable circuit also we have improved the reliability to 95% from 47%.

Our investigation into the reliability and life-time of the bistable circuits have revealed that the stress levels and the corresponding hot-carrier degradation of the devices in a circuit depend on the position of the device relative to other devices and the sequence at which the devices are operated. The techniques developed to reduce the stress levels in identified devices have improved the reliability and the life-time of the circuit. We have also identified the best circuit configuration to reduce hot-carrier degradation. For high reliability VLSI circuits, we should use bistable circuits which we have identified as having best performance and improved reliability in spite of hot-carrier degradation effects.

Chapter 9

Summary and Conclusions

In this chapter we present a summary of the thesis and will review the analysis, results and conclusions presented in this thesis. We also draw some general conclusions from the work. We may not have considered all aspects concerning hot-carrier degradations and reliability of bistable circuits and so it is necessary to put forward a few suggestions for future research in the field of hot-carrier reliability of bistable circuits.

The main objectives of the research was to investigate the effects of wearout processes on the performance and reliability of bistable circuits. The main wearout process affecting the performance and reliability of sub micron MOS devices was identified as hot-carrier degradation. Bistable circuits designed using sub micron CMOS process technology are selected for our investigation into hot-carrier degradation effects. We have also identified a secondary objective as the effects of hot-carriers on the metastable state operations which may also affect the reliability of the circuit.

Even though it is not possible to eliminate hot-carrier degradation in submicron devices, we have demonstrated that hot-carrier stress on the devices can be reduced thereby improving the life-time and the reliability of bistable circuits. We also suggest some design rules and techniques for reducing hot-carrier degradation in bistable circuits.

9.1 A Summary of the Thesis

Hot carrier degradation has been identified as a major reliability concern for CMOS bistable circuits designed using submicron technologies. Bistable circuits were neglected by many researchers while investigating hot-carrier degradation effects in combinational circuits. A clear understanding of hot-carrier generation and the associated

degradation mechanisms was needed before we can suggest ways to reduce hot-carrier stress induced degradations. A review of the literature has shown that research into hot-carriers has been carried out by many researchers as early as nineteen-thirties. A better understanding of the mechanism of the hot-carrier generation in the channel of the MOS devices emerged in recent times and this has led to a renewed interest in research into hot-carrier induced damage in submicron MOS devices and circuits.

Impact ionisation of hot-carriers in the channel of a MOS device and the resulting substrate and gate currents generated are the major effects produced by hot-carriers. We needed a parameter to monitor the hot-carrier stress and the subsequent degradation. Since the gate current generated is reported to be very small, of the order of a few pico ampere, we decided to use the substrate current as the monitor for hot-carrier stress. The peak value of the substrate current is approximately 10% of the drain current at maximum stress conditions for the present technology and so this parameter is a good monitor.

Since existing substrate current models tended to be based on specific process technologies, we decided to develop our own substrate current model for the technology of our choice using existing models but incorporating additional effects for submicron devices not included in other models. The optimisation of this substrate current model led to the development of a new degradation model for the evaluation of the degradation in characteristic timing parameters of the bistables.

It was now necessary to test our substrate current and degradation models on a number of bistable circuits. For this, a number of transparent D-type latch circuits were designed using CMOS technology. Rigorous simulations were carried out to determine the inherent speed and timing parameters of the latch circuits, and the best three circuits were selected for further simulations. These circuits were re-designed using 1- micron and 0.7- micron CMOS technology design rules and simulated to determine the characteristic timing parameters. Our substrate current model was tested on a number of bistable circuits and was optimised.

The selected bistable circuits were analysed using a set of optimised SPICE model parameters for a typical operating cycle. Using the optimised substrate current model, and employing the post processor, the substrate current and the stress factors on each device in the latch circuits were evaluated. The SPICE model parameters for each device in the bistable were degraded proportional to the stress factors. Identified SPICE model parameters were used to model the degradation effects on devices. A standardised stress period was used to compare the degradation effects on characteristic timing parameters for the selected latch circuits.

A new life-time model was developed using the degradation model by specifying 10% degradation in drain current for a device and life-times for all the devices in the latch circuits were determined using this. The reliability of the latch circuits was evaluated using the life-time determined for the critically stressed devices in each of the bistable and the results show that reliability can be improved by reducing the stress on the devices. Other reliability assessment techniques were also employed for the bistables and the reliability calculated were compared and analysed.

As with all bistable circuits, those discussed in this thesis exhibit metastable state operation. When a bistable circuit is operated in the metastable region, it is found to be unreliable due to unusually long decision time encountered in fast submicron CMOS digital systems. The operation of the selected bistable circuits within the metastable window has been analysed in order to determine the susceptibility of the circuits to metastable operation. Using small signal analysis and employing analytical methods, it is possible to calculate the metastable voltage of cross coupled CMOS inverting devices. By pre-setting the inputs of these latches to the calculated metastable voltages, the latches were forced into metastable operation, to determine the metastability resolving time. The resolving time constant τ was also determined from device parameters and this led to the design of latches with minimum resolving time and hence improved reliability. From this analysis it became apparent that the threshold voltage for the MOS transistors has a significant effect on the metastability of the latch. By adjusting the threshold voltages for the n- and p- transistors it is possible to improve the metastability behaviour for the latch circuits.

Based on the analysis of the hot carrier degradation effects on the latch circuits, we have suggested techniques to reduce the hot-carrier stress and to improve life-time. It is possible to reduce the decline in the speed and performance of the latch circuits after hot-carrier stress and hence improve the reliability if circuits are re-designed using the suggested modifications.

The modifications for improving the hot-carrier reliability were incorporated into all the circuits and were re-simulated. The timing parameters were evaluated for the new designs and the life-time of the devices and the latches were evaluated. Reliability of the improved designs were evaluated and the improvement in reliability quantified and found to be significantly improved.

The improved circuits were degraded based on the stress factors and were simulated to determine the degradation effects on the timing parameters and the performance of the circuits. These results were compared with those measured prior to modifications and the improvements quantified.

9.2 Conclusions of the Thesis

For present technologies, nMOS devices have stress levels high enough to generate hot-carriers in the channel during normal operation of bistable circuits. This inevitably tends to degrade the performance of the device, affecting the life-time and reliability of the latch circuits. The main question which required an answer was: *How can we prevent the performance degradation in spite of hot-carrier degradation in the submicron devices currently in use?* A number of techniques have been suggested in this thesis for reducing the hot-carrier stress on devices identified to be under higher than normal stress. We have also identified the circuit configurations which can lead to increased stress levels and hence higher degradation rates. The signal path in a bistable circuit along which higher stress level exists can be identified and avoided by improved circuit configurations. Hot-carrier degradation in pMOS devices has been ignored as the stress and the induced degradations are at least an order of magnitude less in these

devices under normal dynamic operations. As the device dimensions fall further, the degradations in pMOS devices will become more significant.

The most useful method for reducing hot-carrier degradation is by reducing the number of hot-carriers generated in the channel of the nMOS device. Hot-carrier generation can be reduced if we can reduce the peak of the channel electric field. The field has a pronounced peak close to the drain junction and a number of techniques have been employed by other researchers to reduce the peak and to move the peak away from the region most susceptible to damage. Graded junctions and LDD structures have been employed recently and have been found to be effective in reducing the damage due to hot-carriers. Reducing the supply voltage is a second option which may reduce the circuit speed and increase transition times. Reducing the supply voltage also implies reducing the threshold voltage which may adversely affect the noise margins.

Increasing the junction depth X_j is another technique to reduce the hot-carrier generation. The increased junction depth will allow a thicker inversion layer and the charge carriers are diverted away from the gate interface region reducing the interface state generation and the oxide trapping.

9.2.1 Design Rules for Hot-Carrier Reliability

One of the most important outcome from this work are the proposed design techniques for improving CMOS circuit reliability with regard to hot-carrier degradation. Due to time constraints, we have applied the design rules to simple transparent latch circuits only. We believe that the principles developed can be extended to edge-triggered bistables so as to improve the reliability of VLSI and ULSI circuits designed with these devices. The design rules for this are summarised below:

- When designing using sub micron devices, minimum size transistors must be used where ever possible. This will reduce the gate and parasitic capacitances, hence improve the circuit speed and reduce the stress time.
- Select layout symmetry as opposed to signal symmetry when using number of inverting devices connected in series along the signal path. For sub micron devices,

the speeds of carriers in n- and p- devices are comparable due to velocity saturation for electrons occurring earlier than holes. Any small asymmetry in signal will be compensated by the asymmetry due to the next stage. Improved speed and reduced propagation delays effectively reduce the stress time.

- When the n- devices are connected in series as in the case of NAND gates and tri-state devices, the upper device connected to the output node must be switched on first. The *on* resistance of the n- channel acts as a load for the lower n- devices and divert the peak of the field away from the drain of the switching transistor, effectively reducing hot-carrier stress.
- The gates connected to the output node of a bistable circuit are found to be most susceptible to hot-carrier stress and have the most influence on speed and performance degradations. The bistable circuits must be designed such that the n-MOS transistors at the output node have reduced stress levels. This can be achieved by:

(a) Replace the inverting device at the output node by a 2-input or 3-input NAND gate if possible; modify the circuit design if necessary. Avoid using inverters and NOR gates at the output. Tri-state devices and transmission gates should not be used at the output node as these devices are relatively slow.

(b) When using a NAND gate at the output node, the n- device having minimum stress must be placed at the top of the ladder.

(c) If an inverter or a NOR gate is used at the output stage, stress reduction can be achieved by increasing the width and the length of the nMOS transistors while keeping W/L unchanged. Our simulations have shown that hot-carrier stress is significant for sub micron devices only.

- For high reliability circuits, reduce the supply voltage to 3.3 V or lower. When the device dimensions fall to 0.2 micron or lower in the near future, it will become necessary to reduce the supply voltage to improve the hot-carrier reliability of the bistables.
- Reduce the threshold voltage for n- and p- devices to improve the metastable state resolving time.

Increase the junction depth X_j so that the generated hot-carriers are diverted away from the interface, reducing the degradation.

9.3 Recommendations for further work

- We have developed a model for the monitoring of hot-carrier stress on devices in a circuit. The model has been employed successfully to monitor the stress related degradation in characteristic timing parameters of the selected bistable circuits. This process must be extended to other types of bistable circuits such as edge-triggered bistables.
- We have investigated the hot-carrier degradations on nMOS devices in selected bistable circuits. For the present technology, the hot-carrier related stress and degradations are negligible for pMOS devices. As device dimensions are scaled further, the hot-carrier effects will become more significant for pMOS devices. Hence, models for hot-carrier stress on pMOS devices must be also considered in the very near future.
- As the device dimensions are scaled, it will become necessary to scale down the supply voltage. Many recent CMOS processes use a supply voltage of 3.3 V and lower. If a few test devices fabricated using this technology are made available along with the SPICE model parameters, it is worth investigating the stress reduction and hence the improvement in the reliability of the circuits designed using this technology. The reduction in speed and propagation delays must be also investigated.
- Our DC model for stress monitoring was developed using published experimental results for nMOS devices by Lunenborg [5.5] and was extended to AC stress simulations. We would like to validate our AC model using actual data from field or by accelerated laboratory test on identical bistable circuits.
- Further simulations, on a number of MSI circuits such as a ring counter or an 8-bit shift register designed using three of our selected latch circuits, can be used to determine the time-to-failure under hot-carrier stress before and after design modifications to reduce stress according to our recommendations; hence evaluate hot-carrier related reliability for each circuit.

9.4 General Conclusions

As we are approaching deep-submicron (~0.1 μm) technologies, reliability and performance of VLSI and ULSI circuits are influenced by the increased power dissipation and hot-carrier induced degradation which may introduce new failure modes. New problems such as coupling of the signal and metal lines will become more significant because of reduced dimensions and lowering of the isolation barriers. Drain engineering and lowering the power supply voltage can relieve some of the problems. Reliability must be built into (BIR) the circuit design so that wearout failures can be evaluated prior to processing. We need to consider other methods also to counter hot-carrier induced and other reliability issues and these are discussed now:

1. There is a need for efficient circuit level reliability simulator at the design stage for identifying wearout related performance degradations [9.1]. This may require increased processing power for the simulator because of circuit complexity.
2. The reliability simulator can be used to minimise degradations and hence optimise circuit performance.
3. 3D modelling techniques to describe current flow in devices and the effects of all parasitic elements such as interconnects and diffusion layers must be employed for chip reliability analysis.
4. Delay defects will become more significant for fast deep-submicron circuits and so test methods will be needed to detect whether these are processing/ wearout related or imposed by physical limitations of the technology [9.2].
5. Embedded self monitoring test structures must be employed to detect wearout degradations and to counter the effects on performance decay.
6. A new degradation model for pMOS devices must be developed for deep submicron technologies to be used in the reliability simulator.

Recent developments in drain engineering and reduced supply voltage have pushed the hot-carrier reliability of VLSI circuits to higher limits. A few of the recent developments relevant to this field of study are presented here.

Diaz [9.3] has compared the hot-carrier reliability for sub-half micron (3.3 V 0.35 μm titanium salicide CMOS process with 80 Å gate oxide) LDD (lightly-doped drain) and DDD (double-doped drain) structures which tend to ease the peak of the field found near the drain-substrate junction. The degradation in linear drain current after 1000 s stress was found to be negligible for LDD and DDD devices. Another new drain engineering technique to reduce stress is the elevated source/drain (ESD) structure and according to Sun [9.4], hot-carrier stress induced degradation in linear drain current was more for devices having deeper S/D junction compared to devices having shallower S/D junction; but mobility degradation and threshold voltage shift due to hot-electron injection and the observed series resistance increase was more for shallower ESD devices.

Chan [9.5] and Raychaudhuri [9.6] both observed degradation effects due to hot-carrier stress in LDD devices which saturated with time. The former devices were made using 0.8 μm double-level metal, CMOS process with conventional oxide-spacer LDD structures. DC stress using constant-voltage stress conditions were employed and the degradation observed was due to a combination of the series-resistance increase in the LDD region and the carrier-mobility reduction in other regions. Raychaudhuri also used devices of comparable dimensions to the former and has reported a two-stage hot-carrier induced degradation. The early mode (1000 - 3000 s) of the degradation was characterised by a sharp rate of linear g_m degradation and the rate of the late mode degradation was much lower. He also found evidence of threshold voltage shift and mobility degradation. It was also reported that the saturation of the series resistance was due to inversion of the gate-edge LDD region due to hot-carrier damage.

Gonzalez [9.7] reported using optimisation simulations that for a 0.25 μm CMOS technology, optimal EDP (energy-delay product) was found to be at a supply voltage of 250 mV with a threshold voltage of 120 mV. It was suggested that the reduced speed at low voltage supply may force the designers to reduce the level of logic in their design to maintain performance. Until energy efficient techniques are developed, the supply and

threshold scaling is likely to be modest, probably at a rate that maintains constant electric fields within the device.

The above published results indicate that the hot-carrier degradation in submicron devices could not be eliminated completely with drain engineering and by lowering the supply voltage. Hence the work presented in this thesis are relevant for the present technology. We may have to modify the degradation models to accommodate the changes in the drain/source structures and the effect of degradation on the spacer regions. The increase in the substrate current for the deep-submicron technologies are going to introduce higher stress levels and increased degradation and these problems must be addressed at the design stage.

APPENDICES

APPENDIX A

Transistor Dimensions for 3 micron CMOS Design

$L_n = L_p = 3\ \mu m$

	DEVICE	$W_{n(drawn)}$ (μm)	$W_{n(eff)}$ (μm)	$W_{p(drawn)}$ (μm)	$W_{p(eff)}$ (μm)
1	Minimum size	4	2.73	5	2.88
2	Double size	8	6.73	9.5	7.38
3	2-input NAND	7	5.73	5	2.88
4	3-input NAND	10	8.73	5	2.88
5	2-input NOR	4	2.73	8	5.88
6	3-input NOR	4	2.73	11	8.88

Table A1 : Transistor widths (Technology: EM/3)

$L_n = L_p = 3\ \mu m.$

GATE/ DEVICE	W_{eff} (μm)	AD (pm)	AS (pm)	PD (μm)	PS (μm)
INVERTER/ TX GATE					
N-tr	2.73	50	50	10	10
P-tr	2.88	50	50	10	10
D/Size INVERTER					
N-tr	6.73	60	60	15	15
P-tr	7.38	70	70	20	20
2-INPUT NAND					
N-tr	5.73	60	60	15	15
P-tr	2.88	50	50	10	10
3-INPUT NAND					
N-tr	10.73	80	80	20	20
P-tr	2.88	50	50	10	10
2-INPUT NOR					
N-tr	2.73	50	50	10	10
P-tr	5.88	50	50	10	10
3-INPUT NOR					
N-tr	2.73	50	50	10	10
P-tr	8.88	70	70	15	15

Table A2: Transistor Drain & Source Area (AD & AS) and Perimeter (PD & PS) for CMOS design (Process: EM/3)

APPENDIX B

SPICE Device Model Parameters

Process Technology: EM/3

```
N-CHANNEL LEVEL 3 ** EMF - TYPICAL DRIVE
*
.MODEL NMOS3 NMOS (LEVEL=3 VTO=0.902 GAMMA=1.142 NSUB=1.88E16
+CGSO=5.68E-10 CGDO=5.68E-10 CJ=1.0E-4 CJSW=2.5E-10 JS=1.0E-7
+TOX=5.0E-8 NFS=1.985E11 XJ=5.0E-7 LD=8.2230E-7 UO=558
+VMAX=2.732E5 DELTA=0.266 ETA=0.017 THETA=0.045 KAPPA=0.199
+MJ=0.50 MJSW=0.33 PB=0.80
+WD=6.358E-7)
**
** P-CHANNEL LEVEL 3 ** EMF - TYPICAL DRIVE *
*
.MODEL PMOS3 PMOS (LEVEL=3 VTO=-0.504 GAMMA=0.751 NSUB=0.812E16
+CGSO=5.68E-10 CGDO=5.68E-10 CJ=1.0E-4 CJSW=2.5E-10 JS=1.0-7
+TOX=5.0E-8 NFS=6.674E11 XJ=5.0E-7 LD=8.948E-7 UO=322
+VMAX=4.39E5 DELTA=0.095 ETA=0.151 THETA=0.082 KAPPA=0.236
+MJ=0.50 MJSW=0.33 PB=0.76
+WD=1.06E-6
*
** N-CHANNEL LEVEL 1 **
*
*.MODEL NMOS1 NMOS (LEVEL=1 VTO=0.9 UO=500 TOX=5.0E-8
GAMMA=0.54
*+CGSO=4.3E-10 CGDO=4.3E-10 CJ=1.0E-4 CJSW=2.5E-10 JS=1.0E-7
*+LD=0.7E-6 XQC=0.3 THETA=0.004)
*+WD=0.74E-6
*
** P-CHANNEL LEVEL 1 **
*
.MODEL PMOS1 PMOS (LEVEL=1 VTO=-0.52 UO=90 TOX=5.0E-8 GAMMA=0.4
+CGSO=4.3E-10 CGDO=4.3E-10 CJ=1.0E-4 CJSW=2.5E-10 JS=1.0E-7
+LD=0.7E-6 XQC=0.3 THETA=-0.073)
+WD=1.08E-6
.END
```

Process Technology: EC/3

```
** ECPD MODEL 0.7 MOCRON LEVEL 3 * NOV 96 *
*
 *.OPTIONS   TNOM   =   27.00000
 .MODEL NMOS07  NMOS
```

```
+ LEVEL  = 3.0
+ NSUB   = 9.23e+16   TOX    = 150E-10    UO     = 467
+ XJ     = 0.5u
+ RSH    = 213
+ THETA  = 84.4m
* XL     = 0.01u
+ LD     = 0.1u
* XW     = 0.9u
* WD     = 0.45u
+ VTO    = 0.832
+ DELTA  = 3.46
+ GAMMA  = 0.946
+ ETA    = 0.01
+ NFS    = 4E11
+ VMAX   = 159k      KAPPA  = 0
*TLEV   = 1
* BEX    = -1.5      TCV    = -2m
+ CJ     = 503u      MJ     = 0.43
+ CJSW   = 109p      MJSW   = 0.43      PB     = 0.675
+ CGDO   = 200p      CGSO   = 200p      JS     = 2u
*
.MODEL PMOS07  PMOS
+ LEVEL  = 3.0
+ NSUB   = 1e15      TOX    = 150E-10    UO     = 142
+ XJ     = 1n
+ RSH    = 301
+ THETA  =  0.124
* XL     = 0.02u
+ LD     = 0.1u
* XW     = 0.9u
* WD     = 0.45u
+ VTO    = -1.04
+ DELTA  = 3.4
+ GAMMA  = 0.535
+ ETA    = 25.9m
+ NFS    = 8E10
+ VMAX   = 282k      KAPPA  = 8.1
* TLEV   = 1
* BEX    = -1.0      TCV    = 1.52m
+ CJ     = 776u      MJ     = 0.51
+ CJSW   = 572p      MJSW   = 0.51      PB     = 0.7
+ CGDO   = 200p      CGSO   = 200p      JS     = 20u
*
.end
```

Process Technology: EC/13

```
.MODEL NMOS NMOS
+level=13
+vfb0=0.428   lvfb=-11.90u   wvfb=0.27
+phi0=85.6e-03        lphi=0.0        wphi=0.0
+k1=0.729     lk1= -64.37e-3 wk1=9.78e-03
+k2=17.16e-03         lk2=41.47e-03 wk2=0.0
+eta0=0.0     leta=20.0e-03  weta=0.0
+x2e=0.0      lx2e=0.0       wx2e=0.0
+x3e=0.0      lx3e=0.0       wx3e=0.0
+muz=540.0
+x2m=25              lx2m=-12.0       wx2m=10.0
+mus=580.0    lms=-20.0      wms=-30.0
+x2ms=29.0    lx2ms=-12.0    wx2ms=15.8
+x3ms=0.0     lx3ms=0.0      wx3ms=0.310
+vddm=2.2
+u00 = 150.0e-03      lu0 = 0.176     wu0 = 20.00e-03
+x2u0 = 5.0e-03       lx2u0 = -1.49e-03      wx2u0 = 0.0
+u1 = 0.0      lu1 = 38.5e-03 wu1 = 0.0
+x2u1 = -0.0   lx2u1 = 0.0    wx2u1=0.0
+x3u1 = 0.0    lx3u1 = 0.0    wx3u1 = 0.0
+tempm = 25.0
+tox = 150e-10         dl0 = 0.15      dw0 = 0.0
+lref = 20.0u  wref = 20.0u
+n0 = 1.4      ln0 = 0.0      wn0 = 1.0
+nb0 = 0.1     lnb = -0.05    wnb = 0.5
+nd0 = 0.0     lnd = 0.0      wnd = 0.0
+rsh = 0.0
+cgdo = 200p  cgso = 200p
+cj = 486u     mj = 0.43      pb = 0.675
+cjsw = 223p  mjsw = 0.43
+acm = 2.0     js = 2.0u

.MODEL PMOS PMOS
+level=13
+vfb0=-0.480  lvfb=-0.338    wvfb=0.1
+phi0=0.945   lphi= 0.0      wphi=0.0
+k1=0.593     lk1=0.536      wk1=0.0
+k2=0.0               lk2=0.221      wk2=20.0e-03
+eta0=0.0     leta=35.0e-03  weta=0.0
+x2e=0.0      lx2e=0.0       wx2e=0.0
+x3e=0.0      lx3e=0.0       wx3e=0.0
+muz=190
+x2m=8.27     lx2m=-6.33     wx2m=5.0
+mus=200.0    lms=42.0       wms=0.0
+x2ms=7.0     lx2ms=-6.0     wx2ms=0.0
```

```
+x3ms=0.0    lx3ms=6.0     wx3ms=0.0
+vddm=4.0
+u00 = 0.200  lu0 = 0.0638  wu0 = 0.0
+x2u0 = 0.0   lx2u0 = -10.25e-03   wx2u0 = 0.0
+u1 = -100.0e-03      lu1 = 0.1      wu1 = 0.0
+x2u1 = 0.0   lx2u1 = 0.0    wx2u1 = 0.0
+x3u1 = 0.0   lx3u1 = 0.0    wx3u1 = 0.0
+tempm = 25.0
+tox = 150e-10        dl0 = -0.04    dw0 = 0.0
+lref = 20.0u  wref = 20.0u
+n0 = 1.0      ln0 = 0.0      wn0 = 1.0
+nb0 = 0.02    lnb = -0.11    wnb = 0.2
+nd0 = 0.0     lnd = 0.0      wnd = 0.0
+rsh = 0.0
+cgdo = 200p  cgso = 200p
+cj = 600u     mj = 0.510     pb = 0.7
+cjsw = 820p  mjsw = 0.510
+acm=2.0      js = 20.0u
.end
```

Process Technology: EC/6

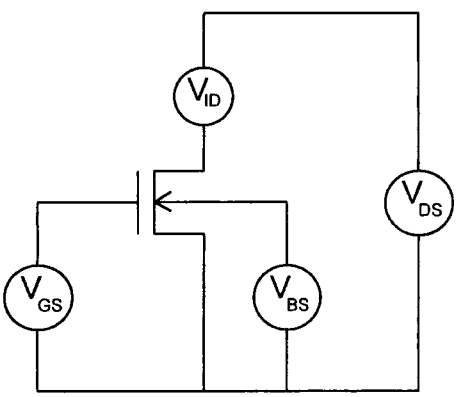
```
* ECPD07 HSPICE LEVEL 6 MODEL: NMOS
*
.MODEL NMOS07 NMOS
+ LEVEL  = 6.0      UPDATE = 1.0
+ NSUB   = 1.965e+16  TOX   = 150.0    BETA   = 97e-6
+ XJ     = 0.25u
+ RSH    = 65
+ MOB    = 2
+ F1     = 372k     F2     = 200m     UTRA   = 563m
+ XL     = 0.04u    LD     = 0.1u
+ XW     = 0.9u     WD     = 0.45u
+ VTO    = 815m
+ NSS    = 0.0
+ NWE    = 193.7n
+ UFDS   = 99.5m    VFDS   = 0.2      FDS    = 84m
+ VB0    = 1.50     GAMMA  = 764m     LGAMMA = 705m
+ VSH    = 650m     NWM    = -197m    SCM    = 1.733
+ WIC    = 2        NFS    = 5E11     WEX    = 17
+ LAMBDA = 10.63u
+ NU     = 1
+ KU     = 1.405    ECRIT  = 87k      MBL    = 555m
+ KA     = 974m     MAL    = 295m
+ CLM    = 3
+ KCL    = 1.08     MCL    = 4.63
+ TLEV   = 1
```

```
+BEX    = -1.5      TCV    = -2m
*+ CAPOP  = 2.0
+ACM    = 2.0
+CJ     = 503u      MJ     = 0.43
+CJSW   = 109p      MJSW   = 0.43      PB     = 0.675
+CGDO   = 200p      CGSO   = 200p      JS     = 2u
*IMPACT IONIZATION MODELS: TRIAL VALUES
*---------------------------------------------------
+IIRAT = 0.0  ALPHA = 1  VCR = 13.5  CAPOP = 2.0
*---------------------------------------------------
* ECPD07 HSPICE LEVEL 6 MODEL : PMOS
*
.MODEL PMOS07 PMOS
+LEVEL  = 6.0       UPDATE = 1.0
+NSUB   = 2.5e+16   TOX    = 150.0     BETA   = 30.16e-6
+XJ     = 0.5u
+RSH    = 80
+MOB    = 2
+F1     = 483k      F2     = 320m      UTRA   = -197m
+XL     = 0.042u    LD     = 0.1u
+XW     = 0.9u      WD     = 0.45u
+VTO    = -1
+NWE    = 56.1n
+UFDS   = 331m      VFDS   = 0.5       FDS    = 286m
+VB0    = 1.5       GAMMA  = 587m      LGAMMA = 653m
+VSH    = -116m     NWM    = -442m     SCM    = 1.01
+WIC    = 2         NFS    = 6E11      WEX    = 14.3
+LAMBDA = 14u
+NU     = 1
+KU     = 9.871     ECRIT  = 486k      MBL    = 803m
+KA     = 1.082     MAL    = 0
+CLM    = 3
+KCL    = 41.91m    MCL    = 6.97
+TLEV   = 1
+BEX    = -1.0      TCV    = 1.52m
+CAPOP  = 2.0       ACM    = 2.0
+CJ     = 776u      MJ     = 0.51
+CJSW   = 572p      MJSW   = 0.51      PB     = 0.7
+CGDO   = 200p      CGSO   = 200p      JS     = 20u
.MODEL ND D
+CJA    = 503u      CJP    = 109p
+EXA    = 0.43      EXP    = 0.43      PB     = 0.675
.MODEL PD D
+CJA    = 776u      CJP    = 572p
+EXA    = 0.51      EXP    = 0.51      PB     = 0.7
.end
```

APPENDIX C

Circuit and Input File for Transistor Characteristics

OUTPUT CHARACTERISTICS



MOSFET CHARACTERISTICS NMOS I_D - V_{DS}

```
*
M1 2 1 0 3 NMOS2 W= 4U L= 3U AD= 50P AS= 50P PD= 10U PS= 10U
VDS 4 0
VGS 1 0
VBS 3 0 DC 0
VID 4 2 DC 0
.DC VDS 0 5 0.2 VGS 0 5 1
.PROBE
.MODEL NMOS2 NMOS LEVEL=2 VTO=0.80 PB=0.67
+CGSO=2.4E-11 CGDO=2.4E-11 CJ=3.5E-4 CJSW=5.2E-10 JS=1.0E-8
+DELTA=4.0 NSUB=13E15 UO=640 UCRIT=6E4 UEXP=0.10 VMAX=5E4
+XJ=0.4E-6 MJ=0.85 NEFF=4.0 NFS=4E11 TOX=500E-10 XQC=0.3
+RSH=40 LD=0.2U MJSW=0.26
.END
```

APPENDIX D

CMOS Technologies

Code	Supplier	SPICE Level	Min. Size (μm)
EM/3	EMF	3	3
EC/3	ECPD	3	0.7
EC/6	ECPD	6	0.7
EC/13	ECPD	13	1
Ph/9	Philips	9	0.7

APPENDIX E

Device Dimensions for CMOS designs

Code	Type	Width (μm)	Length (μm)
N: 1/0.8	nMOS	1	0.8
N: 2/0.8	nMOS	2	0.8
N: 2/1	nMOS	2	1
N: 4/3	nMOS	4	3
N: 4/8	nMOS	4	8
1/0.8	n/p MOS	1	0.8
2/0.8	n/p MOS	2	0.8

APPENDIX F

MATHCAD PROGRAM

SUBSTRATE CURRENT: DL1 N5

$i := 0..200 \qquad j := 0..3$

$x := READPRN(N533)$

$C := 0.9875$

$Beta := 6.07 \cdot 10^{7}$

$Tox := 15 \cdot 10^{-9}$

$Xj := 0.5 \cdot 10^{-6}$

$$Lc := 0.2 \cdot Tox^{\frac{1}{3}} \cdot Xj^{\frac{1}{2}}$$

$W := 2.0 \cdot 10^{-6}$

$L := 0.8 \cdot 10^{-6}$

$Vth := 0.832 \qquad Vbs := 0$

$$Vgt_i := \left|x_{i,3}\right| - Vth - 0.13 \cdot Vbs - 0.25 \cdot \left|x_{i,3}\right|$$

$$Esat_i := 1.1 \cdot 10^{7} + \left(0.25 \cdot 10^{7} \cdot \left|x_{i,3}\right|\right)$$

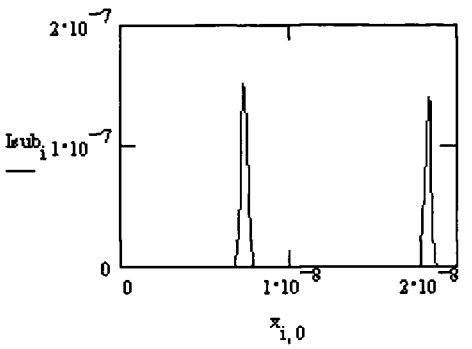
$$Vdsat_i := \frac{Vgt_i \cdot L \cdot Esat_i}{Vgt_i + L \cdot Esat_i}$$

$Vdrive_i := |x_{i,2}| - |Vdsat_i|$

$Alfa_i := \frac{Beta \cdot Lc}{|Vdrive_i|}$ $Id_i := |x_{i,1}|$

$Isub_i := C \cdot Id_i \cdot |Vdrive_i| \cdot \exp(-Alfa_i)$ $X_i := x_{i,0}$ $Y_i := Isub_i$ $Z_i := x_{i,1}$

$WRITEPRN(DN4) := augment(X, Y)$



$H := 10^6$

$m := 2.9$ $n := 0.5$ $S := 7.38$

$t := 36 \cdot 10^3$ $I := 0.0146$

$\sum_i Id_i = 0.0032$

$\sum_i Isub_i = 1.3474 \cdot 10^{-6}$

$$D := \left[\left[\frac{\sum_i Isub_i}{\sum_i Id_i} \right]^m \cdot \frac{\sum_i Id_i}{W \cdot H} \right]^n \cdot t^n$$

$D = 9.7913 \cdot 10^{-5}$ Degn after 10 Hrs opn

$Df := 0.1$ Degradation at failure defined as 0.1(10%)

$$Lt := H \cdot Df^{\frac{1}{n}} \cdot W \cdot \left[\left(\sum_i Isub_i \right)^{-m} \cdot \left(\sum_i Id_i \right)^{m-1} \right]$$

$Lt = 3.7551 \cdot 10^{10}$ seconds

Lifetime Lt calculated is very much under estimated because degradation progresses non-linearly with time.

$T := H \cdot Df^{\frac{1}{n}} \cdot W \cdot (S \cdot W)^{-m} \cdot I^{m-1}$

$T = 6.652 \cdot 10^8$

$\frac{Lt}{3600} = 1.0431 \cdot 10^7$ Hours

Appendix G

PUBLICATIONS

The Effect of Hot-Carrier Degradation on CM S Bistable peration

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Abstract: Hot-carrier degradations in submicron M S devices have become a serious problem in the design of VLSI circuits. It is generally accepted that hot carrier effects will lead to degradation of channel mobility and a shift in the transistor threshold voltage. In this paper the hot carrier degradation on CM S bistable operation is analysed. Three common forms of bistable circuit are considered in a comparative study. The hot carrier stress experienced by each device in a circuit is analysed through a normal operating cycle of the circuit. This is translated to a cumulative parametric shift for each device. Simulations of circuits containing appropriately degraded devices are then performed to assess the change in circuit parameters. Circuit forms which are least susceptible to this form of degradation are identified.

1. Introduction

The scaling of M S transistors to submicron dimensions has caused hot-carrier degradation to become a significant problem in CM S integrated circuits. Dynamic operation of a bistable circuit will give rise to varying stress levels on the transistors leading to non-uniform degradation levels. The mechanisms of hot-carrier degradation and the stress conditions which cause this degradation are well understood [HTH85], [QMH94]. The consequences of the transistor parameter shifts on circuit performance and timing degradations are however hard to predict, as the stress experienced by each transistor in a circuit depends on the circuit configuration and operating conditions.

In this paper we describe a technique which we have used to evaluate the relative and absolute stress levels experienced by all transistors in a number of CM S bistable circuits. The stress on each device is translated into parametric shift in transistors and from this the effect on circuit timing parameters has been evaluated. It has been reported [LK92]

that the degradation rate of nM S transistors during dynamic operation was found to be more severe compared to the degradation rate during static operation. The enhanced degradation has been attributed to the alternating hot-electron and hot-hole injections into the gate oxide during dynamic stress and the generation of interface states [HBG88]. Consequently we have investigated the dynamic stress experienced by devices under normal operating conditions.

The method used to evaluate the stress on each transistor involves calculating the substrate current for each device. This is generally accepted as a reliable means of monitoring hot electron degradation in transistors and is preferred to gate current monitoring due to the magnitudes of the currents involved.

The substrate current is used as a direct measure of stress and this is translated into device parameter shifts using a degradation model which is described in section 3. Parameter shifts are then incorporated into device models for subsequent resimulation of the bistable circuits and we discuss the effect of transistor degradation on circuit performance in section 4.

2. Stress modelling and simulation

The three common forms of bistable circuits selected for analysis are given in fig. 2.1. The circuits were simulated using HSPICE Level 6 Model parameters from a 0.7 μm commercial process under dynamic conditions. A typical operating cycle was used for the simulations so that all the devices were stressed during the simulation cycle. The results of the simulation were used to calculate the substrate current for each of the devices in the circuit. The substrate current model used in these calculations was developed by optimising existing models [SNK86], [HTH85], [Lee86] and by incorporating additional parameters to model the effects of the variation of substrate current with V_{dsat} variation for submicron devices.

ur optimised substrate current model is given by:

$$I_{sub} = C_i \, I_d \, (V_{ds} - V_{dsat}) \exp\{-\beta \, l_c / (V_{ds} - V_{dsat})\} \quad .... \quad (1)$$

where $C_i = 0.9875$, $\beta = 6.07 \times 10^7$ and
$l_c = 0.2 \, (T_{ox})^{1/3} \, (X_j)^{1/2}$.

The values for T_{ox} (gate-oxide thickness) and X_j (drain/

substrate junction depth) for the technology are 15nm and 0.25 μm respectively.

ur model has the following features compared to the other published models:

1. does not depend on extracted parameters based on process technology
2. dependence on device dimensions and channel doping is built into the model (T_{ox} and X_j) and can be easily obtained from SPICE or HSPICE model parameters
3. the variation of substrate current with gate bias is incorporated into the model
4. the exponential dependence of electric field on impact ionisation is included
5. channel length and channel width dependencies of substrate current are built into the model by using the simulated output values for I_d, V_{ds} and V_{dsat} as input to the post processor.

2.1 Stress Simulation Results

The substrate current model was implemented with a MATHCAD postprocessor using the HSPICE output file as input. The substrate current generated by each device during dynamic operation was calculated and used directly as a measure of stress.

For hot carrier effects, stress factor S(t) is usually taken as the normalised substrate current (I_{sub}/W) and the degradation of a device parameter P_i is defined as [HSG92],

$$\Delta P_i = A_i \, I_{sub}/W \qquad \ldots\ldots\ldots (2)$$

where A_i is a proportionality constant dependent on the process technology.

The average drain current and the substrate current for each device in the circuits during the simulation period were recorded and the stress factor calculated and compared. The substrate current plotted for a typical device and the corresponding drain current are given in fig. 2.2.

A representative result of the simulation result for one of the devices in the latch circuit is given below:

Duration of simulation $t = 2$ ns
Average drain current $\Sigma I_d = 0.003$ A
Average substrate current $\Sigma I_{sub} = 7.906 \times 10^{-5}$ A
Stress factor $S = \Sigma I_{sub}/W = 79.06$ A/m

The above device was found to be under severe stress leading

to enhanced degradation. The stress factor for an n- channel transistor having minimum stress was found to be 0.102 A/m.

3. Degradation model

The following *three* HSPICE level 6 parameters were used to model the degradation effect.
(i) NFS (number of fast interface states): At low gate voltages (below half drain voltage) the hot hole effect is dominant and will generate a large number of additional interface states all along the conducting channel and this is modelled as an increase in NFS.
(ii) U : Mobility degradation; this is mainly due to the scattering of electrons in the channel as a result of electron traps generated by hot holes at low to medium gate voltages.
(iii) VT : Shift in threshold voltage is due to trapped electrons at the interface (close to the drain) and that trapped in the gate-oxide. Normally this will give rise to an increased applied gate voltage before channel is inverted and is modelled as increased threshold voltage for the NM S transistor.

It has been reported by Mistry & Doyle [MD93] that the enhanced hot carrier stress damage observed under AC stress conditions is due to three different damage mechanisms which occur during low to medium, medium and medium to high gate voltages. All three modes are necessary to explain the enhanced degradation during dynamic stress and so the three degradation mechanisms are included in this degraded model. The trapping of electrons at the interface is modeled as a threshold voltage shift [MSA81], scattering of electrons at low to medium gate voltages are modeled using mobility degradation [YAY93].

The device degradation [LKK90] is given by,

$$\Delta D = \{(I_{ds}/WH)\ (I_{sub}/I_{ds})^{m}\}^{n}\ t^{n} \qquad \ldots\ldots\ldots\ (3)$$

where the fitting parameters were determined by comparing various published values as well as simulation results and are given by:
$H = 10^{6}$, $m = 2.9$, $n = 0.5$ and t is the effective duration of stress. During the AC simulations, the effective stress time was estimated as 2 ns and this value was kept constant for all the devices in the circuit.

The Life time model of a device was developed using the Berkeley Reliability Simulator (BERT) [LKK90] and other models and is given by,

$$\iota = H\ (\Delta D_f)^{1/n}\ W\ (I_{sub})^{-m}\ (I_{ds})^{m-1} \quad \ldots\ldots\ldots\ (4)$$

4. Degradation Simulation Results

The degradation $\Delta D/D_0$ for the three parameters listed above were calculated using equation (3) for the simulation period. The degradation simulation results obtained for one of the n-channel transistors of the N R gate forming part of a D-Latch circuit (fig. 2.1(a)) is given below:

Device degradation (at t= 2 ns) $\Delta D/D_0 = 1.201 \times 10^{-8}$
Threshold voltage shift (10 Hrs) $\Delta V_t = 0.016$ V

The device degradations calculated for the devices in the circuit were compared to determine the devices which are most susceptible to degradation. The degraded simulation results for the two D-latch circuits are tabulated in Table 4.1.

Table 4.1 Degradation simulation results

Parameter	D-LATCH CIRCUITS Circuit 1 (Fig. 2.1(a)) Degradations			Circuit 2 (Fig. 2.1(c)) Degradations			unit
	0%	10%	20%	0%	10%	20%	
t_r	1.147	1.148	1.183	1.097	1.099	1.109	ns
t_f	0.737	0.786	0.866	0.560	0.560	0.559	ns
t_{pLH}	1.021	1.077	1.156	0.789	0.783	0.783	ns
t_{pHL}	1.211	1.274	1.353	1.494	1.480	1.472	ns
t_{su}	0.658	1.160	1.161	1.100	1.104	1.106	ns
t_h	-0.062	0.437	0.437	-0.480	-0.480	-0.479	ns
t_w	4.500	4.997	4.998	4.000	4.000	4.000	ns
f_{max}	222	200	200	250	250	250	MHz
$t_{c(w)}$	0.596	1.597	1.598	0.721	0.624	0.628	ns
$\Delta D/D_0$	1.201	1.160	1.102	0.370	0.345	0.320	$x10^{-8}$
ΔV_{th}	0.000	0.016	0.032	0.000	0.004	0.008	V

Note: The Degradation $\Delta D/D_0$ was for the transistor in the latches with worst stress; t_r and t_f are the rise time and fall time and were measured for 0% degradation (virgin circuit), 10% degradation and 20% degradation respectively; t_{pLH} and t_{pHL} are the propagation delays from input to output for low to high and high to low transitions respectively; t_{su} is the setup time and t_h is the hold time for the latch. t_w is the minimum pulse width and f_{max} is the maximum frequency of operation; $t_{c(w)}$ is the critical window for metastability.

It can be seen from the table that the delays have increased with degradation but the stress and hence the delays are less for circuit 2 shown in fig. 2.1(c). The effect of degradation on the metastability window is less pronounced for this circuit.

A comparative study of three of the D-latch circuits simulated using this model showed that the most severe degradation is experienced by the circuit which used Tri-state devices and N R gate shown in fig.2.1(a). The minimum stress and degradations were experienced by the circuit which used Universal NAND gates. The stress and the subsequent degradations were moderate for the D-latch circuit which used Transmission gates and inverting devices (fig.2.1(b)).

5. Conclusions

ur investigations have shown that all the devices in a VLSI circuit do not receive the same amount of electrical stress. The level of stress received by each device is a complex function of the transistor location, terminal voltage, current magnitude and duty cycle.

Using substrate current as a monitor, the hot-carrier stress experienced by the devices in a circuit has been modelled. The corresponding degradations in device parameters have been established using circuit level simulations and the shift in circuit delays analysed.

In all the three circuits simulated, it is possible to reduce the stress on transistors for the identified highly stressed devices. Number of techniques can be employed to reduce the stress on these critical devices and thereby improving the overall reliability of the circuit. Another way to reduce the hot-electron-stress is to increase the channel width of the n- channel transistors two or three times for the identified highly stressed critical devices so as to reduce the normalised substrate current (I_{sub}/W).

D-latch circuits which use NAND gates in place of N R gates and Tri-state devices should be employed for high reliability circuits in order to reduce hot-carrier degradation problems.

REFERENCES

[BW91] Brox M and Weber W, "Dynamic degradation in M SFETs- Part I: The physical Effects", IEEE Tran ED-38, no 8, Aug 91, pp 1852-1991.

[HBG88] Heremans P, Bellens R, Groeseneken G, & Maes HE, "Consistent model for the hot-carrier degradation in n-channel and p-channel M SFETs", IEEE tr ele dev v 35, no 12, Dec 88.

[HSG92] Hsu W, Sheu BJ, Gowda SM and Hwang C, "Advanced integrated circuit reliability simulation including dynamic stress effects", IEEE J SS Ckts vol 27, no 3,March 92, pp 247-257.

[HTH85] Hu C, Tam S, Hsu F, Ko P, Chen T, & Terrill K, "Hot electron induced M SFET degradation- model, monitor and improvement", IEEE Tran ED-32, no 2, Feb 85.

[Lee86] Lee M, "BSIM substrate current modelling", Memorandum No: UCB/ERL M86/49, University of California, Berkeley, CA 94720, 3 June 1986.

[LK93] Leblebici Y and Kang S, "Modelling and simulation of hot-carrier induced device degradation in M S circuits", IEEE J SS cks, vol 28, no 5, May 93, pp 585-595.

[LKK90] Lee P, Kuo M, Ko P and Hu C, "BERT - Circuit Aging Simulator (CAS)", Memorandum No.UCB/ERL M90/2, 18 January 1990.

[MD93] Mistry K and Doyle B, "AC versus DC hot carrier degradation i n- channel M SFETs", IEEE Tran ED-40, No 1, Jan 93, pp 96-104.

[MSA81] Matsumoto H, Sawada K, Asai S, Hirayama M and Nagasawa K, "Effect of long term stress on IGFET degradations due to hot electron trapping", IEEE Tr. on ED, vol ED 28, No 8, August 81, pp 923-927.

[QMH94] Quader K N, Minami E R, Huang W, Ko P K, and Hu C, "Hot Carrier Reliability Design Guidelines for CM S Logic Circuits", IEEE J of SS cts, vol 29, No 3, March 94, pp 253-261.

[SNK86] Sakurai T, Nogami K, Kakumu M and Iizuka T, "Hot-carrier generation in submicrometer VLSI environment", IEEE J SS Circuits, vol sc-21, no 1, Feb 86, pp 187-191.

[Wan92] Wang CT (Edited by), "Hot carrier-design considerations for M S devices and circuits", Van Nostrand Reinhold 1992.

[WBK91a] Wang Q, Brox M, Krautschneider WH and Weber W, "Explanation and model for the logarithmic time dependence of p-M SFET degradation", IEEE EDL-12, no 5, May 91, pp 218-220.

[WBK91b] Weber W, Brox M, Kunemund T and others, "Dynamic degradation in M SFETs- Part II: Application in the circuit environment", IEEE Tran ED-38, no 8, Aug 91, pp 1859-1866.

[WHT93] Woltjer R, Hamada A, & Takeda E, "Time dependence of p-M SFET hot-carrier degradation measured and interpreted consistently over ten orders of magnitude", IEEE Tran ED-40, no 2, Feb 93, pp 392-401.

[WKW91] Wang Q, Krautschneider H, Weber W & Schmitt-Landsiedel D, "Influence of M SFET I-V characteristics on switching delay time of CM S inverters after hot-carrier stress", IEEE El dev lett. vol 12, No 5, May 91.

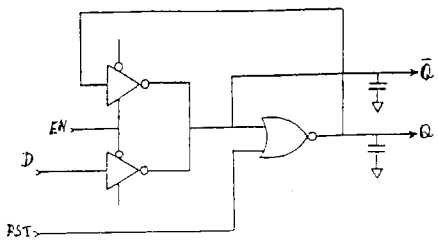
[WR92] Weber W, & Reisinger H, "Failure mechanisms in VLSI circuits: Time dependent dielectric breakdown and hot carrier effects", 3rd European Symposium on electron devices, failure physics and analysis (ESREF'92) ct 5, 1992.

[WRK88] Weber W, Risch L, Krautschneider W and Wang Q, "Hot-carrier degradation of CM S inverters", IEDM 88, pp 208-211.

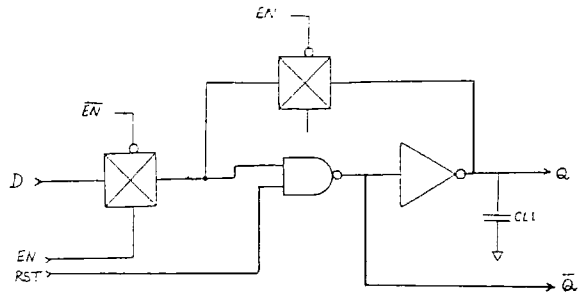
[WWD84] Weber W, Werner C and Dorda G, "Degradation of n-M S transistors after pulsed stress", IEEE EDL-5, no 12, Dec 84, pp 518-520.

[YAY93] Yue C, Agostinelli VM, Yeric GM and Tasch AF, "Improved universal M SFET electron mobility degradation model for circuit simulation", IEEE Tr. on computer aided design og ICs and systems, vol 12, No 10, ctober 1993, pp 1542-1545.

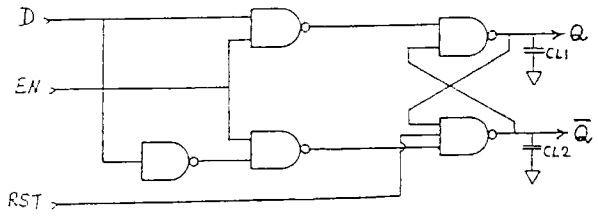
Fig.2.1. D-latch circuits



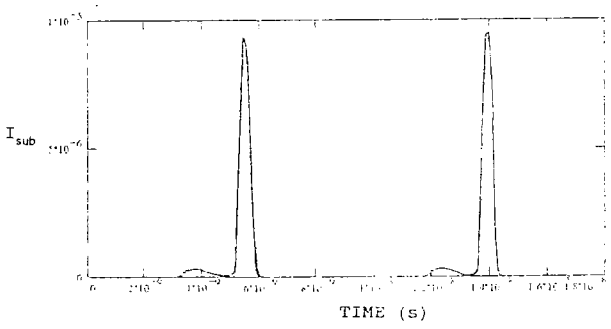
(a) using Tristate devices



(b) using Transmission gates



(c) using Universal NAND gates



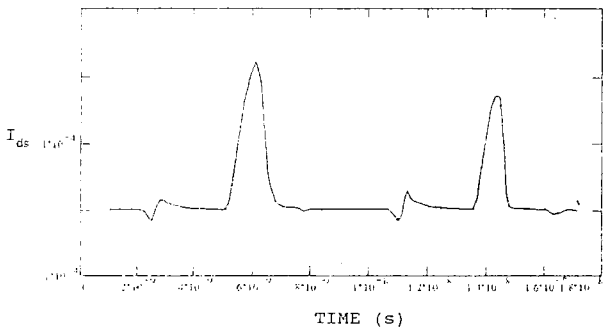


Fig.2.2. (a) Substrate current (b) drain current
for an n-channel transistor in the D-latch circuit.

Simulating Metastable State Operation in Flip-flops

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ABSTRACT:

Flip-flops have been plagued by timing errors introduced by the *metastable state* operation which may occur in any device having two stable states. If the flip-flop outputs linger half way between the logic *high and low* states longer than the normal logic decision time, an erroneous output may be generated. For reliable operation of flip-flops, it is vital to recognise this problem and to prevent it by means of improved design methods. Parametric variations introduced during processing as well as during normal operation are usually responsible for these timing errors and so it is very important to include the metastable state simulations during design stage so as to study the effects on critical parameters and to devise design improvements to reduce this problem.

The inputs of the flip-flop must be adjusted precisely within a fraction of a nanosecond with respect to the clock edge for simulating the metastable state and it can be very frustrating and time consuming. A simple flip-flop can be modelled as two cross coupled inverting devices and so the input nodes may be pre-set to the transition voltages for the devices to simulate the metastable state operation. The metastable state operation of the flip-flops were simulated using this technique and the time evolution of the circuits were studied under different conditions. The determination of the resolving times of various flip-flops and their dependence to critical parameters led to improved designs.

1. Introduction

Metastable state operation of latches and flip-flops has been recognized as a main cause of timing errors in digital systems. These timing errors are due to the unusually long delay in logic decision time due to the metastable state which is between the two stable logic states where it may remain for an indefinite time before resolving itself to one of the stable states. Many research papers have been published on this subject and have

suggested ways for minimizing the errors caused in digital systems due to synchronizer and arbiter malfunction. The problem due to metastable state in latches and flip-flops still remain unresolved even though better understanding of the metastable operation of these elements are at hand.

In this paper, a review of metastable operation in digital bistable circuits is presented in the next section. The evaluation of metastable resolving time from circuit parameters is discussed in section three. In the fourth section, the simulation of latch circuits in the metastable region is presented and conclusions are given in section five.

2. A review of metastability in flip-flops

Metastable is a state between the logic HIGH and logic LOW states in a digital system and is a condition which can occur in any latch or flip-flop if the minimum set-up or hold times are violated. In most cases, the flip-flop will either react to the input and switch to a new stable state or remain in the current stable state. A flip-flop can get confused if the data input changes during set-up or hold time interval preceding the clock pulse. As long as the flip-flop makes some decision, whether to go to a one or a zero in this ambiguous case, all is well. However there is a chance that the input has changed at the wrong time, at exactly the moment of truth, such that the flip-flop cannot make up its mind, its output can hover at the logic threshold literally for microseconds or even worse, go towards one logic state and before settling at this state switch back to the other state! In most flip-flops and other synchronizing circuits, the metastable state may last for only a short period of time, but theoretically this state can persist indefinitely. When the output of a device goes into metastable state the clock to out delay will be grossly affected. This may affect the system's worst case propagation delay and potentially lead to a system crash.

A functional definition of metastability applied to cross-coupled circuits is the occurrence under undriven conditions of an output voltage in a range around transition voltage V_t that cannot reliably be interpreted as either high or low [7]. As discussed in section 3, latch circuits are made by cross coupling two inverting devices. When plotting static transfer curves as shown in figure 1, for the two cascaded inverters, the resulting three intersections indicate three points of equilibrium [5].

A latch or a bistable element in a self-contained synchronous system never has the opportunity to reach a metastable condition since satisfaction of the timing constraints assures that the output is driven to a voltage outside of a metastable range. But if asynchronous inputs are applied to a latch, the data and the clock inputs may change simultaneously producing a metastable state at the outputs of the latch. If this condition persists for more than a clock period, an illegal or incorrect data will be transmitted to the next stage of the digital system.

3. Metastability resolving time

A simple latch is basically two inverting devices cross coupled as shown in figure 2. It is possible to realise this circuit using two NAND gates, two NOR gates or by two inverters. When the latch is in a metastable state, the voltages at the two nodes will be same and is approximately half the supply voltage; inputs and outputs are at the same voltage and this is exactly the voltage known as the transition voltage V_t and in this paper it will be called the metastable voltage V_m . A transistor level circuit for the latch circuit of figure 2 is given in figure 3.

At the metastable state, both n- and p-transistors are biased in the saturation region and has large gains. Hence it is possible to replace the circuit by its small signal model given in figure 4 [6]. The p-transistors are replaced by its equivalent ON resistances in the saturation region and the n-transistors are replaced by its transconductances multiplied by the nodal voltages (current generator) as shown. An ac small signal equivalent circuit of the latch is shown in figure 5 and the voltage evolution at the output nodes are given in figure 6.

When a CMOS inverting device is operated at the metastability region, both the NMOS and the PMOS transistors are in the saturation region and the currents through them are the same. The metastability voltage V_m for an inverting device is given by [6],

$$V_m = \frac{V_{dd} - |V_{Tp}| + V_{Tn}\, b}{1 + b} \qquad .....(1)$$

$$where\ b = \sqrt{\frac{W_n}{W_p}\frac{\mu_n}{\mu_p}} \qquad .....(2)$$

For a balanced inverter if we assume that b = 1 and $|V_{Tp}| = V_{Tn}$ then we have,

$$V_m = 1/2 \ V_{dd}$$

If the two inverting devices in the latch are matched, then by setting the inputs of the latch to 1/2 V_{dd} at t = 0, we can force the latch into a metastable state. A plot of the metastable operation of a nearly matched latch is shown in figure 7.

When the inverters are not matched, V_{m1} and V_{m2} for the two inverters must be calculated using the above equation and by setting the input nodes at the predetermined values, the latch can be operated in the metastable region. The exponential evolution of the voltages at the two output nodes can be expressed as,

$$\Delta V = \Delta V_0 \exp (\alpha t) \qquad .....(3)$$

where ΔV_0 is the initial voltage at the output node at t = 0. The resolving time constant is given by,

$$\alpha = \frac{\ln \Delta V - \ln \Delta V_0}{t} \qquad .....(4)$$

The metastable resolving time t can be determined by simulations. The resolving time constant α can be evaluated from the device parameters using [4],

$$\alpha = \sqrt{\frac{g_{m1} \, g_{m2}}{C_1 \, C_2}} \qquad .....(5)$$

where g_{m1} and g_{m2} are the transconductances of the two n-transistors and is given by

$$g_m = \frac{\mu_n \, \varepsilon}{t_{ox}} \frac{W_n}{L_n} (V_{gs} - V_{Tn}) \qquad .....(6)$$

C_m has very little effect on α but it affects the band width (BW) of the latch. For CMOS inverters, the metastability region is between V_{IL} and V_{IH} and can be calculated from the threshold voltages of the n- and p-transistors [10].

$$V_{IL} = \frac{3 \, V_{dd} - 3 \, |V_{Tp}| + 5 \, V_{Tn}}{8} \qquad .....(7)$$

$$= 2.25 \text{ V.}$$

$$V_{IH} = \frac{5\,V_{dd} - 5\,|V_{Tp}| + 3\,V_{Tn}}{8} \quad \text{.....(8)}$$

$$= 3.15 \text{ V.}$$

These are approximate values for $(\beta_n / \beta_p) = 1$, $V_{Tn} = 0.9$ V and $V_{Tp} = -0.5$ V. Using these values ΔV is approximately 0.90 V and we are justified in using the small signal model for the inverters at the metastable region.

4. Metastability simulations

The operation of the latch circuit as it enters the metastable state and the time evolution of the two outputs Q and Q' resulting the termination of metastability is of paramount importance in the design of synchronizers. A better understanding of the operation of the latch at the metastable state will help us to design a latch which is reliable and hardened against metastable operation.

Eight D-type latch circuits were designed using a CMOS 3 micron commercial process from Edinburgh Microfabrication Facility (EMF). The circuits were coded using SPICE and simulated using MOS LEVEL 3 parameters from EMF. By adjusting the edge of the input data (D) and the clock (EN) we can force the latch into a metastable state.

The plot given in figure 8 is that for the latch TX-NOR having a set-up time of 2.9 ns. It can be seen that output Q did not rise sufficiently before the -ve going edge of the clock and it failed to reach logic high after hovering at metastable voltage for more than 6 ns. It can be seen from plot in figure 9 for latch NAND-N3 that there is at least one interval at which Q and Q' will go into a metastable state with unbound delay time. Plots shown in figures 10 & 11 are metastable simulation plots for the latch circuits NAND-N3 and MX-GATE respectively. In both cases the metastability is found to last for over 12 ns.

The time interval between clock and data must be adjusted precisely close to few pico seconds or smaller to force the latch into the metastable state with both outputs

floating at half supply voltage. Since this was found to be a very time consuming method, a second method suggested in section three by which the input nodes were pre-set to the metastable voltage calculated from device parameters was employed successfully. This forced the latch into metastable state and the time evolution of the output node voltages were studied. The plots are shown in figures 12 and 13 and can be seen that the outputs are at about 2.5 volts at t=0 and evolve into low and high with time t. Determination of resolving time t from simulation plots can lead to the evaluation of α from equation (4).

4.1 Variation of resolving time with SPICE parameter ABSTOL

A number of simulations were carried out for determining the resolving time of the latch after forcing it into metastability. It was noted that when the value of ABSTOL option in the SPICE input deck is varied or if the transient time step is varied (using .TRAN statement), the resolving times plotted were found to differ substantially. This is due to the algorithm used by the SPICE program to force the nodal voltages to converge; a smaller error tolerance or smaller time step producing a different current and voltage convergence since the nodal voltages are very sensitive at the metastable state. The variations were found to be much more when the latch was forced into a metastable state by setting nodes to the metastable voltage at time t=0 and it was less sensitive when simulated with set-up time violations. A plot showing the variations in the plotted output nodal voltages for the former case is given in figure 14.

5. Conclusions

A flip-flop operated in the metastable region is found to be unreliable due to unusually long decision time encountered in fast submicron CMOS digital systems. The conditions under which the flip-flop tends to enter a metastable state has been investigated. A number of bistable circuits were designed and simulations were carried out within the metastable window in order to determine the circuits which are more susceptible to metastable operation.

Using small signal analysis and employing analytical methods, it is possible to calculate the metastable voltage

of cross coupled CMOS inverting devices. By presetting the inputs of these latches to the calculated metastable voltages, the flip-flops were forced into metastable operation. Repeated simulations using this technique led to the determination of the metastable resolving time. The resolving time constant α was determined from device parameters and this led to the design of flip-flops with minimum resolving time and hence improved reliability. The dependence of device parameters to metastability resolving time led to optimization of the device parameters leading to metastable hardened design of bistable elements which could be incorporated into fast, reliable VLSI systems.

It was established from metastable state simulations for the designed latch circuits that threshold voltage for the MOS transistors affect the metastable region. By adjusting the threshold voltages for the n- and p-transistors it is possible to improve metastability resolving for the latch circuits simulated. Other design constraints such as noise margins must be also taken into account when adjusting the threshold voltages for the devices. Inverting devices used in fast synchronizers must be designed to have high gain at the metastable region in order to reduce the resolving time.

6 References

[1]. S. T. Flanagan, "Synchronization reliability in CMOS technology", IEEE J. Solid-state Circuits, vol. sc-20, no. 4, pp. 880-882, Aug. 1985.

[2]. L. Kleeman and A. Cantoni, "Metastable behaviour in digital systems", IEEE D & T of Computers, pp. 4-19. Dec. 1987.

[3]. T. Kacprzak and A. Albicki, "Analysis of metastable operation in RS CMOS flip-flops", IEEE J. Solid-state Circuits, vol. sc-22, no. 1, pp. 57-64, Feb. 1987.

[4]. T. Sakurai, "Optimization of CMOS arbiter and synchronizer circuits with submicrometer MOSFET's, IEEE J. Solid-state circuits, vol. 23, no. 4, Aug. 1988.

[5]. J. U. Horstmann, H. J. W. Eichel and R. L. Coates, "Metastability behaviour of CMOS ASIC flip-flops in theory and test", IEEE J. of Solid-state circuits, vol. 24, no. 1, pp. 146-157, Feb. 1989.

[6]. L. Kim and R. Dutton, "Metastability of CMOS latch/flip-flop", IEEE J. Solid-state circuits, vol. 25, no. 4, Aug. 1990.

[7]. C. Mead and L. Conway, Introduction to VLSI systems, Addison-Wesley, 1980.

[8]. M. Shoji, CMOS Digital Circuit Technology, Prentice-Hall, 1988.

[9]. "Metastability, a study of the anomalous behaviour of synchronizer circuits", PAL Devices Data Book, vol-2, Advanced Micro Devices.

[10]. N. Weste, "Principles of CMOS VLSI Design, Addison-Wesley, 1985.

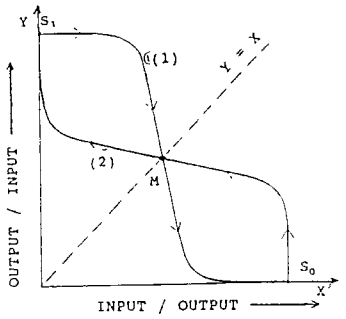

Fig 1. Flip-flop state transfer curve

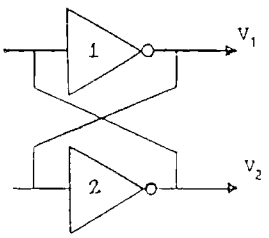

Fig 2. A simple latch

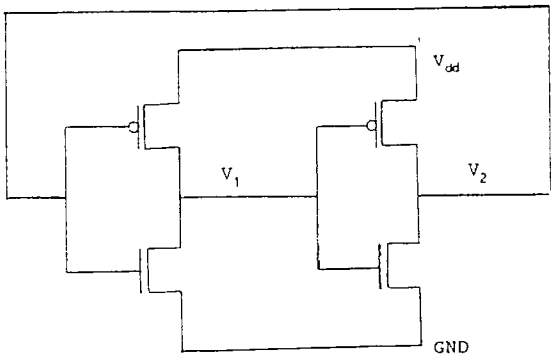

Fig 3. Transistor level circuit for the latc

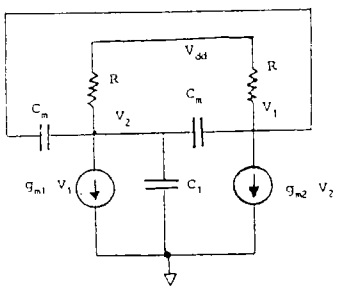

Fig 4. Small signal model of the latc

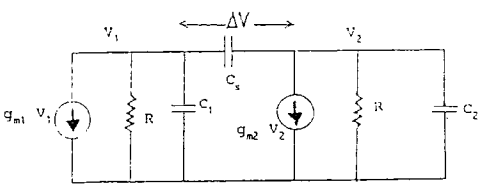

Fig 5. a.c. equivalent circuit of the latch

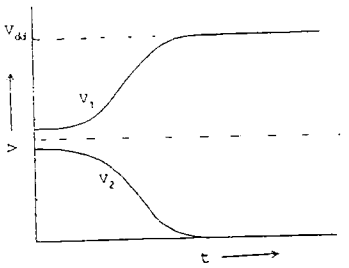

Fig 6. Voltage evolution at outputs of lat

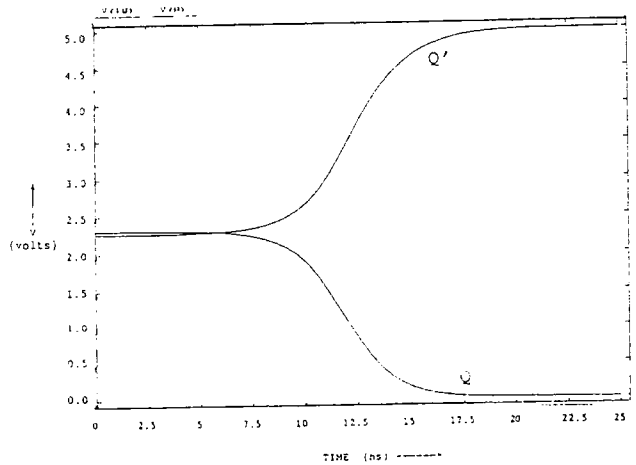

Fig 7. Metastable operation of a nearly matched latch

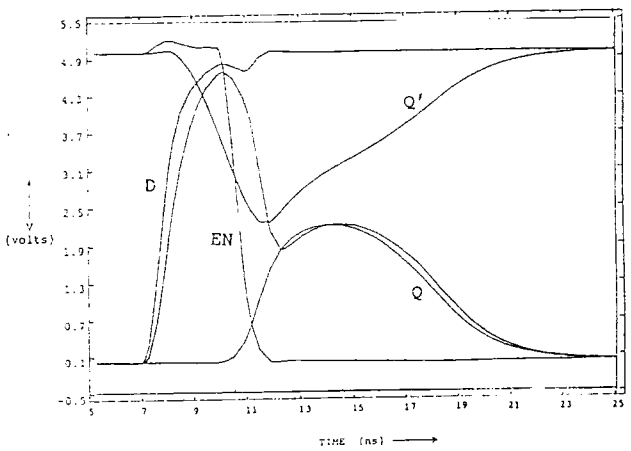

Fig 8. Metastable simulation for TX-NOR

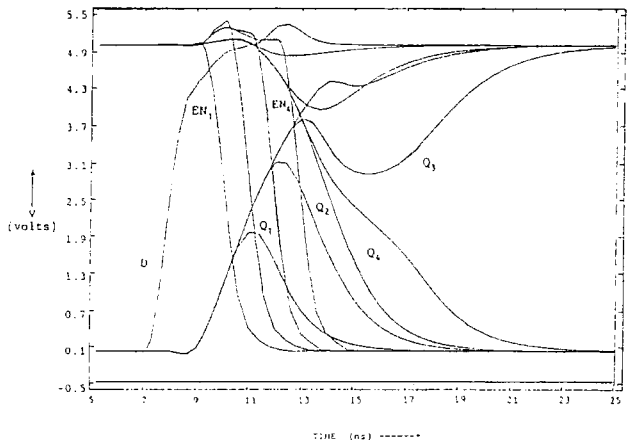

Fig 9. Metastability window for NAND-N3

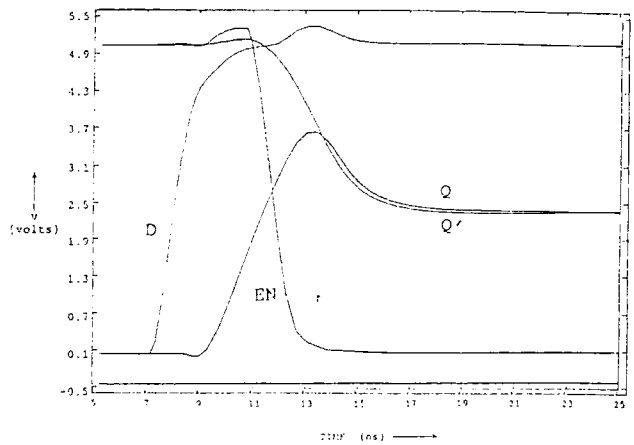

Fig 10. Metastability simulation for NAND-N3

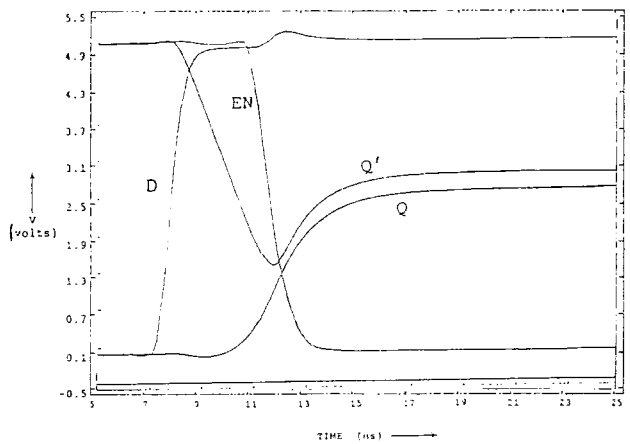

Fig 11. Metastability simulation for MX-GATE

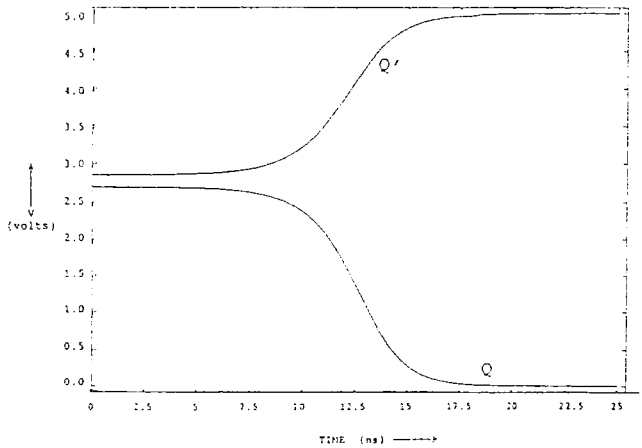

Fig 12. Metastability resolving for MX-GATE

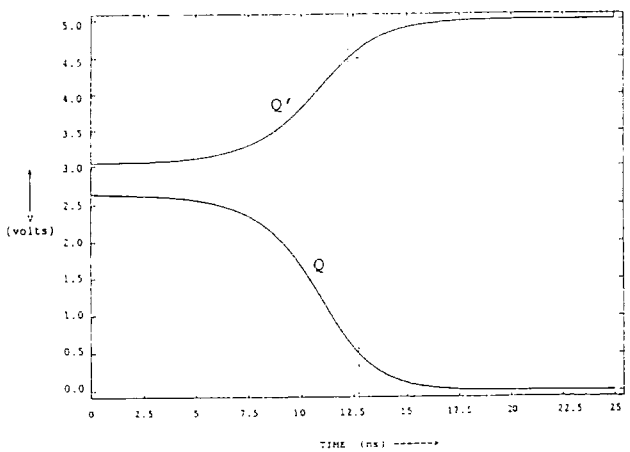

Fig 13. Metastability resolving for TX-NOR

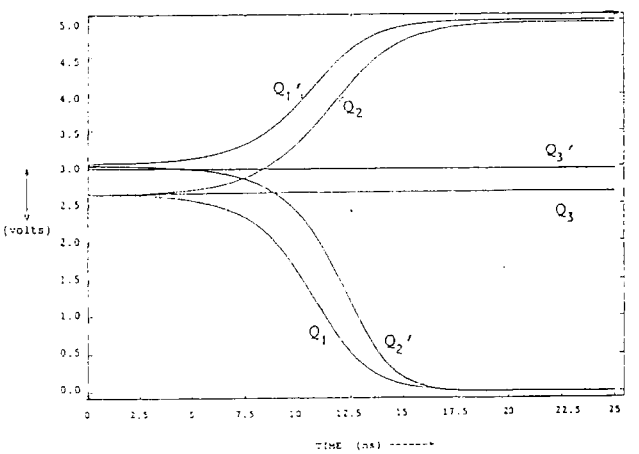

Fig 14. Variation of resolving time with ABSTOL

References

1.1 Pollino E., *The technological revolution and reliability,* Microelectronic reliability-vol II, Artech House Inc., M.A., U.S.A., 1989.

2.1 Takeda E., *Semiconductor reliability for the next century,* Physics World, March 1993, pp 48-52.

2.2 Mistry K., and Doyle B., *How do hot carriers degrade N-channel MOSFETs?,* IEEE Circuits & devices, Jan 95, pp 28-33.

2.3 Amerasekera E.A. and Campbell D.S., *Failure mechanisms in semiconductor devices,* John Wiley, 1987.

2.4 Lathrop J.W., *The changing nature of reliability physics,* Proc. of the 4th international workshop on physics of semiconductor devices, Madras, December 1987, pp 389-398.

2.5 Campbell D.S. and others, *Reliability behaviour of electronic components as a function of time,* 5th international conference quality in electronic componemts, Bordeaux, France, Oct 91, pp 41-48.

2.6 Rubio A., Kajihara S. and Kinoshita K., *Class of undetectable stuck-open branches in CMOS memory elements,* IEE proc. G, vol 139, no 4, Aug 92, pp 503-506.

2.7 Chakravarty S., *A characterization of robust test-pairs for stuck-open faults,* Journal of electronic testing: theory and applications, 1991, pp 275-286.

2.8 Ferguson F., Taylor M., and Larrabee T., *Testing for parametric faults in static CMOS,* Proc. of International test conference, 1990, pp 436-443.

2.9 Liu D.L., and McCluskey E.J., *Designing CMOS circuits for testability,* IEEE Design & Test, Aug 87, pp 43-49.

2.10 Chandramouli R., and Sucar H., *Defect analysis and fault modeling in MOS technology,* Proc International test conference, 1985, pp 313-320.

2.11 Courtois B., *Failure mechanism, fault hypothesis and analytical testing of LSI-NMOS (HMOS) circuits,* pro. VLSI'81, 1981, pp 341-350.

2.12 Pollino E., *The technological revolution and reliability,* Microelectronic reliability-vol II, Artech House Inc., M.A., U.S.A., 1989.

2.13 Goel A.K., *High speed VLSI interconnections, Modeling, analysis & simulation,* Wiley, 1994.

2.14 Burgess N., Wilkins D.R.J., Damper R.I. and Shaw S.J., *Fault effects in MOS circuits and their implications for digital circuit testing,* IEE Electronic design automation conference, March 84, pp 83-89.

2.15 Christiansen D., *Reliability,* IEEE Spectrum, October 81, pp 33-35.

2.16 Doyle E.A., *How parts fail,* IEEE Spectrum, October 81, pp 36-43.

2.17 Mangir T.E., *Sources of failures and yield improvement for RVLSI and WSI: part 1- Sources of failures and yield improvement for VLSI,* IEEE prc., vol 72, no 6, June 1984, pp 690-704.

2.18 Hawkins C.F., and Soden J.M., *Reliability and electrical properties of gate oxide shorts in CMOS ICs,* Proc. IEEE International test conference, 1986, pp 443-451.

2.19 Mouthaan T.J., Petrescu V., de Graaff H.C. and Verwey J., *Modelling of electromigration with focus on the early stages,* Proc. of ICSDT'96, Obninsk,Russia, May 96, pp 48-56.

3.1 Price P.J.,"Calculation of hot electron phenomena", S-S Electronics, vol 21, 1978, pp 9- 16.

3.2 Hilsum C, "Historical background of hot electron physics", S-S Electronics, vo 21, 1978, pp 5-8.

3.3 Lanyon H.P.D.,"Electron transport and ionization in silicon at high fields", S-S Electronics, vol 21,1978, pp 291-295.

3.4 Troutman R.R.,"Silicon surface emission of hot electrons", S-S Electronics, vol 21, 1978, pp 283-289.

3.5 Sze SM, "Physics of Semiconductor Devices", John Wiley, Canada, 1981.

3.6 Wang CT (Edited by), "Hot carrier-design considerations for MOS devices and circuits", Van Nostrand Reinhold 1992.

3.7 Chen M, Leung C, Cochran WT, Jungling W, Dziuba C, & Yang T, "Suppression of hot-carrier effects in submicrometer CMOS technology", IEEE Tran ED, v 35, no 12, Dec 88.

3.8 Weber W, & Reisinger H, "Failure mechanisms in VLSI circuits: Time dependent dielectric breakdown and hot carrier effects", 3rd European Symposium on electron devices, failure physics and analysis (ESREF'92) Oct 5, 1992.

3.9 Takeda E., *Semiconductor reliability for the next century,* Physics World, March 93, pp48-52.

3.10 Doyle B.S., Krakauer D.B., and Mistry K.R., *Examination of oxide damage during high-current stress of n-MOS transistors,* IEEE tran ED, vol 40, no 5, May 93, pp 980-985.

3.11 Doyle BS, & Mistry KR, "The characterization of hot-carrier damage in p-channel transistors", IEEE Tran ED-40, no 1, Jan 93, pp 152-156.

3.12 Ning TH, Cook PW, Dennard RH, Osburn CM, Schuster SE and Yu H, "1 μm MOSFET VLSI Technology: Part IV- Hot-Electron Design Constraints", IEEE tran ED-26, no 4, April 79, pp 346-353.

3.13 Tam S, Ko P and Hu C, "Lucky-Electron model of channel hot-electron injection in MOSFETs", IEEE Tran ED-31, no 9, Sept 84, pp 1116-1125.

3.14 Tam S and Hu C, "Hot-electron induced photon and photocarrier generation in silicon MOSFETs", IEEE Tran ED-31,no 9, Sept 84, pp 1264-1273.

3.15 Hu C, Tam S, Hsu F, Ko P, Chen T, & Terrill K, "Hot electron induced MOSFET degradation- model, monitor and improvement", IEEE Tran ED-32, no 2, Feb 85.

3.16 Leblebici Y and Kang S, "Modelling and simulation of hot-carrier induced device degradation in MOS circuits", IEEE J SS cks, vol 28, no 5, May 93, pp 585-595.

3.17 Heremans P, Bellens R, Groeseneken G, & Maes HE, "Consistent model for the hot-carrier degradation in n-channel and p-channel MOSFETs", IEEE tr ele dev v 35, no 12, Dec 88.

3.18 Lee M, "BSIM substrate current modeling", Memorandum No: UCB/ERL M86/49, University of California, Berkeley, CA 94720, 3 June 1986.

3.19 Chan TY, Ko PK and Hu C, "A simple method to characterize substrate current in MOSFETs", IEEE EDL-5, no 12, Dec 84, pp 505-507.

3.20 Liang C, Gaw H and Cheng P, "An analytical model for self-limiting behavior of hot-carrier degradation in 0.25-μm n-MOSFETs", IEEE EDL-13, no 11, Nov 92, pp 569-571.

3.21 Takeda E, Kume H, Toyabe T, & Asai S, "Submicrometer MOSFET structure for minimizing hot-carrier generation", IEEE Tran ED-29, no 4, April 82.

3.22 Tam S, Ko P, Hu C., and Muller R.S., *Correlation between substrate and gate currents in MOSFETs,* IEEE Tran ED-29, no 11, Nov 83, pp 1740- 1744.

3.23 Takeda E and Suzuki N, "An empirical model for device degradation due to hot-carrier injection", IEEE EDL-4, no 4, April 83, pp 111-113.

3.24 Sakurai T, Nogami K, Kakumu M and Iizuka T, "Hot-carrier generation in submicrometer VLSI environment", IEEE J SS Circuits, vol sc-21, no 1, Feb 86, pp 187-191.

3.25 Sodini C G, Ko P, and Moll J L, "The Effect of High Fields on MOS Device and Circuit Performance," IEEE Tran ED-31, No 10, October 84.

3.26 Velghe R.M.D.A., Klaassen D.B.M. and Klaassen F.M., Unclassified report NL-UR 003/94, MOS Model:9, Philips Research Laboratories, Eindhoven, Netherlands, January 1994.

3.27 Chen K, Saller S, Groves IA, & Scott D, "Reliability effects on MOS transistors due to hot-carrier injection", IEEE Tran ED-32, no 2, Feb 85.

3.28 Takeda E., Nakagome Y., Kume H., Suzuki N. and Asai S., *Comparison of characteristics of n-channel and p-channel MOSFETs for VLSI,* IEEE Tra ED-30, 1983, pp 675.

3.29 Park H, Lee K, & Kim C, "A new CMOS NAND logic circuit for reducing hot-carrier problems", IEEE J SS cts, v 24, no 4, Aug 89.

3.30 Quader K N, Minami E R, Huang W, Ko P K, and Hu C, "Hot Carrier Reliability Design Guidelines for CMOS Logic Circuits", IEEE J of SS cts, vol 29, No 3, March 94, pp 253-261.

3.31 Revil N, Cristoloveanu S and Mortini P, "Aging of optimized submicron MOSFETs under systematic DC, AC and alternating stress conditions", 3rd European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, October 92, pp 451-454.

3.32 Lee P, Kuo M, Ko P and Hu C, "BERT - Circuit Aging Simulator (CAS)", Memorandum No.UCB/ERL M90/2, 18 January 1990.

3.33 Hsu W, Sheu BJ, Gowda SM and Hwang C, "Advanced integrated circuit reliability simulation including dynamic stress effects", IEEE J SS Ckts vol 27, no 3,March 92, pp 247-257.

3.34 Kuo MM, Seki K, Lee PM, Choi JY, Ko PK and Hu C, "Simulation of MOSFET lifetime under AC hot-electron stress," IEEE tran ED-35, no 7, July 88, pp 1004-1011.

3.35 Mistry K & Doyle B, "AC versus DC hot-carrier degradation in n-channel MOSFETs", IEEE Tran ED-40, no 1, Jan 93, pp 96-104.

3.36 Jeng M, Lee P, Kuo M, Ko P and Hu C, "Theory, Algorithms and User's Guide for BSIM and SCALP", Memorandum No. UCB/ERL M87/35, 28 May 1987.

3.37 Tu R, Rosenbaum E, Chan W and others, "Berkeley Reliability Tools- BERT", IEEE Tran CAD-12, no 10, October 93, pp 1524-1533.

3.38 Tu R, Rosenbaum E, Li C, Chan W, Lee P, Liew B, Burnett D, Ko P and Hu C, "BERT - Berkeley Reliability Tools", Memorandum No. UCB/ERL M91/107, 4 December 1991.

3.39 Sheu BJ, Hsu W and Lee BW, "An integrated circuit reliability simulator - RELY," IEEE J SS circuits, vol 24, No 2, April 89, pp 473-477.

3.40 Lunenborg M.M, Wolbert P.B.M., Meijer P.B.L. and others, "PRESS- A circuit simulator with built-in reliability model for hot-carrier degradation", ESREF'93, pp 157-161.

3.41 Lunenborg M.M., *MOSFET Hot-Carrier Degradation, Failure mechanisms and models for reliability circuit simulation,* Ph.D. thesis, University of Twente, Netherlands, 1995.

3.42 Gaensslen FH, & Aitken JM, "Sensitive technique for measuring small MOS gate currents", IEEE EDL-1, no 11, Nov 80.

3.43 Meta-Software, HSPICE user's manual, Meta-Software Inc., Campbell, CA, 1992.

3.44 Velghe. R.M.D.A., Klaassen D.B.M., and Klaassen F.M., *Philips MOS Model:9, Unclassified report NL-UR 003/94,* Philips Electronics, Netherlands, 1994.

4.1 Vladimirescu, A and others (1981) "SPICE version 2G.5 user's guide" Department of Electrical Engineering and Computer Sciences, University of California, Berkeley.

4.2 Meta-Software, HSPICE user's manual, Meta-Software Inc., Campbell, CA, 1992.

4.3 Morant, M. J., "Integrated Circuit Design and Technology" Chapman and Hall, UK, 1990.

4.4 West N., and Eshraghian K., *Principles of CMOS VLSI Design,* Addison-Wesley, USA, 1985.

4.5 Uyemura J.P., *Fundamentals of MOS Digital Integrated Circuits,* Addison-Weslay, USA, 1988.

4.6 Shoji M., CMOS Digital Circuit Technology, Prentice-Hall, 1988.

4.7 Kim L., and Dutton R.W., *Metastability of CMOS Latch/Flip-flop,* IEEE J of S-S Circuits, v-25, no:4, Aug 1990, pp 942-950.

4.8 Antognetti and Massobrio (1988) "Semiconductor Device Modeling with SPICE" McGraw-Hill, USA.

4.9 Advanced Micro Devices, *Metastability a study of the anomalous behavior of synchronizer circuits,* PAL devices data book vol 2, Advanced Micro Devices.

4.10 Pulfrey, D L and Tarr, N G (1989) "Introduction to Microelectronic Devices" Prentice-Hall, UK.

4.11 Geiger, R L (1990) "VLSI design techniques for analog and digital circuits" McGraw-Hill, USA.

4.12 Tuinenga, P W (1988) "SPICE : a guide to circuit simulation and analysis using PSpice" Prentice-Hall, UK.

4.13 Vladimirescu, A and Liu, S (1980) "The simulation of MOS Integrated circuits using SPICE 2", Memorandum No: UCB/ERL M80/7, University of California, Berkeley.

4.14 Walczowski L., Waller W. and Wells E., *CHIPWISE user guide and reference,* University of Kent, Canterbury, UK.

5.1 Leblebici Y. and Kang S., *Modeling of nMOS transistors for simulation of hot-carrier induced device and circuit degradation,* IEEE tr. CAD, vol 11, no:2, Feb 92, pp 235-246.

5.2 Heremans P., Bellens R., Groeseneken G. ans Maes H.E., *Consistent model for the hot carrier degradation in n-channel and p-channel MOSFETs,* IEEE tr. ED, v 35, no: 12, Dec 88, pp 2194-2208.

5.3 Weber W., *Dynamic stress experiments for understanding hot carrier degradation phenomena,* IEEE tr. ED, v 35, no: 9, Sept 88, pp 1476-1485.

5.4 Shoji M., *CMOS digital circuit technology,* Prentice-Hall, USA, 1988.

5.5 Lunenborg M., *MOSFET hot carrier degradation, failure mechanisms and models for reliability circuit simulation,* Ph.D. thesis, University of Twente, Netherlands.

6.1 I. Catt, "Time loss through gating of asynchronous logic signal pulses", IEEE Tran. Electron. Comput., vol EC-15, pp. 108-111, Feb. 1966.

6.2 T. J. Chaney and C. E. Molnar, Anomalous behaviour of synchronizer and arbiter circuits", IEEE Trans. Computers, vol. c-22, no.4, pp. 421-422, April 1973.

6.3 G. R. Couranz and D. F. Wann, "Theoretical and experimental behaviour of synchronizers operating in the metastable region", IEEE Tran. Computers, vol. c-24, no. 6, pp. 604-616, June 75.

6.4 M. Pechoucek, "Anomolous response times of input synchronizers", IEEE Tran. Computers, vol. c-25, no. 2, pp. 133-139, Feb. 1976.

6.5 T. Chaney and F. Rosenberger, "Characterization and scaling of MOS flip-flop performance in synchronizer applications", Caltech Conference on VLSI, pp. 357-374, Jan. 1979.

6.6 T. Chaney, "Comments on a note on synchronizer or interlock maloperation", IEEE Tran. Computers Vol C28, Oct. 1979.

6.7 W. Fleischhammer and O. Dortek, "The anomalous behaviour of flip-flops in synchronizer circuits", IEEE Tran Computers vol C-28, no. 3, pp. 273-276, March 1979.

6.8 H. Veendrick, "The behaviour of flip-flops used as synchronizers and prediction of their failure rate", IEEE J. Solid-state Circuits, vol. sc-15, no. 2, pp. 169-176,April 80.

6.9 L. Marino, "General theory of metastable operation", IEEE tran. Computers, vol. c-30, no. 2, pp. 107-115, February 1981.

6.10 F. Rosenberger and T. J. Chaney, "Flip-flop resolving time test circuit", IEEE J. Solid-state circuits, vol. sc-17, no. 4, pp. 731-738, August 1982.

6.11 P. Stoll, "How to avoid synchronization problems", VLSI Design, pp. 56-59, Nov/Dec. 1982.

6.12 J. Hohl, W. Larsen and L. Schooley, "Prediction of error probabilities for integrated digital synchronizers", IEEE J. Solid-state circuits, vol. sc-19, no. 2, pp. 236-244, Apr. 1984.

6.13 S. T. Flanagan, "Synchronization reliability in CMOS technology", IEEE J. Solid-state Circuits, vol. sc-20, no. 4, pp. 880-882, Aug. 1985.

6.14 L. Kleeman and A. Cantoni, "Metastable behaviour in digital systems", IEEE D & T of Computers, pp. 4-19. Dec. 1987.

6.15 T. Kacprzak and A. Albicki, "Analysis of metastable operation in RS CMOS flip-flops", IEEE J. Solid-state Circuits, vol. sc-22, no. 1, pp. 57-64, Feb. 1987.

6.16 T. Sakurai, "Optimization of CMOS arbiter and synchronizer circuits with submicrometer MOSFET's, IEEE J. Solid-state circuits, vol. 23, no. 4, Aug. 1988.

6.17 J. U. Horstmann, H. J. W. Eichel and R. L. Coates, "Metastability behaviour of CMOS ASIC flip-flops in theory and test", IEEE J. of Solid-state circuits, vol. 24, no. 1, pp. 146-157, Feb. 1989.

6.18 L. Reyneri, D. Corso and B. Sacco, "Oscillatory metastability in homogeneous and inhomogeneous flip-flops", IEEE J. Solid-state circuits, vol.25, no.1, pp. 254-264, February 1990.

6.19 L. Kim and R. Dutton, "Metastability of CMOS latch/flip-flop", IEEE J. Solid-state circuits, vol. 25, no. 4, Aug. 1990.

6.20 C. Mead and L. Conway, Introduction to VLSI systems, Addison-Wesley, 1980.

6.21 M. Shoji, CMOS Digital Circuit Technology, Prentice-Hall, 1988.

6.22 Advanced Micro Devices, "Metastability, a study of the anomalous behaviour of synchronizer circuits", PAL Devices Data Book, vol-2., Advanced Micro Devices.

6.23 N. Weste, "Principles of CMOS VLSI Design, Addison-Wesley, 1985.

6.24 Jerry Jex and Charles Dike, *A fast resolving BiNMOS Synchronizer for Parallel processor interconnect,* IEEE J. Solid-state circuits, vol 30, no 2, February 1995, pp 133-139.

6.25 W.A.M. Van Noije, W.T. Liu and J.N. Navarro S.,Jr., *Precise final state determination of mismatched CMOS latches,* IEEE J. Solid-state circuits, vol 30, no 5, May 1995, pp 607-611.

6.26 C.L. Portmann and T.H.Y. Meng, *Metastability in CMOS library elements in reduced supply and technology scaled applications,* IEEE J. Solid-state circuits, vol 30, no 1, Jan 1995, pp 39-46.

6.27 John P. Uyemura, *Fundamentals of MOS Digital Integrated Circuits*, Addison-Wesley, U.S.A., 1988.

6.28 MicroSim, *MicroSim PSpice A/D Circuit Analysis Reference Manual,* MicroSim Corporation, USA, April 1995.

8.1 O'Connor P.D.T., *Practical reliability engineering,* 3rd edn., John Wiley, UK.

8.2 Kececioglu D., *Reliability Engineering Handbook, vol 2, Prentice-Hall Inc, USA, 1991.*

9.1 Chatterjee P.K., Hunter W.R., Amerasekera A., Aur S., Duvvury C., Nicolian P.E., Ting L.M. and Yang P., *Trends in Deep submicron VLSI and their implications for reliability,* IEEE Proc., 1995, pp 1-11.

9.2 A D&T Roundtable, *Deep-Submicron Test,* IEEE Design and Test of Computers, Fall 1996, pp 102-108.

9.3 Diaz Carlos H, Kopley Thomas E and Marcoux Paul J, *Building-in ESD-EOS reliability for sub-halfmicron CMOS processes,* IEEE Tr ED, v-43, no:6, June 96, pp 991-999.

9.4 Sun Jie J, and others, *The effect of the elevated source/drain dopping profile on performance and reliability of deep submicron MOSFETs,* IEEE Tr ED v-44, no:9, Sept 97, pp 1491-1497.

9.5 Chan Vei-Han and Chung James E, *Two-stage hot-carrier degradation and its impact on submicrometer LDD NMOSFET lifetime prediction,* IEEE Tr ED, v-42, no:5, May 1995, pp 957-962.

9.6 Raychaudhuri A and others, *Features and mechanisms of the saturating hot-carrier degradation in LDD NMOSFETs,* IEEE Tr ED v-43, no: 7, July 96, pp 1114-1121.

9.7 Gonzalez R and others, *Supply and threshold voltage scaling for low power CMOS,* IEEE J SS circuits v-32 no: 8, August 97, pp 1210-1216.