Characterisation of crosstalk defects in submicron CMOS VLSI interconnects

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Abstract

The main problem addressed in this research work is a crosstalk defect, which is defined as an unexpected signal change due to the coupling between signals or power lines. Here its characteristic under 3 proposed models is investigated to find whether such a noise could lead to real logic faults in IC systems. As a result, mathematical analysis for various bus systems was established, with 3 main factors found to determine the amount of crosstalk: i) how the input buffers are sized; ii) the physical arrangements of the tracks; and iii) the number of switching tracks involved. Minimum sizes of the width and separation lead to the highest crosstalk while increasing in the length does not contribute much variation. Higher level of crosstalk is also found in higher metal layers due mainly to the reduced capacitance to the substrate. The crosstalk is at its maximum when the track concerned is the middle track of a bus connected to a weak buffer while the other signal lines are switching. From this information, the worse-case analysis for various bus configurations is proposed for 0.7, 0.5 and 0.35 μ CMOS technologies. For most of conventional logic circuits, a crosstalk as large as about a half of the supply voltage is required if a fault is to occur. For the buffer circuits the level of crosstalk required depends very much on the transition voltage, which is in turn controlled by the sizing of its n and p MOS transistors forming the buffer. It is concluded that in general case if crosstalk can be kept to be no larger that 30% of the supply voltage the circuit can be said to be very reliable and virtually free from crosstalk fault. Finally test structures are suggested so that real measurements can be made to verify the simulation results

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CHAPTER 1 *Introduction*

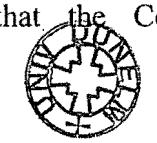
1.1 General Introduction

In the modern world, integrated circuits play a significant role in the electronics industry. The ability to integrate millions of transistors into a single chip offers enormous advantages in terms of yield and performances, allowing more complex systems to operate at higher speed with less power. In the earlier days circuit performance was mainly determined by the switching characteristics of its transistors. But as efforts have been made to increase circuit density by shrinking the transistor size further, undesired effects due to interconnections, which were regarded as insignificant in the past, must now be taken into account. These effects, as will be seen later, can be of various forms, such as delay or noise.

The main problem addressed in this research work is crosstalk defects, which are defects caused by one form of the noise called crosstalk. Generally, crosstalk is defined as an unexpected signal change due to the coupling between signal or power lines. For any engineer or designer designing an integrated circuit, the ability to predict or estimate the amount and nature of crosstalk likely to occur is desirable, at least from a reliability point of view. The scope of this research work is therefore to investigate the characteristics of the crosstalk which occurs in integrated circuits and to underline the effect of this on CMOS circuits. A test structure will also be suggested so that real measurements can be made to verify the simulation results.

1.2 Introduction to important concepts in submicron CMOS circuits

It is essential to understand the trend of CMOS technology in order to appreciate the reasons behind the emergence of this relatively new problem. The transistor has come a long way since it was first integrated into a semiconductor microchip in 1958. Generally it has now been accepted that the Complementary Metal Oxide



Semiconductor (CMOS) Field Effect Transistor is the technology of choice for digital circuits. This is largely due to its low power nature, as most of the power consumption occurs only during the switching period, and to the fact that its switching speed has been vastly improved to a level comparable to that offered by other families of transistors such as bipolar devices. There are actually several ways in which this improvement in speed can be achieved. One of the main method is by reducing the transistor size, which is measured in term of the minimum channel length. Figure 1 shows the technological trend of CMOS and its future prediction[41]. Features as small as 0.28 μm are being used in today consumer products such as the recently launched Intel's PentiumII and research is well underway for sub 0.1 μm devices, moving us into the nanotechnology and the era of ULSI (Ultra Large Scale Integration).

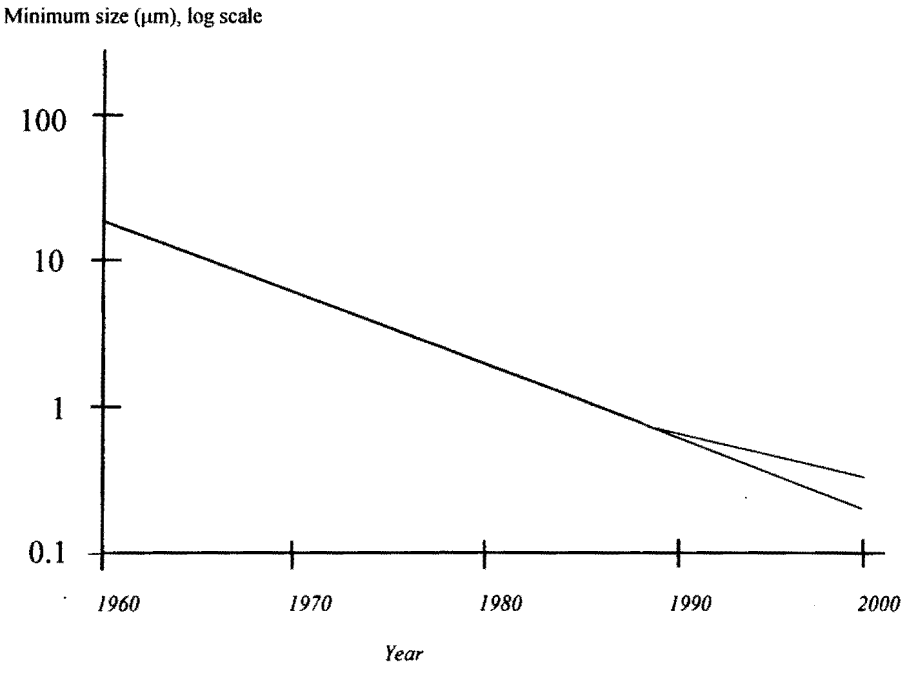


Figure1. Technology trend in CMOS

To illustrate how this reduction in transistor size can result in speed increasing, table1 shows the effects of *ideal* scaling, where the MOS device is equally scaled in five dimensions- the three physical dimensions, voltage supply level and doping concentration, on various transistor parameters. In this *ideal* scaling, the electric filed pattern of the smaller device is identical to that of the larger one.

Parameter	Scaling Factor
Dimensions (W, L, t_{ox}, X_j)	1/S
Substrate doping (N_{SUB})	S
voltages (V_{DD}, V_{TN}, V_{TP})	1/S
Current per device($I_{DS} \alpha \frac{W}{L}\frac{\varepsilon_{ox}}{t_{ox}}(V_{DD}-V_t)^2$)	1/S
Gate capacitance($C_g = \varepsilon_{ox}\frac{WL}{t_{gox}}$)	1/S
Transistor on-resistance ($R_{tr} \alpha \frac{V_{DD}}{I_{DS}}$)	1
Intrinsic gate delay ($\tau = \frac{C_g \Delta V}{I_{av}} = R_{tc} C_g$)	1/S
Power-dissipation per gate (P = IV)	$1/S^2$
Power-delay product per gate ($P \times \tau$)	$1/S^3$
Area per device (A = WL)	$1/S^2$
Power-dissipation density (P/A)	1

Table1 Scaling of MOS transistor

It can be observed from the table that as the dimensions of the transistor are scaled down by a factor of S the intrinsic gate delay which dictates the speed of the circuit is also reduced by the same factor. Thus the circuit can potentially be operated at higher speed. Ideally, according to the table, the supply voltage is also scaled down and hence the circuit would consume less power. This is, however, not always the case as it would be difficult and costly in practise, even though possible, to have multiple supply voltages. The topic regarding transistor scaling will be discussed in more detail in the next chapter. It is sufficient enough here to appreciate the basic idea behind transistor scaling and its main benefits in terms of packing density and increasing in speed.

Digital integrated circuits, however, do not contain only transistors. There exist also the second basic components; the interconnections. The term interconnection in integrated circuits is generally used to describe metal tracks which connect the transistors together to form circuits. The basic tracks structures and parameters are as shown in figure 2. The fact that the tracks lie above the substrate and are separated from it by a dielectric, SiO_2 in a typical IC, means that they will possess a self capacitance (capacitance to the substrate). In earlier technology this wiring capacitance is much less than that of the gate capacitance. For example, 7 μm NMOS technology would typically have a gate capacitance of 20fF per minimum size of transistor. A transistor with W/L = 20 would therefore have a gate capacitance of 400fF. With the die size of the chip typically only a couple of mm^2, a line longer than 1mm is not very likely. One millimetre of the track would contribute only 200fF, hence less than that of the transistor gate. Generally therefore for the older technology such as the 7 μm, circuit behaviour is dominated by the transistor gate capacitance. This is obviously not true for smaller technologies. A 0.7 μm technology would have its gate capacitance of only 40fF(W/L = 20), still much less than that of the line even though the wiring capacitance is also changed because of the change in t_{ox}. The behaviour, especially the speed, of the circuit in this case is clearly dictated by the lines rather than the transistors themselves.

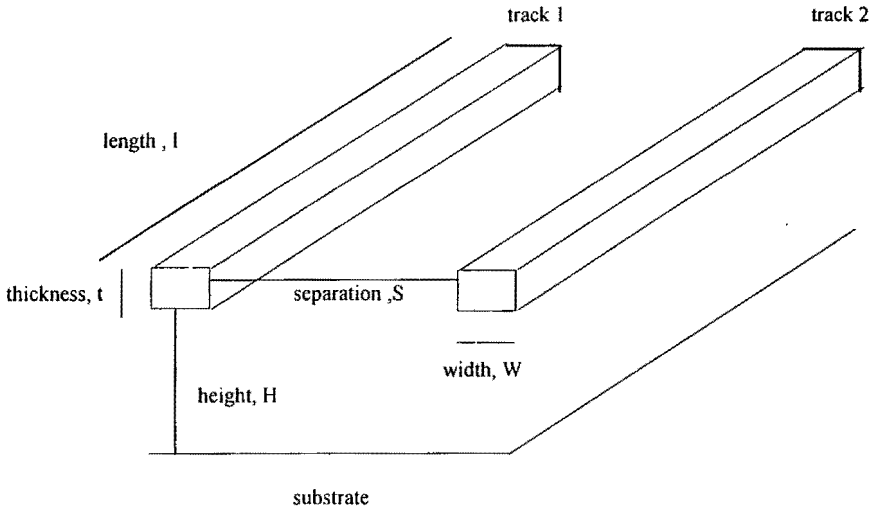


Figure2 Basic interconnection parameters

When transistors are scaled down, all the interconnects will also be reduced by the same factor. It is interesting to note that even though the packing density is increased as a result of scaling, the actual die size is likely to be increased. This is due to the modern demand for much more complex circuits making it very difficult to retain the die size even with the improved packing density. This leads to two concepts of interconnections: a local interconnect where it obeys the scaling rule and a global interconnect where its length is actually increased by the same scale as the dimension of the die. Table 2 summarises the scaling effects on interconnects.

Parameter	Scaling factor
Cross sectional dimensions (W_{int} ,H_{int}, t_{ox})	1/S
Resistance per unit length($R_{int} = \rho_{int} \frac{1}{W_{int} H_{int}}$)	S^2
Capacitance per unit length($C_{int} = \varepsilon_{ox} \frac{W_{int}}{t_{ox}}$)	1
RC constant per unit length ($R_{int}C_{int}$)	S^2
Local interconnect length(l_{int})	1/S
Local interconnection RC delay ($R_{int}C_{int}l^2_{loc}$)	1
Die size (D_c)	S_C (chip scale factor)
Global interconnection length (l_{int})	S_C
Global interconnection RC delay ($R_{int}C_{int}l^2_{int}$)	$S^2S_C^2$
Transmission line time flight (l_{int}/v_C)	S_C

Table2 Ideal Scaling of Local and Global interconnections

It can be seen from the table that global interconnects which apply to any long bus lines in the circuit have their delays increased where as in the local interconnect case, the delay remains the same. The increase in delay will slow down the circuit and may even cause problems for some asynchronous designs. In addition to this, since the global interconnect delay $S^2S_C^2$ is actually independent of driver size, it can not be solved by simply increasing the driver size.

The problem associated with scaling of interconnects is not only confined to signal delay. In reality vertical parameters such as the line thickness H_{int} and the height of the line above the substrate T_{ox} are not actually scaled down as much as that in the vertical plane due to difficulties in processing. The relatively larger H_{int} and T_{ox} make the capacitive coupling between the lines which were negligible in larger technologies more significant. The effects of these scaled interconnects and transistors on the capacitive coupling between lines are investigated in detail in the next chapters and it is the aim of this work to observe and explain the faults caused by such a noise.

1.3 Previous work in the field

The problem of capacitive coupling between lines causing crosstalk is not new. It has long been studied extensively in microwave and RF circuits. A number of papers have also been reported for case of the crosstalk in digital TTL and ECL circuits [1][2] [3]. These results can not, however, be applied directly to the modern CMOS ICs as they tended to treat the interconnects as a lossless lines and to neglect the line capacitance. It is interesting to note that when it comes to VLSI circuits, research has been concentrated mainly on how to achieve an accurate model for the track. Some of the first papers which reported these modelling methods are [4][5][6][7]. Specialised textbook such as that by Goal[8] talks exclusively about modelling and simulation of VLSI interconnects. Research has also been carried out at the University of Durham on the modelling of interconnect and this project builds on the results presented by Mahoney [9]. Even the most recent papers such as those of N.D Arora or N.D. Delorme [10][11] still give an emphasis on accurate modelling of the tracks. The importance of theses papers to this research is that they provide a suitable track model which is required for accurate simulation of crosstalk.

1.4 Thesis outline

The thesis is organised into 6 Chapters:

CHAPTER 1 is a general introduction. It provides the basic idea of crosstalk and its potentially damaging effects on integrated circuits. It also illustrates how the problem

has been raised and what kind of work has been going on regarding it. The chapter provides the aim of the thesis and it's organisation.

CHAPTER 2 It is very important to have accurate models for the transistors and tracks which are to be used for crosstalk measurements based on simulations. Chapter 2 therefore gives extensive discussion about various ways in which transistor and track models can be realised. This can be problematic especially for the modelling of tracks as the methods vary considerably depending on the school of thought. Suitable models are chosen and will be used throughout the research work.

CHAPTER 3 and 4 deal with the characterisation of crosstalk. Once suitable models have been established, investigations are carried out to observe how crosstalk can be influenced by physical parameters of the track such as its length or its thickness, and by transistor parameters such as its size or supply voltage. Various circuit layouts, investigating the number of lines and irregular line structures are also considered. As a result of these investigations, mathematical equations describing various relationships between the crosstalk and certain circuit parameters are given. Susceptibility analysis will also be disscussed as a useful first-hand analysis for any designer concerned with the crosstalk effects.

CHAPTER 5 Having established a knowledge of the characteristics of the crosstalk which may occur in CMOS circuits, the next step is to investigate whether this crosstalk can result in any serious logic faults. It will be seen that it is indeed possible under certain circumstances for logic faults to occur. Examples are given and ways to reduce this effect are discussed.

CHAPTER 6 All the work presented so far has been under simulations. It is, however quite important to verify the simulation results with the values obtained by real measurement if they are to be proved reliable. Measuring real crosstalk is not straight forward and a special test circuit may be needed. A simple yet effective test circuit is proposed here and its method is tested by SPICE simulation.

CHAPTER 7 is a conclusion. It concludes and summarise all the work done within this research. Further work which could complement and contribute more in depth regarding this topic are also suggested.

CHAPTER 2 *Modelling of transistors and interconnects*

Once it has been decided that crosstalk may have significant effect on integrated circuit reliability and that the understanding of its characteristics is desirable, a question is raised: How can we actually measure the crosstalk? One answer which seems quite straight forward at first is that this can be done by fabricating some real sample circuits of different parameters and then taking measurements from them. This method however would require a lot of sample circuits and is likely to be time consuming and high cost. Measuring the crosstalk directly from the sample chips itself may not even be as simple as it may seem and that special test circuit may be required. This method does not look after all to be very promising.

The alternative is to use simulation. Computer Aided Design (CAD) has been revolutionary to the electronic industries. With programmes such as SPICE (Simulation Programme with Integrated Circuit Emphasis), originally developed by the University of California in Berkeley, having proved to be a backbone for circuit designs. Using this programme, designers are provided with opportunities to try and test their circuits extensively to make sure that they function as expected before they are fabricated.

However, in order to use CAD simulation as a mean for initial design and verification of the circuit, it is necessary that the characteristics of all components within the circuits are correctly represented. In other words, this means that all the components must be correctly 'modelled' according to their real behaviour. For crosstalk simulation this implies that the two main components, the transistors and their interconnects must be correctly modelled. The next sections therefore discuss various methods under which transistor and interconnects models can be realised.

2.1 Modelling of the MOS transistor

The characteristics of any particular transistor depend greatly on its technology, or more precisely on how it has been processed. SPICE allows process and device parameters to be used to represent or 'model' any unique transistor. These parameters are normally obtained from measurements of the real device. They will provide a wide range of information about the device which can vary from any physical parameters such the oxide thickness to device characteristics such as its threshold voltage or mobility.

There are actually several levels of accuracy/complexity at which transistors can be modelled. Level 1 is the starting level where a small number of parameters are required. This level should prove to be enough for a very basic transistor. Higher levels require additional parameters but will result in a more accurate simulation of circuit behaviour. These levels are therefore naturally suitable for more advanced transistors. Typically, LEVEL3 is adequate for most of the transistors including those from sub-micron processes. For a very deep sub-micron transistor such as 0.1μm, new models are being developed. Table 3 shows typical CMOS device parameters and their SPICE correspondence.

2.2 Scaling of MOS transistor

Given the availability of any particular MOS transistor model, other smaller and more advanced models can in theory be derived using methods governed by scaling rules. Ideally, these new 'theoretically scaled' transistors would still maintain certain expected characteristics. Within each scaling rule, scaling of a MOS transistor is done by adjusting (i.e. dividing) some scaleable parameters of the transistor by certain values (scaling factors). Different scaling rules consist of different combination of scaling factors. The ideal scaling rule shown earlier, also known as the Constant Electric Field scaling, is actually just one of three popular rules currently used. Table 4 summarise the three methods, which are:

1. Constant Voltage scaling (CV) [12]
2. Constant Electric Field scaling (CE) [13]
3. Quasi-Constant Voltage scaling (QCV) [12]

Parameter	SPICE keyword	Description
-	LEVEL	Model level
V_{TO}	VTO	Zero-bias threshold voltage
t_{ox}	TOX	Gate oxide thickness
N_a	NSUB	Substrate doping
N_{FS}	NFS	Surface fast state doping
μ_o	UO	surface mobility
υ_{max}	VMAX	Maximum drift velocity of carries
η	ETA	Static feedback on threshold voltage
κ	KAPPA	Saturation field factor
θ	THETA	Mobility degradation factor
δ	DELTA	Width effect on threshold voltage
x_j	XJ	Junction depth
C_j	CJ	Zero-bias bulk junction capacitance
J_s	JS	Bulk junction saturation current
J_{sw}	JSW	Sidewall bulk junction saturation current
M_j	MJ	bulk junction grading coefficient
$\varnothing_j$	PB	junction potential
C_{jsw}	CJSW	Zero-bias side wall capacitance
M_{jsw}	MJSW	Sidewall capacitance grading coefficient
C_{GDO}	CGDO	Gate-drain overlap capacitance
C_{GSO}	CGSO	Gate-source overlap capacitance
C_{GBO}	CGBO	Gate-bulk overlap capacitance
-	RD	Drain ohmic resistance
-	RS	Source ohmic resistance
L_d	LD	Lateral diffusion from drain to source
W_d	WD	Lateral diffusion along the line

Table 3 Typical CMOS device parameters and their SPICE correspondence

Parameter	CE	CV	QCV
Dimensions (W, L, t_{ox}, X_j)	1/S	1/S	1/S
Substrate doping (N_{SUB})	S	S	S
voltages (V_{DD}, V_{TN}, V_{TP})	1/S	1	$1/S^{0.5}$
Current per device($I_{DS} \alpha \frac{W}{L}\frac{\varepsilon_{ox}}{t_{ox}}(V_{DD}-V_t)^2$)	1/S	S	$S^{0.25}$
Gate capacitance($C_g = \varepsilon_{ox}\frac{WL}{t_{gox}}$)	1/S	1/S	1/S
Transistor on-resistance ($R_{tr} \alpha \frac{V_{DD}}{I_{DS}}$)	1	1/S	$1/S^{0.75}$
Intrinsic gate delay ($\tau = \frac{C_g \Delta V}{I_{av}} = R_{tc} C_g$)	1/S	$1/S^2$	$1/S^{0.875}$
Power-dissipation per gate (P = IV)	$1/S^2$	$S^{0.5}$	$1/S^{0.25}$
Power-delay product per gate ($P \times \tau$)	$1/S^3$	$1/S^{0.75}$	$1/S^2$
Area per device (A = WL)	$1/S^2$	$1/S^2$	$1/S^2$
Power-dissipation density (P/A)	1	$S^{1.5}$	$S^{1.75}$

Table4 Scaling laws of MOS device

It can be seen that the Constant Electric Field scaling (CE) is termed 'ideal' largely from the device physics point of view. By scaling the device in both horizontal and vertical dimensions the device size is dramatically reduced by the factor of S^2 and the gate delay is also significantly improved. Practising the CE scaling, however, can be troublesome. Since each technology would requires different supply voltage, any electronic system which comprises chips of different technologies such as the PC board would require multiple power supplies. This can prove to be very ineffective and costly.

The Constant Voltage scaling (CV), by contrast, offers a more practical solution. In this scheme, the dimensions are scaled while the voltages are kept constant allowing a single level supply source to be used. As a result, the Constant Voltage scaling has

actually been one of the most commonly used. It must be pointed out however that the normal operating voltage of 5 volts used in most electronics circuit can not be applied to any CMOS of technology smaller than 0.6 micron. This is due to the effects such as hot carriers, junction or oxide breakdown which would degrade the device reliability. For smaller devices therefore reduction in supply voltage is unavoidable. The other alternative, the Quasi-Constant Voltage scaling (QCV) scheme is regarded as an intermediate scheme between the CE and CV. Here the dimensions are scaled by 1/S while the voltages are by $1/S^{0.5}$.

In practise, scaling rules have been only used as a reference for development of new models. It would be unwise to create a new SPICE model directly based on an available model with the use of a certain scaling rule. Because there are a number of device parameters which are process dependent and not covered by the rule, using these in the new model could result in incorrect device characteristics. The SPICE models of transistors, therefore are normally obtained from direct measurements or provided by companies or research institutes who created them. The work done here was based on there models available at the department; the 0.7, 0.5 and 0.35 microns. All the simulation has been run using the PSpice package which is one of the commercial versions of the original SPICE. PSpice is a product of MicroSim.

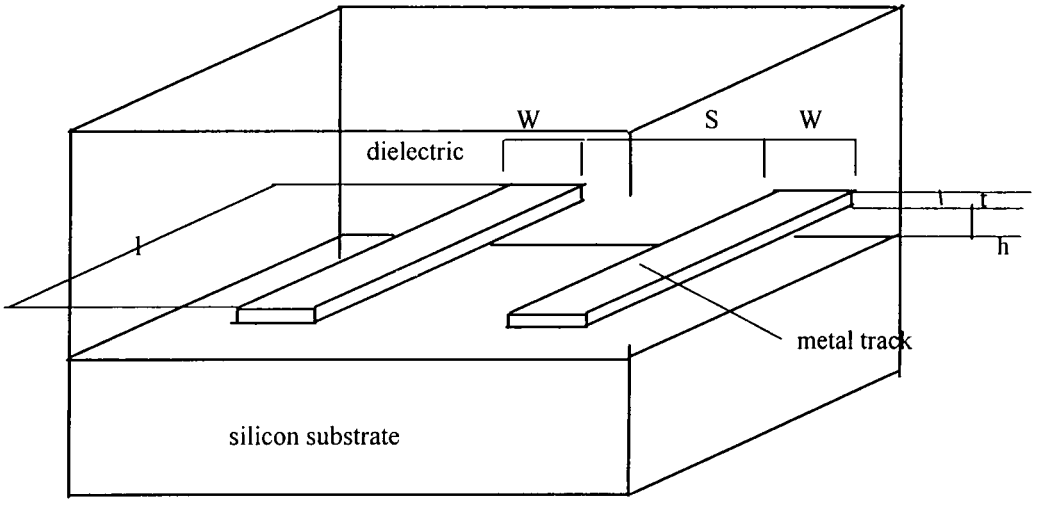
2.3 Modelling of VLSI interconnects

The second component which needs to be modelled correctly is the interconnection. By convention it is generally assumed that wires in an integrated circuit are lossless. A lossless line is interpreted as having no capacitance, resistance or inductance. Hence, the voltage at all points in the wire are identical. At first glance the obvious compromise noticed here is that in reality a wire must at least possess some resistance, no matter how small it is. The value may be small enough to be negligible in most cases but it may not be accurate enough when considering a sub-micron VLSI circuit. The argument also applies to the capacitance and inductance inherent in the line. Apart from the self capacitance, the capacitive coupling between signal lines which is the main reason behind the problem of crosstalk must also be modelled correctly if the simulation results are to be valid. The next sections will discuss how interconnect can be

modelled. Effectively this results in various RCL circuits which can be used to represent the interconnect with different accuracy and simplicity.

2.3.1 The Lumped Capacitor model

As mentioned earlier, the simplest way to model interconnect is as a lossless line, neglecting all the capacitive, resistive and inductive values. In actual VLSI circuits, however, track capacitance can have a significant effect on the performance of the circuit and its presence is unavoidable. To discuss the reason behind this, first a typical track structure in VLSI interconnect is shown in the following figure 3.



W = *track width* *h* = *track height*

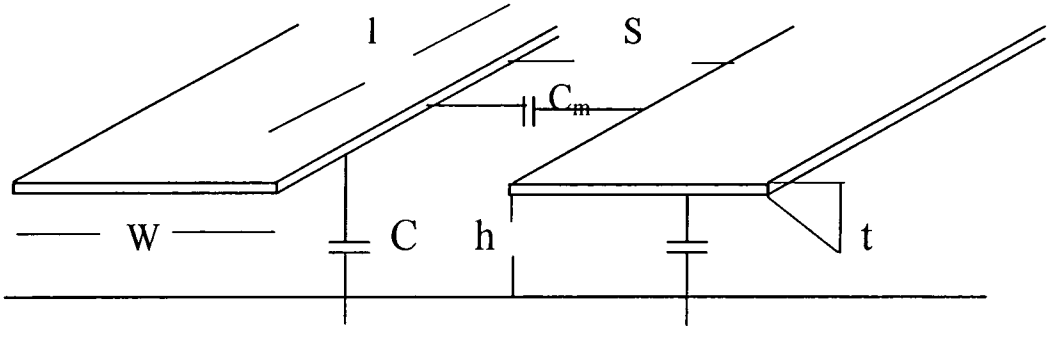
l = *track length* *S* = *track separation*

t = *track thickness*

Figure 3 Typical track structure

As can be seen from the figure, interconnections in VLSI basically consist of metal layers deposited over the substrate and surrounded by some dielectric medium. Typically the metal used is Aluminium while the dielectric would be SiO_2. According to the figure there are five physical parameters which can be used to represent the tracks; the width of the track(w), the track thickness(t), its height above the substrate(h), the length and the separation (s) between the tracks.

In its simplest form, with the width of the line being relatively large, the capacitive coupling between the lines can approximately be regarded as a result of the equivalent parallel plate capacitance of the cross section of the side of the lines plus some fringing capacitance. In this case the value can be relatively small and hence negligible. The resistance of the line will also be small as the cross-section is relatively large and the line's capacitance is dominated by the parallel plate capacitance between the line and substrate. The idea is summarised in figure 4.



where $C \approx \epsilon Wl/S$ large $R = \rho l/Wt$ small

$C_m \approx \epsilon tl/S$ small and negligible

Figure 4 Simplified case for larger tracks

This simplified view works well for larger technology. For the more modern chip however, this model can be insufficient. As the whole chip is being scaled to a smaller and smaller size, not only the transistors are scaled down but also their interconnects. The scaling of interconnect has actually been introduced in table 2 in the first chapter. The important point to note here is that while all of the horizontal parameters such as the width and separation are scaled properly, the thickness and the height which are vertical parameters are not. Due to difficulties in silicon processing it is common that vertically the chip is not scaled as aggressively as in the horizontal dimension. This results in the coupling capacitance having a relatively larger value when compared to the reduced track to substrate capacitance.

For these reasons, the simplest model which can be used to accurately represent small geometry interconnect must comprise the track capacitance and the coupling capacitance between the lines. The resistance of the track will increase as a result of the scaling. But if the source resistance is large enough the track's resistance may be omitted without any severe effect. The model which includes only capacitance of the tracks and the coupling capacitance is the lumped capacitor model. It is called lumped because, as the name suggests, the capacitors which represent the tracks and coupling capacitance are actually lumped together. Figure 5 shows how a 3-line system can be modelled. The ways by which the capacitive values and the resistance of the tracks, if necessary, are calculated can be quite complicated and will be treated separately in section 2.4 .

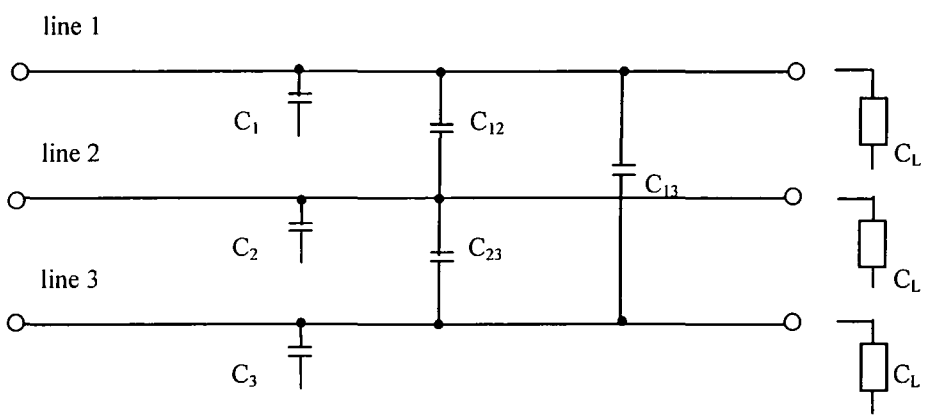


Figure 5 Lumped Capacitor model for 3 lines system

2.3.2 The Lumped Resistor-Capacitor Model (Lumped RC)

The lumped RC is almost similar to the lumped capacitor model. The only difference is that in this model the track resistance is also taken in to consideration. This is important, for example, if a long bus line is of interest, the longer the line the larger its resistance will be. Resistance per unit length also increases with scaling in more advanced technologies. This is because the size of the track is reduced its cross-sectional area is reduced and hence its resistance will actually increase. Sufficiently large resistance can introduce further problems such as the line delay and therefore its presence can not be neglected. Figure 6 shows an example of a lumped resistor-capacitor model of 3 bus lines.

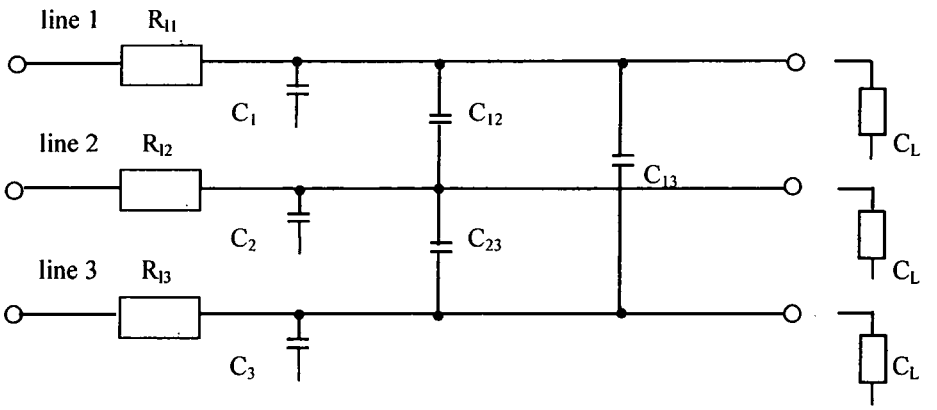
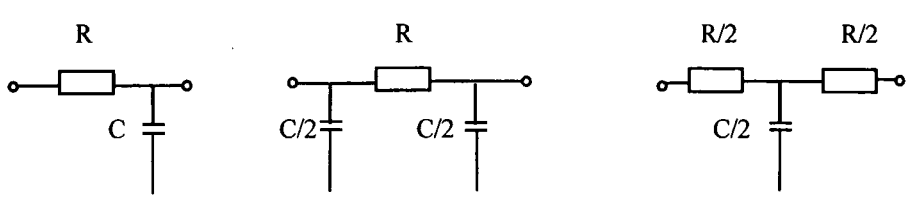


Figure 6 Lumped Resistor Capacitor model for 3-line system

2.3.3 The distributed RC models

In the previous two models, all the capacitors and resistors which represent the capacitances and resistances of the lines are lumped at one node for each line. In reality, however, the capacitance and resistance of the line are actually distributed along the line and should not be assumed to be lumped at any particular point. This idea has resulted in the introduction of various 'distributed RC models'. The three most popular models are the π, T and L models. Generally speaking, distributed RC modelling can be done by dividing the capacitances and resistances similar to that obtained under the lumped RC model into subsections. Each of the π, L and T models will have its own way of modelling the sub-section. Figure 7 shows sub-section modelling using L, π and T configuration.



(a) L model (b) π model (c) T model

Figure 7 L, π and T sub-section models

Between the three models it has actually been shown by Sakurai[14] that the L configuration can results in an error of as much as 30 per cent. The π and T models are consideably better and produce almost identical results. The T model, however, requires

2 nodes per section compared to only one node required by the π model, as seen above. These extra nodes imply more computational activities and introduce unnecessary complexity to the SPICE simulation. Thus, the π model is preferred. Figure 8 shows how a single line can be modelled using n-section π configuration.

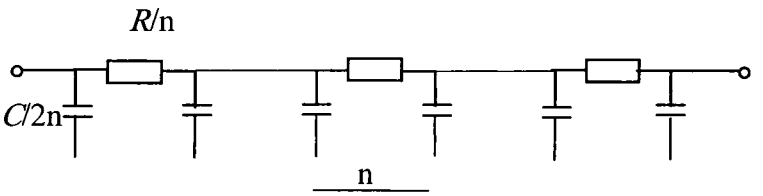


figure 8 n-section π model for a single track

According to figure 7, C and R are respectively the line capacitance and resistance used in the lumped model. The number n represent the number of sections the line is divided into. The larger the n the more accurate the model will be. It can actually be shown further that as the number of the subsection n approaches infinity, the line is governed by the equations:

$$\frac{dI}{dZ} = -C\frac{dV}{dt} \qquad \text{and} \qquad \frac{dV}{dZ} = -RI \tag{2-1}$$

Where V and I are voltage and current respectively and Z represent distance along the track. The two equations can actually be combined together to produce the diffusion equations describing voltage and current propagation along an RC line. The equations are:

$$\frac{d^2V}{dZ^2} = RC\frac{dV}{dt} \qquad \text{and} \qquad \frac{d^2I}{dZ^2} = RC\frac{dI}{dt} \tag{2-2}$$

These equations, even though they represent a more accurate way of modelling the tracks, are not realisable under the SPICE simulations. However it is possible to use large number of subsections so that the results achieved are comparable to that obtained directly from the equations. The problem with this is that it will make the circuit very

complex which may not be entirely desirable. Sakurai has shown that 3 state π model had an error of less than 3 per cent[14] compared to an analytical calculations.

When using the π model for crosstalk analysis, not only the lines are divided into subsections as shown earlier but also the coupling capacitance between them. The way in which the coupling or mutual capacitance can be modelled is exactly the same as the track or self capacitance shown previously. Figure 9 shows the example of a 3-section π modelling of 2-line bus. It can be imagined from the figure that the circuit can get very complex if a system involving multiple lines is of interest and as a result there must be some trade-off between accuracy and complexity. Further information about various distributed RC modelling can be found in [15]-[20]

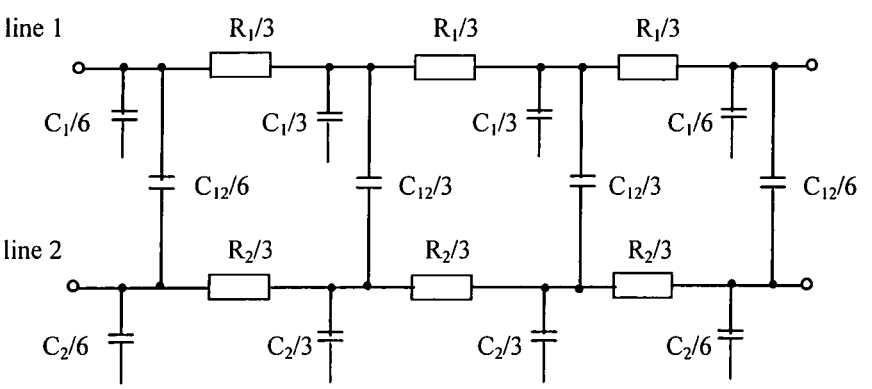


Figure 9 3-section π model of 2-line bus

2.3.4 Transmission line model

In previous sections, the interconnections were treated either as a lumped capacitive load for general cases or as a distributed RC lines in case of the lines having significant resistances due to the scaling effect. These models should prove to be sufficient for most cases. In an extreme case where the signal wavelength approaches the wire length, however, the transmission line properties of these on-chip interconnections must be observed. To have waveforms with sizes comparable to the lines requires that the lines are sufficiently long and that the circuit is operating at a very high speed. This is increasingly the case as the die size continues to increase and the

operating speed is being pushed higher and higher. Modern CMOS circuitry could require operation speed approaching or even exceeding giga hertz level. This can be very demanding of driving a large load.

The main difference between the models considered so far and the transmission line model is that it takes into the account the effect of inductance. The inductance becomes important as lines get longer and signal speed up causing an increase in *LdI/dt*. Because of the inductance, the current into the line can not be increased indefinitely by reducing the source resistance of the driver as inductors resist changes in the current by generating a reverse electromotive force. This limits the amount of current flowing into the line and introduces a fundamental limit to how fast a voltage/current waveform can travel down the line since a limited current can only charge up a certain length of a capacitive line at a given time period. As a result , the line is no longer equipotential but actually accommodates a travelling wave.

Generally, transmission line modelling is an established subject and has been carried out extensively for the analysis of other areas such as the microstrip in microwave circuits. The basic idea of transmission line calculation is given in appendix A. Here, the derivation of the attenuation along a resistive transmission line (lossy) is shown. Figure 10 illustrates the subsection of a lossy transmission line which has been modelled in a similar fashion to that given in appendix A.

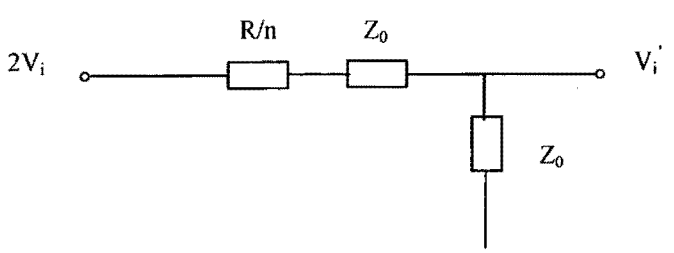


Figure 10 Subsection of a lossy transmission line

In figure 10, R is the total line resistance between the source (x =0) and the point of observation (x = 1), while n is the number of subsections. The voltage across a subsection can be expressed as:

$$V_i' = \left(\frac{2Z_0}{2Z_0 + R/n}\right) V_i \tag{2-3}$$

and the voltage at the point of observation is:

$$V(x = l) = \left(\frac{2Z_0}{2Z_0 + r/n}\right)^n V(x = 0) \tag{2-4}$$

Given that:

$$\lim_{n\to\infty}\left(1 + \frac{x}{n}\right)^n = e^x \tag{2-5}$$

The value of V (x =l) can then be calculated as n goes to infinity as:

$$\frac{V(x = l)}{V(x = 0)} = \lim_{n\to\infty}\left(\frac{2Z_0}{2Z_0 + r/n}\right)^n \tag{2-6}$$

$$= \lim_{n\to\infty} \frac{1}{\left(1 + \frac{R/2Z_0}{n}\right)^n}$$

$$= e^{-R/2Z_0} \tag{2-7}$$

Using a similar approach, a lossy transmission line can be modelled for the SPICE simulation as given in figure 11. Here z_0 is equal to $\sqrt{\frac{L}{C}}$

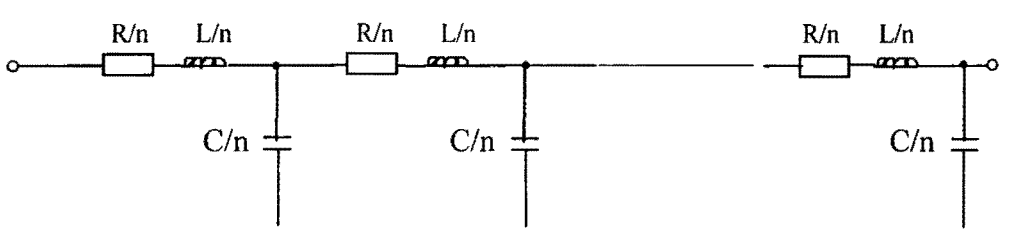


Figure 11 Approximate circuit for SPICE simulation of a lossy transmission line

It is a rule of thumb [39] that the transmission line phenomena become significant when

$$t_r < 2.5t_f \tag{2-8}$$

Where t_r is the rise time and

t_f is the time-of-flight delay and is defined as

$$t_f = \frac{l}{v} \tag{2-9}$$

Where l is the length of the line and

v is the propagation speed.

The line can act as a lumped capacitor when:

$$t_r > 5t_f \tag{2-10}$$

To summarise the effect of different modelling of the track on the waveform, figure 12 shows the output characteristics of tracks modelled using methods discussed previously. These are being driven by identical inverter buffers, with each of the inputs being switched from 0 to 1. The 0.7 micron CMOS transistors were used to realise the inverters while the track parameters were kept at 1 cm in length, 0.7um in thickness and height, and 1um in width.

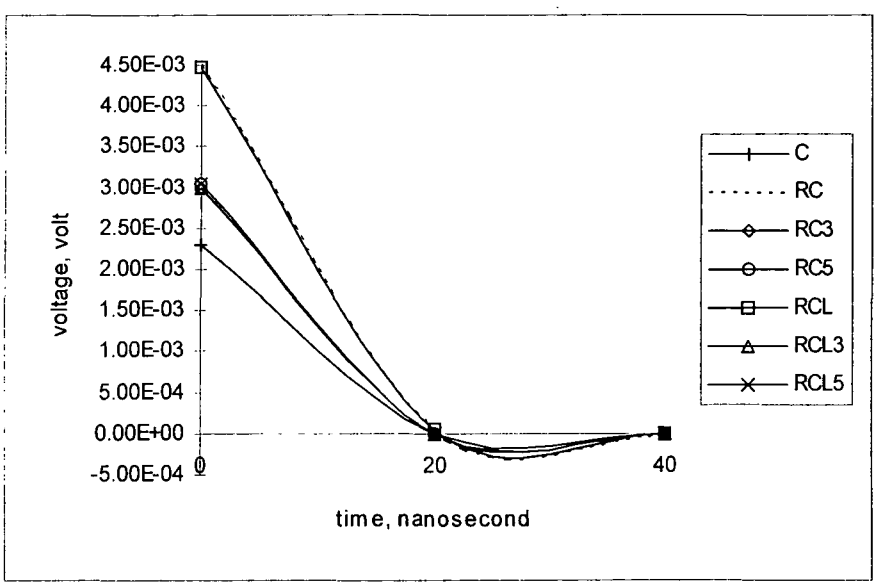


Figure 12 Switching characteristics of track differently modelled

From figure 12, it can be seen that the increase in the number of sub-sections in the distributed model at this level has little effect on the output waveform and may introduce unnecessary complexity to the simulation. Another interesting point is that the lumped capacitor model can have a significantly different result from the others if the line resistance is comparable to that of the source. The difference, however will start to get narrower as the source resistance increases and starts to dominate the whole circuit. The transmission line models, according to the figure, produce very similar results to the distributed RC models. This is to be expected as the circuit was operated at an appropriate speed for CMOS ICs which is too slow for the RCL model to start showing any significant effect on the output waveform.

2.4 Resistance, Capacitance and Inductance Calculations

Once it has been established which method of track modelling is to be used the next important procedure is to actually calculate the values of these total resistance, capacitance and inductance that the lines possess. These three quantities are dependent of the physical parameters of the tracks such as their thickness and can be difficult to find, especially in the capacitance and inductance cases where they can be influenced by the position and combination of the lines involved. Calculations of these values, especially the capacitance, have actually been the main research interest and several ways of achieving them have been proposed as a result. Generally, these methods can be characterised into two schools of thought. The first group tries to simplify the relationships between the physical parameters and the RCL values into simple equations by accepting to tolerate some error in the results. The other group, in contrast, aims to find the very accurate values of the resistance, capacitance and inductance. They achieve this by mean of numerical analysis which can be very complex. Hence there must be some trade-off when choosing any of these available methods. The next sections discuss ways in which these RCL values can be derived and the most suitable methods to be used in the project are proposed.

2.4.1 Calculation of the track resistance

The calculation of the resistance of the track is probably the most straight forward. It is well known that a resistance of any conductor is directly proportional to its length and is inversely proportional to its cross-sectional area. For VLSI interconnection, the resistance of a track is given by:

$$R = \rho \frac{l}{Wt} \qquad \text{Where} \quad \rho \text{ is the resistivity of conductor material} \qquad (2\text{-}11)$$

W= track width, t= track thickness, l=track length

See figure 2, page 1-4

It can be seen from the equation that the resistance of the line increases as the line gets longer. Furthermore, scaling of the track means that the width of the line(W) will also be reduced, resulting in further increasing of the track resistance. High resistance is not desirable as it will introduce further delay which can seriously affect the operating speed of the circuit.

The problem of having large resistance, according to the equation, can ideally be solved to by increasing the thickness of the track. In reality, however, a resistance can only be reduced to some certain point where further increase in the thickness would no longer have any effect. This is due to the skin effect which is inherent in any alternating current. The critical value where the thickness still has effect on resistance is called the skin depth and is given by the equation:

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}} \qquad (2\text{-}12)$$

Where δ is the skin depth, μ is the permeability, ρ and f are the conductivity of the material and the sine wave frequency respectively. It can be seen from the equation that as the frequency increases the skin depth or the critical depth will be reduced. It should be noted, however, that for frequency less than 10GHz the skin depth is greater than the actual thickness of the line[21][22]. Since a real signal has a spectrum of sine wave components which extends up to its bandwidth, this means that only the components of very high frequencies will be affected by the skin depth and that the final resistive

characteristics of the line should not be significantly affected. The skin depth effect is therefore not included in the calculation of track resistance.

2.4.2 Calculations of self and mutual capacitances within the tracks

Methods of calculating the values of the mutual and self capacitance of the interconnection are of great interest as these capacitances are the main factor which can determine the performance of the whole circuit. The following sections, starting from the very basic models, illustrate various methods by which capacitance of the lines can be extracted.

2.4.2.1 The parallel-plate capacitor model

The simplest way of describing the capacitance of the interconnect is to treat it as a parallel plate capacitor. In this case, a capacitor with finite capacitance is formed between the track and the substrate, as shown in figure 13. According to the model, a uniform electric field is formed only between the bottom of the tracks and the substrate. This model omits several facts and so in reality, in order to have this model valid the tracks must be extremely thin so that all the fringe capacitances can be neglected. The lines must also be much closer to the substrate than to each others so that the self capacitance dominates. Having thin lines with relatively large separations and no electric field between them also means that there is no coupling capacitance between any of the line. The model is therefore, rather unrealistic and not ideally suitable for this work.

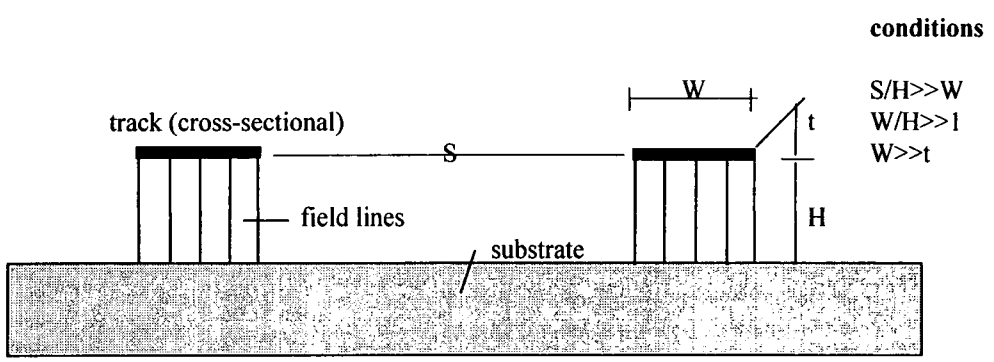


Figure 13 The parallel-plate model of track capacitance

2.4.2.2 The Schwartz-Christoffel model

The Schwartz-Christoffel model is the improved version of the parallel-plate model. The difference is that it has also taken into account the effects of having an electric field coming from the top of the conductors. This model, however, still fails to recognise the presence of the coupling capacitance between the conductors. The reason behind this is that again the thickness of the tracks is assumed to be negligible. This is due to the fact that originally the model was derived for microstrips used in microwave circuits and that microstrips themselves have much larger width compared to their thickness.

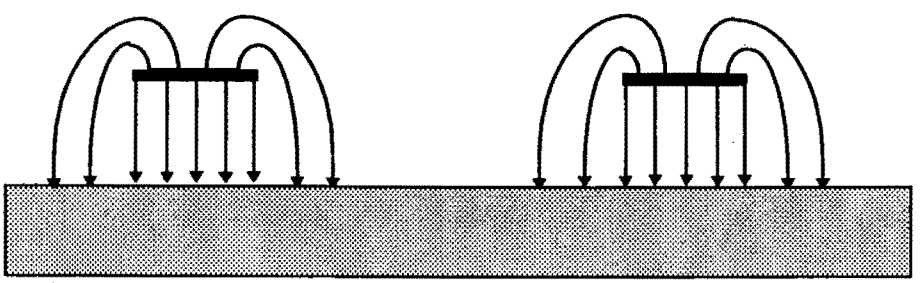


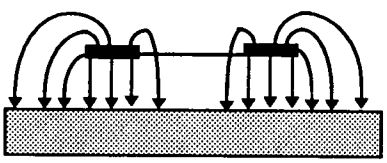
Figure 14 The Schwartz-Christoffel Transformation

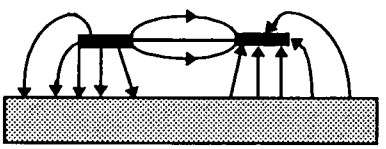
2.4.2.3 The Lewis model

In addition to the previous two models, a number of other analytical models have been proposed, some of which were particularly developed for microelectronic structure. These models, as well as being able to calculate the coupling capacitance between the conductors, do not have limitations on the thickness, separation or width of the tracks. The normal procedure with these models would be to consider first the simplest case of two symmetric conductors and then to apply the results to the more general cases. Among the models, the simplest and most convenient way is to describe the wave propagation of a signal along a coupled pair of symmetric lines as a sum of an even and odd mode of propagation. The Lewis method is actually one of the simplest methods which applies the idea and can be used to demonstrate this idea.

The method was first published in his paper[23]. It was built on the earlier work by K.C. Gupta[24]. Lewis showed that for two adjacent symmetrical conductor strips the propagation modes can be reduced to even and odd modes corresponding to an even and odd symmetry of the field lines. The idea is as shown in figures 15 and 16.

Even Mode **Odd Mode**



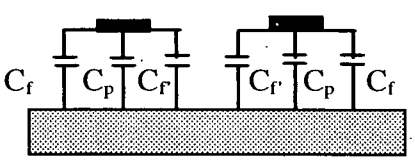


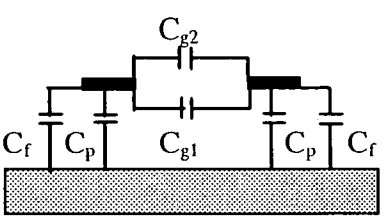
15 *16*

Figures 15-16 Field lines in even and odd modes coupled microstrips

As can be seen from the figure, the difference between the two modes is that in the even mode where the conductors have the same voltage, the electric field exists only between the conductors and the substrate. In the odd mode, by contrast, each of the conductors actually has different voltages so the field lines are split between the substrate and the other conductor. The equivalent capacitance models for these 2 modes can be derived as shown below in figures 17-18.

Even Mode **Odd Mode**





17 18

Figures 17-18 Even and odd mode capacitance models

In the even mode, C_p is equivalent to the parallel-plate capacitance seen previously. C_f is the outer fringe capacitance which can be found as a half of the difference between capacitance derived from the Scwartz-Christoffel and simple parallel-plate models. The inner fringe capacitance C_f will have the value equal to C_f

multiplied by the ratio of the height over the separation. The other two capacitors C_{g1} and C_{g2} which are required in the odd model can be extracted from two complex formulas given in the book by Gupta[24].

The Lewis model, even though having proved to be simple enough, has several limitations. One of the conditions is that all the conductors must be of the same size and have identical separations. This can be very impractical as it is more than likely that bus structure in integrated circuit would comprise several tracks of different sizes and separations. The others limitations, such as that it can only be applied to tracks on the same level or that the conductor width must be equal to or less than twice the height of the conductor for multi-conductors system, severely restrict the use of this model in modern conductor system. It is therefore necessary that a more accurate and flexible model should be founded.

2.4.2.4 The Numerical Methods for Capacitance Calculation

Numerical techniques can be used to model any arbitrary conductors with a high accuracy. As has been mentioned before, the trade-off would be that the model derived would be very complex and a powerful simulator is required. There are actually three principle numerical techniques which are used to calculate capacitances in arbitrary conductor system namely, the finite element method (FEM) [25][26], the boundary element method (BEM)[27][28] and the partial element equivalent circuit technique (PEEC) [29][30]

- The finite element method (FEM)

Capacitances can be found under the finite element method by way of partitioning the tracks into a mesh of elements to model the electric field and hence determine its potential distribution. By the application of the electric field on the conductors or the use of a potential energy technique the charge on each conductor can be found and together with the potential distribution the capacitances are derived. The technique can be applied to any non homogeneous conductors, even with a curved geometry.

- The boundary element method (BEM)

The boundary element method is the most commonly used technique for multiconductor system calculation of intensive capacitive and inductive matrices. This method is known as the Green's function. In many ways it is similar to the FEM. But instead of modelling the electric field as in the FEM case, it is the charges on the conductor that are preferred. The method works by actually replacing all conductor surfaces and dielectric interfaces with the charge distribution that exits in free space to create a potential distribution equivalent to the original system. The electric field of any given point is then calculated under the superposition principle as the cumulative effects of all the changes present in the system. A Green's function is then defined which gives the potential at any point based the distribution of the total charge in the system with the reference point normally being the infinite ground plane. Because only conductor surfaces are needed for the calculation the computational efficiency is dramatically improved.

- The partial element equivalent circuit technique (PEEC)

Under the third method, the PEEC, the conductors are broken into rectangular cells where equivalent capacitances and inductances are calculated for each cell. The cells are then combined together to form a three-dimensional mesh of capacitors and inductors. The method promises a more efficient way of calculating the conductors parameters as they already inherit the three dimensional structure in each cell. The approximation of each cell to be rectangular is justifed as the metal conductors in ICs are almost always of rectangular form.

All the three techniques described here provide very accurate ways of calculating capacitance of the conductors. They may differ slightly on ways of achieving the results and the limitations which are posed upon them but for VLSI interconnect the results are mostly comparable, as discussed in [9]. The common feature of these methods, however, is the requirement of a powerful simulator as they are all very computational intensive. A further constrain is also imposed by the fact that the methods generally

require the inversion of extremely large matrices, needing therefore large memory resources. Any alternative method which require less computing while retaining or providing a similar level of accuracy given by these numerical methods is very much desirable. Such a method can actually be realised using Matthaei's model.

2.4.2.5 Matthaei's Method for capacitance calculation

The Matthaei's method can be said to be a method which actually combines the ideas of even-odd mode analysis as in the Lewis's case with the boundary element method. It was reported for the first time by Matthaei in his paper in 1992[31]. The idea is mostly similar to BEM. But instead of determining the charge distribution through the solution of the Green's function, a very complex procedure, it further simplifies the model by allowing two charge basic functions as a mean of modelling each side of the conductor. For the whole circuit therefore, a square matrix of only eight times the total number of conductors is required, significantly reducing the computational requirements.

The two charge functions are almost similar to the even and odd mode functions used in Lewis's method. The only difference is that rather than describing the electric field or equivalent capacitance as in Lewis's method, they actually describe the charge distribution within the conductor. Figure 19a shows the cross-section of a conductor of width W in x-y plane. Its length is in the k plane with direction into and out off the paper. Figure 19b and c show the corresponding odd and even charge functions.

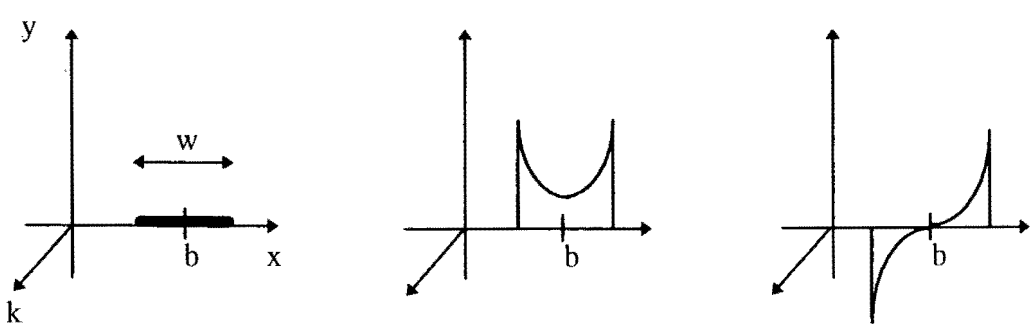


Figure 19 a) The cross-sectional trip b) Its even function c) Its odd function

According to the figure, it can be shown[40] that for the even-symmetric function the potential arising from the charge distribution at any point z in the complex plane is:

$$\phi_e(z,b,w) = q\left(\frac{1}{\varepsilon_0} H_e(z,b,w)\right) \tag{2-13}$$

where

$$H_e(z,b,w) = \left(-\frac{1}{2\pi}\right) \mathrm{Im}\left(\arcsin\frac{2(z-b)}{w}\right) \tag{2-14}$$

And for the corresponding odd function, a potential at any point Z is given by:

$$\phi_o(z,b,w) = g\left(\frac{1}{\varepsilon_0} H_o(z,b,w)\right) \tag{2-15}$$

where

$$H_o(z,b,w) = \mathrm{Re}\left((z-b) - sign(\mathrm{Re}(z-b))\sqrt{(z-b)^2 - \left(\frac{w}{2}\right)^2}\right) \tag{2-16}$$

In these equations, w is the width of the conductor, b is the position of the centre of the conductor and ε_0 is the dielectric constant. The constant g in equation (2-15) will be cancelled out in later equations since the odd-symmetric distribution has a net charge of zero.

Matthaei's method has actually been studied extensively by P. Mahoney at the University of Durham and a MSc thesis has been produced as a result[9]. Comparisons between this model and others have been extensively discussed and Matthaei's method showed to be the favourable method for VLSI interconnection modelling. The method has proved to have reasonably accurate results while requiring only minimal amount of computations. It can also be applied to any arbitrary system consisting of tracks of different sizes lying on different levels, making it very versatile. The work here will therefore continue to use the Matthaei's method as a mean of calculating the capacitance of the tracks. The following table shows an example of a capacitive matrix derived using Matthaei's method. The capacitance matrix shown is for a system of 8 conductors,

each with 1 μm width, 0.7 μm thickness, 0.7 μm height above the ground, 1 cm long and 1um of separation. The symmetry of the matrix can be seen where C_{ij} is equal to C_{ji}. This should come as no surprise as they actually represent the same value. It can also be seen that the coupling capacitance between adjacent lines is the most significant capacitance in the system. This again is as expected since the places of these capacitances are directly next to each other with only the dielectric medium between them. It is these values which should dominate the characteristics of the crosstalk.

j \ i	1	2	3	4	5	6	7	8
1	1690ff	407.95	35.45	15.34	9.73	5.71	4.12	3.9
2	407.95	1820	397.37	31.04	12.9	7.18	4.68	4.12
3	35.45	397.37	1820	396.94	30.81	12.78	7.18	5.71
4	15.34	31.04	396.94	1820	396.87	30.81	12.90	8.73
5	9.73	12.9	30.81	396.84	1820	396.94	31.04	15.34
6	5.71	7.18	12.78	30.81	396.94	1820	397.37	35.44
7	4.12	4.68	7.18	12.90	31.04	397.37	1820	407.94
8	3.9	4.12	5.71	8.73	15.34	35.44	407.94	1690

C_{ij} is a coupling capacitance between line i and j , in femto farad

Table 5 Example of capacitance matrix derived under Mathaei's method

2.4.3 Calculation of track inductance parameter

The final components of interest are the equivalent inductors, even if they are only required in the transmission model. There are several ways to calculate directly the inductance matrix for multiple line interconnection systems. Alternatively the inductance matrix can simply be derived from the capacitance matrix. This is a very interesting alternative since the capacitance matrix is readily available from Mathaei's method, a lot of time and efforts can be spared. The relationship can be found by first consider the transmission line equations describing the voltage and current propagation through the line:

$$-\frac{d}{dZ}[V] = j\omega[L][I] \qquad (2\text{-}17)$$

$$-\frac{d}{dZ}[I] = j\omega[C][V] \qquad (2\text{-}18)$$

where [L] and [C] are respectively the inductance and capacitance matrices. Voltages and currents in the lines are also represented in vector forms of [v] and [I] respectively. Combining the two equations together would give:

$$\frac{d^2}{dZ^2}[V] = -\omega^2[C][V][L] \tag{2-19}$$

If we further assume that neither [L] nor [C] are frequency dependent and that all nodes have the same propagation velocity υ then:

$$[L] = \frac{1}{\upsilon^2}[C]^{-1} \tag{2-20}$$

It is quite obvious from the equation 2-20 that ideally the inductance matrix can therefore be found as an inverse matrix of the capacitance matrix multiplied by some constant $1/\upsilon^2$. This is not quite yet true for silicon-based microelectronics systems since they actually possess different field distributions are complicated due to the fact that different dielectric constants are present for substrate and dielectric. The differences in field distributions will actually result in variations of propagation velocities. Adjustment can be made by introducing a new matrix $[C_0]$ which is a capacitance matrix derived by considering the system to be in free space with a relative dielectric constant of unity and propagation velocity of the speed of the light in free space *c*. Together with the fact that for a silicon-based circuits the dielectric materials can be ignored as there is a negligible difference in magnetic permeability between silicon and free space[32]. The inductance matrix is then given by:

$$[L] = \frac{1}{c^2}[C_0]^{-1} \tag{2-21}$$

The following table shows the resulting inductive matrix derived under these rules. The tracks physical parameters are similar to the ones used in the capacitive matrix example.

j \ i	1	2	3	4	5	6	7	8
1	2740	662.97	219.12	93.37	48.74	29.58	20.09	15.13
2	662.97	2670	644.08	212.01	90.00	46.94	28.67	20.08
3	219.12	644.08	2670	641.71	210.91	89.50	49.44	29.58
4	93.37	212.01	641..71	2670	641.34	210.94	90.00	48.73
5	48.74	90.00	210.91	641.34	2670	641.71	212.01	93.35
6	29.58	46.94	89.50	210.94	641.71	2670	644.08	219.21
7	20.09	28.67	49.44	90.0	212.01	644.08	2670	662.96
8	15.13	20.08	29.58	48.47	93.35	219.21	662.96	2740

Table 4 Example of inductance matrix , pH

2.5 Summary of the chapter

This chapter provides the theoretical analysis of the possible models for transistors and their interconnections. Accurate models are necessary for the circuit simulation to have its results valid. The scaling laws for MOS transistor can be used as guideline, but for a more accurate and reliable model, the transistor parameters must be extracted directly from real device. For the case of interconnections, modelling involves 2 steps. The first step is to decide how the tracks are best represented in term of RCL network. The results here actually suggest the 3-stage RC π model is the most suitable. Once the type of network is decided, the second step is to calculate the accurate values of these capacitances, inductances and resistances. Various techniques have been discussed with the Matthaie technique is chosen as the best compromise between the accuracy the numerical methods offer and the simplicity provided by several analytical techniques.

CHAPTER 3 *Characterisation of Crosstalk*

The previous chapter has seen the efforts of modelling the transistor and it interconnects resulting in several possible alternatives. Once suitable models have been identified the next step is to actually design sample circuits based on these models to study the resulted crosstalk through simulations. The ability to anticipate the characteristics of crosstalk that is likely to occur should prove to be a valuable asset when designing modern integrated circuits as any potential malfunctions caused by the crosstalk noise can be avoided. The behaviour of crosstalk depends on various factors. Circuit configurations and technology used can have enormous influence on the crosstalk generated. This chapter, by building up gradually from basic to more complex circuits, reveals relationships between circuits parameters and the associated crosstalk. Emphasis is given on both theoretical and practical points of view.

Crosstalk in Two Signal Lines

The crosstalk in two signal lines represents the simplest situation where such noise can occur. The relationships involved in a system of two lines are easier to analyse, both mathematically and in simulation, than those produced by complex configurations such as a multiple line system. For these reasons the model can be used to illustrate the basic ideas behind the occurrence of crosstalk, before moving on to the more advanced models. The circuit configuration of a two signal lines system itself can be of various forms. The next sections will therefore analyse these possible configurations, starting from the most basic set-ups. Understanding gained from analysing these models will then be used as a basis for the more advanced set-ups.

3.1 Crosstalk in a Simple Two Parallel Line System

In any circuit where two signal lines are laid parallel a coupling capacitance is formed between them. If the signal in one of the line is switching the coupling capacitance will force the signal in the other line to face a sudden change for a short period of time. The idea is illustrated in the figure below.

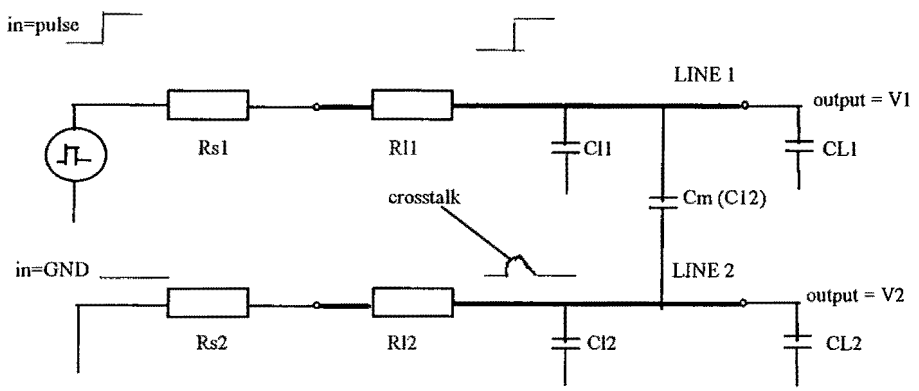


Figure 20 Crosstalk in 2-line system

According to the figure, R_{S1} and R_{S2} are the source resistances of line 1 and line 2 respectively. For simplicity both of the lines are shown here using a lumped RC model. Each of the lines has its own self (or line) capacitance C_l to the ground plane, and is driving a capacitive load C_L. The input of line 1 is connected to a pulse-signal source via R_{S1} while line 2 is grounded at its input. The presence of the mutual capacitance C_m (or C_{12}) between the lines results in spike-like signal induced in line 2. The model can be analysed mathematically with varying complexity, depending on the type of the set-up of the parameters chosen. This can generally be divided into four main situations; The first and simplest situation is when the two lines as well as the two sources are identical. The second and the third situations are when only either the source resistances or the lines are identical. For the remaining situation all the parameters can be arbitrary.

3.1.1 Crosstalk in Two Identical Lines With Identical Source Resistors

This case typifies the simplest situation where crosstalk can be analysed. The circuit is similar to that in figure 20, only now the lines and source resistances are required to be identical. Having identical lines implies that the impedances of the lines are equal, resulting in $R_{l1} = R_{l2}$ and $C_{l1} = C_{l2}$. For most of the circuits discussed here, the capacitive loads C_{L1} and C_{L2} are assumed to be equal. This is done for simplicity reason given the fact that it is very likely that for many cases these buses would be driving identical buffers. If these conditions are met, then it can be shown, as given in appendix B, that the output voltages V_1 and V_2 are:

$$V_1 = V_{DD} - \frac{V_{DD}}{2}\left[e^{\frac{-t}{RC}} + e^{\frac{-t}{R(C+2C_m)}} \right] \qquad (3\text{-}1)$$

$$V_2 = \frac{V_{DD}}{2}\left[e^{\frac{-t}{RC}} - e^{\frac{-t}{R(C+2C_m)}} \right] \qquad (3\text{-}2)$$

Where $R_{l1} = R_{l2} = R_l$, $R_{S1} = R_{S2} = R_S$ ——— $R = R_l + R_S$

$C_{l1} = C_{l2} = C_l$, $C_{L1} = C_{L2} = C_L$ ——— $C = C_l + C_L$

In these equations, V_1 is the response to the switching signal on line 1. It can be seen from the equation 3-1 that V_1 switches from zero to supply voltage V_{DD} with some delay introduced by two exponential functions. The case can be compared to the normal situation of a lossy line driving a capacitive load. In that case the rise time is controlled by a decaying exponential with time constant of RC, giving $V_1 = V_{DD}(1-e^{t/RC})$. In this situation, however, there exits two exponentially decay functions with different time constants RC and $R(C+2C_m)$ and it is the summation of these which controls the overall switching characteristics of V_1

Ideally, if there was no crosstalk line 2 would see no change in the voltage V_2 which would remain at ground. That is obviously not the case here according to equation 3-2. The voltage in line 2 is now actually proportional to the difference between the two exponential functions of equation 3.1. The size of crosstalk is also controlled by the amplitude of the supply voltage. Figure 21 shows the examples of V_1 and V_2 derived

from the equations. The signals are achieved by the use of the MATLAB which is an interactive, matrix-based programme for solving complex numerical problems. MATLAB software is a product of the Mathwork Co.

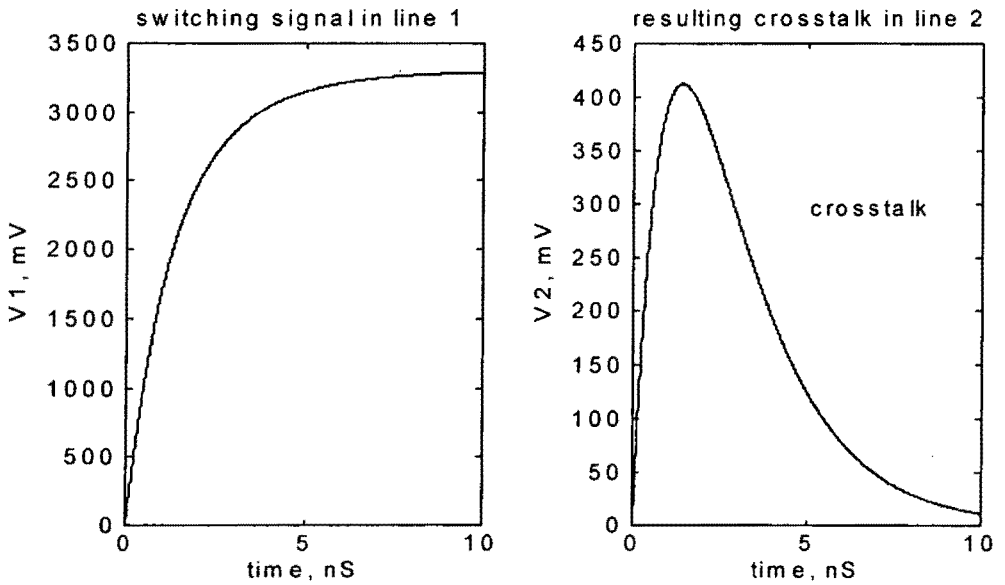


Figure 21 Switching characteristic of line 1 and its corresponding crosstalk in line 2

In this example the supply voltage is set at 3.3V. Each of the lines has the combined line and load capacitance of 1 pF, a reasonable value for a typical interconnect of around 1 cm long. The coupling capacitance C_m is set at 0.5 pF, slightly exaggerated for a better demonstration. The crosstalk generated here has a maximum amplitude of 412.5 mV with it pulse period of around 5 ns. These two parameters are indeed the two major factors which can determine the level of severity of the problem that the crosstalk can cause in the circuit. The higher the amplitude and the wider the width, the more likely that the crosstalk will have significant effects. Normally, the width of the crosstalk is described in term of t_{50} - a time taken between two points in the crosstalk where $V = V_{DD}/2$. It can be shown that by increasing the size of R, normally be mean of increasing the source resistance R_s, the width of the crosstalk pulse will be increased. The effect is demonstrated in figure 22. It is understandable that such an effect arises since increasing R_S means that the current through the capacitors is reduced - hence slowing down the charging and discharging activities. Alternatively it can also be interpreted that by increasing the R, the time constants RC and R(C+2Cm) are increased - resulting in two slower exponential functions.

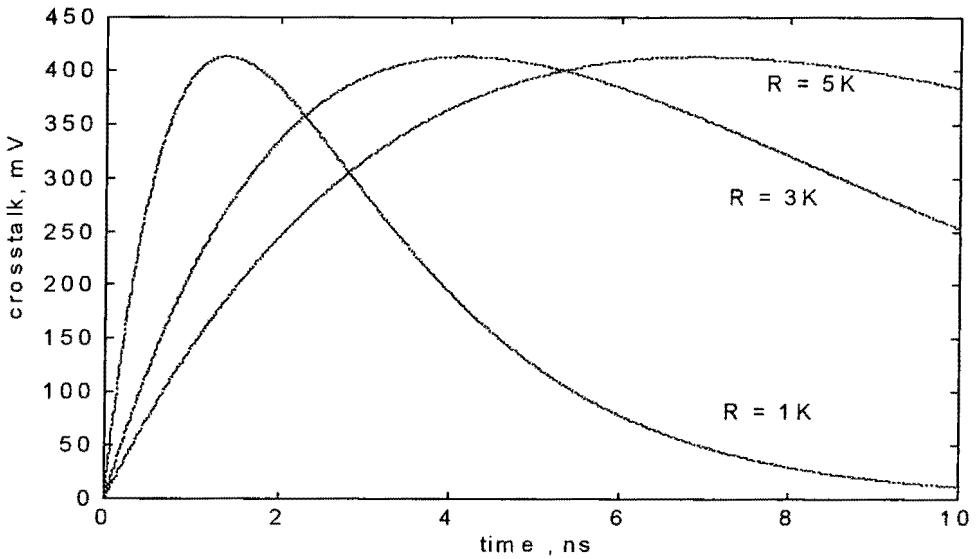


Figure 22 Crosstalk under different R

It can be argued from the equation that it is not only an increase in R which can increase the width of the crosstalk pulse. Increasing C, the summation of line and load capacitance, will also result in larger time constants and hence the same effect would be expected. The difference, however, will be that by increasing C not only will the width be increased but significantly the amplitude will be reduced. It can be shown that the maximum crosstalk in this case (identical lines & sources) is independent of R, as indicated in figure 22. The derivation of maximum crosstalk amplitude together with its MATLAB functions are given in appendices B and C. Shown here is the final equation:

$$V_{2,\max} = \frac{V_{DD}}{2}\left[e^{\frac{-(C)}{2C_m}\ln\left[\frac{C+2C_m}{C}\right]} - e^{\frac{-[C+2C_m]}{2C_m}\ln\left[\frac{C+2C_m}{C}\right]} \right] \qquad (3\text{-}3)$$

As can be seen from the equation, the only parameters which determine the maximum crosstalk are C, C_m and V_{DD}. The maximum crosstalk is clearly directly proportional to the supply voltage V_{DD}. The relationship between the maximum crosstalk and the two capacitance values C and C_m, however, can be harder to verify. Figure 23 shows how the maximum crosstalk varies with the coupling capacitance, given different line capacitance (for load capacitance C_L << line capacitance C_l, then $C \approx C_l$). In each of

the figure 23 a), b), c) and d) the MATLAB result is plotted against the SPICE simulation results where the lines are modelled in the Lumped C, lumped RC and 3-stage π configurations. Here the source resistances are set at 1 kΩ and the resistance of the lines are 400 Ω.

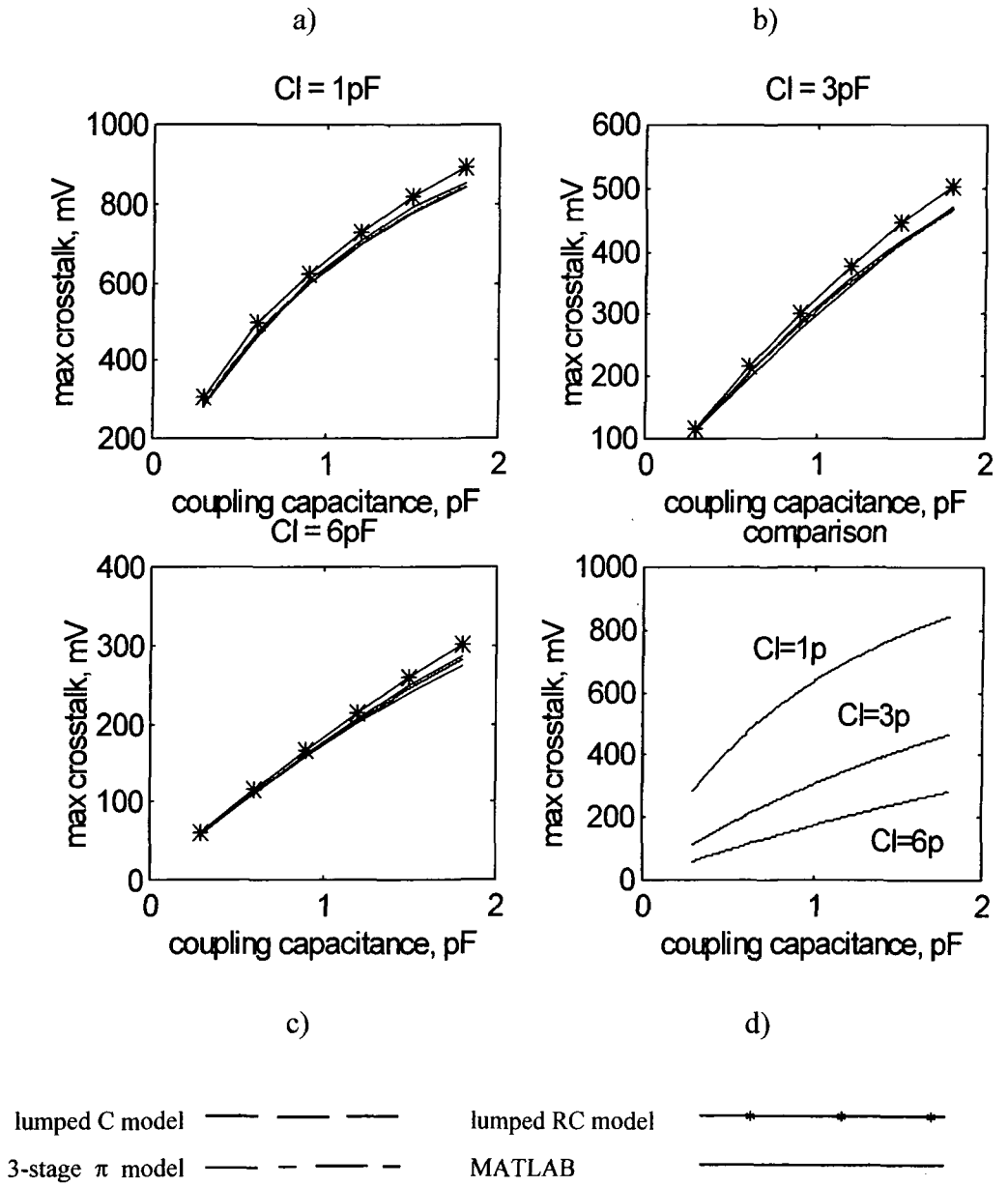


Figure 23 The maximum crosstalk under different C and C_m

It can be seen from the figures that the mathematical equation provides fairly accurate results compared to the simulations. The 3-stage π model tends to produce a slightly higher value of crosstalk. That is understandable since the mathematical model was derived under the assumption that the lines were modelled using the lumped

configuration. The difference, however, is only minimal and the mathematical model can still be a useful way of obtaining an initial prediction of maximum crosstalk.

Another interesting point to be noted is that even though in theory the maximum crosstalk is not affected by the sizes of the source resistance as long as they are equal, the simulation shows some contradicting results. Figure 24 illustrates the effect of changing the source resistance on the maximum crosstalk. Using the lumped models the maximum crosstalk seem to be fluctuating while under the π model the value can be significantly higher, especially if the source resistances are small. One reason for this effect can be that when deriving the equations, the switching time of the signal in line 1 was assumed to be ideal, i.e. time taken for the signal to switch from 0 to V_{DD} , and vice versa, is zero. This can not be achieved in the SPICE simulation where the rise and fall times must be properly defined to have some values which are not zero. Given this, therefore, for comparison the values should be kept as close to zero as possible when programming the SPICE. However, having too fast a rise/fall time can result in the simulation being unable to converge and is unrealistic. For these reasons the rise and fall time used are kept in the range of 1-100 ps, depending on the type of circuits. The difference between these values and that assumed in the derivation ensure that for a considerable period of time the behaviour of the circuit is not properly defined by the equations, hence changing the predicted crosstalk.

It should also be stated that the differences introduced by the lumped models are very small and hence can be neglected. For the 3-stage π model case, the effect of changing resistance can be severe if the source resistances are artificially small. But as they increase to more practical values, the different is significantly reduced and the resulting crosstalk is comparable to the rest. This is due to the fact that when the source resistances are large enough they start to dominate the whole circuit and the π model will eventually behave like the lumped counterparts. The increase in maximum crosstalk introduced by the π model can also be significantly reduced if lines with larger capacitance are used.

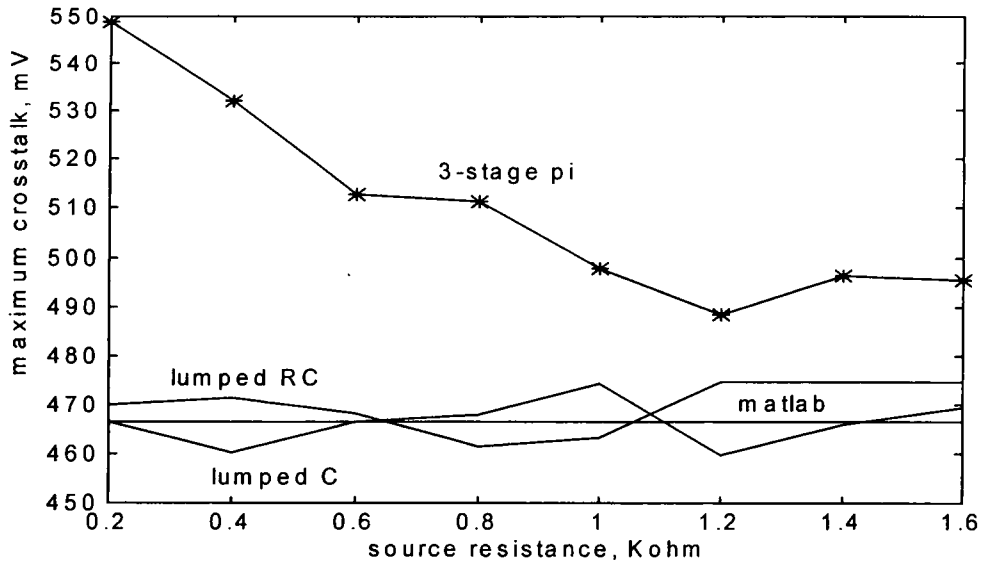


Figure 24 Maximum crosstalk as source resistances increase

To summarise the effects, it can be said that for a system of two identical lines/sources, increasing the source resistances will result in the crosstalk of greater width. On top of that, the signal in line 1 would have to operate in a slower speed because of the further delay introduced. This is illustrated in figure 25. Increasing the capacitance of the lines will also result in an increase of crosstalk width. But unlike the situation when increasing R would not affect the maximum crosstalk amolitude, in this case the maximum crosstalk would actually be reduced. Reduction of crosstalk is desirable, but by equally increasing capacitance in both lines, the undesirable effect of extra delay is also introduced.

The amount of the crosstalk, on the other hand, is apparently controlled by the value of the coupling capacitance. The larger the coupling capacitance C_m, the bigger the crosstalk. This, however, also depends largely on the size of line capacitance, as can be seen from figure 23 d). The same value of C_m would result in a larger crosstalk if the lines capacitance is smaller. The effect is demonstrated in figure 26. In both figure 25 and 26, the supply voltages are set at 3.3 volts.

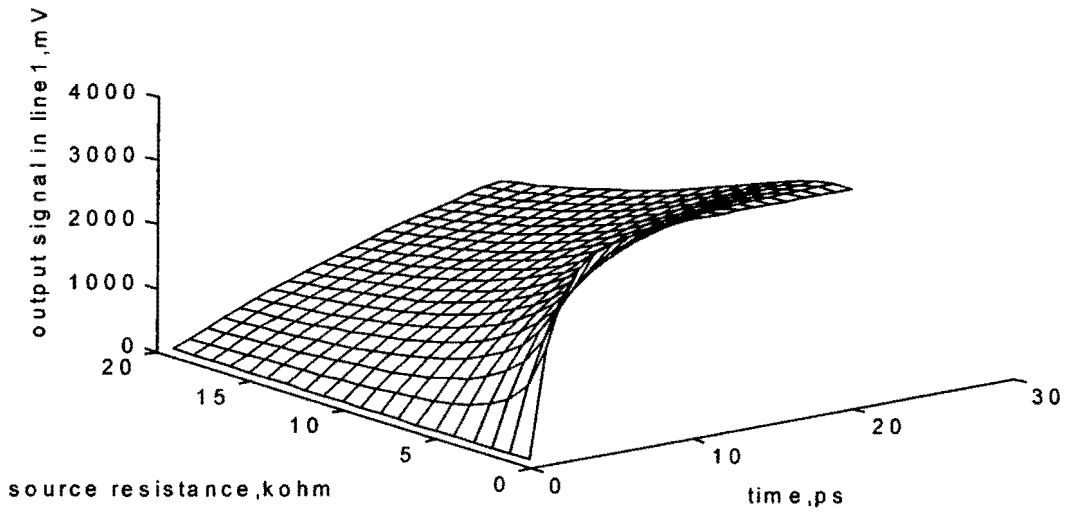


Figure 25 Switching signal (output) in line one, as source resistance increases

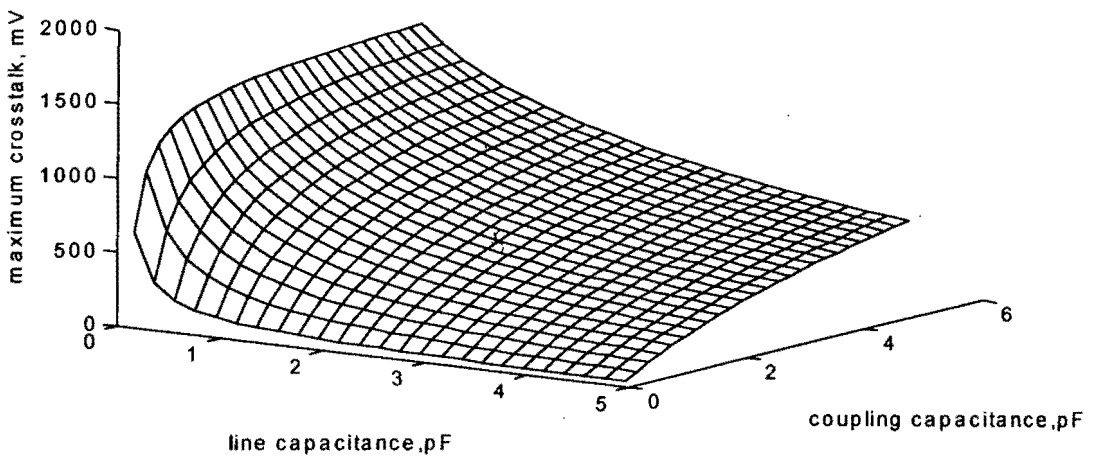


Figure 26 Variation of maximum crosstalk under different C and C_m

3.1.2 Crosstalk in Two Identical Lines with Different Source Resistance

One condition which was assumed throughout the previous section was that for both of the sources, their resistances must be equal. This is one constraint which may not necessarily be true for all cases. To demonstrate the effect of having different resistances for the sources, figure 27 shows the variation of maximum crosstalk caused by the use of different values of the source resistance. In the figure the lines are set to be

0.4 μm wide, 0.4 μm thick, 0.4 μm above the substrate, and 5 cm long. The supply voltage is 3.3. volts.

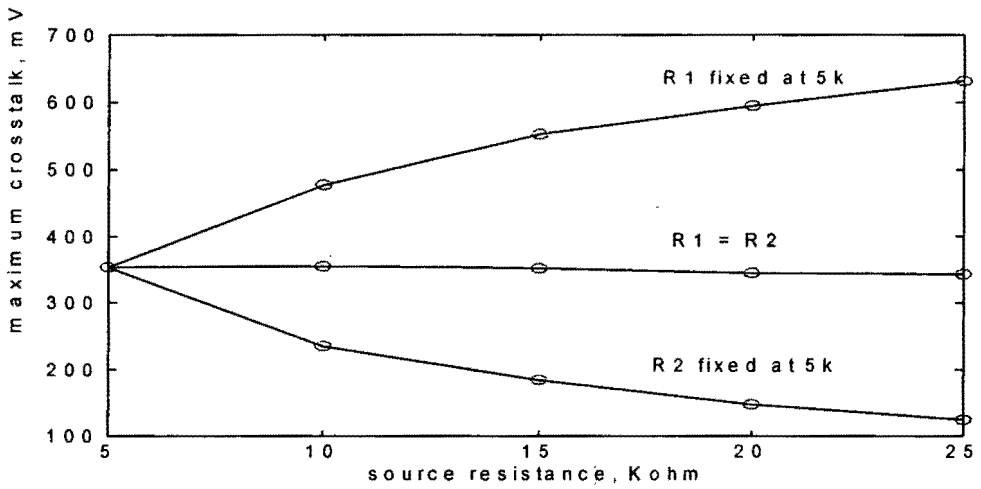


Figure 27 Effect of having different sources on the maximum crosstalk

The simulation result in the figure 27 shows some interesting facts. First of all, if both of the sources are kept equal the crosstalk maximum remains roughly the same as R_s increases. That is exactly how it should behave according to the analysis of the previous section. However, it is also apparent from the figure that, once the source resistance in the line 1 is increased, given that the source in line 2 remains the same, the amplitude of the crosstalk starts to fall. The effect is reversed if it is the source R_{S2} which increases.

This effect can be explained by considering that approximately the crosstalk is controlled by two RC constants which are determined by R_{S1} and R_{S2}. A small source resistance in line 2 (R_{S2}) will allow any crosstalk occurring in line 2 to discharge back more rapidly since the time constant $R_{S2}C$ is smaller. Hence, the maximum crosstalk is less. The effect is opposite if R_{S1} is less than R_{S2}. To be more precise, the analysis presented in Appendix B shows that the crosstalk generated (V_2) and its output counter part in line 1 V_1 are governed by the equations:

$$V_1 = \left[\frac{-V_{DD}}{\left(\frac{1}{F_2} - \frac{1}{F_1}\right)}\right]\left[-\frac{1}{F_1}e^{S_1 t} + \frac{1}{F_2}e^{S_2 t}\right] + V_{DD} \tag{3-4}$$

$$V_2 = \left[\frac{-V_{DD}}{\left(\frac{1}{F_2} - \frac{1}{F_1}\right)}\right]\left[-e^{S_1 t} + e^{S_2 t}\right] \tag{3-5}$$

where $$S_1 = \frac{(C+C_m)(R_1+R_2) + \sqrt{(C+C_m)^2(R_2-R_1)^2 - 4R_1R_2C_m^2}}{-2R_1R_2\left(C_m^2 + (C+C_m)^2\right)} \tag{3-6}$$

$$S_2 = \frac{(C+C_m)(R_1+R_2) - \sqrt{(C+C_m)^2(R_2-R_1)^2 - 4R_1R_2C_m^2}}{-2R_1R_2\left(C_m^2 + (C+C_m)^2\right)} \tag{3-7}$$

$$F_1 = -\frac{1}{C_m}\left[\frac{1}{R_1S_1} + (C+C_m)\right] \tag{3-8}$$

$$F_2 = -\frac{1}{C_m}\left[\frac{1}{R_1S_2} + (C+C_m)\right] \tag{3-9}$$

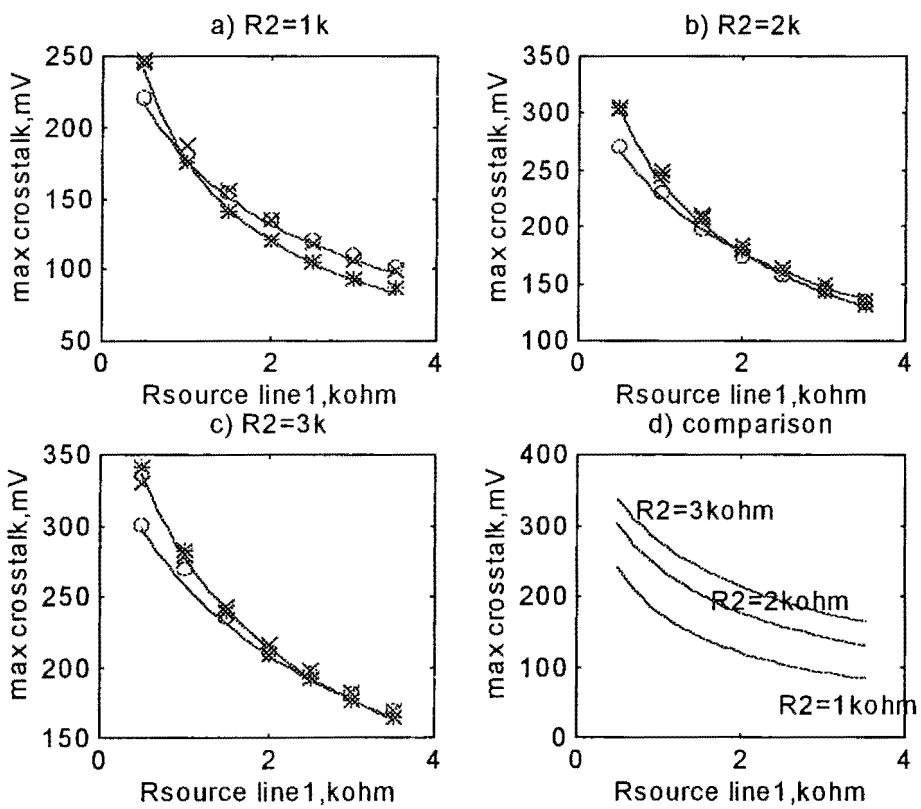
and the maximum occurs when:

$$t = \frac{1}{(S_2 - S_1)}\ln\left(\frac{S_1}{S_2}\right) \tag{3-10}$$

The equations are quite complicated and can not be manually analysed. So, as in the previous section, the equations have been programmed as 2 MATLAB functions, here are the *'gcrt'* and *'gcrm'*. The *'gcrt'* function (general-case crosstalk under different resistance, in time domain) takes any arbitrary values of the supply voltage (V), R_1(kΩ), R_2(kΩ), C(pF), C_m(pF) and t(ns) respectively and produces the corresponding value of V_2 in mV. For example typing v = gcrt(3.3,1,2,0.7,0.2,2) would calculate V_2 with V_{DD}= 3.3V, R_1=1K, R_2=2K, C=0.7pF, C_m=0.2pF and at t =2ps. For this example the answer would be v = 326 mV. Any parameter used can also be programmed as a range of arbitrary values so the programme is very flexible and can be used to produce any 2-D or 3-D graphs, as seen earlier. The other function, the *'gcrm'* is the 'general-case crosstalk

under different resistance, maximum' function. As the name suggests it is used to find maximum crosstalk and is of the form gcrt (V_{DD},R_1,R_2,C,C_m). The units are the same as those in *'gcrt'*.

To compare the mathematically derived crosstalk with the equivalent simulation results, the graphs of figure 28 show the plots of maximum crosstalk derived under MATLAB against the results from SPICE simulations. Three models, the lumped C, lumped RC and π are used to model the lines. For this example the line capacitance is set at 1.61pF, the coupling capacitance is at 275.95 fF and resistance of each line is 400 ohms. These parameters actually correspond to the lines of 1 μm width, 0.7μm thick, 0.7 μm height , 1 μm separation and 1 cm long.

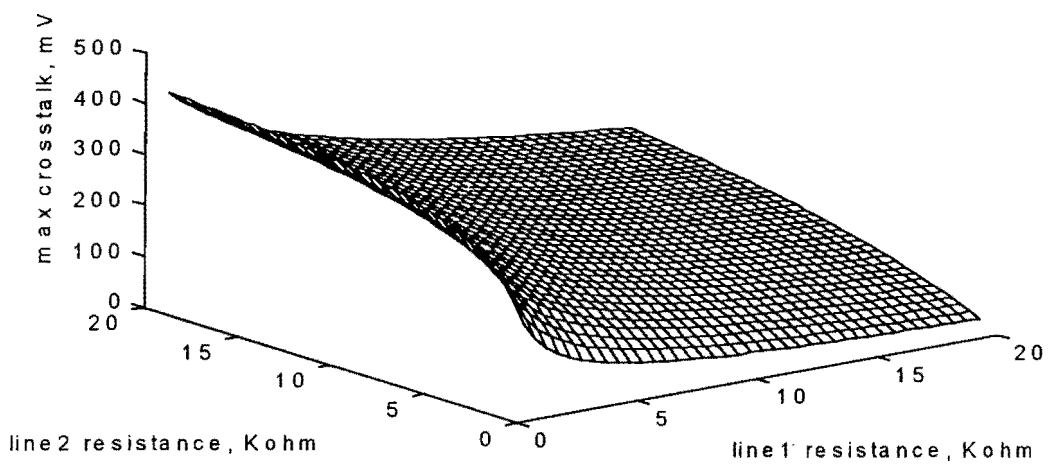


* lumped C model x 3-stage π model

o lumped RC model —— MATLAB model

Figure 28 Maximum crosstalk under different sources, simulations and MATLABs

In these figures, direct comparisons between simulation and MATLAB results are given in figures a)-c). In each of the figures there are two mathematically derived lines corresponding the two situations depending on whether the resistance of the lines are included (similar to the lumped RC model) or not (as the lumped C). The results show that these models provide very similar results. Hence it is fair to say that the mathematically generated models can be used to describe the behaviour at the circuit. Figure 28 d) also confirms the simulation results in Figure 27 that by increasing R_{s1} the maximum crosstalk will be reduced while increasing R_{S2} would have the opposite effect. The relationship can be illustrated more clearly in the three-dimensional graph shown in Figure 29. It can be seen from this figure that the effect can be more dramatic (i.e. significantly increase or decrease) if smaller values of R_1 or R_2 are employed.



given line 1 resistance = $R_{S1}+R_{l1}$

line 2 resistance = $R_{S2}+R_{l2}$

Figure 29 Maximum crosstalk under different resistance of the lines&sources

So far only the relationships between the source resistances and the maximum crosstalk have been discussed. There is actually another concern which should also be addressed: how does the combination of the source resistances effect the crosstalk in the time domain. To investigate this effect, the Figures 30a and 30b show the crosstalk in the time domain for different sources. In figures 30 a), c) and e) R_1 is varied from 1 to 20 kΩ while R_2 is kept at 5, 10 and 15 kΩ respectively. From the figures it can be seen that not only the maximum crosstalk amplitude is expectedly decreased as R_1 increases, but the

time taken to reach the maximum also increases as R_2 increases. In contrast, for figures 30 b), d) and f) where R_2 is varied and R_1 is fixed at 5,10,15 kΩ, the crosstalk increases as R_2 gets higher but it still takes longer time to reach maximum as R_1 increases.

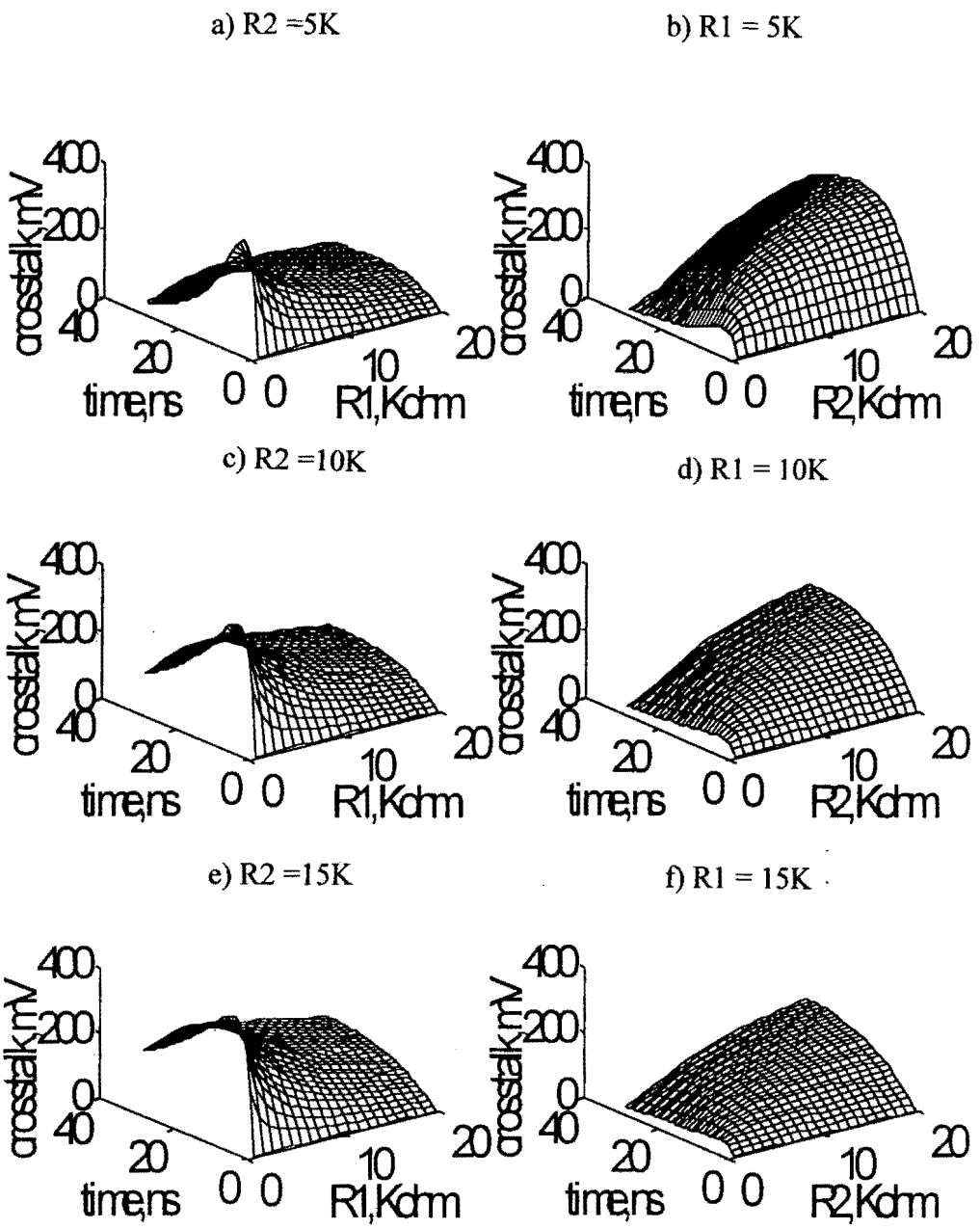


Figure 30 Crosstalk in time domain as sources change.

The effect of having different sources on the time taken to reach the maximum crosstalk t_{ct} can actually be demonstrated as shown in the figure below. The Figure is derived from equations 3-6,7,10. It reveals that increasing either R_1 or R_2 would results in faster t_{ct}. The time, however, will reach its maximum when $R_1 = R_2$. Any further increasing of the source R1 would actually result in faster t_{ct}. Equally increase in both of the sources would always result in slower t_{ct}

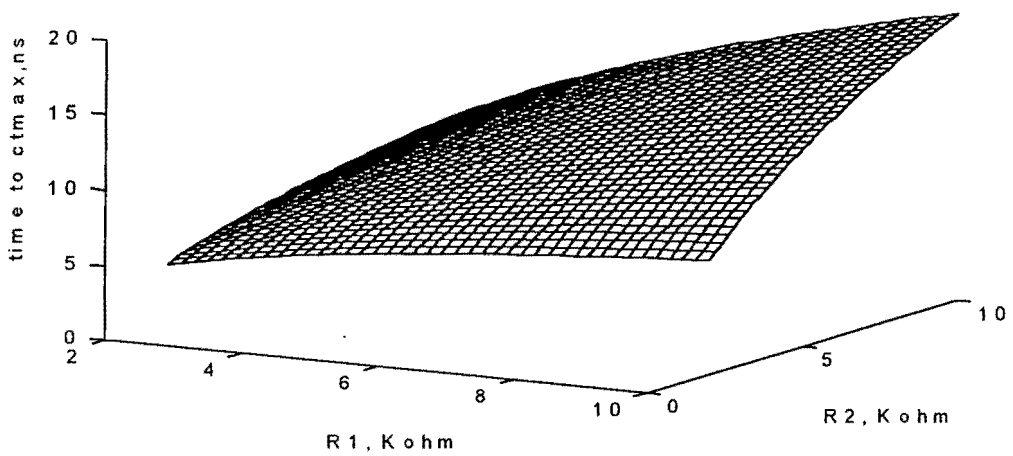


Figure 31 Variation of time taken to reach maximum crosstalk t_{ct} against R_1&R_2

3.1.3 Crosstalk in Two Parallel-Line System with Different Line Capacitance

For the previous 2 sections the derivations were under the assumption that the lines must be identical. In real situations, however, it can be quite common to have buses formed by different sizes of parallel lines. Having signal lines of different sizes normally implies that they are of different width, since this is the only physical parameter of the track which can be adjusted by the designer; the rest are process controlled. The track with larger width obviously would have a larger track capacitance and a smaller resistance. However, if the values of the source resistances are equal and are larger than that of the lines then it can be assumed that $R_1=R_2 \approx R_S$ and hence the equation governing V_1 and V_2 can be expressed as:

$$V_1 = \left[\frac{-V_{DD}}{\left(\frac{1}{F_2} - \frac{1}{F_1}\right)}\right]\left[-\frac{1}{F_1}e^{S_1 t} + \frac{1}{F_2}e^{S_2 t}\right] + V_{DD} \tag{3-11}$$

$$V_2 = \left[\frac{-V_{DD}}{\left(\frac{1}{F_2} - \frac{1}{F_1}\right)}\right]\left[-e^{S_1 t} + e^{S_2 t}\right] \tag{3-12}$$

where $$S_1 = \frac{(C_1 + C_2 + 2C_m)R + \sqrt{(C + C_2 + 2C_m)^2 R^2 - 4R^2(C_1C_2 + C_1C_m + C_2C_m + 2C_m^2)}}{-2R^2(C_1C_2 + C_1C_m + C_2C_m + 2C_m^2)} \tag{3-13}$$

$$S_2 = \frac{(C_1 + C_2 + 2C_m)R - \sqrt{(C + C_2 + 2C_m)^2 R^2 - 4R^2(C_1C_2 + C_1C_m + C_2C_m + 2C_m^2)}}{-2R^2(C_1C_2 + C_1C_m + C_2C_m + 2C_m^2)} \tag{3-14}$$

$$F_1 = -\frac{1}{C_m}\left[\frac{1}{R\,S_1} + (C_1 + C_m)\right] \tag{3-15}$$

$$F_2 = -\frac{1}{C_m}\left[\frac{1}{R\,S_2} + (C_1 + C_m)\right] \tag{3-16}$$

and the maximum occurs at V_2 when:

$$t = \frac{1}{(S_2 - S_1)}\ln\left(\frac{S_1}{S_2}\right) \tag{3-17}$$

For further investigation, these equations are used to provide the MATLAB functions, *'gcct(V_{DD},R,C_1,C_2,C_m,t)'* and the *'gcct(V_{DD},C_1,C_2,C_m)'*. In the *gccm* (general-case crosstalk with different line capacitance, maximum) function, *R* is not required because as equations 3.12-17 are combined together all the *Rs* are actually cancelled out. This means that the maximum crosstalk does not depend on resistance value as long as the resistance is the same for both lines. Figure 32 shows how the maximum crosstalk changes under different values of the line capacitance. Here for simplicity the coupling capacitance is fixed at 0.2pF. In reality, however, by increasing the width of one of the lines, the coupling capacitance will also be slightly increased from

the value obtained under identical lines configurations. The effect will be discussed more in the later chapters.

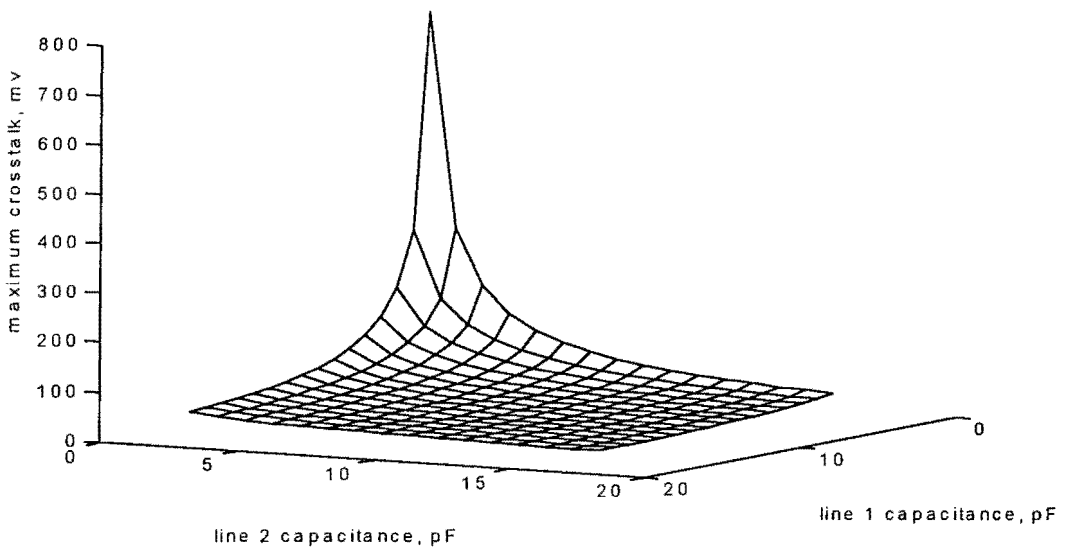


Figure 32 Maximum crosstalk under different line capacitance

It can be seen from the figure that the crosstalk will be significantly larger if the capacitances of the lines are small. This results from the fact that in this case the coupling capacitance would have a relatively large value and hence more effect. The Figure also shows that the crosstalk will reach its maximum when C_1 is equal to C_2. Increasing either of the values would reduce the maximum crosstalk. Hence there must be some trade-off between the speed of the circuit and its reliability, where a minimum of crosstalk is desired. This is an interesting conclusion which confirm a general design principle: faster circuits will be less reliable.

3.1.4 Crosstalk in An Arbitrary Two Parallel-Line System

This case represents the last and most general case under which the crosstalk between 2 parallel lines can be analysed. Here any of the important parameters, R_1, R_2, C_1, C_2, C_m, t and V_{DD} can be of any values. Relationships, however, can be more difficult to specify. Effectively, the behaviour of the crosstalk is influenced by the combined effects seen in the previous 2 sections. Shown here are the mathematical equations which represent the relationships between the crosstalk and the circuit parameters.

Corresponding MATLAB functions *gcrct($V_{DD}, R_1, R_2, C_1, C_2, C_m, t$)* and *gcrcm($V_{DD}, R_1, R_2, C_1, C_2, C_m$)* are given in Appendix C.

$$V_1 = \left[\frac{-V_{DD}}{\left(\frac{1}{F_2} - \frac{1}{F_1}\right)}\right]\left[-\frac{1}{F_1}e^{S_1 t} + \frac{1}{F_2}e^{S_2 t}\right] + V_{DD} \tag{3-18}$$

$$V_2 = \left[\frac{-V_{DD}}{\left(\frac{1}{F_2} - \frac{1}{F_1}\right)}\right]\left[-e^{S_1 t} + e^{S_2 t}\right] \tag{3-19}$$

$$S_1 = \frac{R_1C_1 + R_2C_2 + C_m(R_1 + R_2) + \sqrt{\left[R_1C_1 + R_2C_2 + C_m(R_1 + R_2)\right]^2 - 4\left[R_1R_2C_m^2 + R_1R_2(C_1 + C_m)(C_2 + C_m)\right]}}{-2R_1R_2C_m^2 - 2R_1R_2(C_1 + C_m)(C_2 + C_m)} \tag{3-21}$$

$$S_2 = \frac{R_1C_1 + R_2C_2 + C_m(R_1 + R_2) - \sqrt{\left[R_1C_1 + R_2C_2 + C_m(R_1 + R_2)\right]^2 - 4\left[R_1R_2C_m^2 + R_1R_2(C_1 + C_m)(C_2 + C_m)\right]}}{-2R_1R_2C_m^2 - 2R_1R_2(C_1 + C_m)(C_2 + C_m)} \tag{3-21}$$

$$F_1 = -\frac{1}{C_m}\left[\frac{1}{R_1 S_1} + (C_1 + C_m)\right] \tag{3-22}$$

$$F_2 = -\frac{1}{C_m}\left[\frac{1}{R_1 S_2} + (C_1 + C_m)\right] \tag{3-23}$$

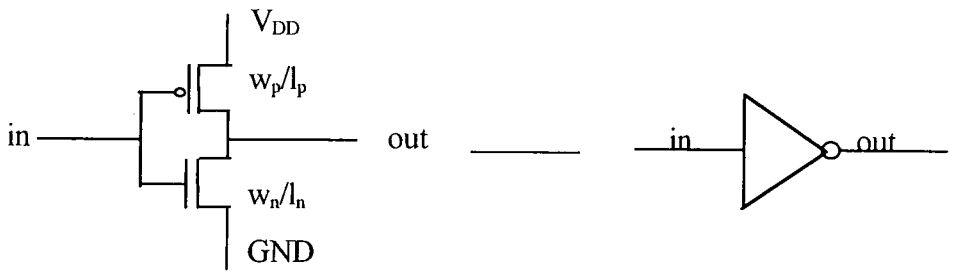
and the maximum in V_2 occurs when :

$$t = \frac{1}{(S_2 - S_1)}\ln\left(\frac{S_1}{S_2}\right) \tag{3-24}$$

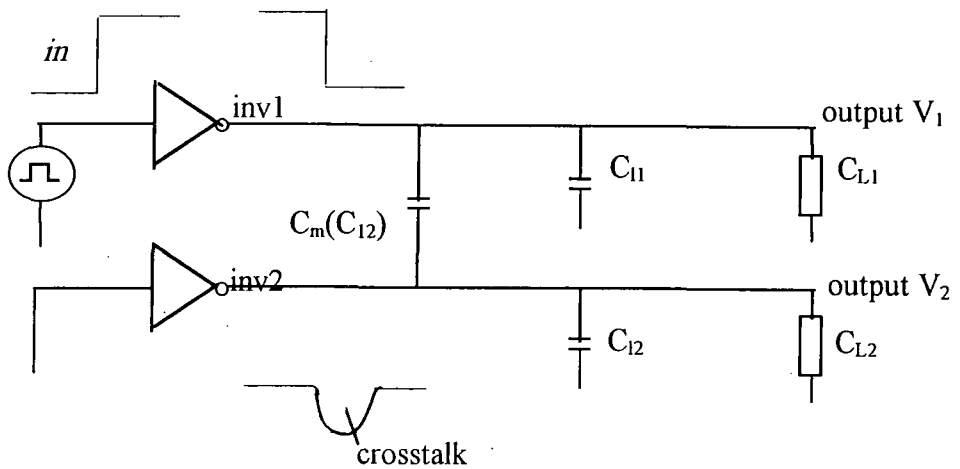
3.2 Crosstalk in Buffered Line Systems

In the previous sections, mathematical equations have been derived for crosstalk in term of various circuit parameters. In all of the cases, the sources were assumed to be simple resistors. Although the assumption was reasonable for mathematical analysis purposes, in reality this is not the case. For a system comprising long bus lines, the configuration in which the crosstalk most likely to occur, the tracks are in most cases

driven by some buffers. The most commonly used buffer is the simple CMOS inverting buffer. Figure 33 shows the typical arrangement of the circuit.



a) CMOS inverter and its symbol



b) A typical circuit configuration of two signal lines with buffers

Note: all transistor substrate connections are assumed to be connected to appropriate supply circuits

Figure 33 Crosstalk in buffered lines

The analysis of the circuit is more complicated than that done previously. This is due to the fact that the inverter buffer is not as simple as the resistive source which is a passive component. The inverter is an active device and, even though it is often treated as a 'digital' component, it is the analogue characteristics such as its switching behaviour which determine the crosstalk noise. The only adjustable parameter which controls the characteristics of the inverter and hence the resulting crosstalk is the width of each transistor, as the rest are fixed by the technology used (the minimum transistor length is normally used for obvious reason). The following figure shows how

crosstalk can vary with varying transistor width. Here W_1 and W_2 denote the width of the transistor in line 1 and 2 respectively. For all the inverters the width of the PMOS and NMOS are kept at 3.3 ratio for equal rise and fall time. The Figure shown uses 0.7 μm technology with line capacitance of 1.61pF and the coupling capacitance of 275.97 fF, the same specification as those in figure 28.

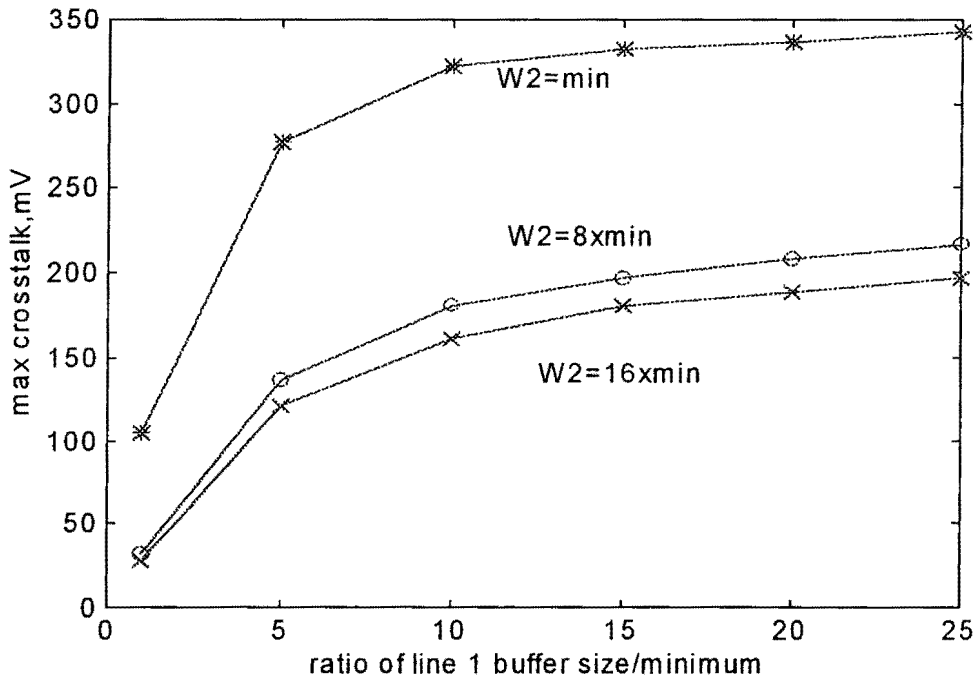


Figure 34 Crosstalk with different transistor width

It can be seen that increasing the widths of the transistors forming the buffer in line 1 would result in greater crosstalk. On the other hand, by increasing the widths of transistors in line 2 the crosstalk is actually reduced. This effect is in line with the analysis of crosstalk variation with some resistance presented earlier in section 3.1.1.

The analysis, however, is not as simple as it may appear. Unlike the ideal resistive source where its value is always constant. The equivalent resistance of the buffer is changing all the time due to the fact that during switching the inverter is going through a number of states and hence can not be governed by one equation. Its effect therefore is more difficult to analyse. To confirm this the Figure 35 shows how the maximum crosstalk is changing with the strength of the buffers (i.e. their widths) equally

increasing. This ideally would result in an unchanged crosstalk as both of the buffers, and hence their equivalent resistances, always stay equal. The figure shows the crosstalk for various length of line.

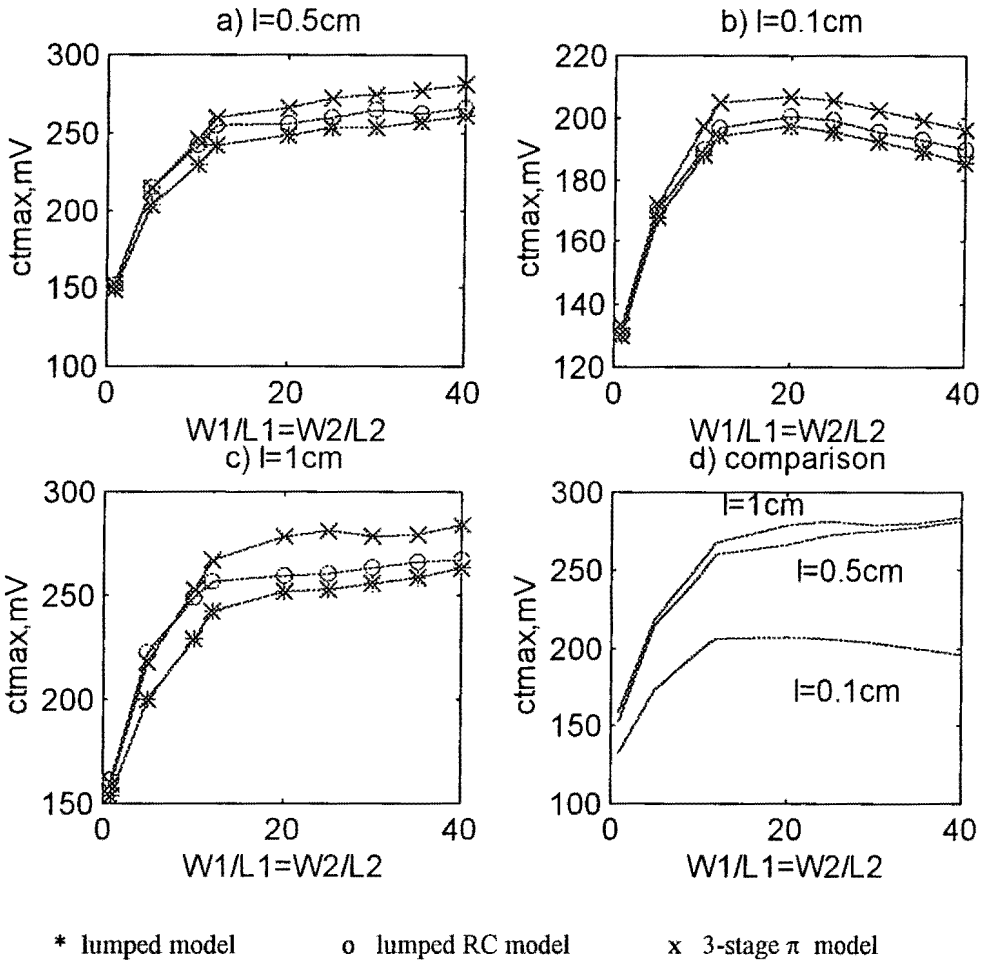


Figure 35 Maximum crosstalk against buffers with equally increased sizes(0.7 μm tech)

It can been seen from Figure 35 that instead of staying at the same value the maximum crosstalk changes rapidly from a very low value when the buffers are at their minimum sizes to reach its peak at some value before starting to fall again. The shorter the line (the lower the capacitance value), the smaller the buffers' size required to reach the peak point. In the case of tracks in integrated circuits, the bus length is likely to be 1-2 cm at most so according to the graph the peak for this technology can be stated to be at around $W_1/W_2 = 20$. Precise prediction is difficult because so many factors are involved. For this analysis the input to the buffer in line 2 is connected to the ground

signal. This means that the transistor in the buffer can be approximately be treated as a fixed resistance. It must be the switching buffer in line 1, therefore which possesses the changing characteristics of equivalent resistance resulting in the crosstalk shown. Due to this complexity it is wise to use simulation as the best way to investigate relationships between the crosstalk and various parameters rather than the numerical analysis used in previous sections.

When combining the effects seen in Figures 34 and 35, it is reasonable to assume that the crosstalk will be maximum when W_2 is 20-time its minimum width and W_1 be any value higher than $20xW_{min}$. As W_1 continues to increase, the crosstalk will also increase. The actual results are demonstrated Figure 36.

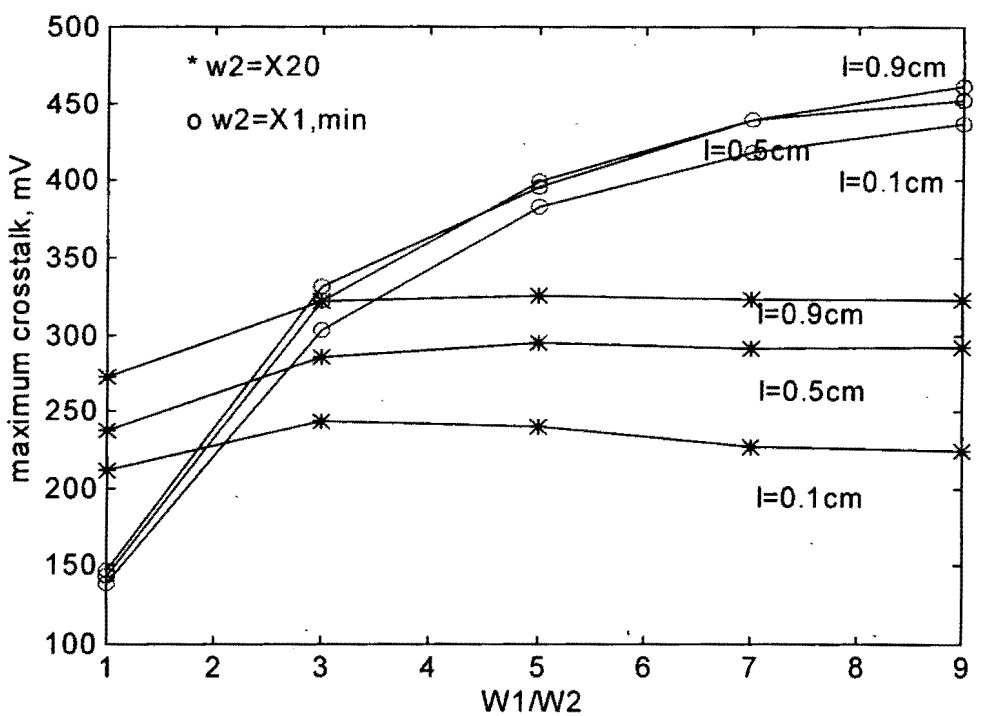


Figure 36 Maximum crosstalk vs the ratio of W_1/W_2, with different W_2 and l

As can be seen from the figure, the crosstalk on line 2 is greater at high ratios of W_1/W_2 when W_2 is minimum width. The ratio of W_1/W_2 does not however have significant effect for large values of W_2. This reveals an important point for the design of buses: that the crosstalk will be more severe on a line if the drive strength of the buffer driving the line is kept at its minimum or very small value while the buffer of the

line which is induction the noise is relatively larger. This knowledge will be very useful when considering the worst-case analysis in the next sections.

Figure 36 reveals not only the effect of using different buffers on the crosstalk. It can also be seen from the figure that by increasing the length of the tracks the crosstalk is increased. The change is more obvious when W_2 is large while the increase is almost negligible if W_2 is small. Furthermore, it is not only the length of the lines which can also influence the resulting crosstalk, there are other physical parameters which can also have an influence and the next section discusses their effects in details.

3.3 Influence of Different Tracks on The Crosstalk

In sections 3.1.1.1-.4, the characteristics of the crosstalk have been expressed in terms of certain parameters such as the line and coupling capacitance, or the resistance of the source or the line itself. These values, even though they can be used as an effective mean of expressing the behaviour of the crosstalk, are not the actual parameters which are directly of concern by the designer. In the last section the source resistance was replaced by the buffer transistors where a controllable parameter such as the transistor width can be adjusted to give different crosstalk. In similar ways, the behaviour of the crosstalk can be expressed in terms of the physical parameters of the track such as it length or width.

There are actually five parameters of the tracks, as seen in figure 3, which have an effect on the resistance, and the self and mutual capacitances of the lines - the three parameters which determine the resulting crosstalk. The parameters are namely the width, height, length, thickness and the separation between the tracks. The following figures show how the resistance and capacitance of the lines can be influenced by these physical parameters. In each of the figure, except in the varying length case, only one of the parameter is changing according to the value given in x axis, the length is fixed at 5cm and the rest of the parameters are kept at 0.4 um. For varying length case, the others are kept at 0.4 um.

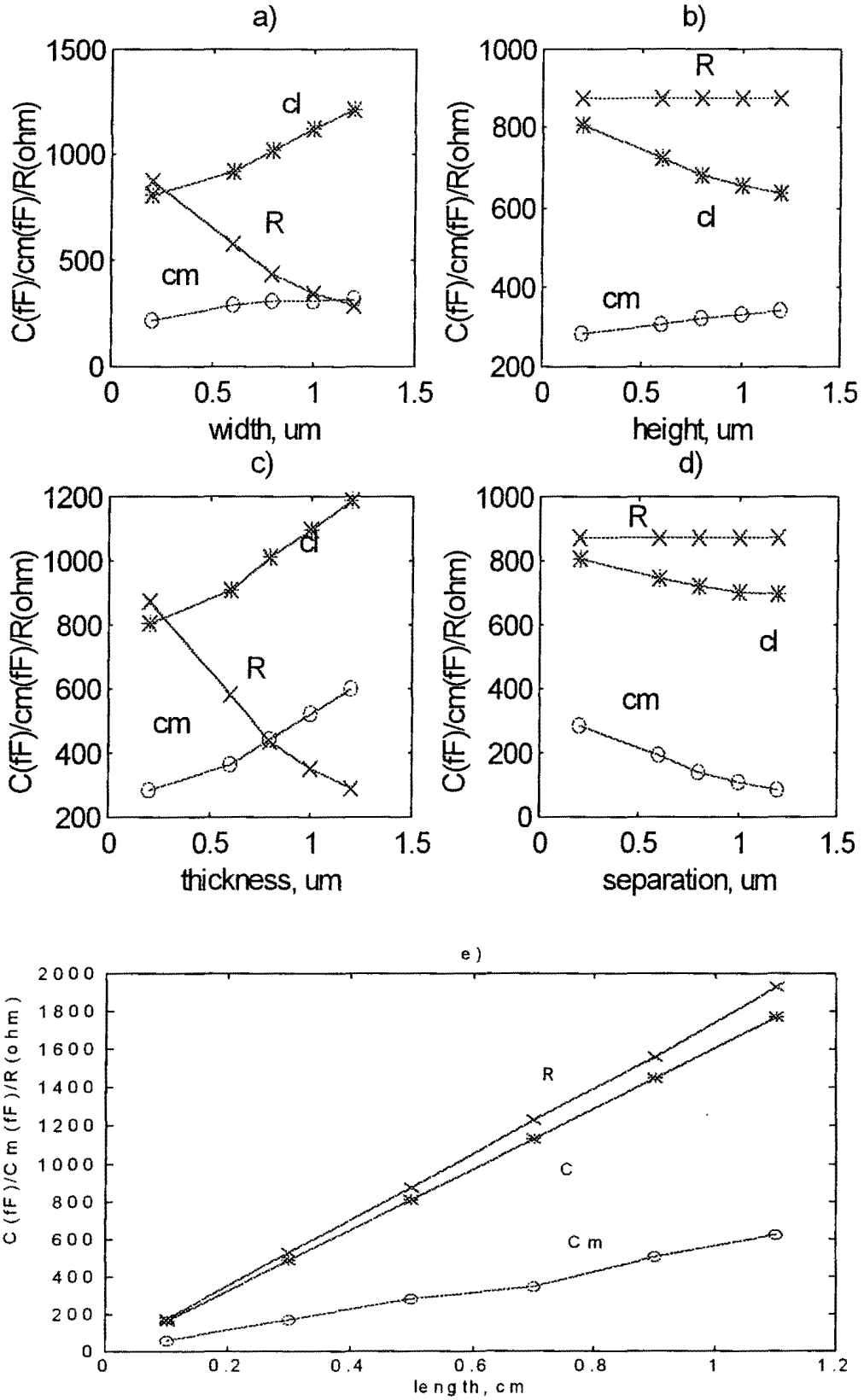
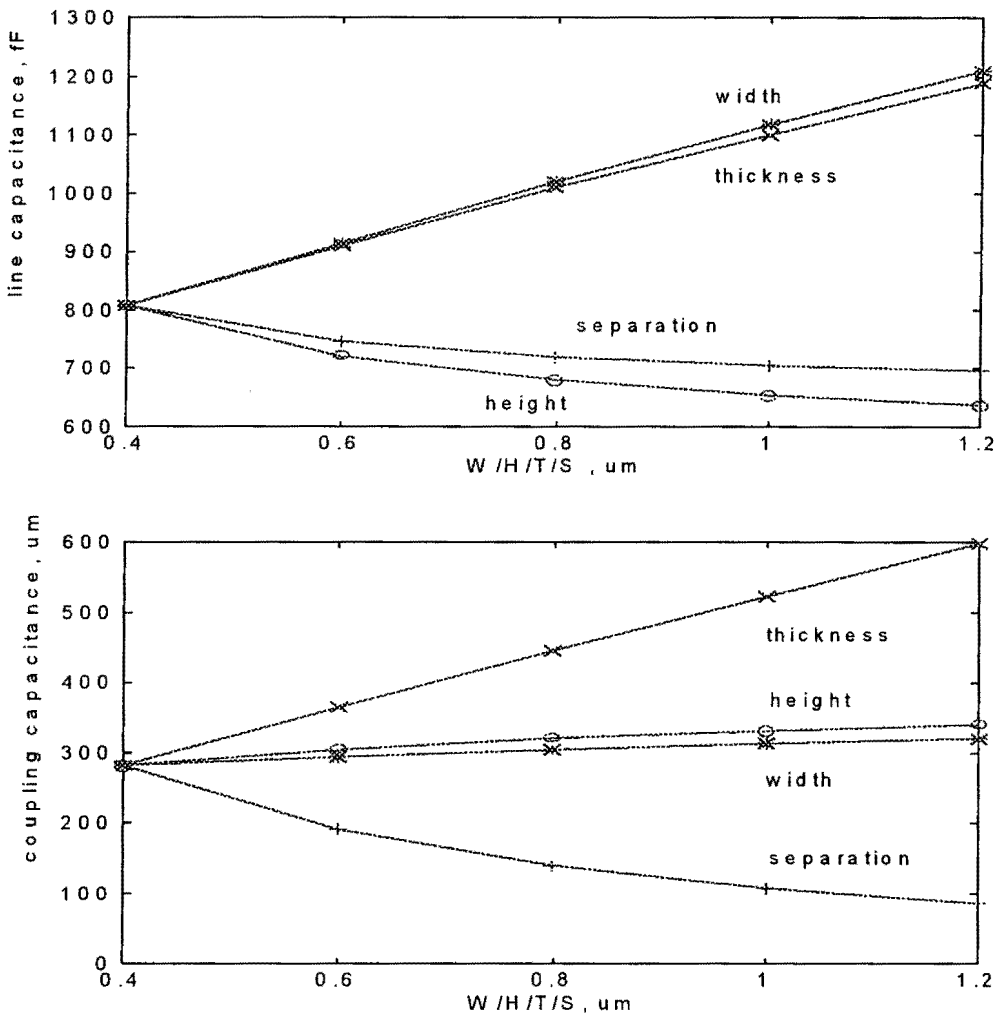


Figure 37 Changing of resistance, line and mutual capacitance against track's parameters

As discussed previously, the worst crosstalk will occur when the coupling capacitance is high and the self capacitance is low. It can be seen from Figure 37 that the coupling capacitance can be increased by increasing any of the five parameters, except the seperation. Increasing the width and length, however, would also introduce an increase in line capacitance and as a result there is no guarantee that the resulting crosstalk will also be higher. Thus the crosstalk seems to be affected most by the increase in track height above the ground plane. The following figure compares the effect of each parameters on the line and coupled capacitance.



W=width H=height T=thickness S=seperation

Figure 38 Self (line) and coupling capacitances against physical parameters of the track

The top figure shows the effect on the line capacitance. It can be seen that by increasing the width or thickness the capacitance is increased. Increasing the height and

separation, on the other hand, would result in a smaller line capacitance, although the effect of the separation is less. The coupling capacitance, according to the bottom figure, is maximised by increasing the thickness of the track. Increasing the width and height would also result in a larger coupling capacitance, but by smaller amount.

These figures, even though they illustrate how self and mutual capacitance can be influenced by the physical parameters of the tracks, do not give the clear picture of how the crosstalk will be affected. Simulations have been carried to investigate such an effect and the Figures 39 and 40 shown the resulting crosstalk against various parameters. As previously done, the lumped C, lumped RC and 3-stage π models are used.

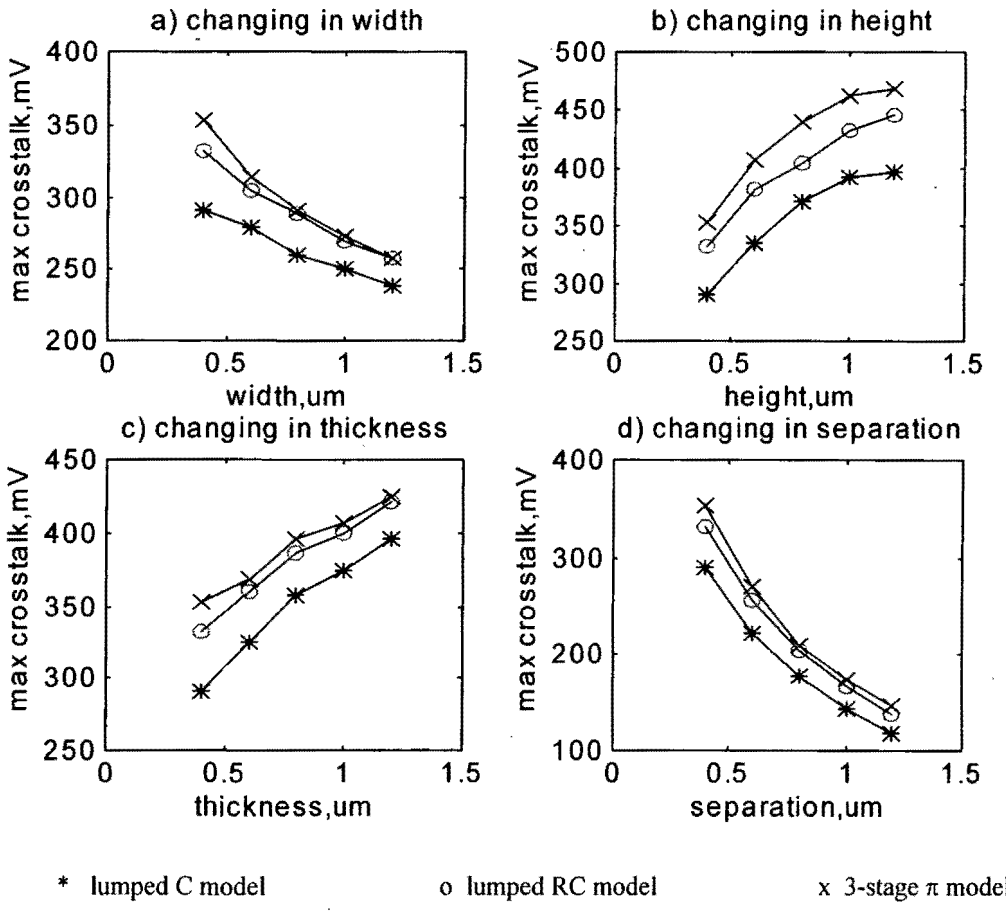


Figure 39 Simulation results indicating crosstalk against various parameters, simulations

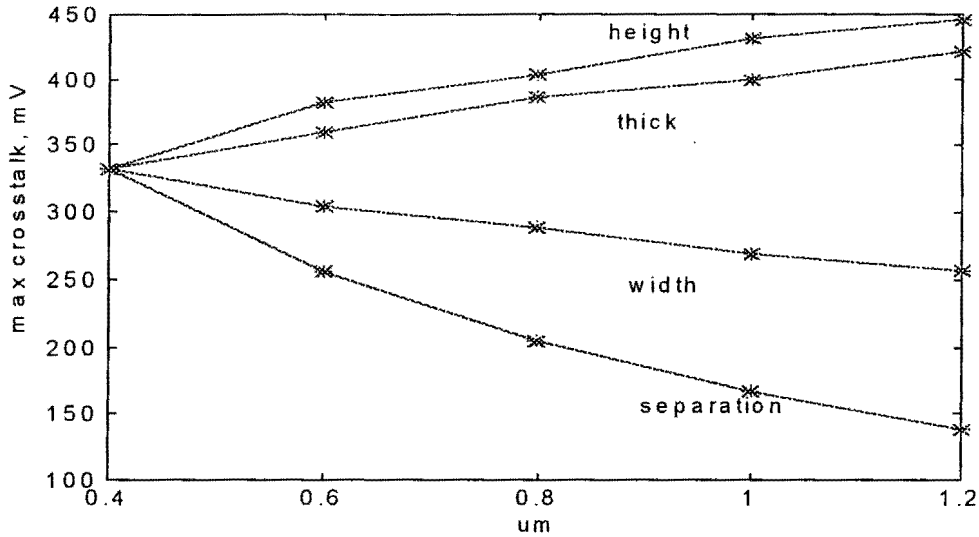


Figure 40 Variation of crosstalk with various track parameters

According to the results shown in the figures, the crosstalk will be higher if the thickness of the track or their height above the substrate is increased. Between these two, increasing the height would have more effect. Reduction of crosstalk can be achieved by increasing the separation or increasing the track width. Increasing the separation, however, would also result in the circuit requiring large area which can be very undesirable. Increasing the width, on the other hand, not only increases the size of the circuit but will also reduce its speed. Thus when designing an integrated circuit busses, compromise must be made between the desired performance in terms of high speed and minimal size circuits and the circuit reliability for which crosstalk must be small

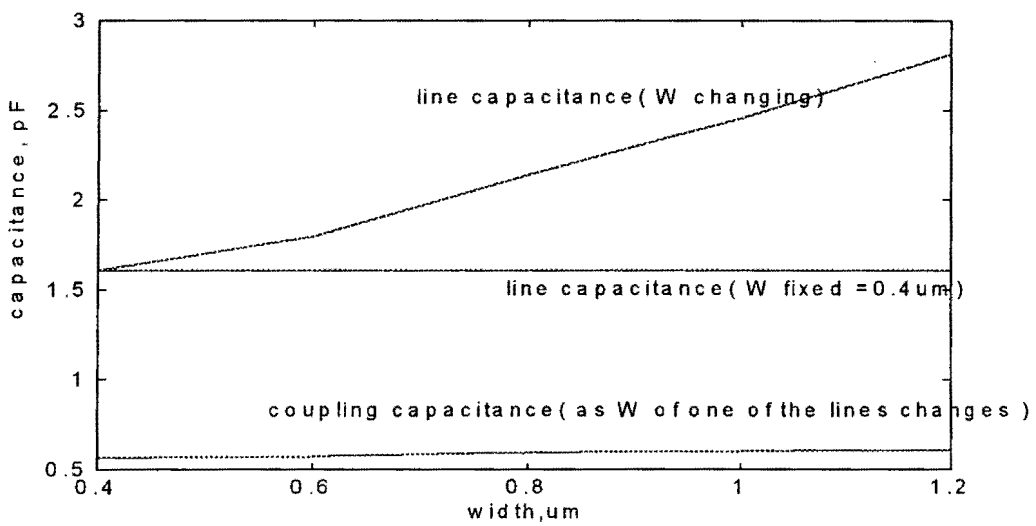
3.4 Crosstalk in an Irregular Structured Two-line System

Practically, when designing integrated circuits, it is not necessary that two bus lines should have the same parameters, as has been assumed throughout the previous section. The thickness and height are normally given by the technology used and so can not be altered. That leaves the lines width, length and the separation between them as the values that the designer is able to adjust. The effect of various parameters on regular-structured two lines system on crosstalk have been shown in the previous section. In the irregular case the bus lines can actually be classified to two configurations. The first

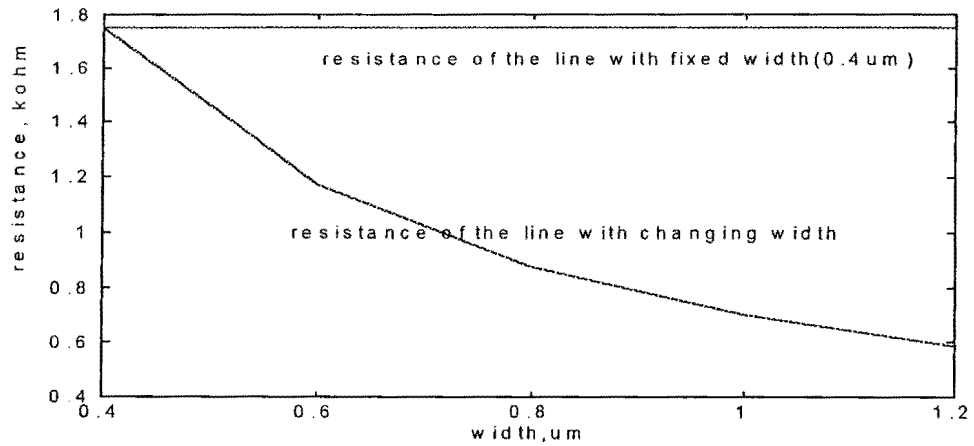
situation is when the width is different for each line and the second situation is when there is a branch (or branches) in any of the line or the length is not equal.

3.4.1 Crosstalk in Lines of Different Width

In sections 3.1.1.2-3 we have separately looked at the effect of the two lines having different resistance and capacitance on the crosstalk. In a system where the lines have different width the effect on the crosstalk is combination of changes in both. This is due to the fact that by increasing the width, not only the line capacitance will be made larger but the resistance will be made smaller. Increasing the width of either of the lines would also introduce more coupling capacitance, since this effectively introduces more electric field from the top and bottom of the tracks. Figure 41 shows how resistance and capacitance change with width. Here the separation, height and the thickness are kept at 0.4 μm, the values for 0.35 μm technology. The length of the lines is assumed to be 1 cm.



a) self and mutual capacitance vs track width



b) track resistance vs track width

Figure 41 Resistance and capacitance of the tracks as the track width changes

Even though the figures confirm the previous arguments. The real effects on crosstalk can be more difficult to analyse. If the width of line 2 is the one which is increased, this actually means that C_2 is increased and R_2 is decreased. Increasing the capacitance of any of the lines alone would result in smaller crosstalk, as discussed in section 3.1.1.3. On top of that, reduction in R_2 would also have the same effect of reducing crosstalk, as discussed in section 3.1.1.2. Together, it is certain that the resulting crosstalk will be less. The argument is confirmed by simulation results shown in Figure 42 (a)

If, however, it is actually in line 1 where the width is larger, the situation can be different. Even though the increase in one of the line capacitances will guarantee some reduction in crosstalk, the resulting smaller resistance of line 1 will have the effect of actually increasing the crosstalk. Thus the final outcome of the crosstalk depends on whether it is the unequal capacitances or resistances which actually have more effect on the crosstalk. In larger technologies, the resistance of the line is relatively low due to its large size. The total resistance is therefore dominated by the source resistance. Hence in this case the change in line resistance due to the change in width will result in little different in total resistance of the lines and so less effect on crosstalk. In smaller technologies, however, the line resistance is high and its value is comparable to that of

the source. The change in line resistance, therefore, can have more effect on crosstalk. Figure 42b) summarises the idea.

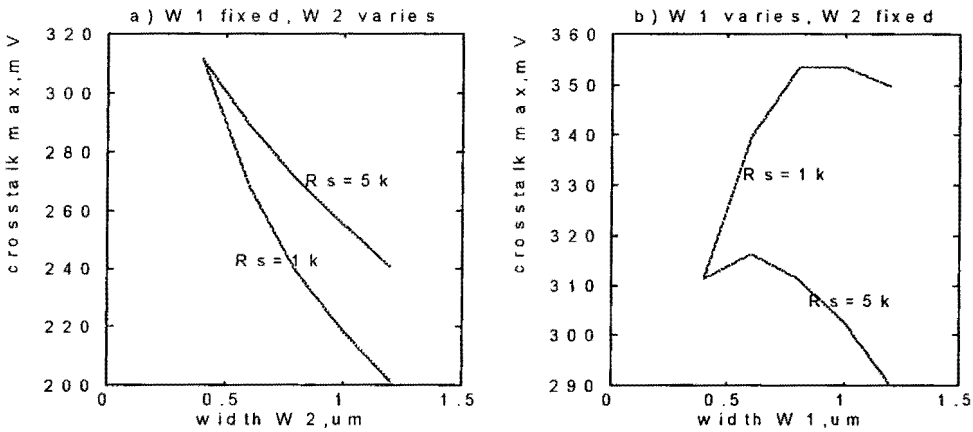


Figure 42 Crosstalk under different line width

3.4.2 Crosstalk in Lines with Branches

Another possibility where the problem of irregularity can occur is when one or both of the lines has branches. In integrated circuits, the signal buses can be regarded as a main medium where signals are carried though various parts of circuits. It is very likely, therefore, that the lines are connected to large number of sub circuits and thus each line is expected to have large fan-outs. This actually ensures that there are to be branches in the lines. This is illustrated in Figure 43.

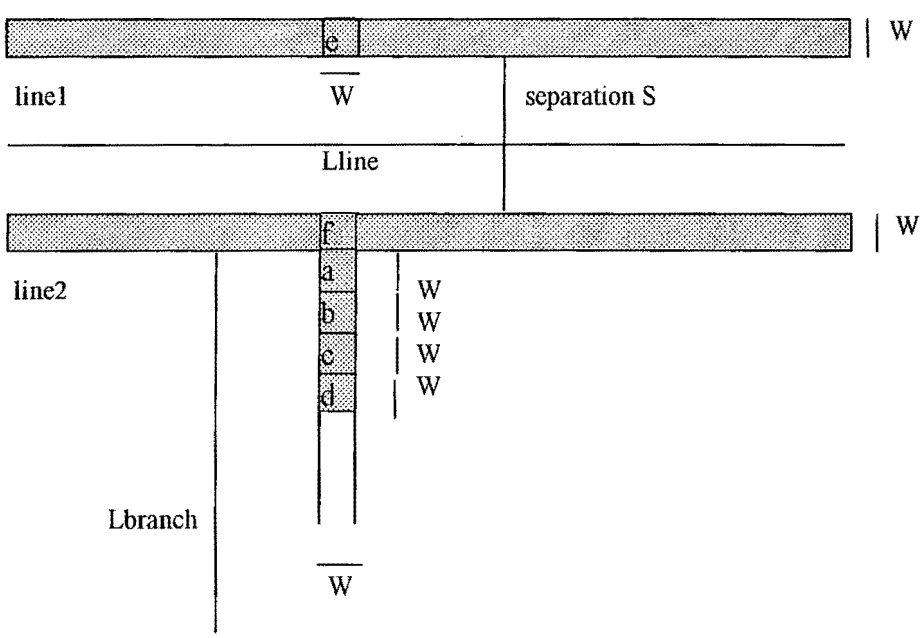


Figure 43 2-line system with branching track

To consider first the effect of a branch on the coupling capacitance, the branch line is divided into square blocks of WxW size, where W is the width of the signal lines and the branch. Block a, as seen in the figure is the closest block to the signal line. It can be assumed that roughly the block is parallel to the equal sized block e in the other line and thus they can be treated in the same way as a normal parallel lines considered previously, with the length of W and the separation of W+S. The separation between block b,c,d and e would be S+2W, S+3W and S+4W respectively. The following table shows how these equivalent blocks contribute to the coupling capacitance.

	Self capacitance, aF	line resistance, ohm	coupling capacitance,aF
Block a	Ca = 57.51	Ra = 70m	Cae = 11.22
Block b	Cb = 55.79	Rb = 70m	Cbe = 6.86
Block c	Cc = 55.2	Rc = 70m	Cce = 4.63
Block d	Cd = 54.96	Rd = 70m	Cde = 3.32

Table 7 Capacitances and resistances in branches

It can be seen from the table that these blocks add very little coupling capacitance when compared to the coupling capacitance caused by the two signal lines which can be hundreds of picofarads for a centimetre long line. The other equivalent blocks in the branches which are further away would contribute even less coupling capacitance. It is therefore justified to say that having branches will have virtually no effect on the coupling capacitance.

Adding branches to the signal lines, however, will surely introduce changes in total line capacitance and resistance. In the case of total capacitance, the value will be increased proportionally to the length of the branch line. For the total resistance, the value will be virtually unchanged. Hence the effect of branching will only be the further introduction of capacitance and the situation is therefore similar to that discussed in section 3.1.1.3, where the lines are with different capacitance. Figure 44 illustrates the effect of branching on the maximum crosstalk. Here the 0.35 μm technology is used, with the width, separation, thickness and the height of the lines are all 0.4 μm[36]. It can

be seen that by introducing the branch in either or both of the signal lines the crosstalk is effectively reduced.

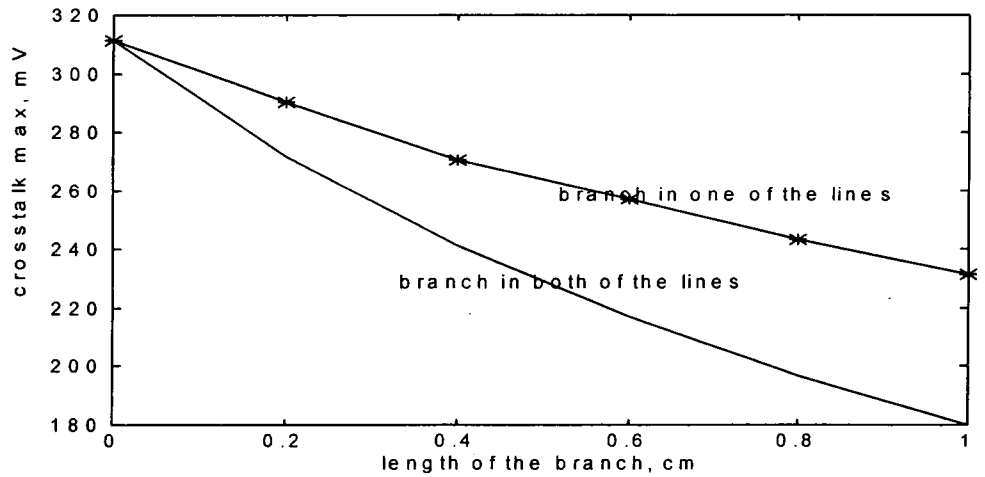


Figure 44 Crosstalk with branching

3.5 Worst-case Analysis of Crosstalk in a Two Line System

So far the effects of various parameters on the crosstalk have been generally discussed. Because so many factors are involved it is very difficult to find simple expressions which could cover all the effects on the crosstalk. If, however, the object is such that a first hand prediction of the crosstalk for a given technology is to be realised, together with the fact that there are number of parameters which are defined by the technology used and can not be altered, then a simple relationship is possible.

For the tracks in an integrated circuit, the thickness and the height of the tracks are given by the process technology. That leaves the width, length and the separation between them that the designer can adjust. The minimum values of width and separation are specified in the process design rules and would typically be near that of the minimum dimension technology. It has been shown that by increasing the separation, the crosstalk is reduced. Thus if the separation is kept at the minimum, the worst-possible crosstalk will result. The same can be said for the width, even though it has been shown that by increasing the width in line 1 the crosstalk can be increased. The increase is however relatively small and together with the fact that for a low-power and high-speed IC design the width would ideally be kept at its minimum value anyway, it is

therefore reasonable to keep the width at its minimum for the worst-case analysis. The length has been shown to have little effect on crosstalk (section 3.1.2) so it can be kept at any respectable value.

Worst-case analysis is a useful method because, under this condition, if the designer is satisfied that the crosstalk would not result in a reliability problem, then adjusting any parameters would always result in a further reduction of crosstalk which is desirable. If all the track parameters are fixed as discussed above then the controllable parameters which determine the crosstalk would be the sizes of the buffers. It has been shown that by having the minimum size buffer in the non-switching line and a larger buffer in the switching line the crosstalk is maximised. Thus for worst-case analysis a relationship can be defined in term of the maximum crosstalk and the sizing of the transistors in buffer 1. The physical values of the tracks in various technologies are given in table 8. These values are gathered from [33]-[36]

technology	height, μm	thickness, μm	width, μm	separation, μm
0.35	0.4	0.4	0.4	0.4
0.5	0.6	0.6	0.8	0.8
0.7	0.7	0.7	1.0	1.0
1.0	0.8	0.8	1.5	1.5
1.5	0.9	0.9	2.4	2.4

Table 8 Track parameters for various technologies

Once the values of the parameters are decided, simulations are carried out to find the relationships between the ratio of the buffers and the crosstalk produced. Different characteristics are obtained for different technology since the physical parameters of the tracks and the transistor technology are different. Simple polynomial equations can then be used to describe the relationships. The polynomial equations shown below are obtained using curve fitting facility available in MATLAB. They represent the result with maximum error of around 10 percent and can be used for the value of x up to x = 100, where x is the ratio between W_1/W_2. (W_1 is the n-channel transistor width of the buffer in line1 and W_2 is the transistor width of the buffer in line 2, for this case W_2 is at

its minimum) Here only 0.7, 0.5 and 0.35 μm technologies are shown as the older technologies are virtually obsolete.

- for 0.7 μm technology:

$$ct_{max} = -0.0001x^4 + 0.021x^3 - 1.6219x^2 + 46.9282x + 123.5717 \quad (3\text{-}25)$$

- for 0.5μm technology:

$$ct_{max} = -0.0001x^4 + 0.0198x^3 - 1.5727x^2 + 44.0932x + 119.7107 \quad (3\text{-}26)$$

- for 0.35 μm technology:

$$ct_{max} = -0.0001x^4 + 0.0189x^3 - 1.4427x^2 + 41.8455x + 148.9282 \quad (3\text{-}27)$$

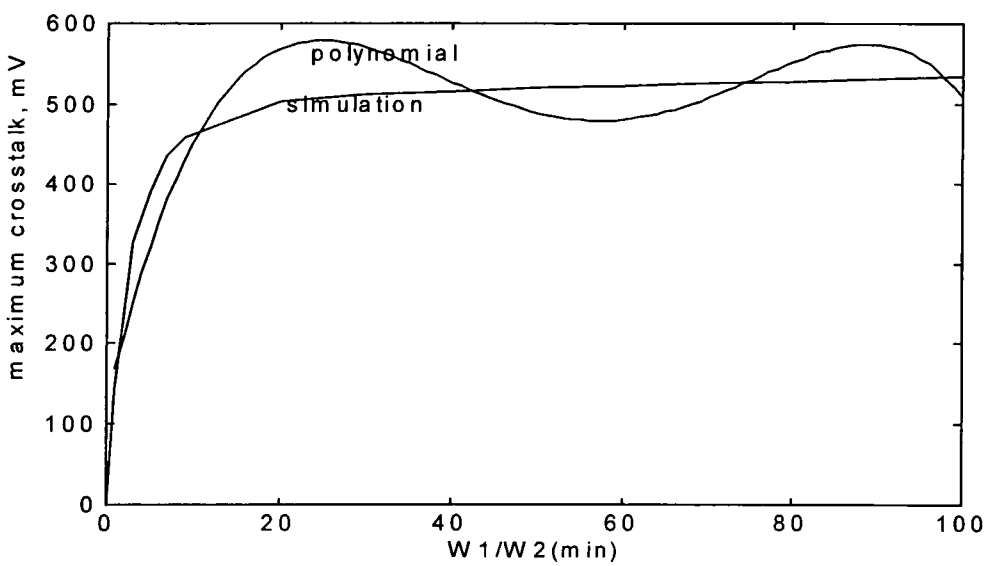


Figure 45 Maximum crosstalk vs W_1/W_2

Figure 45 shows the result of the 0.7 μm case. It can be seen that even with the large ratio, the amount of crosstalk is still relatively insignificant in term of potential source for logic fault. It can be said therefore that in the 2-line system the crosstalk generated is not large enough to cause any malfunctioning to the circuit. Given this result, the potentially more error-prone multiple-line system is investigated in the next chapter.

3.6 Summary

In the chapter, we have seen how various factors can influence the crosstalk. They can be categorised into three main factors. The first factor is the sizing of the buffers. It has been shown that crosstalk is maximised when a line has a weak buffer and is influenced by lines with larger buffer. Furthermore, even when all buffers in a bus are the same dimensions, crosstalk increases with increasing buffer dimensions. The second factor is the physical parameters which between them control the impedance (predominately resistance and capacitance) of the tracks. Most of the parameters, however are process defined while the adjustable width and the separation are normally kept at their minimum values. The last factor is the number of the switching lines. The larger the number the higher the crosstalk. Out of the discussions, mathematical equations and MATLAB functions for the ideal 2-line system have been produced. Worst-case analysis for the sizing of buffers for arbitrary crosstalk in the 2-line given certain crosstalk has been produced for each technology.

CHAPTER 4 *Crosstalk in Multiple-line System*

In chapter 3, crosstalk in the 2-line system was extensively discussed. The configuration was useful as it can be used to clearly express how the crosstalk can be influenced by various factors. In practise, however, it is most common that more than two lines are used to form signal buses in ICs. For example sending a byte word would require 8 signalling lines to transmit the data. Given this reason it is important therefore to investigate the characteristics of the crosstalk under such circumstances and then to decide whether it could cause any faults to the system. Furthermore, there are actually a number of metal layers used in modern ICs, and the analysis is therefore divided into two categories, one when all the tracks in on the same layer and the other is when the tracks are on different layes.

4.1 Crosstalk in Single Level Multiple Line system

In this system, the metal tracks run parallel to each other on the same layer above the substrate (height H). Each line is driving a capacitive load C_L and is connected to an input buffer. The set-up is as shown in Figure 46.

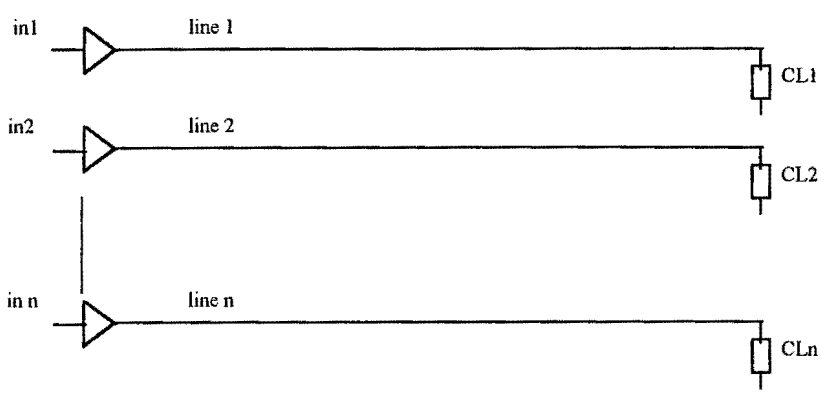


Figure 46 Single level multiple-line system

Unlike in the 2-line system situation where there is only one coupling capacitance between the lines, in the multiple-line system there exists coupling capacitance between every pair of the lines. This results in a complicated structure of the circuit which can be difficult to analyse. Using Mattaei's method [31] described in chapter 2, the self and mutual capacitances, can be presented in term of capacitance matrix. Table 9 shows an example of such a matrix.

j \ i	1	2	3	4	5	6	7	8
1	1690	407.95	35.45	15.34	9.73	5.71	4.12	3.9
2	407.95	1820	397.37	31.04	12.9	7.18	4.68	4.12
3	35.45	397.37	1820	396.94	30.81	12.78	7.18	5.71
4	15.34	31.04	396.94	1820	396.87	30.81	12.90	8.73
5	9.73	12.9	30.81	396.84	1820	396.94	31.04	15.34
6	5.71	7.18	12.78	30.81	396.94	1820	397.37	35.44
7	4.12	4.68	7.18	12.90	31.04	397.37	1820	407.94
8	3.9	4.12	5.71	8.73	15.34	35.44	407.94	1690

in femto farad

Table 9 Capacitive matrix

According to the table, C_{ij} is the coupling capacitance between line i and j, while C_{ii} is the self capacitance in line *i*. For this example the matrix represents a system of 8 lines. The technology used is the 0.7 um with the track parameters as shown in table 8. The length of the lines is set at 1 cm. It can be seen that the matrix is symmetric. This is due to the fact that C_{ij} and C_{ji} actually represent the same value. The coupling capacitance between the immediately adjacent lines provides the largest value of capacitance. This comes as no surprise as the separation between these is smallest and there is no other lines between them Figure 47 shows how the crosstalk varies across the bus. The graph represents time separate simulations in which the line to be analysed is held fixed at 3.3v (via a buffer with input = 0) and the other tracks are simultaneously switched to 0. Here all the buffers are of the same size.

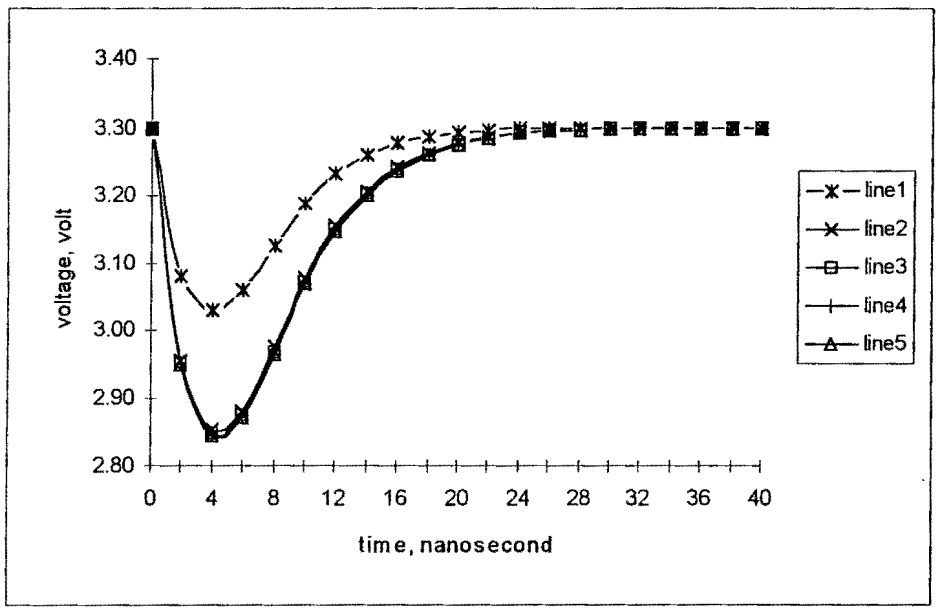


Figure 47 Variation of crosstalk in different line.

By having only one of the lines not switching while the rest are, it can be seen that the largest crosstalk is developed when the line is in the middle(line 4 or 5 in this case). Direct mathematical analysis is complicated but generally it can be said that coupling between any two lines reduces significantly as their separation increases, as seen in Table 9. By having the non-switching line in the middle it is ensured that the minimum possible separation exits between the non-switching line and the furtherest switching line. Thus the total effect of the coupling pairs is maximised. In another example shown in Figure 48, the crosstalk on the middle line caused by various combinations of switching lines is shown.

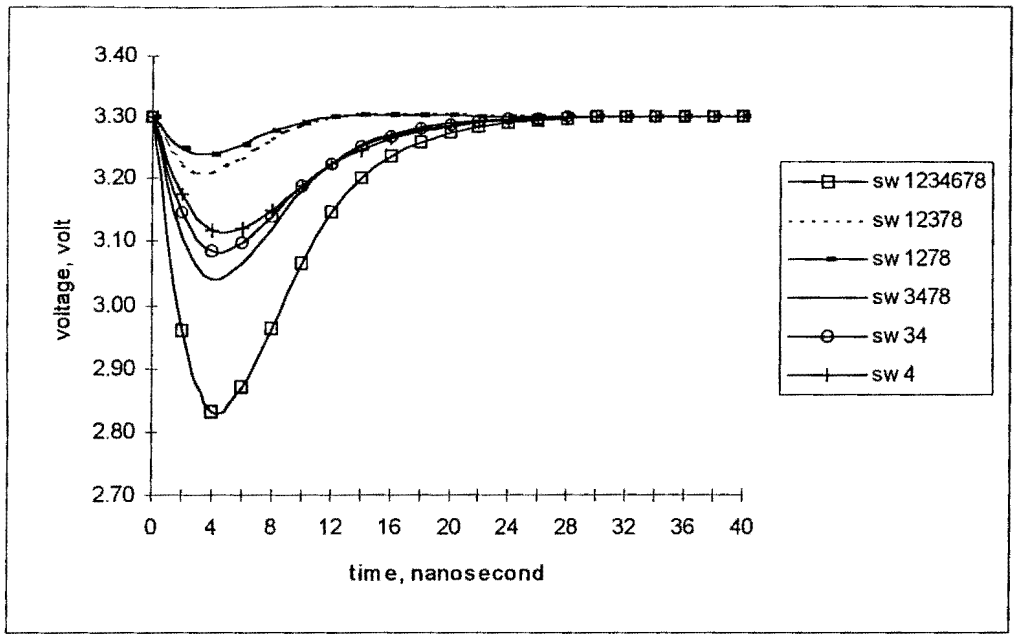
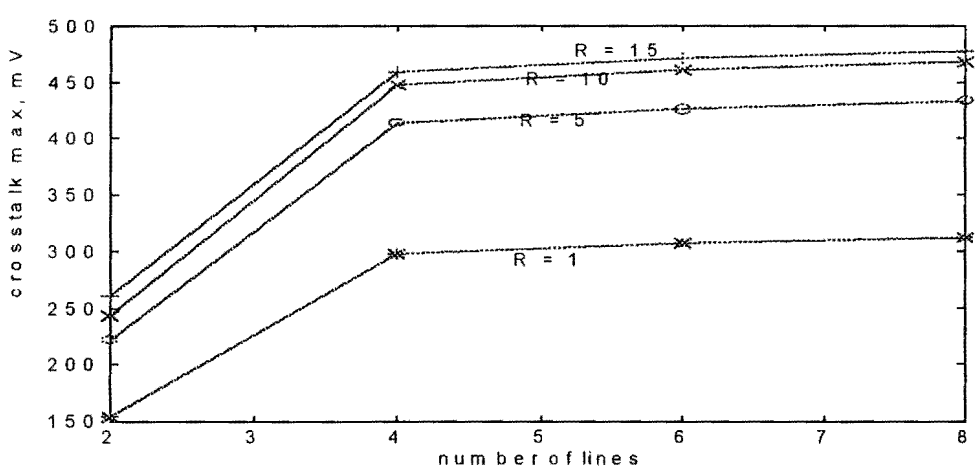


Figure 48 Crosstalk under various switching configurations

It can be seen, together with the result from figure 47, that the largest crosstalk is caused by having the non-switching line in the middle while the rest are all switching. In these figures, the number of the lines in the system were kept at 8. Different numbers of lines result in different amounts of the crosstalk. The following figure shows how crosstalk changes when the number of the lines is increased.



R = ratio between the actual and minimum size of the buffers

Figure 49 Variation of crosstalk with increasing number of lines in bus

In figure 49, the crosstalk is measured on the middle line which is the only non-switching line. It can be seen that by increasing the number of the lines the crosstalk will increase. The effect is expected since having more lines means that further coupling capacitances caused by the additional lines are introduced, leading to a stronger overall effect of coupling capacitance on the line. The figure also reveals the effect of sizing the buffers on the crosstalk. Here all the buffers in the bus are at equal sizes and the figure plots the resulting crosstalk for sets of the buffers of various sizes. It can be seen that by having larger sizes for all the buffers the crosstalk in increased. The effect is similar to the one discussed in section 3.1.2 (figure 25) where the maximum crosstalk will in fact fall slowly again once the buffers' sizes are well past 20 times their minimum.

To show more clearly how the set-up of the buffers can influence the resulting crosstalk further simulations have been run as shown in Figure 50. In this figure the system comprises eight signal lines ,with line five being the middle and non-switching line. Three experiments are illustrated with the buffer in line 5 having the sizes indicated. The result shows that, as seen with the 2-line case, largest crosstalk is occurred when the buffer of non switching line is kept at minimum while the others have higher values. The higher they are the larger the crosstalk.

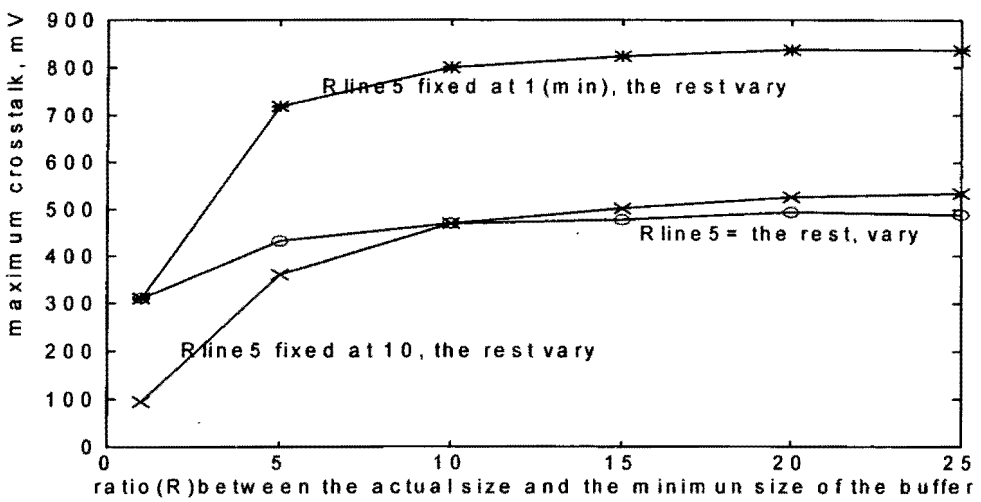


Figure 50 Crosstalk with different set-up of buffers

4.2 Worst-case Analysis of Multiple Line System

In the 2-line system it has been shown that worst-case analysis is acieved by having all the physical parameters of the tracks at their minimum and the crosstalk is then found to be governed by the size of the buffer in the switching line, with the buffer in the non-switching line kept at minimum size. With the result shown in the previous section we see that crosstalk in multiple line system will also be increased by adding more switching lines, the worst-case analysis of the crosstalk in multiple-line system can then be found as a combination of both effects. The configuration can be such that the buffer of the non switching line is to be kept at its minimum size while the others buffers as well as the number of the switching lines are adjusted. Figure 51 shows some results under such conditions using 0.7 μm technology.

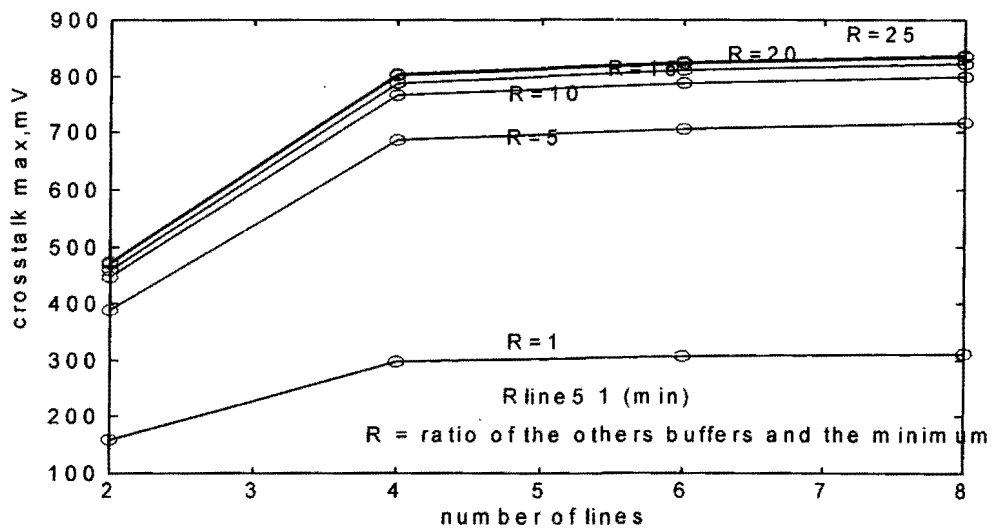


Figure 51 Crosstalk under different number of lines and sizes of buffers

It can be seen from the Figure that the crosstalk will increase by either increasing the number of switching lines or the buffer ratio. Because this involves two determining factors, a simple relationship can not be found between these and the crosstalk is hard to extract. The figure, however, also reveals that the crosstalk does not change significantly as the buffer ratio goes past a value of ten. Thus a simple equation describing relationship between the crosstalk and the number of the switching lines is possible for the worse-case situation if the buffer ratio is to be kept at a large value. It is reasonable

to say, according to the figure, that the ratio between the switching and non-switching buffers of 25 should be enough for the worst-case situation. Figure 52 shows how the crosstalk varies with the number of the switching lines with this value of ratio.

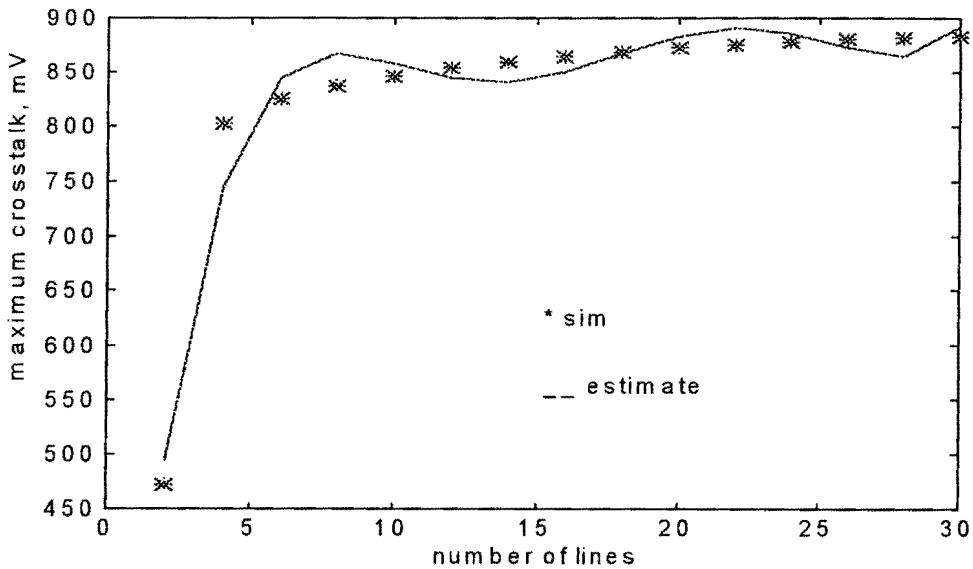


Figure 52 Maximum crosstalk VS number of switching lines

The figure shown above is for a 0.7 μm technology. The polynomial equation for the maximum crosstalk in terms of the number of the switching lines for this worst-case configuration is then given below, together with the equations for other technologies. This equations are valid for the number of switching lines up to 30,

- for 0.7 μm technology:

$$ct_{max} = 0.001n^5 - 0.868n^4 + 2.9176n^3 + 45.45n^2 + 35.17n + 4.698 \quad (4\text{-}1)$$

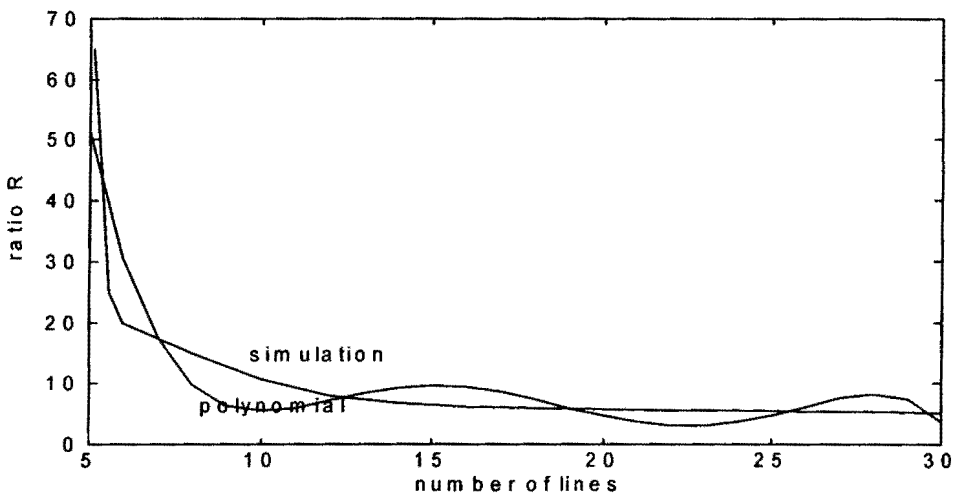
-for 0.5 μm technology:

$$ct_{max} = 0.0006n^5 - 0.0573n^4 + 2.1454n^3 - 37.8n^2 + 309.886n - 47.2029 \quad (4\text{-}2)$$

-for 0.35 μm technology:

$$ct_{max} = 0.0004n^5 - 0.0435n^4 + 1.7528n^3 - 33.1425n^2 + 291.0365n - 59.6542 \quad (4\text{-}3)$$

Alternatively, instead of finding the relationship between the crosstalk and the number of lines, another way of interpreting the results is to find the relationship between the size of the buffers and the number of lines given a particular level of crosstalk. For the 0.7 μm technology, it can be seen from the graph that the crosstalk does not increase much regardless of how large the number of the lines or the buffers are. The crosstalk in this case is set at 25 percent of the supply voltage (825 mV) and the relationship between the number of line and the sizes of the buffers is as given in Figure 53.



R is the ratio between the actual size of all the buffers(except in line 5) and the minimum size
R of line 5 (the middle non-switching line) is kept at minimum, i.e. =1

Figure 53 Number of lines vs the buffers' sizes given crosstalk of 825m V

Using the result shown in figure 53 a polynomial equation describing relationship between the number of the lines and the size of the buffers can be found as shown in equation (4-4). Here n is the number of the lines and R is the size of the switching buffers given as a ratio to it minimum value.

$$R = -0.0002n^5 + 0.0234n^4 - 0.8476n^3 + 14.5726n^2 - 118.5591n + 337.9206 \qquad (4\text{-}4)$$

The equation is useful in such a way that it guarantees that given a particular number of lines, using the value of R obtained from the equation for the switching buffers would ensure that the crosstalk produced will be around 25 percent of the supply voltage. Any alterations from the set-up such as lowering the values of the switching buffers, increasing the value of the non-switching buffer, having different combination of

switching or non switching lines, or adjusting any of the physical parameters of the tracks from their minimal values would always lead to crosstalk, which is clearly not desirable.

For the smaller technologies it is likely that crosstalk will be higher. The following equations show the results. These equations are valid for number of the lines up to 30

- for 0.7 μm technology , 25 % crosstalk: (the equation is valid for $n \geq 5$)

$$R = -0.0002n^5 + 0.0234n^4 - 0.8476n^3 + 14.5726n^2 - 118.5591n + 337.9206 \qquad (4\text{-}5)$$

- for 0.5 μm technology, 25 % crosstalk : ($n \geq 3$)

$$R = -0.0003n^5 + 0.0274n^4 - 0.9404n^3 + 145.0397n^2 - 110.9246n + 305.6295 \qquad (4\text{-}6)$$

- for 0.35 μm technology, 25 % crosstalk: ($n \geq 3$)

$$R = -0.0001n^5 + 0.0051n^4 - 0.1771n^3 + 2.8687n^2 - 21.6365n + 66.0155 \qquad (4\text{-}7)$$

4.3 Crosstalk in Multi Layer Metal Multiple Line Systems

In early technologies, it was common for a process to have one metal layer. Any signal tracks which must be laid-out crossing other signals were converted into polysilicon tracks. Polysilicon however, possesses relatively larger resistance and self capacitance and therefore having large number of poly lines can slow the circuits. On top of that, modern technology requires circuits of increasingly complicated functions that in order to keep the die size reasonably small signals may have to cross each other several times. Thus integrated circuits normally now contain at least 2-3 metal layers, and with state-of -the-art Ics, even more layers are used. Most of the time the signal tracks cross each other othogonally, meaning that there are only fractional parts of the tracks which are directly above or below the others, resulting in very small coupling capacitance between them. It is, however possible that the tracks may run parallel to each other. In

this case the coupling capacitance introduced can be significant and can not be neglected. The following figure shows an example of the two metal layer with four signal lines.

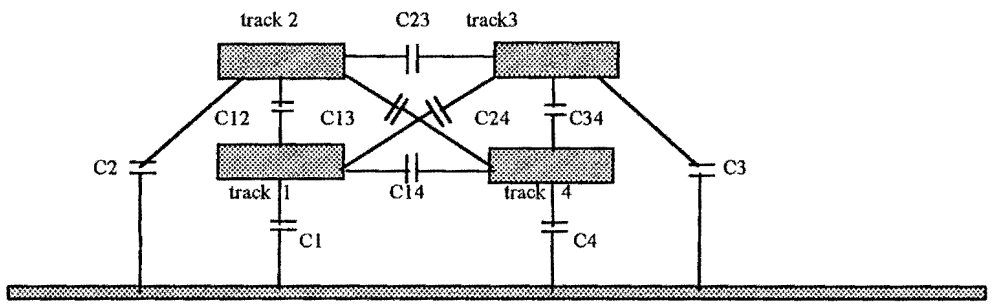


Figure 54 Two layers, 4-line system

The figure shows the equivalent capacitance network for 2-layer tracks. For 1 cm long lines in a 0.35 μm technology, if all the lines are parallel with the inter-layer thickness of 0.4 μm and the tracks are all similar, then the capacitance matrix is:

i \ j	1	2	3	4
1	1600	549	380	563.69
2	549	1150	681	380
3	380	681	1159	549
4	563.69	380	549	1600

Table 10 Capacitance matrix for 2-layer 4-line system, fF

It can be seen from the table that the coupling capacitance introduced by having another line directly above it is relatively large with the value comparable to that introduced by the neighbouring line in the same plane. To illustrate the effect on the crosstalk, simulation results are shown below comparing the results from various

switching configuration in the 2-layer system with those from the single-layer 2-line system.

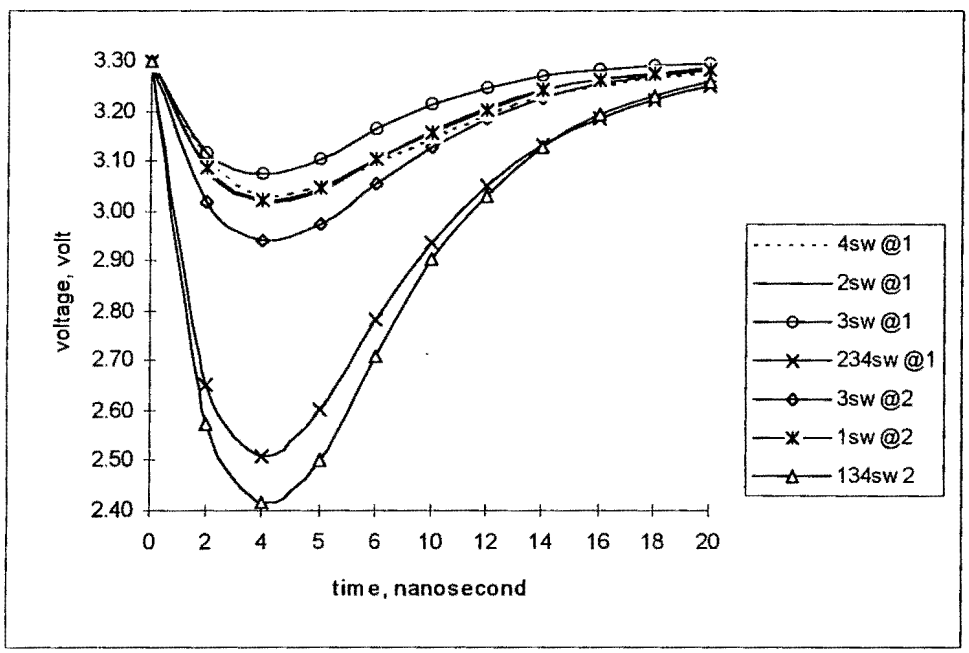


Figure 55 Crosstalk in 2-layer system

It can be seen from the figure that the introduction of additional layers lead to an increasing in crosstalk. Results from simulations performed by the author show that for worst-case analysis, where a similar configuration to the single layer analysis is used together with all additional lines lying above the original lines switching, the value of the crosstalk produced would be approximately doubled. The crosstalk in the second layer tracks alone would have a value about 30% higher than the original analysis due to the fact that the self capacitance is lower as the tracks are farther above the substrate.

For all of these results, one must be very careful when dealing with the higher level tracks. Under typical design rules, it is common that the metal tracks in the higher level can have the width and the separation values to be up to 50% larger than those in the immediate lower level. These increases in width and separation will lead to larger

track self capacitances and smaller coupling capacitances respectively. Together this will mean that the crosstalk between neighbouring lines on the same higher level may not be as high as expected under the all-identical lines arrangement discussed earlier. Results actually show that by increasing the width and separation by 50% the crosstalk in the single higher-level tracks is slightly less than that in Metal1. The values of the dominant coupling capacitances, the ones between the tracks directly above each others, however will remain almost the same and thus for the multi-level configuration the earlier analysis still holds. It should be stated here that, since the higher-level tracks often carry global signals such as the clock signals or the supply voltage, it would not be common to find data signals in higher layers implying that the situation of having multiple -level tracks all lying parallel to each others will be rare. Although it may occur in certain types of integrated circuit.

4.4 Summary of the chapter

The chapter introduces further analysis into systems of multiple lines, both in a single and multiple planes. It has been showed the effect of various switching configurations on the crosstalk, with a result showing largest crosstalk at the middle line. Its value is influenced by the number of the switching lines, and the ratio of the switching and non switching buffers. From this, mathematical equations and MATLAB functions for; 1) worst-case crosstalk given certain number of switching lines, 2) number of lines allowed given certain level of crosstalk and 3) ratio of the buffers allowed for the given crosstalk are developed.

CHAPTER 5 *Fault Effects of Crosstalk Defects*

In the previous chapters, the characteristics of crosstalk under various circuit configurations was extensively studied and an understanding of the crosstalk that can be expected given any particular situation has been established. Even though this information is very important on its own, its usefulness can be extended. It would be very advantageous to the designer to understand the real effects of the crosstalk on the operations of circuits and to appreciate the type of circuits and the circumstances under which any fault effect caused by crosstalk can lead to logical faults. It is the intention of this chapter to provide some analysis of such situations. However, since numerous types of circuits exist it is not possible for each type to be individually analysed. In this chapter therefore, circuits will be divided into several groups where crosstalk faults will be separately discussed. The groups are as shown below and they cover most types of circuits.

- Buffer circuits
- Static circuits
- Dynamic circuits
- Other circuits

5.1 Fault Effects on Buffer Circuits

Buffer circuits can be said to be the circuits most likely to be found connected to signal buses. Typically, it is necessary for signal lines to be buffered from the circuits at the receiving ends as these may have large input capacitances which can significantly reduce the speed of operation. The simplest form of buffer circuit is the inverter buffer, similar to that seen in the previous chapter. Figure 56 shows how buffers are placed in the system.

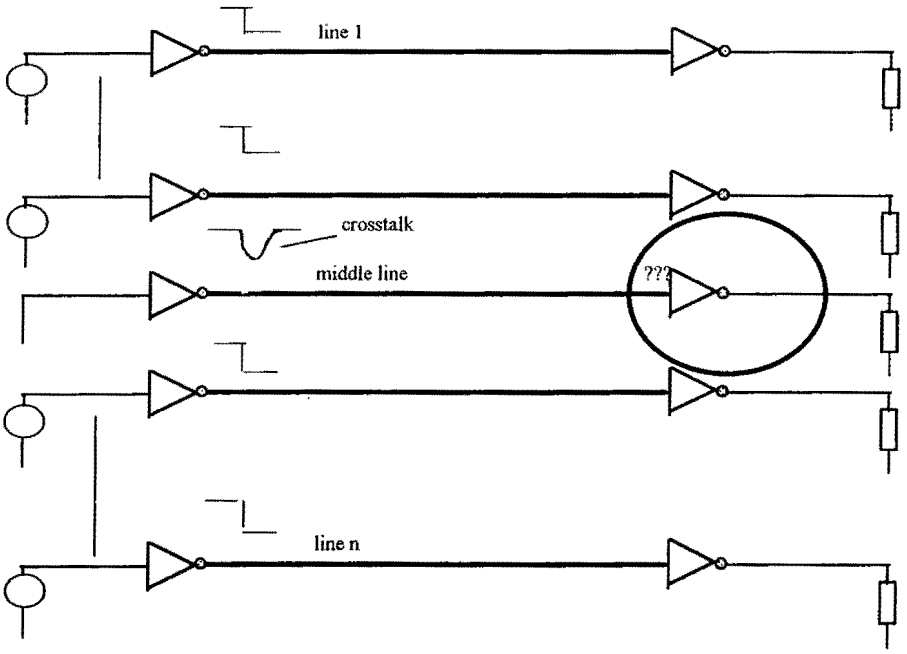


Figure 56 Signal lines driving buffers

The system shown in figure 56 represents the model used for the worst-case analysis, as discussed in the previous chapter. Here the system comprises n signal lines with all but the middle line are switching. Crosstalk is induced in the middle line. The worst-case configuration is used here mainly because it is the most likely to cause crosstalk. However, the following argument applies to any other combinations of signals

The area of interest is circled in the figure. The analysis is carried to investigate if the crosstalk, with its characteristics influenced by factors discussed in the previous chapter, can cause a logical fault. Clearly this would depend on whether the amount of the crosstalk on the line is large enough for the output buffer to switch. However, the transfer characteristic of the buffer itself is also an important factor. Different transistor dimentions in the inverter can result in different level of input required for the buffer to respond.

Although there are a number of different types of the buffer circuits, here only the CMOS inverter buffer will be discussed. This is mainly because it is the most widely used buffer due to its simplicity. The transfer characteristic of a CMOS inverter is best described by the following figure. It can be seen that it is the transition voltage V_{th} which determines the mount of input required.

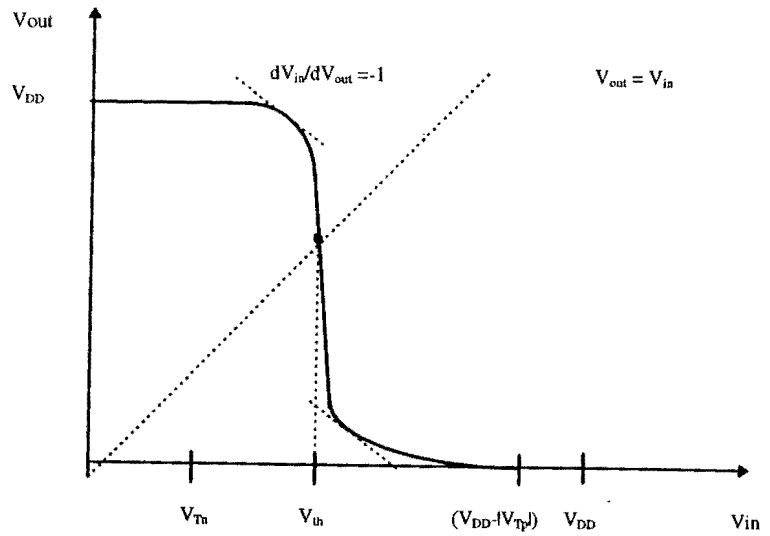


Figure 57 CMOS inverter characteristics

According to the figure, the transition voltage V_{th} is the input voltage when $V_{in} = V_{out}$. Because both of the transistors are in saturation mode, it can then be said that:

$$\frac{\beta_n}{2}(V_{th}-V_{Tn})^2=\frac{\beta_p}{2}\left(V_{DD}-V_{th}-|V_{Tp}|\right)^2 \qquad (4\text{-}1)$$

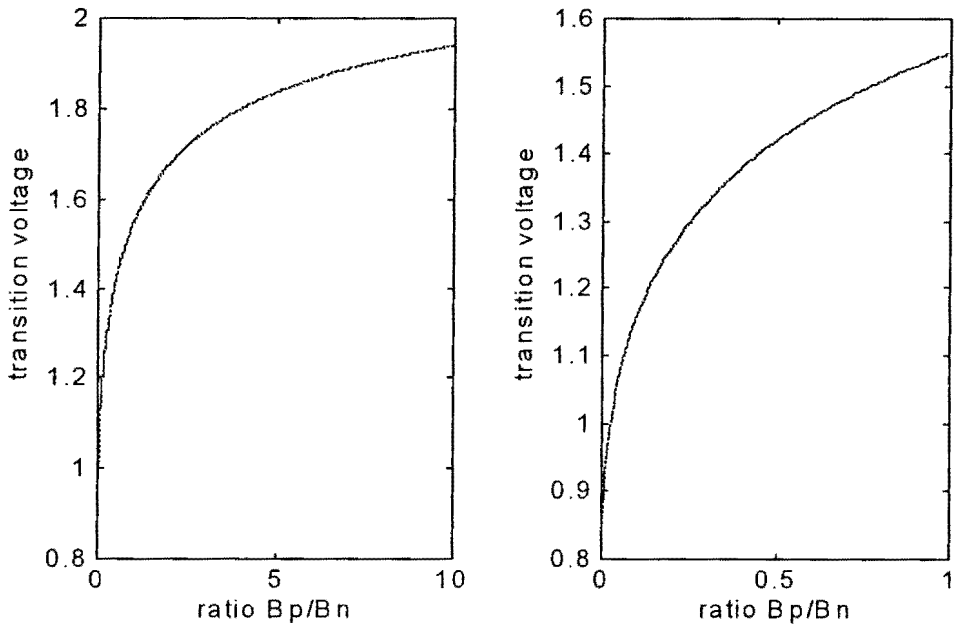
Rearranging the equation 4-1 gives:

$$V_{th}=\frac{V_{Tn}+\sqrt{\frac{\beta_p}{\beta_n}}\left(V_{DD}-|V_{Tp}|\right)}{\left(1+\sqrt{\frac{\beta_p}{\beta_n}}\right)} \qquad (4\text{-}2)$$

where $\beta_n=\mu_n\left(\frac{W}{L}\right)_n \qquad \beta_p=\mu_p\left(\frac{W}{L}\right)_p \qquad (4\text{-}3)$

Equation 4-2 illustrates that the transition voltage is controlled by the threshold voltage of each transistor, the supply voltage and the ratio between the transconductance of the p and n channel transistors. The transconductance itself is proportional to the mobility of the majority carriers in the device and its channel width, as shown in equation 4-3. If the transconductance and the absolute value of the threshold voltages of the p and n devices are equal it can be seen, according to equation 4-2, that transition voltage is precisely half of the supply voltage. Otherwise for the general case where only the width can be said to be adjustable at the designing level, it is the relationship between the

transition voltage and the width of the transistors forming the inverter which is of interest. Figure 58 shows how the transition voltage changes for different transconductance ratio of p and n channel transistors for a 0.7 μm technology, Vdd = 3.3 v.



a) Vt as W/L of PMOS changes

b) Vt as W/L of NMOS changes

Figure 58 Transition voltage under different W_p/W_n ratio

It can be seen that as the ratio of W_p/W_n gets bigger the transition voltage increases. That would mean that a larger input voltage would be required before the inverter output will switch from high to low. However, this also implies that a smaller voltage dip from the supply voltage level is required to cause the buffer to switch from low to high. Thus it can be said that the output buffer is more susceptible to a low-to-high output fault if the width of the p-channel transistor is much larger than that of the n-channel. The situation is reversed if $W_n >> W_p$ and in this case the buffer is more susceptible to a high-to-low fault.

Figure 59 shows the simulation result of a system of eight-lines on metal 2-layer with a worst-case switching configuration. The technology used is 0.35 μm with the ratio of the switching and non-switching input buffers being 25. The W_p/W_n of the output

buffer here is 3.3. It can be seen that a logic fault is introduced on the output of the non-switching line in the middle where the output is wrongly switched from 0 to V_{DD}. Because the crosstalk pulse is very narrow the period of the resulting fault will be very short. However, for circumstance where the output signal is actually connected to edge-triggered circuits or the fault occurrs simultaneously with the clock edge. Then a logic fault may propagate into subsequent circuits.

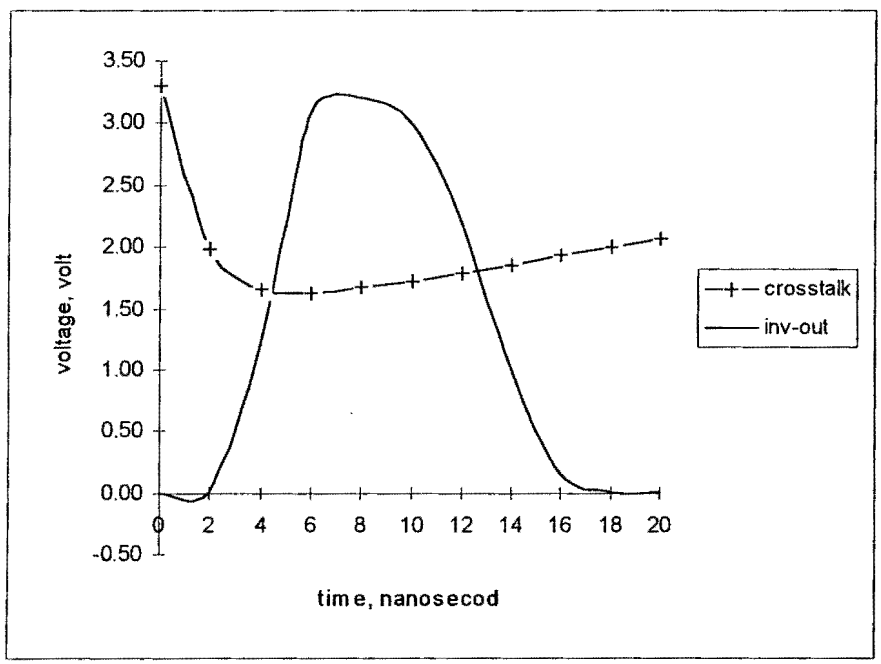


Figure 59 Logic fault in output buffer

5.2 Fault Effects on Static MOS Circuits

Under normal circumstances, it is very likely that the circuits used would be static. This is due to the superiority of such circuits in terms of performance and reliability, apparently making it very difficult for faults to be introduced. It is possible that a wide rage of circuits would be directly connected to bus lines. In this section the effect of crosstalk on static circuits will be discussed, starting from combinational circuit, then followed by bistable circuits.

5.2.1 Faults in Combinational Circuits

Combinational circuits are the most fundamental part of a digital system. They are the circuits which are used to perform various Boolean functions. To discuss each of these individually would prove an impossible task. Here the simple 2 input NAND gate is used as the sample case. The results can be extended to other circuits with appropriate modifications.

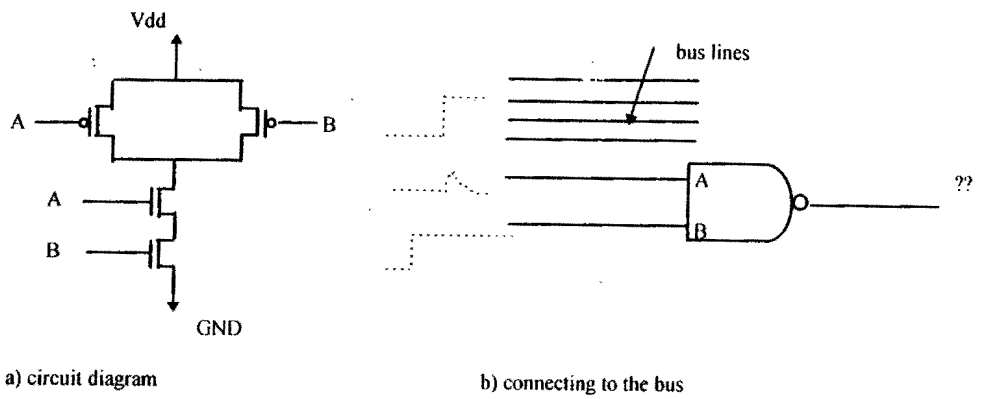


Figure 60 Two input NAND gate

Figure 60 a) shows the typical CMOS NAND circuit. An example of how crosstalk might effect the operation of the gate is given in figure 60 b). Here the input B of the gate is set high while the input A is initially low, leaving the output at logic 1 state. Input A is supposed to remain low but as the other signal lines are simultaneously switched a crosstalk is induced in input A. If the crosstalk is large enough it is possible that the gate would recognise both of the inputs as being high and as a result the output would switch to logic low value.

The amount of the crosstalk required, as for the inverting buffer, depends on the sizing of the transistors. Clearly the crosstalk must be at least as large as the threshold voltage of the n or p-channel transistor just to turn it on. For crosstalk only slightly larger than the threshold voltage a small current will flow. This would result in only a slight dip in the output of the NAND gate from its logical high value for this case. The change in the output is more significant if the width of the n-channel transistors, which are the pull-down devices, is increased. The effect is reversed for low-to-high

output switching and larger width p-channel transistors would then be required. Figure 61 helps to illustrate the effect. Here the crosstalk is set at 1.1 volts with the pulse width of 5 ns. This is a typical value of the crosstalk that can occur in a system of 12 lines (metal 1) using 0.35 μm Technology and a logical fault is produced.

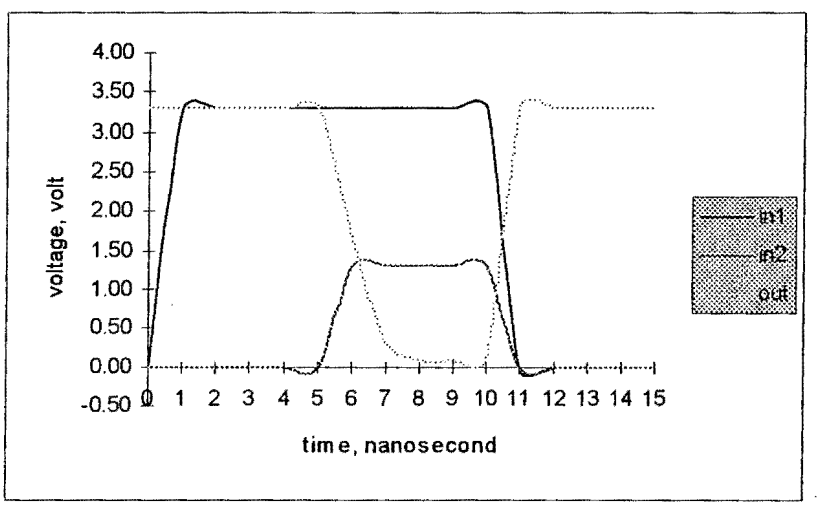


Figure 61 Crosstalk effect on NAND gate

From analogy with the inverting buffer, it can be seen that static logic gates can be more susceptible to crosstalk faults under certain design conditions. It is common practise however, for the transconductance, $\beta = \mu W/L$, of the n and p-channel transistors to be the same in order to achieve symmetric rise and fall time. This would produce a transition voltage of around a half of the supply voltage. The transition voltage will not be exactly 50% of Vdd since the threshold voltages of the PMOS and NMOS are not necessarily equal and the values also vary due to process drift. For an example 0.7 μm technology used in this work, equal βs would result in a transition voltage of 45%, while 42% and 40% arise for the 0.5 μm and 0.35 μm technologies respectively. It is reasonably then to suggest that generally for combinational circuits to register a wrong input value it is likely that the level of crosstalk needed in the input(s) would be around 40-50% of the supply voltage under normal circumstances.

5.2.2 Faults in Bistable Circuits

As for combinational circuits, faulty input signal(s) introduced by crosstalk can potentially cause the malfunction of bistable circuits. However, noise on edge sensitive inputs may lead to a fault effect being latched. Figure 62 shows a simple RS flip-flop with the set signal coupled by the switching of signals in other lines. The output of the flip-flop is as a result giving an incorrect logic high output.

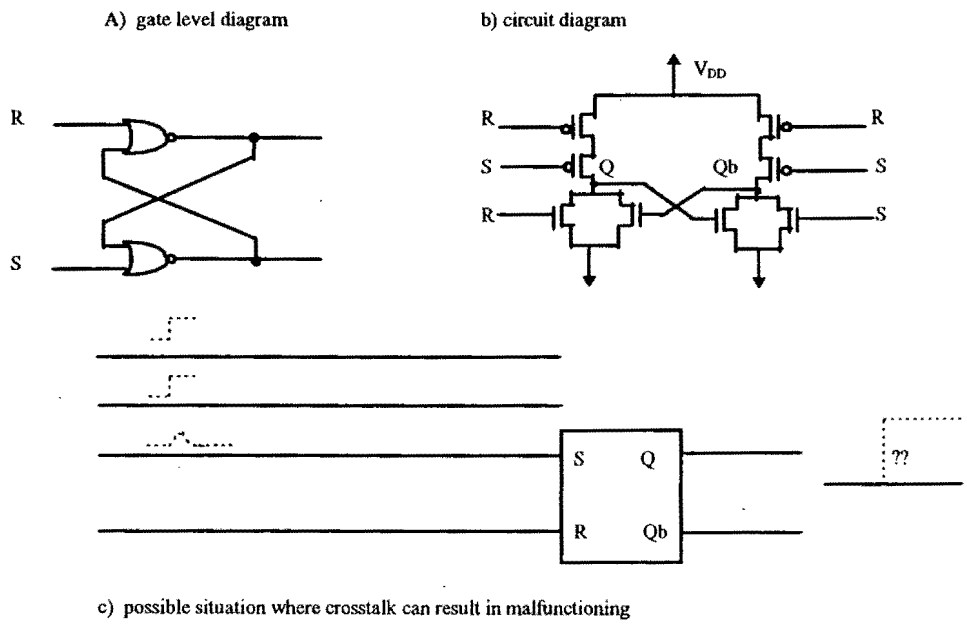


Figure 62 The RS flipflop

This simple arrangement can be used to reveal the potential malfunction which can be caused by the crosstalk. Here the flipflop is wrongly 'set'. As with the previous cases, certain amplitude and width of the crosstalk are required before the flipflop would recognise such an input as valid. Furthermore, as for the simple gate, for the flipflop with equal β value for the pull-down and pull-up networks, the amplitude of the crosstalk required would be just below $V_{DD}/2$. Figure 63 shows the simulation results of a flipflop connected to a system of eight bus lines. The set input is connected to the non-switching line in the middle of the set while the others are switching. The result confirms the prediction that the flipflop can be mistakenly set and hence a fault is produced.

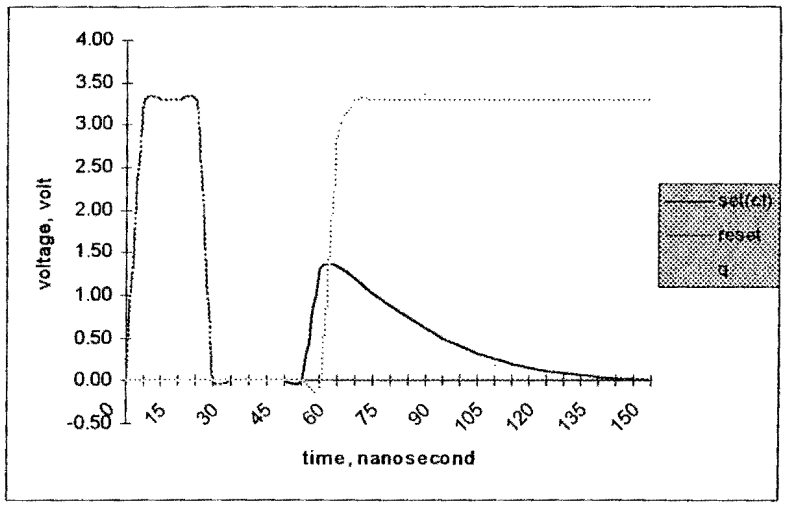


Figure 63 Simulation of the set input of an RS flipflop connected to a signal bus

Clearly faults will not only be introduced through control input(s) of a circuit, it is also possible that a clock signal input can be affected. To demonstrate this the positive-edge trigger D-type flipflop is studied. It basic structure is as shown in figure 64.

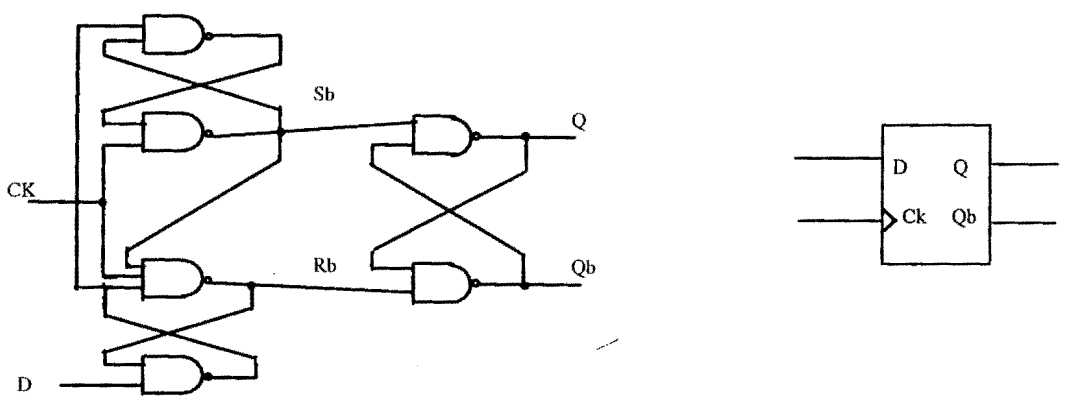


Figure 64 Positive edge-trigger D-type flipflop

Crosstalk can cause a fault in this circuit in two ways. i) It is possible that the crosstalk occurs at the D input and that an incorrect value is read at the active edge of the clock pulse. Clearly this requires coincidence within the data setup line of the crosstalk noise and the clock edge which makes this fault less likely to occur than other crosstalk failures. As for the flipflop, the amplitude of the crosstalk must be around 50%

of V_{DD} to guarantee and effect. ii) It is also possible that the crosstalk occurs on the clock input. That could result in data being latched at the incorrect time leading to a failure of the circuit. It is important to note that the significance of crosstalk depends on the width as well as its amplitude. To some extent, the larger the width of the pulse the lower the amplitude that will be required to cause a fault. This, however, will be true only to a certain value. For the example case the width of the crosstalk larger than 7 ns second would not result in any lower of amplitude necessary to switch the logic. Correspondingly that minimum requirement for the amplitude is found to be 1.5 volts for 3.3 supply voltage, which is roughly about 45%. This is very much possible as the amount of the crosstalk required is similar to those previous cases.

It should be noted here that even though in theory the crosstalk can effect the clock input of the logic, this will only occur under certain circumstances. This is due to the fact that crosstalk requires a number of signals to be switching simultaneously and that in synchronous circuits the signal would be switching only at the clock edge. This means that it is not possible to have an unexpected rising clock edge due to switching of other signals, unless the signal are switching with respect to another clock. It is therefore unlikely to be the source of concern for any single clock circuits. Faults on the clocking signals of multiple-clock system can occur not only in bistable circuits, but also on clocked combinational circuits too. This will be discussed in the next section. The following circuit shows a sample of clocked CMOS NAND circuit.

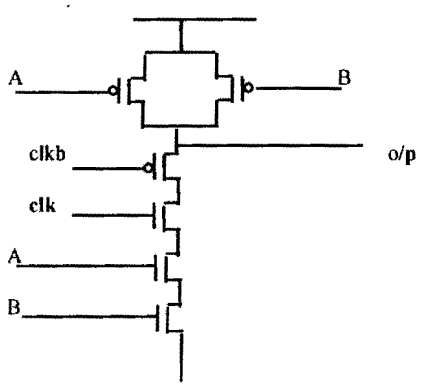


Figure 65 Clocked NAND circuit

5.3 Fault Effects in Dynamic Circuits

Dynamic circuits are commonly used in digital ICs. They are termed dynamic because they make use of the existence of capacitances in nodes to hold the desired data. Because the inherent capacitors can hold the data only for a short period of time they must be constantly updated, thus dynamic. Dynamic circuits offer advantages in term of smaller number of transistors required and lower power operation. However, they need to be very carefully designed to ensure correct operation at the desired speed.

5.3.1 Analysis of Dynamic Circuits

Figure 66 shows an example of a dynamic circuit. Shown here is a 3-input NAND gate. The part of the circuit in the dotted block can actually be replaced by any other nMOS circuit realisation of Boolean functions. The operation of the circuit is divided into 2 states. When the clock is low the output is charged to a high value(Vdd) regardless of the inputs and the circuit is said to be in the precharging state. When the clock goes high the logic of the output is evaluated according to the values of the inputs. This is the period where the output is valid. Figure 67 shows an example of the operation of the 3-input NAND gate.

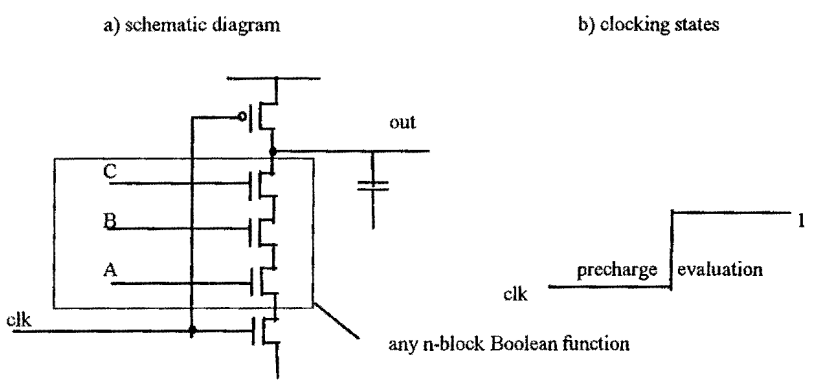


Figure 66 Dynamic CMOS logic

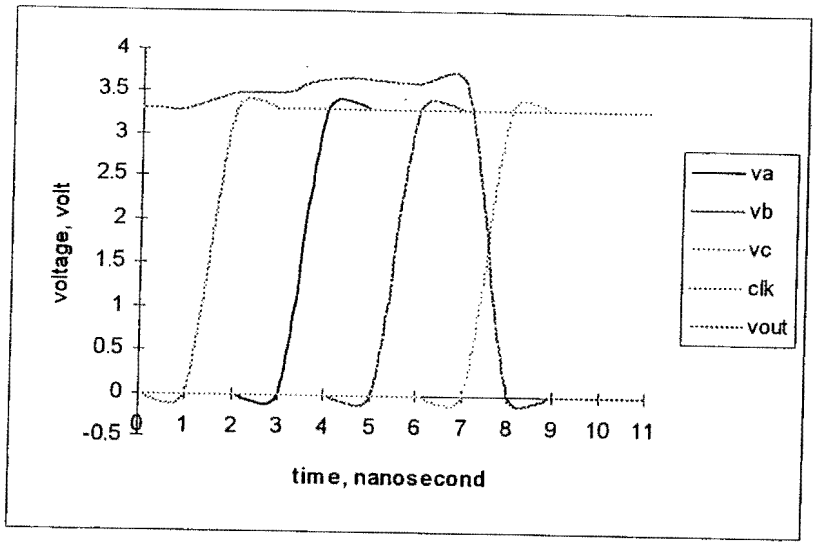


Figure 67 The normal operation of the dynamic 3-input NAND gate

5.3.1.1 The Effect of Crosstalk at the Input Signal(s) of Dynamic gates

At first glance, the effect of the crosstalk looks to be similar to the previous examples with crosstalk coupled at either the input(s) or clock signal. The difference however, will be that if the crosstalk noise is coupled into one of the inputs of a dynamic gate, a lower level of crosstalk will be required to make the logic gate fully switch. This is due to the fact that, unlike a typical CMOS logic gate, the pull-up device is only connected to the clock signal. Thus if the signal affected is not the clock it is ensured that, during the evaluation phase, the pull-up transistor is completely cut off and hence less strength is required in the pull-down transistors to switch the output from high to low. According to simulations for a 3.3 V supply voltage, crosstalk with amplitude of about 1 volt is enough for the gate to recognise the input as a full logic high and subsequently fully switch the output. Their value actually accounts for only 30% of the supply voltage- significantly less than the 45% requirement in typical CMOS gates. A crosstalk of 1-volt amplitude is perfectly possible as discussed in the previous chapter and the figure below shows a sample of simulation results. Here a dynamic 3-input NAND gate is switching to low as one of the inputs is crosstalk coupled, the other two inputs stay high.

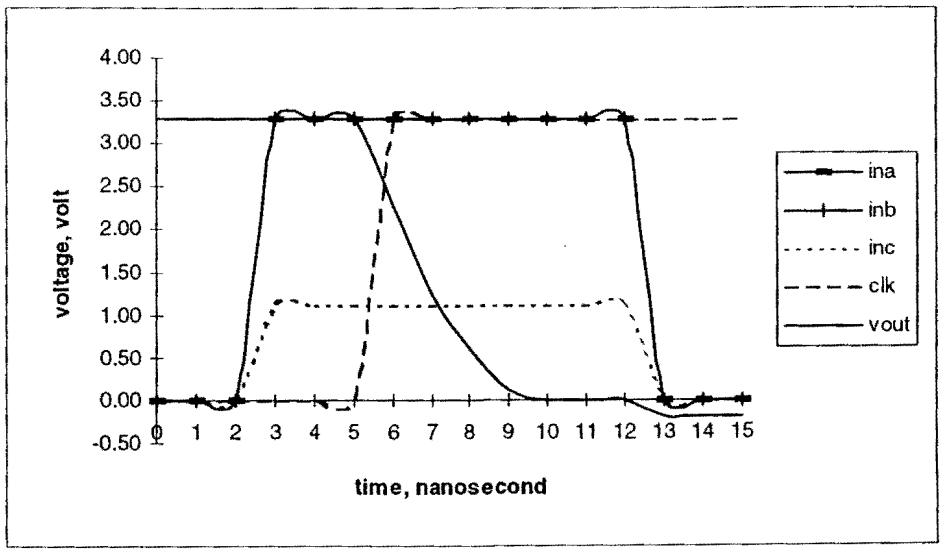


Figure 68 Crosstalk fault in dynamic 3-input NAND circuit

To compare the results for the 3-input NAND gate with other dynamic circuits, further simulations have been carried out mainly on NOR and NAND gates with different fan-in. The results reveal similar outcomes that approximately the same level of the crosstalk (30%) is required for faults to occur, with the type of dynamic circuits or the number of inputs not having a significant effect on the outcome. Figure 69 shows the crosstalk fault in the dynamic 3-input NOR gate

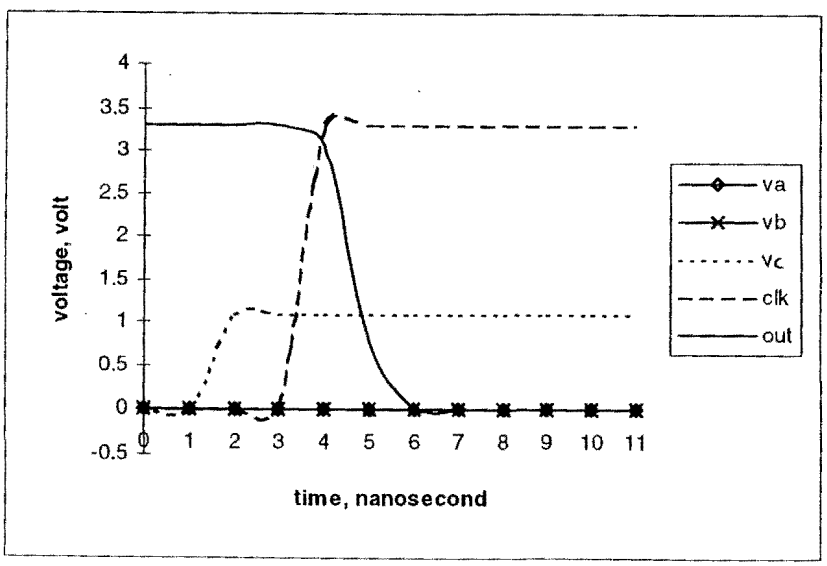


Figure 69 Crosstalk fault in the dynamic 3-input NOR gate

5.3.1.2 The Effect of Crosstalk at the Clock Signal

The second situation which needs to be considered regarding crosstalk in dynamic circuits is when the fault signal is coupled not to the input signal(s) but instead to the clock signal. It can be seen from Figure 66 that the clock signal is the signal which controls the state of the circuit. Having an incorrect clock signal could lead to a potential disastrous situation of incorrect precharging or evaluation the circuit at the wrong time. It is necessary to separate the analysis form the case of having crosstalk at the input(s) as discussed in the last section because, unlike this situation where the coupled signal affects only the pull-down transistors, here the crosstalk will affect both the pull-up and pull-down devices as both are connected to the clock signal.

Effectively, The situation can be said to be similar to that of the CMOS inverter discussed in section 4.1. During the precharging state the clock signal is low. If crosstalk occurs there, the amount of the crosstalk required to turn off the p-channel transistor and to turn on the n-channel transistor connected to the clock signal in order to have the fault switching will be similar to that of the inverter buffer. The situation is reversed for the crosstalk in the evaluation state. Because of the similarity between the clocking inputs and the inverter buffer, the amount of crosstalk required would be the same, which is approximately 45% of the supply voltage under normal circumstances. Simulation results exactly confirm the prediction. Figure 70 shows an example of crosstalk in the clock input, with the amplitude of the noise at 1.5 V. Here all the transistors are sized for equal rise and fall time. Similar to the CMOS inverter case, difference in the sizes of the transistors driven by the clock signal can result in the circuit being more or less prone to the crosstalk. Here a large PMOS transistor can make the circuit more vulnerable to crosstalk in the evaluation state while a large NMOS can make to circuit more sensitive to noise during the precharging period.

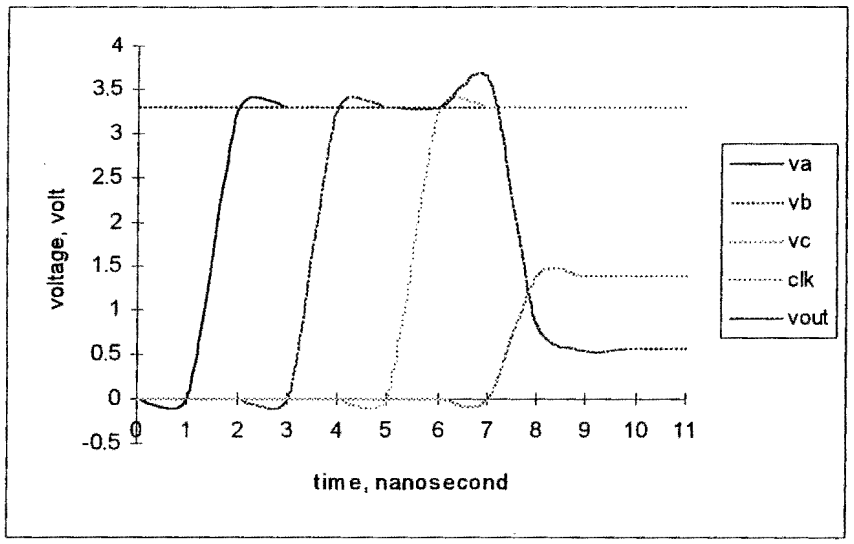


Figure 70 Crosstalk at clock signal in dynamic circuit

5.3.2 Charge Sharing in Dynamic Circuits

Not only are dynamic circuits potentially more prone to crosstalk faults as discussed in the previous section but they have another problem of charge sharing which could result in the circuit being even more susceptible to crosstalk fault. The problem of charge sharing arises because of capacitive potential divides that arise in the circuits in various states. The problem is best illustrated as shown in the figure 71.

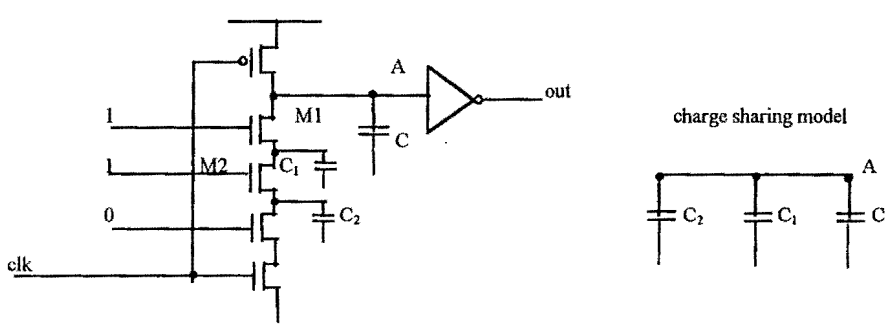


Figure 71 Charge sharing in dynamic CMOS logic

It can be seen from the figure that additional capacitors C_1 and C_2 are introduced to the circuit during the operation of the gate. Ideally, if the inputs are as shown in the

figure, in the evaluation state the voltage at node A will remain at V_{DD}. The presence of the parasitic capacitors C_1 and C_2, however, will result in a charge sharing situation where under charge conservation principle it can be written that:

$$CV_{DD} = (C + C_1 + C_2)V_A \tag{4-4}$$

and hence the voltage at node A can be found as:

$$V_A = \frac{C}{C + C_1 + C_2} V_{DD} \tag{4-5}$$

This can occur if transistors M1 and M2 are off during the pre-charge phase but switched on during the evaluate phase. It can be seen from the equation that if C_1 and C_2 have the values comparable to that of C the voltage at node A can be seriously affected. For example if C_1=C_2=0.5C then V_A would be $0.5V_{DD}$. This value can easily switch the inverter connected to node A and as a result the output will be in an incorrect state. The combined effect of this charge sharing phenomenon and the crosstalk coupled to an input can be that for any coupled input signal above the threshold voltage of the transistor, not only the pull-down transistor would be turned on but the parasitic capacitance at the drain of transistor would also come in to effect. Thus the circuit can be said to be even more prone to error. For example in the dynamic 3-input NAND gate it may only require one input to be correct and another one being noise coupled to successfully switch the output instead of 2 correct inputs and one coupled as seen previously. The effect is illustrated in Figure 72.

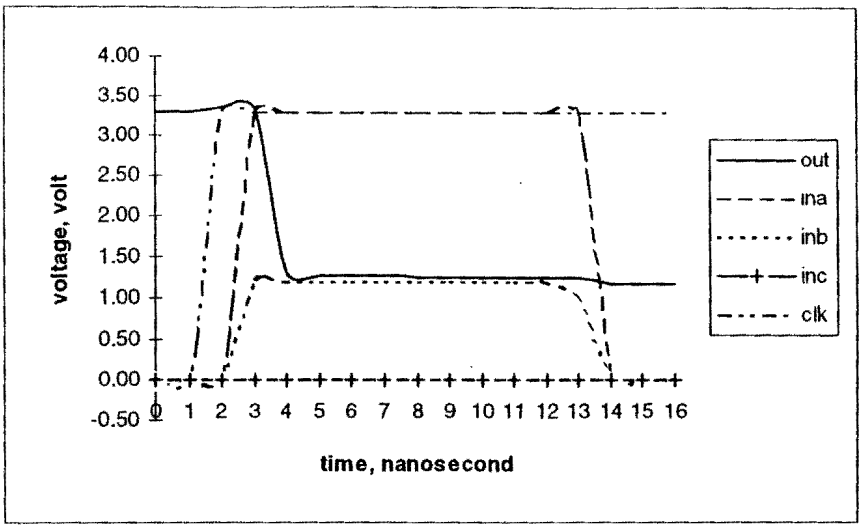


Figure 72 Charge sharing fault in dynamic CMOS NAND gate

5.4 Fault Efects in Other Circuits

Between the buffer, static and dynamic circuits, most of the conventional CMOS circuits are covered. These are however a few other types of circuits which operate differently and are worth mention here. The first type is the pseudo-nMOS circuit. As the name suggests the circuits use CMOS technology to realise an equivalent nMOS circuit. This is done by replacing the depletion-mode NMOS pull-up transistor with a PMOS transistor whose gate input is permanently connected to ground. The approach is illustrated by the three-input NAND gate shown in Figure 73.

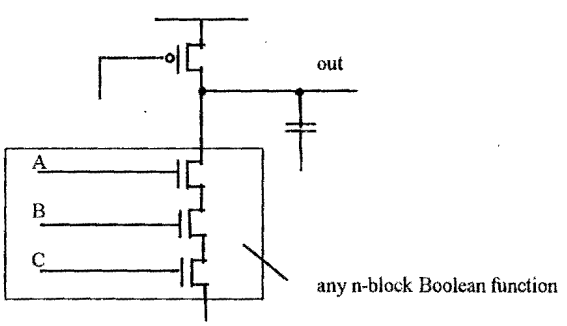
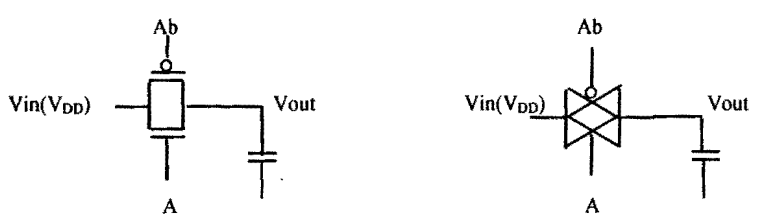


Figure 73 Three input pseudo-nMOS NAND gate

The advantage of using this approach is that it significantly reduces the number of transistors required as only one pull-up device is used. The drawback, however, will be that it would consume more power as the pull-up is always turned on and larger size nMOS transistors are required. The sizing of the transistors is a very important issue here because, unlike the typical CMOS logic case where sizing is mainly for the control of speed, pseudo nMOS logic gates need sufficiently large pull-down devices to successfully switch the output to logic 0. This aspect can be decisive when considering the problem of crosstalk, as has been shown earlier that large pull down devices can lower the amount of crosstalk required to cause a logic fault. Thus in pseudo-nMOS circuit where it is common to have large NMOS transistors it is therefore more likely transistors will arise which are less tolerant to faulty coupled inputs.

A further type of circuits which should be mentioned is Pass Transistor Logic. Pass transistor logic circuits are becoming more and more popular as power consumption becomes a problem in CMOS circuits. Figure 74 shows a CMOS transmission gate(TG) and its circuit characteristics as a primitive element of the conventional CMOS pass transistor logic. The circuit consists of two transistors forming a switch where the signal at the input will be transferred to the output if the controlling signal A connected to the nMOS gate is high (and its complementary Ab is low). Single nMOS or pMOS transistor can also be used to form the gate but in both cases the output logic swing is reduced by the threshold voltage.



a) transmission gate b) symbol

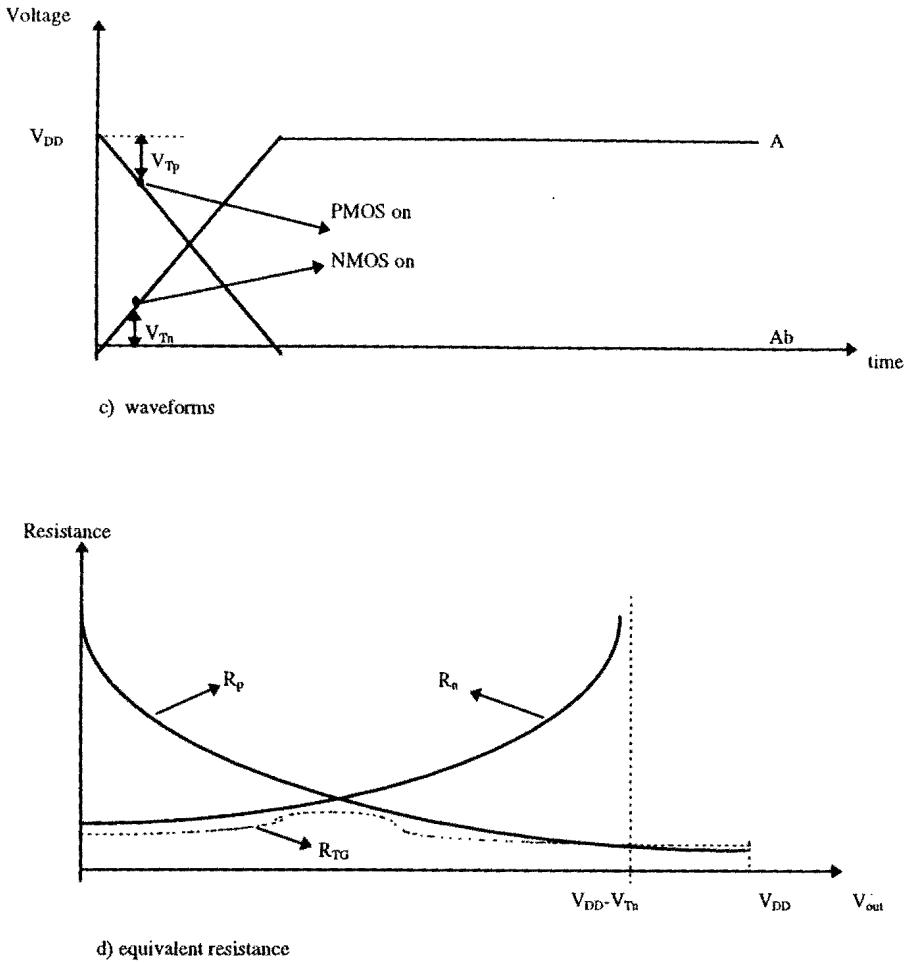


Figure 74 Transmission gate (TG)

It can be seen from the figure that the transmission gate offers full and fast logic switching due to its relatively low resistance. If the input is at logic 1 (Vdd), in order for the output to switch fully to logic 1 the enable signal A must have the value of the supply voltage. If the signal A is relatively small but large enough to turn the transistor on the output will not be zero but will have a small value of $V_A - V_t$. Thus, when considering the possible fault due to crosstalk, because of the fact that the coupled signal will be significantly less than the supply voltage, the resulting output would stay at a very low voltage and can not be interpreted as a high signal. For these reasons, the transmission gate, and hence the conventional pass transistor logic can be said to be very good in tolerating crosstalk noise. The arguments can also be applied to other types of pass transistor logics such as the complementary pass transistor logic (CPL).

CHAPTER 6 *Test Circuits and Structures for Crosstalk Measurements*

In the previous chapters, the behaviour of the crosstalk and its corresponding faults have been discussed in term of simulation results. Even though SPICE simulation is a very effective and reliable method of circuit analysis, its accuracy depends very much on the validity of the models used. It is possible that even though the circuits and the tracks are perceived to be correctly modelled according to the theory, there still exits some hidden factors which are not considered when deriving the models but could yet affect the results. It would therefore be a positive move to get fabricated some test circuits and then measure these to investigate whether the results are comparable to that simulated.

The methods used to measure the crosstalk in the sample circuits need some further consideration, the main question, however, will be: "What kind of circuits are best to allow necessary measurements of crosstalk under various configurations to be performed. It should be possible for input signals to the tracks to be easily adjusted, and the structures should provide a range of track configurations. The crosstalk generated should also be clearly detected by the probe. The latter problem arises because of the fact that crosstalk only happens as glitches and a probe, which has a relatively large capacitance, could easily remove any crosstalk it intends to read. Thus for this problem some buffering circuits may need to be introduced.

In the simplest form the measurements can be performed by having simple parallel tracks fabricated into a chip with their ends individually connected to external input sources and probes. In a system consisting of a large number of tracks this would involve a large number of inputs, all of which must be able to switch simultaneously as it is a precondition of many crosstalk faults. A large number of chips with different tracks would also be required if the physical effects of the tracks such as the length or separation are to be examined. For these reason special arrangement in the from of a test circuit are introduced to allow easier measurements.

6.1 A Proposed Circuit for Crosstalk Measurements

There are various ways in which crosstalk measurements can be made. The method used depends on the priority of such a test; which characteristics of the crosstalk are of interest, how large the test coverage is desired and what level of complexity of the additional circuits are tolerated. The test circuit suggested here is not the only solution or the most optimised, but rather a compromise between the simplicity of the structure, the test coverage and the ease of measuring.

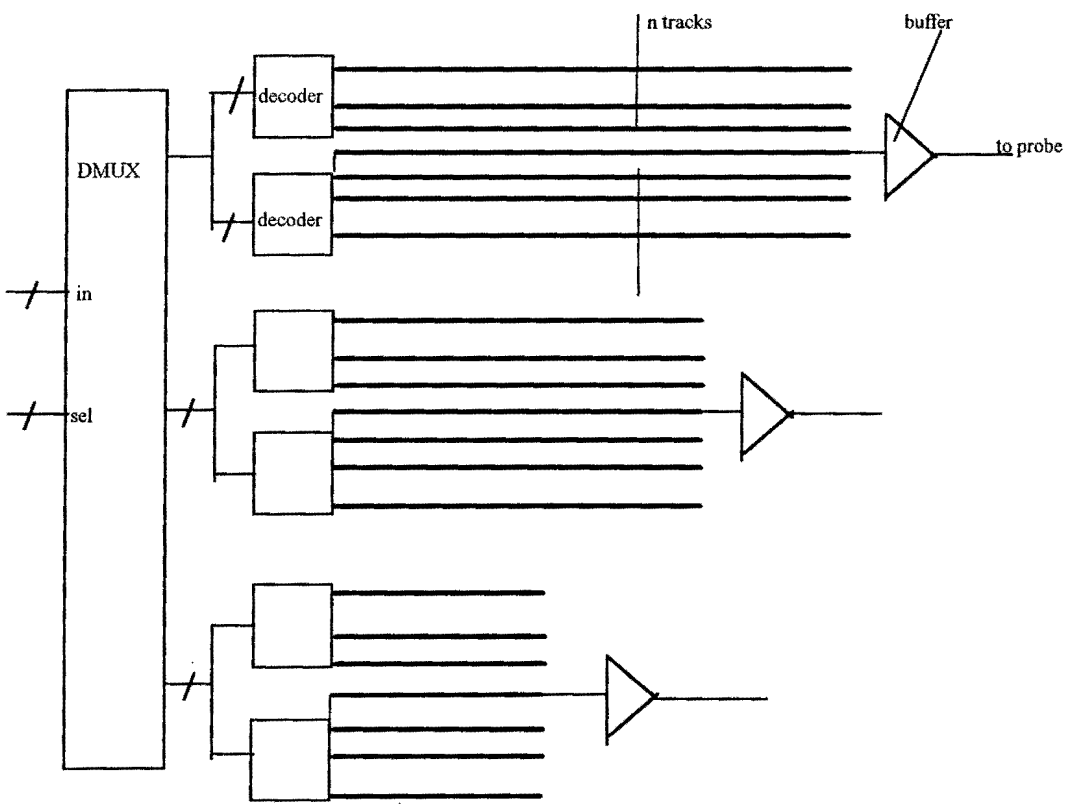


Figure 75 Test circuit for crosstalk measurement

Figure 75 shows the basic structure of the suggested test circuit. Apart from the tracks of various length three additional components are introduced, the demultiplexer, the decoders and the output buffers. The demultiplexer is used to select the group of

tracks to which the input signals will be directed. This is the simple procedure used to select the desired physical parameters of the tracks to be investigated. Shown here are groups of tracks with different length. In practise the difference can also be set to other parameters such as the separation. The decoders would then switch the selected tracks according to the inputs. This procedure is designed to reduce number of input signals required. This is, however, at the expense of only limited combinations of input signals allowed. Here the crosstalk is deliberately read form the middle track as potentially it is the track which is most affected by the crosstalk. At the end of the track the output buffer is placed before the resulting signal is read at the probe. The three main components are discussed in more detail in the following sections.

5.2 The Demultiplexer

The demultiplexer is used to select the group of tracks the inputs are to be connected to. The operation is controlled by the select signals. The test structure in the figure has 3 groups of tracks so requiring a 2-bit selecting signal. The demultiplexer can be realised using various techniques. Here the switching logic circuit is preferred due to its relative simplicity and low power consumption. The table showing operating characteristics of a one bit demultiplexer and its circuit diagram are shown below.

select1	select0	out3	out2	out1
0	0	0	0	0
0	1	0	0	in
1	0	0	in	0
1	1	in	0	0

Table 11 Demultiplexer truth table

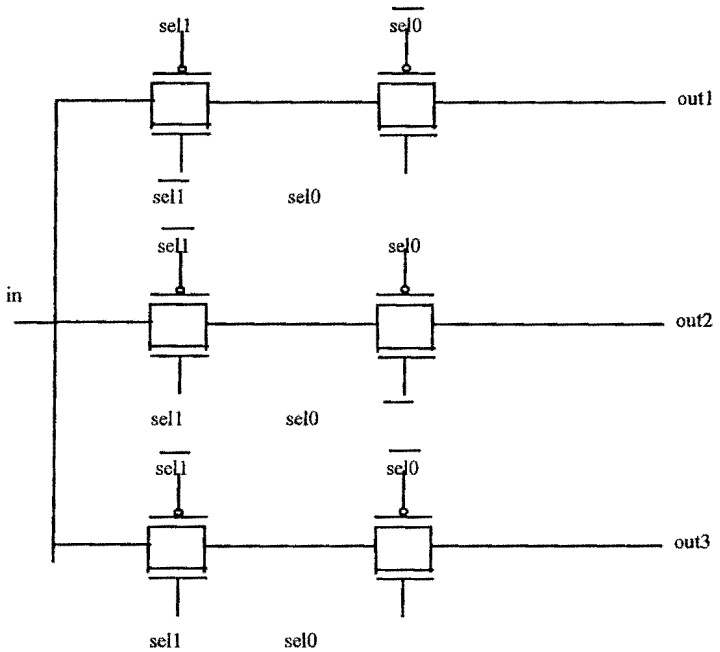


Figure 76 Demultiplexer

The operation of the demultiplexer is quite straight forward. Complementary pass transistor technique is used here to realise the switches which are controlled by the selecting signals sel0 and sel1. The signal 'in' will be passed to one of the outputs whose NMOS transistors in the line are all connected to the selecting signals which are high. For this 3-ouput demultiplxer only 12 transistors are required which is very effective. In addition to the circuit diagram above, the equivalent stick diagram of the demultiplexer is shown in figure 77. The stick diagram is a useful step in turning circuit into real mask layout which is necessary for any circuit to be fabricated into a chip. It offers a very structured and area optimised yet visibly clear way of designing a layout. The task of turning the stick into real mask layout in then carried by a CAD compiler. In this test circuit, three set of input signals are required, as discussed in the following section. Thus three of demultiplexer circuits are required, one for each set of inputs.

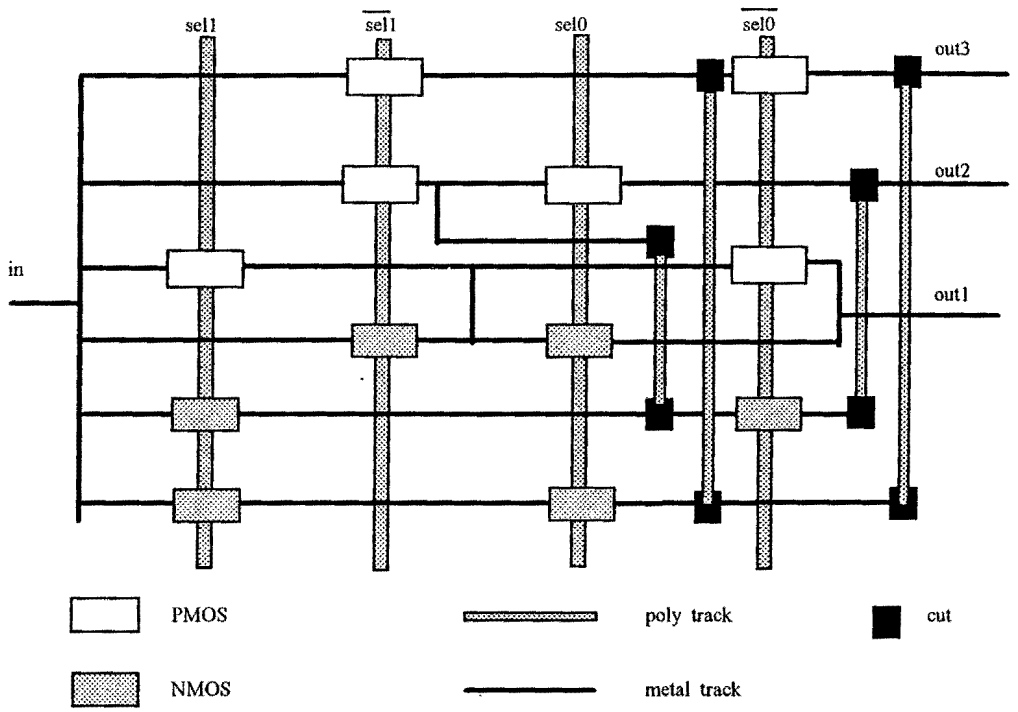


Figure 77 Stick diagram of the 3-output demultiplexer

6.3 The Decoder

The second component introduced is the decoder. The decoder is used because it is undesirable to assign one input signal for each track since that would require a large number of external inputs. An n-input decoder can produce 2^n output signal combinations which, if used carefully, could significantly reduce the number of the input signal required while still covering the necessary combination of signal to the tracks. Here 3-input decoders are used providing eight output signals which is adequate while keeping the number of input signals reasonably low. The truth table of the decoder chosen is as shown in Table 12. Here A,B and C are the input signals while lines1-7 are the seven output signals.

A	B	C	line7	line6	line5	line4	line3	line2	line1
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	1
0	1	1	0	0	0	0	1	1	1
1	0	0	0	0	0	1	1	1	1
1	0	1	0	0	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
logic			A.B.C	A.B	A.(B+C)	A	A+B.C	A+B	A+B+C

Table 12 Decoder truth table

It can be seen from the table that the decoder is used here only as means of controlling the number of switching lines. The intention is that since it has been shown in the simulation part mainly the behaviour of the crosstalk against the number of switching lines it is therefore a good idea to keep the same switching arrangement for the measuring part as well so that direct comparisons can be made. As can be seen from the figure 75, for each group of tracks, 2 decoders are used with the crosstalk being measured from the non-switching line in the middle. The 2 decoders are actually the complement of each other so that if C is selected, for example, the 2 signalling lines next to the middle line will be switched. The number of the switching lines will symmetrically increase from the inner to the outer tracks in both directions as the combination of inputs changes. Under this method only 3 input signals are required to address 14 tracks, significantly reduce the 14-input requirement for the direct method. This method, obviously is at the expense of only certain combinations of input being possible. The input signals can be more arbitrary by changing the coding of the decoder if desired but the number of outputs will also be reduced. It is suggested here that 15 tracks should prove to be reasonable number for the crosstalk measurement and under this test structure 45 metal tracks will be fabricated into single chip.

Realisation of these decoders is quite straight forward. Equivalent combinational logic for each of the track is given as shown in the table 12. Implementation of these circuits can be easily done using standard CMOS techniques. The resulting layout obtained by the Chipwise CAD programme is given in figure 81.

6.4 The output buffer

The last component is the buffering circuit. As has been stated earlier the buffer circuit is needed to prevent the direct contact between the track of interest and the probe which can have a large capacitance. One of the simplest solutions is to use an operational amplifier as the buffer. Chosen here is a simple 2-stage CMOS amplifier which has a performance that is well above the requirements of being a buffer while requiring only 8 transistors. The symbolic and circuit diagrams are shown in figure 78, together with sample simulations. It is not necessary that the op-amp should provide voltage gain so a unity feedback is connected between its input and output. Using here is the inverting configuration.

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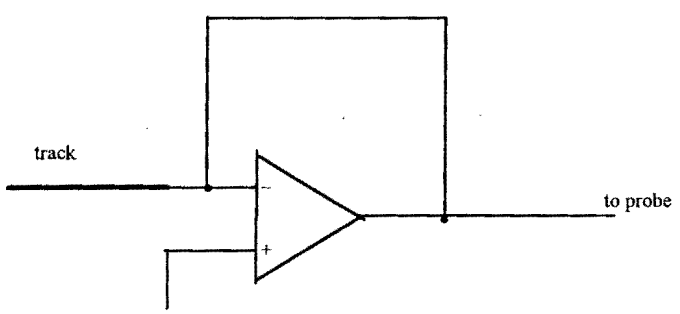
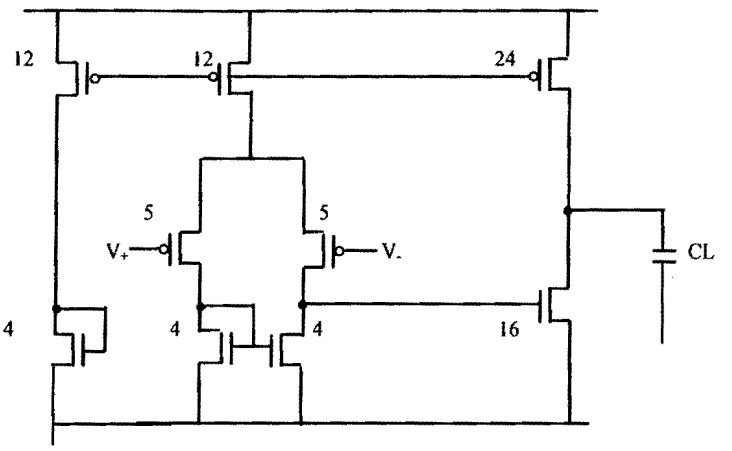
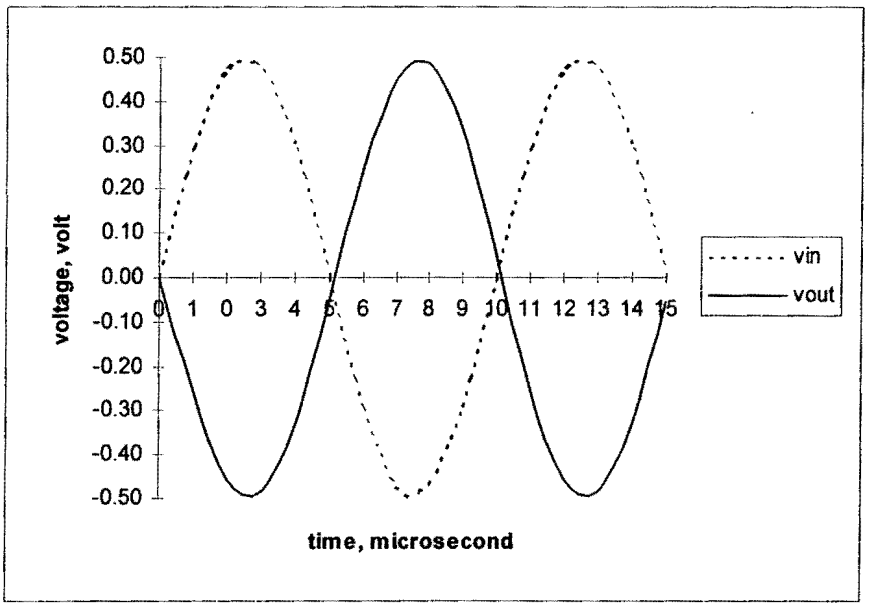


a) 2-stage op-amp symbolic diagram



b) Circuit diagram



c) Desired circuit response

Figure 78 Two stage CMOS buffer

In total, three amplifiers will be required for a single test chip. The following figure shows the simulated sample waveforms of the final test structure. According to the results, the test structure looks to be performing as expected.

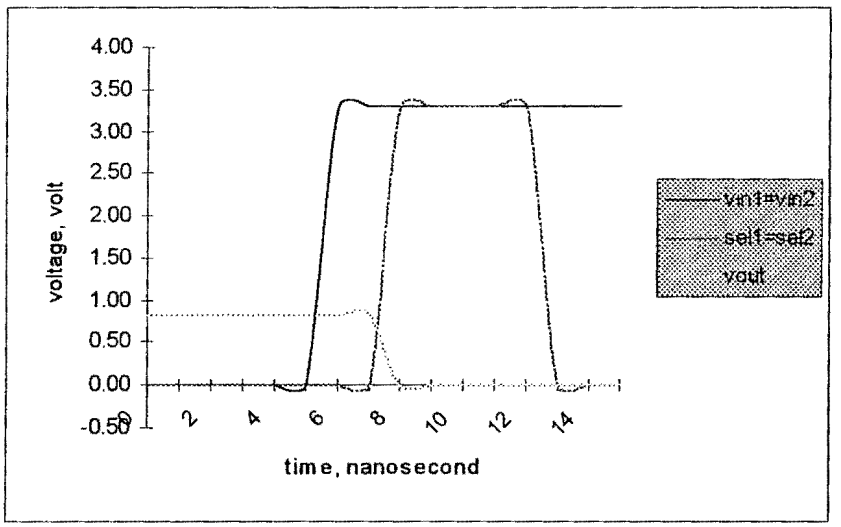


Figure 79 Sample operation of the test structure

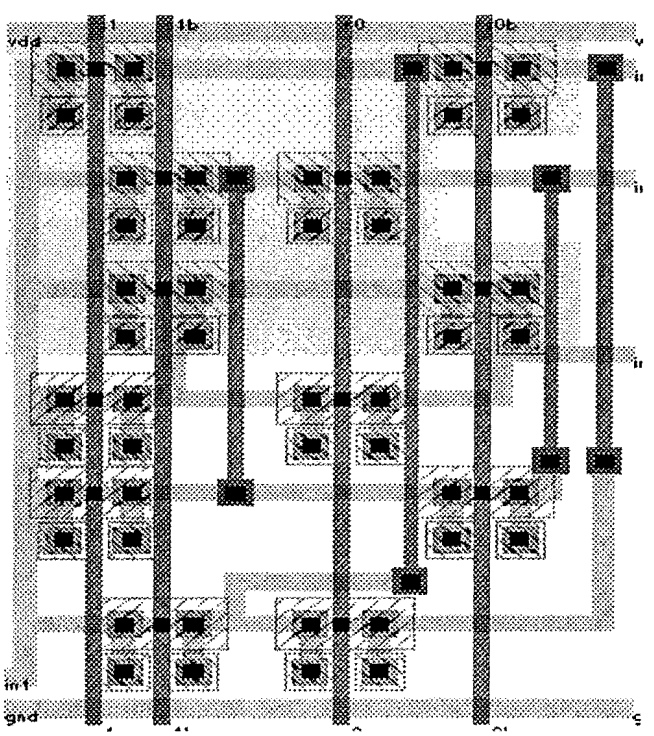


Figure 80 Demultiplexer layout

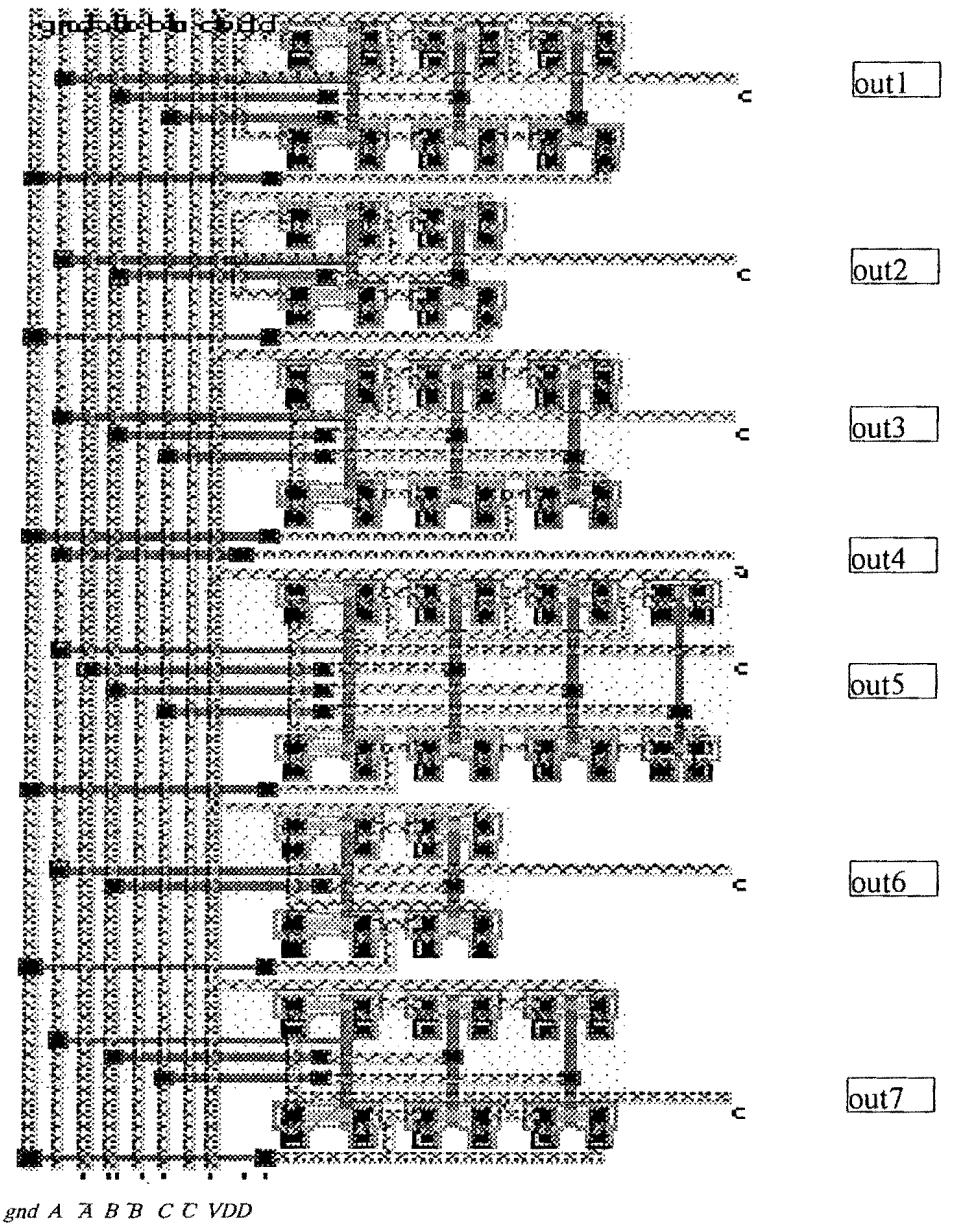


Figure 81 Decoder layout

6.5 Possible variations of the proposed circuit

For the proposed configuration seen in the earlier sections, the aim was to investigate the variation of crosstalk in the middle track as the number of switching signals increase and to measure the resulting crosstalk under the track with different length, all under worst-case configuration. Even though this arrangement provides a

reasonable test coverage while keeping the structure simple, it does not cover all the parameters which can have an effect on the resulting crosstalk as seen in the simulations. It would be very useful if the effect of the crosstalk under different values of those parameters, such as the width of the track, for example, can be investigated. To overcome that problem, it is suggested that the test circuit could be adjusted in various ways so that other useful measurements can be carried and the simulation results can be verified. While the previously proposed circuit can still be used as a primary test configuration, further adjustments can be made to the circuit, mainly within 3 parts of the circuit, so that the influence of any parameter of interest on the crosstalk can be investigated. Those three parts are:

- The physical parameters of the tracks
- The controlling circuits
- The output circuits.

6.5.1 Adjusting the Physical Parameters of the Tracks

In chapter 3, the effects of different track parameters on the crosstalk have been discussed. From the discussions the worst-case configuration for the physical parameters of the tracks have been proposed. Under the configuration the vertical parameters of the track such as the thickness are kept at the values defined by the process while the width and track separation parameters are kept at their minimum values. The track parameters under this worst-case situation are used in the test circuit previously suggested mainly because the crosstalk will have its maximum value under this arrangement and so its variation due to other parameters such as the number of the switching inputs can be easily read. If, however, the priority is to investigate the changes of the crosstalk under different track parameters, the proposed test circuit could still be used, with some adjustments.

It can be seen from the figure 75 that the tracks are divided into 3 groups, with identical set of controlling circuits assigned for each group. In the proposed circuit the tracks are all identical except that different values of track length are assigned for each group of the track. This is in effect an arrangement to study the effect of the length of the

track on the crosstalk as when reading the crosstalk from the probes the only parameter which is different will be the length of the track. Similarly , therefore, for any other physical parameters to be investigated, this can be done by assigning the different value of that parameter between the groups. For example, if it is desired to investigate the effect of having different separation on the crosstalk, different values of separation may then be assigned to tracks in different groups. For example the tracks in group one may all be separated by 0.4 μm while those in group two and three are separated by 0.6 and 0.8 μm respectively. The argument is also valid for the width and the length of the track while having different values of any of the vertical parameters deposited on the substrate can not be achieved without modeification of the process.

6.5.2 Adjusting the Controlling Circuits

The second adjustment which can be introduced to the circuit is within the controlling circuit, or more precisely the decoders. In the proposed circuit the decoder is set in such a way because the intention is only to use it as a controlling circuit to control the number of the switching signals. The 3-bit input signal which represents the value of 0-7 is decoded to provide the number of the outputs which will be switched from 0-7 lines accordingly. Under this configuration the behaviour of the crosstalk as the number of the switching lines increases can be investigated. The decoder is used here to reduce the number of inputs. This is however, at the expense of limited combinations of the switching signals allowed.

If, however, the aim of the investigation is to observe the variations of the crosstalk under various combinations of the switching signals as seen in the simulations, the decoder can be adjusted accordingly. The 3-input decoders are used here so any of them can have any arbitrary 2^3 =8 combinations of the outputs which are directly connected to the tracks. With 2 decoders for each of the groups and here 3 groups of tracks is suggested, if the tracks are all similar the possible combinations of switching signal can be 8*8*3 =192 combinations. This should provide sufficient test cover range. Table 13 shows a sample of the alternative coding scheme for the decoder.

A	B	C	line7	line6	line5	line4	line3	line2	line1
0	0	0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	1	1	0
0	1	0	0	0	1	0	0	1	0
0	1	1	1	1	0	0	1	1	0
1	0	0	0	0	0	1	0	0	0
1	0	1	0	1	0	1	1	1	1
1	1	0	0	0	1	1	1	1	1
1	1	1	1	1	0	1	1	1	0
logic			B.C	C	$B.\overline{C}$	A	A.B+C	A+C	A.C

Table 13 A sample of an alternative coding scheme for the decoder

Additional to these possible decoder arrangements, further controlling circuits may also be introduced to the test circuit to make the measurements even simpler. For example, instead of having a 3-bit input signal to select the combinations of the switching tracks, a 3-bit counter with any desired sequence can be added before the demultiplexer so that now only one input signal is only required to generate a sequence of different switching signals.

6.5.3 Adjusting the Output Circuit

The last part of the test circuit which can be rearranged is the output circuit. In the proposed circuit the 2-stage CMOS amplifier with unity gain is suggested. It is purely used here as a buffer between the track and the input of the probe. As a result the actual characteristics of the crosstalk can be observed. The buffer is connected to the middle track as this is where the worst-case crosstalk occurs. In practice, however, the buffer can be connected to any of the track which are of interest. Furthermore, it is also possible to attempt to verify the fault effects of crosstalk defects as seen in chapter 5. In this case the buffer circuit will be replaced by any of the logic circuits discussed earlier; conventional , dynamic or pass transistor circuits. The probe is then connected to the output of the circuit to investigate whether faulty wrong switching of the circuit occurrs.

6.6 Summary

In this chapter a test circuit is proposed. The design is a compromise between the test coverage and the complexities of the design and operation. Under this arrangement the variation of the crosstalk against the number of the switching tracks and the changing of one physical parameter of the track can be investigated. The actual characteristics of the crosstalk can then be observed through the probe with the help of a CMOS buffer. Adjustments can be made to various parts of the circuit if other relationships between any other circuit and track parameters and the crosstalk are to be studied. The physical parameters of the track can be changed from the worse-case configuration used in the proposed design while the coding scheme of the decoders can also be adjusted to any arbitrary value. The output buffers can also be replaced by the actual logic circuits to investigate if, in practice, faults can be introduced by the crosstalk as seen in simulations.

CHAPTER 7 *Further Discussion and Conclusions*

7.1 Further Discussion

In addition to all the analysis discussed in the previous chapters, this section provides further discussion about some significant aspects of the results obtained through this work. It is also an intention for this section to provide some useful tables where various results can be directly compared and clearly represented so that they can be used as a quick reference for the reader.

VLSI Interconnects

The first group of results which should be further addressed here are those concerning the modelling of VLSI interconnects, i.e. the metal tracks. This is basically a procedure of representing the tracks as an RCL network. The following table compares the results obtained for the various techniques. The conclusion is that the the 3-stage π model is preferred.

Model	Comps	Complexity	Accuracy	Good for
The lumped C model	C	simplest	poor	rough cal, $R_S >> R_{line}$
The Lumped RC model	R, C	simple	adequate	rough cal
The distributed RC model	R,C	ave	good	high speed CMOS
- The π model	R, C	T> π>L	π>T>L	(3-stage π preferred)
- The T model	R, C			
- The L model	R, C			
The transmission model	R, C, L	most complex	best	very high speed GaAs

Table 14 Interconnect models

RCL Calculation

Once the type of the RCL network is decided, the next step is to extract the values of the equivalent R, C and L from the physical parameters of the tracks. Resistance extraction is straight forward and as the value of the inductance can be found from the capacitance, emphasis is given to the capacitance extraction. Table 15 summarises the advantages and disadvantages of the various methods discussed.

Method	Complexity	Accuracy	Special Characteristics
The parallel-plate C	simplest	poor	neglect the fringe C and C_m, no crosstalk
The Schwartz-chr	simple	acceptable	include fringeCbut still no $C_m$and crosstalk
The Lewis' Met	medium	adequate	provide crosstalk but need regular tracks
The numerical Met	complex	very good	computation extensive (FEM,BEM,PEEC)
The Matthaei's Met	quite complex	good	compromise between Complex&Accuracy

C_m = mutual (or coupling) capacitance

Table 15 Capacitance extracting methods

Crosstalk Characterisation

In chapter 3, the characteristics of the crosstalk have been discussed in terms of relationships between the crosstalk and various circuits parameters. Analysis of the crosstalk in a 2-line system is used to provide some basic understanding of the characteristics of the crosstalk before more complex configurations are introduced. The general effects of various circuit parameters on the crosstalk in a 2-line system are as summarised in the table 15.

In table 16, the relationships are given between the crosstalk and the capacitance, resistance or the width of the transistor. Alternatively general relationships between the crosstalk and the actual track parameters can also be stated The relationships are as shown in the table 17.

Configurations	Results
For ideal resistive sources	
Identical sources&lines	
$R_1=R_2$ increase	increase in crosstalk pulse width, crosstalk amplitude unchanged, slow down of the switching signal in 1
$C_1=C_2$ increase	increase in crosstalk pulse width, crosstalk amplitude reduced
C_m increases	crosstalk amplitude increases
$R_1 \neq R_2$, $C_1=C_2$	
R_1 increases	crosstalk amplitude decreases
R_2 increases	crosstalk amplitude increases
	** note that the ct width max when $R_1=R_2$, increase either R_1or R_2 will reduce the ct width*
$R_1 = R_2$, $C_1 \neq C_2$	
C_1 or C_2 increases	crosstalk ampluitude reduced but also the speed of the circuit
$R_1 \neq R_2$, $C_1 \neq C_2$	combine the above effects
For CMOS buffer sources	
W_1 increases	crosstalk amplitude increases
W_2 increases	crosstalk amplitude decreases
	** note that given the same ratio of W_1/W_2, small W_2 will result in a higher crosstalk*

1 = the switching line

2 = the coupling line

Table 16 Behaviours of the crosstalk in a 2-line system

Increasing parameter	Line capacitance	Coupling capacitance	Crosstalk
The width W	largest increased	third largest increased	second lagest decreased
The height H	largest reduced	second largest increased	largest increased
The thickness T	increased	largest increased	second lagest increased
The separation S	reduced	reduced	largest decreased

* the crosstalk does not seem to change as the length of the line increases, unless it is extremely long

Table 17 Influences of the track parameter on C, C_m and Ct

From the above tables, a general understanding of how the crosstalk changes given a change in any parameter can be formed. However, as a lot of parameters are involved a precise analysis can be hard to develope. In chapter 3 the worst-case analysis is discussed. Under worst-case analysis a lot of parameters are fixed so that simple relationships between the crosstalk and various other parameters which are specified by the designer, can be developed. If the amount of crosstalk under the worst-case configuration satisfies the designer, then the circuit can be said to be crosstalk tolerant.

Worst-case analysis for a 2-line system

In this configuration, all the track parameters are set at their minimum value as seen in table 8. Relationship is then found between the maximum crosstalk and the ratio of W_1/W_2 . Simple equations describing the such relationship for 0.7, 0.5 and 0.35μm technologies are then derived as shown below.

- for 0.7 μm technology:

$$Ct_{max} = -1.62(W_1/W_2)^2 + 46.92(W_1/W_2) + 123.57$$

- for 0.5μm technology:

$$Ct_{max} = -1.57(W_1/W_2)^2 + 44.09(W_1/W_2) + 119.71$$

- for 0.35 μm technology:

$$Ct_{max} = -1.44(W_1/W_2)^2 + 41.84(W_1/W_2) + 148.92$$

It should be noted that as the ratio W_1/W_2 gets bigger, the rate of increase in crosstalk starts to fall. Generally, for the same ratio, using smaller technology will result in higher crosstalk. The amount of the crosstalk produced in this 2-line system, however, is too small to stand any realistic chance of causing logic fault. For example for W_1/W_2 =80 in 0.7 μm technology, the crosstalk will only be around 0.5V. Smaller technology will give

a slightly higher value but still considered to be too small. (more detail can be found on chapters 3 and 4).

Worst-case analysis for a multiple-line system

Similar to the 2-line case, worst-case analysis is also possible for the multiple-line system. The interesting relationship is between the number of the switching lines and the amount of crosstalk. For this worst-case analysis the track parameters are kept at minimum values, the crosstalk is read from the middle track and the ratio between the switching and non-switching buffers is set at 25. The resulting equations are given below. Similar to the 2-line case, the rate of increase of the crosstalk falls as the number of switching lines gets bigger. For 20 switching lines in a 0.7μm technology the crosstalk is about 0.9V. Slightly higher values will be found for the smaller technologies. This level of crosstalk may be just possible to cause fault switching in certain type of circuits, as seen in chapter 4. Further to this, the introduction of additional layers could worsen the situation by significantly increase the amount of crosstalk, as discussed in chapter 3.

- for 0.7 μm technology:

$$Ct_{max} = -0.87n^4 + 2.91n^3 + 45.45n^2 + 35.17n + 4.69$$

-for 0.5 μm technology:

$$Ct_{max} = -0.05n^4 + 2.14n^3 - 37.8n^2 + 309.88n - 47.20$$

-for 0.35 μm technology:

$$Ct_{max} = -0.04n^4 + 1.75n^3 - 33.14n^2 + 291.03n - 59.65$$

where n is the number of switching lines

Fault effect of crosstalk

After studying the characteristics of the crosstalk, investigations have been carried to see if this crosstalk can cause faults to logic circuits. Table 18 summarises the results

Type of circuit	effects
Buffer circuits	The amount of the crosstalk required to cause a faulty output depends on the transition voltage of the buffer. This transition voltage can be adjusted by sizing the PMOS and NMOS transistor. In normal circumstances where equal rise and fall time is desired, crosstalk of around 45% of the supply voltage will be required to cause a faulty output.
Static circuits	The amount of the crosstalk required for both combinational and bistable circuits is similar to that of the buffer
Dynamic circuits	- if signal is coupled in the input the amount of crosstalk required can be significantly less, only 30% of the supply voltage - if signal is coupled to the clock signal, 45% will be required
Other Circuits	- for the pseudo-nMOS circuits, the amount of the crosstalk required is also high but under certain conditions fault switch may occur by smaller crosstalk. - the pass transistor logic seems to be very good in tolerating crosstalk fault

Table 18 Crosstalk effects on logic circuits

Test circuits

The proposed test circuit is a compromise between the complexities of layout and operation, and the test coverage. Adjustments can be made if the objects of the investigation are not covered by the test. Table 19 summarises the arrangement.

The test circuit	Behaviour of the crosstalk covered
The proposed test circuit	- crosstalk as the number of the switching lines increases - crosstalk against any one of the track parameters
By adjusting the track layout	- crosstalk against any of the track parameters
By adjusting controlling circuits	- crosstalk against any arbitrary combinations of the switching signals
By adjusting the output circuits	- CMOS op-amp is used to study the actual waveform of the crosstalk - the buffer can be replaced by any logic circuits discussed in chapter 4 to investigate the fault effects

Table 19 The test circuits for crosstalk measurements

7.2 Conclusions

This research work concentrates on the effects of crosstalk signals on the signalling buses in an integrated circuit. The aim is to investigate whether such noise could lead to real logic faults being introduced in IC systems. Crosstalk is an unwanted signal caused by coupling between neighbouring signal lines. The problem of crosstalk was rather insignificant in older integrated circuits but it must now be considered in the modern ICs due to the shrinking in technology which results in significantly larger amounts of the crosstalk being produced.

Rather than directly measuring from sample circuits, the methods used in this investigation involved analysis circuit simulation using SPICE. Computer simulation of electronics circuits is very effective technique for circuit design and analysis providing that accurate models are used. For the crosstalk analysis, 2 types of models are required. For any conventional circuit parts in the system, accurate models of the transistors are required. These models vary according to the technology. The second type of the model is for the physical tracks which form the buses themselves. Basically they can be represented in terms of an RCL network. There are a number of techniques which can be used to convert information about tracks in term of their physical parameters to the conventional RCL circuits with different complexity and accuracy. Here the 3-stage π networking technique is preferred together with Matthaei's method for capacitance and inductance extractions.

The characteristics of the crosstalk under these models has been thoroughly investigated. Mathematical analysis for the simple 2-line system was established in order to form a basic understanding before more complicated arrangements were studied. Simulation results confirmed the trend that the crosstalk gets more and more significant as CMOS technology gets smaller. Within the same technology 3 main factors determine the amount of crosstalk: i) how the input buffers are sized; ii) the physical arrangements of the tracks; and iii) the number of switching tracks involved. Differences in physical parameters

parameters of the tracks can lead to different levels of crosstalk. However, between these parameters, only the length and the width of each track and the separations between them can be determined by the designer, the rest are strictly given by the process. Minimum sizes of the width and separation lead to highest crosstalk while increasing in the length does not contribute much variation. The results also show higher level of crosstalk occur in higher metal layers due mainly to the reduced capacitance to substrate More significant effects, however, come from the sizing of the input buffers and the number of signal involved in generating the crosstalk. The crosstalk is at it maximum when the track concerned is in the middle track of a bus connected to a weak buffer while the other signal lines are switching. From this information, the worse-case analysis for the allowable sizing of buffers for an arbitrary crosstalk in the 2-line system and for arbitrary number of lines given certain crosstalk are derived for the 0.7, 0.5 and 0.35 μ CMOS technologies.

The knowledge gained about crosstalk from this initial study was then used to see if it could be the source for logic faults. The results show that for most conventional logic circuits, a crosstalk as large as about a half of the supply voltage is required if a fault is to occur. For the buffer circuits the level of crosstalk required depends very much on the transition voltage, which is in turn controlled by the sizing of its n and p MOS transistors forming the buffer. There are also non-conventional types of circuits such as the dynamic circuits which can be more prone to the crosstalk. On the other hand some can be little affected by such a signal. The examples of such circuits are the pass transistor ones. Non the less, it is fair to conclude that in general case if crosstalk can be kept to be no larger that 30% of the supply voltage the circuit can be said to be very reliable and virtually free from crosstalk fault.

The final part of the work is to provide the test circuit for the real waveforms to be measured as a way to verify the simulation results. The method suggest here is not the absolute answer but is one choice which compromises the needs of circuit simplicity, large test coverage and easiness for the measuring. Possible adjustments to the test circuit are also suggested. For all these efforts, it is a good idea if some ways of reduction of this crosstalk can be founded. Reduction of crosstalk is actually a large topic by its own right and needs to be separately worked on. There are many ways by

which reduction can be done. Certain rules can be used when laying out the circuits so that the chance of having a large crosstalk an be avoided or certain novel fault tolerance circuits may be used. These alternatives , however, have their own pros and cons. Few recent papers [37][38] are suggested here so that those interested can study them as a complement of this work.

Appendix A Circuit Models for transmission Lines

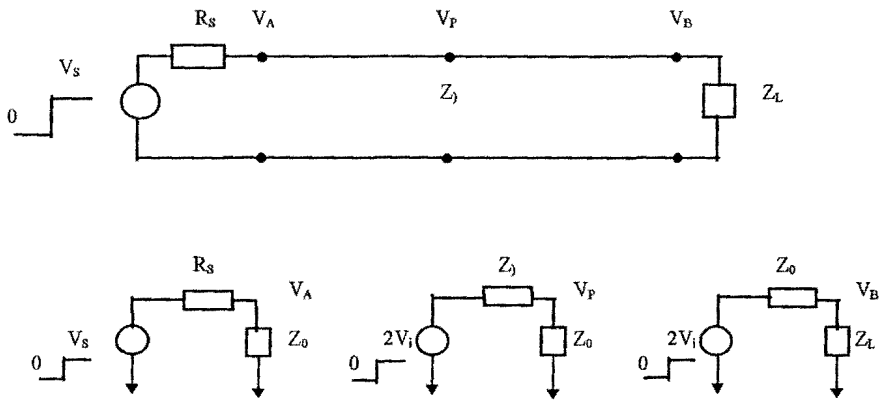


Figure A-1 Circuits models for transmission lines. The equivalent circuits at the source end, at an intermediate point along the line, and at the receiving end

According to the figure, simple network analysis can show that:

$$V_A = \frac{Z_0}{R_S + Z_0} V_S \qquad \text{(A-1)}$$

At the intermediate point the circuit is modelled as shown above. The Voltage step used is $2V_i$ rather than just V_i. Where V_i is the magnitude of the step travelling along the line. This is to take to the account of the reflections and to satisfy the continuity of current and voltage. The resulting V_P is then:

$$V_P = \frac{Z_0}{Z_0 + Z_0} 2V_i = V_i \qquad \text{(A-2)}$$

The equation above shows that the step will travel with no attenuation. In the same way for the wave travelling though different mediums with impedances changing from Z_1 to Z_2 , the voltage step transferring to second line V_t is given by:

$$V_t = \frac{Z_2}{Z_1 + Z_z} 2V_i \qquad \text{(A-3)}$$

And the reflected wave V_r is:

$$V_r = V_t - V_i \quad \text{(A-4)}$$

$$= \frac{Z_2 - Z_1}{Z_1 + Z_2} V_i \quad \text{(A-5)}$$

For the load end:

$$V_B = \frac{Z_L}{Z_0 + Z_L} 2V_i \quad \text{(A-6)}$$

$$V_r = \frac{Z_L - Z_0}{Z_0 + Z_L} V_i \quad \text{(A-7)}$$

According to these equations, if the receiving end is an open circuit ($Z_L = \infty$), then the incident voltage step doubles at the output ($V_B = 2V_i$, $V_r = V_i$) If the load impedance is less than Z_0, the polarity of the reflection is opposite of the incident wave and if the load impedance is the same as line impedance ($Z_L = Z_0$) then $V_B = V_i$ and $V_r = 0$.

Appendix B Mathematical analysis of the crosstalk in 2 parallel lines

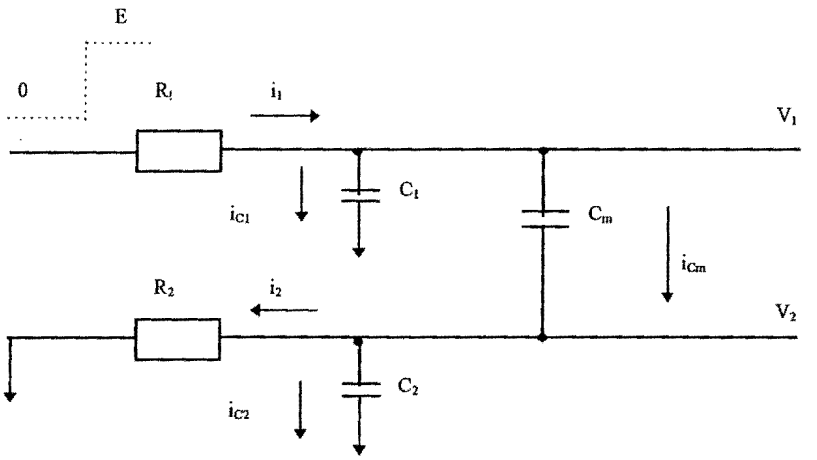


Figure A -2 2-parallel-line system

$$i_{R1} = i_{C1} + i_{Cm}$$

$$\frac{E - V_1}{R_1} = C_1 \frac{dV_1}{dVt} + C_m \frac{dV_m}{dt}$$

$$E - V_1 = R_1 C_1 \frac{dV_1}{dt} + R_1 C_m \frac{dV_1}{dt} - R_1 C_m \frac{dV_2}{dt}$$

$$E - V_1 = R_1 (C_1 + C_m) \frac{dV_1}{dt} + R_1 C_m \frac{dV_2}{dt} \qquad \text{(B-1)}$$

$$i_2 + i_{C2} = i_{Cm}$$

$$\frac{V_2}{R_2} + C_2 \frac{dV_2}{dt} = C_m \frac{dV_1}{dt} - C_m \frac{dV_2}{dt}$$

$$V_2 = -R_2 (C_2 + C_m) \frac{dV_2}{dt} + R_C C_m \frac{dV1}{dt} \qquad \text{(B-2)}$$

Rearranging B-1

$$V_1 = -R_1 (C_1 + C_m) \frac{dV_1}{dt} - R_1 C_m \frac{dV_2}{dt} + E$$

Given that

$$a = -R_1 (C_1 + C_m) \qquad c = R_2 (C_m)$$

$$b = -R_1 (C_m) \qquad d = -R_2 (C_2 + C_m)$$

And that

$$V_1 = x$$
$$V_2 = y$$

Then 1 and 3 can be rewritten respectively as:

$$x = a\frac{dx}{dt} + b\frac{dy}{dt} + E \quad \text{(B-3)}$$

$$y = d\frac{dy}{dt} + c\frac{dx}{dt} \quad \text{(B-4)}$$

If x and y are represented as

$$x = Ae^{et}$$
$$y = Be^{st}$$ Where A, B, s, t are arbitrary numbers.

And given

$$k = x - E$$

Then from B-3

$$Ae^{st} = (aAs + bBs)e^{st}$$
$$A(1 - as) = bBs \quad \text{(B-5)}$$

And from B-4

$$Be^{st} = (dBs + cAs)e^{st}$$
$$B(1 - ds) = cAs \quad \text{(B-6)}$$

(B-5)/(B-6) gives:

$$\frac{(1 - as)}{as} = \frac{bs}{(1 - as)}$$

$$s = \frac{-(a + d) \pm \sqrt{(a + d)^2 + 4(bc - ad)}}{2(bc - ad)} \quad \text{(B-7)}$$

For identical lines connecting to identical sources

Then $R_1 = R_2 = R$, $C_1 = C_2 = C$

Given $h = -R_1(C + C_m)$ and $j = RC_m$, then

$$a = -R_1(C_1 + C_m) = -R(C + C_m) = h \quad \text{(B-7.1)}$$
$$b = -R_1(C_m) = -RC_m = -j \quad \text{(B-7.2)}$$
$$c = R_2(C_m) = RC_m = j \quad \text{(B-7.3)}$$
$$d = R_2(C_2 + C_m) = -R(C + C_m) = h \quad \text{(B-7.4)}$$

Therefore

$$S = \frac{-2h \pm \sqrt{4h^2 + 4\left(j^2 - h^2\right)}}{2\left(j^2 - h^2\right)} = \frac{-h \pm j}{j^2 - h^2} \qquad \text{(B-8)}$$

Solving B -8 using B -7.1 -7.4 gives

$$S_1 = -\frac{1}{RC} \qquad S_2 = -\frac{1}{R\left(C + 2C_m\right)} \qquad \text{(B-8.1)}$$

Because the equations B - 3 and B -4 will have the answers in the forms of:

$$k = A_1 e^{S_1 t} + A_2 e^{S_2 t} \qquad k = x - E \quad , \quad x = V_1$$
$$y = B_1 e^{S_1 t} + B_2 e^{S_2 t} \qquad , \quad y = V_2 \qquad \text{(B-9)}$$

Rearranging B - 5 gives:

$$\frac{B}{A} = \frac{1}{bS} - \frac{a}{b} \qquad \text{(B-10)}$$

Solving B - 5 together with B - 8.1 gives:

$$\frac{B_1}{A_1} = -1 \qquad \text{(B-11)}$$

$$\frac{B_2}{A_2} = 1 \qquad \text{(B-12)}$$

At initial state, $t = 0$, $V_2 = 0 = y$, $V_1 = 0$, $k = -E$

Therefore from B - 9 :

$$k(0) = A_1 + A_2 = -E$$
$$\text{and} \quad y(0) = B_1 + B_2 = 0 \qquad \text{(B-13)}$$

Given that $B_2 = G$ for G = arbitrary value, then from B - 11 and B -12:

$$B_1 = -G \quad , \quad A_2 = G \qquad A_1 = G \qquad \text{(B-14)}$$

Putting back values of As in B -13 gives:

$$2G = -E \quad \text{or} \quad G = -\frac{E}{2} \qquad \text{(B-14.1)}$$

Hence, using results obtained in B - 8.1, 9, 14, 14.1, the final equations for signal in identical lines and sources are:

$$V_1 = V_{DD} - \frac{V_{DD}}{2}\left[e^{\frac{-t}{RC}} + e^{\frac{-t}{R\left(C+2C_m\right)}} \right]$$

$$V_2 = \frac{V_{DD}}{2}\left[e^{\frac{-t}{RC}} - e^{\frac{-t}{R(C+2C_m)}} \right] \qquad \text{(B-16)}$$

Maximum crosstalk will then occur when $\frac{dV_2}{dt} = 0$, solving B -16 shows that that would be when:

$$t = \frac{1}{(S_2 - S_1)} \ln\left(\frac{S_1}{S_2}\right) \qquad \text{(B-16.1)}$$

For signal in 2 identical lines but connected to input sources with different resistances

Using similar methods, the final equations are:

$$V_1 = \left[\frac{-V_{DD}}{\left(\frac{1}{F_2} - \frac{1}{F_1}\right)} \right]\left[-\frac{1}{F_1} e^{S_1 t} + \frac{1}{F_2} e^{S_2 t} \right] + V_{DD} \qquad \text{(B-17.1)}$$

$$V_2 = \left[\frac{-V_{DD}}{\left(\frac{1}{F_2} - \frac{1}{F_1}\right)} \right]\left[-e^{S_1 t} + e^{S_2 t} \right] \qquad \text{(B-17.2)}$$

where $$S_1 = \frac{(C+C_m)(R_1+R_2) + \sqrt{(C+C_m)^2 (R_2 - R_1)^2 - 4R_1R_2C_m^2}}{-2R_1R_2\left(C_m^2 + (C+C_m)^2\right)} \qquad \text{(B-17.3)}$$

$$S_2 = \frac{(C+C_m)(R_1+R_2) - \sqrt{(C+C_m)^2 (R_2 - R_1)^2 - 4R_1R_2C_m^2}}{-2R_1R_2\left(C_m^2 + (C+C_m)^2\right)} \qquad \text{(B-17.4)}$$

$$F_1 = -\frac{1}{C_m}\left[\frac{1}{R_1 S_1} + (C+C_m) \right] \qquad \text{(B-17.5)}$$

$$F_2 = -\frac{1}{C_m}\left[\frac{1}{R_1 S_2} + (C+C_m) \right] \qquad \text{(B-17.6)}$$

and the maximum occurs when

$$t = \frac{1}{(S_2 - S_1)} \ln\left(\frac{S_1}{S_2}\right) \qquad \text{(B-17.7)}$$

For signal in 2 parallel line with different capacitances connected to sources with identical resistances

$$V_1 = \left[\frac{-V_{DD}}{\left(\frac{1}{F_2} - \frac{1}{F_1}\right)}\right]\left[-\frac{1}{F_1}e^{S_1 t} + \frac{1}{F_2}e^{S_2 t}\right] + V_{DD} \qquad \text{(B-18.1)}$$

$$V_2 = \left[\frac{-V_{DD}}{\left(\frac{1}{F_2} - \frac{1}{F_1}\right)}\right]\left[-e^{S_1 t} + e^{S_2 t}\right] \qquad \text{(B-18.2)}$$

where $$S_1 = \frac{(C_1+C_2+2C_m)R + \sqrt{(C+C_2+2C_m)^2 R^2 - 4R^2\left(C_1C_2 + C_1C_m + C_2C_m + 2C_m^2\right)}}{-2R^2\left(C_1C_2 + C_1C_m + C_2C_m + 2C_m^2\right)} \qquad \text{(B-18.3)}$$

$$S_2 = \frac{(C_1+C_2+2C_m)R - \sqrt{(C+C_2+2C_m)^2 R^2 - 4R^2\left(C_1C_2 + C_1C_m + C_2C_m + 2C_m^2\right)}}{-2R^2\left(C_1C_2 + C_1C_m + C_2C_m + 2C_m^2\right)} \qquad \text{(B-18.4)}$$

$$F_1 = -\frac{1}{C_m}\left[\frac{1}{R\,S_1} + (C_1 + C_m)\right] \qquad \text{(B-18.5)}$$

$$F_2 = -\frac{1}{C_m}\left[\frac{1}{R\,S_2} + (C_1 + C_m)\right] \qquad \text{(B-18.6)}$$

and the maximum occurs at V_2 when

$$t = \frac{1}{(S_2 - S_1)}\ln\left(\frac{S_1}{S_2}\right) \qquad \text{(B-18.7)}$$

For any arbitrary 2-parallel-line system

$$V_1 = \left[\frac{-V_{DD}}{\left(\frac{1}{F_2} - \frac{1}{F_1}\right)}\right]\left[-\frac{1}{F_1}e^{S_1 t} + \frac{1}{F_2}e^{S_2 t}\right] + V_{DD} \qquad \text{(B-19.1)}$$

$$V_2 = \left[\frac{-V_{DD}}{\left(\frac{1}{F_2} - \frac{1}{F_1}\right)}\right]\left[-e^{S_1 t} + e^{S_2 t}\right] \tag{B-19.2}$$

$$S_1 = \frac{R_1C_1 + R_2C_2 + C_m(R_1 + R_2) + \sqrt{\left[R_1C_1 + R_2C_2 + C_m(R_1 + R_2)\right]^2 - 4\left[R_1R_2C_m^2 + R_1R_2(C_1 + C_m)(C_2 + C_m)\right]}}{-2R_1R_2C_m^2 - 2R_1R_2(C_1 + C_m)(C_2 + C_m)} \tag{B-19.3}$$

$$S_2 = \frac{R_1C_1 + R_2C_2 + C_m(R_1 + R_2) - \sqrt{\left[R_1C_1 + R_2C_2 + C_m(R_1 + R_2)\right]^2 - 4\left[R_1R_2C_m^2 + R_1R_2(C_1 + C_m)(C_2 + C_m)\right]}}{-2R_1R_2C_m^2 - 2R_1R_2(C_1 + C_m)(C_2 + C_m)} \tag{B-19.4}$$

$$F_1 = -\frac{1}{C_m}\left[\frac{1}{R_1 S_1} + (C_1 + C_m)\right] \tag{B-19.5}$$

$$F_2 = -\frac{1}{C_m}\left[\frac{1}{R_1 S_2} + (C_1 + C_m)\right] \tag{B-19.6}$$

and the maximum in V_2 occurs when

$$t = \frac{1}{(S_2 - S_1)} \ln\left(\frac{S_1}{S_2}\right) \tag{B-19.7}$$

Appendix C MATLAB functions

% units used %
% capacitance - picofarad , resulting crosstalk - millivolt %
% resistance - kilo ohm , time - nanosecond %
% supply voltage - volt %

For identical lines connecting to identical sources

% crosstalk in time domain %
% a = sct(supply voltage, resistance, self capacitance, mutual capacitance, time) %

```
function a = sct(v,r,c,m,t)
s =(-1)./(r.*c)
j = (-1)./(r.*(c+2.*m))
f = -1
h = 1
a =(-1).*1000.*v.*(-1)./((1./h)-(1./f)).*((-1).*exp(s.*t)+exp(j.*t))
```

% maximum crosstalk%
% a = scm(supply voltage,self capacitance, mutual capacitance,) %

```
function a = scm(v,c,m)
s =(-1)./(c)
j = (-1)./(c+2.*m)
f = -1
h = 1
t = 1./(j-s).*log(s./j)
a =(-1).*1000.*v.*(-1)./((1./h)-(1./f)).*((-1).*exp(s.*t)+exp(j.*t))
```

For signal in 2 identical lines but connected to input sources with different resistances

% crosstalk in time domain %
% a = gcrt(supply voltage, R1, R2, self capacitance, mutual capacitance, time) %

```
function a = gcrt(v,r,b,c,m,t)
s =( (c + m).*(r+b)+ sqrt( ((c+m).^2).*((b-r).^2)-4.*r.*b.*(m).^2 )./((-2).*r.*b.*(((m).^2)
   +((c+m).^2)))
j =( (c + m).*(r+b) - sqrt( ((c+m).^2).*((b-r).^2)-4.*r.*b.*(m).^2 )./((-2).*r.*b.*(((m).^2)
  +((c+m).^2)))
f = ((-1)./m.*((1./r./s)+c+m))
h = ((-1)./m.*((1./r./j)+c+m))
a =1000.*v.*(-1)./((1./h)-(1./f)).*((-1).*exp(s.*t)+exp(j.*t))
```

% maximum crosstalk%
% a = gcrm(supply voltage,R1,R2,self capacitance, mutual capacitance,) %

```
function a = gcrm(v,r,b,c,m)
s =( (c + m).*(r+b)+ sqrt( ((c+m).^2).*((b-r).^2)-4.*r.*b.*(m).^2 )./((-2).*r.*b.*(((m).^2)
   +((c+m).^2)))
j =( (c + m).*(r+b) - sqrt( ((c+m).^2).*((b-r).^2)-4.*r.*b.*(m).^2 )./((-2).*r.*b.*(((m).^2)
          +((c+m).^2)))
f = ((-1)./m.*((1./r./s)+c+m))
h = ((-1)./m.*((1./r./j)+c+m))
```

```
t = 1./(j-s).*log(s./j)
a =1000.*v.*(-1)./((1./h)-(1./f)).*((-1).*exp(s.*t)+exp(j.*t))
```

For signal in 2-parallel-line with different capacitances connected to sources with identical resistances

% crosstalk in time domain %
% a = gcct(supply voltage, R, C1,C2, mutual capacitance, time) %

```
function a = gcct(v,r,c,f,m,t)
s =( r.*(c+f+2.*m)+sqrt( r.*r.*(c+f+2.*m).*(c+f+2.*m)-4.*r.*r.*(c.*f+c.*m+f.*m+2.*m.*m) )
   )./((-2).*r.*r.*(c.*f+c.*m+f.*m+2.*m.*m)  )
j = ( r.*(c+f+2.*m)-sqrt( r.*r.*(c+f+2.*m).*(c+f+2.*m)-4.*r.*r.*(c.*f+c.*m+f.*m+2.*m.*m) )
   )./((-2).*r.*r.*(c.*f+c.*m+f.*m+2.*m.*m)  )
f = ((-1)./m.*((1./r./s)+c+m))
h = ((-1)./m.*((1./r./j)+c+m))
a =1000.*v.*(-1)./((1./h)-(1./f)).*((-1).*exp(s.*t)+exp(j.*t))
```

% maximum crosstalk%
% a = gccm(supply voltage,C1,C2, mutual capacitance,) %

```
function a = gccm(v,c,f,m)
s=((c+f+2.*m)+sqrt((c+f+2.*m).*(c+f+2.*m)4.*(c.*f+c.*m+f.*m+2.*m.*m))).//((2).*(c.*f+c.*
m+   f.*m+2.*m.*m)  )
j=((c+f+2.*m)sqrt((c+f+2.*m).*(c+f+2.*m)4.*(c.*f+c.*m+f.*m+2.*m.*m))).//((2).*(c.*f+c.*m+
f.   *m+2.*m.*m)  )
f = ((-1)./m.*((1./s)+c+m))
h = ((-1)./m.*((1./j)+c+m))
t = 1./(j-s).*log(s./j)
a =1000.*v.*(-1)./((1./h)-(1./f)).*((-1).*exp(s.*t)+exp(j.*t))
```

For any arbitrary 2-parallel-line system

% crosstalk in time domain %
% a = gcrct(supply voltage, R1, R2, C1,C2, mutual capacitance, time) %

```
function a = gcrct(v,r,b,c,f,m,t)
s=((r.*c+b.*f+m.*r+m.*b)+sqrt(((r.*c+b.*f+m.*r+m.*b).^2)-4.*r.*b.*(m.^2)-
   4.*r.*b.*(c+m).*(f+m))).//((-2).*r.*b.*(m.^2)-2.*r.*b.*(c+m).*(f+m))
j=((r.*c+b.*f+m.*r+m.*b)-sqrt(((r.*c+b.*f+m.*r+m.*b).^2)-4.*r.*b.*(m.^2)-
   4.*r.*b.*(c+m).*(f+m))).//((-2).*r.*b.*(m.^2)-2.*r.*b.*(c+m).*(f+m))
f = ((-1)./m.*((1./r./s)+c+m))
h = ((-1)./m.*((1./r./j)+c+m))
a =1000.*v.*(-1)./((1./h)-(1./f)).*((-1).*exp(s.*t)+exp(j.*t))
```

% maximum crosstalk%
% a = gcrcm(supply voltage,R1,R2,C1,C2, mutual capacitance,) %

```
function a = gcrcm(v,r,b,c,f,m)
s=((r.*c+b.*f+m.*r+m.*b)+sqrt(((r.*c+b.*f+m.*r+m.*b).^2)-4.*r.*b.*(m.^2)-
   4.*r.*b.*(c+m).*(f+m))).//((-2).*r.*b.*(m.^2)-2.*r.*b.*(c+m).*(f+m))
j=((r.*c+b.*f+m.*r+m.*b)-sqrt(((r.*c+b.*f+m.*r+m.*b).^2)-4.*r.*b.*(m.^2)-
   4.*r.*b.*(c+m).*(f+m))).//((-2).*r.*b.*(m.^2)-2.*r.*b.*(c+m).*(f+m))
f = ((-1)./m.*((1./r./s)+c+m))
h = ((-1)./m.*((1./r./j)+c+m))
t = 1./(j-s).*log(s./j)
```

```
a =1000.*v.*(-1)./((1./h)-(1./f)).*((-1).*exp(s.*t)+exp(j.*t))
```

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