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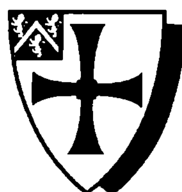
Organic Transistors based on Pentacene and Dibenzothiophene derivatives

by

Daniel Kolb, BA (Oxon) MSc (Lond)



Submitted in conformity with the requirements for the degree of Doctor of Philosophy
School of Engineering
University of Durham

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Abstract

Organic Transistors based on Pentacene and Dibenzothiophene derivatives

Daniel Kolb, BA (Oxon) MSc (Lond)

This thesis is concerned with the fabrication and characterisation of organic thin film transistors. Initially, pentacene thin films were investigated, with results comparable to those found in published literature. Initial studies of pentacene transistors revealed a poor hole mobility of 6.3×10^{-3} $cm^2/V/s$. Improvements in the fabrication process (using a more conductive silicon wafer as the gate, and treating the silicon oxide surface with a silanising agent) increased the mobility to around 0.1 $cm^2/V/s$. Better pentacene deposition conditions allowed a polycrystalline structure to form, with dendritic grains of the order of 2–3 µm in size. This increased the mobility of the transistor further, to 0.54 $cm^2/V/s$.

Treatment of the silicon oxide surface prior to pentacene deposition was found to affect significantly the hysteresis in the transfer characteristics. Removal of photoresist with acetone and propan-2-ol prior to pentacene deposition resulted in fairly large threshold voltages, with an average shift between the off-on and on-off threshold voltages of 9.7 V. Application of an oxygen plasma prior to deposition resulted in decreased threshold voltages, and a reduced threshold voltage shift of 3.8 V. The hysteresis was attributed to charge trapping on the oxide surface due to organic contamination; the oxygen plasma served to reduce this. X-Ray Photoelectron Spectroscopy measurements confirmed this — following a plasma treatment, the carbon content on the surface was reduced significantly. Incorporation of a layer of gold nanoparticles between the oxide and pentacene was found to provide charge traps — this might be exploited in memory devices.

Replacing the silicon oxide with PMMA produced favorable results. Negative threshold voltages with low hysteresis were observed for all the devices. Mobilities of up to 0.21 $cm^2/V/s$ were recorded for devices with a 124 nm PMMA layer; a thinner (80 nm) layer of PMMA resulted in reduced mobility, as did a thicker (350 nm) layer.

Replacing the silicon oxide with sputtered hafnium oxide produced devices with a large number of defects. Deposited pentacene did not form optimal crystal structures, and the output characteristics of a number of devices showed no significant variation with source-drain voltage. These output characteristics were therefore assumed to be the result of leakage through the oxide. The measured device that showed reasonable output characteristics was found to have a mobility of 0.59 $cm^2/V/s$, demonstrating that hafnium oxide could have good potential as a dielectric, if deposited in a manner not resulting in a leaky oxide.

Three dibenzothiophene-based molecules, synthesised in the University of Durham, were characterised and thin film transistors fabricated. 3,7-bis(dibenzothiophene-4-yl)-dibenzothiophene-*S*,*S*-dioxide exhibited the characteristics of an air-stable *n*-type device, with a mobility of 3.5×10^{-6} $cm^2/V/s$. A related molecule, 3,7-bis(4-(ethylsulfonyl)phenyl)dibenzo[*b*,*d*]thiophene, incorporating additional electron-deficient groups, did not exhibit any field-effect-modified behaviour. A third molecule, that did not contain electron-deficient groups, exhibited *p*-type behaviour, and transistors showed good output characteristics, but only possessed a mobility of 3.7×10^{-5} $cm^2/V/s$; the low mobility was attributed to the lack of long-range order in the structure of the deposited film.

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1 Introduction

Organic transistors are currently the subject of substantial international research, with many potential commercial applications. Compared to traditional silicon devices, they have low production costs; much of the processing can be performed at or near room temperature; and the techniques involved tend to be simpler than those for silicon.

Since the first postulation of organic conductors in 1911 [1] and particularly since they were first discovered in 1954 [2], research has progressed to the point where, today, organic devices are appearing in commercial products in increasing volume. Whilst organic transistors will never fully replace silicon due to speed issues, there are a multitude of applications, such as flexible displays, where their particular qualities far outweigh the speed benefits of silicon. The ability to fabricate organic transistors on flexible substrates allows for the fabrication of "paper" displays: the transistors are used as the driving circuitry for an organic LED display.

The aim of the research in this thesis is threefold. Firstly, to characterise pentacene and pentacene transistors fabricated on a silicon oxide dielectric, and to investigate the effect of various surface treatments of the SiO_2 on the transistors. Secondly, to compare the characteristics of pentacene-based transistors with different dielectrics to those made on SiO_2. Thirdly, to investigate the properties of some new materials, based on the dibenzothiophene moiety, synthesised in the Department of Chemistry in the University of Durham.

Chapter 2 gives an introduction to organic semiconductors, with a brief outline of how semiconducting behaviour arises in organic molecules. An overview of the materials used in research is provided, including some current research into new semiconducting molecules. Chapter 3 introduces thin films and their formation techniques: the techniques relevant to this work are described, and other formation techniques are summarised. Chapter 2 covers transistors, describing the operation of a field effect transistor and introducing organic thin film transistors. Dielectric surface treatments are briefly covered, and a summary of recent OTFT research is also provided.

Details of the experimental techniques used in this research are given in chapter 4. The methods used to fabricate the transistors are described, along with a discussion of the techniques used to characterise the devices and materials. Results for pentacene films and transistors made from pentacene on silicon oxide are given in chapter 5. The effects of the pentacene film morphology, and the effect of various silicon oxide surface treatments, on the characteristics and performance of the transistors are reported. Chapter 6 compares the characteristics of pentacene transistors on poly(methyl methacrylate) and hafnium oxide dielectrics, and hence provides a contrast between these dielectric materials and SiO_2. Chapter 7 focuses on the characterisation and FET performance of three new materials, all based on the dibenzothiophene moiety, which were synthesised at the University of Durham.

Chapter 8 offers conclusions drawn from the work reported, and provides some suggestions for further work.

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2

Organic Semiconductors and Transistors

2.1 Introduction

This chapter provides an introduction to organic semiconductors and transistors. Sections 2.2 and 2.2.1 summarise the electronic structure of atoms and bonding within organic compounds. Section 2.3 gives a brief introduction to inorganic semiconductors; section 2.4.2 provides the analogue for organic molecules. A short history and important research milestones of organic semiconductors are outlined in section 2.4.1. The operation of a metal-oxide-semiconductor field effect transistor (MOSFET) is given in section 2.5.1, the model yields the equation for source-drain currents in the linear and saturation regions. Section 2.5.2 compares the MOSFET to a thin film transistor, and introduces the grain boundary barrier model. A brief history of the organic thin film transistor is given in section 2.5.4.

The research in this thesis concentrates on the effect of surface treatments on silicon oxide / pentacene-based organic thin film transistors, the effect of replacing silicon oxide with alternative dielectrics, and the characterisation of some new materials. Surface treatments affecting OTFT performance are outlined in section 2.6. Sections 2.7.1 and 2.7.2 summarise some recent research in the fields of organic semiconducting materials and OTFTs, respectively.

Name	Symbol	Permitted values	Property
Principal	n	Positive integers (1, 2, 3, ...)	Orbital energy (size)
Angular momentum	l	Integers from 0 to $n-1$	Orbital shape
Magnetic	m_l	Integers from $-l$ to 0 to $+l$	Orbital orientation
Spin	m_s	$+\frac{1}{2}$ or $-\frac{1}{2}$	Direction of electron spin

Table 2.1: Summary of quantum numbers of electrons in atoms.

2.2 Electronic structure of atoms

During the latter part of the 19th century, it was found that many phenomena involving electrons in solids could not be explained in terms of classical mechanics. Quantum mechanics was thus developed to explain the observations. One of the early outcomes of quantum mechanics was the development of the Bohr atomic model, in which electrons were assumed to revolve around the atomic nucleus in discrete orbitals. An assumption in the Bohr model is that only certain orbits with fixed radii are stable around the nucleus [1]. The Bohr model was found to have significant limitations, and several improvements and enhancements were proposed. A significant improvement was regarding the electron as a charge contained within a spherical shell at a given radius, instead of a small finite particle moving around an orbit.

An electronic orbital, therefore, is a region of space in an atom or molecule where an electron with a given energy may be located. Due to the requirement of stable orbits, the electrons occupy well-defined spherical regions, distributed in various shells and subshells. In the quantum mechanical model, the shells and subshells are spatial regions around the nucleus where the electrons are most likely to be located. Each electron is characterised by a set of quantum numbers (principal, angular moment, magnetic and spin) which specify the size, shape and orientation of an electron's probability density function: the quantum numbers are summarised in table 2.1. The principal quantum number specifies the main shell where an electron is located, which gives the total energy of the electron. The angular momentum (orbital) number specifies the

magnitude of the orbital momentum; the l values 0, 1, 2, 3 indicate the electron subshell, corresponding to s, p, d, and f orbitals, respectively. The number of energy states for each subshell is determined by m_l: for an s subshell, there is a single energy state, whereas for p, d and f subshells there exist three, five and seven states. Each electron additionally has a spin direction, m_s, associated with it.

An atomic orbital is defined as a one-electron wavefunction $\psi(x, y, z, t)$. The corresponding probability distribution function $|\psi|^2$, defines the probability of finding an electron per unit volume at x, y, z and at time t. $|\psi|^2$ has wave-like properties: its amplitude can be positive, corresponding to a wave crest, or negative, corresponding to a wave trough; a node is formed when a crest and trough meet. In three-dimensional waves, the nodes are two-dimensional surfaces at which $\psi = 0$. Consequently, atomic orbitals may be characterised by their corresponding nodes, related to the quantum numbers: the 1s orbital has no nodes, its wavefunction is spherically symmetrical and its numerical value decreases exponentially from the nucleus; the 2s orbital has one spherical node; and the $2p_{x,y,z}$ orbitals have nodes in the yz, xz and xy planes respectively. Figure 2.1 schematically depicts s and p orbitals; the + and - signs represent the arithmetic sign of the wavefunction — the signs determine how wavefunctions will combine when they interact (see section 2.2.1). The dashed lines represent nodal surfaces.

Electron states are filled according to the Pauli Exclusion Principle*. When all the electrons occupy the lowest possible energies, the atom is in its ground state. The outermost filled shell is occupied by the valence electrons, which participate in bonding between atoms and are responsible for many of the physical and chemical properties of the resulting molecule.

2.2.1 Hybridised orbitals and bonding

The electron configuration for carbon is $1s^2 2s^2 2p^2$ — i.e. the inner s shell is filled and of the four valence electrons, two are in the outer s orbital and two in p orbitals. As the s orbital is spherically symmetrical, it can form a

*No two fermions can have identical quantum numbers

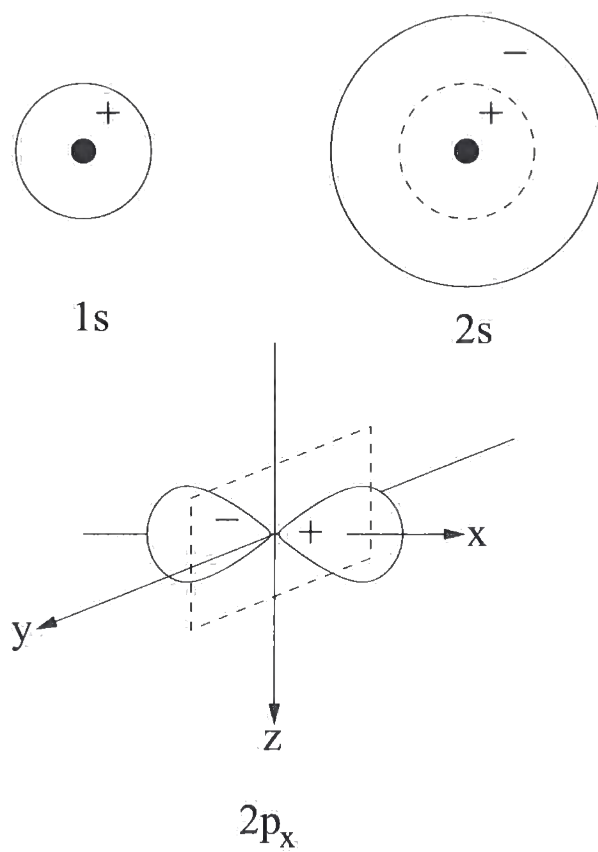


Figure 2.1: Schematic representations of s and p orbitals (from [1]).

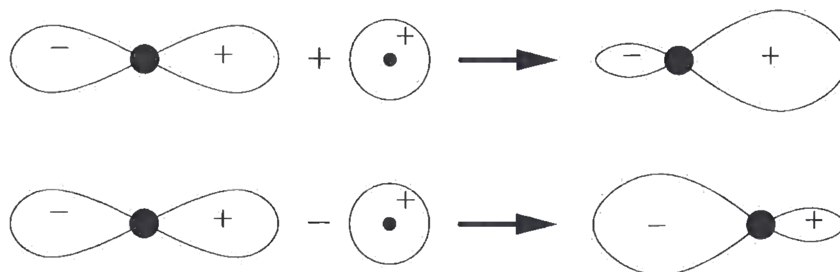


Figure 2.2: Mathematical combination of s and p orbitals to give two sp hybrids.

bond in any direction, whereas the p orbitals tend to form bonds along their axes. When two or more valence electrons are involved in bonding with other atoms, hybrid orbitals are constructed by combining the wavefunctions of the 2s and 2p orbitals. In the simplest case, the 2s orbital hybridises with a single p orbital, resulting in two sp hybrids, 180° apart; two p orbitals remain. The sp hybrids resulting from the sum and difference of the two wavefunctions are shown in figure 2.2.

Other combinations of orbitals lead to different hybrids. With three groups bonded to a central atom, three sp^2 hybrids are constructed from one s and two p orbitals — the hybrid lies in the plane of the two p orbitals, and the remaining p orbital is perpendicular to that plane. Similarly, four sp^3 hybrids can be derived from an s orbital and three p orbitals; in this case the hybrids form a tetrahedron: this is demonstrated in the structure of methane, which consists of four $C(sp^3)$–H(1s) bonds.

Although carbon tends to form four covalent bonds (with four sp^3 hybrids), it can also form double and triple bonds with itself using sp^2 and sp hybrids, respectively. Ethene, for example, contains two $C(sp^2)$–H(1s) bonds on each carbon; a third sp^2 hybrid forms a single $C(sp^2)$–$C(sp^2)$ bond in the plane of the molecule: a σ bond. A p orbital is 'left over' on the carbons, which lies perpendicular to the plane of the six atoms; the two p orbitals are parallel to each other and have regions of overlap above and below the molecular plane — the overlapping regions form sideways bonding π bonds. Figure 2.3 illustrates the bonding in ethene.

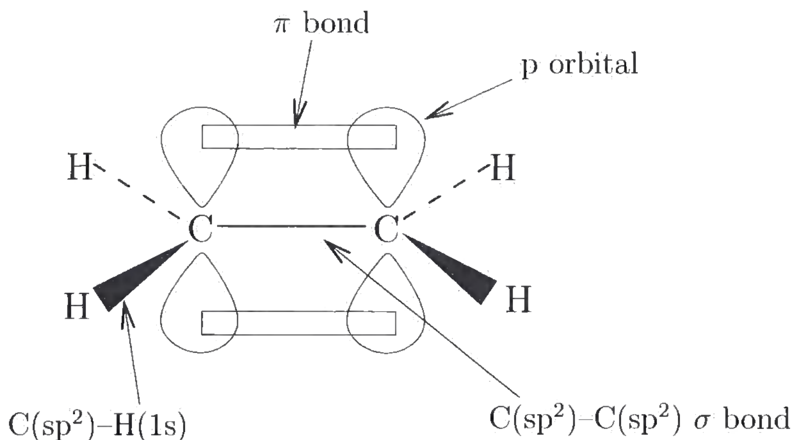


Figure 2.3: Bonding in ethene.

When a number of atoms are in close proximity, their atomic orbitals tend to overlap — in the case of overlapping p orbitals, the π electrons are able to localise over the whole molecule (see section 2.4.2).

2.3 Inorganic semiconductors

Solid state materials can be grouped into three classes — insulators, semiconductors and conductors, broadly defined by their conductivities. Insulators have conductivities in the order of 10^{-18} to 10^{-8} S/cm; conductors have conductivities above 10^4 S/cm; semiconductors have conductivities between these values [2]. This wide range of conductivities can be attributed to the arrangement of electrons in the solids' crystal structures.

2.3.1 Nearly-Free Electron Model

Although the free electron model of metals† gives a good insight into a number of properties of the material, including thermal and electrical conductivity, the model falls down on a number of points, such as the distinction between metals

†Valence electrons in a metal crystal structure are assumed to be completely detached from their ions (an electron 'gas'); electron-electron interactions are neglected; and the crystal lattice is not taken into account

and insulators, and many transport properties. Extending the free electron model to take into account a periodic potential of a solid crystal lattice causes new properties to emerge, the most important of which is the possibility of an energy band gap arising between valence and conduction band electrons [3].

A full derivation of the origin of electron bands and bandgaps is out of the scope of this thesis, as it is readily found in most solid state physics books. However, some important stages to the derivation are outlined below:

For a free electron gas in three dimensions, the Schrödinger equation is

$$\begin{aligned} -\frac{\hbar^2}{2m}\nabla^2\psi_{\mathbf{k}}(\mathrm{r}) &= \epsilon_{\mathbf{k}}\psi_{\mathbf{k}}(\mathbf{r}) \\ \Rightarrow -\frac{\hbar^2}{2m}\left(\frac{\partial^2}{\partial x^2}+\frac{\partial^2}{\partial y^2}+\frac{\partial^2}{\partial z^2}\right)\psi_{\mathbf{k}}(\mathrm{r}) &= \epsilon_{\mathbf{k}}\psi_{\mathbf{k}}(\mathbf{r}) \qquad (2.1) \end{aligned}$$

where ∇ is the gradient operator, $\hbar$ the reduced Planck constant, m the mass of an electron, $\psi_{\mathbf{k}}$ the electron wavefunction, and $\epsilon_{\mathbf{k}}$ the electron energy.

If the electrons are confined to a cube of edge L, the resulting wavefunction is the standing wave

$$\psi_n(\mathbf{r}) = A\sin\left(\frac{\pi n_x x}{L}\right)\sin\left(\frac{\pi n_y y}{L}\right)\sin\left(\frac{\pi n_z z}{L}\right) \qquad (2.2)$$

where n_x, n_y, n_z are positive integers, and the origin is at one corner of the cube. The wavefunctions also need to satisfy periodic boundary conditions with period L, thus

$$\psi(x+L,y,z) = \psi(x,y,z) \qquad (2.3)$$

and similarly for y and z. Hence equation 2.2 will only hold true when

$$\psi_n(\mathbf{r}) = A\sin(k_x x)\sin(k_y y)\sin(k_z z) \qquad (2.4)$$

$$k \equiv \frac{2n\pi}{L} \qquad (2.5)$$

where n is any positive or negative integer, or 0.

To explain band structure, this free electron model needs to be extended slightly.

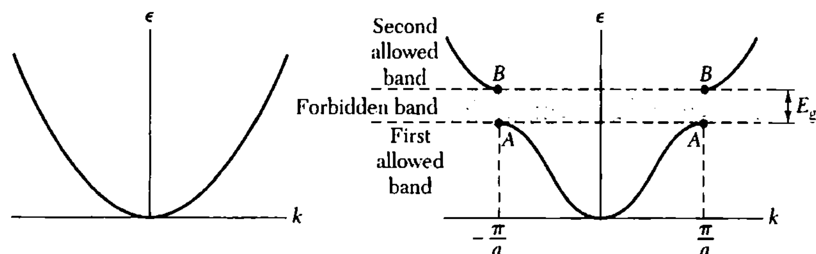


Figure 2.4: Plot of energy ϵ versus wavevector k for a free electron, and for an electron in a monatomic linear lattice of lattice constant a (image taken from [3]).

Bragg reflection[‡] is a characteristic of waves travelling in a crystal — this reflection of electron waves is the cause of energy (band) gaps: at Bragg reflection, wavelike solutions to the Schrödinger equation do not exist.

Figure 2.4 shows the energy versus wavevector for a free electron, and for a nearly-free electron with an energy gap at $k = \pm\pi/a$; other energy gaps occur at integer multiples of $\pm\pi/a$ — i.e. conditions required for Bragg scattering. At these points, the wavefunctions of the electrons are not travelling waves, but are standing waves: they are continually Bragg reflected between $+\pi/a$ and $-\pi/a$. These standing waves can be formed from two travelling waves:

$$\exp\left(\pm i\pi\frac{x}{a}\right) = \cos\left(\frac{\pi x}{a}\right) \pm i\sin\left(\frac{\pi x}{a}\right) \tag{2.6}$$

so the standing waves are

$$\psi(+) = \exp\left(i\frac{\pi x}{a}\right) + \exp\left(-i\frac{\pi x}{a}\right) = 2\cos\frac{\pi x}{a} \tag{2.7}$$

$$\psi(-) = \exp\left(i\frac{\pi x}{a}\right) - \exp\left(-i\frac{\pi x}{a}\right) = 2\sin\frac{\pi x}{a} \tag{2.8}$$

The two waves cause an accumulation of electrons at different regions, and hence have different values of potential energy in the field of the ions of the lattice — this is the origin of the energy gap. The magnitude of the energy gap and the occupation of the energy bands determines whether the crystal acts as an insulator, semiconductor, or conductor.

[‡]Reflection from crystal planes

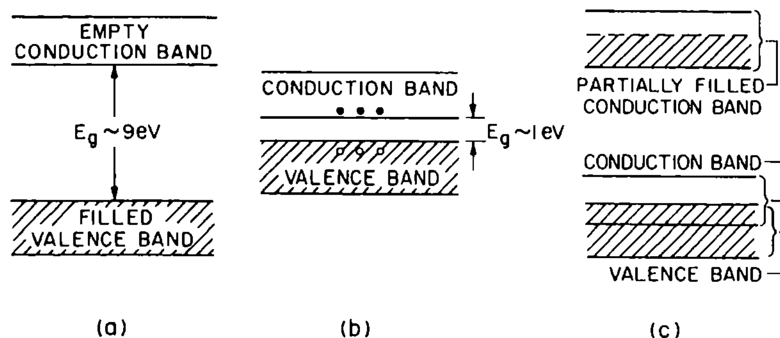


Figure 2.5: Schematic energy band representations of an insulator, a semiconductor, and a conductor (taken from [2]).

Figure 2.5 shows schematic representations of these properties. In an insulator, the valence electrons (section 2.2) completely fill the valence band, and there is a large gap between this and the conduction band. In a conductor, the conduction band is partially filled, or overlaps with the valence band so there is no band gap. In these cases, the electrons can easily move to higher energy levels when they gain kinetic energy, and hence current conduction readily occurs. In a semiconductor, the valence band is filled; however, the band gap is sufficiently small that thermal excitation can give electrons enough energy to jump to the conduction band, leaving a hole in the valence band. When an electric field is applied, both the electrons and holes will gain energy and conduct electricity.

2.4 Organic semiconductors

2.4.1 History

Most organic materials are electrical insulators with values of room temperature electrical conductivity in the range 10^{-9} - 10^{-14} Scm^{-1} [4] (10^9 - 10^{14} Ωcm resistivity). However, it was predicted in 1911 that certain organic solids may exhibit an electrical conductivity comparable to that of metals [5]; this was later confirmed in 1954 when Akamatu *et al.* reported a room temperature conductivity of around 10^{-1} Scm^{-1} for a bromine/perylene complex [6]; perylene (see figure 2.6) itself being an insulator with a room temperature

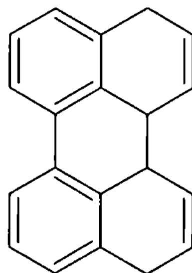


Figure 2.6: Perylene molecule.

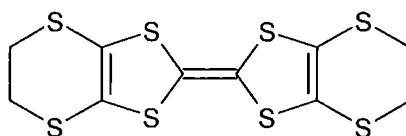


Figure 2.7: BEDT-TTF molecule.

conductivity of around 10^{-15} - 10^{-17} Scm^{-1}. Considerable further work was done in synthesising and investigating properties of both donor and acceptor molecules; a major milestone was the synthesis of the acceptor molecule tetracyano-*p*-quinodimethane (TCNQ) and the donor molecule tetrathiafulvalene (TTF), which were combined in 1972 to form the charge transfer salt (TTF)(TCNQ). This was the first organic solid to show metallic conductivity over an extended temperature range [7].

As further work was undertaken into organic conductors, it was found that some TTF derivatives exhibited superconducting properties; a notable one is a charge-transfer salt of bisethylenedithiotetrathiofulvalene (BEDT-TTF; figure 2.7, κ-$(\mathrm{BEDT\text{-}TTF})_2\mathrm{Cu(NCS)}_2$ (κ denoting the packing arrangement of the BEDT-TTF molecules), which has a critical temperature of 10.4 K [8, pages 76, 107].

Meanwhile, in 1977, Shirakawa, MacDiarmid and Heeger (Nobel Prize in Chemistry, 2000) discovered that oxidation of one of the polyacetylene film isomers (*trans*-isomer, shown in figure 2.8, is the thermodynamically stable form at room temperature) with halogens made the films $\sim 10^6$ times more conductive than the unhalogenated films [9]. This paper lead to a large amount

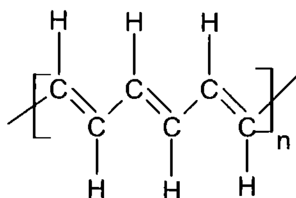


Figure 2.8: *trans*-isomer of polyacetylene.

of research into conducting polymers, distinct from the research into conductive low molecular weight organic materials.

The work in this thesis is based on small molecule semiconductors, and thus following sections will only concentrate on these.

2.4.2 Band structure of molecular crystals

A molecular crystal may be regarded as a miniature lattice with a precisely spaced series of atoms in close proximity to each other, giving rise to a good overlap of their atomic orbitals. The intramolecular interactions between the atoms lead to a splitting of the $2p_z$ orbitals and to a localisation of the π electrons over the whole molecule. As a result, bonding orbitals[§] take up the electrons whereas the antibonding orbitals[¶] remain empty [1]. Thus there is a highest occupied molecular orbital (HOMO) energy level and a lowest unoccupied molecular orbital (LUMO) energy level, analogous to the valence and conduction bands in inorganic semiconductors (section 2.3).

Most organic solids are insulators due to there being a large energy difference between the HOMO and LUMO levels, with the HOMO level being completely filled, and the solids are usually molecular, not possessing a system of covalent bonds extending over macroscopic distances, hence quantum mechanical interactions between the HOMOs of adjacent molecules are small and the valence band formed by these interactions is very narrow. Similarly, the conduction band arising from the interactions between the LUMOs is also

[§]The wavefunction formed from the sum $\psi_A + \psi_B$ of two single electron wavefunctions

[¶]The wavefunction formed from the difference $\psi_A - \psi_B$ of two single electron wavefunctions

small, so the band gap is essentially that of the free molecule. This is also true for any σ-bonded polymers (e.g. polyethylene).

To obtain a larger conductivity and hence semiconducting behaviour, the HOMO–LUMO gap needs to be reduced; this can be achieved by including heteroatoms with lone pair electrons (e.g. polyaniline or polyaromatics), or with extensive π-bonding [7]. With pentacene, for example (see section 2.7.1), incorporating the molecule into a larger crystal structure drastically changes the HOMO and LUMO levels: from around 1.2 eV (for the single molecule) to around 2.8 eV (for the crystal) for the LUMO level, and from 6.5 eV to 5 eV for the HOMO level. In the acene series, from benzene to pentacene, as the number of benzene rings increase, the size of the π electron system increases, and the HOMO–LUMO bandgap correspondingly decreases [1].

A large number of small-molecule semiconductors exist; a summary of some of these materials can be found in section 2.7.1.

2.5 Transistors

2.5.1 Field-effect transistor

A field effect transistor is a unipolar device (currents are carried predominantly by either electrons or holes), in which the conductivity of the semiconductor is modulated by a transverse electric field [10]. Figure 2.9 shows a photograph of the first MOSFET (Metal-Oxide-Semiconductor FET), fabricated in 1960 with a thermally oxidised silicon substrate (over 100 nm) and a channel length of over 20 µm [2]. A perspective view of a silicon MOSFET is shown in figure 2.10; it consists of a p-type semiconductor substrate in which two n-type regions (the source and the drain) are formed; the gate is formed by direct metal contact to the oxide. The remainder of this section will describe n-channel FETs.

When no voltage is applied to the gate, the source-to-drain electrodes correspond to two p-n junctions connected back-to-back; the only current that can flow is a reverse leakage current (this is the case for an enhancement mode device; a depletion mode device continues to have a small conductive channel, and requires a negative gate voltage to turn the transistor 'off'). When a

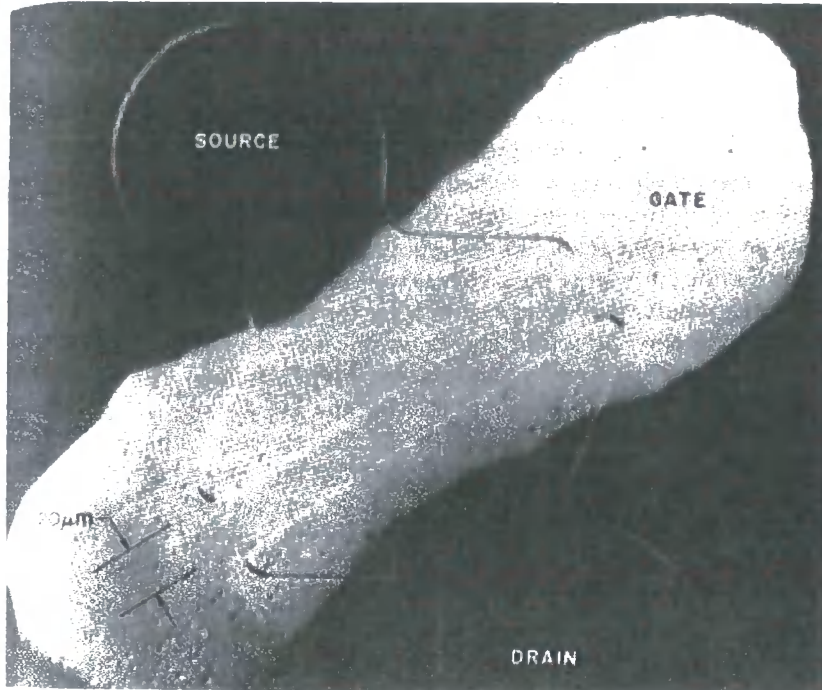


Figure 2.9: First MOSFET fabricated using a thermally oxidised silicon substrate (taken from [2]).

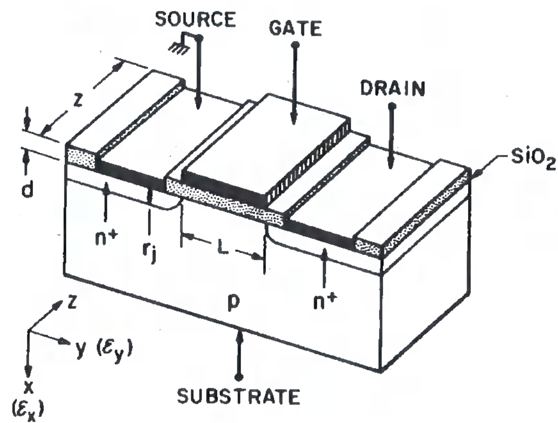


Figure 2.10: Perspective view of the MOSFET (taken from [2]).

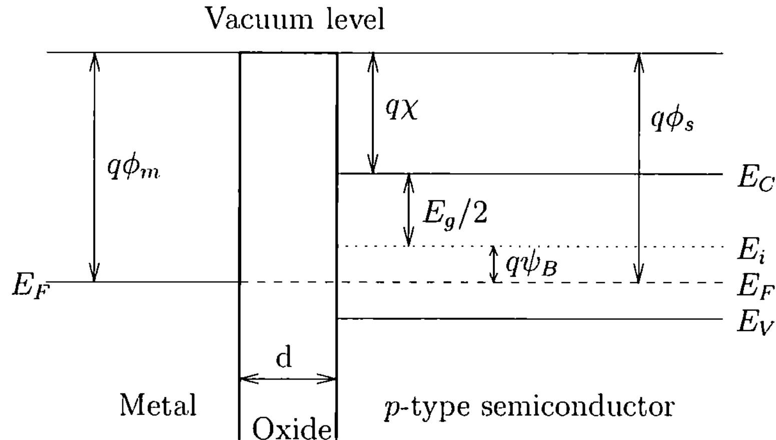


Figure 2.11: Energy band diagram of an ideal MOS diode at $V = 0$ (from [2]).

large enough positive voltage is applied to the gate (greater than the threshold voltage), an n-type channel (surface inversion layer) is formed between the two n-type regions, so the source and drain are connected by a conducting n-channel. The conductance of the channel can be modified by varying the gate voltage.

The formation of the inversion layer can be explained by looking at the case of a MOS diode (the gate contact of the MOSFET is essentially a MOS diode). For an ideal MOS diode, the following assumptions are made:

1. At zero applied bias, the energy difference between the metal work function and semiconductor work function is zero.

2. The only charges that exist in the diode under any biasing conditions are those in the semiconductor and those with equal but opposite sign on the metal surface adjacent to the oxide

3. There is no carrier transport through the oxide under DC biasing conditions

The energy band diagram for an ideal MOS diode at zero bias is shown in figure 2.11. $q\phi_m$ and $q\phi_s$ are the metal and semiconductor work functions, $q\chi$ the semiconductor electron affinity, $q\psi_B$ the energy difference between the

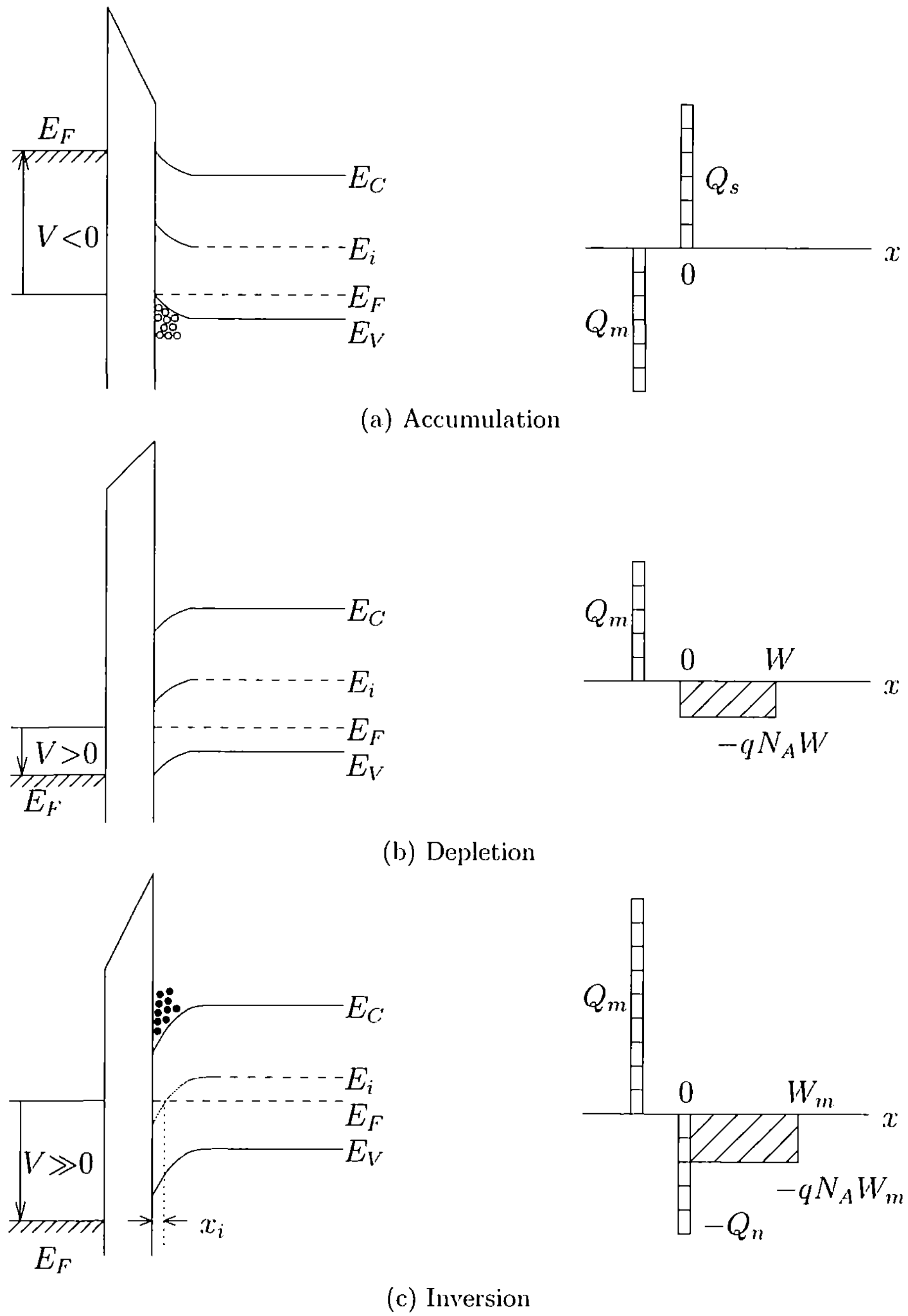


Figure 2.12: Energy band diagrams and charge distributions of an ideal MOS diode (from [2]).

Fermi level E_F and the intrinsic Fermi level E_i. When the diode is biased with positive or negative voltages, three cases may exist at the semiconductor surface: the energy band diagrams and charge distributions for these are shown in figure 2.12. In the ideal diode, no current flows in the device (assumption 3), thus the Fermi level in the semiconductor will remain constant. In figure 2.12a, a negative voltage is applied to the metal, thus the bands near the semiconductor surface are bent upward. The carrier density in the semiconductor depends on the difference between E_i and E_F in the relation

$$p_p = n_i e^{(E_i - E_F)/kT} \tag{2.9}$$

where n_i is the intrinsic carrier concentration. The upward bending increases $E_i - E_F$, and hence increases the carrier concentration close to the oxide surface — i.e. an accumulation of holes.

When a small positive voltage is applied (figure 2.12b), the energy bands bend downward, and thus the hole concentration is reduced — i.e. a depletion of holes. The space charge per unit area, Q_{sc}, in the semiconductor is given by the charge within the depletion region:

$$Q_{sc} = -qN_A W \tag{2.10}$$

where W is the width of the depletion region and N_A is the substrate doping.

Figure 2.12c shows the case when a larger positive voltage is applied: the bands bend more so that E_i crosses over E_F. The electron concentration, similar to the hole concentration given in equation 2.9, is given by

$$n_p = n_i e^{(E_F - E_i)/kT} \tag{2.11}$$

When $E_F > E_i$, as is the case with the large positive voltage, the electron concentration at the surface is larger than n_i, which in turn is larger than the hole concentration. As $n_p > p_p$, the surface is thus inverted. As the bands are bent further, the conduction band edge approaches the Fermi level; at this point the electron concentration increases rapidly. After this point most of the additional negative charges in the semiconductor consist of the charge Q_n

due to the electrons in a narrow n-type inversion layer. The width of this inversion layer tends to range from 1 – 10 nm [2]. Once an inversion layer is formed, the surface depletion layer width reaches a maximum — an increase in potential will result in a large charge increase in the inversion layer, and thus not have an effect on the depletion layer. Thus the charge per unit area in the semiconductor is given by

$$Q_s = Q_n + Q_{sc} \tag{2.12}$$

where Q_{sc} corresponds to the space charge per unit area at $W = W_{max}$.

When a potential is applied, this voltage will appear partly across the oxide and partly across the semiconductor. Thus

$$V = V_{ox} + \psi_s \tag{2.13}$$

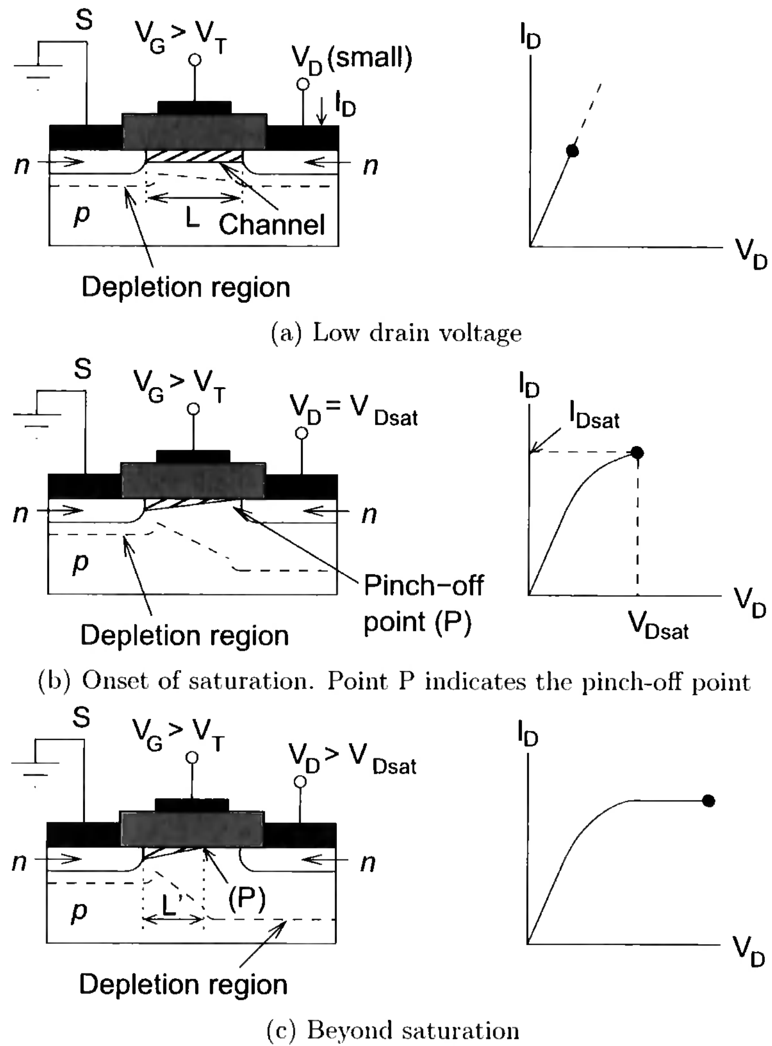
where ψ_s is the semiconductor potential and V_{ox} is the potential across the oxide (thickness d) given by

$$V_{ox} = \mathcal{E}_{ox} d = \frac{|Q_s|\, d}{\epsilon_0 \epsilon_{ox}} \equiv \frac{|Q_s|}{C_{ox}} \tag{2.14}$$

Figure 2.13 shows a schematic of the MOSFET operation, and output I-V characteristics when the gate voltage is above the threshold voltage (i.e. an inversion layer has been formed). If a small drain voltage is applied (figure 2.13a), electrons will flow from source to drain through the conducting channel. Thus the channel simply acts as a resistance, and I_D is proportional to V_D — the linear region of operation. The total charge induced in the semiconductor per unit area, Q_s, at a distance y from the source is given from equations 2.13 and 2.14 by

$$Q_s(y) = -\left[V_G - \psi_s(y)\right] C_{ox} \tag{2.15}$$

where $C_{ox} = \epsilon_0 \epsilon_{ox}/d$ is the gate capacitance per unit area and $\psi_s(y)$ is the surface potential at y.



(a) Low drain voltage

(b) Onset of saturation. Point P indicates the pinch-off point

(c) Beyond saturation

Figure 2.13: Operations of the MOSFET and output I-V characteristics (from [2]).

The charge in the inversion layer, from equations 2.12 and 2.15 is

$$\begin{aligned} Q_n(y) &= Q_s(y) - Q_{sc}(y) \\ &= -\left[V_G - \psi_s(y)\right] C_{ox} - Q_{sc}(y) \end{aligned} \tag{2.16}$$

$\psi_s(y)$ at inversion can be approximated by $2\psi_B + V(y)$, where $V(y)$ is the potential at a point y away from the source. $Q_{sc}(y)$ can be formulated|| by

$$Q_{sc} = -qN_a W_{max} \simeq -\sqrt{2\epsilon_s q N_A \left[V(y) + 2\psi_B\right]} \tag{2.17}$$

Substituting equation 2.17 into 2.16 gives

$$Q_n(y) \simeq -\left[V_G - V(y) - 2\psi_B\right] C_{ox} + \sqrt{2\epsilon_s q N_A \left[V(y) + 2\psi_B\right]} \tag{2.18}$$

The conductivity of the channel at position y can be approximated by

$$\sigma(x) = qn(x)\mu(x) \tag{2.19}$$

For a constant mobility, the channel conductance is then given by

$$g = \frac{w}{L}\int_0^{x_i} \sigma(x)dx = \frac{w\mu}{L}\int_0^{x_i} qn(x)dx \tag{2.20}$$

where w is the channel width and L the channel length. The integral corresponds to the total charge per unit area in the inversion layer, and is therefore equal to $|Q_n|$. The channel resistance of a section dy is

$$dR = \frac{dy}{gL} = \frac{dy}{w\mu\,|Q_n(y)|} \tag{2.21}$$

and thus the voltage drop is

$$dV = I_D dR = \frac{I_D dy}{w\mu\,|Q_n(y)|} \tag{2.22}$$

where the drain current is independent of y. Substituting equation 2.18 into

||The derivation is out of the scope of this thesis but may be found in section 5.4.1 of [2].

2.22 and integrating from source ($V = 0$, $y = 0$) to drain ($V = V_D$, $y = L$) yields

$$I_D \simeq \frac{w}{L}\mu C_{ox}\left\{\left(V_G - 2\psi_B - \frac{V_D}{2}\right)V_D \right.$$
$$\left. \frac{2}{3}\frac{\sqrt{2\epsilon_s q N_A}}{C_{ox}}\left[(V_D + 2\psi_B)^{3/2} - (2\psi_B)^{3/2}\right]\right\} \quad (2.23)$$

In the case of small V_D (transistor operating in the linear mode), this equation reduces to

$$I_D \simeq \frac{w}{L}\mu C_{ox}\left(V_G - V_T\right) \qquad V_D \ll V_G - V_T \quad (2.24)$$

where V_T is the threshold voltage given by

$$V_T \simeq \frac{\sqrt{2\epsilon_s q N_A\left(2\psi_B\right)}}{C_{ox}} + 2\psi_B \quad (2.25)$$

The derivation of V_T is outside the scope of this thesis, but can be found in section 5.4.1 of [2].

As the drain voltage increases, it reaches a point at which the width of the inversion layer at $y = L$ is reduced to zero (figure 2.13b). The charge, $Q_n(y)$ at $y = L$, therefore becomes zero, and the number of mobile electrons at the drain are reduced drastically; the drain current and voltage at this point are designated I_{Dsat} and V_{Dsat}. Beyond this 'pinch-off' point, the drain current remains essentially the same because for $V_D > V_{Dsat}$, at point P the voltage V_{Dsat} remains the same. Thus the number of carriers arriving at P from the source, and hence source-drain current, remains the same. The major change is a decrease in L to L', as in figure 2.13c.

The value of V_{Dsat} can be obtained from equation 2.18 under the condition $Q_n(L) = 0$:

$$V_{Dsat} \simeq V_G - 2\psi_B + K^2\left(1 - \sqrt{1 + \frac{2V_G}{K^2}}\right) \quad (2.26)$$

where $K \equiv \sqrt{\epsilon_s q N_A}/C_{ox}$. Substituting equation 2.26 into 2.23 gives the saturation current

$$I_D \simeq \frac{w\mu\epsilon_0\epsilon_{ox}}{2dL}(V_G - V_T)^2 \equiv \frac{\mu w}{2L}C_{ox}(V_G - V_T)^2 \qquad V_D > V_G - V_T \quad (2.27)$$

In the saturation region, the mobility can be obtained (graphically) by plotting the square root of the saturation current against gate voltage and obtaining the gradient:

$$\text{gradient} = \sqrt{\frac{1}{2}\mu\frac{w}{L}C_{ox}} \quad (2.28)$$

which can be rearranged to obtain a mobility

$$\mu = \frac{2(\text{gradient})^2 L}{wC_{ox}} \quad (2.29)$$

2.5.2 Thin-film transistor

A thin film transistor (TFT) is a field effect transistor made by depositing thin films of dielectric, semiconductor, and contacts over a supporting substrate. In comparison, in the MOSFET, the semiconductor also doubles as the substrate for the n-type regions and the dielectric. Probably the most common use of TFTs is in liquid crystal displays; these transistors are usually fabricated on glass substrates.

The transistors reported on in this work are all thin-film transistors, using organic semiconductors as the active layer. The substrates are almost all silicon wafers; conductive silicon was chosen due to its ability to act directly as the transistor gate, and the relative ease of growing a good quality oxide as the dielectric.

2.5.3 Grain-boundary barrier model

The semiconducting layers in TFTs are commonly amorphous or polycrystalline silicon; in organic TFTs pentacene, which tends to form a polycrystalline structure when deposited, is a common material. With a polycrystalline material, a grain-boundary barrier model (illustrated in figure 2.14) can be applied. This model assumes that carriers are transported at inter-poly-grains

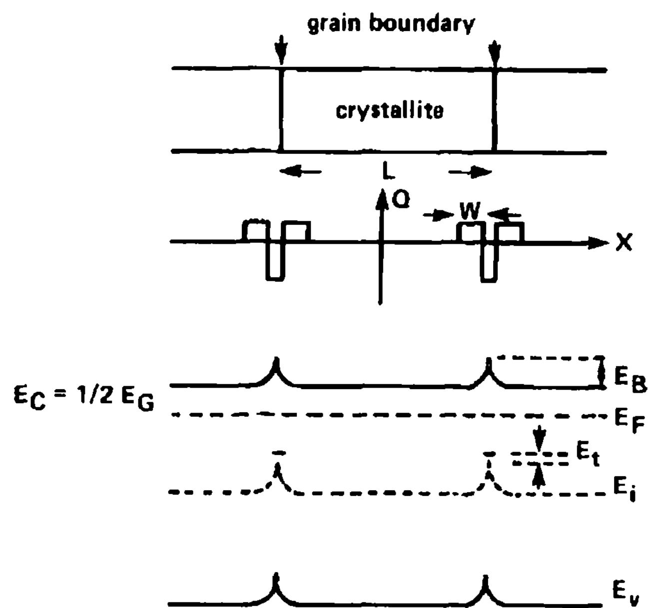


Figure 2.14: Grain structure, charge distribution and band diagram assumed in the grain boundary trapping model (taken from [11]).

by thermionic emission over the grain boundary barrier and that no scattering is taking place in the grains [11]. The trap density N_t can be determined from a Levinson plot of $\ln(I_D/V_G)$ against $1/V_G$. The Levinson model is based on the predicted transistor drain current in the linear regime [12], given by

$$\begin{aligned} I_D &= \mu_0 V_D C_{ox} \left(\frac{W}{L}\right) V_G \exp\left(-\frac{E_B}{kT}\right) \\ &\equiv \mu_0 V_D C_{ox} \left(\frac{W}{L}\right) V_G \exp\left(-\frac{s}{V_G}\right) \end{aligned} \tag{2.30}$$

where E_B is the potential barrier height, μ_0 is the trap-free mobility, and the thermally activated mobility is

$$\mu = \mu_0 \exp\left(-\frac{E_B}{kT}\right) \equiv \mu_0 \exp\left(-\frac{s}{V_G}\right) \tag{2.31}$$

Screening causes E_B to fall as V_G increases, hence N_t can be estimated from the slope s of the Levinson plot using the formula

$$s = \frac{q^3 N_t^2 t}{8\epsilon k T C_{ox}} \tag{2.32}$$

where t represents the thickness of the semiconducting layer, and ϵ is the dielectric constant of the semiconductor (which can be taken as 4 for pentacene [12]).

2.5.4 Organic TFT

Replacing the silicon in a TFT with an organic semiconductor has been an area of active research for the last 20 years. Compared to silicon, organic devices have relatively low mobilities, and so are not suitable for applications requiring high switching speeds. However, they have advantages over silicon for applications that require large-area coverage, structural flexibility, low-temperature processing and low cost; such applications include the driving circuitry for "paper" displays, or low end data storage such as RFID tags [13]. Table 2.2 lists the highest reported mobility for organic FETs published between 1986 and 1997 (more recent developments are given in section 2.7.2).

Year	Mobility ($cm^2/V/s$)	Material
1986	10^{-5}	polythiophene
1988	10^{-4}	polyacetylene
	10^{-4}	phthalocyanine
	10^{-4}	poly(3-hexylthiophene)
1989	10^{-3}	poly(3-alkylthiophene)
	10^{-3}	α,ω-hexathiophene
1992	0.02	α,ω-hexathiophene
	2×10^{-3}	pentacene
1993	0.05	α,ω-di-hexyl-hexathiophene
1994	0.06	α,ω-di-hexyl-hexathiophene
1995	0.03	α,ω-hexathiophene
	0.038	pentacene
	0.3	C_{60}
1996	0.02	phthalocyanine
	0.045	poly(3-hexyxthiophene)
	0.13	α,ω-di-hexyl-hexathiophene
	0.6	pentacene
1997	1.3	pentacene

Table 2.2: Field effect mobilities of early OTFTs (taken from [14]).

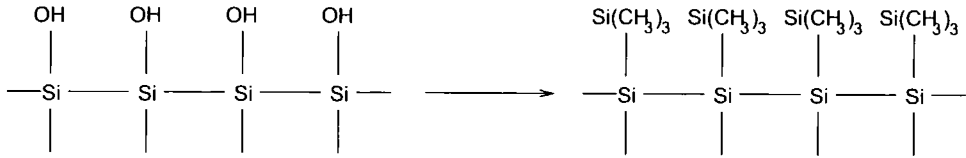


Figure 2.15: Treatment of SiO_2 surface with silanising agent.

2.6 Organic TFT dielectric surface treatments

For organic FETs using a silicon oxide dielectric, a number of studies have shown that the oxide surface is very important to the mobility and characteristics of the transistors ([15–18], also sections 5.4.2, 5.4.6 and 5.4.8). Reduction in mobility, or increase in hysteresis in the transfer or output characteristics have been attributed to charge trapping at the oxide surface. Two surface treatments are commonly used to minimise these trapping states: firstly, an oxygen plasma ([17, 18]; section 5.4.6) is used to remove residual organic contamination; this procedure is primarily performed after stripping photoresist from the oxide surface. Secondly, a silane treatment (section 5.4.2) can be applied to modify chemically the SiO_2 surface: normally, the surface is terminated with -OH groups, which act as good charge traps; the silanising agent substitutes these groups with $(CH_3)_3$-Si- groups [15], which render the oxide surface hydrophobic. Figure 2.15 illustrates this group substitution. Two silane-based surface treatments are used in the course of this work: dicholorodimethylsilane (DMDS; $(CH_3)_2Cl_2Si$) and hexamethyldisilazane (HMDS; $(CH_3)_3$Si-NH-Si$(CH_3)_3$, reported in [15]).

2.7 Recent research

There exists a large body of published literature about organic semiconductors and thin film transistors [19]. A summary of some of the research is given below.

2.7.1 Organic semiconducting materials

There exist a large number of small-molecule semiconductors, which can be broadly grouped into a few different types.

Linear acenes, such as anthracene, tetracene, or pentacene (see chapter 5) consist of a number of benzene molecules arranged in a straight line. They are important materials in electrical applications because the band gap is controllable by selecting the number of aromatic rings [20]: the more rings, the smaller the band gap. Most published work on acenes concerns devices made out of pentacene, such as transistors or diodes [21], as pentacene is a well-established, reliable semiconducting material with good carrier mobility. There has been investigation into doping the pentacene films with iodine and alkaline metals [20, 22, 23]; achieving maximum conductivity of 150 $\mathrm{Scm^{-1}}$ for highly ordered films heavily doped with iodine, and 2.8 $\mathrm{Scm^{-1}}$ for a rubidium-doped film, which turned the film into an n-type semiconductor. A derivative of a linear acene, 5,6,11,12-tetraphenyltetracene (rubrene) has been reported to have a carrier mobility of $\sim$ 20 $\mathrm{cm^2/V/s}$ at room temperature, increasing to $\sim$ 30 $\mathrm{cm^2/V/s}$ at around 150 K [24]. This appears to be one of the highest mobilities reported for an organic semiconductor.

Thiophene-based molecules (see also chapter 7) are a popular alternative to acenes. A large body of published work exists on the synthesis and properties of thiophene-based materials — reported improvements over pentacene include better resistance to oxidation [25]. Transistor mobilities reported are not as high as those for pentacene; nevertheless they have reasonable values: 0.15 $\mathrm{cm^2/V/s}$ [25, 26], increasing up to 1.0 $\mathrm{cm^2/V/s}$ [27].

There have been reports of other materials used as semiconductors, for example copper phthalocyanines [28] or azurin proteins [29]. A number of other materials have been reported with n-type behaviour: some of these are summarised in the section below. Section 2.7.2 contains more details on transistor performances of various materials.

n-type organic semiconductors

A characteristic feature of most organic semiconductors is strong trapping of electrons but not holes — i.e. the materials exhibit p-type conduction [30]. However, in order to make complementary FETs it is necessary to obtain n-type materials with electron mobilities of the same order as hole mobilities in p-type materials. Although there has been a large amount of research into n-type semiconductors in recent years, many n-type materials only work in a vacuum or inert atmosphere because ambient oxygen and moisture can act as electron traps [31].

It has been shown that by incorporating electron deficient groups into normally p-type materials, it is possible to improve the electron transport properties, thus obtaining n-type behaviour [32]. Thiophenes are common materials to incorporate electron deficient groups in due to the ease of functionalising the group [33]; mobilities of these materials have been found to be reasonable: incorporation of a trifluoromethylphenyl derivative into a dithiazolylbenzothiadiazole derivative yielded a field effect mobility of 0.068 $cm^2/V/s$ [33], while incorporating the trifluoromethylphenyl group onto a thiazolothiazole unit yielded a mobility of up to 0.30 $cm^2/V/s$ [34].

Naphthalenetetracarboxylic diimide compounds have been used in the fabrication of n-channel FETs: it was found that an unfluorinated compound exhibited a mobility of 0.16 $cm^2/V/s$ under vacuum, but the device rapidly deactivated on exposure to air; fluorinated compounds, however, were relatively stable in air but at a reduced mobility ($\sim$ 0.01 $cm^2/V/s$) [35]. One of the highest reported mobilities for n-type devices was for the compound N,N'-bis(2,2,3,3,4,4,4-heptafluorobutyl)-perylene tetracarboxylic diimide, which exhibited a field-effect mobility of 0.75 $cm^2/V/s$ in nitrogen, reducing to 0.56 $cm^2/V/s$ in air but remaining stable for more than 50 days [31].

2.7.2 OTFTs

Given the large volume of research into organic TFTs, a summary of a selection of papers published in the last few years is given in table 2.3.

Two main approaches to OTFT research are evident. One aspect involves investigating the semiconducting and FET behaviour of newly synthesised molecules; these transistors tend to be fabricated on silicon / silicon oxide with gold contacts, as this is a common configuration that has produced reliable devices. A significant number of these molecules are based on thiophenes; mobilities of these molecules, where semiconducting behaviour was evident, varied between around 0.05 $cm^2/V/s$ and >1 $cm^2/V/s$. Halik *et al.* [27] found, when investigating sexithiophene-based molecules, that the length of alkyl chains in alkyl-substituted molecules had a significant effect on the mobility of the transistors: reducing the alkyl chain length from ten to six units increased the mobility (for top contact devices) from 0.1 to 1.0 $cm^2/V/s$. This was attributed to the alkyl chains forming an intrinsic barrier separating the thiophene backbone from the contacts, thus increasing the effective contact resistance. Removing the alkyl chains entirely reduced the carrier mobility to 0.07 $cm^2/V/s$; this was attributed to the presence of optimised alkyl chains resulting in enhanced molecular ordering and improved π–π stacking in the active layer. Molecules exhibiting n-type behaviour (see also section 2.7.1) typically contained electron-deficient fluorine groups; although these were air-stable, mobilities tended to be < 0.1 $cm^2/V/s$. Higher mobility n-type devices tended to work only in vacuum, degrading rapidly in air. Only recently have high-mobility, air-stable n-type molecules been synthesised [31].

Another aspect of the research investigates the optimisation of the fabrication methods and conditions of OTFTs. Usually, pentacene is used due to its air-stability, reliability as a semiconductor and potential for high mobilities. It has been found that two major factors contribute to the performance of the transistors: pentacene deposition conditions and dielectric surface treatment. The rate of pentacene deposition affects the crystal size [36] (see also sections 5.2.3 and 5.4.4) — the larger crystal sizes result in fewer inter-grain boundaries, and thus a corresponding increasing in mobility is observed. Depositing the pentacene onto a substrate held at an elevated temperature also resulted in increased mobility [12,16,17]. Treating a silicon oxide dielectric (see section 2.6) with silane-based surface treatments was found to increase the mobility of transistors [15] (see also section 5.4.2), due to chemical modification of the

oxide surface to remove charge traps. Oxygen plasmas have been found to increase mobility and reduce hysteresis in the devices [17] (see also section 5.4.6); these have been attributed to a physical reduction in trapping states on the dielectric surface: the oxygen plasma removing carbon contamination from the surface. Replacing silicon dioxide with other dielectric materials has shown promise: organic dielectrics such as PMMA [37] or polyimide [38] have resulted in devices with reasonable mobilities, low hysteresis and negative threshold voltages. An Atomic Layer Deposition deposited Al_2O_3 / HfO_2 bi-layer [39] was found to reduce the threshold voltage compared to silicon oxide, but also reduced the mobility by an order of magnitude. Using a titanium gate electrode with TiO_2 dielectric, capped with a styrene-based layer [40] resulted in a transistor with a low threshold voltage (-0.48 V) and a high mobility (0.8 $cm^2/V/s$).

Table 2.3: Structure and results of OTFTs published in recent years.

Authors	**Structure**	**Results**
Sheraw *et al.* (2002) [41]	Polyethylene naphthalate (PEN) film substrate, Ni gate, SiO_2 dielectric, Pd electrodes, pentacene semiconductor	Mobility: 1.2 $cm^2/V/s$; on-off current ratio: 10^8
Baude *et al.* (2003) [13]	Glass substrate, Ti/Au gate, e-beam evaporated Al_2O_3 dielectric, styrene-based surface treatment, pentacene semiconductor, Au electrodes	Mobility: 1.5 $cm^2/V/s$; -5 V threshold voltage; 2V/decade subthreshold slope; on-off ratio: 10^6–10^7
Halik *et al.* (2003) [27]	Si substrate, PVP dielectric, oligothiophene-based semiconductor, Au electrodes	Mobilities ranged from 0.07 to 1.1 $cm^2/V/s$; on-off ratios ranged from 10^2 to 10^5, depending on semiconducting material and device layout

Continued on next page

Authors	**Structure**	**Results**
Qiu *et al.* (2003) [42]	Glass substrate, ITO gate, PMMA dielectric, pentacene semiconductor, Au electrodes	Mobility: 4.2×10^{-2} $cm^2/V/s$ in air, reducing over time; 2.6×10^{-2} $cm^2/V/s$ when encapsulated in UV resin, remaining fairly constant over time
Puigdollers *et al.* (2004) [37,43]	Si substrate, Cr gate with Au contact, PMMA dielectric, pentacene semiconductor, Au electrodes	Mobility: 0.01 $cm^2/V/s$; -15 V threshold voltage; 2.1 V/decade subthreshold slope; on-off ratio: 10^3
Wang *et al.* (2004) [44]	Si substrate, SiO_2 dielectric, Ti/Au electrodes, pentacene semiconductor	For a 9 nm channel length, mobility: 0.046 $cm^2/V/s$, on-off ratio: 97
Kim *et al.* (2004) [39]	Si substrate, HfO_2/Al_2O_3 dielectric grown using ALD, pentacene semiconductor, Au electrodes, indium gate contact	Mobility: 0.024 $cm^2/V/s$; on-off ratio: 10^2; threshold voltage: -0.25 V (reduced from 15.3 V for transistor using SiO_2 dielectric)

Continued on next page

Authors	Structure	Results
Wang *et al.* (2004) [12]	Glass substrate, sputtered Cr gate, PECVD deposited SiO_2 dielectric, pentacene semiconductor, Au electrodes	In vacuum: mobility: 0.43 $cm^2/V/s$, threshold voltage: -7.26 V, subthreshold slope: 1.7 V/decade, on-off ratio: 10^6. In air: mobility: 0.11 $cm^2/V/s$, threshold voltage: -20 V, subthreshold slope 5 V/decade; on-off ratio: 10^5. Difference between air and vacuum results attributed to diffusion of H_2O, O_2, and CO_2 molecules into pentacene film, causing charge trapping
Murphy *et al.* (2004) [45]	Si substrate, SiO_2 dielectric, diester functionalised sexithiophene derivative semiconductor, Au electrodes	Mobility: 0.05 $cm^2/V/s$ after annealing; on-off ratio: $> 10^5$
Daraktchiev *et al.* (2005) [46]	Si substrate, SiO_2 dielectric activated by exposure to oxygen plasma for 5 min in 0.1 mbar O_2 atmosphere at -40 V bias, pentacene semiconductor, Au electrodes	Mobility: 0.1 $cm^2/V/s$; threshold voltage: 16 V

Continued on next page

Authors	**Structure**	**Results**
Majewski *et al.* (2005) [40]	Polyester foil substrate, titanium evaporation followed by anodisation in 10^{-3} M citric acid using Pt counter electrode to make TiO_2 insulation, capped with a thin spin-coated layer poly(α-methylstyrene), pentacene semiconductor, Au electrodes	Mobility: 0.8 $cm^2/V/s$; threshold voltage: -0.49 V; subthreshold slope: 130 mV/decade; on-off ratio: $> 10^4$
Ando *et al.* (2005) [34]	Si substrate, SiO_2 dielectric, thiazolothiazole derivative or bithiophene derivative semiconductors, Au electrodes	Mobilities ranged from 0.12 to 0.30 $cm^2/V/s$; on-off ratios of 10^5–10^6; semiconductors were n-type
Unni *et al.* (2005) [38]	ITO-coated glass substrate and gate; HD Microsystems PI-2555 polyimide dielectric; pentacene semiconductor, Au electrodes	Mobility: 0.16 $cm^2/V/s$; threshold voltage: -6.4 V; subthreshold slope: 7.5 V/decade; on-off ratio: $\sim 10^4$
Akhtaruzzaman *et al.* (2005) [33]	Si substrate, SiO_2 dielectric, trifluoromethylphenyl derivative of dithiazolylbenzothiodiazole semiconductor, Au contacts	Mobility: 0.05 $cm^2/V/s$; threshold voltage: 20 V; on-off ratio: 10^4; semiconductor was n-type
Yagi *et al.* (2005) [15]	Si substrate, Au/Ti/Al gate contact, SiO_2 dielectric, HMDS surface treatment, pentacene semiconductor, Au electrodes	Mobility: 0.2 $cm^2/V/s$; threshold voltage: -0.8 V

Continued on next page

Authors	Structure	Results
D'Amico *et al.* (2005) [29]	Si substrate, SiO_2 dielectric, azurin protein semiconductor, Au electrodes	Ambipolar behaviour exhibited; threshold voltage of 0.8 V for n-type behaviour, and -4.4 V for p-type
Koo *et al.* (2007) [47]	Si substrate, Ti gate electrode, PEALD deposited Al_2O_3 dielectric, HMDS surface treatment, pentacene semiconductor, Au electrodes	Mobility: 0.38 $cm^2/V/s$; threshold voltage: 1 V; subthreshold slope: 0.6 V/decade; on-off ratio: $> 10^8$
Klauk *et al.* (2007) [28]	Glass or PEN substrate, Al gate, Al_2O_3 + n-octadecylphosphonic acid self-assembled monolayer, pentacene or $F_{16}CuPc$ semiconductors	Mobility: 0.6 $cm^2/V/s$ for pentacene and 0.02 $cm^2/V/s$ for $F_{16}CuPc$
Kitamura and Arakawa (2007) [48]	Glass substrate, TiSi gate, TiSiO dielectric, pentacene (p-type) or C_{60} (n-type) semiconductor, Au electrode for pentacene; LiF/Al electrode for C_{60}	Pentacene: mobility: 0.59 $cm^2/V/s$, threshold voltage: -0.84 V; C_{60}: mobility: 0.68 $cm^2/V/s$, threshold voltage: 0.80 V
Oh *et al.* (2007) [31]	Si substrate, SiO_2 dielectric, OTS surface treatment, PTCDI-C4F7 semiconductor, Au electrodes	Mobility: $\sim$ 0.67 $cm^2/V/s$ in N_2, $\sim$ 0.51 $cm^2/V/s$ in air; on-off ratio: 10^5 in N_2, 10^6 in air

2.8 Summary

The operation of semiconductors and transistors have been introduced. A summary of how electron bonding can give rise to semiconducting properties of organic molecules has been given, along with a brief history of organic

semiconductors. The operation of field-effect transistors, and a brief account of the history of OTFT research have been summarised. Dielectric surface treatments affecting OTFT performance have been outlined, and finally a short overview of recent research into organic semiconductors and OTFTs has been given.

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3

Thin Film Technologies

3.1 Introduction

This chapter gives a brief introduction to the properties of thin films, and mainly concentrates on their formation techniques. The techniques relevant to this work are described and other deposition techniques are summarised. Thin film transistors and their fabrication techniques are discussed in Chapter 2.

3.2 Thin films

Historically, the physical dimension of thickness was used to draw a distinction between thin and thick films — the boundary was commonly taken at 1 μm [1]. More appropriately, films are classified as thin or thick depending on whether they exhibit surface-like or bulk-like properties. Some thin films, for example, have a strength of around 200 times that of the annealed bulk sample, and several times that of cold worked material. Electrically, as a metal film thickness becomes of the same order as the electron mean free path, the effective conductivity is reduced due to scattering of electrons at the film surface [2].

Thin films are used in many fields, for example: optical reflective and anti-reflective coatings; electronic devices like capacitor dielectrics or field effect transistors; hard coatings for cutting tools; and corrosion-resistant coatings [1].

3.3 Thermal oxidation

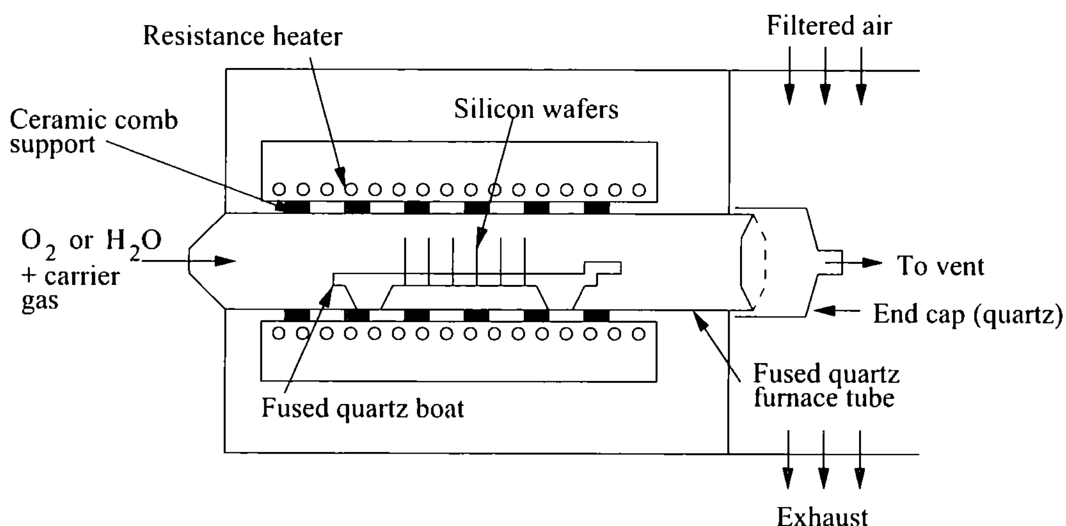
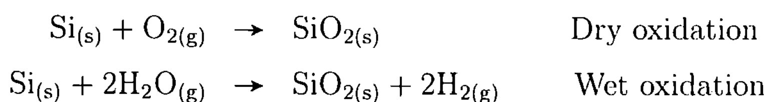


Figure 3.1: Basic thermal oxidation setup [3].

The thermal oxidation of silicon is a key step in the fabrication of silicon semiconductor devices. It is also commonly used in the fabrication of OTFTs as the silicon and silicon oxide provide a very good combination of gate and gate dielectric. A basic thermal oxidation setup is shown in figure 3.1. The silicon wafers are held vertically in a quartz boat and are subjected to a flow of pure dry oxygen, or water vapour, at a temperature of 900–1200°C. The following reactions describe the thermal oxidation of silicon in oxygen or water vapour:



$$Si_{(s)} + O_{2(g)} \rightarrow SiO_{2(s)} \qquad \text{Dry oxidation}$$

$$Si_{(s)} + 2H_2O_{(g)} \rightarrow SiO_{2(s)} + 2H_{2(g)} \qquad \text{Wet oxidation}$$

Oxides grown in dry oxygen have the best electrical properties; however considerably more time is required to grow the same oxide thickness at a given temperature in dry oxygen than in water vapour. The oxides used in this work were of the order of 100 nm in thickness, and therefore were grown using dry oxidation.

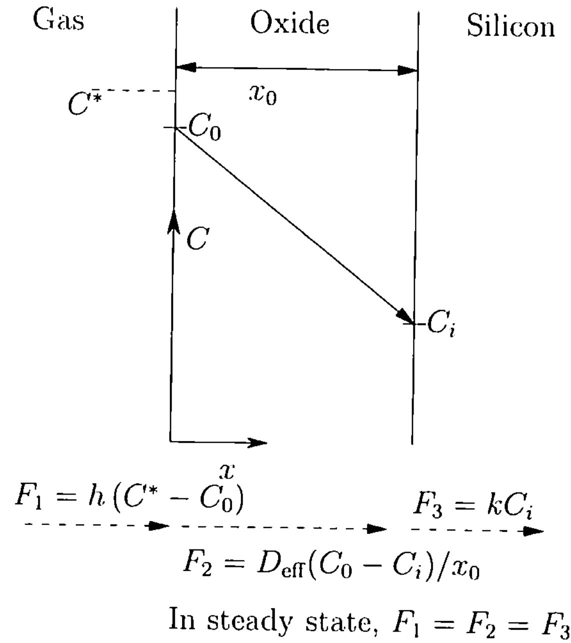


Figure 3.2: Model for the oxidation of silicon (adapted from [4]).

The Si/SiO_2 interface moves into the silicon during the oxidation process — this creates a fresh interface region, with any surface contamination on the original silicon ending up on the oxide surface [3].

The Deal-Grove model [4] describes mathematically a general relationship for the thermal oxidation of silicon. Figure 3.2 shows a model of an Si/SiO_2 interface and surface, with an oxide thickness x_0. The oxidant must go through the following stages:

1. It is transported from the oxidising gas to the outer surface where it reacts or is adsorbed.

2. It is transported across the oxide film towards the silicon.

3. It reacts at the silicon surface to form a new layer of SiO_2.

The model further assumes that the fluxes of oxidant in the above steps are identical (i.e. a steady state has been reached).

The flux of oxidant from the gas to the vicinity of the outer surface is

$$F_1 = h\,(C^* - C_0) \tag{3.1}$$

where h is a gas-phase transport coefficient, C_0 is the concentration of the oxidant at the outer surface of the oxide at any given time and C^* is the equilibrium concentration of the oxidant in the oxide. C^* can be related to the partial pressure of the oxidant in the gas by Henry's Law*:

$$C^* = Kp \tag{3.2}$$

The flux of oxidant across the oxide layer is given by Fick's First Law of Diffusion†:

$$F_2 = -D_{\text{eff}}\frac{\mathrm{d}C}{\mathrm{d}x} \tag{3.3}$$

at any point x within the oxide layer, where D_{eff} is the effective diffusion coefficient and $\mathrm{d}C/\mathrm{d}x$ is the concentration gradient of the oxidant in the oxide. In the steady state, F_2 is constant at any point in the oxide film (i.e. $\mathrm{d}F_2/\mathrm{d}x = 0$). Consequently, the concentration of the oxidant is linear, and therefore the flux is

$$F_2 = D_{\text{eff}}\frac{C_0 - C_i}{x_0} \tag{3.4}$$

where x_0 is the thickness of oxide at a given time, and C_0 and C_i are the concentrations of oxidant in the oxide at the oxide surface and Si/SiO_2 interface, respectively. The coefficient D_{eff} incorporates effects of space charges due to ionic transport species — it has been shown that if oxide thickness is large enough compared to the space-charge regions, D_{eff} is approximately twice the actual diffusion coefficient [4, 6]. At the Si/SiO_2 interface, the oxidation rate is proportional to the concentration of the oxidant, so the flux is given by

$$F_3 = kC_i \tag{3.5}$$

*At a constant temperature, the amount of a given gas dissolved in a given type and volume of liquid is directly proportional to the partial pressure of the gas in equilibrium with that liquid

†The particle flow per unit area is directly proportional to the concentration gradient of the particle [5]

where k is the rate constant for the oxidation reaction.

Due to the steady-state condition, $F_1 = F_2 = F_3$. Using equations 3.4 and 3.5, C_i can be eliminated so the flux becomes

$$F = \frac{D_{\text{eff}} C_0}{x_0 + D_{\text{eff}}/k} \tag{3.6}$$

The rate of oxide growth is given by the flux divided by the number of molecules, N, of the oxidant that are incorporated per unit volume of the oxide layer, so

$$\frac{\mathrm{d}x_0}{\mathrm{d}t} = \frac{F}{N} = \frac{D_{\text{eff}} C_0}{N\left(x_0 + D_{\text{eff}}/k\right)} \tag{3.7}$$

At a time $t = 0$, $x_0 = x_i$, which corresponds to the initial thickness of oxide on the surface of the wafer, this gives

$$x_i^2 + A x_i = B\tau \tag{3.8}$$

or

$$t = \frac{x_0^2}{B} + \frac{x_0 A}{B} - \tau \tag{3.9}$$

$$\Rightarrow \quad x_0^2 + x_0 A = B\left(t + \tau\right) \tag{3.10}$$

where $A \equiv 2D_{\text{eff}}/k$, $B \equiv 2D_{\text{eff}}C_0/N$, and $\tau \equiv x_i^2/B + Ax_i/B$.

This leads to the solution

$$x_0(t) = 0.5A\left[\left\{1 + \frac{4B}{A^2}\left(t + \tau\right)\right\}^{\frac{1}{2}} - 1\right] \tag{3.11}$$

For short times, with $(t + \tau) \ll A^2/4B$

$$x_0(t) = \frac{B}{A}\left(t + \tau\right) \tag{3.12}$$

Oxide growth is proportional to time, and the ratio B/A is called the linear (growth) rate constant. The growth rate is limited by the reaction at the silicon interface.

For long times, where $t \gg A^2/4B$ and $t \gg \tau$

$$x_0(t) = \sqrt{Bt} \quad (3.13)$$

Oxide growth is proportional to the square root of time, and B is the parabolic rate constant. The growth rate is limited by the diffusion through the existing layer.

Both the parabolic and linear rate constants have a temperature dependence of the form of an Arrhenius relationship:

$$D = D_0 \exp\left(\frac{-E_A}{kT}\right) \quad (3.14)$$

where E_A is the activation energy for the reaction.

Experimentally, measured results agree with this model over a wide range of oxidation conditions [3, 4, 6, 7].

3.4 Deposition techniques

There exist a number of methods of forming or depositing thin films. Methods that have been used for the work contained in this thesis are described in the following sections, while section 3.4.6 gives a brief outline of other deposition methods.

3.4.1 Vacuum sublimation / thermal evaporation

Vacuum sublimation, or thermal evaporation, is a common deposition technique for depositing metals and small organic molecules. A schematic diagram of a vacuum evaporation system is shown in figure 3.3.

The first evaporated thin films were probably the deposits that Faraday obtained by exploding gold wires in atmospheres of oxygen and hydrogen [9]. Further experimentation in the 19th century was stimulated by interest in the optical phenomena associated with thin films. For a number of decades evaporated thin films were only the domain of academic interest until the

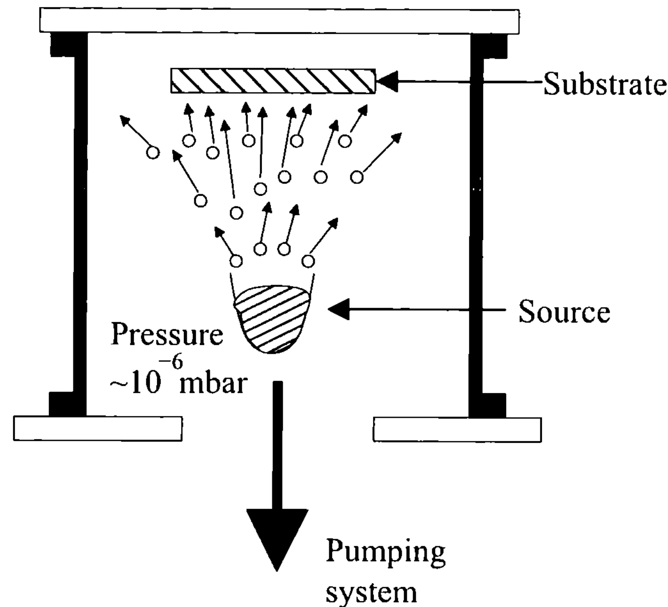


Figure 3.3: Schematic diagram of a thermal evaporation system (from [8]).

development of vacuum equipment had progressed enough to allow large-scale applications and control of film properties [10].

Although vacuum evaporation is referred to as a single process, it consists of several distinguishable steps, which are outlined below.

Evaporation of source material

The first step is the transition of a condensed phase, either solid or liquid, into the gaseous state. This may be treated as a macroscopic or atomistic phenomenon: the macroscopic approach is based on thermodynamics; the latter on kinetic theory of gases.

In thermodynamics, the condensed and gaseous states of materials are characterised by functions dependent on pressure, temperature, volume and mass. In a state of thermodynamic equilibrium, the condensed and gaseous states exist at the same temperature and in contact with each other without undergoing net changes — i.e. the amounts of evaporating and condensing material are equal. Under these conditions, solids and liquids have characteristic vapour pressures which are functions of temperature.

The transformation of a condensed phase into vapour involves the conversion of thermal energy supplied to the evaporant into mechanical energy as represented by the expansion into vapour. This thermal energy may be supplied in a number of ways. Resistive heating, often of a tungsten filament or boat, is used to deposit metals and a number of small organic molecules. This method is not particularly efficient as it generally heats up a larger area of the holder than is in contact with the evaporant — i.e. a lot of the heat is wasted. In an electron-beam deposition system, a stream of electrons is accelerated through a high voltage (5–10 kV) and focused on the evaporant surface. Most of the electrons' kinetic energy is converted into heat and temperatures exceeding 3000°C may be obtained [10]. Since the energy is concentrated on an area of the surface of the evaporant, the rest of the evaporant can be maintained at a lower temperature, thus reducing interactions between the evaporant and support materials.

According to the Second Law of Thermodynamics, the conversion of thermal to mechanical energy is limited because a fraction must go to increasing system entropy. This conversion is most efficient if the change occurs reversibly. The most common way of expressing the energy balance of reversible phase transitions is

$$\Delta G = \Delta H - T\Delta S \tag{3.15}$$

where G is the Gibbs' Free Energy, H the enthalpy, T the temperature, and S the entropy associated with the process. ΔG constitutes a quantitative measure for the driving force associated with a system change from one state to another: knowledge of ΔG thus makes it possible to determine the stability of one state relative to another. If there is no driving force, two states are at equilibrium, so by stipulating $\Delta G = 0$, the values of the macroscopic variables can be derived. In the case of a pure condensed phase in contact with its own vapour, the resulting relationship defines the equilibrium pressure of a material as a function of temperature.

The Clausius-Clapeyron Equation[‡] describes the change in equilibrium vapour pressure with temperature for a system:

$$\frac{\mathrm{d}p}{\mathrm{d}T} = \frac{H_g - H_c}{T\left(V_g - V_c\right)} \tag{3.16}$$

where p is the equilibrium vapour pressure and V the molar volume, and the subscripts c and g denote condensed and gaseous phases, respectively. To solve this, it is assumed that V_c can be neglected because it is very small compared to V_g, and the vapour is assumed to be an ideal gas. $H_g - H_c$ is the molar heat of evaporation, $\Delta_e H$. Replacing V_g using the ideal gas law[§] the equation becomes

$$\frac{\mathrm{d}p}{p} = \frac{\Delta_e H \mathrm{d}T}{\mathrm{R}T^2} \tag{3.17}$$

where R is the universal gas constant. This can be integrated to give

$$\ln p \approx \frac{\Delta_e H}{\mathrm{R}T} + \text{constant} \tag{3.18}$$

If the evaporation is treated as an atomistic phenomenon, based on the kinetic theory of gases, then a number of properties of the evaporant can be described, such as the rate of evaporation and the directionality of evaporating molecules. A full derivation can be found in [10, Chapter 1].

The Hertz-Knudsen equation gives the most general form for the evaporation rate equation:

$$\frac{\mathrm{d}N_e}{A_e \mathrm{d}t} = \alpha_v \left(2\pi m k T\right)^{-\frac{1}{2}} \left(p^* - p\right) \tag{3.19}$$

which described the number of molecules, $\mathrm{d}N_e$, evaporating from a surface area A_e during a time $\mathrm{d}t$. This is equal to the impingement rate of molecules on a surface, $(2\pi mkT)^{-1/2}p$, with the pressure p replaced with the equilibrium vapour pressure p^* minus the hydrostatic pressure p of the evaporant in the gas phase. T is the temperature of the material, m the mass of a molecule of material and k is Boltzmann's constant. α_v is introduced to relate the observed

[‡] A derivation is given in [10] and is therefore not reproduced here

[§] $pV = nRT$; however, as molar volumes are being used, n, the number of molecules, is taken as part of the volume term; hence $pV_g = RT$

evaporation rate with the theoretical evaporation rate ($\alpha_v = 1$). The rate is reduced due to a certain number $(1-\alpha_v)$ of vapour molecules that contribute to the evaporant pressure but not to the net molecular flux from the condensed to the vapour phase — Knudsen argued this was due to molecules on the evaporating surface being reflected back into the gas rather than incorporated into the liquid. The theoretical maximum evaporation rate occurs when $p = 0$ — i.e. no evaporating molecules return to the surface.

The mass evaporation rate from a solid (derived by Langmuir in 1913 [11]) is given by multiplying the molecular evaporation rate by the mass of an individual molecule, thus giving the Langmuir expression

$$\Gamma = m\frac{\mathrm{d}N_e}{A_e\mathrm{d}t} = \left(\frac{m}{2\pi kT}\right)^{\frac{1}{2}} p^* \tag{3.20}$$

Material transport from source to substrate

Because of collisions with ambient gas atoms, a fraction of the vapour atoms will be scattered. From kinetic theory, the mean free path λ[¶] of gas atoms is given by

$$\lambda = \frac{kT}{p\pi d^2\sqrt{2}} \tag{3.21}$$

where d is the diameter of the molecules. Thus as the pressure is reduced, the mean free path increases. For common gases (O_2, N_2, etc.) the mean free path is approximately 0.1 µm at atmospheric pressure, 10 cm at 10^{-3} mbar, and 100 metres at 10^{-6} mbar [10, 12]. Since collisions are statistical events, the actual free paths vary: the distribution of these is given by the exponential decay function

$$\frac{N}{N_0} = \exp\left(\frac{-l}{\lambda}\right) \tag{3.22}$$

where N/N_0 is the fraction of molecules which have not suffered a collision as yet after travelling a free path of length l. According to equation 3.22, 37% of all molecules traverse a distance at least as long as the mean free path without

[¶] The mean free path is the average distance molecules travel between collisions

being deflected — i.e. 63% of the molecules will have been deflected in a distance less than the mean free path. Thus, to keep collisions and deflections of the evaporant minimised between the source and substrate, the mean free path of the molecules must be considerably larger than the source-substrate distance.

Keeping a low pressure also reduces contamination from reactions between the source and residual atmosphere.

Deposition on the substrate

Figure 3.4 illustrates the various stages of film growth on a substrate. The substrate surface is covered with a number of adsorption sites and a molecule becomes bound to one of these with a characteristic energy. The adsorbed atoms may still re-evaporate or migrate to adjacent adsorption sites, or single atoms may combine with others. Once a group of atoms reaches a certain size, it is more likely to grow than decay: the formation of these stable 'islands' is known as nucleation. Individual 'islands' continue to grow by the addition of more single hopping atoms. Eventually, the 'islands' coalesce with their neighbours to form an interlinking network; the uncoated areas diminish until a single continuous film is formed. This may not occur until a large amount of material has been deposited (a thickness of a number of nm) [12].

The thickness of the deposited film will, depending on the geometry of the evaporating system, vary along the substrate. For a point source and plane substrate (illustrated in figure 3.5), the deposition rate varies as $(\cos\theta)/r^2$, where r is the radial distance of the substrate from the source and θ is the angle between the radial vector and the normal to the substrate. The derived equation, giving the film thickness d as a function of the distance from the central point of the substrate, l, is

$$\frac{d}{d_0} = \left[1 + \left(\frac{l}{h}\right)^2\right]^{\frac{3}{2}} \tag{3.23}$$

where d_0 is the film thickness at the central position on the substrate (where vapour condenses normally) and h is the normal distance of the point source

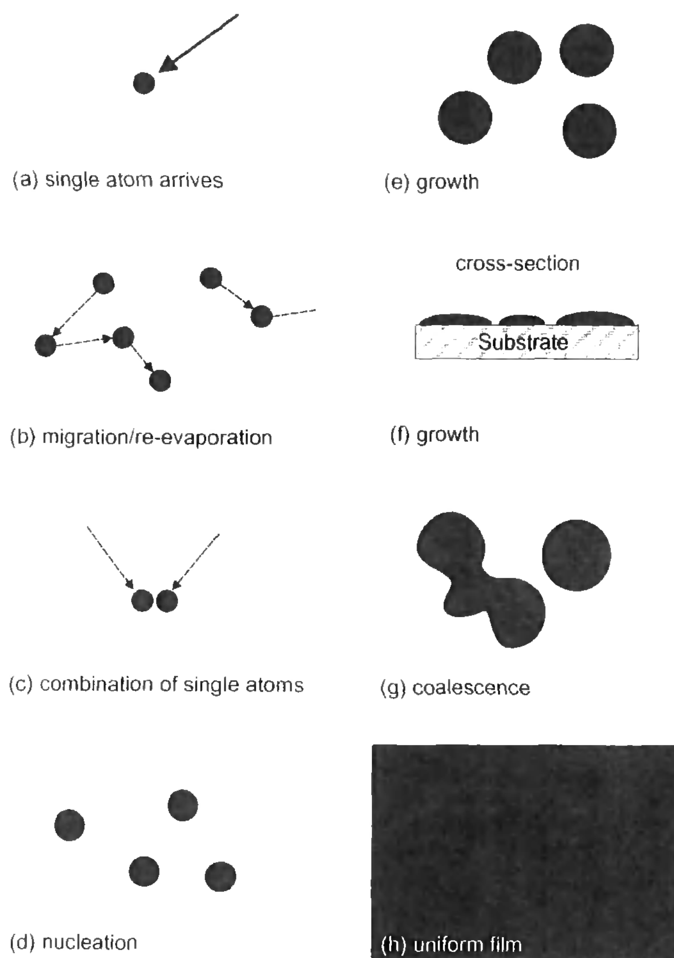


Figure 3.4: Stages of growth of a thermally evaporated film (taken from [12]).

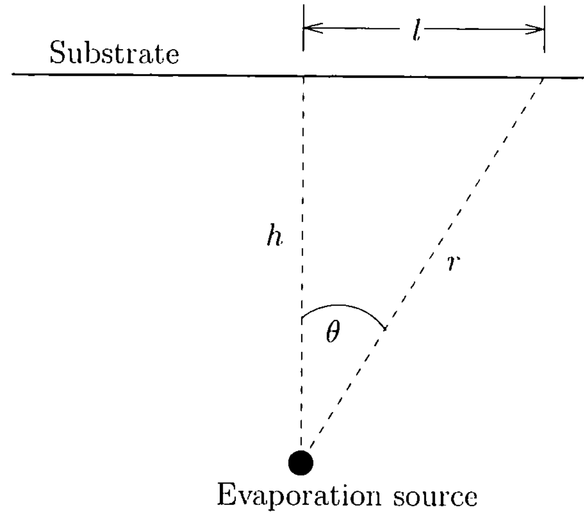


Figure 3.5: Evaporation geometry from a point thermal evaporation source onto a plane substrate (taken from [12]).

to the substrate. The effect of thickness variation can be minimised by using a larger area source [12].

The structure of an evaporated film will depend on a number of deposition parameters, outlined below. Evaporated films tend to follow the substrates on which they are evaporated, so any defects on the substrate would be reproduced in the film. The substrate temperature is one of the most important parameters in film growth — a higher substrate temperature provides more kinetic energy to the condensing molecules, so they have enough energy to move to a site of lower surface potential and form a preferred structure; it has been found that the crystal growth of pentacene is improved by keeping the substrate at an elevated temperature [13, 14]. However, at much higher substrate temperatures, re-evaporation may occur. With a faster deposition rate, the higher arrival rate of atoms on the substrate means there are many atoms moving across the surface and and nucleation rate is high; thus films deposited quickly tend to have a smaller grain size than those deposited more slowly. At high rates, the films can become amorphous as the atoms do not have time to migrate across the substrate before being buried by other atoms. The variation of grain size with deposition rate (source temperature) is reported in section

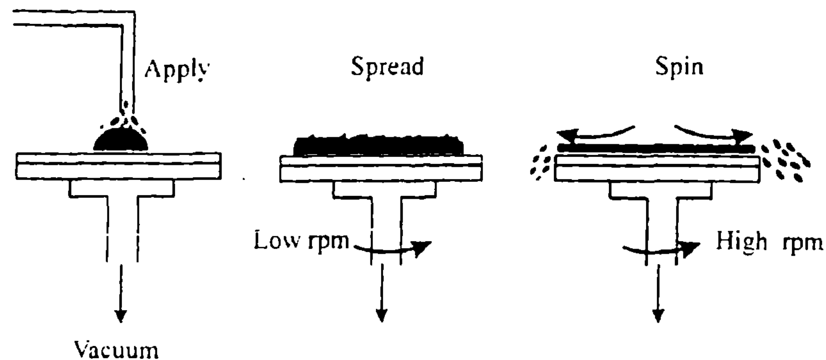


Figure 3.6: Schematic representation of spin-coating (taken from [8]).

5.2.3. The residual gas atmosphere in the chamber also has an effect on film quality — more residual gases give a greater chance of the gases being trapped in the formed film. Additionally, there is a greater chance that the evaporated molecules are deflected before they land on the substrate, or that a chemical reaction between the evaporant and the residual gases occurs [1].

3.4.2 Spin-coating

Spin-coating is a common technique in microelectronics and organic electronics, used to deposit a polymer film, initially dissolved in an appropriate solvent, onto a substrate (this technique is commonly used to deposit photoresist onto silicon wafers). Figure 3.6 outlines schematically the spin-coating procedure. Initially, a quantity of solution is applied to a substrate that is held onto the spin coater by means of a vacuum chuck. The substrate is then spun at a slow speed (around 250–500 rpm) to disperse the solution evenly onto the wafer. After this dispersion step, the substrate is accelerated to a high angular velocity (around 1000–6000 rpm), held at this speed for 10–60 seconds, and rapidly brought to rest. During the high-speed spin, centrifugal forces force the liquid radially outwards. Excess material is driven off the edge of the substrate, the remainder is retained as a thin surface layer by surface tension and viscous forces [15]. The film is normally then baked for a time (commonly between two and around twenty minutes) to drive off any residual solvent. Films pro-

duced using spin-coating are found to be very uniform in thickness, except at the periphery of the substrate.

A theoretical model for the process is described in [16]. This model assumes a Newtonian fluid (linear relationship between shear stress and shear rate) is rotating on an infinite plane. Coriolis forces and gravitational gradients are neglected [17]. Using cylindrical polar co-ordinates (r, θ, z) with origin at the centre of rotation, and the plane spinning at angular velocity ω, the z dependence of the radial velocity v of the liquid at any point (r, θ, z) can be found by equating the viscous and centrifugal forces per unit volume so that

$$-\eta\frac{\partial^2 v}{\partial z^2} = \rho\omega^2 r \tag{3.24}$$

where η is the viscosity of the liquid, ρ the liquid density, and v the velocity $v(z)$ in the $\vec{r}$ direction. Equation 3.24 can be integrated using the boundary conditions that $v = 0$ at the surface-liquid interface $(z = 0)$, and $\partial v/\partial z = 0$ at the surface of the film $(z = h)$ where the shearing force must vanish. Therefore

$$v = \frac{1}{\eta}\left(\frac{-\rho\omega^2 r z^2}{2} + \rho\omega^2 r h z\right) \tag{3.25}$$

The radial flow q per unit length of circumference is

$$q = \int_0^h v dz = \frac{\rho\omega^2 r h^3}{3\eta} \tag{3.26}$$

To obtain a differential equation for h, the equation of continuity is applied

$$r\frac{\partial h}{\partial t} = -\frac{\partial(rq)}{\partial r} \tag{3.27}$$

Thus, substituting in equation 3.26 results in

$$\frac{\partial h}{\partial t} = -K\frac{1}{r}\frac{\partial}{\partial r}\left(r^2 h^3\right) \tag{3.28}$$

where $K = \rho\omega^2/3\eta$.

In the case where h is independent of r (i.e. a uniform distribution of the film[||]), equation 3.28 becomes

$$\frac{\mathrm{d}h}{\mathrm{d}t} = -2Kh^3 \tag{3.29}$$

$$\Rightarrow h = \frac{h_0}{(1 + 4Kh_0^2 t)^{\frac{1}{2}}} \tag{3.30}$$

where the constant h_0, which is independent of r, corresponds to the initial height of a fluid layer. If t is large (i.e. $4Kh_0^2 t \gg 1$), then equation 3.30 reduces to:

$$h = \left[\frac{3\eta}{4\rho\omega^2}\right]^{\frac{1}{2}} t^{-\frac{1}{2}} \tag{3.31}$$

which shows that the film thickness is independent of the initial height of liquid on the substrate.

As the solution of equation 3.28 is uniquely determined when h is given at time $t = 0$, it follows that equation 3.30 is the solution corresponding to an initially uniform distribution $h = h_0$: thus, if the initial distribution of fluid is uniform, it will remain so with time, as the thickness is decreased. Equation 3.30 shows that a fluid layer decreases in thickness by a factor $1/\sqrt{2}$ in a time

$$\tau = \frac{1}{4Kh_0^2} \tag{3.32}$$

which shows that a thicker layer will reduce in height more rapidly than a thinner one. Thus any non-uniformity in the initial distribution would be removed as centrifugation continues. This is borne out by the general solution of equation 3.28, which can be found in [16].

The above derivation has assumed a Newtonian fluid. There has been work produced in deriving equations for non-Newtonian fluids: Acrivos *et al.* [18] have solved the general form of equations describing the flow of a power-law non-Newtonian fluid on a rotating disk.

[||]This is borne out by experimental evidence [15]

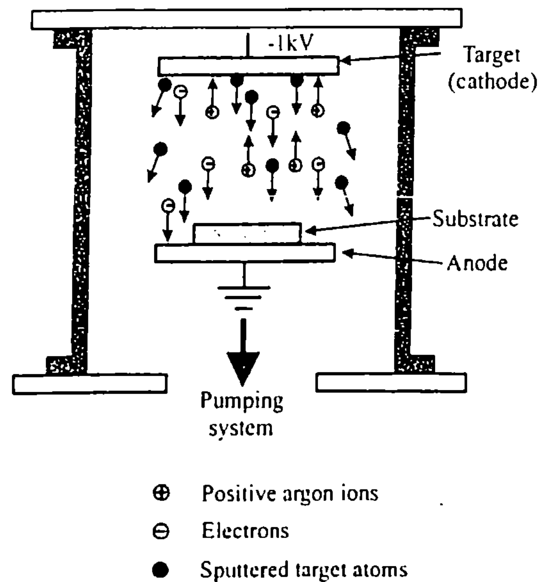


Figure 3.7: A schematic of a sputtering system (taken from [8]).

3.4.3 Sputter coating

Sputtering is based on the momentum exchange of accelerated ions incident on a target of source material [12]. This causes some of the surface atoms to be ejected from the target and end up deposited on any solid close to the target. Although sputtering was discovered in 1842 by W. R. Grove, and was used for depositing films as early as 1877, sputtering as a method for depositing thin films with controlled properties has only gained momentum since the 1950s [2].

A schematic of a sputtering system is shown in figure 3.7. The sputtering chamber is evacuated and filled with an inert gas (normally argon). A DC potential of several kV is applied between the target (cathode) and the anode, to which the substrate is attached. This potential difference causes the gas to ionise, and the positive ions are accelerated to the target and cause sputtering of the atoms, which end up deposited on the substrate.

The rate of sputtering can be increased by increasing the gas pressure, which causes the number of ions and discharge current to increase. However, as the pressure is increased, the atoms suffer more collisions and are prevented

from reaching the anode. Therefore, an optimum pressure needs to be found to balance the mean free path of the atoms and the sputtering rate — this has been found to be in the range of 25–75 mbar [12].

For sputtering insulating materials, a DC potential cannot be used due to the accumulation of positive surface charges on the target, thus stopping the gas ions from hitting the surface. In this case, an RF alternating current must be used.

The principal advantages of sputtering are that almost any material can be sputtered, and that because no heating is required, materials that are either difficult to evaporate, or would dissociate on heating, can be deposited [12].

Detailed descriptions of sputtering can be found in various books on thin films, e.g. Chapters 3 and 4 of [10], or Chapter 4 of [2].

3.4.4 Langmuir-Blodgett deposition

The Langmuir-Blodgett (LB) deposition technique involves the vertical movement of a solid substrate through the monolayer/air interface. In 1919, Irving Langmuir reported that a monomolecular oil film could be deposited on a glass surface by dipping the substrate into water covered with a monomolecular film (oleic acid), and slowly withdrawing the substrate [19]. Further work by Katharine Blodgett found that other oils could be made to adhere to glass substrates by applying a surface pressure to the film, and wetting the glass with acid or alkaline water [20]. Further developments made it possible to deposit multiple layers on glass and metals [21, 22].

The materials used in LB deposition are normally amphiphilic (possessing a hydrophilic head group and hydrophobic tail) [1]. Three different deposition methods are possible with LB deposition: X-type, where a monolayer is transferred on the downstroke only and molecules are aligned head-to-tail with the tail on the substrate; Z-type, where a monolayer is transferred on the upstroke only and molecules are aligned as with X-type, but with the head on the substrate; and Y-type, where a monolayer is deposited on each traversal of the monolayer/air interface, and the molecules stack in a head-to-head and tail-to-tail pattern [23].

3.4.5 Self-assembly and Layer-by-Layer deposition

Layer-by-layer deposition using the self-assembly technique is described in detail in a paper by Decher *et al.* [24]. In this technique, a positively charged planar surface is immersed in a solution containing an anionic polyelectrolyte. This causes a monolayer to be adsorbed onto the surface. Due to the high concentrations of polyelectrolyte, a number of ionic groups remain exposed to the interface with the solution, thus the charge is reversed. The substrate is then rinsed in water, and immersed in a solution containing a cationic polyelectrolyte. A monolayer this electrolyte is adsorbed, and hence the original charge is restored.

The steps can be repeated in a cyclic fashion, thus multilayer assemblies of the electrolytes can be built up on the substrate.

3.4.6 Other deposition techniques

A number of other deposition techniques exist, which are outside the scope of this thesis to describe fully. A list of a few extra deposition techniques with a short description is provided for the sake of completeness.

Inkjet printing is a useful deposition method for large areas of polymeric films. A solution of the polymer to be deposited replaces the ink in a standard (or very slightly modified) inkjet printer, and droplets of the polymer (of the order of a few pl per drop) are forced out of the nozzle. The physical properties of the polymer solution must be matched to a specific printer: the viscosity must be low enough to allow for rapid refilling of the nozzle, whilst the surface tension must be sufficiently high to hold the ink in the nozzle without dripping [12].

Sol-gel processing involves the suspension of a solid in a liquid, the removal of the liquid, and finally the densification of the solid [8]. This has been used to form highly dense films of ceramics and glasses. Sol-gel processing allows potentially higher purity and homogeneity compared with traditional glass melting or ceramic powder methods, and allows the processing to take place and much lower temperatures [25].

Electroplating is a common deposition method, having been known for at least a hundred years. The apparatus consists of an anode and a cathode immersed in a suitable electrolyte [10, Chapter 5]. As current is passed through the electrolyte, the anode material is deposited on the cathode. The mass deposited per unit area is given by the equation $M = JtE\alpha$, where J is the current density, t is the deposition time, E is the electrochemical equivalent (from the second law of electrolysis), and α is the current efficiency, which is the ratio of the experimental to theoretical weight deposited. Some metals cannot be deposited in an aqueous electrolyte, as other (non-deposition) reactions are more probable. This can sometimes be avoided by the use of non-aqueous media, for example molten baths of metal salts.

Anodisation is a similar technique to that of electroplating, but, rather than the anode metal ionising and depositing on the cathode, oxidation occurs on the anode (through reaction with water), resulting in a film of anodic oxide. The increasing resistance as the oxide grows causes a continuous decrease in the electrolytic current [8], therefore the thickness can be controlled by applying a constant voltage and letting the current reduce to a negligible value. Anodisation is a useful technique for forming protective coatings over an underlying metal to protect it from atmospheric oxidation or chemical corrosion, and for creation of dielectrics (e.g. tantalum oxide for use in capacitors) [2, Chapter 5].

Electroless plating was invented by A. Brenner and G. E. Riddell in 1946 who were attempting to electrodeposit a nickel-tungsten alloy on the inside of a tube [2, Chapter 1]. To decrease the extent of anodic oxidation, they added a hypophosphite to the bath, and placed the anode inside the tube. This led to the plating of the tube both inside and out, even without any electric current. It had then been found that materials that do not normally accept electroless plating, were able to do so if washed in a palladium chloride solution. This technique permits plating on selected areas and inside holes where electroplating is accomplished with difficulty.

Chemical reduction is used to deposit metals without involving electrode potentials. A substrate is is placed into a solution of the metal salt, and the metal is precipitated out by the use of a reducing agent. This technique is

commonly used for silvering mirrors: the silver is in an ammoniacal solution of silver nitrate, and is subsequently precipitated by the addition of a reducing agent such as sugar, sodium potassium tartrate, or formaldehyde [2, Chapter 1].

Chemical Vapour Deposition (CVD) is based on the decomposition and/or radical generation of chemical species [26, Chapter 11]. The desired material is deposited directly from the gas phase onto the surface of the substrate. CVD systems can operate at atmospheric pressure, often used for deposition of the silicon dioxide passivation layer in integrated-circuit processing; as hot-wall, low-pressure systems (LPCVD), commonly used to deposit polysilicon, silicon dioxide and silicon nitride; and in a plasma reactor: the primary advantage of the plasma-enhanced CVD (PECVD) process is that the formation of the plasma permits the reaction to take place at low temperatures [5, Chapter 6].

Atomic Layer Deposition (ALD), or Atomic Layer Epitaxy (ALE) is a modification of the CVD technique. Reactant vapours are let into the deposition chamber as alternating pulses; between these pulses, the chamber is purged using an inert gas. ALD relies on the fact that all the process steps are saturative — i.e. a tightly-bound monolayer is chemisorbed on the surface, and the purging steps remove the excess molecules from the chamber. Thus the next gas will only encounter the surface monolayer with which it reacts. ALD allows for accurate and simple film thickness control, uniformity over large areas, and high film qualities at relatively low temperatures [27].

Ion plating [28] is a deposition method where the substrate is made a high voltage sputtering cathode, while the metal to be deposited is evaporated from a suitable filament, as in thermal evaporation techniques. An inert gas plasma is contained in the plating chamber, between the source and substrate — the plasma, along with the cathode, acts as a sputtering system, and hence is able to remove surface contaminants and barrier layers before film deposition. For a film to form, it is necessary for the deposition rate to exceed the sputtering rate: in materials that do not sputter easily (such as aluminium), this problem is not important; for other materials (such as gold), the problem matters and deposition parameters need to be appropriately controlled [10].

Epitaxy describes the growth technique of arranging atoms in single-crystal fashion upon a crystalline substrate so that the lattice structure of the newly grown film duplicates that of the substrate [29, Chapter 1]. This allows extremely pure films to be grown whilst being able to control dopant levels. The three types of epitaxial processes are vapour-phase (VPE), in which the crystal film is deposited from a gas (in the case of silicon growth, the gas is silicon tetrachloride in hydrogen); liquid-phase (LPE), in which a crystal film is deposited from the liquid phase: this allows depositions of different materials on the same substrate, and therefore can be used to make heterojunctions (e.g. Ge-Si, GaAs-GaP); and molecular beam epitaxy (MBE), in which crystal growth is achieved in an ultrahigh vacuum environment ($< 10^{-8}$ mbar) through the reaction of multiple molecular beams with a heated single-crystal substrate. Although MBE is a very slow process (around 1 monolayer/second), it allows very fine control over the composition of the crystal film, and considerably better structural resolution in the direction of growth compared to VPE and LPE.

3.5 Summary

A brief introduction to thin films has been given. Formation methods of thin films that have been used in this work have been described; other formation methods have been summarised.

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4

Experimental Methods

4.1 Introduction

This chapter provides a description of the techniques used for fabricating and characterising the semiconducting materials and complete devices. Sections 4.2 and 4.3 describe the fabrication process for the transistors used in this work. Deposition methods for the dielectric, semiconductor and contacts have been described in section 3.4. Sections 4.4 and 4.5 outline the techniques used for the optical, physical and electrical characterisation of the devices.

4.2 Device Fabrication

This section describes the methods for fabricating devices. The precise steps to make individual devices are given in chapters 5, 6 and 7. All the work was undertaken in a class 1000 clean room.

4.2.1 Substrate preparation

For electrical and physical characterisation of the organic semiconducting material, glass microscope slides were used as substrates. For electrical characterisation of the transistors, highly doped 111-orientation and 110-orientation silicon wafers, purchased from Siltronix (prime grade, single-side polished), of resistivity around 10^{-3} Ωcm, were used.

In both cases, the substrates were cleaned in peroxymonosulphuric acid (Caro's acid) for 30 minutes to remove any organic residues, and then rinsed thoroughly in deionised water. The acid was prepared by reacting hydrogen peroxide with sulphuric acid in a 1:1 ratio:

$$H_2O_2 + H_2SO_4 \rightleftharpoons H_2SO_5 + H_2O$$

As this is a strong oxidising agent, a thin layer of oxide is formed on the silicon wafer [1]; this was removed by placing the wafers in 4% hydrofluoric acid until the surface was rendered hydrophobic.

4.2.2 Dielectric preparation

Oxidisation

Silicon dioxide dielectrics were prepared using dry thermal oxidation. A temperature profile for the furnace was obtained, and the results are shown in figure 4.1.

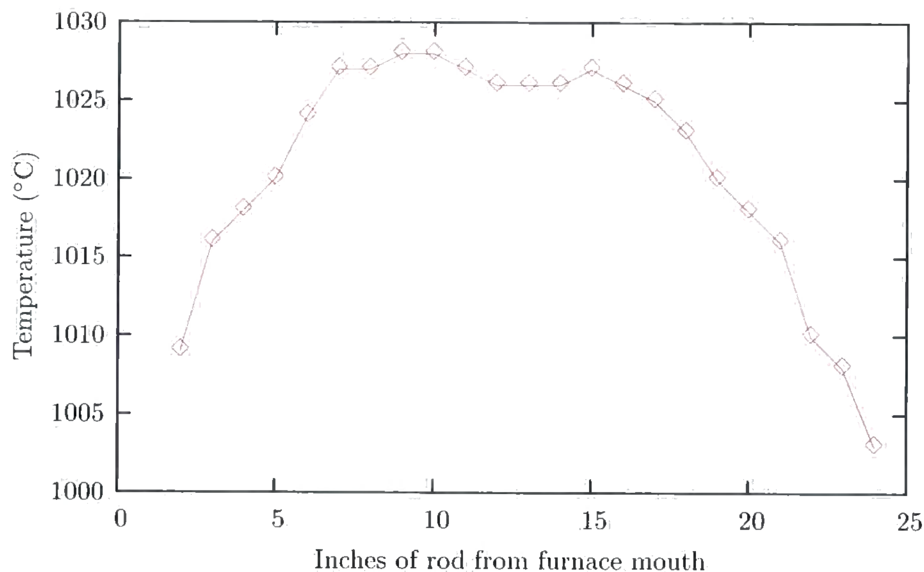


Figure 4.1: Furnace temperature profile at nominal temperature of 1030°C.

Freshly cleaned silicon wafers were placed into the mouth of a furnace heated up to 1050–1060°C under 2 l/minute nitrogen gas flow for 10 minutes.

The wafers were pushed to the centre of the temperature 'flat zone' of the furnace and left for a further ten minutes. The nitrogen flow was then turned off, and oxygen was let into the furnace at a flow rate of 3 l/minute for the duration of the oxidation (around 90–100 minutes). Once the time had elapsed, the oxygen flow was turned off, the nitrogen flow restored, and the furnace allowed to cool to its standby temperature of 620°C. After a further 15 minutes, the wafers were removed from the furnace.

This process resulted in SiO_2 thicknesses of around 120–130 nm, as measured by ellipsometry.

To improve transistor mobilities, the silicon oxide surface was treated with a silanising agent (see section 2.6). Two alternative silanising methods were used: in one, the wafer was placed in a solution of 2% DMDS in 1,1,1-trichloroethane (supplied by VWR) until the surface was rendered hydrophobic; in the other, HMDS (98%, supplied by Acros Organics) was coated on the wafer for approximately one minute, then spun off and the wafer rinsed under deionised water.

Spin coating

Polymethylmethacrylate (PMMA) dielectrics were spin-coated using a Laurell Technologies WS-400B-6NPP/LITE spin-coater. A solution of 2.5% PMMA (secondary standard grade, supplied by Sigma-Aldrich), molecular weight 93K, in anisole (supplied by Chestech) was prepared, and placed onto a clean silicon wafer. The wafer was initially spun at 500 rpm for five seconds for initial PMMA dispersal, followed by a spin at a higher speed for 30 seconds to reduce the PMMA to the desired thickness. The wafer was then baked at 120°C for two minutes to cure the PMMA.

Sputter coating

Hafnium Oxide (HfO_2) dielectrics were deposited on silicon wafers (both freshly cleaned and with a ~5nm SiO_2 film) using a Mantis Deposition Ltd. sputter coater. The deposition chamber was evacuated to a pressure of around 3×10^{-5} mbar, at which time 60.8 standard cubic centimetres/minute (sccm) of argon

gas, and 1 sccm of oxygen gas was let into the chamber: this resulted in a deposition pressure of around 8×10^{-3} mbar. The substrate was heated to 200°C or 300°C, and slowly rotated to ensure a more even deposition across the surface. A plasma was created using a 250W RF power source which allowed the HfO_2 to be deposited from the target to the substrate at a rate of 0.05 – 0.07 Å/s.

The hafnium oxides were deposited at the National Technical University of Athens, as part of a collaborative project between the NTUA and the University of Durham.

4.2.3 Semiconductor deposition

The organic materials were deposited by thermal evaporation onto substrates held at room temperature using an Edwards Auto306 evaporator (shown in figure 4.2). The materials were evaporated from a ceramic resistively-heated oven, with a working range of up to 500°C. The chamber was evacuated to a pressure of less than 10^{-6} mbar, then approximately 30 nm of the material was deposited at a rate of around 0.05–0.1 nm/s, as measured using a quartz crystal sensor connected to an Edwards FTM7 film thickness monitor.

4.2.4 Contacts

To form the source and drain contacts, 30–40 nm gold was evaporated onto the semiconducting layer using an Edwards 306 thermal evaporator, through a Kapton shadow mask mounted on a brass plate, at a pressure of around 5×10^{-6} mbar. The mask is shown in figure 4.3. The deposition rate and film thickness were monitored by a quartz crystal sensor connected to an Edwards FTM7 film thickness monitor.

A gate contact was made to the silicon wafer by removing oxide from the back of the wafer, and using conductive silver paste to attach aluminium foil to the wafer.

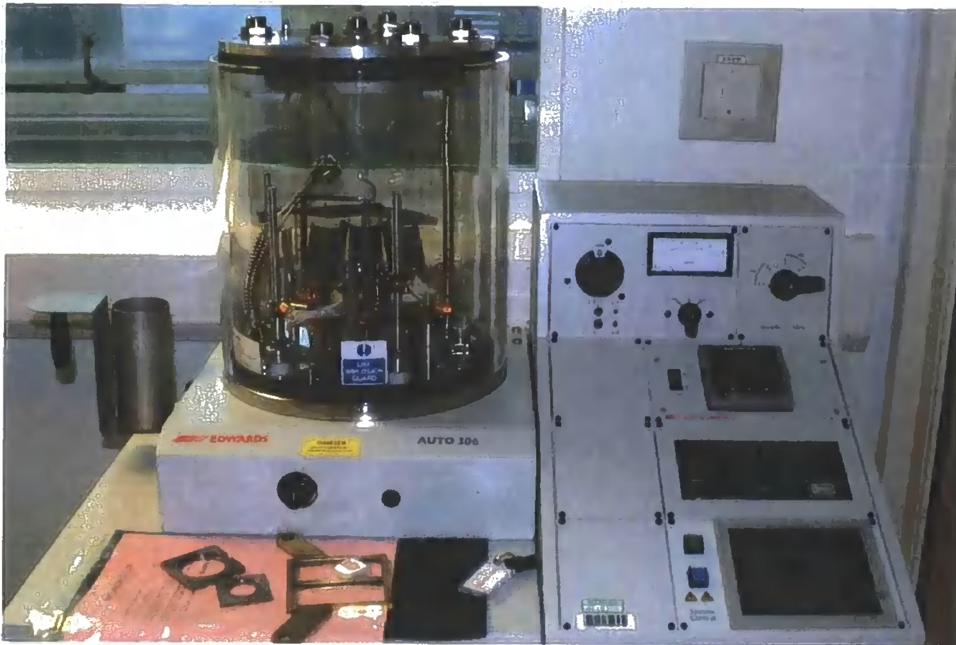


Figure 4.2: Photograph of Edwards Auto306 evaporator.

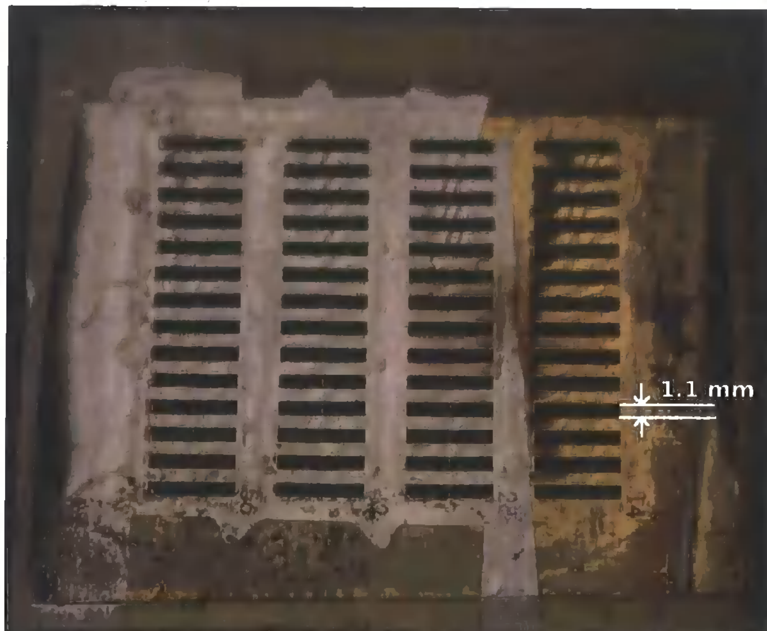


Figure 4.3: Shadow mask for patterning a set of transistor devices (channel length of 50 µm and width of 1.1 mm).

4.2.5 Lithography

Experiments using lithographic techniques are described fully, where relevant, in chapter 5. An overview of lithographic processing is given here for the sake of completeness.

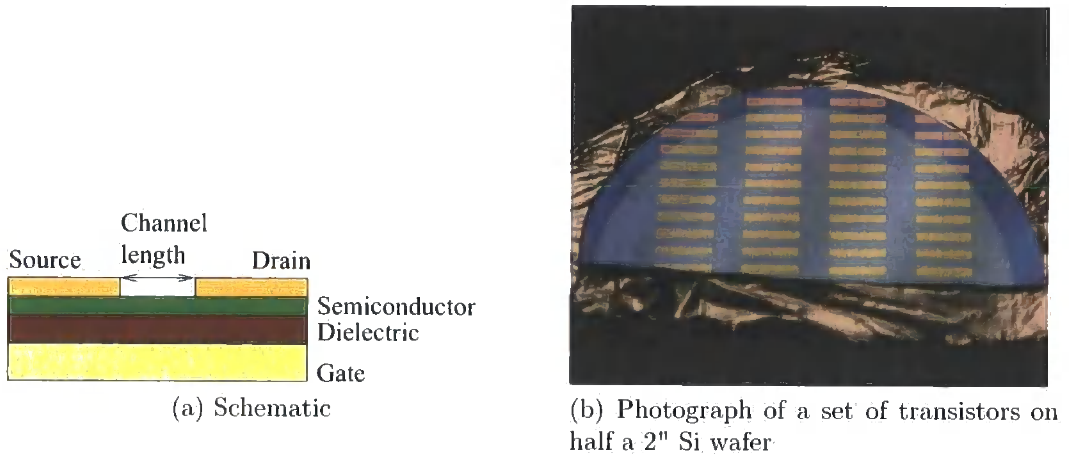
Shipley S1813 photoresist was applied onto the surface of a freshly oxidised wafer, and then spun at 500 rpm for 5 seconds for initial dispersal, followed by a spin at 3700 rpm for 30 seconds to obtain the desired thickness of resist. The wafer was baked at 95 °C for 2 minutes to soft-bake the resist. The resist was exposed to UV light for 10 seconds, through a mask, using a Karl-Süss 401000 mask aligner, and then developed using Microposit 351 developer, in a 1:3 ratio of developer to deionised water. After any further processing on the patterned wafer, the remaining resist was stripped off using acetone, followed by a rinse in propan-2-ol and deionised water.

4.2.6 Plasma etching

After stripping the photoresist, some oxide surfaces were subject to an oxygen plasma treatment. This was performed in a YES-500 plasma etcher, using a partial pressure of 1.6 mbar and a delivered power of 200 W. The substrates were placed on a floating electrode and subjected to the plasma for 17 minutes.

4.3 Standard device layout

Figure 4.4a shows a schematic representation of the transistors fabricated for this work. These were fabricated in a top-contact configuration: the semiconductor was deposited on top of the dielectric, and source-drain contacts were evaporated on top of the semiconductor through a contact mask. This resulted in contacts with a channel length of 50 μm and width of 1.1 mm. The silicon wafer was used as a common gate for all the devices. Figure 4.4b shows a photograph of a finished device.



(a) Schematic

(b) Photograph of a set of transistors on half a 2" Si wafer

Figure 4.4: Schematic and photograph of transistor.

4.4 Physical characterisation

4.4.1 Ellipsometry

Ellipsometry uses the change in the state of polarisation of light reflected from a substrate to measure, non-destructively, the thickness and refractive index of films [2, Chapter 11]. A schematic representation is shown in figure 4.5. The change in polarisation is dependent on the optical constants of the substrate, the angle of incidence of the light source, the optical constants of the film, and the film thickness. The thickness, therefore, can be determined by knowing or otherwise measuring the other parameters.

To measure film thicknesses, a Rudolph Research AutoEL-IV ellipsometer was used. The monochromatic light source was generated using a white light source, and a filter, allowing wavelengths of 632.8 nm, 546.1 nm, or 405.0 nm to be used. Most of the film thicknesses reported in this work were measured at 632.8 nm.

4.4.2 Absorption Spectroscopy

Absorption spectroscopy measures the amount of light absorbed by a material across a range of wavelengths. The intensity of light passing through an absorbing material is reduced according to the Beer-Lambert Law [4]:

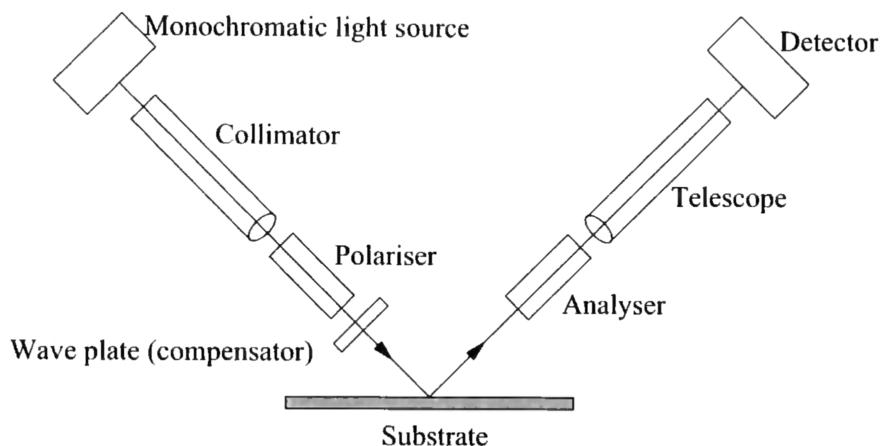


Figure 4.5: Schematic representation of an ellipsometer. [3]

$$I = I_0 10^{-\alpha l c} \qquad \alpha = \frac{4\pi k}{\lambda} \tag{4.1}$$

where I is the intensity of light after passing through the material, I_0 is the intensity of the incident light, l is the distance the light travels through the material, c is the concentration of absorbing species in the material, α is the absorption coefficient of the absorber, and k is the extinction coefficient. Equation 4.1 is often written as

$$A = \log_{10}\left(\frac{I_0}{I}\right) \tag{4.2}$$

where $A = \alpha l c$ is the absorbance of the sample.

The optical absorption spectra were measured using a Perkin-Elmer Lambda 19 UV / VIS / NIR spectrophotometer. The spectrophotometer's light source emitted a beam in the wavelength range 300 nm to 900 nm, with the absorption measured at each wavelength in steps of 1 nm. A baseline was recorded using two clean glass slides in the reference and measurement beam. The slide in the measurement beam was replaced with the sample-coated slide, while the slide in the reference beam remained for background correction.

4.4.3 Atomic Force Microscopy

An atomic force microscope allows detailed surface profiles to be obtained. Figure 4.6 illustrates the principles of operation.

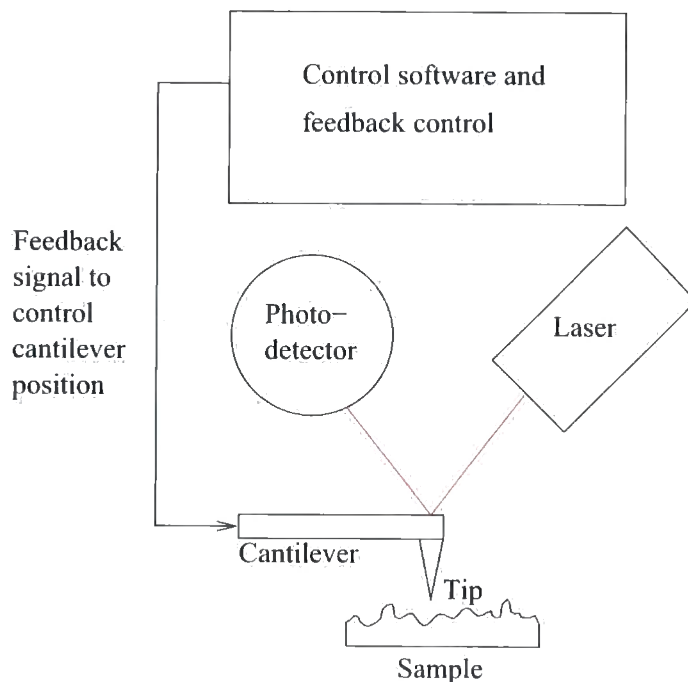


Figure 4.6: Schematic diagram of an AFM [5].

A Veeco Digital Instruments Dimension 3100 AFM was used to produce surface scans for film morphologies. The AFM consists of a sharp tip attached to a cantilever [6]. As the tip approaches the surface of the material, forces between the surface and the tip cause the cantilever to deflect — this deflection is measured by the reflection of the laser moving relative to the photodetector. A feedback loop is used to keep the tip from crashing into the sample surface by keeping the tip a certain distance from the surface. In contact mode, the force between the tip and the surface is kept constant during scanning by maintaining a constant deflection. In TappingMode™, the cantilever is driven to oscillate near its resonant frequency [7]. When the tip approaches the surface, the amplitude of the oscillation changes; the height of the cantilever is adjusted to maintain a set oscillation amplitude, and can therefore be used to image a surface without coming into contact with it, thus soft surfaces that

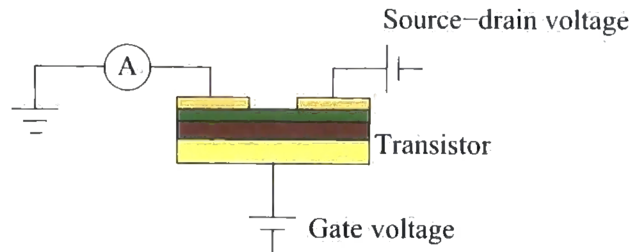


Figure 4.7: Schematic of the three-terminal transistor measurement setup.

may be damaged by physical contact of the AFM tip may be scanned. The atomic force micrographs shown in this work were taken using TappingMode™.

4.5 Electrical characterisation

Two-terminal and three-terminal electrical measurements were made using a PC-driven HP 4140B picoammeter and DC voltage source. The measurements were made in air under ambient light in an electrically grounded metal sample chamber; connections to the sample were made using gold ball probes. All electrical connections between the 4140B and the probes were screened to minimise noise interference. A schematic of the three-terminal transistor measurement setup is shown in figure 4.7, and a photograph of the sample chamber is given in figure 4.8.

Voltage scan rates were 1 V steps at 1 V every 2 seconds. Transistor transfer characteristics were obtained by sweeping the gate voltage from off to on, and back again, while holding the source-drain voltage constant. Output characteristics were obtained by holding the gate voltage constant while sweeping the source-drain voltage, and repeating the sweep and different gate voltages. Transistor mobilities were obtained from fitting a straight line to a plot of the square root of the output saturation currents against gate voltage. Threshold voltages were obtained by plotting the square root of the transfer characteristic current against voltage, and finding the voltage intercept of the linear portion.

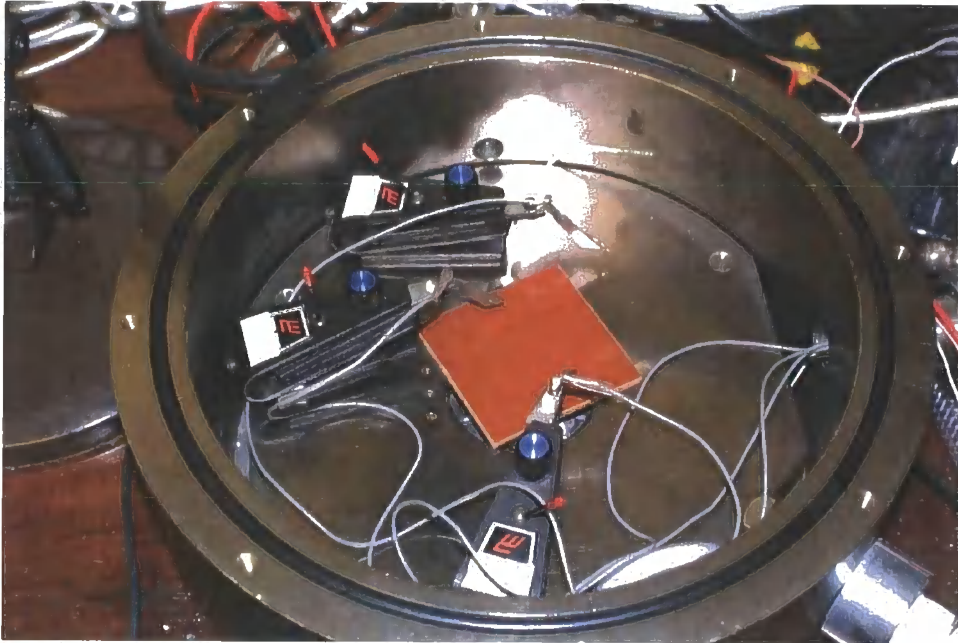


Figure 4.8: Photograph of the measurement sample chamber.

4.6 Summary

The methods used for substrate preparation and transistor fabrication have been provided. Methods used for characterising thin films have been described, as has the electrical measurement technique for complete transistors.

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5

Pentacene/SiO_2-based OTFTs

5.1 Introduction

Pentacene is a common small molecule organic semiconductor used in OTFTs, largely due to its good hole mobility, comparable to that of amorphous silicon, and its easy of deopsition by thermal evaporation.

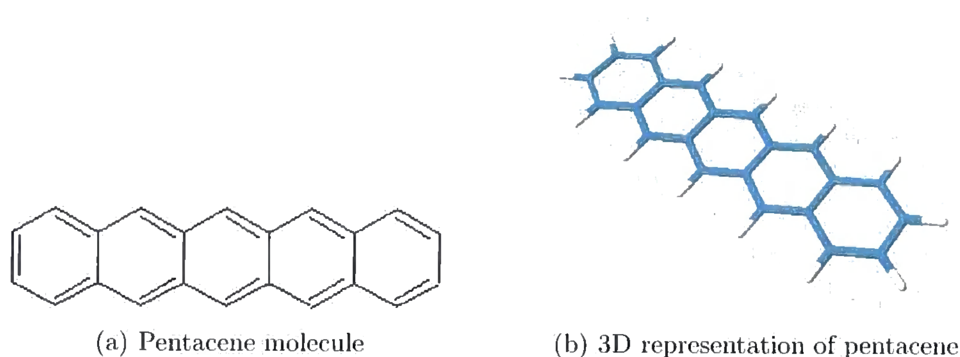
The physical characterisation of pentacene is initially presented, with results consistent with published literature. Initial transistor devices exhibited poor hole mobilities; these have been attributed to the structure of the evaporated pentacene films. Improvements in the device fabrication and organic deposition conditions lead to an improvement in the mobility of around two orders of magnitude. The treatment of the silicon oxide dielectric surface prior to pentacene deposition was found to be very important — X-Ray Photoelectron Spectroscopy measurements confirmed that organic contamination on the surface of the SiO_2 caused charge trapipng and thus resulted in devices with a large hysteresis in the transfer characteristic. Incorporating gold nanoparticles between the silicon oxide and pentacene resulted in large charge trapping; this effect was used in the investigation of memory device [1].

The pentacene used in the investigation was purchased from Sigma-Aldrich with a purity of 99.9%, and used without any further purification. Although most of the results were obtained using pentacene films deposited in the Edwards Auto 306 organics evaporator (see section 4.2.3), some of the results have been obtained using an evaporator designed and built in the School of Engineering — this evaporator is described fully in [2].

5.2 Physical characterisation of pentacene

5.2.1 Chemical structure

Pentacene is a linear acene, consisting of five benzene rings. The chemical structure is shown in figure 5.1.



(a) Pentacene molecule (b) 3D representation of pentacene

Figure 5.1: The pentacene molecule.

5.2.2 Absorption spectrum

Figure 5.2 shows the absorption spectrum of pentacene (90 nm thick) on a glass slide. The spectrum shows an absorption peak between 620 and 690 nm, and the pentacene is transmissive in the blue region (between 320 and 540 nm). This is consistent with the colour of the film, as can be seen in figure 5.3. The spectrum is comparable to one obtained by [3], indicating that the pentacene molecule did not dissociate during evaporation. There is a major absorption peak at 680 nm, with the 'shoulder' starting at around 700 nm; this wavelength corresponds to an energy of around 1.8 eV, and thus the absorption can be attributed to being due to the pentacene molecule's bandgap (1.82 eV [4]); photons of this energy are absorbed by electrons in the HOMO band, which are then excited into the LUMO band.

5.2.3 Film morphology

One of the biggest influences on carrier mobility in a semiconductor device is the size of the crystals formed during deposition. Within a crystal, electrons

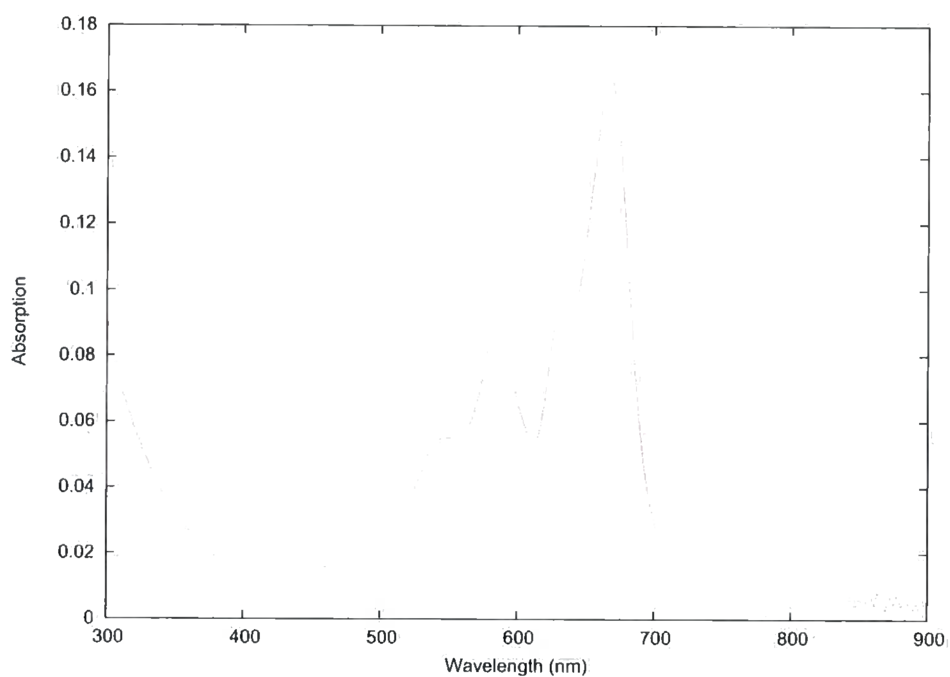


Figure 5.2: Absorption spectrum of a 90 nm thin film of pentacene between 300 and 900 nm.

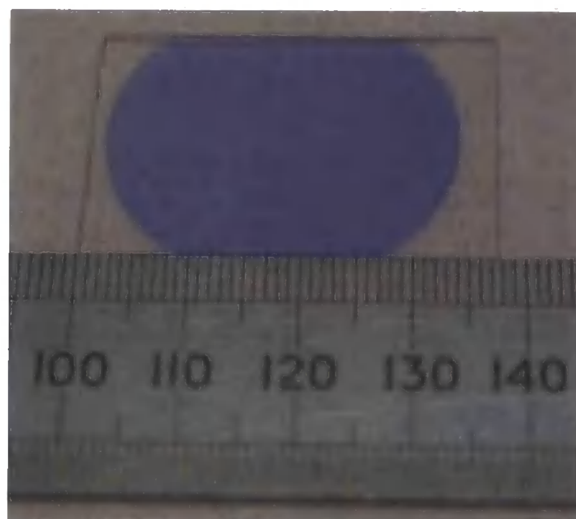


Figure 5.3: Photograph of a 133 nm pentacene thin film on glass slide (38 mm × 25 mm).

are fairly free to move around. However, in a polycrystalline material, charge carriers get trapped in the grain boundaries, which serve to reduce the effective mobility (see section 2.5.3).

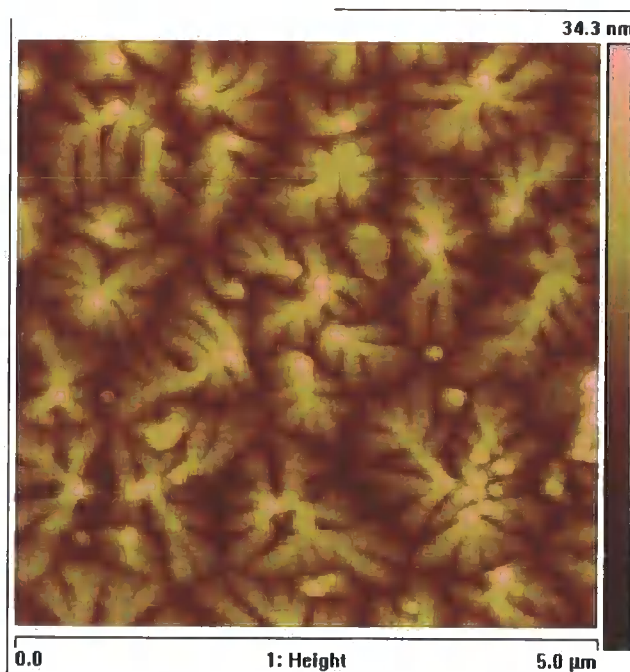
Figure 5.4a shows an atomic force microscope (AFM) scan of pentacene evaporated at a pressure of approximately 2.15×10^{-6} mbar and a source temperature of 174°C, at a rate of 0.05–0.1 nm/s. It can be seen that pentacene forms a polycrystalline structure, with dendritic grains. The grains are approximately 1 – 1.5 μm in diameter.

Pentacene evaporated at a lower temperature of 154°C, at a rate of 0.03 nm/s, has a larger grain size of around 2–3 μm in diameter; at 147°C, with a deposition rate of around 0.015 nm/s, it was also found to have a 2–3 μm grain size. Evaporating at a higher temperature (203°C, with an evaporation rate of 1.5 nm/s) gave the film structure shown in figure 5.4b. Only small irregular grains, around 150–200 nm in diameter, are observed: no dendritic structure is apparent, as it is with the slower evaporated pentacene. The small grains are most likely caused by the condensing pentacene molecules not being able to migrate to a site of lower surface potential (thus forming a crystal structure) before further molecules bury the ones already on the surface. This is consistent with [5], where it was reported that flash evaporating pentacene resulted in small irregular grains, along with low mobilities for TFTs. The home-built evaporator was only able to flash evaporate organic material as it was not possible to control the evaporation process properly; hence all early devices fabricated and reported on in this thesis possess relatively low mobilities.

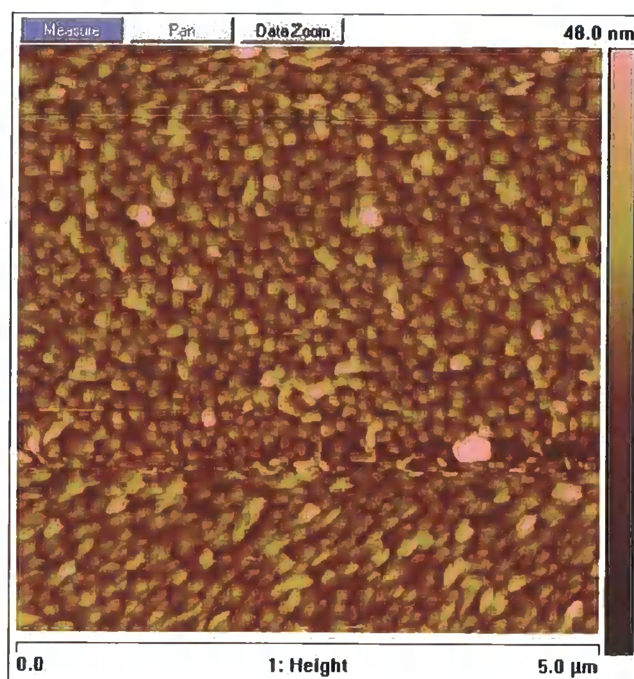
5.3 Electrical characterisation

To measure the electrical conductivity of pentacene, a set of equidistant gold contacts (1.4 mm separation, 75.5 mm long) were evaporated through a shadow mask onto a 90 nm thick pentacene layer on a glass microscope slide. For comparison to the conductivity of glass, a set of chrome/gold contacts were evaporated onto a clean glass slide.

In-plane currents at voltages varying between +50 V and -50 V (in steps of 1 V, starting at 0 V) were measured across a number of the contacts in a number



(a) Evaporated at 174°C.



(b) Flash evaporated at 203°C.

Figure 5.4: 5 µm × 5 µm AFM scans of evaporated pentacene.

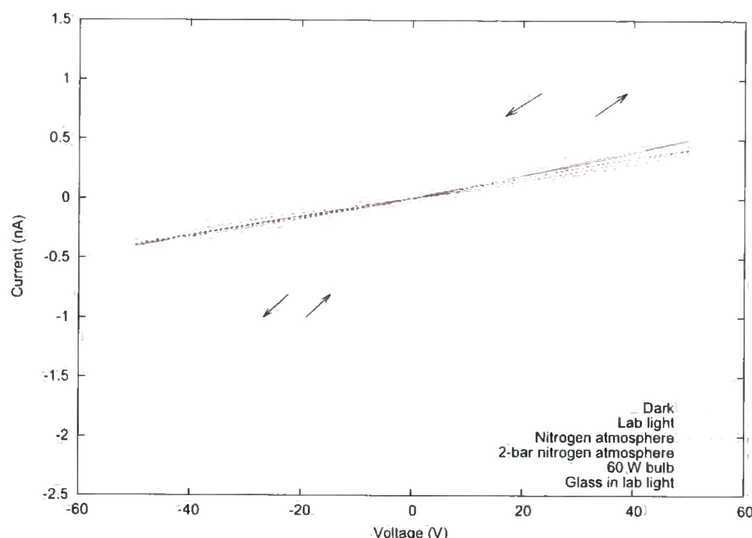


Figure 5.5: I-V characteristics for pentacene in various environments, and for a glass slide in ambient light.

of environments — darkness, ambient lab light, under a 60 W incandescent bulb, and in a nitrogen atmosphere. Figure 5.5 gives an indication of the resistance of the pentacene film in the various environments between a pair of adjacent contacts. As can be easily seen from the graph, the number of charge carriers are significantly increased in the presence of light. This is expected from the absorption spectrum, which has an absorption peak at around 680 nm, corresponding to an energy of around 1.8 eV, the bandgap of pentacene (1.82 eV [4]).

Applying linear regression to the I-V curves yields a resistance for pentacene of 1.12×10^{11} Ω for measurements taken in the dark, whereas under a 60 W incandescent bulb, the resistance decreases by a factor of four, to 2.75×10^{10} Ω. For comparison, the resistance between adjacent contacts on a clean glass slide was 1.3×10^{11} Ω.

Given that the resistances of the glass slide and the glass slide with pentacene are very similar, no conclusions can be drawn as to how much of the current is carried by the pentacene and how much by the glass itself. However, there is evidence that the presence of light increases the number of charge carriers in the pentacene, and hence in this state, there is current being carried by the pentacene film.

5.4 Transistor measurements

5.4.1 Initial experiments

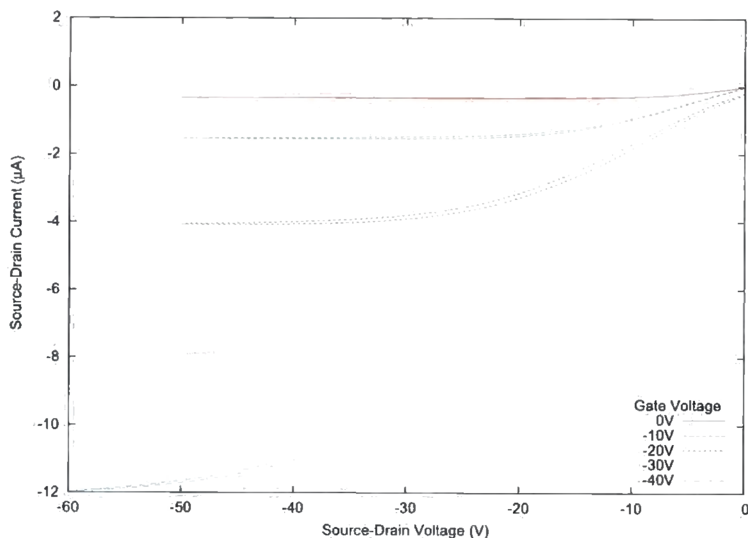
The first devices fabricated during the course of this work were fabricated on 0.1 Ωcm silicon wafers, with the pentacene being deposited in the home-built organics evaporator. Typical characteristics are shown in figure 5.6.With a channel length of 70 μm and width of 1.6 mm and SiO_2 thickness of 105 nm, and using equation 2.29, a mobility of 6.3×10^{-3} $cm^2/V/s$ is obtained. Although this value is low, it is comparable to the mobilities obtained in [5] for flash evaporated pentacene (10^{-4} $cm^2/V/s$, rising to 2×10^{-3} $cm^2/V/s$ after annealing). AFM scans (see section 5.2.3) confirm the relatively small grain size, which explains the low mobility.

5.4.2 Silane treatment

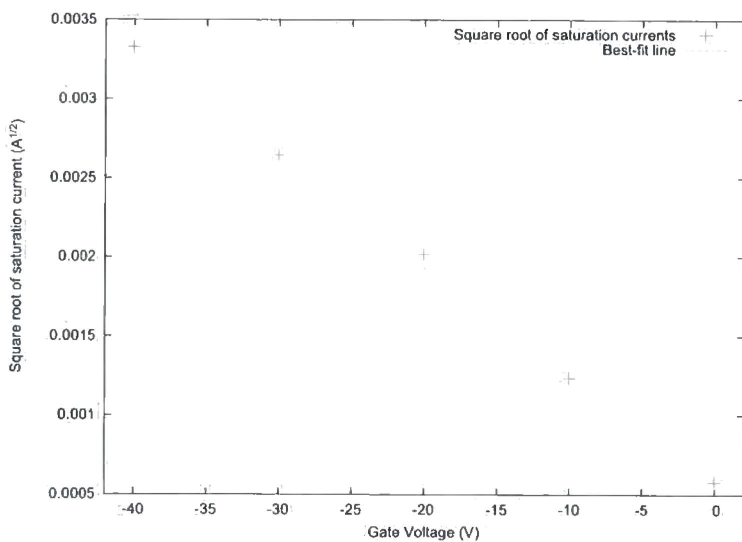
One of the ways of improving transistor mobilities is to modify the dielectric surface (indeed the dielectric surface appears to be crucial in the performance of SiO_2/pentacene transistors; see section 5.4.6); this causes the electronic properties (e.g. surface states) of the semiconductor/dielectric to be modified. It has been reported [6] that treating the SiO_2 surface with a silanising agent improves the device performance (see also section 2.6).

Two sets of transistors were fabricated on 0.1 Ωcm Si wafers: to provide a fair comparison, the oxides were grown, and the pentacene and contacts were evaporated, at the same time. One of the oxidised wafers was placed into a dimethyldichlorosilane (DMDS) solution until the surface was rendered hydrophobic. Excess silanising agent and solvent were removed from the wafer by rinsing it in acetone, isopropanol, and deionised water.

It was found that the saturation currents for the DMDS treated wafer were approximately 60% higher than those of the untreated wafer. This resulted in a mobility of 5.0×10^{-3} $cm^2/V/s$ for the untreated wafer, and 8.9×10^{-3} $cm^2/V/s$ for the DMDS treated wafer — the DMDS treatment increased the mobility by approximately 80%.



(a) Output characteristic



(b) Square root of saturation currents against gate voltage

Figure 5.6: Characteristics of initial devices fabricated.

5.4.3 Improving the gate

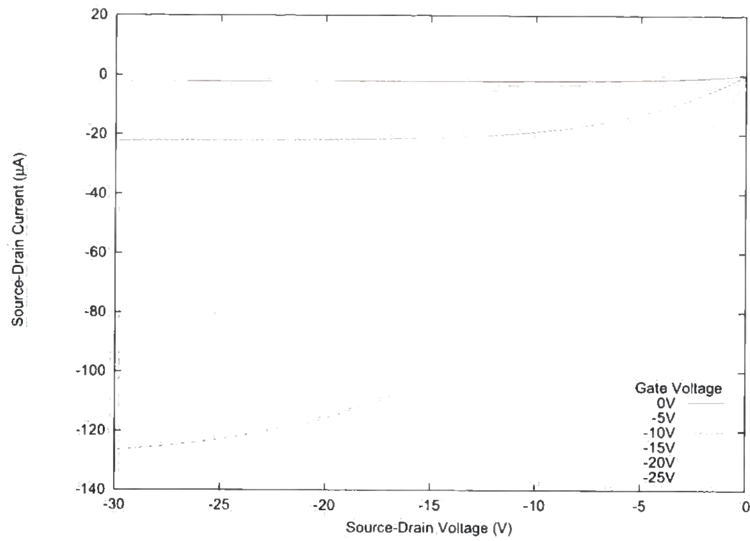
A higher mobility transistor was fabricated by replacing the 0.1 Ωcm resistivity silicon wafer with a 10^{-3} Ωcm resistivity wafer. The saturation currents were found to be an order of magnitude greater than those of previous devices; the mobility was 0.105 $cm^2/V/s$, an order of magnitude greater than that reported in section 5.4.2.

5.4.4 Effect of grain size

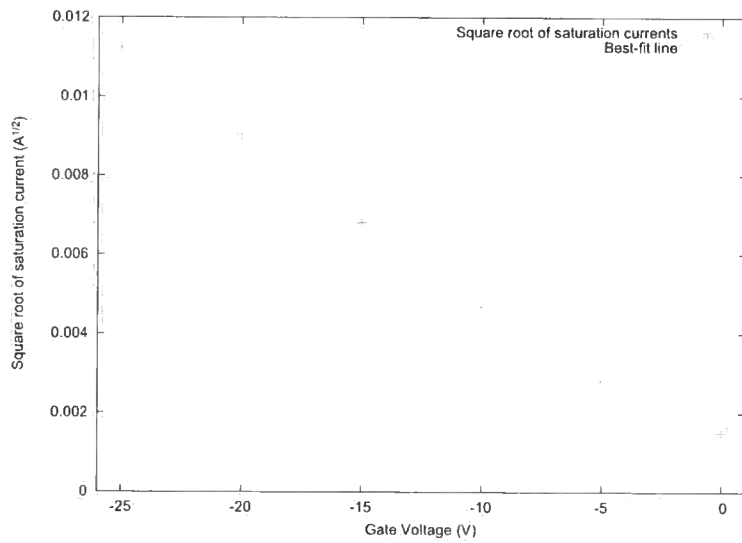
As described in section 5.2.3, the grain size of pentacene should have a significant effect on the mobility of the transistors. It has been shown in the previous sections that flash evaporated pentacene, which does not form a good crystal structure, yields low mobilities (of the order of 10^{-2} – 10^{-3} $cm^2/V/s$). When a good crystal structure was formed (as seen in figure 5.4a), the mobilities increased significantly. Figure 5.7a shows the I-V characteristics of a device fabricated on pentacene with a 2–3 μm crystal size (similar in structure to the pentacene shown in figure 5.4a). The mobility can be extracted by plotting the square root of the saturation current against gate voltage, as given in figure 5.7b, which gives a mobility of 0.54 $cm^2/V/s$. Although this is not the highest value reported in the literature, it is a respectable value for a transistor fabricated without any optimisation (e.g. holding the substrate at an elevated temperature during pentacene deposition [5, 7–10]). Compared to the initial devices fabricated (section 5.4.1 and figure 5.6), it can be seen that the output currents are an order of magnitude larger, even with reduced gate voltages. The shape of the I-V curve is also closer to that of an ideal transistor (figure 2.13).

With a transistor fabricated on pentacene with a grain size of around 0.5 μm, the mobility of transistors was below 0.2 $cm^2/V/s$; thus demonstrating that the larger the crystal grains, the higher mobility is obtained.

The grain barrier boundary model can be applied to these devices to obtain the trap-free mobility and trap density. Figure 5.8 shows the Levinson plot ($\ln(I_D/V_G)$ against $1/V_G$ in the linear region of the transfer characteristic) for the off-on sweep (at -20 V source-drain voltage) of the device shown in figure 5.7. Using equation 2.32, and taking the semiconductor thickness as 30 nm



(a) Output characteristics



(b) Square root of saturation current against gate voltage

Figure 5.7: Characteristics of device fabricated on pentacene with 2–3 μm crystal size.

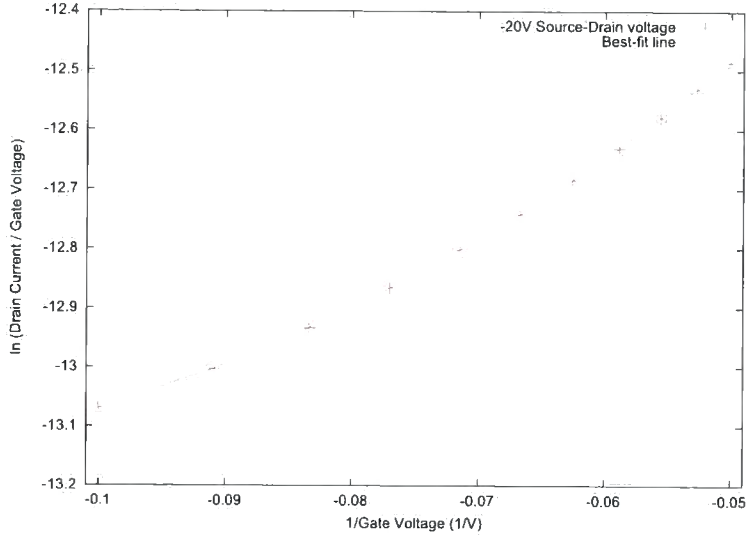


Figure 5.8: Levinson plot for linear region of transistor.

and room temperature to be 294 K, this gives the trap density as 6.27×10^{18} cm^{-2}. Using equation 2.31, at a gate voltage of -20 V, this gives the potential barrier height, E_B, to be 15 meV, and the trap-free mobility, μ_0, to be 0.98 $cm^2/V/s$.

5.4.5 Improving the gate contact

The contact to the gate (the Si wafer) for the devices reported above had been made by removing silicon oxide from the back of the silicon wafer with a diamond pen and attaching aluminium foil to the exposed silicon using silver paste. However, the mobility of the transistors could vary as much as by a factor of three across the wafer. Figure 5.9 shows I-V characteristics between two electrodes of silver paste, 20 mm long and 4 mm wide, with 15 mm separation, on a clean silicon wafer. As can be seen, the silver paste provides a non-Ohmic contact to the silicon. When two aluminium contacts were evaporated a similar distance apart, they were found to produce a good ohmic contact to the silicon, with a very low resistance (data not shown).

To evaporate aluminium directly onto silicon, it was necessary to etch selectively part of the silicon oxide, whilst leaving the rest of the oxide intact for use as the gate dielectric. One method that was attempted involved etching the back side of the silicon wafer in a reactive ion etcher. Devices subsequently

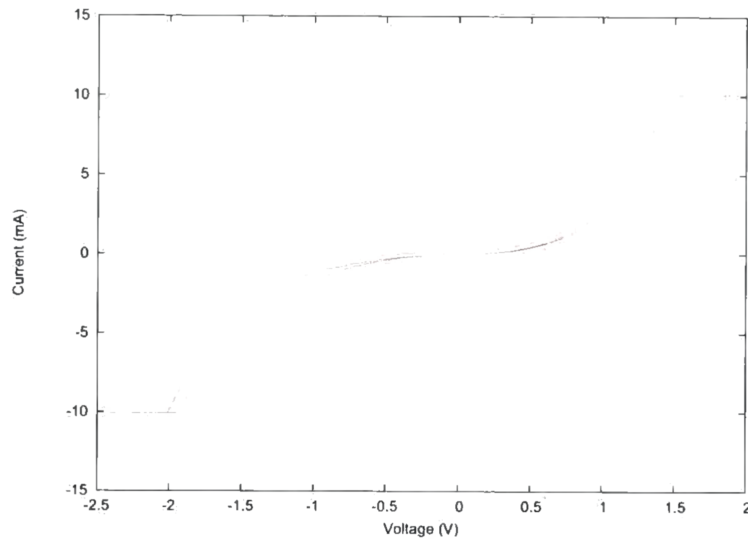


Figure 5.9: I-V characteristic for silver paste contacts on silicon.

fabricated on such wafers exhibited very large hysteresis in the transfer characteristics, as shown in figure 5.10. Another disadvantage of etching wafers in the RIE was the difficulty in patterning the silicon oxide for selective etching.

An alternative method of etching back the silicon oxide was to use hydrofluoric acid. This required the front side of the wafer to be protected from the acid. Shipley S1813 photoresist was therefore spin-coated onto the front of the wafer, and baked at 95°C for 15–20 minutes, which made the resist resistant to HF. After the oxide was etched away, the photoresist was removed with acetone and isopropanol. Transistors fabricated on these wafers exhibited very similar hysteresis effects to those fabricated on wafers that had been etched in the RIE. The origin of this hysteresis is discussed in section 5.4.6.

5.4.6 SiO_2 surface treatment

The large hysteresis reported in section 5.4.5 could be attributed to treatment or modification of the silicon oxide surface. Smith and Hill [10] reported that treatment of the silicon oxide with an oxygen plasma after cleaning with organic solvents served to considerably reduce hysteresis. It was decided to see if a similar effect could be observed when fabricating transistors after removing the photoresist in a number of ways [11].

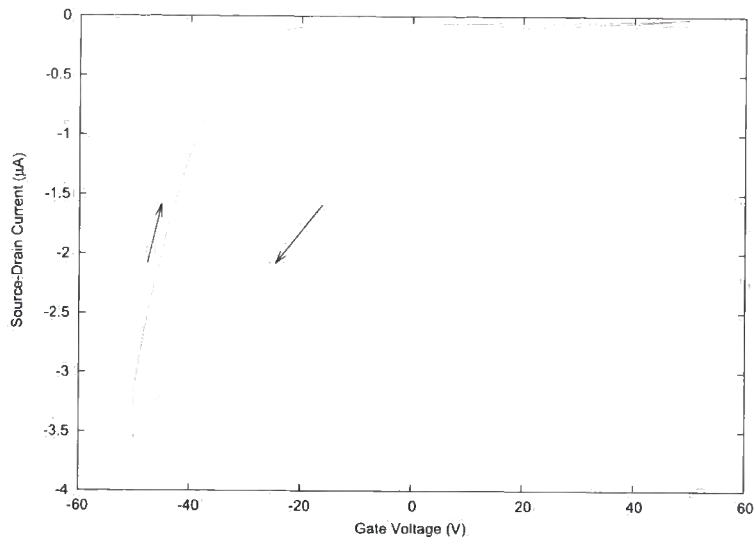


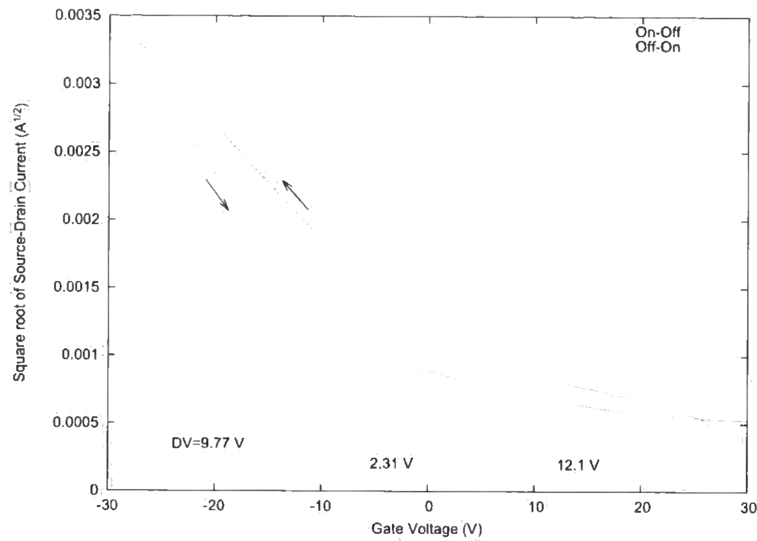
Figure 5.10: Transfer characteristics at -20 V source-drain voltage for RIE-etched wafer.

S1813 photoresist was spin-coated onto silicon wafers with 135 nm thermally-grown oxide, at a speed of 500 rpm for 5 seconds for initial dispersal, followed by 3700 rpm for 30 seconds to reduce to the desired thickness (1.3 μm); the resist was then soft-baked at 95°C for 2 minutes. The resist was stripped off in the following ways, after which transistors were fabricated (the gate contact being made to the silicon with silver paste): Microposit 1112A stripper*; 1112A stripper followed by an oxygen plasma; acetone and isopropanol; acetone and isopropanol followed by Caro's acid†; acetone and isopropanol followed by oxygen plasma; and acetone and isopropanol followed by Caro's acid and oxygen plasma. The oxygen plasma had a partial pressure of 1.6 mbar and a delivered power of 200 W; the substrates were placed on a floating electrode and subjected to the plasma for 17 minutes.

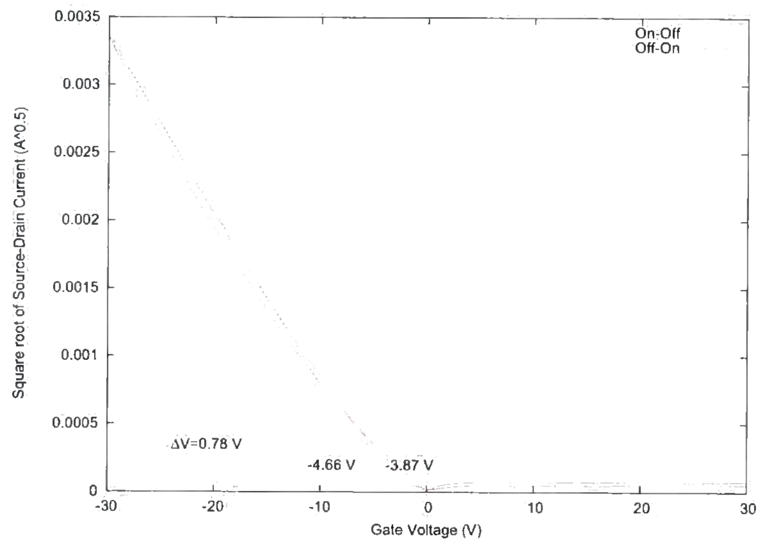
Figure 5.11a shows the off-on and on-off transfer curves for an FET that had photoresist removed with just acetone and propanol. The square root of the drain current is plotted as a function of the gate voltage, and the threshold voltage is defined as the voltage intercept of a fit to the linear portion. A shift

*1112A stripper is commonly used in the semiconductor industry for removing photoresist

†Caro's acid is used to remove organic residues: see section 4.2.1



(a) Without plasma treatment



(b) With plasma treatment

Figure 5.11: Transfer characteristics for devices where the photoresist was removed with acetone and propanol, optionally followed by an oxygen plasma treatment.

Preparation	V_{th} (off–on) (V)	V_{th} (on–off) (V)	ΔV_{th} (V)
1112A stripper	6.34	-1.64	7.98
1112A stripper, oxygen plasma	31.98	11.08	20.90
Acetone and isopropanol	11.30	1.63	9.67
Acetone and isopropanol, Caro's acid	6.49	-2.48	8.98
Acetone and isopropanol, oxygen plasma	3.21	-0.563	3.77
Acetone and isopropanol, Caro's acid, oxygen plasma	8.77	3.57	5.20

Table 5.1: Average hysteresis and threshold voltages for the various device preparations.

in threshold voltage is clearly evident. For comparison, figure 5.11b shows the off-on and on-off transfer curves for a FET where the resist was removed using acetone and propanol, followed by a plasma treatment. Although there is still a shift in threshold voltage, this shift has been considerably reduced. Table 5.1 summarises the average hysteresis in the I-V measurements for each type of preparation.

The threshold voltage shifts can be attributed to charge trapping at the semiconductor/gate dielectric interface. The threshold voltages shift according to the relation $\Delta V_{TH} = -Q_{int}/C_{ox}$ [12], where ΔV_{TH} is the threshold voltage shift, Q_{int} the interface charge, and C_{ox} the oxide capacitance per unit area.

As a positive gate bias is applied, electron trapping states on the interface become populated. This, therefore, causes a positive shift in the threshold voltage. As the gate voltage is made more negative, more holes are induced to balance the stored charge. When the gate voltage is swept from negative to positive (on-off scan), it starts from hole accumulation and no stored negative charge. Hence for the same gate voltage, the extra holes result in a larger drain current for the off-on sweep [9].

The negative threshold voltages for the on-off sweep can be attributed to hole trapping at the interface: similar results have been reported by Smith and Hill [10] when cleaning SiO_2 surfaces prior to pentacene deposition.

The results may be explained if the origin of the electron traps is attributed to organic contaminants on the surface of the silicon oxide: removal of the photoresist with acetone and isopropanol still results in a large number

of residual organic molecules trapped on the oxide surface. Oxygen plasma cleaning is widely used in the semiconductor industry to remove organic contaminants during wafer processing as the plasma is very efficient at removing these residues. This does not explain the results obtained with the 1112A stripper, where the plasma treatment increased the hysteresis. This is most likely due to the chemical composition of the stripper, which contains a number of inorganic compounds [13].

To verify if the origin of the traps was due to organic residues on the oxide surface, X-Ray Photoelectron Spectroscopy (XPS) measurements were obtained for hexamethyldisilazane (HMDS) treated silicon oxide surfaces where the photoresist had been stripped off with acetone and isopropanol only, and where the acetone and isopropanol had been followed by an oxygen plasma. The XPS measurements were performed using a VG ESCALAB II electron spectrometer equipped with an unmonochromated Mg $K\alpha_{1,2}$ X-ray source (1253.6 eV) and a concentric hemispherical analyser. Photoemitted electrons were collected at a takeoff angle of 30° from the substrate normal, with electron detection in the constant analyser energy mode (CAE, pass energy 20 eV). Each XPS spectrum was referenced to the C(1s) hydrocarbon peak centred at 285.0 eV and fitted using Marquadt minimisation computer software to a linear background with equal full-width at half-maximum Gaussian components.

If the traps were due to organic residues, it would be expected to see a much lower carbon content on the surface of the plasma-cleaned oxide.

Table 5.2 shows the results of the XPS measurements on the two samples. The results clearly show a reduction in carbon for the plasma-cleaned sample, supporting the theory that the charge trapping was caused by organic contamination. The surface stochiometry has not changed significantly after plasma cleaning (O:Si ratio was 2.07 before plasma cleaning, and 2.14 after plasma cleaning), showing the plasma does not alter the silicon oxide structure. The results are therefore indicative of a reduction in surface contamination.

Figures 5.12 and 5.13 show the Si(2p) and O(1s) spectra for both samples. It can be seen that the spectra before and after plasma treatment do not change, apart from a shift to higher binding energies. This shift may be attributable to the silicon existing in a more electropositive environment — the increase in electronegative oxygen atoms from the plasma depletes the silicon of electrons. The origin of the difference of the shift of the O(1s) peak (0.5 eV) and the Si(2p) peak (1 eV) is unknown.

Preparation	Elemental Composition (%)		
	Carbon	Oxygen	Silicon
Acetone and Isopropanol	11.7	59.5	28.8
Acetone and Isopropanol, oxygen plasma	7.8	62.8	29.4

Table 5.2: XPS summary for plasma-cleaned and non-plasma cleaned SiO_2 surfaces.

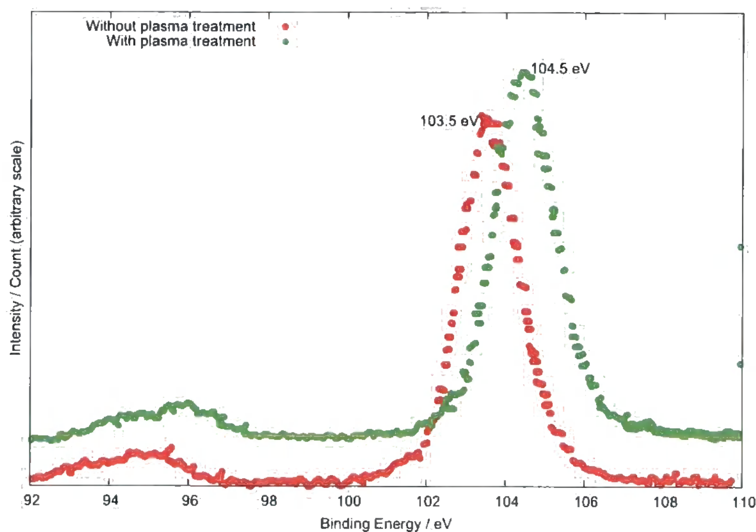


Figure 5.12: Si(2p) spectra for samples cleaned in acetone and isopropanol, optionally followed by an oxygen plasma.

Figure 5.14 shows the C(1s) spectrum for the plasma-cleaned sample. In addition to the C(1s) peak at 285 eV, there is another peak at 300.3 eV, with a similar intensity. This binding energy is similar to that of Ra(4f) (299.0 eV) or Y(3p3) (299.2 eV) [14], however it is very unlikely to be one of these elements due to the experimental methods used to produce the samples. The origin of the peak therefore remains unknown, although it is believed to be due to surface contamination of the SiO_2. The binding energies of the C(1s) peaks do not shift after a plasma treatment, although the reduction in carbon on the surface results in a lower intensity peak at 285 eV.

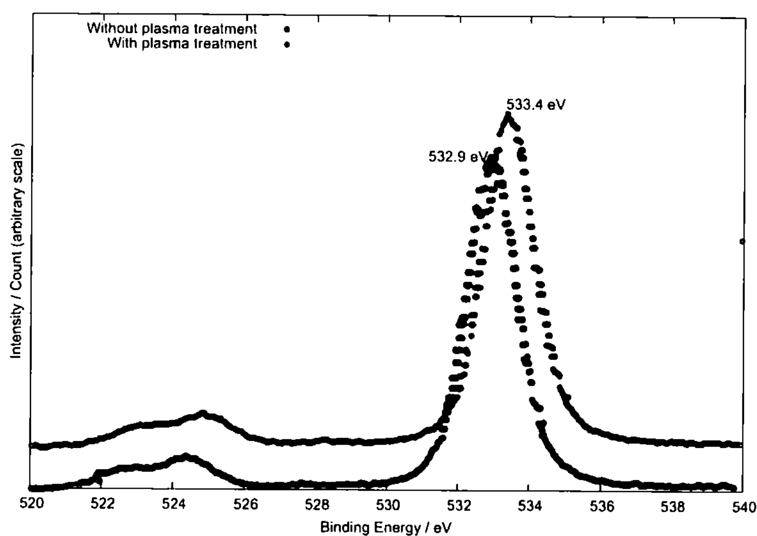


Figure 5.13: O(1s) spectra for samples cleaned in acetone and isopropanol, optionally followed by an oxygen plasma.

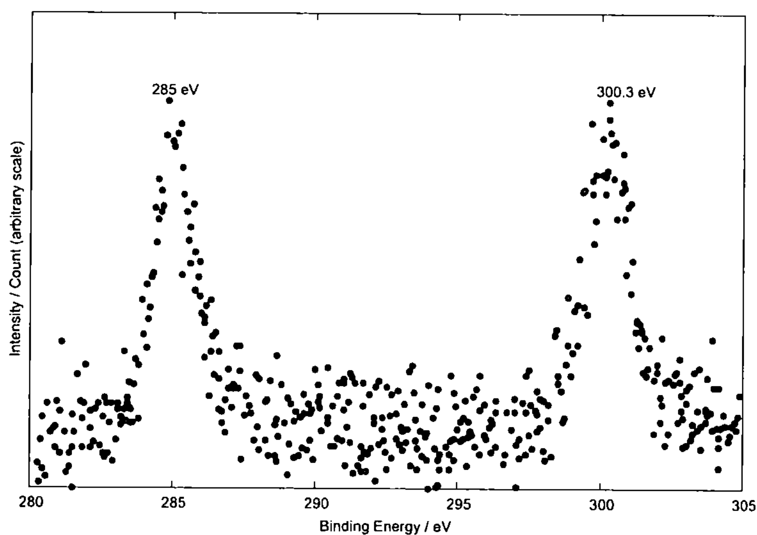


Figure 5.14: C(1s) spectrum for sample cleaned in acetone and isopropanol, followed by an oxygen plasma.

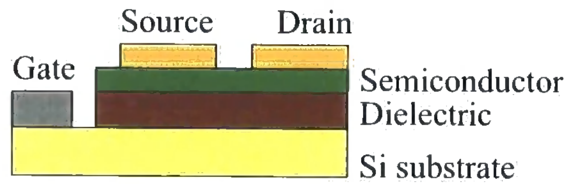
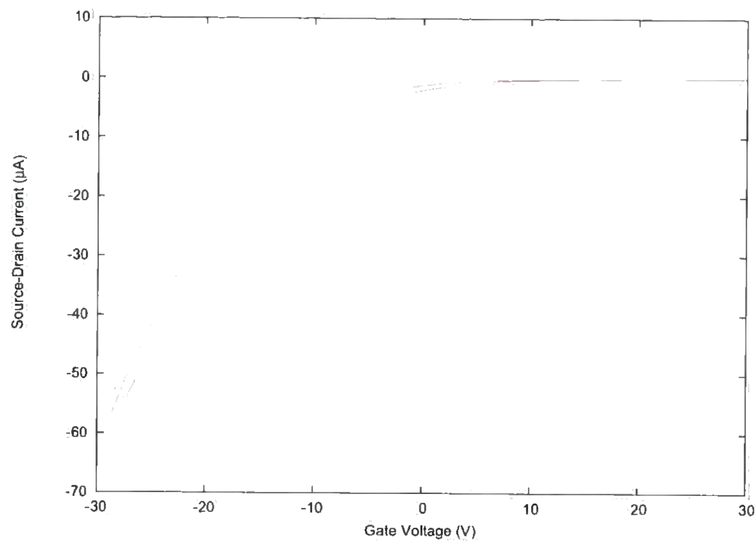


Figure 5.15: Schematic of a transistor with the gate contact on the top side of the substrate.

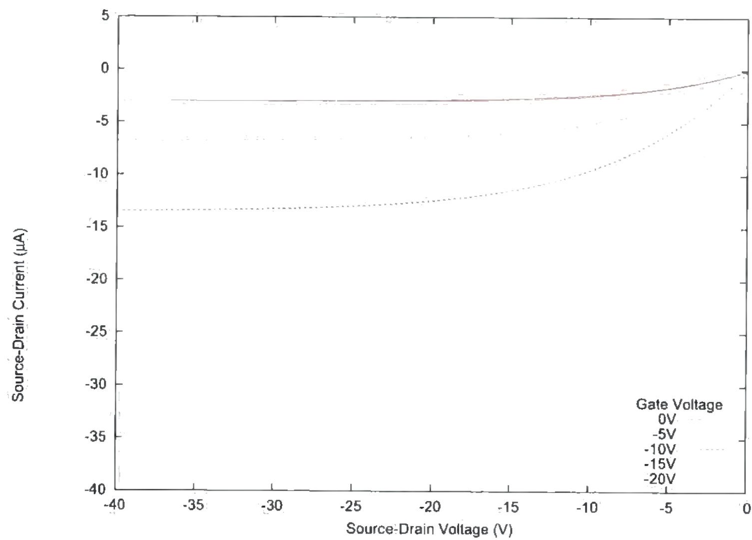
5.4.7 A transistor with an improved gate contact

Having established that plasma cleaning was able to reduce significantly hysteresis in the transistor, it was attempted to fabricate another transistor with a gate contact directly on to the silicon wafer, using the structure shown in figure 5.15.

S1813 was spun onto a freshly oxidised silicon wafer and baked for 2 minutes at 95°C. An edge of the wafer was exposed to UV light, and the resist then developed in Microposit 351 developer. The remaining resist was baked for a further 15 minutes at 95°C, to make the resist resistant to hydrofluoric acid. The wafer was placed in HF to strip back the exposed oxide; once the silicon was reached, the remaining photoresist was removed with acetone and isopropanol, and ~120 nm aluminium was evaporated onto the exposed silicon as a gate contact. The wafer was then subjected to a plasma clean, followed by an HMDS surface treatment, and pentacene and gold source-drain contacts were then evaporated. The results are shown in figure 5.16; the mobilities were around 0.17 $cm^2/V/s$. However, the mobilities of devices across the wafer were found to be more consistent than those devices fabricated using silver paste for the gate.



(a) Transfer characteristics at -20 V source-drain voltage



(b) Output characteristics

Figure 5.16: Characteristics of a device fabricated with a gate on top of the substrate.

	V_{th} (Off–On)	V_{th} (On–Off)	ΔV_{th}
Without nanoparticles	35.75	2.81	32.94
With nanoparticles	48.98	-2.68	51.66

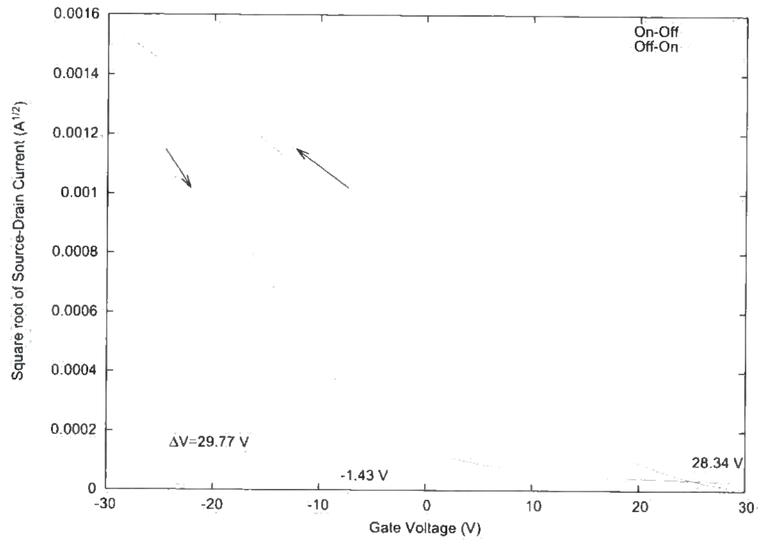
Table 5.3: Threshold voltages and shifts for devices incorporating gold nanoparticles and without nanoparticles.

5.4.8 Gold nanoparticles

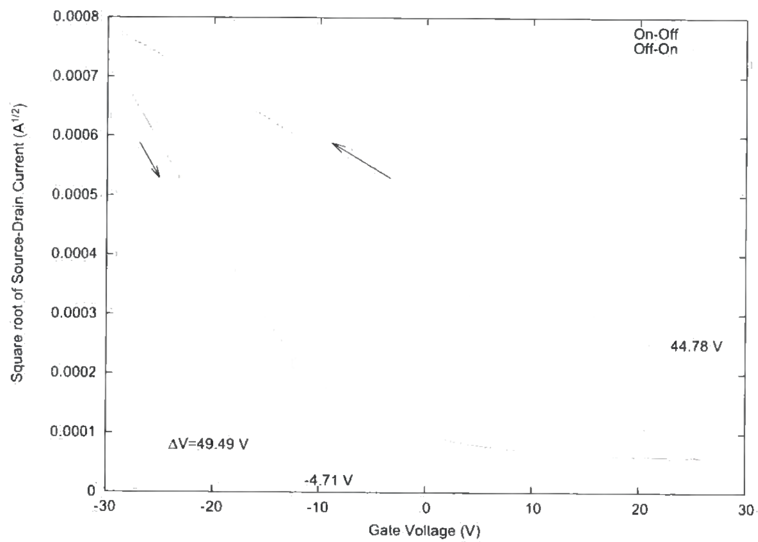
In all of the devices reported above, there is a leakage current flowing between source and drain terminals when a gate voltage is applied, even though 0 V was applied to the source. Jia *et al.* [15] have attributed a major source of this leakage current to the effective expansion of the source-drain electrodes from the conducting accumulation layer when unpatterned OTFTs are on. They found they could substantially reduce the leakage current to levels comparable to the leakage current through the SiO_2 dielectric by patterning the semiconductor and limiting the film to the channel area. Patterning the semiconductor had also previously been reported to reduce the leakage current [16]. Additionally, it had been reported (Molloy *et al.*, unpublished work) [17] that the leakage current could be reduced by incorporating a layer of gold nanoparticles between the silicon oxide and the pentacene film.

Gold nanoparticles (Q-Au) of nominal diameter 10 nm were deposited by LB deposition onto HMDS-treated silicon oxide before pentacene and gold contacts were evaporated. Figure 5.17 compares the transfer characteristics of a device with and without nanoparticles. Although the device without nanoparticles has a large hysteresis, which could be attributed to organic contamination during the device fabrication, the device incorporating nanoparticles demonstrates a significant increase in the hysteresis. Table 5.3 summarises the threshold voltages and threshold voltage shifts across a number of devices, with and without nanoparticles. As in section 5.4.6, the results are consistent with adding traps (both electron and hole) to the semiconductor / dielectric interface. Gold nanoparticles have been used as charge storage elements in memory devices [1, 18–20], and hence act as good charge traps.

Figure 5.18 shows the output characteristics of the devices shown in figure 5.17. There is no significant reduction in the leakage currents between the

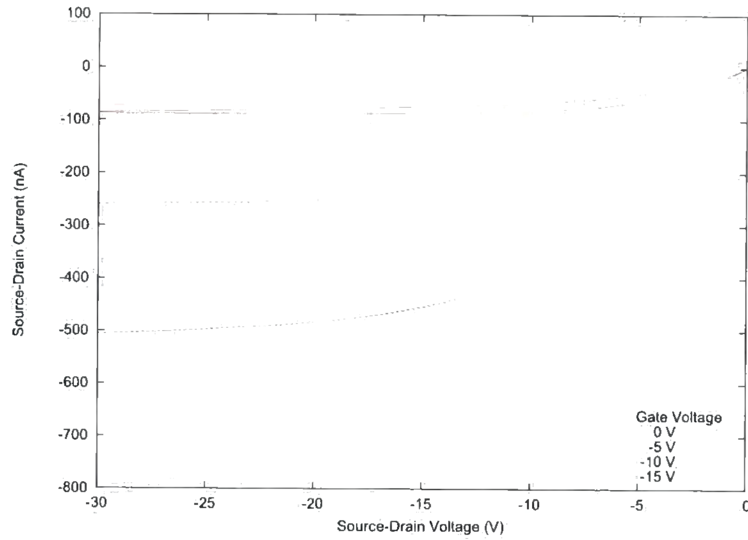


(a) No nanoparticles

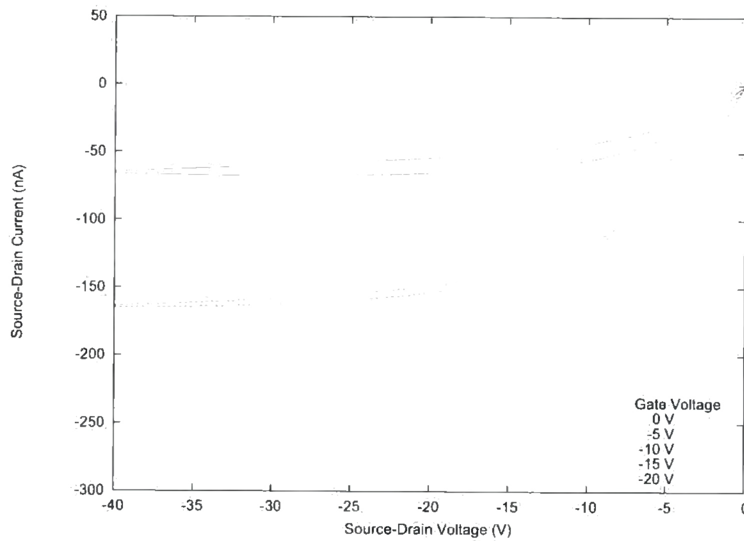


(b) With nanoparticles

Figure 5.17: Transfer characteristics for devices incorporating nanoparticles and without nanoparticles, source-drain voltage of -20 V.



(a) No nanoparticles



(b) With nanoparticles

Figure 5.18: Output characteristics for devices with and without nanoparticles.

devices incorporating nanoparticles and those without nanoparticles. However, the mobility is reduced from 5.5×10^{-3} $cm^2/V/s$ to 5.7×10^{-4} $cm^2/V/s$ — an order of magnitude reduction. The low mobilities, even on the device not incorporating nanoparticles, could be attributed to flash evaporated pentacene — i.e. not having formed a good crystal structure during evaporation.

5.5 Summary

Physical and electrical characterisation were performed on pentacene thin films, with the reported results consistent with published data. Transistors using pentacene on silicon oxide have been fabricated; initially with poor mobilities, but with the mobilities improving as processing and understanding of the effects of SiO_2 surface treatments improved. Hysteresis in the devices was attributed to charge trapping at the SiO_2/pentacene interface (confirmed when incorporating gold nanoparticles into the device structure), which was attributed to organic contamination on the SiO_2 surface (confirmed by XPS measurements). The charge trapping due to gold nanoparticles was used in further research into organic memory devices [1].

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6
Alternative gate dielectrics

6.1 Introduction

Although silicon oxide is a common dielectric for fabrication of OTFTs, there are various arguments for replacing this material with another. Silicon / silicon oxide devices suffer from a number of processing issues — high temperatures are needed to grow the oxide layer, and the silicon is brittle, so flexible devices cannot be fabricated in this manner. Replacing the SiO_2 with an organic insulator that can be spin-coated or inkjet printed is therefore desirable to be able to make these flexible transistors. Additionally, as silicon transistors become smaller, with a corresponding reduction in gate dielectric thickness, gate leakage currents will become significant, thus reaching the limits of SiO_2 [1]. The use of high-k dielectrics, which would give a higher capacitance for an equivalent thickness, has been the subject of a large amount of research; hafnium oxide has produced favourable results due to its high dielectric constant and good physical and chemical properties [2], both with silicon transistors (new transistors from Intel and IBM are already incorporating HfO_2 into their gate dielectrics [3]) and with organic transistors using pentacene [4,5].

In this work, pentacene-based transistors have been fabricated using poly (methyl methacrylate) (PMMA) as an organic insulator, and hafnium oxide (k $\sim$ 25) as a high-k dielectric. The devices have been characterised to compare their performance to devices fabricated on silicon oxide.

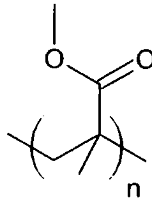


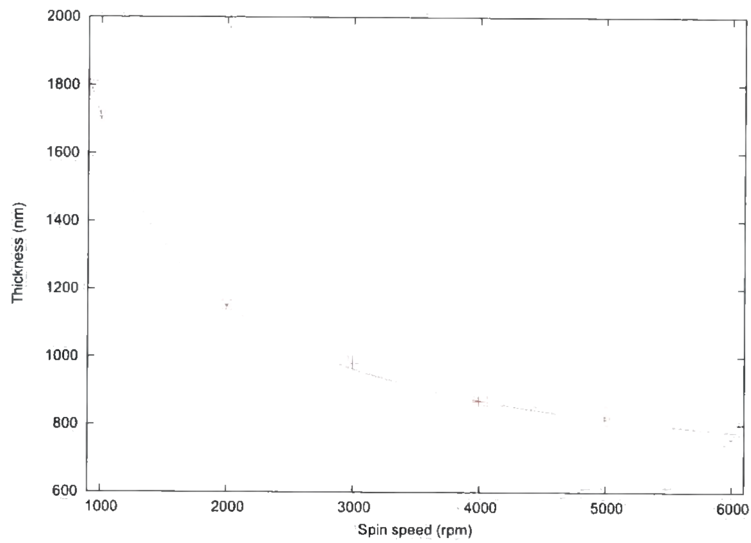
Figure 6.1: The PMMA molecule.

6.2 PMMA dielectric

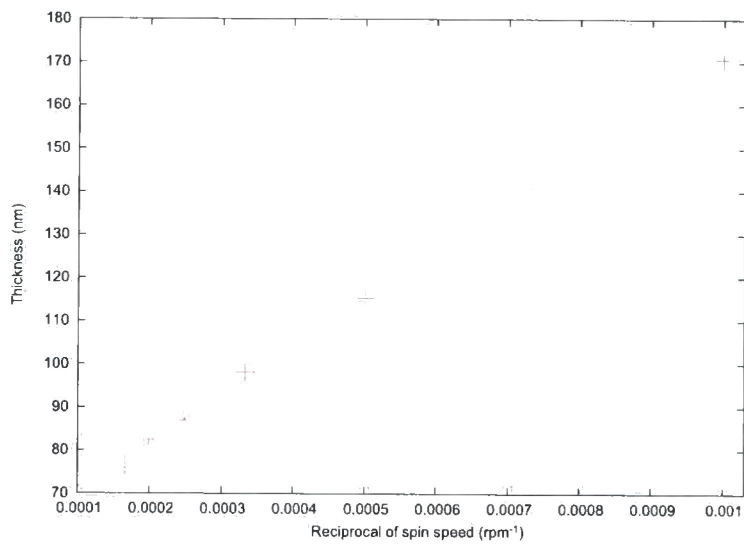
Poly(methyl methacrylate) (PMMA) was chosen as the organic dielectric due to its thermal and mechanical stability, high resistivity, and similar dielectric constant to that of silicon oxide [6]. Its molecular structure is shown in figure 6.1. Additionally, PMMA has easily hydrolysed ester groups which make it highly soluble, and hence suitable for spin coating. Section 4.2.2 details the deposition procedure of PMMA dielectrics. The work in this section has been carried out in collaboration with Ben Shuler, a final year project student [7].

A spin curve for the PMMA solution was initially obtained in order to be able to spin a known thickness of dielectric. PMMA has a refractive index of 1.496 at a wavelength of 632.8 nm [8]. The PMMA was spun on to freshly cleaned silicon wafers and the thickness was measured by ellipsometry. Figure 6.2a shows the spin curve obtained. The curve has been found to fit well with spin-coating theory — as shown in figure 6.2b, the thickness was proportional to the reciprocal of the spin speed (equation 3.30).

Figure 6.3 shows the transfer characteristic for a transistor with a 124 nm PMMA dielectric layer; the source-drain voltage was held at -20 V. The threshold voltage is around -4.5 V, and it can be seen that there is very little hysteresis in this characteristic — the threshold voltage shift is only 0.11 V. The current saturation at gate voltages below -20 V is most likely due to a current limit on the voltage source being activated. Figure 6.4 shows the output characteristics and the square root of saturation currents plotted against gate voltage for the same device. The shape of the output curve is unusual when compared with ideal characteristics, or even the pentacene / SiO_2 devices. Good saturation currents were obtained, with a very definite transition



(a) Thickness against spin speed



(b) Thickness against reciprocal of spin speed

Figure 6.2: Spin curve for 2.5% PMMA (93k) in anisole.

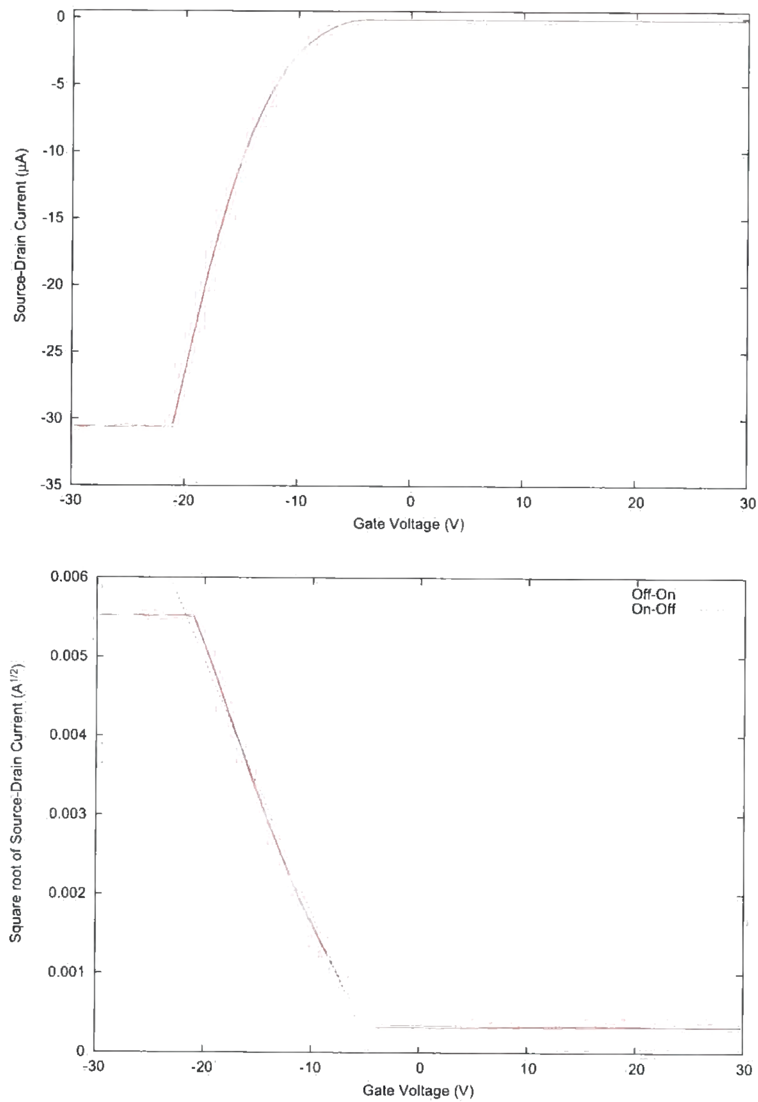
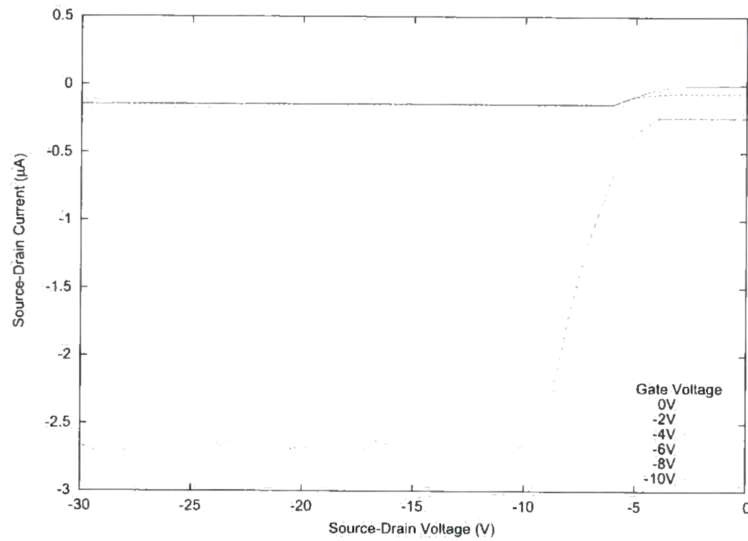
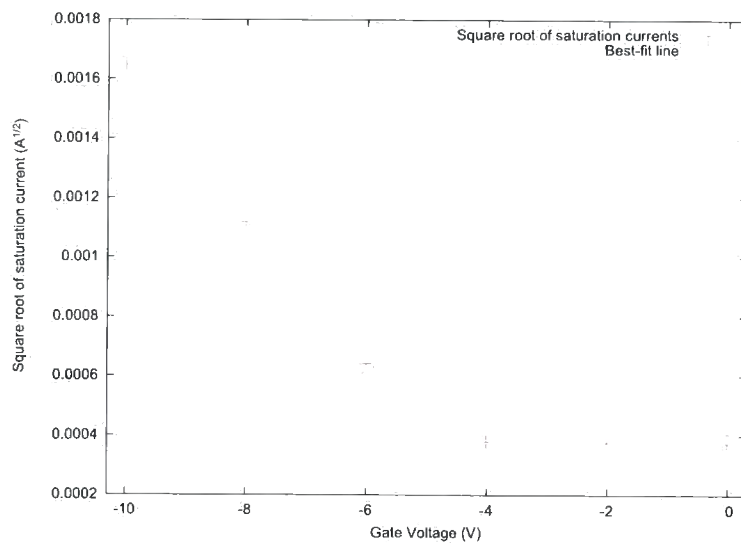


Figure 6.3: Transfer characteristics at -20 V source-drain voltage of transistor on 124 nm PMMA dielectric. There is negligible hysteresis between the on-off and off-on curves (0.11 V).



(a) Output characteristics



(b) Square root of saturation current against gate voltage

Figure 6.4: Output characteristics of transistor on 124 nm PMMA dielectric.

between the linear and saturation regions. To obtain the mobility, the square root of the saturation currents were plotted against gate voltage. Above the threshold voltage of -4.5 V, there is a linear dependence between the saturation current and the square of the gate voltage, as is predicted in simple transistor theory (equation 2.27). Applying linear regression to the above-threshold gate voltages, and using a dielectric constant for PMMA of 3.9, yields a mobility of 0.21 $cm^2/V/s$. This value is comparable to SiO_2-based transistors reported in previous sections. It was found that when thinner PMMA films were used, transistor mobilities were correspondingly reduced — with an 80 nm film, the transistors only had a mobility of 0.058 $cm^2/V/s$.

PMMA layers of 700 nm have succesfully been used in other works [6, 9] (mobilities of 0.01 $cm^2/V/s$ and threshold voltages around -15 V). It was therefore attempted to fabricate a transistor using a thicker PMMA layer. A 250 mg/ml solution of PMMA in anisole was spun for 50 seconds onto a clean silicon wafer: this film was measured to be 350 nm thick. Transfer and output currents for a typical transistor fabricated on this dielectric are shown in figures 6.5 and 6.6. Compared to the transistors fabricated on 124 nm PMMA, the currents are approximately three orders of magnitude smaller. This can be attributed to the thicker PMMA layer resulting in a smaller electric field being applied to the semiconductor, thus the reduced currents are observed. Additionally there is a larger threshold voltage shift, of approximately 3.61 V. Although at the applied voltages, the currents did not saturate, the curves indicate the onset of saturation; further increasing the source-drain voltage should demonstrate full saturation characteristics. When plotting the square root of the saturation current against gate voltage, the final values of the source-drain currents were taken as an approximation to the saturation current; the mobility calculated from this data was 4.55×10^{-5} $cm^2/V/s$.

From these results, it can be seen that PMMA is a viable alternative to silicon dioxide as a dielectric material. It appears that there should be an optimum PMMA thickness to obtain an optimal transistor mobility without leakage occurring between the gate and source-drain contacts. However, further investigation would be needed to determine an optimum thickness.

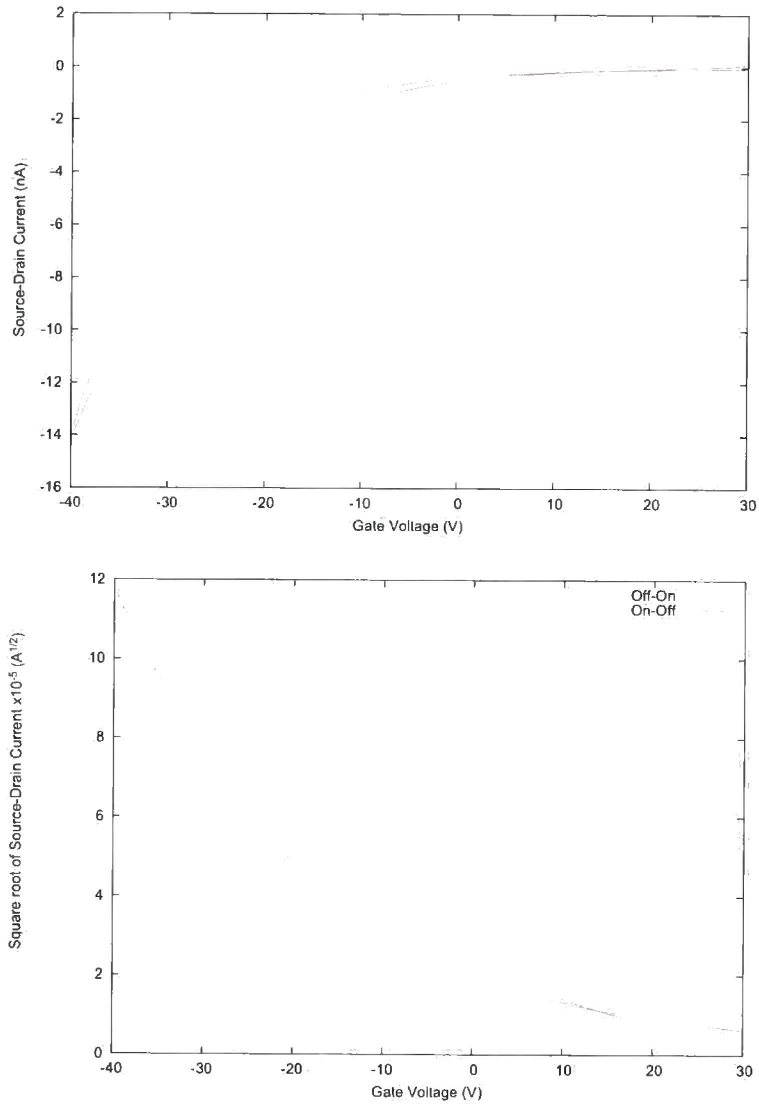
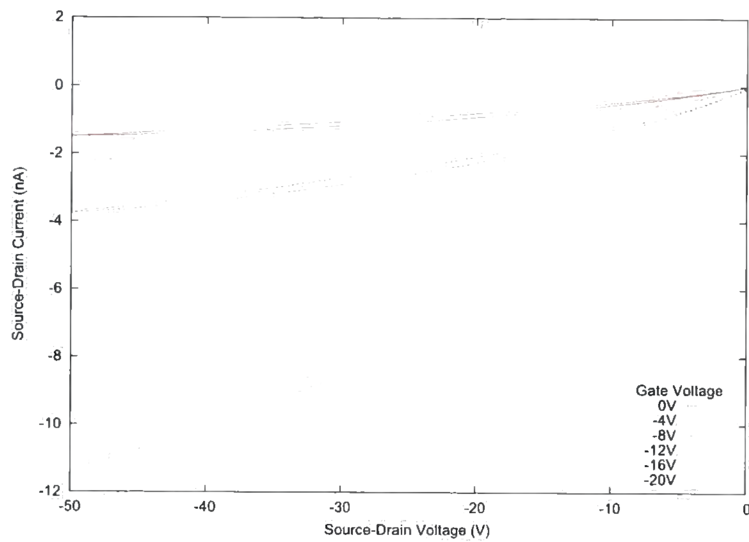
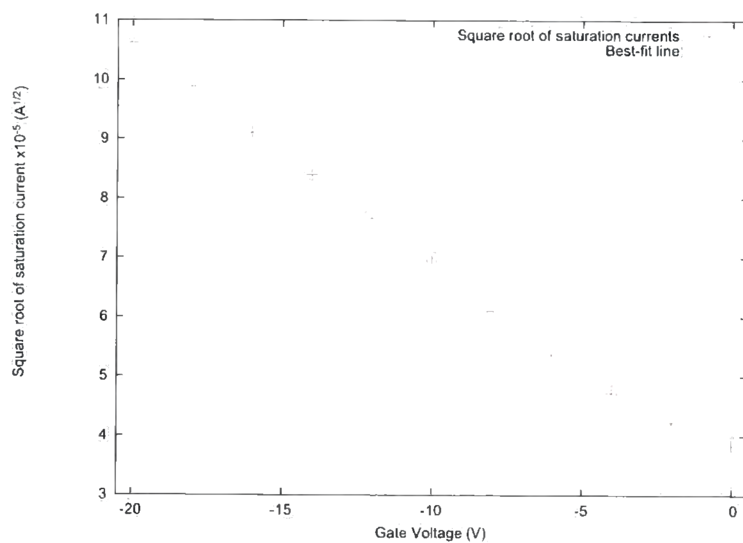


Figure 6.5: Transfer characteristics at -20 V source-drain voltage of transistor on 350 nm PMMA dielectric.



(a) Output characteristics



(b) Square root of saturation current against gate voltage

Figure 6.6: Output characteristics of transistor on 350 nm PMMA dielectric.

Sample	Silicon doping	SiO_2 thickness (nm)	Substrate temperature (°C)	HfO_2 thickness (nm) FTM*	Ellipsometer 632.8 nm	546.1 nm
P1	*p*	4.81	300	30	55.3	—
P1S	*p*	—	300	30	52.5	52.6
P2	*p*	6.95	300	25	36.3	—
P2S	*p*	—	300	25	37.0	35.0
P3	*p*	4.22	300	15	26.0	—
P3S	*p*	—	300	15	24.7	24.8
P4	*p*	8.02	200	30	54.0	—
P4S	*p*	—	200	30	55.4	53.8
P5	*p*	5.52	200	15	29.53	—
P5S	*p*	—	200	15	29.6	29.5
N1	*n*	4.25	200	25	47.3	—
N1S	*n*	—	200	25	48.7	49.6
N2	*n*	10.5	300	25	38.9	—
N2S	*n*	—	300	25	39.5	40.2

Table 6.1: Summary of hafnium oxide deposition parameters and film thicknesses.

6.3 Hafnium oxide dielectric

To investigate the performance of HfO_2 / pentacene devices, hafnium oxide was deposited onto silicon substrates, as described in section 4.2.2. Ellipsometry was used to obtain a more accurate measurement for the HfO_2 thickness than was given on the deposition chamber's film thickness monitor. The refractive index was obtained using the Cauchy formula $n(\lambda) = A + B/\lambda^2 + C/\lambda^4$ with $A = 1.875$, $B = 6.28 \times 10^3$ nm^2 and $C = 5.80 \times 10^8$ nm^4 [10], giving n(632.8 nm)=1.894 and n(546.1 nm)=1.903. Table 6.1 summarises the substrates, deposition parameters and HfO_2 thicknesses.

In order to examine the surface of the hafnium oxide, atomic force micrographs of a number of samples were taken: appendix C contains these micrographs. Figures 6.7, 6.8 and 6.9 compare the morphology of a 1 µm × 1 µm area of samples P1 and P2 with SiO_2. Even though the hafnium oxides on the samples were deposited under similar conditions, there is a significant difference in the morphology between the two samples. This may be attributed

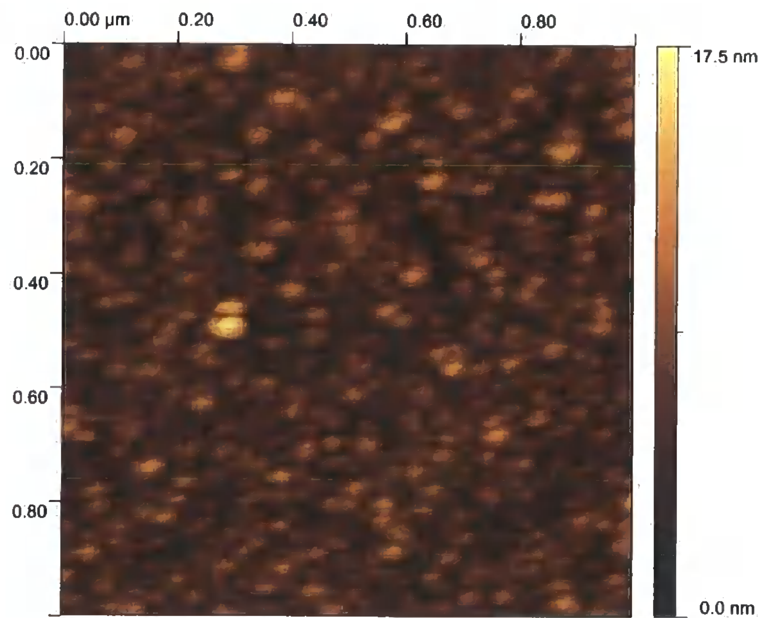


Figure 6.7: 1 µm × 1 µm AFM image of hafnium oxide, from sample P1

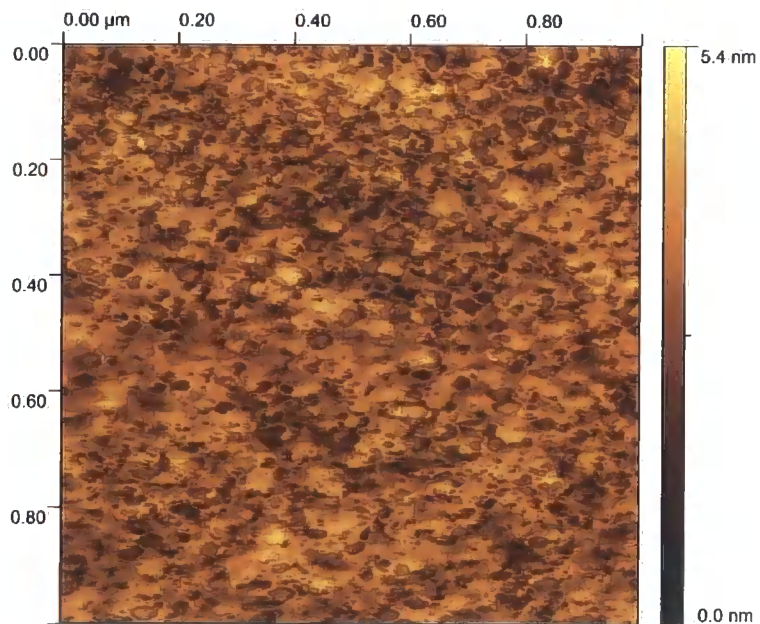


Figure 6.8: 1 µm × 1 µm AFM image of hafnium oxide, from sample P2

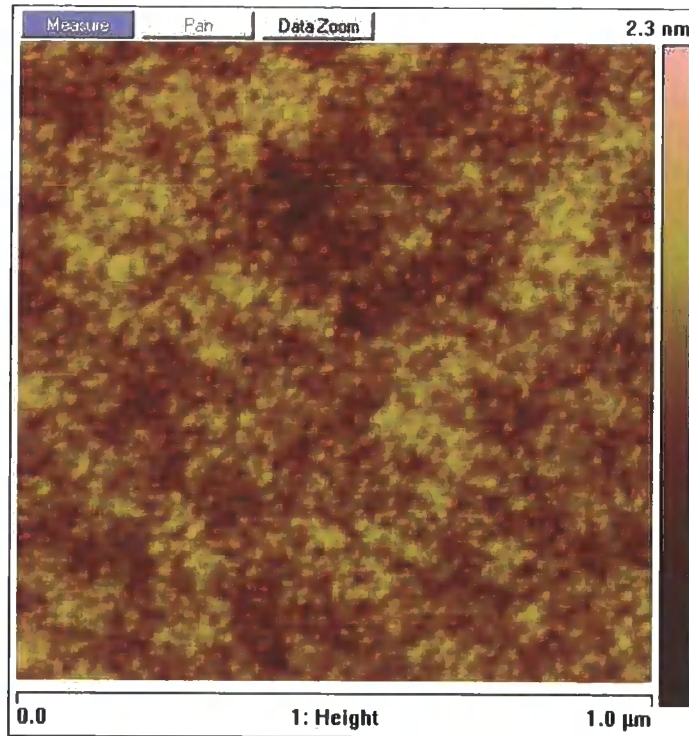


Figure 6.9: 1 µm × 1 µm AFM image of silicon oxide

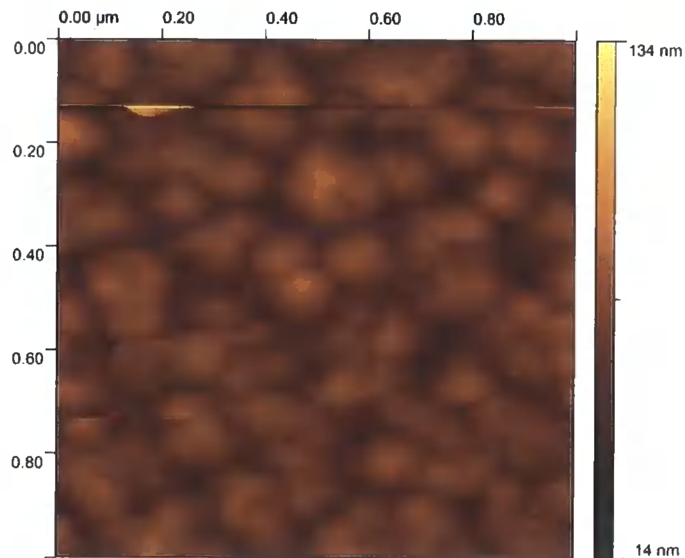


Figure 6.10: 1 µm × 1 µm AFM image of pentacene deposited on hafnium oxide, from sample P1

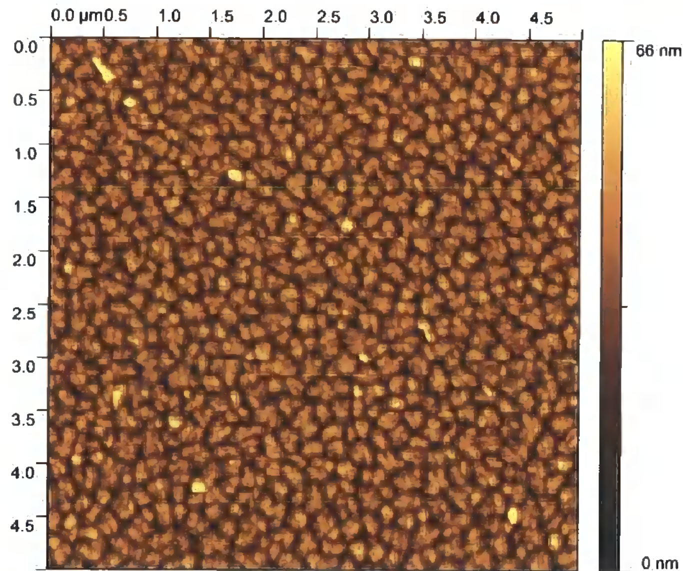


Figure 6.11: 5 µm × 5 µm AFM image of pentacene deposited on hafnium oxide, from sample P1

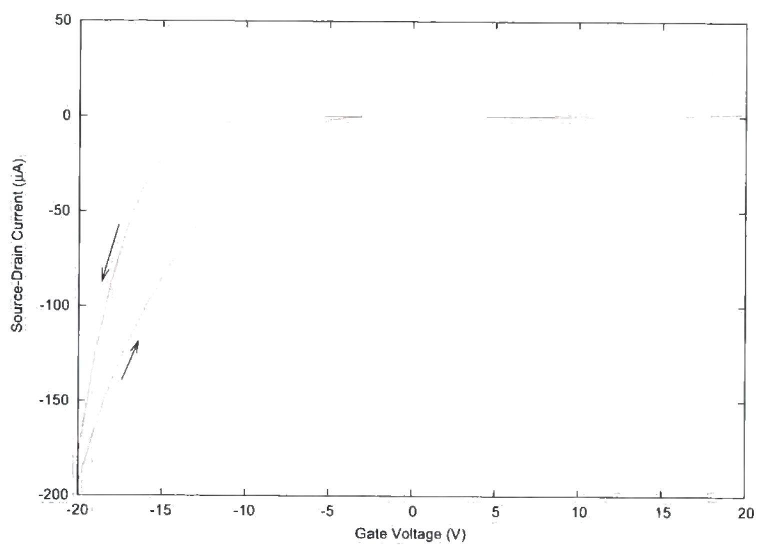
to a lack of fine control over the deposition procedure, resulting in large variations between samples. It can also be seen that the hafnium oxide surfaces are noticeably rougher than the thermally grown silicon oxide (the hafnium oxide samples have a mean roughness of 0.55 – 1.4 nm, whereas the silicon oxide sample has a mean roughness of only 0.16 nm). This roughness can be attributed to the deposition method and conditions — if the incident ions have low energy, they are less likely to migrate across the substrate surface to sites of lower surface potential (see section 3.4.1), and thus rougher surfaces result. Bhatt and Chandra [11] have reported this effect with sputtered SiO_2 films: increasing the RF sputtering power decreased the film roughness.

Figures 6.10 and 6.11 show AFM images of pentacene evaporated at 160°C, at a rate of 0.03 – 0.1 nm/s. Although the evaporation rate was similar to that yielding dendritic grain structures on SiO_2 (figure 5.4a), only small pentacene grains are observed, around 200 nm in diameter. These are similar in size to grains observed in the 'flash' evaporated pentacene, shown in figure 5.4b, but appear to have some evidence of a dendritic structure.

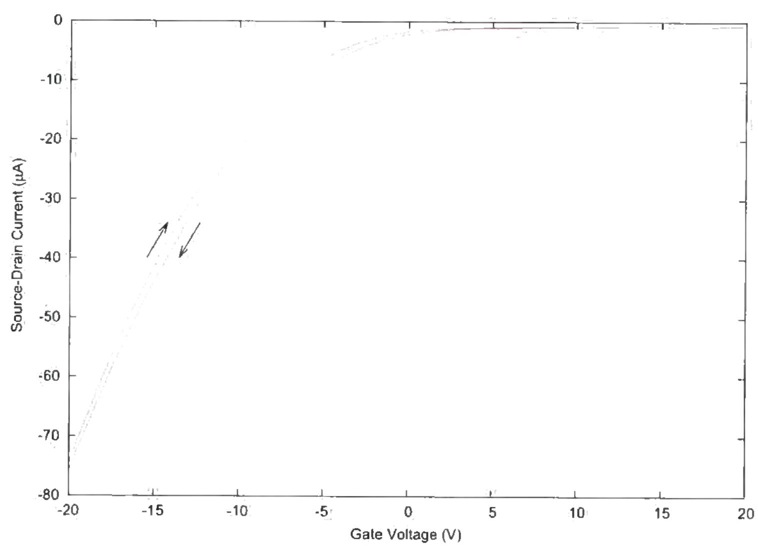
The reason for the much smaller grains on the hafnium oxide could be attributed to the surface morphology of the oxide. Due to the surface roughness, when the pentacene molecules condense on the surface, they are unable to migrate to their preferred nucleation sites. As a result they are unable to form the larger dendritic structures that are seen on the flat thermally-grown silicon oxide.

To make transistors, gold source-drain contacts were evaporated through a shadow mask, and a gate contact was established to the silicon with silver paste and aluminium foil. A number of devices under investigation appeared to be shorted between the gate and source-drain contacts; this was attributed to leaks through the dielectric layer. Figure 6.12a shows the transfer characteristics of a device fabricated on substrate N2, with a source-drain voltage of -10 V. It can be seen that the current is modified by the field effect. Compared to the highest performing pentacene device reported in this work (section 5.4.4; figure 6.12b shows the transfer characteristic of this device), it can be seen that the currents in the hafnium oxide device are approximately four times the magnitude of the silicon oxide device, even with the reduced source-drain voltage. The currents are proportional to the gate oxide capacitance; the increased dielectric constant and reduced thickness of the hafnium oxide compared to the silicon oxide increases C_{ox} and thus the higher currents are observed. There is considerable hysteresis in all of the tested devices; treating the hafnium oxide surface with an oxygen plasma had no significant effect on reducing the hysteresis. This may be attributable to the rougher surface of the HfO_2 compare to SiO_2 resulting in a larger number of charge traps that cause the hysteresis. A notable difference to the silicon oxide devices is that the hysteresis is anticlockwise rather than clockwise; i.e. the on-off threshold voltage has a smaller magnitude than the off-on threshold.

The threshold voltage shift for the device in figure 6.12a is 11 V,with both on-off and off-on threshold voltages being negative; this can be reasonably compared to a silicon oxide device cleaned with acetone and propanol, with an average threshold voltage shift of 9.7 V (section 5.4.6). Given $\Delta V_{TH} = -Q_{\text{int}}/C_{\text{ox}}$, where Q_{int} is the interface charge and $C_{\text{ox}} = \epsilon_0 \epsilon_{\text{ox}}/d_{\text{ox}}$; ϵ_{ox} for hafnium oxide is larger than for silicon oxide, and d_{ox} is smaller for the hafnium, it can be seen that, to maintain a similar ΔV_{TH}, the hafnium oxide device will



(a) Hafnium oxide device, -10 V source-drain voltage



(b) Silicon oxide device, -20 V source-drain voltage

Figure 6.12: Transfer characteristics of a pentacene device on HfO_2 and SiO_2.

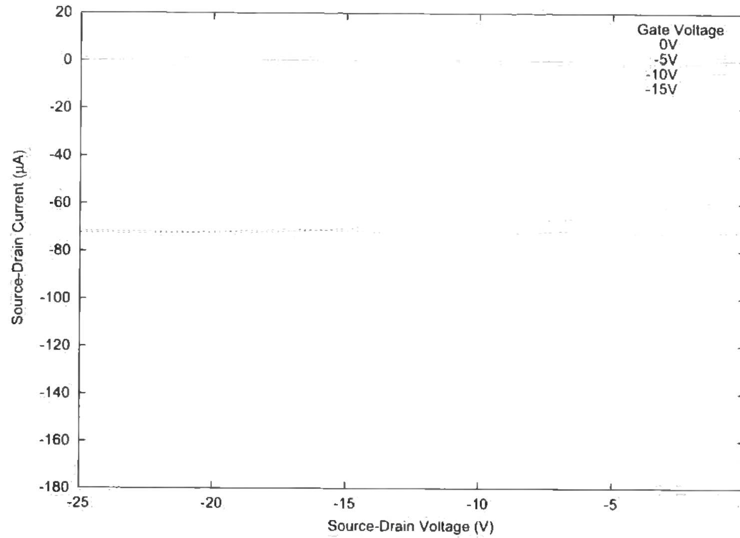
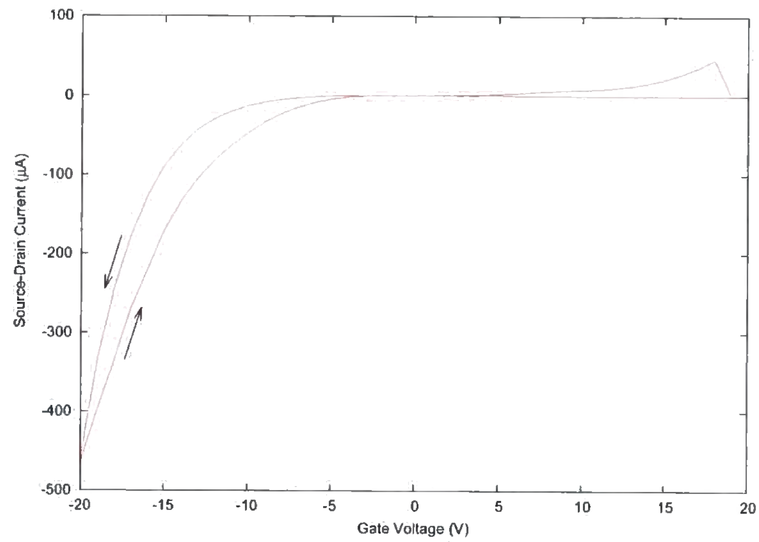


Figure 6.13: Output characteristics of HfO_2 device fabricated on substrate N2. The source-drain currents are independent of the source-drain voltage, so are most likely due to leakage between the gate and drain.

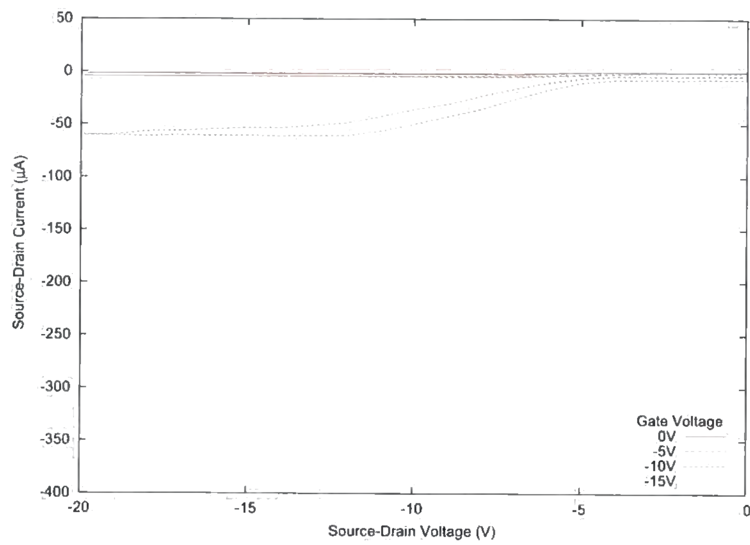
have to have a larger interface charge than the silicon oxide device. Because the threshold voltages are both negative, and the off-on threshold voltage is more negative than the on-off threshold, the interface charge is opposite polarity to that of silicon oxide devices — i.e. the hafnium oxide contains hole traps rather than electron traps. As the gate bias is made negative, hole trapping states become populated, causing a negative shift in the off-on threshold voltage. When sweeping from on to off, extra electrons are induced to balance the stored holes, hence resulting in larger currents for the on-off sweep.

Figure 6.13 shows the output characteristics of the device whose transfer characteristics are shown in figure 6.12a. The source-drain currents are independent of the source-drain voltage, therefore are most likely due to leakage currents between the gate and drain contacts.

Figure 6.14 shows the transfer and output characteristics of a device fabricated on substrate N2S. The hysteresis is smaller than that of the device on substrate N2, with a threshold voltage shift of 5 V. The output characteristics show evidence of a linear region and a saturation region (above the gate threshold voltage), however there is a large amount of hysteresis in the source-drain current. The mobility for this device may be obtained by plotting the square



(a) Transfer characteristics at -5 V source-drain voltage



(b) Output characteristics

Figure 6.14: Characteristics of transistor on 40 nm HfO_2 dielectric.

root of the source-drain current against gate voltage from the transfer characteristic, and using the gradient obtained in the linear portion in equation 2.29. For the off-on sweep, taking the dielectric constant of HfO_2 to be 21 [1] and the thickness to be 40 nm, this gives a mobility of 0.59 $cm^2/V/s$.

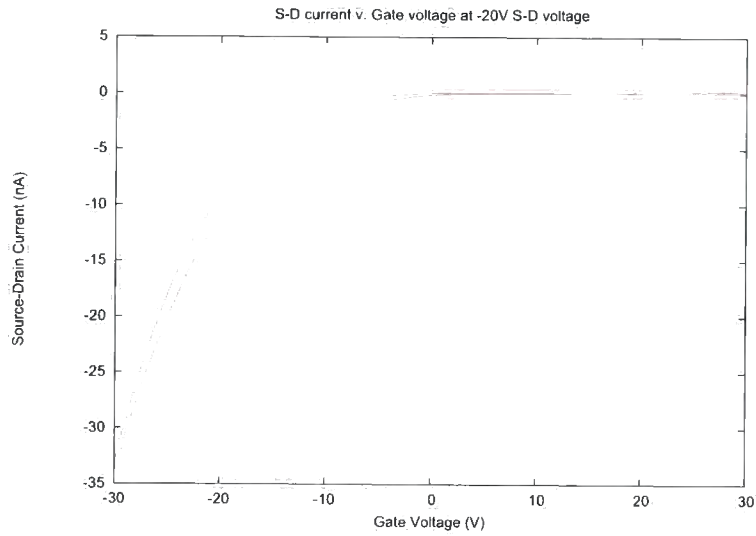
From the measured devices, it appears that it may be possible to fabricate transistors using only hafnium oxide as the dielectric, however, the quality of the deposited films would need to be improved. Current favourable results ([4,5]) have been obtained using an Al_2O_3/HfO_2 two layer dielectric, deposited using atomic layer deposition.

6.4 A transistor on a flexible substrate

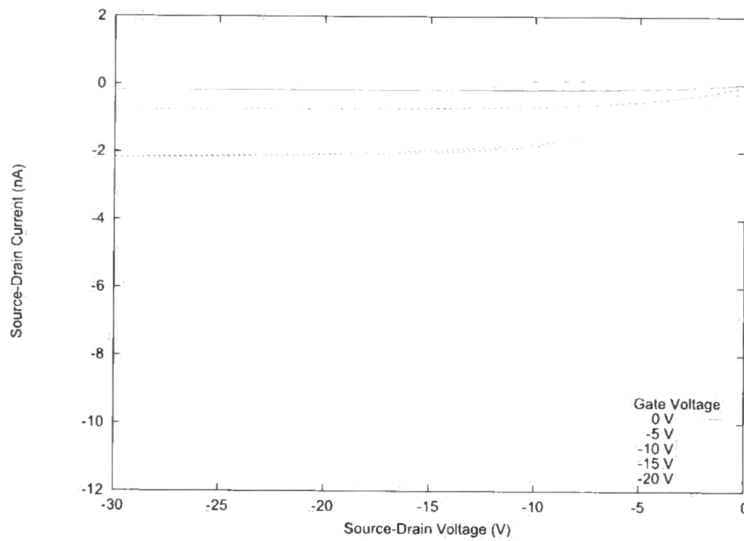
An attempt was made to fabricate a transistor on a flexible substrate. To ensure that the substrate was flat during processing, a silicon wafer was used to hold the substrate.

Gold was sputtered onto a clean silicon wafer to assist in detaching the flexible substrate from the wafer. To form the substrate, five layers of Pyralin PI2525 polyimide, from HD Microsystems, were spin coated onto the wafer; each layer was spun at 500 rpm for 5 seconds, followed by 2300 rpm for 30 seconds to give a 10 μm thick layer, then softbaked at 120°C for 30 seconds and 150°C for a further 30 seconds. The polyimide was cured using the following cure profile: heating from room temperature to 200°C, ramp rate 4°C/minute in air; hold for 30 minutes at 200°C in air; heating from 200°C to 300°C, ramp rate 2.5°C/minute in nitrogen; hold for 60 minutes at 300°C in nitrogen; gradual cooling to room temperature [12].

360 nm of aluminium was evaporated on top of the polyimide to form the gate for the transistors. On top of this, ~350 nm of PMMA was spin-coated to provide the dielectric; this was baked for 2 minutes at 120°C. Pentacene and gold source-drain contacts were evaporated on top of the PMMA. To allow contact to the aluminium gate, some PMMA was removed using acetone. A photograph of the device is shown in figure 6.16. The transfer and output characteristics are given in figure 6.15. The transfer characteristic displays very low hysteresis (a 2 V change in the threshold voltage), and both off–on



(a) Transfer characteristic at -20 V source-drain voltage



(b) Output characteristic

Figure 6.15: Characteristics of transistor fabricated on polyimide substrate.

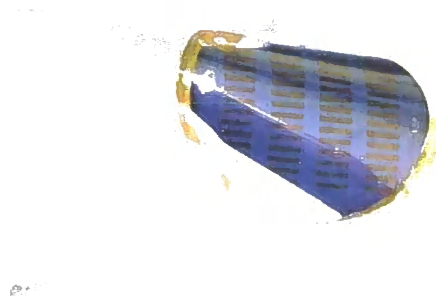


Figure 6.16: Photograph of a transistor on a polyimide substrate.

and on–off threshold voltages are negative. The output shows reasonably good saturation at higher source-drain voltages, although there is a leakage current present. Using the saturation currents, and taking the dielectric constant of PMMA to be 3.9, the mobility comes out to be 1.5×10^{-4} cm^2/V/s.

The characteristics and mobility of this transistor were noticeably better than those reported for a transistor fabricated on a similar thickness of PMMA in section 6.2. It is likely that using a thinner dielectric layer would improve the device performance.

6.5 Summary

Experiments were undertaken to replace the silicon oxide dielectric with an organic dielectric and a high-k dielectric. PMMA was found to behave reasonably well as an insulator, with devices showing little hysteresis, and mobilities comparable to those fabricated on silicon oxide. Sputtered hafnium oxide was found to be non-ideal as a dielectric, with a number of devices either shorting out or showing no dependence between the source-drain voltage and current. One device that exhibited some transistor characteristics was found to have a mobility of 0.59 cm^2/V/s, demonstrating that hafnium oxide could have good potential if deposited using an alternative method which would result in a non-leaky dielectric layer. Finally, an attempt was made to fabricate a transistor on a flexible substrate using a PMMA dielectric.

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[12] HD Microsystems™, *Product Information Pyralin®PI2525, PI2555, PI-2575 & PI2556.*
HD Microsystems™.

7

Dibenzothiophene-based OTFTs

7.1 Introduction

Although acenes (specifically pentacene) are well known and often used organic semiconductors, other materials may be, and have been, used. The dibenzothiophene moiety has been the subject of some study, as it has been found to exhibit high hole mobilities of 0.15 $cm^2/V/s$ and device on-off ratios of $> 10^6$ [1] (see also section 2.4). Incorporation of an electron deficient dibenzothiophene-*S*,*S*-dioxide group into a material will increase its electron affinity [2], thus offering a strategy for the design of *n*-channel devices. This chapter gives results for three materials based on the dibenzothiophene moiety, all synthesised in the Chemistry Department of the University of Durham.

7.2 IR-35F

7.2.1 Physical characterisation

Chemical structure

IR-35F (3,7-bis(dibenzothiophene-4-yl)-dibenzothiophene-*S*,*S*-dioxide ($C_{36}H_{20}O_2S_3$); molecular weight 580.74) is a dibenzothiophene-based molecule, incorporating the electron deficient dibenzothiophene-*S*,*S*-dioxide group. The chemical structure is shown in figure 7.1.

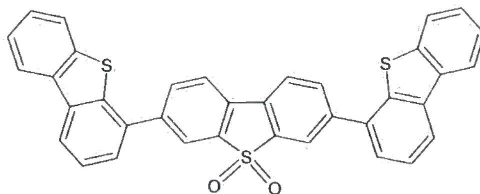


Figure 7.1: The IR-35F molecule.

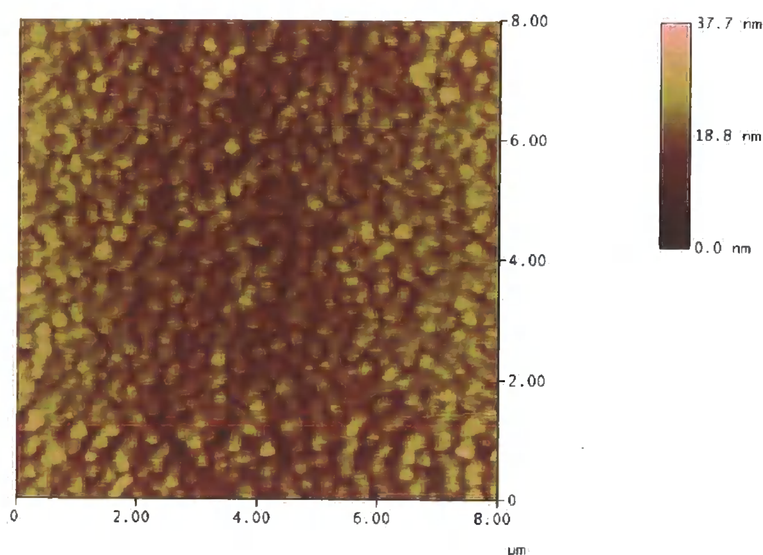


Figure 7.2: AFM image of thermally evaporated IR-35F on glass.

Film morphology

Figure 7.2 shows an atomic force micrograph of a 30 nm thermally evaporated IR-35F film on glass. The morphology is similar to that of flash-evaporated pentacene (figure 5.4b), consisting of small, irregular grains, around 300 nm in size. Pentacene, evaporated under similar conditions onto glass had a grain size of 100–200 nm. The small grain structure is most likely due to the evaporation taking place in the home-built evaporator, which did not allow for fine control of the evaporation procedure.

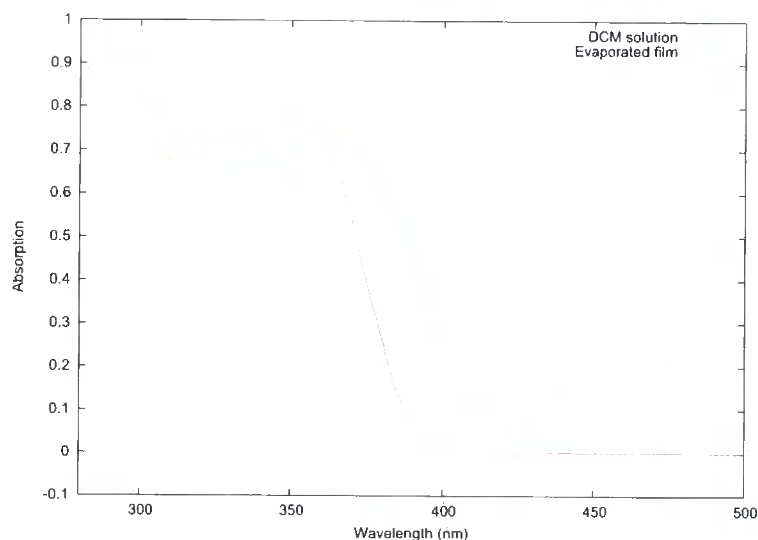


Figure 7.3: Absorption spectra of IR-35F in DCM and evaporated film.

Absorption spectrum

Figure 7.3 shows the UV-VIS absorption spectra of IR-35F in dichloromethane (DCM) and as an evaporated film. The two spectra are broadly similar, indicating the material did not dissociate during deposition, however some significant differences are apparent. The spectrum of the evaporated film is broader than that of the solution, with fewer well defined features. The evaporated film spectrum is also red shifted compared to the solution. Similar effects have been reported for solutions and thin films of phthalocyanines and perylene [3, Chapter 5]; these were attributed to the formation of aggregates or interactions between molecules making up the solid film. The evaporated film starts absorbing around 420 nm, corresponding to an energy of 3.0 eV. This may be the band gap of IR-35F — electrons are excited from the HOMO to the LUMO bands at this energy; however, no other data are available to confirm this. Below 300 nm, absorption from the glass substrate becomes significant, and hence no useful absorption data for the film can be obtained.

A photograph of a ~300 nm thick IR-35F film (measured as a step height on an AFM) on a glass slide, next to a clean glass slide, is shown in figure 7.4. The film appears to be very pale yellow in colour.

Figure 7.4: Photograph of IR-35F on glass slide (75 × 25.4 mm each).

7.2.2 Electrical characterisation

To measure the electrical conductivity of IR-35F, a set of gold contacts, 34.9 mm long with 1.4 mm separation were evaporated through a shadow mask onto a 300 nm thick IR-35F layer on a glass microscope slide. In-plane currents at voltages varying between -50 V and +50 V (in steps of 1 V) were measured across a number of contacts in a number of environments. Figure 7.5 gives an indication of the resistance of the IR-35F film between adjacent contacts in a number of environments. The graph shows the film has very low conductivity — applying linear regression to the I-V curves yields a resistance of 2×10^{12} Ω of IR-35F under UV light*, and 3×10^{12} Ω for the other conditions. This increase in conductivity under UV light correlates to the increase in absorption of the molecule at shorter wavelengths.

Given the resistances of the glass slide and glass slide with IR-35F are very similar, no conclusions can be drawn as to how much of the current is carried by the IR-35F and how much by the glass itself. However, there is evidence that in the presence of UV light, the number of charge carriers in the IR-35F film increases, and hence some more current is carried by the IR-35F.

*The UV wavelength used was 253.7 nm

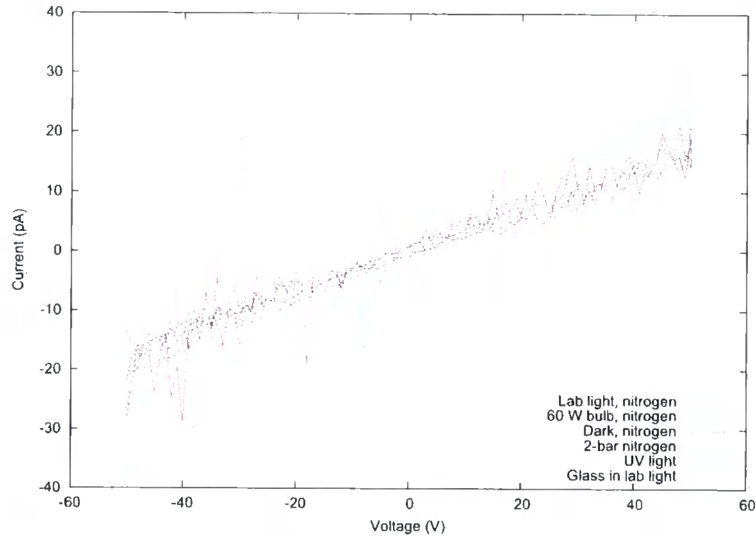


Figure 7.5: I-V characteristics for IR-35F in various environments, and for a glass slide in ambient light.

The variation of conductivity with temperature follows the relation

$$\sigma = \sigma_0 \exp\left(-\frac{\Delta E}{kT}\right) \tag{7.1}$$

where ΔE is the activation energy, k is Boltzmann's constant, and T is the temperature [4, Chapter 2]. Figure 7.6 shows a plot of ln(conductance) against $1/T$ for both a clean glass slide and IR-35F on a glass slide. The activation energy can be obtained from the gradient of the slope, $\Delta E/k$. Using linear regression to obtain best-fit lines yields an activation energy of 1.13 eV for the clean glass slide, and 1.2 eV for the IR-35F film. This confirms that it is likely that almost all of the current is going through the glass slide.

7.2.3 Transistor device

Transistor devices were fabricated in the top-contact configuration, using ~30 nm IR-35F as the active layer, evaporated at a rate of ~0.1 nm/s. Figure 7.7 shows the saturation transfer characteristics (source-drain held at +70 V) of one of the devices. An increase in current due to the field effect is evident

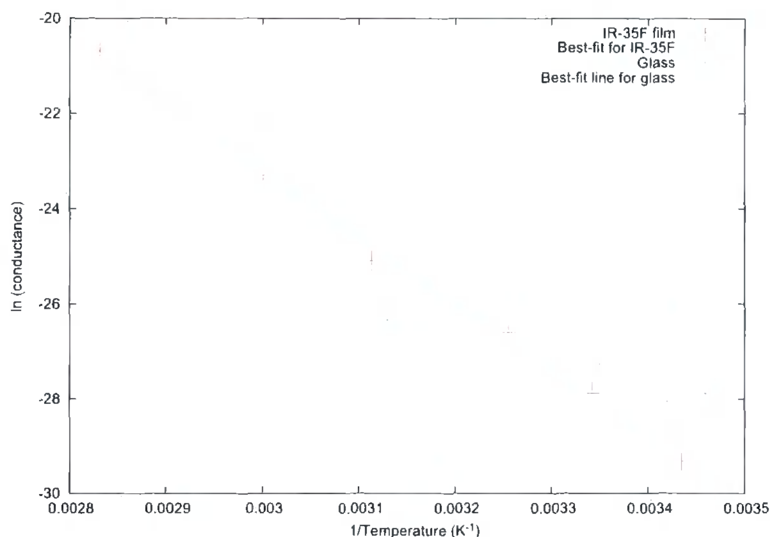
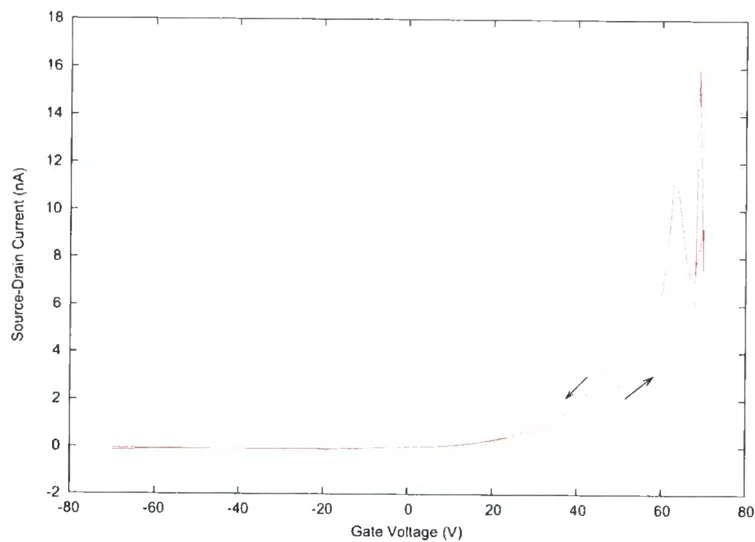


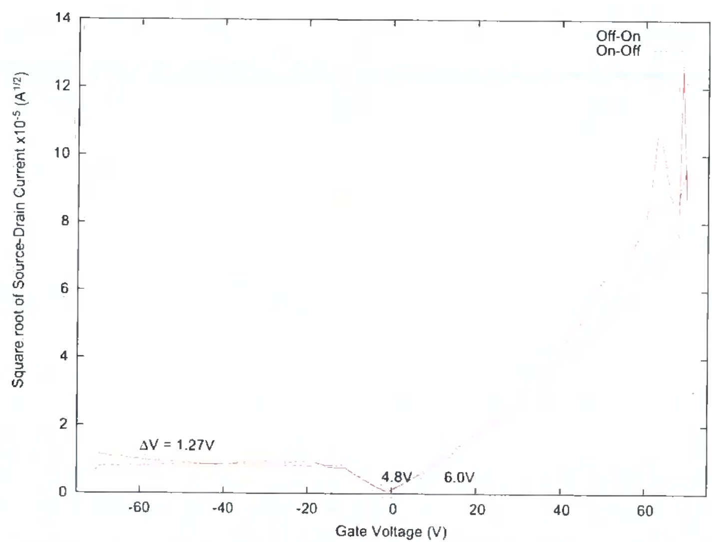
Figure 7.6: ln(conductance) against temperature reciprocal for IR-35F film and glass.

when a positive gate voltage is applied. It can also be seen there is only a small hysteresis in the transfer characteristic. Plotting the square root of the drain current and fitting a line to the linear portion yields a threshold voltage of 4.8 V for the off-on sweep, and 6.0V for the on-off sweep. The device therefore appears to act as an n-channel enhancement mode device, confirming the IR-35F is an n-type semiconductor.

The output characteristics are shown in figure 7.8. The devices exhibited good saturation, however the output characteristic outside the saturation region is non-linear. This can be attributed to contact effects between the metal contact and organic semiconductor, where the metal forms a Schottky barrier with the semiconductor, rather than an ohmic contact [5]. Plotting the square root of the saturation current against gate voltage to obtain mobility shows that the saturation currents do not conform to the simple transistor model: there appears to be a fourth order relationship between the saturation currents and the gate voltage. Attempting a linear fit to the curve results in a carrier mobility of 3.45×10^{-6} cm^2/V/s [6]. Although this is very low, it is likely that it could be improved by improving the film deposition, which may possibly result in an improved crystal structure as with pentacene; or using a lower work function metal, such as aluminium, to form the source-drain contacts.

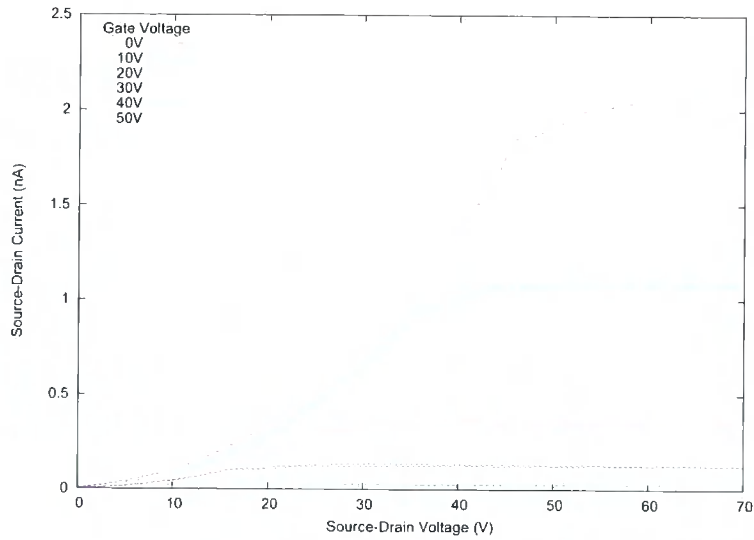


(a) Transfer characteristic

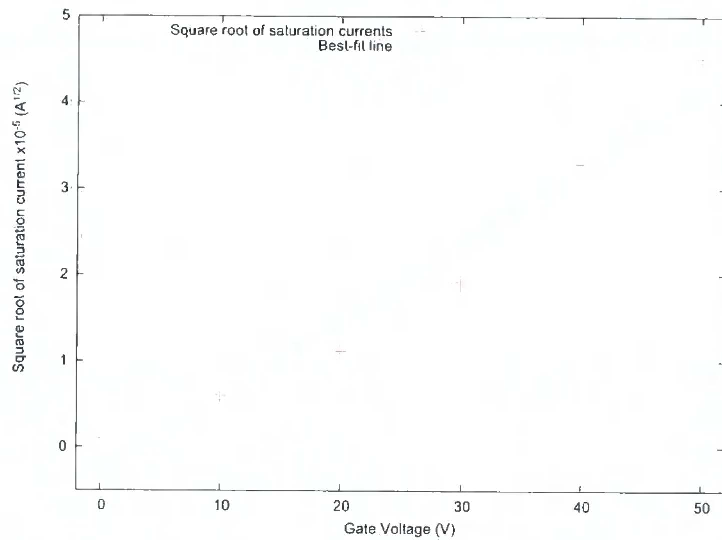


(b) Transfer characteristic showing the square root of the source-drain current

Figure 7.7: Transfer characteristics of IR-35F transistor at +70 V source-drain voltage.



(a) Output characteristic



(b) Square root of saturation currents against gate voltage

Figure 7.8: Output characteristics of IR-35F transistor.

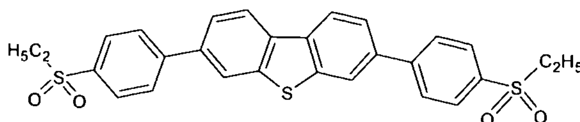


Figure 7.9: The EC-08A molecule.

7.3 EC-08A

The results of the IR-35F devices showed that the material had potential for an n-type semiconductor. It was thought that increasing the number of electron deficient groups could increase the charge carrier mobility of the devices.

7.3.1 Physical characterisation

Chemical structure

The chemical structure of EC-08A (3,7-bis(4-(ethylsulfonyl)phenyl)dibenzo-[b,d]thiophene ($C_{28}H_{24}O_6S_3$); molecular weight 552.68) is shown in figure 7.9.

Absorption spectrum

Figure 7.10 shows the UV-VIS absorption spectra of EC-08A in DCM and as an evaporated film. As with IR-35F, the material is fairly transmissive, with significant absorption only occurring below ~380 nm. The spectrum of the evaporated film is broader and not as well defined as that of the DCM solution, although the two spectra are otherwise broadly similar, indicating the EC-08A did not dissociate during evaporation. As with IR-35F, the thin film spectrum is red shifted compared to the DCM solution. The absorption of the film starts around 390 nm, corresponding to an energy of 3.2 eV. This may be the bandgap of the molecule, however no other data are available to confirm this. In general, the HOMO and LUMO levels would need to be measured to determine the bandgap. At shorter wavelengths, the absorption of the evaporated film is, other than for some noise, very high — this can be attributed to the glass substrate absorbing the UV light.

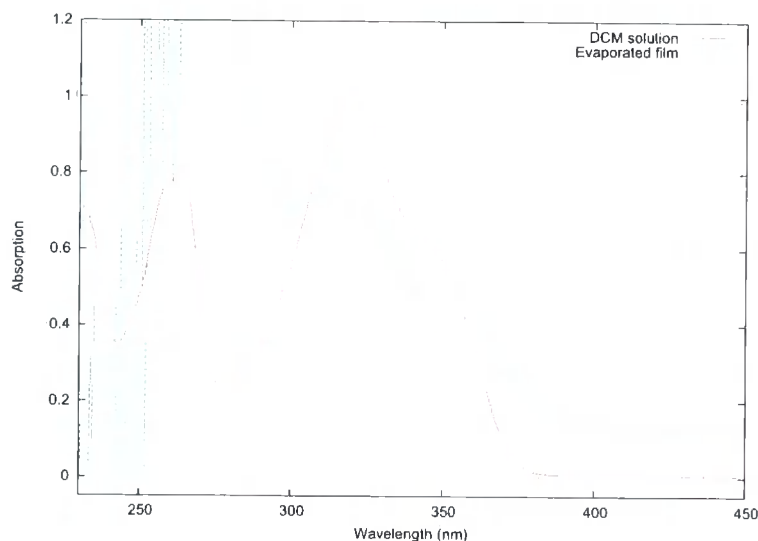
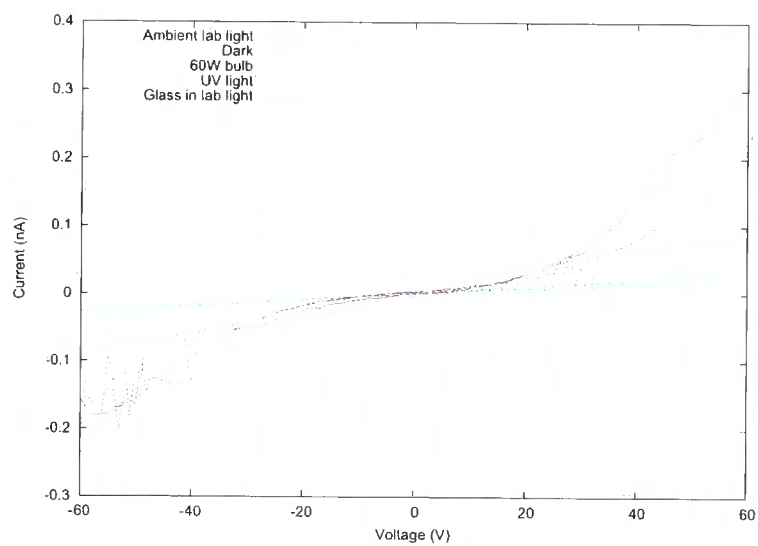


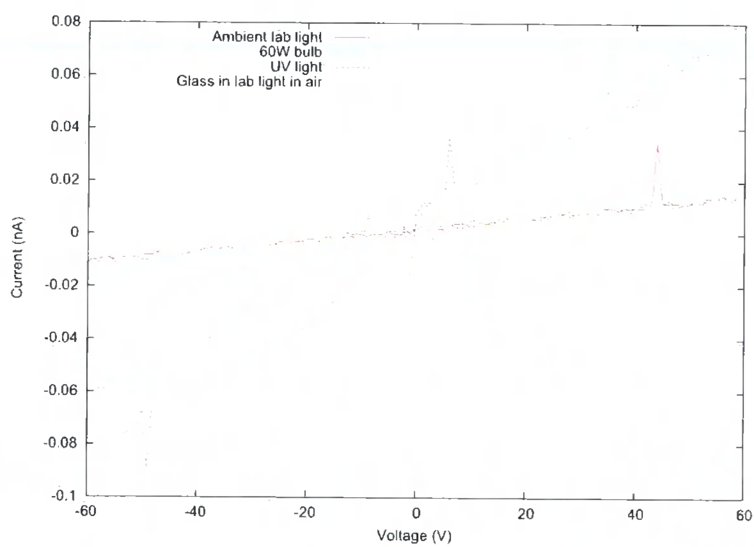
Figure 7.10: Absorption spectra of EC-08A in DCM and evaporated film.

7.3.2 Electrical characterisation

To measure the electrical conductivity of EC-08A, a set of aluminium contacts, 34.9 mm long with 1.4 mm separation were evaporated through a shadow mask onto a 120 nm thick EC-08A layer on a glass microscope slide. Currents and voltages varying between -60 V and +60 V (in steps of 1 V) were measured across adjacent contacts in a number of environments. Figure 7.11 gives an indication of the resistance of the EC-08A films under various lighting conditions, both in air and under vacuum. It can be seen that the two characteristics are substantially different: under vacuum, the film behaves as an ohmic conductor, whereas in air, the characteristics are noticeably non-ohmic. Under vacuum, the resistance of the film is approximately the same under both ambient lab light and under a 60 W incandescent bulb — applying linear regression to the I-V curves yields a resistance of $\sim 4.5 \times 10^{12}\ \Omega$ — whereas under a UV light, the resistance decreases to $7.7 \times 10^{11}\ \Omega$. These values are very similar to those for glass; only under UV light there are enough charge carriers in the film to be able to differentiate between current carried by the glass substrate and current carried by the EC-08A film. In air, the conductivity of the EC-08A was highest under ambient lab light, and reduced under UV light. However, after keeping



(a) Air



(b) Vacuum

Figure 7.11: I-V characteristics for EC-08A in various environments.

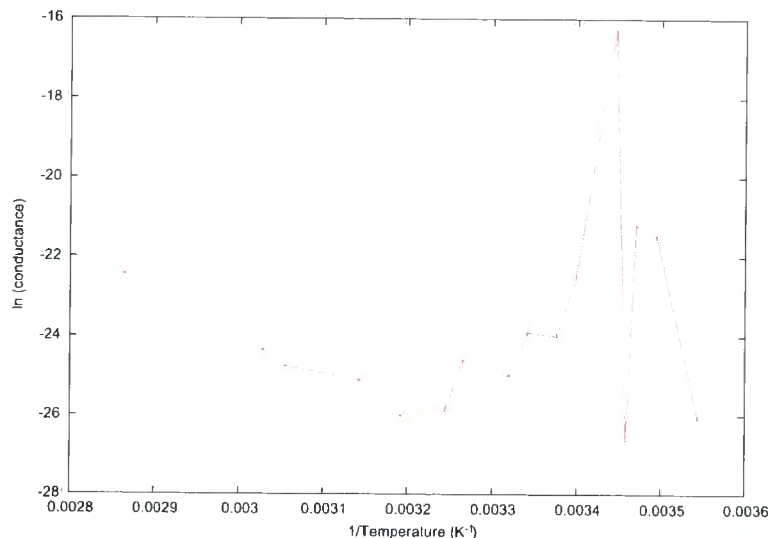


Figure 7.12: ln(conductance) against temperature reciprocal for EC-08A film in air.

the film under vacuum in a desiccator for a few days, then re-measuring the I-V characteristics in air, under ambient lab light and UV light, it was found that the conductivity was higher under UV light than in ambient light, but the film again showed non-ohmic current-voltage dependence. A possible explanation for this behaviour is that in air the EC-08A film absorbs moisture and oxygen — this then leads to a shift in the energy bands of the molecule, so that there is no longer an ohmic contact between the metal and the semiconductor; instead, charge is injected from the metal into the semiconductor. Under vacuum, absorbed moisture is drawn out of the molecule, causing the energy bands to shift back to levels where an ohmic contact is made between the metal and the semiconductor.

In an attempt to find the activation energy of the EC-08A films, resistances at a number of temperatures were obtained. Figure 7.12 shows a plot of ln(conductance) against the reciprocal of temperature in air. The activation energy could not be determined from this plot as the curve does not follow a straight line.

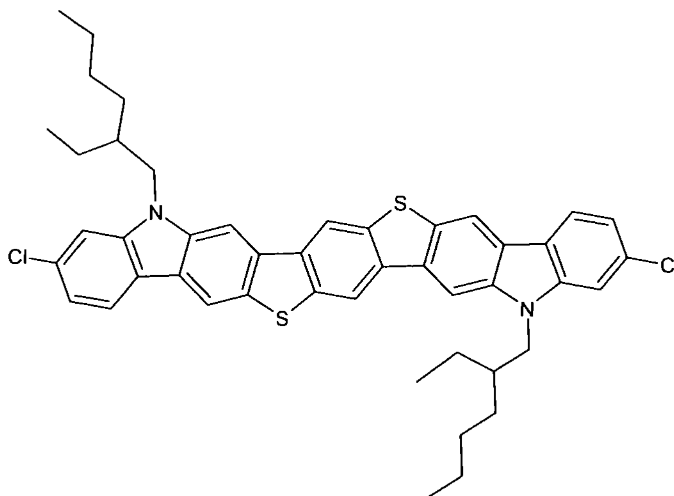


Figure 7.13: The CSW-652 molecule.

7.3.3 Transistor device

None of the EC-08A-based transistor structures exhibited any field-effect behaviour. It was therefore concluded that despite the structural similarities between IR-35F and EC-08A, the addition of the extra electron deficient groups and the ethyl groups to the molecule altered its properties in a way that stopped the semiconducting behaviour that was apparent in IR-35F.

7.4 CSW-652

7.4.1 Physical characterisation

Chemical structure

CSW-652 ($C_{46}H_{46}Cl_2N_2S_2$; molecular weight 761.9) is a molecule based on dibenzothienobisbenzothiophene (DBTBT) [1]. Its chemical structure is shown in figure 7.13. In contrast to the previously reported molecules, this molecule was predicted to be a p-type semiconductor, due to the lack of any electron-deficient groups.

Film morphology

Figure 7.14 shows an atomic force micrograph of a film of CSW-652 on silicon oxide, and, for comparison, an atomic force micrograph of silicon oxide on the same scale. An AFM step-height measurement showed the thickness of the film to be around 25-30 nm. The film appears to follow the morphology of the underlying silicon oxide: no obvious crystal structure is visible in the CSW-652 AFM scan; increasing the scan area to 30 μm × 30 μm continued to show no obvious long-range crystal structure to the film.

The non-crystalline structure of the film can be attributed to the carbon chains off the molecule preventing the molecule from forming an ordered crystal structure.

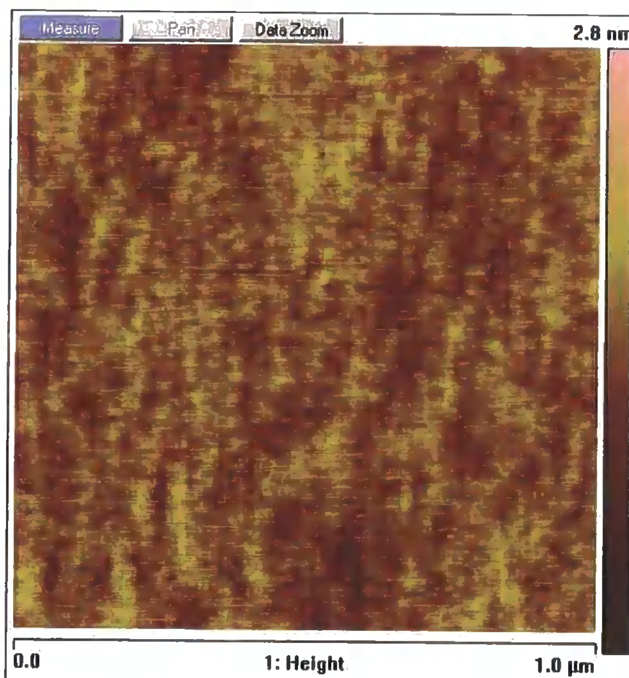
Absorption spectrum

A UV-VIS-NIR absorption spectrum was taken of a CSW-652 film on a glass slide. However, no differentiation could be made between the absorption spectrum of the film and that of a clean glass slide, therefore no conlusions can be drawn about the molecule from this experiment.

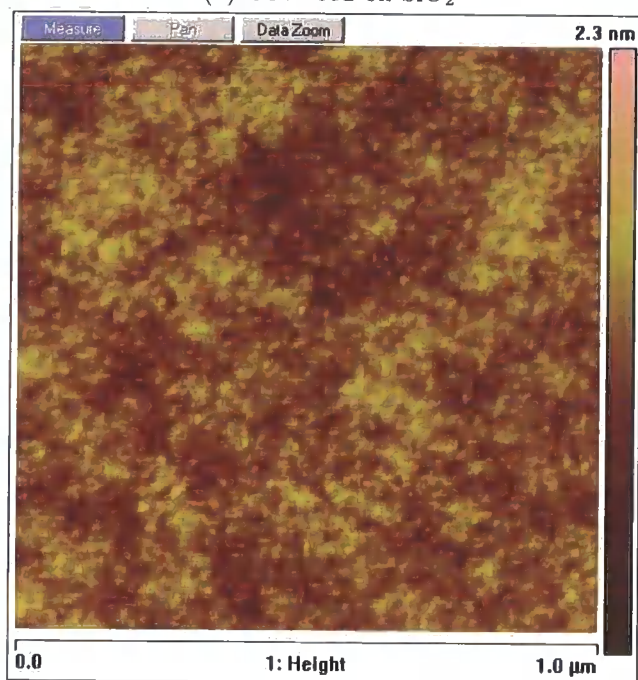
7.4.2 Transistor device

Transistor devices were fabricated in the top-contact configuration, using ~ 30 nm CSW-652 as the active layer, evaporated at a rate of ~ 0.05 nm/s. Figure 7.15 shows the saturation transfer characteristics (source-drain held at -40 V) of one of the devices. An increase in current as a negative gate voltage is applied is evident. There is a small amount of hysteresis present, which can be attributed to charge trapping on the silicon oxide surface.

The output characteristics are shown in figure 7.16. The devices exhibited reasonable saturation, with the IV characteristics outside the saturation region appearing linear. Plotting the square root of the saturation currents against gate voltage to obtain mobility indicates that the devices conform fairly well to the simple transistor model, giving a mobility of 3.71×10^{-5} cm^2/V/s. Although the mobility value is very low, which can be attributed to the lack of a good crystal structure, the transistors demonstrate good saturation, and good linearity in the linear region of the output characteristics. As predicted from the molecular structure, the film behaved as a p-type semiconductor.

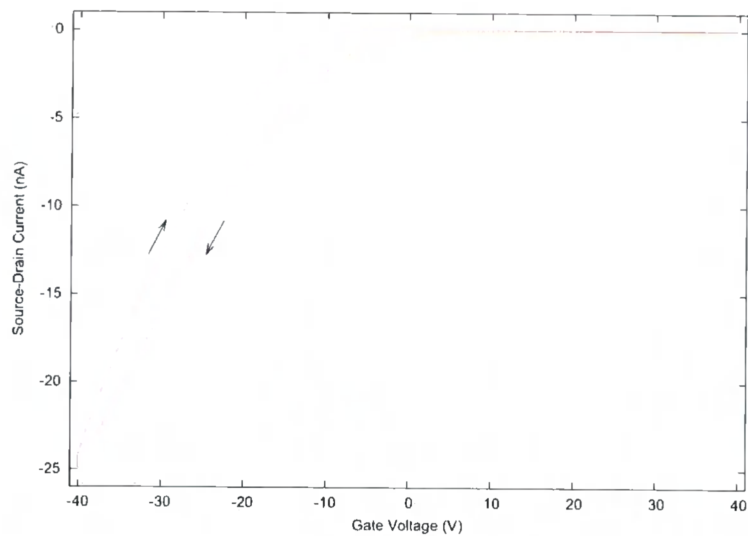


(a) CSW-652 on SiO_2

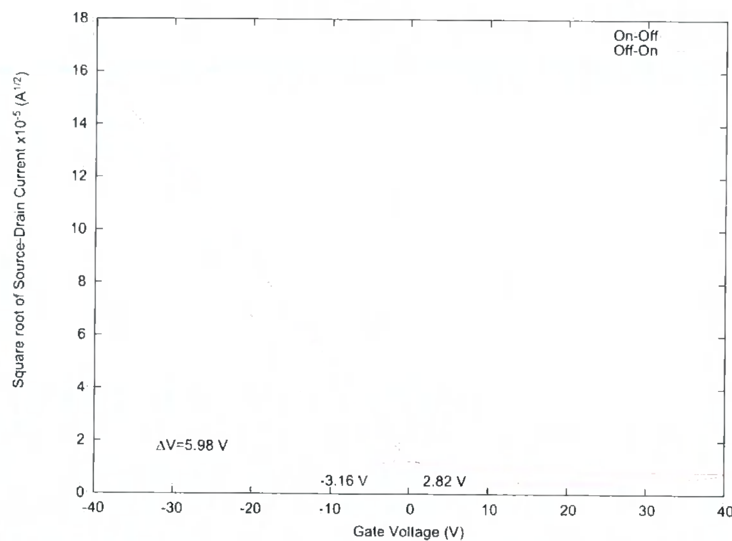


(b) SiO_2

Figure 7.14: 1 µm × 1 µm atomic force micrograph of CSW-652 on SiO_2, and SiO_2.

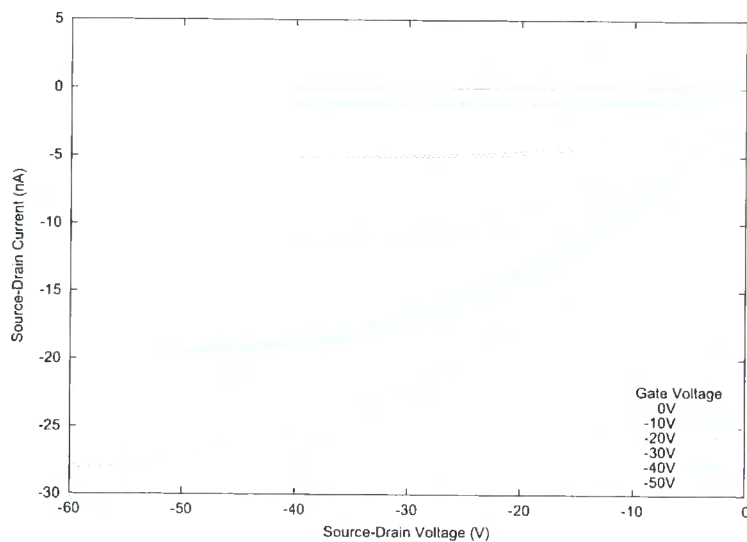


(a) Transfer characteristic

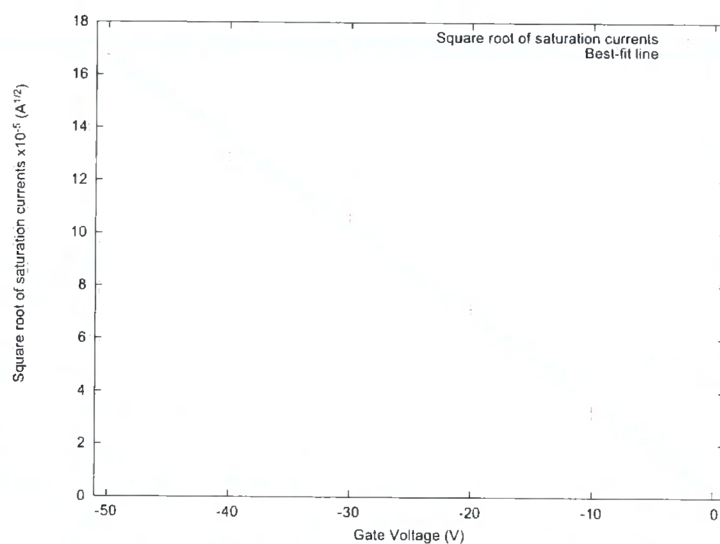


(b) Transfer characteristic showing the square root of the source-drain current

Figure 7.15: Transfer characteristics of CSW-652 transistor at -40 V source-drain voltage.



(a) Output characteristic



(b) Square root of saturation currents against gate voltage

Figure 7.16: Output characteristics of CSW-652 transistor.

7.5 Summary

Physical and electrical characterisation were performed on three new materials synthesised in the Department of Chemistry and the University of Durham. IR-35F was found to be an air-stable n-type semiconductor, with a possibility of improving its performance through optimising deposition conditions and device fabrication. EC-08A was thought to have a possibility of better mobility than IR-35F due to the increased electron deficient groups, however was found to exhibit no transistor behaviour. CSW-652 was found to exhibit the properties of a p-type semiconductor with good transistor characteristics, but low mobility. The low mobility was attributed to the lack of a good crystal structure of the deposited film, which in turn was attributed to the carbon chains off the molecule inhibiting any large-scale crystal growth.

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8

Conclusions and further work

8.1 Conclusions

The purpose of this research was to characterise pentacene and pentacene-based field effect transistors on silicon oxide, and examine the effects of various SiO_2 surface treatments on these transistors; to compare the devices fabricated on silicon oxide with ones made on alternative dielectrics (PMMA and HfO_2); and to investigate the properties of some new materials synthesised in the Department of Chemistry at the University of Durham.

Physical and electrical characterisation of evaporated pentacene films found the properties of the films to be comparable to the published literature on pentacene films [1–4]. Initial measurements on transistor devices showed poor mobilities; however, as the fabrication process was improved, mobilities increased considerably. The grain size of the evaporated pentacene was found to be key to optimising the mobilities — controlled evaporation of pentacene allowed the pentacene to form dendritic crystals of a few micrometres in size: a mobility of 0.54 $cm^2/V/s$ was obtained with a grain size of 2–3 μm, whereas a grain size of 0.5 μm only yielded a mobility of 0.2 $cm^2/V/s$. Uncontrolled evaporation of pentacene led to a film morphology consisting of small, irregular grains; transistors fabricated on these films had mobilities of the order of 10^{-2} - 10^{-3} $cm^2/V/s$.

The mobility of transistors across a silicon wafer was found to vary by up to a factor of three. This was attributed to the silver paste, which was used

to form a back contact to the silicon gate, not making an ohmic contact with the silicon. Replacing the silver paste with evaporated aluminium noticeably improved the consistency of devices across a wafer: the aluminium formed an ohmic contact to the silicon with considerably lower resistance than the silver paste.

The treatment of the silicon oxide surface prior to pentacene deposition was found to be crucial to the performance of the transistors, specially relating to hysteresis in the saturation transfer characteristics and threshold voltage shifts. Treating the silicon oxide with a silane surface treatment was found to increase mobilities by up to 80% — the silane treatment rendered the surface of the silicon oxide hydrophobic by replacing hydroxyl groups on the surface of the oxide with silane groups, which reduced the number of electron/hole traps on the oxide/pentacene interface. Photoresist was applied to the silicon oxide surface, then stripped off with acetone and isopropanol, a common technique when patterning devices lithographically. A large hysteresis was seen in the saturation transfer characteristic of the transistors, with an average threshold voltage shift of 11.3 V. Treating the surface with an oxygen plasma after stripping resulted in a drastic reduction of the hysteresis, with an average threshold voltage shift of 3.2 V. The hysteresis was attributed to organic contamination on the oxide surface causing charge trapping at the silicon oxide/pentacene interface, with the oxygen plasma removing the contamination. X-Ray photoelectron spectroscopy (XPS) measurements confirmed that the silicon oxide surface after an oxygen plasma treatment contained less carbon than before the plasma treatment.

A number of the pentacene/SiO_2 devices exhibited leakage currents. It had previously been found, in the course of investigating charge storage (memory) devices, that incorporating gold nanoparticles between the SiO_2 and pentacene eliminated these leakage currents [5]. Attempting to reproduce these data showed that there was no significant effect on the leakage currents between devices incorporating nanoparticles and those without. However, hysteresis in the transfer characteristic increased with the incorporation of the nanoparticles: this was consistent with adding electron/hole traps to the oxide surface. Gold nanoparticles act as good charge traps, having been incorporated into memory structures [6–9].

Replacing the silicon oxide dielectric with PMMA had some success. Devices fabricated on PMMA had negative threshold voltages, and considerably smaller hysteresis than devices fabricated on to silicon oxide. The shapes of the output characteristic curves were unusual compared with an ideal characteristic, or even similar devices on SiO_2. Devices incorporating a ~120 nm layer of PMMA performed better than those with only a very thin (<100 nm) layer. Conversely, a much thicker layer of PMMA reduced performance significantly. It was therefore concluded that there is an optimum PMMA thickness to optimise transistor mobility; however, further work is needed to experimentally determine the optimum thickness.

Devices fabricated on hafnium oxide exhibited a number of problems. A large number of devices were shorted between the gate and source-drain contacts, which was attributed to leaks through the oxide layer. Other devices exhibited reasonable transfer characteristics, with the threshold voltage hysteresis indicating the hafnium oxide contained hole traps, compared with silicon oxide, containing electron traps. However, the output characteristics of most of these devices showed no significant dependence between the source-drain voltage and source-drain current, thus the measured output currents were most likely due to leakage between the gate and drain contact. On a device which exhibited reasonable output characteristics, the mobility of the device was measured to be 0.59 $cm^2/V/s$, thus demonstrating that pure hafnium oxide has potential to be used as a dielectric, if the deposition methods could result in an improved quality film:atomic layer deposition of an Al_2O_3 / HfO_2 bilayer has already been shown to produce good results [10, 11].

Three new materials based on the dibenzothiophene moiety, synthesised in the University of Durham, were characterised. IR-35F was found to evaporate readily, not dissociating during the evaporation procedure. Although electrically insulating, it was found that the conductance could be altered by the field effect; this demonstrated that the molecule acted as an n-type semiconductor. Transistors exhibited good saturation, but the output characteristic outside the saturation region was non-linear; this was attributed to contact effects between the metal contact and organic semiconductor. There appeared to be a fourth-order relationship between saturation currents and gate voltage; nevertheless, fitting a simple transistor model gave a mobility of 3.45×10^{-6}

$cm^2/V/s$.

In an attempt to increase electron mobility, EC-08A was synthesised. The molecule had a similar structure to IR-35F, but increased the number of electron-deficient groups. Electrical characterisation of EC-08A showed ohmic characteristics when the film was under vacuum, but non-ohmic characteristics when in air. When attempting to fabricate transistors using this molecule, it was found that the conductance of the film was not altered by the field effect. It was concluded that, by the addition of the extra electron-deficient groups and ethyl groups into the molecule, the properties of EC-08A were altered in a way that inhibited semiconducting behaviour.

Lastly, CSW-652, a molecule based on DBTBT [12], was found to exhibit p-type semiconducting properties, and transistors made using this molecule conformed fairly well to the simple transistor model, exhibiting good saturation, and linear characteristics outside the saturation regions. However, the currents were low and the mobility was only 3.71×10^{-5} $cm^2/V/s$; this was attributed to the lack of a good crystal structure of the deposited film, which in turn was attributed to the carbon chains off the molecule inhibiting large-scale crystal growth: it was suggested that removal of these chains might allow for structured crystal growth in the evaporated film.

8.2 Suggestions for further work

The pentacene transistors fabricated on silicon oxide have been shown to exhibit good characteristics with reasonable mobilities for non-optimal pentacene deposition conditions. However, the devices tended to exhibit leakage currents flowing between the source and drain terminals when a gate voltage is applied, with 0 V applied to the source. It has been reported [13, 14] that patterning the semiconductor reduces these currents. Therefore, to improve the performance of the transistors, investigation could take place into finding the optimal pentacene deposition conditions (substrate temperature and semiconductor pattern) in order to regularly obtain mobilities of more than 1

$cm^2/V/s$.

Organic devices have often been used for chemical sensors — the presence of a chemical being characterised, for example, by a change in electrical conduction [15, Chapter 10]. It could be possible to fabricate a chemically-activated transistor by using an inverted structure — the source and drain contacts being encapsulated under the dielectric layer, with the gate exposed to the environment; thus, with an appropriate gate contact, presence of the chemical to be sensed could be detected by the transistor turning off or on. This could have a potential advantage over a traditional sensor in that the semiconductor and contacts can be shielded by the dielectric layer from the environment in which the sensor is placed.

Flexible transistors may be used as the driving circuitry for active matrix 'paper' displays. The transistors fabricated on the polyimide substrate exhibited good characteristics, but with low mobilities. Further investigation into this device structure should yield improved operation, and thus there would be potential for using the transistors as the switching circuits for organic LED pixels.

The hafnium oxide devices showed potential for fabricating devices with high currents. However, the deposition conditions and method used resulted in oxide layers with a large number of leaks. Using different deposition methods may allow for deposition of a higher density oxide layer resulting in fewer leaks; this has already been demonstrated using an Al_2O_3 / HfO_2 bilayer [10, 11]. Alternatively, a solution-cast dielectric (e.g. PMMA) might act as a planarising layer on top of the hafnium oxide and thus serve to reduce leakage.

To enable fabrication of low-power circuits, complementary semiconductors of similar mobilities need to be used. Although p-type semiconductors are well established, high mobility air-stable n-type devices are still a matter of research. The IR-35F used in this work was air-stable, but with low mobility, and hence it is suggested that this molecule could be used as the basis for further research. It is likely that the mobility could be increased by a couple of orders of magnitude by optimising the deposition conditions, and the transistor fabrication process. Replacing the sulphur atoms on the dibenzothiophene groups with an electron-deficient sulphur dioxide group may lead to increased electron mobility, while not significantly altering the molecule's

overall structure (as was the case for EC-08A).

CSW-652 has shown promise as a p-type semiconductor, despite the lack of visible long-range crystal structure (hence the low transistor mobility). It is suggested that removing the carbon chains from the molecule would allow the molecule to form a good crystal structure; further work would involve an investigation into the morphological and electrical properties of derivatives of CSW-652: with a good crystal structure there is a possibility for the mobility of the molecule to approach that of pentacene.

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In preparation.

B

Transistor summary

This appendix summarises the results for the transistors used in this work. Unless otherwise stated, all the transistors were fabricated on a silicon substrate with a silicon oxide dielectric, pentacene as the semiconductor and gold source-drain contacts; contact was made to the silicon gate with silver paste and aluminium foil.

The subthreshold slope is defined as

$$S = \frac{\partial |V_G|}{\partial |\log |I_D||}$$

in the subthreshold region of the transfer characteristic.

Section	Transistor structure	Mobility ($cm^2/V/s$)	Threshold Voltage Off-On	On-Off	On-Off Ratio	Subthreshold slope (V/decade)
5.4.1	Standard structure	6.3×10^{-3}	-4.6	19.5	2.1×10^4	17.1
5.4.2	Standard structure	5.0×10^{-3}	-5.6	37.7	4.7×10^3	16.5
5.4.2	DMDS surface treatment	8.9×10^{-3}	-10.05	20.5	5.2×10^4	21.3
5.4.3	DMDS surface treatment	0.105	10.3	74.6	155	23
5.4.4	DMDS surface treatment, pentacene with 2–3 μm grains	0.54	0.44	1.50	105	104
5.4.4	DMDS surface treatment, pentacene with 0.5 μm grains	0.2	1.2	4.3	2.9×10^4	24.3
5.4.5	RIE etch back of Si wafer, evaporated Al as gate	N/A	-14.4	44.5	144	39

Continued on next page

Section	Transistor structure	Mobility ($cm^2/V/s$)	Threshold Voltage On-Off	Off-On	On-Off Ratio	Subthreshold slope (V/decade)
5.4.5	S1813 photoresist, HF etch back of wafer, remove resist	N/A	-21.3	66.3	339	13.1
5.4.6*	S1813 resist, removed with 1112A stripped, HMDS surface treatment	N/A	-1.64	6.34	1.4×10^3	25
5.4.6	S1813 resist, removed with 1112A stripper, oxygen plasma, HMDS surface treatment	N/A	11.08	31.98	889	7.0

Continued on next page

*The values given for this section are averaged from all the measured devices of each preparation

Section	Transistor structure	Mobility ($cm^2/V/s$)	Threshold Voltage On-Off	Threshold Voltage Off-On	On-Off Ratio	Subthreshold slope (V/decade)
5.4.6	S1813 resist, removed with acetone and isopropanol, HMDS surface treatment	N/A	1.63	11.30	126	103
5.4.6	S1813 resist, removed with acetone and isopropanol, Caro's acid, HMDS	N/A	-2.48	6.49	8.5×10^3	11.6
5.4.6	S1813, removed with acetone and isopropanol, oxygen plasma, HMDS	N/A	-0.563	3.21	996	†

Continued on next page

† Values ranged from 16 to 422 V/decade, so no reasonable value can be given

Section	Transistor structure	Mobility ($cm^2/V/s$)	Threshold Voltage On-Off	Threshold Voltage Off-On	On-Off Ratio	Subthreshold slope (V/decade)
5.4.6	S1813, removed with acetone and isopropanol, Caro's acid, oxygen plasma, HMDS	N/A	3.57	8.77	2.3×10^3	72.2
5.4.7	S1813, patterned, HF to remove exposed oxide, S1813 removed with acetone and isopropanol, evaporated Al gate, oxygen plasma, HMDS surface treatment	0.17	-0.94	1.41	2.9×10^3	12.5
5.4.8‡	HMDS surface treatment	5.5×10^{-3}	2.81	35.75	955	13.1

Continued on next page

‡Values are averaged from all the measured devices

Section	Transistor structure	Mobility ($cm^2/V/s$)	Threshold Voltage On-Off	Threshold Voltage Off-On	On-Off Ratio	Subthreshold slope (V/decade)
5.4.8	HMDS, Q-Au gold nanoparticles	5.7×10^{-4}	-2.68	48.98	763[§]	11.9
6.2	124 nm PMMA dielectric	0.21	-4.44	-4.55	266	3008
6.2	80 nm PMMA dielectric	0.058	-4.11	-4.07	213	2006
6.2	350 nm PMMA	4.55×10^{-5}	-4.73	-1.10	351	11.2
6.3	39 nm HfO_2	N/A	-4.08	-12.49	97.6	3.7
6.3	40 nm HfO_2	0.59	-6.28	-11.29	3.8×10^3	110
6.4	Polyimide substrate, Al gate, PMMA dielectric	1.5×10^{-4}	-6.19	-4.20	482	12.9
7.2.3	DMDS surface treatment, IR-35F semiconductor	3.45×10^{-6}	6.0	4.8	135.5	170

Continued on next page

[§] The on-off ratios varied a lot between devices and so it was not possible to draw any conclusions as to the effect of gold nanoparticles on the on-off ratio

Section	Transistor structure	Mobility ($cm^2/V/s$)	Threshold Voltage On-Off	Off-On	On-Off Ratio	Subthreshold slope (V/decade)
7.4.2	CSW-652 semiconductor	3.71×10^{-5}	-3.16	2.82	346	70

C

HfO_2 AFM images

This appendix contains all the atomic force micrographs taken when profiling the surface of the hafnium oxides (section 6.3). The images correspond with the samples listed in table 6.1.

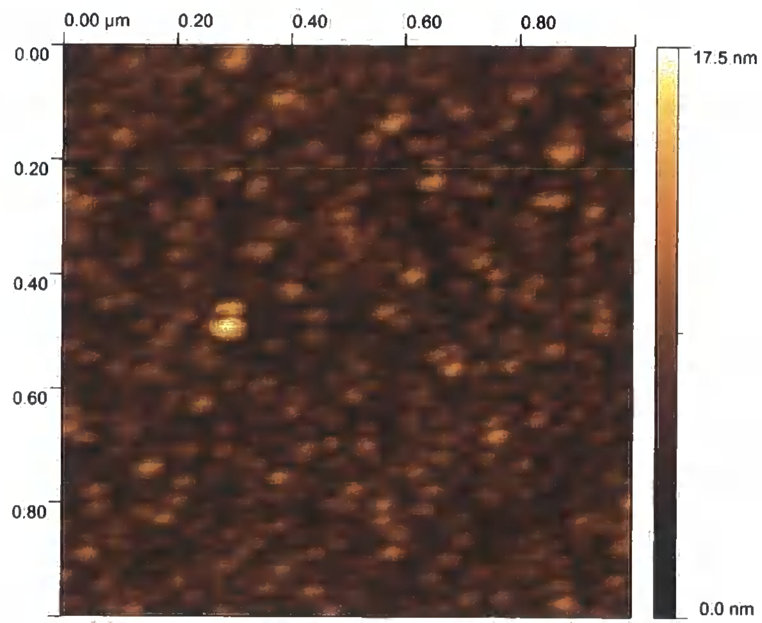

Figure C.1: P1

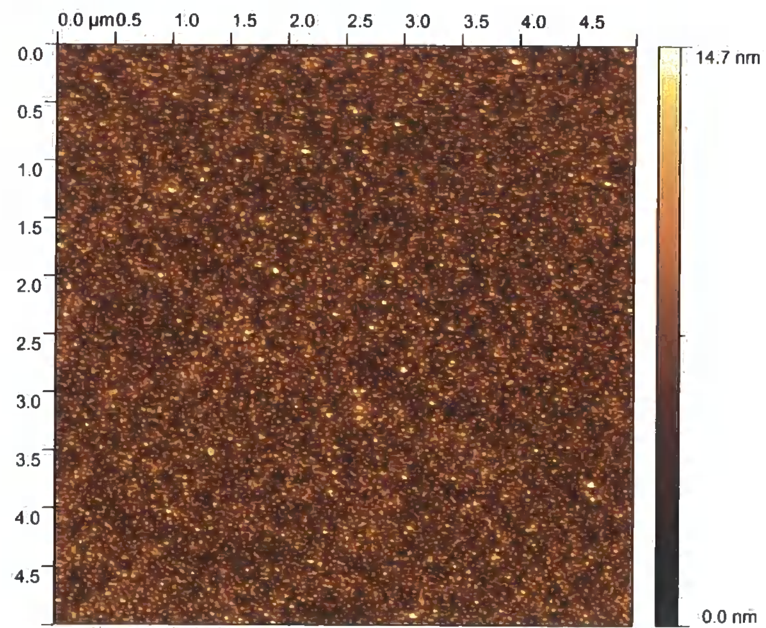

Figure C.2: P1S

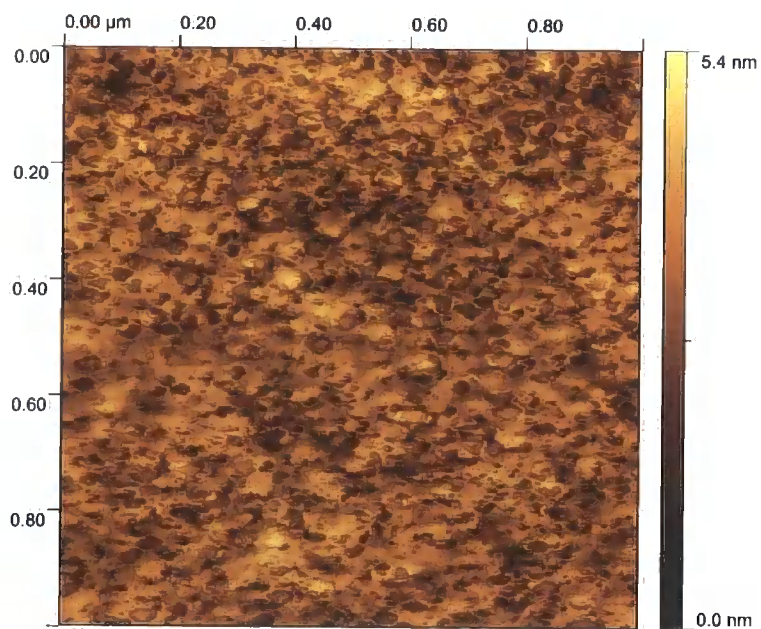

Figure C.3: P2

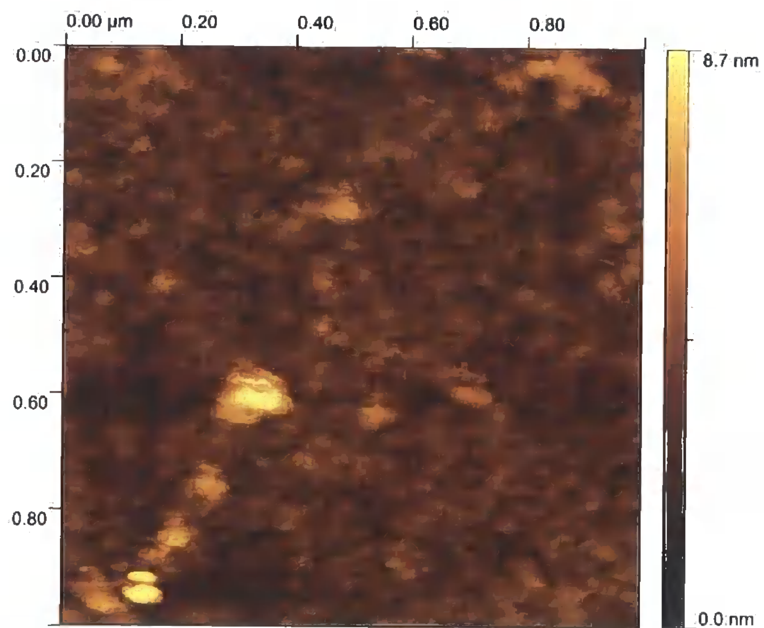

Figure C.4: P2

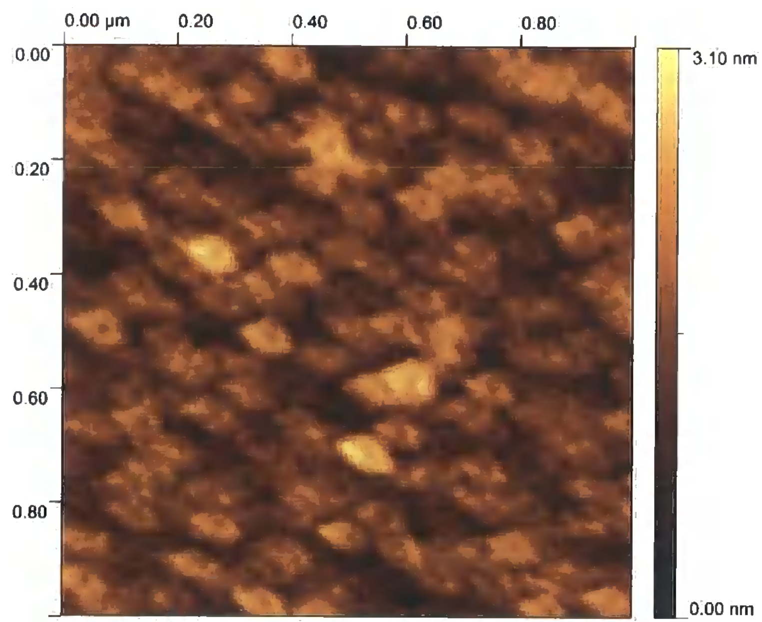

Figure C.5: P3

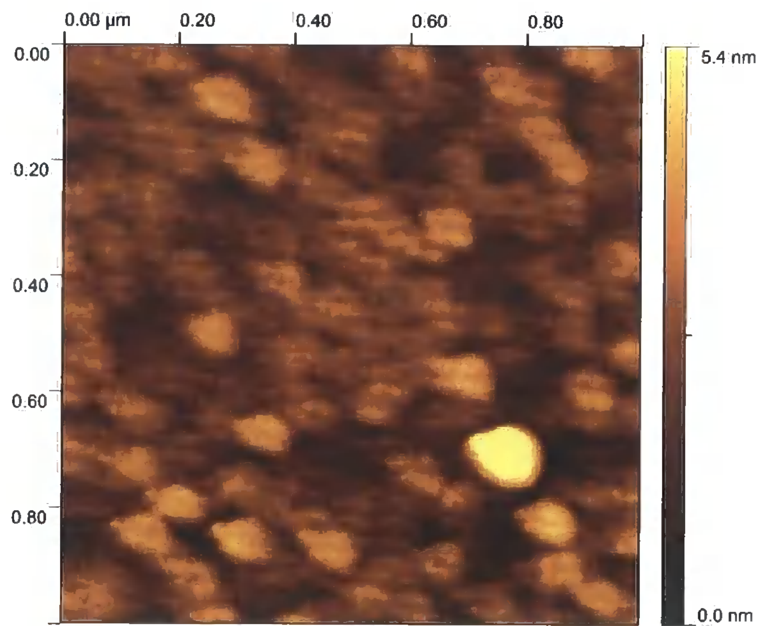

Figure C.6: P3

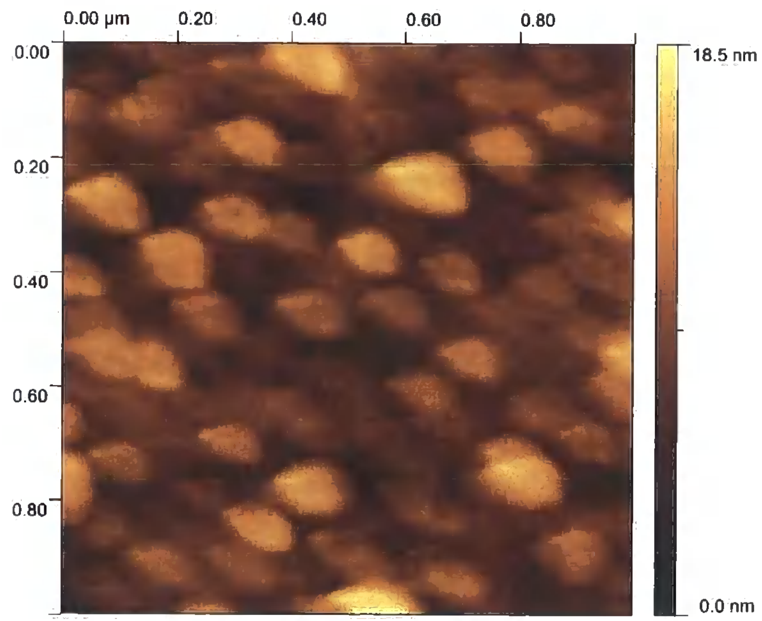

Figure C.7: P4

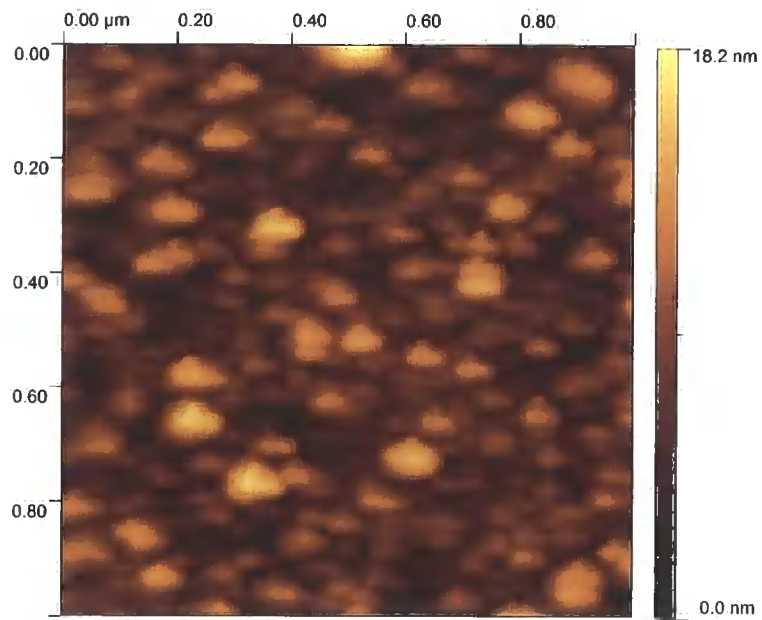

Figure C.8: P4

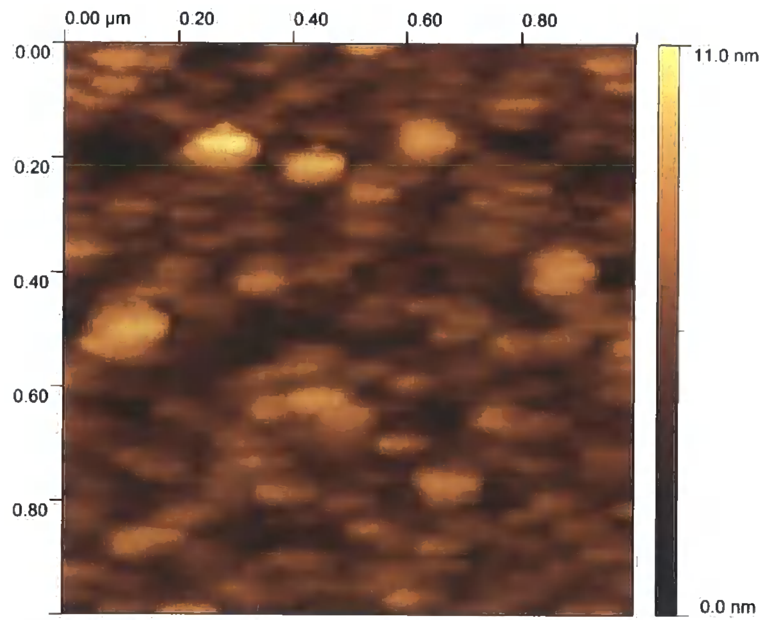

Figure C.9: P4

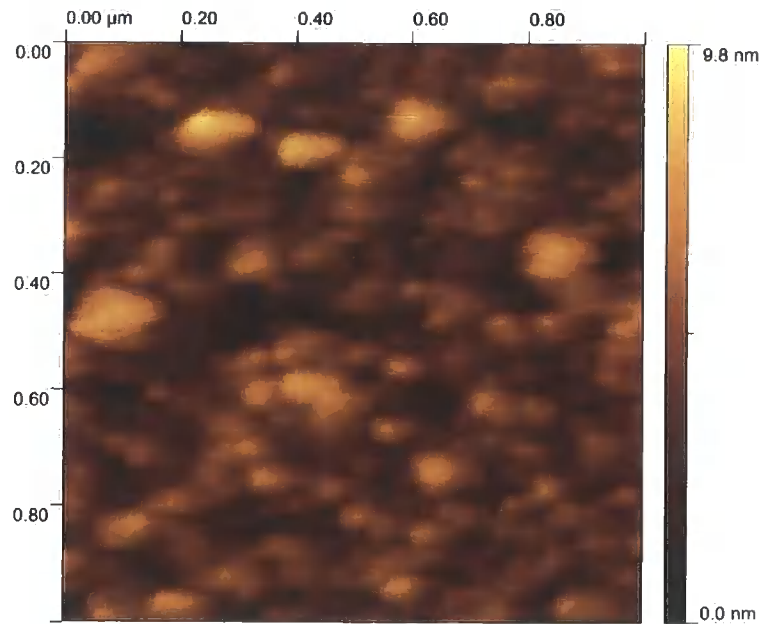

Figure C.10: P4

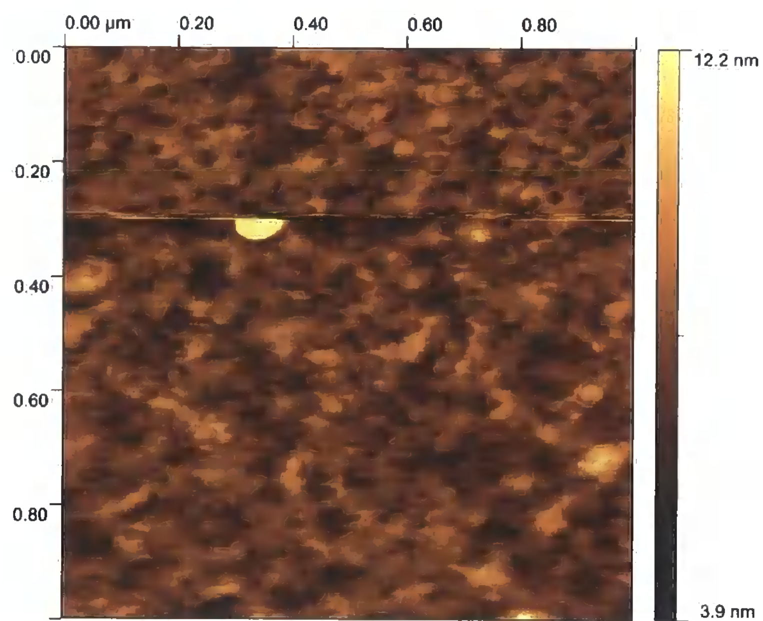

Figure C.11: P5

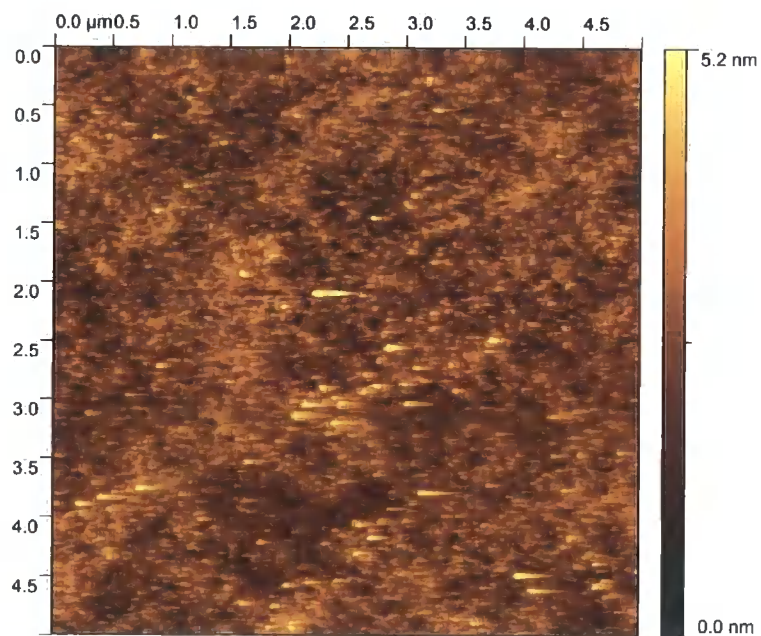

Figure C.12: P5

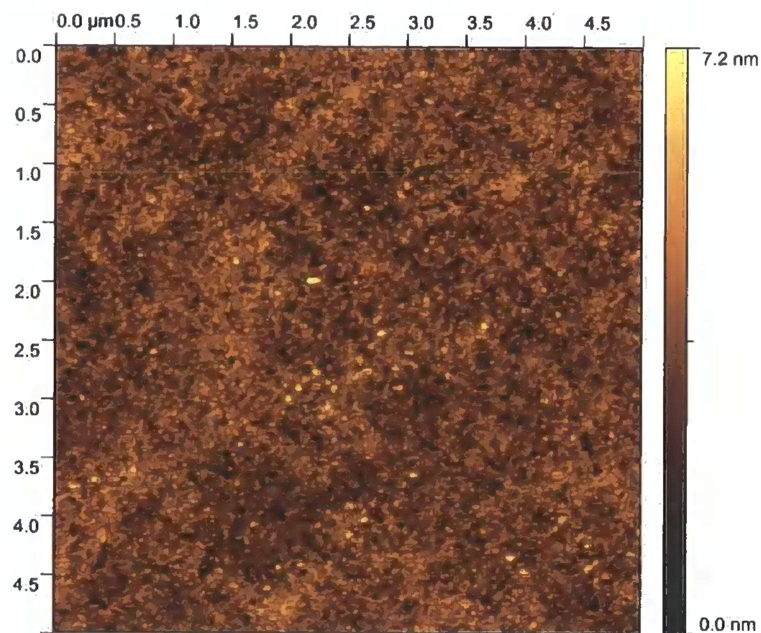

Figure C.13: P5

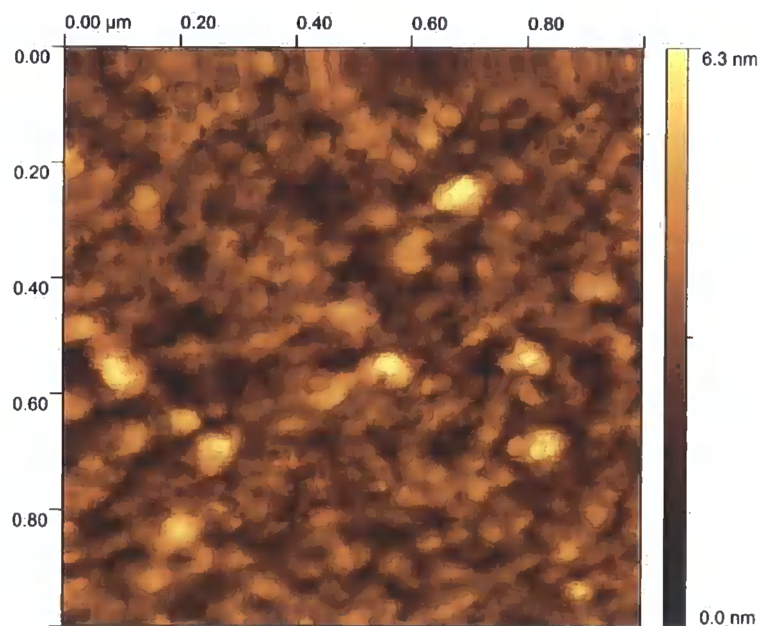

Figure C.14: P5

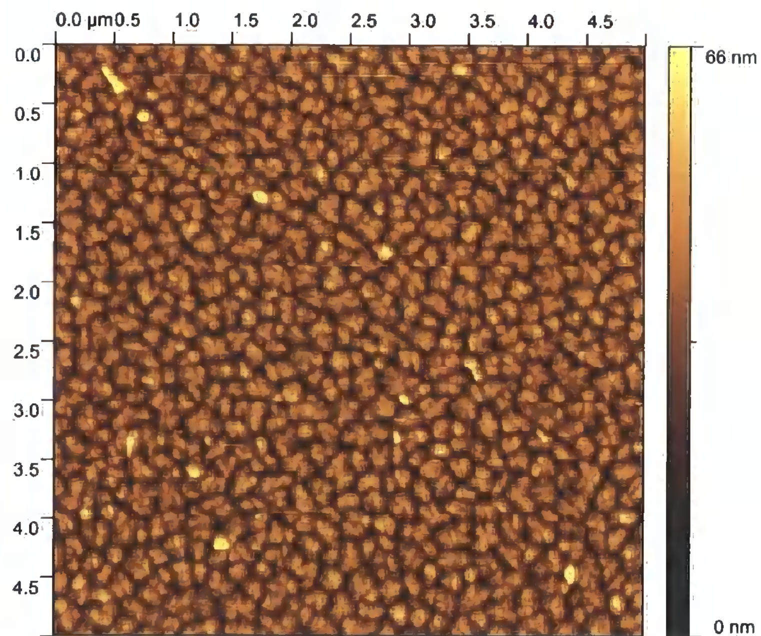

Figure C.15: P1 with pentacene

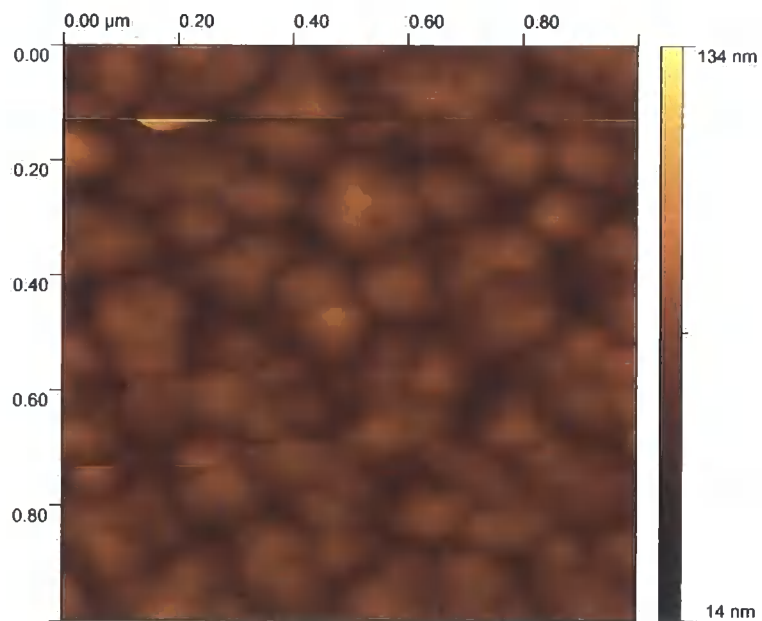

Figure C.16: P1 with pentacene

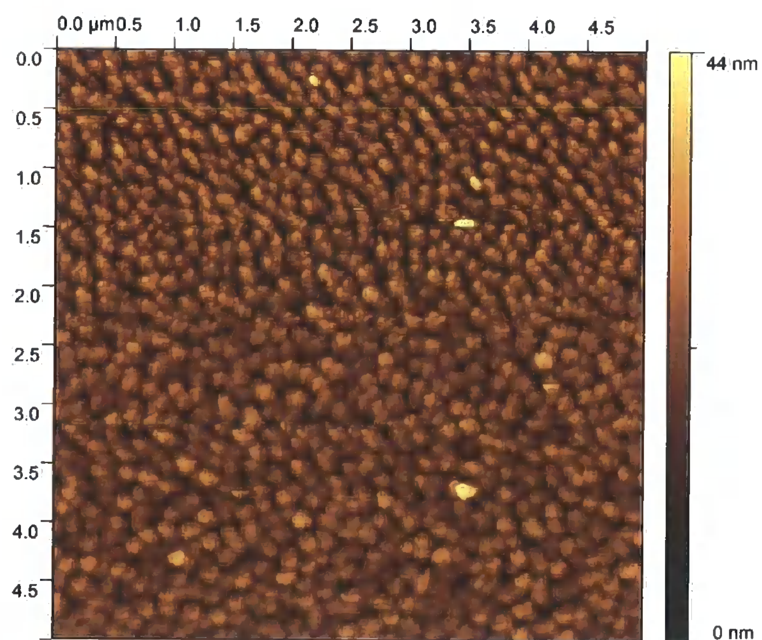

Figure C.17: N2 with pentacene