SiC MOSFET Based SSCB For Aviation System Applications

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Abstract

The Solid-State Circuit Breaker (SSCB) is a critical device for the protection of DC power distribution systems such as those found in renewable energy and aerospace applications. With the development of the DC distribution system at medium voltage levels that are over 1kV and the requirement of the SSCB short circuit performance becomes more critical to protect the network. Therefore, an optimised control system to minimize the overcurrent and short circuit time when the fault occurs for SSCB based on SiC MOSFET is introduced in this thesis. The maximum short circuit survival time is a critical parameter to evaluate the MOSFET short circuit ability. Therefore in this thesis, the maximum short circuit survival time of three different SiC MOSFETs from the same family is estimated from three different experimental circuit characters, including the overcurrent and overvoltage, the Gate state and the safety junction temperature, and used to designed the control system for short circuit test. The shut down time of different MOSFETs is obtained from the short circuit test to evaluates the performance of the control system. The shut down time of MOSFET driven by convex drive signal is the shortest, followed by linear, and the concave drive signal is the longest. Meanwhile, the shut down time decreases with the drive signal drop speed increasing. In addition, the MOSFET with higher on-state resistance has the shorter shut down time. In the future, the high power applications require the higher rated voltage SSCB, therefore, the series or parallel connected MOSFETs are proposed to increase the rated voltage and current of SSCB. To avoid the voltage and current, which are higher than rated values, applied to and flowing through the individual MOSFET to destroy the device, the control system are required to generate the synchronous drive signals to control the MOSFET, which is a challenge for the future drive signals and control system.

Declaration

The work in this thesis is based on research carried out at the Department of Engineering, Durham University, United Kingdom. No part of this thesis has been submitted elsewhere for any other degree or qualification and it is all my own work unless referenced to the contrary in the text.

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List of Abbreviations

AC	Alternating current
ADC	Analog-to-Digital Converter
AEA	All Electrical Aircraft
AMBA	Advanced Microcontroller Bus Architecture
ASIC	Application Specific Integrated Circuit
DAC	Digital-to-Analog Converter
DC	Direct current
DMA	Direct Memory Access
DUT	Device Under Test
EMF	Electromotive Force
ESD	electrostatic Discharge
ETO	Emitter Turn-OFF Thyristor
FCLs	Fault Current Limiters
FPGA	Field-Programmable Gate Array
FUL	Fault Under Load
GaN	Gallium Nitride
GTO	Gate Turn-OFF Thyristor

HFET	Hetero-Structure Field Effect Transistor
HSF	Hard Switching Fault
HVDC	High Voltage Direct Current
IGBT	Insulated-Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Thyristor
JFET	Junction Field Effect Transistor
MEA	More Electrical Aircraft
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MOV	Metal Oxide Varistor
PL	Programmable Logic
PS	Processing System
PWM	Pulse Width Modulation
RB-IGCT	Reverse Blocking Integrated Gate-Commutated Thyristor
ROM	Read-Only Memory
SCR	Silicon-Controlled Rectifier
SD-D-semi-SJ MOSFET	Schottky-Drain Connected Semisuperjunction Metal-Oxide-Semiconductor Field-Effect Transistor
SiC	Silicon Carbide
SiC-SIT	Silicon Carbide Static Induction Transistors
SSCB	Solid-State circuit Breaker
SSFCL	Solid-State Fault Current Limiter
SoC	System on Chip
TTL	Transistor-Transistor Logic
TVS	Transient Voltage Suppression
UAV	Unmanned Aerial Vehicle
WBG	Wide Bandgap

CHAPTER 1

Introduction

The development of DC power distribution systems has significantly increased in pace in recently years. The requirement of high performance DC circuit breakers to protect the DC grid and devices from faults is more critical in these higher rated voltage systems, and have to minimize both the overcurrent and noise, whilst demonstrating shorter short circuit time. Because the DC current has no natural zero point, and the fault current rise speed is significantly faster than in an equivalent AC system, the AC circuit breaker cannot be used in DC circuit protection. Traditional mechanical DC circuit breakers were developed from the AC circuit breaker to protect large scale DC circuits. Passive mechanical DC circuit breakers use LC oscillation circuits to generate an artificial zero point in the fault current to trigger the blocking of the DC circuit, and the active mechanical DC circuit breaker uses the capacitor to decrease the overall duration of the oscillations. The mechanical DC circuit breaker is a low loss, high control reliability and low cost breaker, and the first mechanical HVDC circuit breaker was installed in 2017 [1]. However, the mechanical DC circuit breaker has the drawback of slow reaction speed and short operational life [2], which results in a large the short circuit time when a fault occurs. To decrease the short circuit time, the solid-state

circuit breaker (SSCB) has been proposed [3]. SSCBs use semiconductor devices to control the conduction in the circuit. When the faults occur, the semiconductor device will block the circuit within a short period and the energy in the system will be absorbed by an overvoltage component, such as a metal oxide varistor (MOV). The SSCB has the advantages of smaller volume, faster response speed and high reliability in comparison to the mechanical breaker [4]. However, the power loss during normal operation of the SSCB is large and the overcurrent during a fault is significantly large when the SSCB is used in the high power applications [5]. The overcurrent results in the generation of significant electrical noise when the circuit is blocked and has the potential to destroy the semiconductor device in SSCB [6]. Therefore, a large number of research has focused on decreasing the overcurrent and short circuit time to improve the performance of SSCB which used in DC circuit protection applications [7] [8] [9] [10].

The MOV is an useful solution to reduce the overcurrent, which is paralleled with the semiconductor device. When the semiconductor device conducts, the potential difference between the MOV terminals is low and so the MOV will have a high impedance and so the current will flow through the semiconductor devices. When the semiconductor devices blocked, the surge in the circuit results in the increase of voltage across MOV and the decrease of MOV resistance. Therefore the overcurrent will flow through the MOV rather than the semiconductor devices. The fault energy is easier to be absorbed by MOV which is also helpful to reduce the overcurrent in the system. However, the MOV increase the volume of the SSCB and will wear out under repeated fault conditions.

A novel short circuit detection circuit and feedback control system is proposed to replace the control for the conducting and blocking operation of the semiconductor device, which will not increase the number of device required in the SSCB [11]. The control system generates the stepped drive signal to block the MOSFET in the SSCB. When the fault occurs, the short circuit detection circuit detects the fault current and the Gate-Source signal for the MOSFET will drop from 18 V to 9 V, which is the Gate plateau voltage. Meanwhile, the Drain current will drop from 160 A to 40 A, but not directly drop to zero. The drive signal will remains to 8 V for

600 ns and subsequently drop to -5 V to totally block the MOSFET, and the Drain current will remains to 40 A for the same 600 ns before dropping to 0 A. In the traditional pulse control signal, the step control signal can significantly reduce the impact of the overcurrent on the circuit when the short circuit fault occurs. This can be observed from that the noise in the Drain current for a MOSFET driven by the step control signal which is significantly smaller than that driven by pulse control signal. However, the 600 ns plateau results in an increase in the short circuit time and with the increase of the application voltage, the number of the steps in the waveform will increase and this will result in a longer plateau in the control signal. Therefore, it is a challenge to reduce the short circuit time and overcurrent using the technique because the improvements in one of parameters results in the degradation in the performance of the other. To solve this issue, novel control signals are introduced in this thesis to balance the overcurrent and short circuit time.

In this thesis, continuously changing drive signals, that are described as linear, convex and concave, are used to replace the step control signal during the transition to the blocking condition to eliminate the plateau to reduce the short circuit time. The short circuit performance of all three drive signals will be compared to select the optimized drive signal to control the MOSFET in a SSCB application. To identify the optimum conditions to minimize the short circuit time and overcurrent, multiply drive signals with different transform time from maximum to minimum voltage will be evaluated to obtain the optimized value. In addition, three SiC MOSFETs with different on resistance from the same family were evaluated in this thesis to identify the impact of the on resistance and Gate charge on the short circuit performance and to identify the optimum MOSFET to realize the SSCB for 270 V DC protection. Finally, two different fault current detection methods, based on the current shunt and voltage divider were tested and the performance is compared in this thesis to optimize the performance of the control system.

The structure of the rest of the thesis is as follows: in Chapter 3, a short circuit test platform is introduced and short circuit tests with pulse control signals are used to determine the short circuit characteristics and maximum short circuit withstand time of different MOSFETs to support the design and construction of the control system. The short circuit performance for a SSCB system driven by a pulse can be used to enable the comparison of the system performance when driven by the novel drive signal.

In Chapter 4, a novel control system for the Gate-Source voltage of the MOSFET based on FPGA is introduced. The FPGA is used to collect the current and voltage levels in the SSCB in real time to identify the working condition of the main circuit, and generate the corresponding drive signal to minimize the effect of any fault conditions. The novel drive signal has three operating conditions, described as normal, transform and error. When the main circuit operates under normal conditions, the FPGA will generate the normal drive signal, which maintains the MOSFET in normal conduction conditions. When the fault occurs, the current in main circuit rises rapidly and the FPGA generates the linear, convex and concave transform signal to place the MOSFET into blocking. The FPGA generates the error drive signal to ensure the MOSFET remains in blocking until the fault has been cleared. The type and shut down time of the drive signal are all controlled by the FPGA which enable flexibility to optimize the control signal for a specific application.

In Chapter 5, a short circuit test platform and the control system with isolation and amplifier circuit is introduced. Meanwhile, the short circuit performance of the novel drive signals is determined. To obtain the optimum drive signal, three different drive signals with different transform time, including the linear, convex and concave drive signal, are tested in Chapter 5 and the drive signal with the shortest short circuit time will be the optimum choice. To compared the impact of different MOSFETs on the novel drive signal short circuit performance, three SiC MOSFET with different on-state resistance from the same family are tested, and the advantages and drawbacks of the current shunt and voltage divider detection are also introduced in Chapter 5. Finally, the optimum drive signal and control system for SiC MOSFET based SSCB is summarized.

In Chapter 6, the conclusion of all Chapters is Summarized. Meanwhile, the future work and potential improvement of the novel drive signal and control system are introduced.

In this thesis, the short circuit characteristics of SiC MOSFETs, from the same family, has been verified to obtain the fault reason of the MOSFETs. The test results are used to design the control system in Chapter 4 and can be used as a reference for other experiments using the MOSFETs from the same family. A novel drive signal with three parts, including the normal part, adjustable transform part and error part is designed based on FPGA. The MOSFET drive ability has been verified in Chapter 4. Be different with the traditional pulse drive signal, the novel drive signal can minimize the overcurrent and short circuit time by changing the waveform and drop speed of the transform part. Therefore, the SSCB controlled by the novel drive signal can limit the overcurrent without the external device, such as the MOV, during the fault, which reduces the number of devices used in SSCB and the weight and volume of the SSCB. This makes the SSCB, controlled by the novel drive signal, has advantages in the applications which have the critical requirement of weight and volume. The results have been verified in Chapter 5 and can be used as a reference to drive the MOSFETs from the same family.

CHAPTER 2

A review of SSCB

2.1 Overview of SSCB

Short circuit faults may occur in a power system which results in the devices of the power system becoming damaged by huge overcurrent and overvoltage. Therefore, to protect the devices and ensure the safety of the overall circuit, a protection circuit is required to block the current flow. A fuse is an example of a protection circuit for power systems, which is composed of a metal and protective case. When the short circuit fault occurs, the overcurrent results in the rapid rise of the temperature of the wire and the fuse will melt to block the current in the circuit. However, fuses cannot be controlled which cannot meet the requirement of the smart power system development. Therefore, circuit breakers based on controllable semiconductor devices are proposed to replace fuses to protect power systems. Solid state circuit breaker (SSCB) is a no moving parts semiconductor apparatus, which is used to protect electrical circuits from fault overcurrent interruption. The main components of a SSCB are the power semiconductor device, the feedback control system and the voltage clamping circuit [12]. The power semiconductor device is the main part of the SSCB which is used to block and conduct the main circuit. The feedback signal

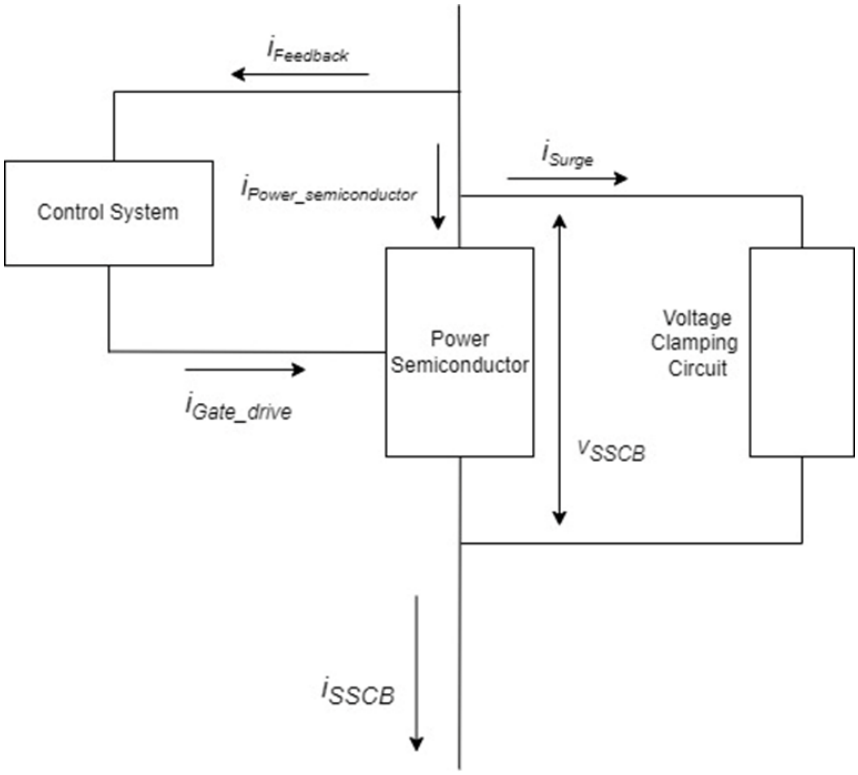

Figure 2.1: The block diagram of SSCB components

$i_{Feedback}$ is a signal level measurement, which transform the main circuit working condition and is obtained by the current shunt. The voltage and current sensor can measure the voltage across the power semiconductor and the current through the main circuit, which can be used to judge the main circuit working conduction. The control system can generate the corresponding drive signals to control the conducting and blocking of power semiconductor, according to the working state of the main circuit. When the main circuit works normally, the control system will conduct the power semiconductor, and when the main circuit faults, the control system will block the power semiconductor. The clamping circuit is used to protect the power semiconductor device from the overvoltage during the short circuit fault. The block diagram of typical SSCB components is shown in Figure 2.1.

The power semiconductor is the key device in SSCB to control the conduction and blocking mode operation of the circuit according to the circuit state. It is required to have a high rated voltage and high switching frequency to enable higher voltage and fast reaction applications [13]. However, the overvoltage that occurs across the power semiconductor during the overcurrent fault can be significantly

higher than the rated voltage, therefore, the voltage clamping circuit is necessary in SSCB to limit V_{SSCB} and protect the power semiconductor [14]. The control system has two sections, including the sensors, including the current sensor and the voltage sensor, and the Gate-drive circuit. The current and voltage sensors collect the feedback current and voltage signals from the main circuit and transform the signals to the Gate-drive circuit, which will generate the corresponding drive signal to control the power semiconductor devices [15].

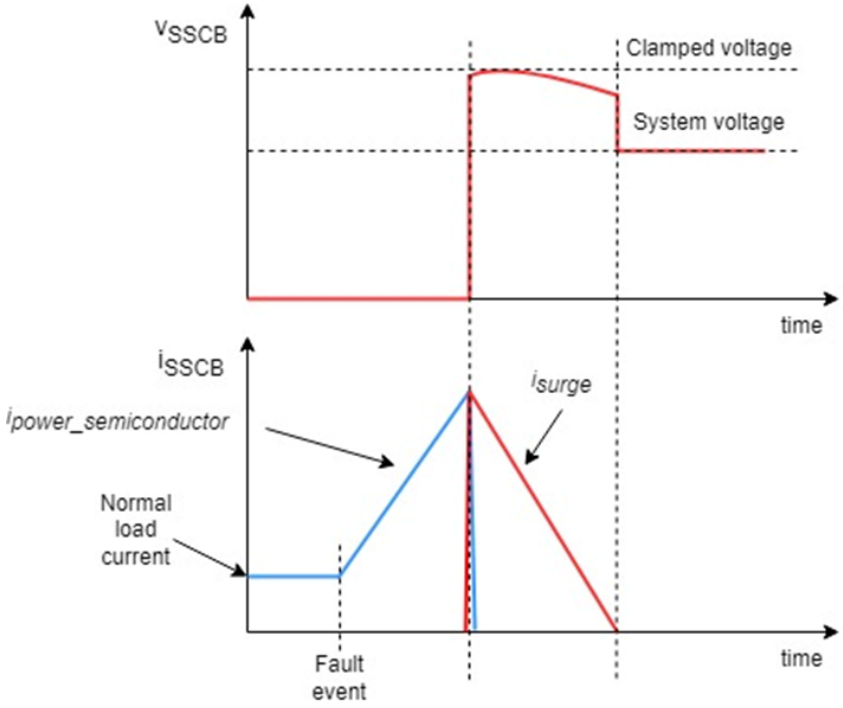

Figure 2.2: Typical waveform of the SSCB

A typical waveform of the SSCB during the short circuit fault is shown in Figure 2.2 [12]. Under normal working conditions, the power semiconductor device stays in the on-state where V_{SSCB} is low, and the gate drive circuit generates sufficient Gate-Source voltage to keep the power semiconductor in a stable and low on-resistance state. When the overcurrent fault occurs, the current through the power semiconductor begins to rise rapidly limited by the inductance in the circuit. The current sensor will collect the current feedback data and it will be compared with the threshold. When the feedback data exceeds a threshold, the control system judges that the circuit operation state has changed from normal to error and the drive circuit controls the power semiconductor to block the current flow to protect

the circuit from the excess current. As the power device is operating in blocking, the I_{SSCB} reduces to zero and V_{SSCB} rises. To ensure the safety of the circuit, the SSCB is designed to block the circuit as rapidly as possible, however this results in significant dI/dt and dV/dt, which may result in rapid temperature rise inside the MOSFET and destroy the whole device [16]. The voltage clamping circuit is included to mitigate this problem. The circuit limits the overvoltage and keeps it within a safe range and allows the increased I_{SSCB} to pass through the clamp circuit to protect the power semiconductors from the short circuit current damage. The flow of current in the clamping circuit allows the I_{surge} to rise almost simultaneously with the drop in the current through the semiconductor device. The current through the device keeps decreasing to release the fault energy until it reaches zero. After that, the circuit remains in the blocking state, where the current remains at zero and the voltage is at the system voltage.

In recent years, the SSCB is widely used in many applications, especially those operating at low voltage (48-1500 V) and lower range of medium voltage (5-10 kV) [12]. This is because the SSCB has many significant advantages, compared with the traditional electromechanical breakers and fuses [2].

Firstly, the SSCB contains no moving parts which reduces risks from the arc, which appears during the process of contact separation. The circuit control of SSCB is realised by controlling the condition of the semiconductor devices, while the electromechanical breakers control the circuit by the movement of metal contacts, when the fault occurs and the metal contacts will become physically separated. However, in contrast with the AC current that is common in large scale transmission and distribution, DC current does not have natural zero current crossing points, which results in the arc always appearing during the mechanical contacts separation process. Arcing will result in the generation of significant noise and reduce the service lifetime of the breakers by melting the metal contacts and potentially risking burns to the operators [17]. Compared with electromechanical breakers, SSCB has lower safety risks, and no moving parts reducing the maintenance costs and extending the service lifetime of breakers.

Secondly, the response time and shut down time of the semiconductors based

solutions are typically more than three orders shorter than those of magnitude electromechanical breakers. The current flow through the SSCB is controlled by the Gate-Source voltage of the power semiconductor device, and once it is lower than the threshold voltage, the channel in power semiconductor device will be closed with a several microseconds turn off time. The turn off time during the short circuit fault is larger than the data shown in MOSFET datasheet, because the condition is different. Considering the system delay, the whole shut down time of SSCB, from the detection of the short circuit to the interruption of the current flow interrupted, could be several microseconds. In contrast, the electromechanical breakers rely on the movement of metal contacts to control the current flow in the circuit. The mechanical movement takes a greater time than blocking the electronic charge, furthermore, the arc further delays the shut down time as the circuit is fully blocked only after the disappearance of the arc [18]. This results in the total shut down time of electromechanical breakers being significantly longer than that of SSCB, and may reach several milliseconds [3].

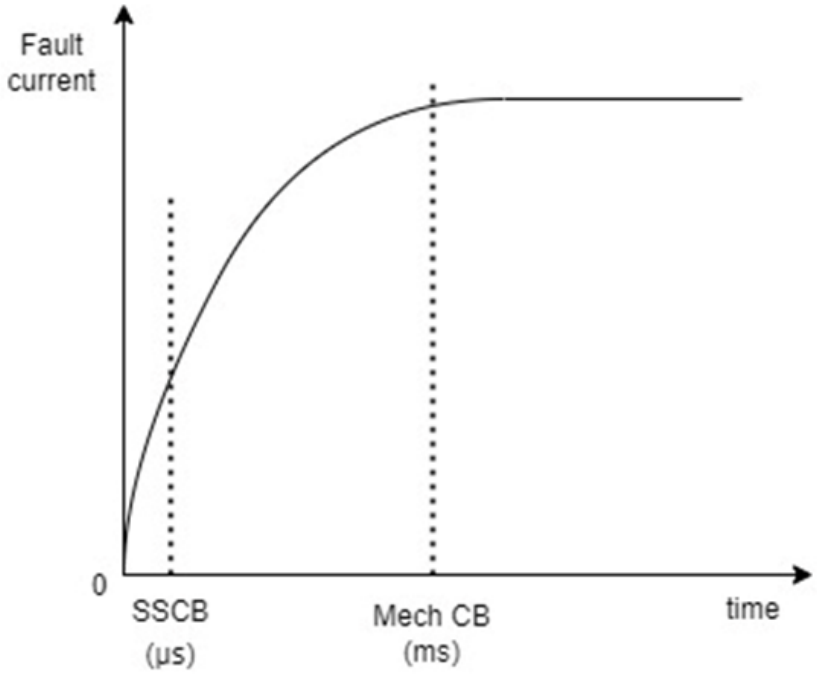

Figure 2.3: Response time of SSCB and electromechanical breaker

Moreover, because of the fast reaction ability, SSCB can interrupt the short circuit current during a short time and limit the peak value of overcurrent and

the fault energy. As shown in Figure 2.3 [19], when the fault occurs, the fault current will rise rapidly and remain the steady state value. As the reaction time of SSCB is several orders of magnitude shorter than that of electromechanical circuit breakers, the peak current value through the SSCB before turn off is much smaller than the current through the electromechanical breakers. Finally, the SSCB has less electrical noise compared with the electromechanical breakers, which can be attributed to the lack of moving parts. Besides the advantages mentioned above, SSCB also offers several additional benefits for most power distribution applications and some special applications.

2.2 SSCB Applications

With the development of power semiconductor technology, the performance of SSCB is increasing in terms of the rated voltage reducing, power loss and the short circuit current withstand time, hence the SSCB is more and more widely applied in power distribution systems and renewable energy system to replace traditional electromechanical circuit breakers. Applications include the shipboard distribution system, computer database installations, aircraft and high-altitude flight power distribution and power supply systems, the protection for battery systems using renewable energy storage, renewable energy power station, DC power converter protection, railway transportation and the infrastructure for electric vehicle charging. Among them, the applications on aircraft and high-altitude flight, with renewable power system, are very attractive. High-altitude solar flight can supply the global stratospheric earth observation services to service for a wide range of applications such as maritime surveillance, border monitoring, mapping, forest fires and emergency response. Advanced solar panels system provides the high-altitude solar flight with long-lasting autonomous operation capability for months. The solar panels system with advanced SSCB can further improve the reliability of high-altitude solar flight in global stratospheric earth observation services [20]. The advantages and development of the SSCB in these applications will be introduced in this section, with protection future improvements and technical requirement will also be described.

2.2.1 *SSCB applied on shipboard power distribution system*

Considering the high reliability requirements for shipboard distribution systems, DC distribution is preferred as it can directly connect with the energy storage system and redundant buses. Therefore, a more efficient, faster protection and increased reliability DC circuit breaker is necessary, which supports the application of SSCB [19]. Shipboard systems now mostly use low-voltage DC power distribution systems to connect the variable frequency drives and other loads with the DC feed, which reduces the weight and the volume necessary for the front-end AC/DC converters [21]. A range of SSCB topologies are widely used, including the Coupled-Inductor DC breaker and bidirectional Coupled-Inductor DC breaker [22]. However, the future shipboard requires the integration of a wider range of power sources and loads connected to a common bus, which increases the voltage and power levels of the DC bus and leads the power transmission from generation to electrical zones where the performance aligns with medium-voltage DC systems [23]. New challenges for SSCB relates to improving the availability and reliability for 1000 V/ 1000 A medium voltage level applications, as the higher voltage level brings higher overcurrent during fault conditions [24].

2.2.2 *SSCB applied on data centre*

Data centres play an important role in data storage and provision of the internet. With the sharp increase in the number of cloud-based services, a significant increase in the number of data centres is expected, but this increase results in need for the higher reliability and higher power level for the individual data centre [25]. Compared with the traditional AC power distribution system, DC power distribution has huge advantages in increased efficiency and reliability. Under the same working conditions, the conduction loss of DC distribution is just 37% of the equivalent AC system, which results in an increase of 1%-2% in the efficiency for DC power distribution [26] [27]. The uninterruptible power supply of DC distribution requires fewer transformers and converters in comparison to AC system, resulting in increases

in the reliability of the DC distribution system [28]. As the power interruption for data centre has a huge impact on the economy and the data centre consumes around 8% of the total world energy, there are extremely stringent requirements in terms of the efficiency and reliability for the data centre power supplies and the AC distribution system are generally replaced by DC networks [29] [30]. Meanwhile, the circuit protection for AC distribution, like the fuses and the molded case circuit breakers, are not suitable for DC operation, because they cannot meet the fast operation requirement and this limitation results in the circuit breakers have the maintenance and limitation problems under repetitive operation. Hence, a SSCB based on a Silicon Carbide Static Induction Transistors (SiC-SIT) has been proposed to protect the DC distribution system [31]. The SIT structure has very low on-state resistance which is around 1.1 mΩ [32] and large safe operating area compared with fuses which ensure reduced power loss and higher reliability [33] [34]. Therefore, the number of the device used in parallel connection can be reduced and the conducting power loss is low. Be different with the existed semiconductor DC circuit breakers investigation, SiC-SITs can reduce the overvoltage during the fault by gate drive control, rather than the additional circuit components. Therefore, the control system designed in this thesis is easier to reduce the impact of short circuit overvoltage on the main circuit with SiC-SIT [31]. The SSCB which has advantages in power management is one of the hot topics for future data centre in current research [35] [36] [37] [38] [39]. The electrical load of a data centre can be considered as comprising an inflexible load, which must not lose the power supply during the fault condition and flexible load, which could be directly cut off from the system during the fault condition. Therefore, the solid state circuit breaker that can identify load types and implement different short-circuit protection schemes offers a significant advantage over conventional technology to improve the overall performance of the data centre [25].

2.2.3 *SSCB applied on aircraft*

The development of the aviation industry promotes the move to aircraft with a greater level of more electric aircraft and the all electric aircraft. Compared with

the traditional aircraft which operate using pneumatic, hydraulic and mechanical energy as the main power source for actuators, the more electric aircraft has significant advantages in reliability, ease of maintenance whilst offering lower through life costs ability and the functionality often referred to as the more electric aircraft [40]. The power distribution system of more electric aircraft is based on a combination of a DC and an AC power system at the same time. Because the DC power distribution system has the advantages of low line voltage drop, high power supply quality, light weight and reliable operation, the protection and safe operation of DC power distribution system becomes critical [41]. The requirements of the DC power distribution system are fast response to fault conditions, simple structure, light weight, lower volume and high reliability. Bidirectional protection is also required in aerospace to isolate the fault from either the source or the loads. Therefore, the slow reaction speed electromechanical breaker and fuses are not suitable, and the SSCB is the best choice [42]. However, the traditional SSCB which uses an auxiliary SCR in series with passive resonant elements to reverse bias the main switch cannot meet the requirements, because when the fault occurs and detected, the auxiliary SCR must be actively controlled to bias the main switch before the fault current exceeds the fault current capability of the main switch. In addition, another SCR is required to reset the capacitor for the next turn-off cycle which results in the critical challenge of detection and reaction timing, and more devices increases the weight and reduces the reliability.

To improve the performance, the Z-source SSCB has been proposed which has the potential isolate the fault without the need for complex detection and control circuits, which has resulted in more structures being proposed [43] [44] [45]. The diagram of Z-source SSCB is shown in Figure 2.4.

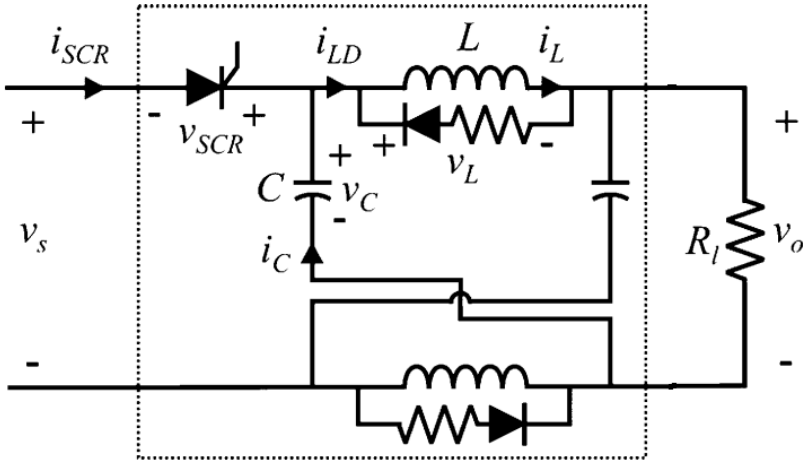

Figure 2.4: The Z-source SSCB

Applying the diode full-bridge to a Z-source SSCB may enable bidirectional protection with just one control switch, but increasing the number of diodes increases the on-state power loss and the normally on working condition magnifies this disadvantage, which is shown in Figure 2.5 [46].

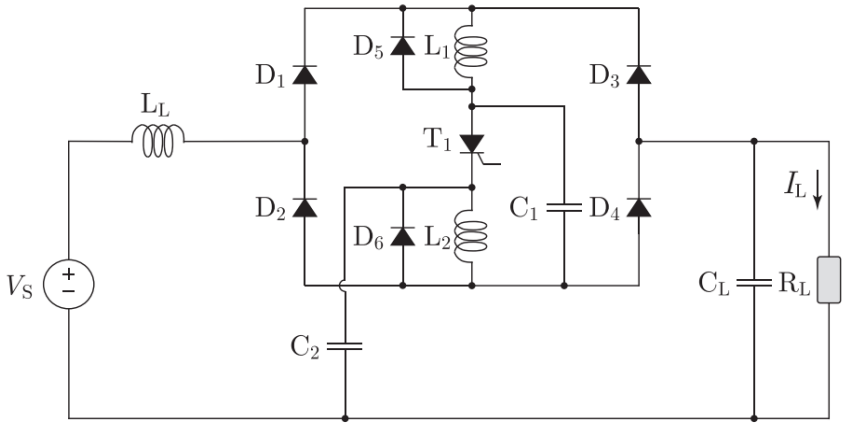

Figure 2.5: The bidirectional Z-source SSCB

Another structure to enable bidirectional protection in a DC circuit is the transformer, which could reduce the number of devices in the protection circuit to simplify the structure. However, this results in significant weight, large volume and a significant increase in conducting power loss [47]. The diagram is shown in Figure 2.6.

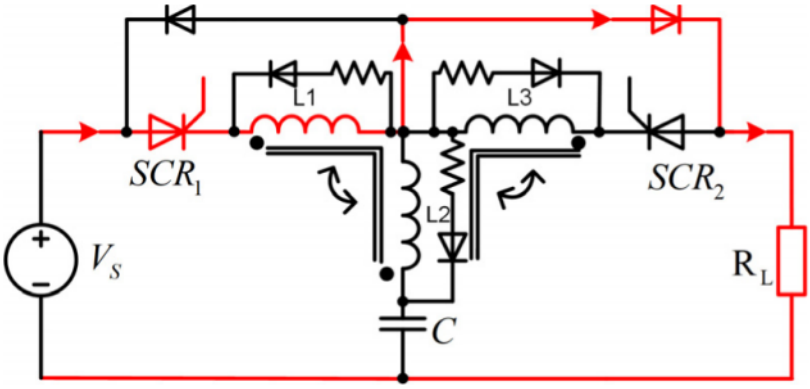

Figure 2.6: The bidirectional Z-source SSCB with transformer

To reduce the conduction power loss and volume, a structure with five capacitors was designed which is shown in Figure 2.7. During the normal working conduction, the energy will flow through the two inductors and thyristor and the conduction loss is effectively limited [48].

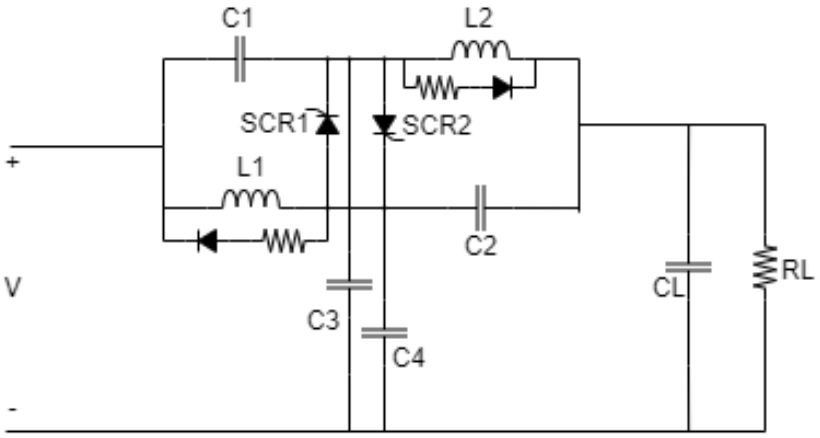

Figure 2.7: Novel bidirectional DC SSCB

2.2.4 *SSCB applied on renewable energy*

Environment protection encourages the development of renewable energy and the SSCB is also widely applicable for this opportunity. Electric vehicles are one of the low carbon technologies but the increasing number of electrical vehicles and the supporting infrastructure results in significant challenges for urban construction [49]. The demand of urban loads is always evolving because of the development of the

city and the intermittent nature of the load. As the voltage level of high power electric vehicle charging stations could reach several kilovolts, resulting from the power density, any fault in the supply grid will result in the fault voltage being several times greater and so potentially destroy the loads and protection equipment simultaneously. The easiest way to solve this issue is to use protection equipment with higher rated voltage, but the planning and construction time for urban infrastructure and limits in urban space, make this hard to be realised [50]. As an alternative, additional fault current limiters (FCLs) are proposed to limit the fault voltage between the maximum withstand voltage of protection equipment and the rated working voltage to protect the protection equipment and loads.

There are two main types of FCLs, one of them is the variable impedance superconductors and another is the solid-state FCLs based on SiC power semiconductor electronics [51] [52] [53]. Compared with the variable impedance superconductors, SiC solid-state FCLs have two main advantages, wider bandgap and higher breakdown electric field. The wide band gap of SiC supports the SSFCL to work at junction temperatures exceeding 600 °C with very little junction leakage current, which is of significant benefit for reducing the volume of the FCL and protection equipment by simplifying the requirements for the cooling system. The higher breakdown electric field of SiC, in comparison to conventional semiconductors, allows the device to have a thinner drift region and to reduce the device size, resulting in a 100 times faster reaction speed [54]. This enables the reduction in the size of passive components in the snubber circuit, such as capacitors that are physically bulky at high voltages. Additionally, the higher breakdown electric field increase the rated voltage for each device and offers the potential to reduce the number of series connected devices in high voltage applications. By reducing the cooling system and the number of devices, the size of protection system can be reduced [55] [56] [57].

Battery storage is an important technology for renewable energy, especially when faced with an unstable power supply, such as wind turbine generation and solar energy coupled with the demands of the changing energy demand. A battery has the potential to store excess energy and supply the power when the demand exceeds supply. The battery storage system has two parts, including the energy storage

station and subsequent transmission. As the voltage level and the protection requirements are different for the two sections, the protection equipment for them are different [58].

The battery station is composed of a number of multi-series connection low voltage level battery rooms. It is required to supply high quality and stable power for the grid, therefore, a common bus breaker is not suitable and each battery room requires a DC circuit breaker. When one battery room demonstrates a fault, the breaker may isolate the single room with the fault and enable the remaining rooms to operate as normal to ensure the stable power supply. However, increasing the number of breakers results power loss and maintenance costs, so each breaker is required to have reduced conduction losses and fast reaction speed. To meet these requirements, SiC-SSCB is preferred to be used as battery room protection device [59]. In contrast, transmission voltage is much higher and could reach several megavolts. Therefore the protection equipment is required to demonstrate high rated voltage, bidirectional isolation, small size and small thermal dissipation. A solid-state transformer based on IGBT-SSCB is suitable and have advantages in the protection equipment applications [60].

2.2.5 *SSCB applied on DC power system and converter*

During the past few decades, the semiconductor device technology for DC power converter has been one of the hot topics and the utilisation of that increases sharply in a number of applications, including renewable energy, automobile, DC power system and telecommunication [61] [62] [63] [64] [65]. To improve the performance of the DC power converter, research has focused on the development of low power loss, higher rated voltage and operating temperature switching devices [66]. Therefore, the SiC MOSFET, which has the higher power density, reliability and operational temperature, is widely used in high performance DC power converters, where a fast reaction, high reliability, low power loss and low cost protection equipment is required to isolate it from the short circuit fault [67]. There are two main problems that make the SiC MOSFET highly suitable for high performance circuit breakers. Compared with SiC JFET, the SiC MOSFET has smaller chip area and higher

current density, however, these result in the lower short circuit withstand ability of the SiC MOSFET and it increases the requirement of reaction speed of protection equipment [68]. Secondly, the thinner oxide in comparison to conventional silicon based devices, to decrease the threshold voltage results in the poor interface quality and low reliability [69]. Three methods are proposed to build the protection circuit for SiC MOSFET converter, including the SSCB, the desaturation technique and the active dynamic fault evaluation overcurrent protection. Compared with other two methods, SSCB has three advantages. Firstly, the small size makes the SSCB is easily integrated into a gate drive circuit. Secondly, the protection performance of SSCB is not decided by any specific devices. It means the SSCB could be applied in converters based any kinds of power semiconductor device. Finally, the SSCB could be applied in all voltage/current level protection, but the power loss under high power application, like the back-to-back converter in renewable energy system, should be considered [70].

The consideration of the SSCB applied in DC power system and converter includes the device and circuit topology. Silicon IGBT and IGCT have be widely used in SSCB for DC power converter. The current sensor assists the control system to block the circuit when the fault occurs and the clamping circuit is used to absorb the energy caused by fault current to protect the SSCB [71]. In addition, the SSCB based on the silicon IGBT has a fast reaction speed, which reaches a few microseconds, in the protection of 10-kV/1-kA DC power system [72]. The SiC semiconductor devices, including SiC JFETs, MOSFETs and SITs, are also preferred in SSCB for DC power converter because they have lower power loss, higher power density and can be operated under a higher temperature. In addition, the SiC JFET and diodes can connected in a back-to-back structure to realise the bidirectional SSCB, which has been reported in [73]. Furthermore, a self powered SSCB combined with a DC converter, with low conduction loss and fast reaction time without any auxiliary power sources, is proposed to simplify the drive circuit for SSCB in DC power system protection [74]. The schematic of the self powered SSCB is shown in Figure 2.8. The self powered SSCB uses the normally on SiC JFET to control the circuit, which can reduce the power loss because the JFET has no requirement of power

during the normal operation condition. In addition, the voltage across the device is used as the feedback signal to detect the operation condition of circuit but not the Drain current, and the Gate is controlled by the leakage power from a fast reaction DC/DC converter when the fault occurs [74].

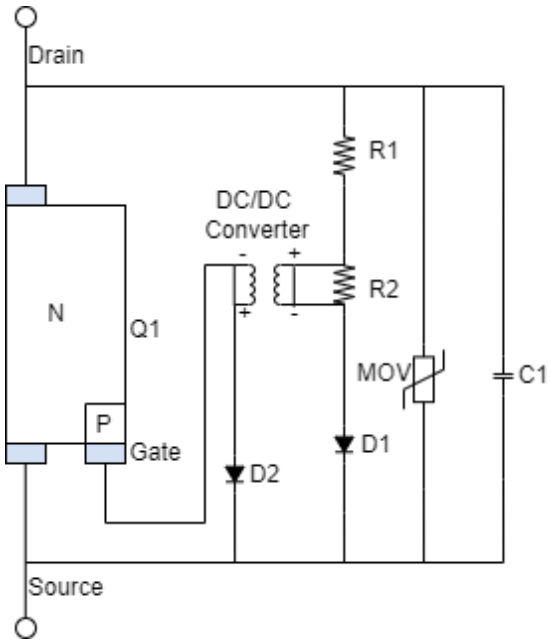

Figure 2.8: Self powered SSCB

2.3 Key issues and challenges within the technology

As described previously, SSCB is the preferred solution in multiple DC power applications and current research is seeking to improve the performance by minimizing the power loss, increasing the power density whilst reducing cost, including the the selection of the power semiconductor devices, circuit topologies, the design of the overvoltage clamping and overcurrent limit circuits, the control system and the drive signals, recognition and sensing of the fault current in circuit [75]. The key technical challenge for each topic is described as well as an outline of the future plans for SSCB development.

2.3.1 *The power semiconductor technologies*

The power semiconductor device is one of the most important components when designing the SSCB. Normally, the selection of the power semiconductor is based on the technical requirements of the application, and the optimisation of the topology will be designed later to realise the combination of different devices in SSCB. Therefore, it is important to understand the characteristics of the relevant power semiconductor device types. The main characteristics considered when selecting the power semiconductor devices are the current blocking direction, overvoltage withstand capability and the passive characteristics of the power semiconductor devices, including the semiconductor material used in devices, the internal structure of the devices and the devices are normally on or normally off devices.

Bipolar power semiconductor devices can conduct or block the current in both directions, which makes them widely used in bidirectional applications, such as the electric vehicles and power station charging [76]. In contrast unipolar devices normally conduct or block current in a single direction. A greater number of devices and a complex topology are required to form the system to realise the bidirectional capability, which increases the cost and reduce the reliability of the SSCB. Therefore, the selection of whether the device is bipolar or not, is based on the application requirements of the SSCB and this has a significant impact on the topology design.

The overvoltage withstand capability is another important characteristic of the power semiconductor devices. As the SSCB is designed for use in circuit protection, it will be required to withstand an overvoltage which is normally 2 or 3 times the rated voltage, when the fault occurs. If the fault voltage of the application exceeds the breakdown voltage of the power semiconductor devices, the SSCB may be destroyed and cannot protect other devices in the circuit. The rated breakdown voltage of the power semiconductor devices depends on the semiconductor materials and the structure of the devices. The current-voltage relationship of the main power semiconductor devices on the market, with different materials and structures, are summarized in Figure 2.9 [12].

The power semiconductor devices can be divided into two categories according to the material properties of the semiconductor material. One observation from the

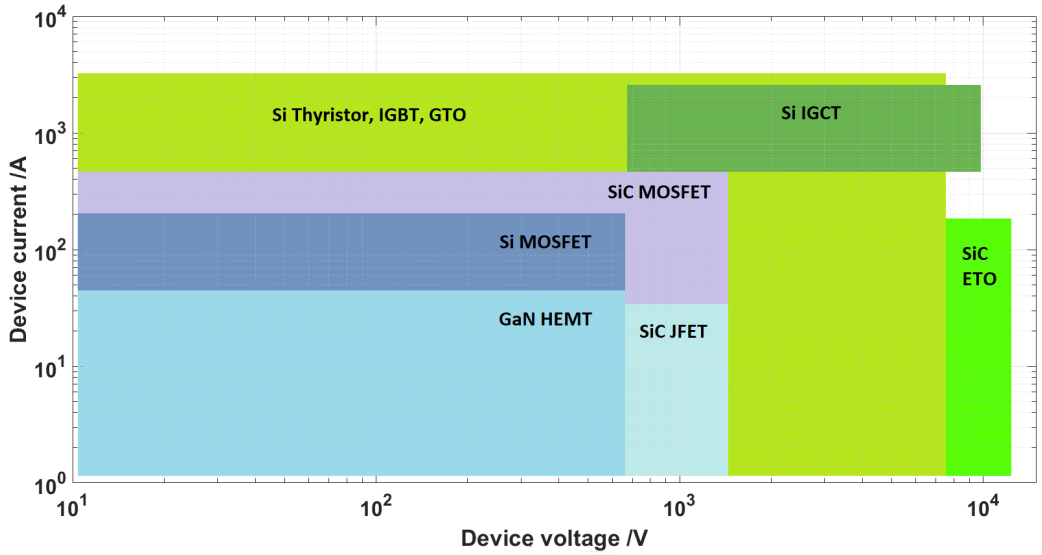

Figure 2.9: IV relationship of power semiconductor devices

Figure 2.9 is that silicon (Si) devices can withstand an extended range of the voltage level and the current depending on the device type. Wide bandgap (WBG) devices, including those manufactured from silicon carbide (SiC) devices and gallium nitride (GaN) have the superlative material properties to support the power semiconductor devices for high temperature and voltage operation. Furthermore, WBG devices can be operated with higher switching speed, which can increase the efficiency, reaction speed and decrease volume of the system using the WBG devices [77].

Besides the choice of semiconductor, the structure also has a significant impact on the rated voltage of power semiconductor devices. Silicon devices have many fundamental structures, including the thyristor, insulated-gate bipolar transistor (IGBT), gate turn-OFF thyristor (GTO), integrated gate-commutated thyristor (IGCT), emitter turn-OFF thyristor (ETO), metal-oxide-semiconductor field-effect transistor (MOSFET) and junction field-effect transistor (JFET). The MOSFET and the JFET are unipolar devices, while the thyristor, IGBT, IGCT, GTO, ETO are all the bipolar devices. According to the Figure 2.9, Si bipolar devices are suitable for operation in the medium voltage range, which is from around 1.5 kV to 7.5 kV, and a high current range, which is from 500 A to 3 kA. This voltage range supports the use of Si bipolar devices such as those found in power distribution net-

works, especially the high power and voltage applications. Meanwhile, the Si bipolar devices have the high short circuit ability and gate oxide reliability in high power applications [78]. As for the WBG devices, the SiC ETO has the highest maximum rated voltage which reaches 10 kV, and the SiC MOSFET and SiC JFET have 1.7 kV maximum rated voltage which is higher than the 650 V maximum rated voltage of the GaN HEMT. As for the current, the maximum current of the SiC MOSFET and the SiC ETO are very close, at around 500 A and 250 A. Current generations of GaN HEMT and the SiC JFET can withstand around 50 A. Although the rated voltage and the current of the WBG devices are lower than Si devices, the WBG devices can be applied in the high temperature and the high switching speed applications, as well as the low conduction power loss applications such as the circuit breakers. In addition, the performance and static characteristics of WBG devices will be expected to rise as the technology matures.

Si and WBG devices have all been considered for the design of SSCB. SSCBs based on the Si bipolar devices, including the Si IGBT, Si GTO/ETO and Si IGCT are the preferred choice for medium voltage distribution systems and high voltage DC applications, because of the good reliability in long term operation and the good capability of fault overcurrent [79]. For example, a 600 V/6 kA hybrid switch based on the Si IGBT has been demonstrated for the realisation of a bi-directional DC zero voltage switch. Furthermore, six parallel IGBTs structure has been verified in overcurrent test and the maximum current shared by IGBTs reaches a peak of 8000 A [80]. The DC electric railways also require the fast operation when used as a circuit breaker to reduce the damage from the short current to the equipment. Meanwhile, the high thermal conductivity of the semiconductor and packaging is a challenging design requirement for circuit breakers. Therefore, a new hybrid circuit breaker, comprising an IGCT and mechanical breaker, has been proposed which has the advantages of both the mechanical breaker, which has a low power loss caused by a contact resistance below 10 $\mu\Omega$, and power semiconductor breaker, which enables fast operation with a reaction speed around a hundred microseconds. This was demonstrated in 4 kA/ 1.5 kV system [81]. A low on-state voltage and a fast switching speed GTO breaker is also presented for protecting a 4.5 kV /

3 kA circuit [82]. Furthermore, the improved devices ETO, which comprises a combination of a GTO and a MOSFET, is also widely considered to be optimal in 15 kV / 200 A and 22 kV medium voltage distribution applications [83] [84].

Unipolar Si MOSFET SSCBs normally are used in low voltage and low power applications, because in the low voltage and low power applications, the Si MOSFET has a little higher efficiency and much lower cost, in comparison with WBG devices [85]. One of the typical Si MOSFET application is the more electric aircraft distribution system, which uses ± 270 V / 200 A DC power supply. Furthermore, the SSCB based on Si MOSFET has a good overload capability, with operation around 2000 A demonstrated, and low power loss both in steady state and transient state in this application [86]. The Si MOSFET can also be used to realise a SSCB with a 1200 V SiC JFET in a cascade configuration for 400 V / 25 A applications. When the fault occurs, the gate drive circuit for the MOSFET will generate positive chain reaction with the MOSFET, which is series connected with the drive circuit, and it will establish the negative Gate-Source voltage for JFET and hence turn it off [87].

In contrast with Si devices, commonly used WBG devices are unipolar, including the SiC MOSFET, SiC JFET, and GaN bidirectional FETs [88]. As a hot topic of recent research, multiple SSCBs based on the SiC MOSFET has been reported in the literature. For example, the compact 700 V SSCB is designed for the high temperature application, which can work in environments up to 200 ℃ [89]. The SiC MOSFET can also be used in high power and middle voltage application, and a 25 kW / 1200 V unidirectional SSCB based on the SiC MOSFET has been designed, which can detect the fault current within 0.9 μs [90]. In contrast with other published results, that SSCB uses the desaturation detection method to detect the short circuit fault rather than detecting the overcurrent by current sensors, which results in that SSCB has a faster reaction speed [91]. As for the overcurrent, the SiC SSCB can operate with the cooling system to allow a range of overcurrent through the circuit for longer time meanwhile remains the fast reaction speed to limit the fault current compared to the normal operation, which increases the overcurrent withstand ability and reliability of circuit. That SSCB with the air cooling system can conduct 102 A

fault current for over 50 minutes and the fault current can reach over 300 A when the SSCB is operated with the liquid cooling system [92]. Therefore, the SiC MOSFET SSCB is a flexible device and can be widely applied to DC circuit protection for a range of voltage and power requirements.

Another SiC unipolar device, with a good performance in SSCB, is the SiC JFET. There are a number of significant advantages in the use of SiC JFETs in circuit protection. Firstly, the SiC JFET has a very low on resistance, which results in lower power loss and higher efficiency during normal operation. Secondly, in contrast to the MOSFET, SiC JFET is a normally on device, which means it does not require the drive current to turn on the device, but just the shut down signal [93]. It is suitable for the working conduction of SSCBs and reduces the complexity and the power loss of the drive circuit under normal operating conditions. In addition, the SiC JFET is also reliable in long time operation under the hard switching and high temperature conditions. The SSCB based on the 1200 V vertical-channel implanted-gate SiC JFET can be repeatedly pulsed over 2.4 million times at 150 ℃, and block 115 A conducting current, which is 13 times over the rated current of the SiC JFET under 150 ℃ [94].

GaN is another WBG material that has attracted significant interest in SSCB design in recent years, because it has the high critical electric field, lowest on resistance among the commercial WBG unipolar devices, and low gate charge which can reduce the turn on and shut down time of the GaN power semiconductor devices [95]. GaN based power electronics such as the GaN HFET have lower commutation loop and parasitic inductance, enabling high switching speed, which enables the SSCB to increase operating efficiency and hence power density [96] [97]. The relevant voltage level for the GaN HFET structures is around 600 V, which has the direct competition with the Si based devices [98]. However, in contrast with Si based power semiconductor devices, the GaN HFET is a lateral structures, which give it more freedom for monolithic integration with additional diodes, half-bridge modules and integrated gate drivers [99].

SSCB based on bipolar WBG semiconductor devices is suitable for high voltage applications, because the bipolar WBG semiconductor devices have high knee volt-

age which result in increased power loss in low voltage applications. As an example, a 4.5 kV SSCB based on the 15 kV SiC ETO has been verified to successfully block the fault current over 200 A, which demonstrates the suitability for medium voltage power distribution applications [100].

2.3.2 *The circuit topology for SSCB*

As mentioned previously, the circuit topologies are optimized based on the requirements of the specific application and the characteristics of the power semiconductor devices including the power loss, rated voltage and the switching speed. In this section, the widely used circuit topologies for SSCB circuits are introduced.

The anti parallel reverse blocking structure is one of the preferred topologies for the SSCB design, which is shown in Figure 2.10, offering low power loss during conduction and can block the current from both directions in the circuit, which makes it is more flexible and more efficient in circuit protection applications.

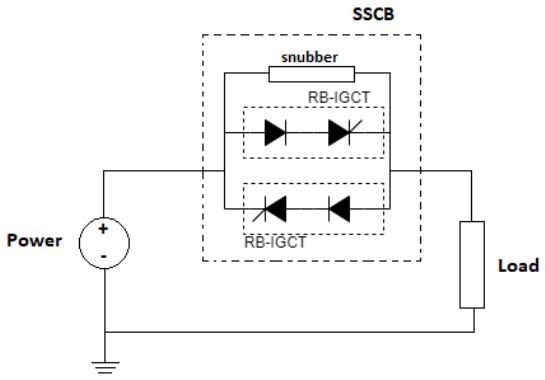

Figure 2.10: SSCB based on anti parallel reverse blocking IGCT

The anti parallel topology can reduce the number of active devices by 60% and the on state voltage drop by 70%, in comparison with the conventional H-bridge topology at an equivalent voltage level, which results in a significant advantage in overall system power loss [101]. A range of fully controlled power semiconductor devices can be utilized in the realisation of the reveres blocking SSCB, including the IGCT, MOSFET and JFET. The conduction of the IGCT is similar with a thyristor, which results in the low power loss, and the integration of the low inductive gate results in the high hard switching capability, which is similar with the IGBT during

blocking processing. Therefore, comparing with the IGBTs, the IGCTs have the lower voltage drop during conducting and are preferred in the design of reverse blocking SSCB. As an example, a 1 kV DC bidirectional SSCB based on the reverse blocking IGCT has been designed [102].

Reverse blocking IGCT (RB-IGCT), as a current controlled switch with the integrated gate, is normally used to solve the phase change fault and the enable protection in HVDC power systems [101]. The package and the structure of the IGCT is similar to that of the GTO. However, compared with the GTO, the IGCT has lower on state voltage and better hard switching turn off capability, because during the conduction, the IGCT operates in a manner similar to a thyristor and the low inductance of the integrated gate. Furthermore, the IGCT has no problems relating to the overvoltage snubber circuit, which reduces the complexity of the circuit design [103]. The performance of the SSCB based on RB-IGCT devices has been verified in 1 MW application, demonstrating low conduction loss, which is less than 1 kW operating with 1 kA current, and can block the fault current higher than 6.5 kA, with a voltage drop below 1 V [104].

The JFET, with normally on operation, is significantly different to the MOSFET or IGBT when used in bidirectional power electronic circuits, including matrix converters, multi-level converters and solid state breakers [105]. The diagram of JFET bidirectional SSCB is shown in Figure 2.11.

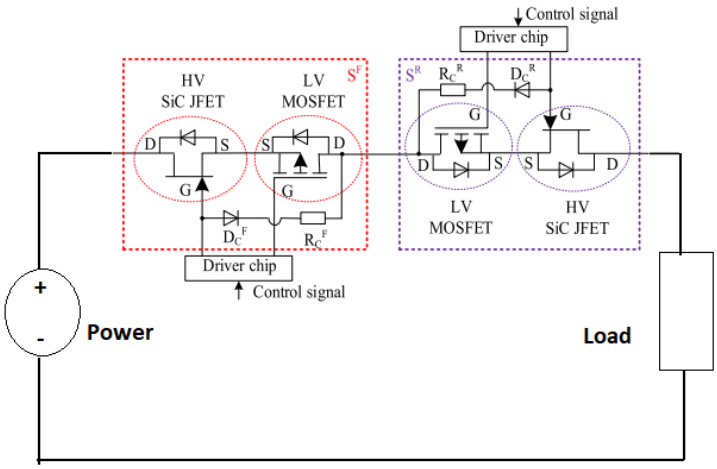

Figure 2.11: The diagram of JFET bidirectional SSCB

To realise the bidirectional capability, the SSCB based on the MOSFET or IGBT normally requires two MOSFETs and two anti parallel diodes, which increases the number of the devices in the circuit. As an improvement, the JFET device can form the bidirectional switch with two anti series connection SiC JFETs without any anti parallel diodes, which reduces the weight of the power electronic circuit. In this structure, the forward and reverse current are carried by the main channel of JFET rather than the body diode, which reduces the conducting power loss because the on resistance of the JFET is much smaller than the on resistance of the body diode [106]. Besides the advantages introduced above, the bidirectional SSCB based on the anti series connection SiC JFET structure also has the high operation switching frequency and efficiency. Normally, the normally on SiC JFET will be cascode connected in the protection circuit with a low voltage Si MOSFET, which is used to solve the potential safety issues of JFET during turn on or abnormal gate driver conditions. However, in this conventional cascode structure, the control of the SiC JFET source potential is indirectly realised by controlling the MOSFET, which limits the maximum switching frequency and efficiency. To solve the problem, two cascode structures are anti series connected where the MOSFET is permanently conducting which can be regarded as a resistance and the JFET can be directly controlled by drive signal which increases the operation switching frequency and efficiency [107].

MOSFETs are also widely used in reverse blocking bidirectional circuit breakers. To improve the reverse blocking capability of the MOSFETs in bidirectional SSCB applications, a novel vertical MOSFET with the high workfunction Schottky-Drain and Schottky-Drain connected semisuperjunctions (SD-D-semi-SJ MOSFET) has been proposed, which has the significantly high reverse breakdown voltage and low specific on resistance compared with the SD-SJ MOSFET and SD-semi-SJ MOSFET [108]. The SD-D-semi-SJ MOSFET is composed of the SD-connected semi-SJ structure and top assist layer, while the schematic is shown in Figure 2.12. Meanwhile, in 3 kV applications, the conduction loss of the reverse blocking SiC MOSFET bidirectional breakers is 35% lower than the traditional anti serially connected structure and the blocking voltages in both directions are higher than 3 kV, offering a

significant advantage over the reverse blocking SiC MOSFET SSCB in the high voltage bidirectional applications [109].

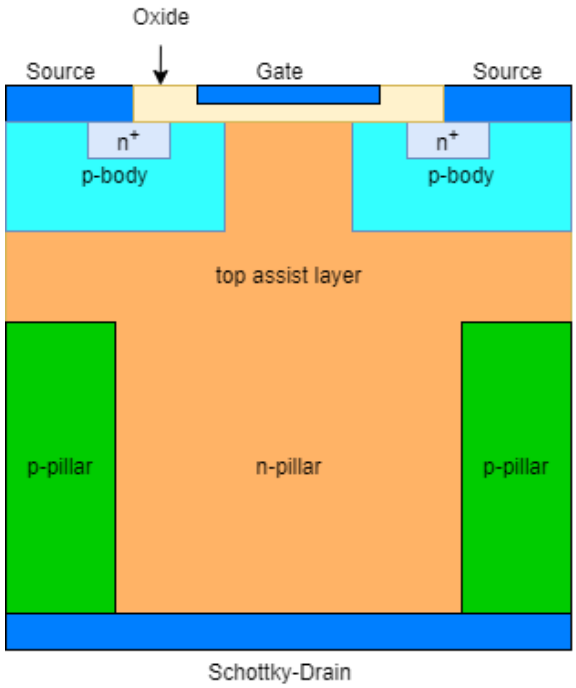

Figure 2.12: SD-D-semi-SJ MOSFET schematic

Normally, reverse blocking SSCB circuit are formed using the fully controlled power semiconductor devices, and there are also a range of topologies for semi-controlled devices such as the silicon-controlled rectifier (SCR) in SSCB design, including the voltage or current source breaker, the Z source breaker, the T source breaker, coupled inductor breakers [110] and the H-bridge type breaker [111].

The anti-parallel SCR is a low conduction loss SSCB topology which is suitable for high current applications. However, because this topology cannot block the current through the gate terminal without additional components, the SSCB based on SCR devices requires additional circuit to help blocking the current. There are two common methods to solve the problem, one is using the voltage source such as the capacitor to help blocking the current for the SCR, which is called the voltage source circuit breaker [112], the other is directly creating a zero current crossing, which is called the current source circuit breaker [113]. The Diagram of the anti-parallel SCR SSCB is shown in Figure 2.13.

In addition to the voltage source and the current source circuit breaker topologies,

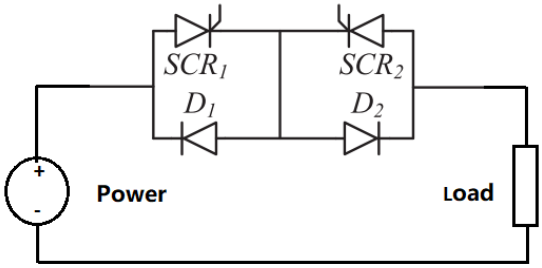

Figure 2.13: The Diagram of the anti-parallel SCR SSCB

the Z-source breaker is also based on the use of SCR devices. Z-source circuit breakers are widely used in low voltage and medium voltage applications, such as onboard ship power systems [114]. The traditional SCR breaker blocks the current by the series connection of the auxiliary SCR and the passive resonant devices. When the fault occurs, the auxiliary SCR needs to turn on and shut down the main switch before the fault current over the withstand ability of the main circuit. After that, another SCR will reset the capacitor ahead of the next turn off cycle. However, this operation method results in a number of significant problems, one of those is the critical requirement of the detection and reaction speed. To solve the problem, a Z-source breaker with LC circuit has been proposed, which can automatically switch the main SCR circuit during the fault. Compared with the traditional SCR breakers, the Z-source breaker has a number of advantages, including the fast reaction and operation speed, simplified control and higher reliability of the source and SCR devices, because the fault current does not pass through them [115]. A significant issue for SCR breakers is the control method, which can react to extremely large transient faults. To solve this issue, a new control strategy, which can react according to both the rate of the fault current rise and the absolute value of the fault current, has been proposed [116].

The T-source circuit breaker has further advantages over the Z-source breaker, including the incorporation of a low pass filter, common ground and no reflected current. However, because of the higher number of semiconductor devices required in the circuit, the power loss is an order of magnitude greater than an equivalent Z-source topology. Therefore, a new type of the bidirectional T-source circuit breaker has been developed that uses fewer semiconductor devices and can reduce more

the condition power loss by over 40% in comparison compared with the traditional T-source breaker topologies [117]. The diagram of bidirectional T-source SSCB is shown in Figure 2.14.

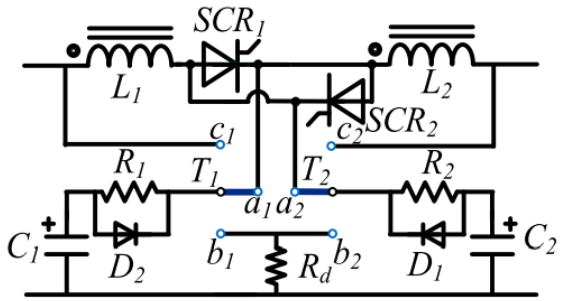

Figure 2.14: The diagram of bidirectional T-source SSCB

Normally on devices such as the JFET have the advantage in SSCB compared with the normally off device, simplifying the control circuit for the JFET, hence the operating process of the JFET is more suitable for the circuit breaker. The widely used topology for JFET is the series connection of multiple JFETs in a super cascode configuration, with the MOSFET control circuit, for the high voltage applications. However, the challenge in this topology is the voltage balance between the JFETs during the turn on and turn off transients. If the voltage is not balanced during switching, the fault overcurrent may result in significant imbalance between individual devices, resulting in permanent damage. Therefore, a new topology utilizing JFET without the MOSFET control circuit has been proposed, which incorporates a dynamic and static voltage balance network. The circuit diagram is shown in Figure 2.15. In the topology, the diode is used to protect the JFET from the overvoltage higher than the DC power supply divided by the number of the JFET. The capacitors are used to balance the dynamic voltage shared by devices during the turn on and turn off processing. Two resistor networks are used to balance the static voltage across the JFET. The design ensures the equal sharing of the voltage during the switching processing and reduces the power loss at the same time, and can be applied in the HV/MVDC protection system [118].

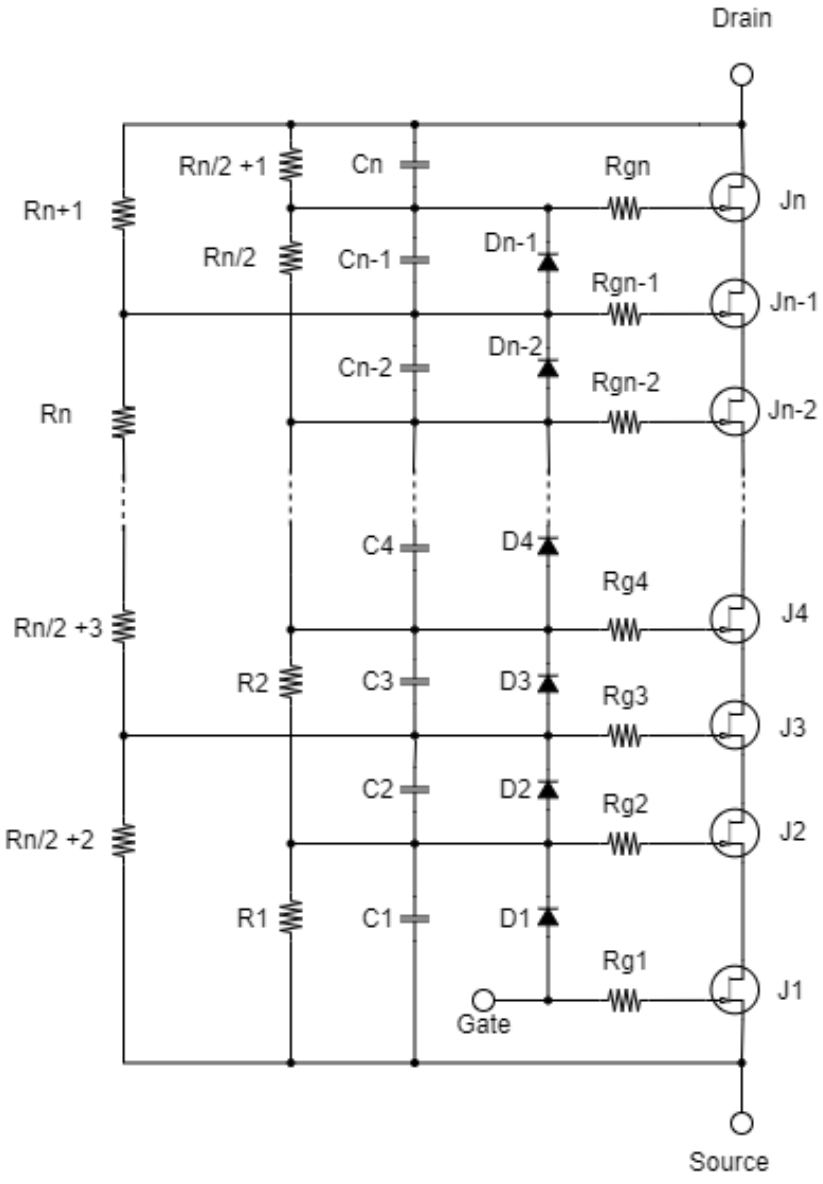

Figure 2.15: Single gate drive for series connected JFET

2.3.3 *The snubber circuit*

The SSCB can protect the overall power circuit from faults, however, the series connection SSCB topology normally has to withstand significant overvoltage and overcurrent during the fault condition, which may destroy the power semiconductor devices. Therefore, the SSCB should not only protect the circuit but also protect itself, and the voltage clamp is proposed to reduce the overvoltage stress on an individual component or replace the power semiconductor device to withstand the fault voltage and current. The clamping circuit is normally connected in parallel with the solid state switch and comprises by the energy-absorbing components and acts as a low pass filter. The design is based on the characteristics of the energy-absorbing components including the clamping voltage level, the ability to absorb energy and the peak value of the fault current. Several designs of the clamping and snubber circuit are introduced in this section, including the transient voltage suppression (TVS) diode, metal oxide varistor (MOV) and the capacitor based snubber circuit [119].

The simplest snubber circuit is the parallel connection of the capacitor with the power semiconductor device. During the fault condition, the capacitor will be charged and the rate of change and the peak voltage across the power device will reduce. However, the capacitor can process oscillations in the circuit with any parasitic inductance and so the RC snubber is proposed to solve the problem, which is composed by the capacitor and a series connected resistor [120]. Furthermore, the inclusion of the resistor results in the voltage drop of the power semiconductor switches during the turn off process, and so a further improvement, named the RCD snubber is proposed, which is composed of a RC snubber circuit with a paralleled diode across the resistance. RCD snubbers can not only reduce the voltage drop during the turn off but also significantly reduce the oscillation [121].

TVS devices can absorb the fault energy by transforming the overload current to replace the devices in the main circuit and hence clamping the fault voltage within the safe range for the power device. With the development of high speed IC circuits, TVS devices are required to operate with a faster reaction speed and the low parasitic inductance, as well as the ability to clamp the voltage at a low level at the high fault current. Therefore, the electrostatic discharge (ESD) TVS is

proposed. The ESD TVS is based on the reverse biased P-N junction diodes, which will breakdown at the voltage level 10% to 20% higher than the rated voltage. The main advantages of this type of overvoltage protection is the fast reaction speed and the lack of snapback. However, the high resistivity results in high clamping voltage when operated with a high fault current [122]. The active voltage clamping circuit series string of the TVS can also be used in 1.2 kV SSCB applications to realise low cost and reduce the overall size of the SSCB [123]. The small size and low weight make this suitable for the more electric aircraft system [124]. TVS devices can also be applied in the drive circuit for series connection power semiconductor devices in SSCB, where the TVS helps coupling the gate drive signals [125].

MOV is another type of the widely used snubber circuit in SSCB design, which can be made from materials such as zinc oxide. In the SSCB design, it is paralleled with the power semiconductor switch. When the main circuit operates under normal condition, the voltage across the MOV is below the clamping voltage and the MOV shows a high impedance. The current will pass through all the power semiconductor switches, which are series connection in the main circuit. When the fault occurs, the power semiconductor switch blocks the circuit and the voltage across the switch and the MOV snubber circuit rises to the clamping voltage. In this condition, the impedance of the MOV decreases rapidly and the overcurrent will pass through the MOV, which reduces the overcurrent stress of the power semiconductor switch, and absorb the fault energy within the MOV [126]. To verify the performance of the MOV, a range of characteristics should be considered, including the voltage clamping performance, the operation voltage range and the surge current capability. Compared with the TVS snubber circuit, the MOV has wider operation range which can reach 3.5 kV per device, lower cost and the capability to absorb the overcurrent is also greater. However, the drawback of the MOV is the high ratio of the peak clamping voltage and the maximum operation voltage, which reduce the operation voltage level at the DC bus for solid state switch [127]. Therefore, to apply the MOV in the high voltage DC power system, the rated voltage requirement of the main solid state switch becomes critical. The electronic MOV (eMOV) is proposed to decouple the peak clamping voltage based on thyristor technologies to increase the SSCB

efficiency, power density, reliability and reduce the cost. Meanwhile, the eMOV has less conducting loss and smaller size compared with the traditional MOV [128].

To ensure the fault current can be blocked, the clamping voltage is normally established to exceed the system voltage, which enables faster shut down speed. However, the high clamping voltage has a negative impact on the voltage clamping performance of both the MOV and TVS and results in more voltage stress to the system. Otherwise, if the clamping voltage is too close to the system voltage, the shut down time will be excessive and may result in the damage to the devices in the main circuit. Therefore, the clamping voltage is preferred as 1.5 times to 2.2 times of the steady state reference voltage of the SSCB [120].

2.3.4 *The gate drive circuit*

Besides the choice of the power semiconductor devices and the clamping circuit, the drive circuit is also critically important for the design of the SSCB circuit. The drive circuit is used to apply the control signal to enable conducting or blocking of the power semiconductor devices, according to the condition of the main circuit. The drive circuits for different power semiconductor devices and topology have different requirements. For example, MOSFETs and IGBTs are both voltage driven devices and the drive circuit required is a voltage drive circuit. In contrast the thyristor is a current driven device and the drive circuit has to supply a specific current. Meanwhile, the control logic is also decided by the static characteristics of the power semiconductor devices such as normally-on or normally-off. Furthermore, according to the different voltage requirement of the application, the power semiconductor devices can be a single device or multiple in series connection, and the drive circuit for them can be classified appropriately. In contrast with the drive circuit for a converter, the SSCB drive circuit does not work at high switching frequency and simply controls the circuit transition from conducting to blocking when the fault occurs. Meanwhile, the drive circuit for SSCB will continually supply the drive power to support the operation of the power semiconductor devices whilst in the on-state or off-state. Therefore, the power loss of the drive circuit is mainly determined by the on-state and off-state power requirement of the power semiconductor devices,

rather than the switching power loss.

With increasing the power demand, the voltage level of power distribution systems is rising, which results in the increase of the rated voltage requirement of any SSCB circuits used for protection. However, the rated voltage of the most commonly used single power semiconductor device in SSCB design cannot exceed 10 kV with current technology level. Therefore, a series connection topology is required to support the SSCB to be used in high voltage applications such as distribution and transmission networks. The series connection results in new challenges for SSCB design and one of these is the drive circuit design. For the SSCB based on a single power semiconductor device, the drive circuit needs to operate the single device only. However, in series connection topology, the balanced voltage distribution during the shut down is significantly important, because the unbalance voltage may exceed the rated voltage of the device used in SSCB, resulting in damage. To balance the voltage distribution, the drive circuit is required to operate the series devices synchronously, which is different with the operation of the drive circuit in converter.

The single drive circuit based on the passive components and diodes is proposed to balance the voltage distribution between two series connected MOSFETs, which is shown in Figure 2.16 [129]. This circuit has a small cost because of the small number of devices, and has demonstrated a 1.5 μs shut down time.

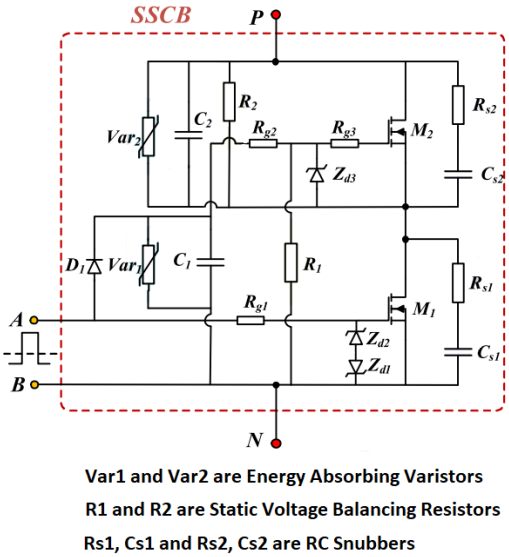

Figure 2.16: The single drive circuit based on the passive components and diodes

Furthermore, a single gate drive circuit for three series connected IGBTs is proposed and the circuit diagram is shown in Figure 2.17. It has higher power density and lower cost, however, it is difficult to realise the synchronisation of the turn-off within three devices and the shut down start time for the three devices are different, resulting in gate oscillation and the voltage unbalance between the devices during the voltage recovery process [130].

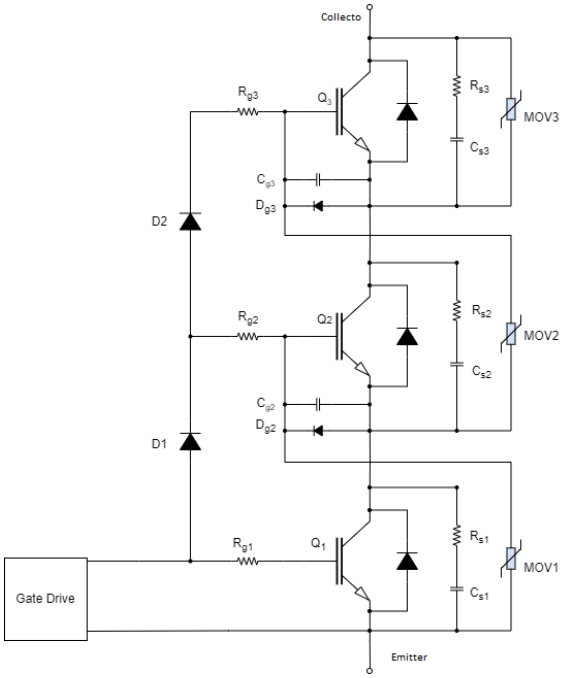

Figure 2.17: Circuit diagram of single gate drive for three series connected IGBTs

Besides the signal gate drive circuit for series connection topology, the challenge of realizing multiple gate drive circuit is also a hot topic in this research area [131] [132] [133] [134] [135]. In contrast to the signal to the gate drive circuit that controls multiple power semiconductor devices connected to the passive devices such as diodes and capacitors, the multiple gate drive circuit supplies the individual control signals for each power semiconductor device separately. This results in the multiple gate drive circuit having significant the advantage in applications that require increased numbers of power semiconductor devices connected in series [136]. The schematic of the drive circuit for series connection power semiconductor devices is shown in Figure 2.18.

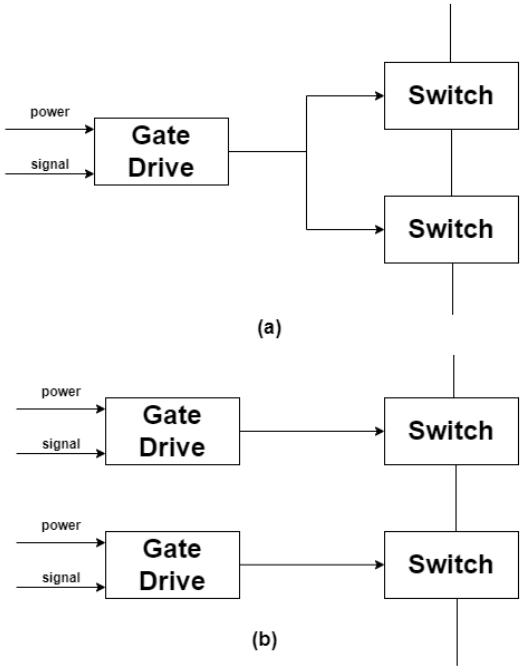

Figure 2.18: The drive circuit schematic for series connection switches (a) A signal drive circuit (b) each switch has an independent drive circuit

2.3.5 *The fault detection and sensors*

The Gate drive circuit controls the power semiconductor devices according to the condition of the main circuit, therefore the feedback signals which show the characteristics main circuit condition are required. To collect the feedback signals and create a closed loop control system, the sensors and the method to detect the circuit fault with a low time latency are required in the SSCB design. The control system, as a real time system, is required to demonstrate fast reaction and high operating speed, therefore, as an important part of the control system, the sensor requires a high bandwidth to detect the rapidly rise fault current and voltage. Because the step fault signal detected by the low bandwidth sensors will be distorted, resulting in the detected rise time to be greater than the actual rise time, increasing the response time of the control system. Furthermore, the main circuit operates in the conduction condition the majority of the time and the power loss resulting from the main circuit current through the sensors should be limited, which results in the low power loss requirement of the sensors. Besides the fast reaction and the low power

loss, the interface and the compatibility with control systems should be considered when selecting the sensors for the control system [137].

A large number of different current sensors can be used to measure the current value, including the current shunt [138], the hall effect current sensor [139] and the giant magneto-resistive current sensor [140], which are the direct current measurement sensors. Besides directly measuring the current, there are also indirect current measurement methods applied in SSCB design, including assuming the current can be determined from knowledge of the voltage across the main power semiconductor device and the rate of change of the current [141], and detecting the slope of the main circuit current to reduce the delay which results from the fault current rise time and the operation speed of the control system. Because the slope of the current is significant at the beginning of the fault condition and can be detected earlier by the control system in comparison to the method that compares the current with a threshold value. Hence, the current slope detection method can increase the reaction speed of the control system [142]. The calculation of the current slope is realised by the analog or digital circuit, rather than directly from the sensors in the circuit. The challenges for current slope detection are the accuracy and speed of calculation, and the risk of false triggering [143].

As the SSCB is series connected in the circuit, the current through the SSCB is normally used to detect and evaluate the working conduction of the main circuit. When the circuit works normally, the current through the main circuit remains at the rated value. When the fault occurs, the current raises rapidly and can be detected easily. Therefore, the current threshold is used to evaluate the circuit working condition. Once the current value from the current sensors is larger than the current threshold, the main circuit must work under the fault and the circuit breaker will be triggered to blocking the circuit [144]. Furthermore, the voltage sensor can be used to detect the voltage across the power semiconductor device or the inductor, which can also be used to evaluate the circuit working condition [145]. A summary of three different sensors is shown in Table 2.1 [146]. However, the fair integrability of the hall effect current sensor increases the complexity of SSCB. The current shunt and rogowsik are better selections for SSCB design.

	Current shunt	Rogowski	Hall effect current sensor
Cost	low	low	high
Bandwidth	DC∼10 MHz	0.1∼100 MHz	close to 1 MHz [147]
Sensitivity	mV/A	10 mV/A	20∼150 mV/A
Saturation, hysteresis	No	No	Yes
Linearity	Very good	Very good	Poor
Operation temperature	-55∼125 ℃	-20∼100 ℃	-40∼125 ℃
Footprint	8×6×2.5 mm	Height < 4mm	6×5×1.7 mm
Integrability	Excellent	Excellent	Fair
Material technology	simple	simple	complicated

Table 2.1: Comparison of different current sensors [146]

2.4 The future of the SSCB development

Solid state circuit breaker can be widely used in low voltage and high voltage applications, both AC and DC, with the advantages including the fast response and suppressed arc breaking, resulting in high reliability and the long operation life. However it also has several challenges which are the requirements of the future design [148] [149]. Firstly, the on state resistance cannot be ignored, despite modern devices resistance value that is having a several milliohms. Acting as protection devices in the main circuit, the SSCB works in conducting condition the majority of the time, therefore the on resistance results in the rapid power dissipation and reduces the system efficiency, especially for long duration operation [150]. Secondly, the semiconductor devices are used in SSCB design as the switch to control the blocking and conducting of the circuit. However, these devices are sensitive to the overvoltage and overcurrent resulting from the circuit faults, which results in the design of the SSCB having to consider the main circuit protection but also protect the semiconductor devices from the circuit faults, to extend the service life [151]. Thirdly, the cost, weight and physical volume of the semiconductor SSCB are critical limitations for applications that have constraints in terms of power density and weight, such as deployment on aircraft [152]. Furthermore, the bidirectional SSCB is a hot topic for the future development, which results in the challenges including cost reductions and the number of devices, the complexity of the control system design and the lower reliability [153] [154] [155] [156] [157]. To be applied in the

higher voltage and power applications, the power semiconductor devices of SSCB are normally series or parallel connected, which results in the voltage or current balance problem and increasing costs [158]. The drawbacks mentioned above are all the future challenges for the SSCB design and a lot of research is trying to improve the performance of SSCB from several different aspects, including the higher quality power semiconductor devices, new topology and drive circuit design.

The development of the semiconductor technology has a significant impact on the performance of the SSCB. During the period between 1980 and 1990 silicon devices were widely used as solid state switches, such as the Si IGBT, Si IGCT and Si GTO. The technology of the silicon device is mature and it can be applied in a wide range of voltage and current applications. As an improvement, the wide bandgap semiconductor device was proposed in 1989 [159]. Compared with the traditional Si devices, the wide bandgap devices, such as silicon carbide (SiC) and gallium nitride (GaN) devices, have the faster shut down speed [160], lower power loss, better breakdown capability, higher frequency and the ability to operate in high temperature environments [151]. Although WBG semiconductor devices have already demonstrated rapid improvements in the performance of the SSCB, they have drawbacks including the high cost and low reliability, which resulted in the slow application of WBG devices into the mainstream power electronic market. The main challenges for WBG SSCB are accelerating cost reduction [161] and the development of the high-quality freestanding substrates, which are the important part of vertical device design [162]. In the future, the development of the WBG device will bring itself towards the maturity and it will be a hot topic of SSCB development [163] [164] [165] [166] [167].

As the semiconductor device is easily destroyed by overvoltage and overcurrent during the circuit fault, the method to protect the semiconductor device and reduce the leakage current is important in the future SSCB design [168]. To protect the semiconductor device, the additional diodes, resistors and capacitors are used to build the RC or RCD clamping circuit, which is used to limit the voltage across the semiconductor device during the fault. The RCD snubber circuit, which uses a fast recovery diode to clamp the changing voltage, is better than the capacitor snubber

and LC snubber circuit for medium-capacity applications, as there is no oscillation between C and L [169]. Furthermore, the MOV is also widely used to absorb the fault energy and clamp the voltage [170].

The topology is another important technology for future evolution of the SSCB design. The single SSCB with just one power semiconductor device is just suit for the low voltage and low power applications. To improve the voltage and current ability, multiple devices are series or parallel connected. Furthermore, more complex topologies are proposed to improve the performance, such as the Z-Source, which is the new generation of SSCB. The Z-Source SSCB has a simple control circuit and can automatically disconnect the fault load by using the capacitor to absorb the transient fault current. Furthermore, it can limit the fault current by the impedance of itself and be operated in bidirectional mode [171]. The diagram of the Z-Source SSCB is shown in Figure 2.19. When the circuit works normally, shown in Figure 2.19 (a), the current through the circuit is stable, which results in the inductor can replace the conduct line and the capacitor can be regarded as being open circuit. Therefore, the current flows through the inductor and the circuit is conducting. When the fault occurs, as shown in Figure 2.19 (b), the voltage across the load drops to zero and the capacitors paralleled with the load begin to discharge. As the direction of the capacitor current is opposite to the SCR conducting direction, the SCR will be disconnected naturally. Furthermore, the gate drive circuit of the SCR will remove the drive signal to ensure the isolation of the circuit from the fault source before the SCR voltage becomes negative. In Figure 2.19 (c), the current through two series LC circuits and the LC circuits begins resonating until the current through the inductors drops to zero. Finally in Figure 2.19 (d), the inductors releases the energy saved in process (c) by the RL circuits and the current will drop to zero when the energy is totally absorbed by the resistances [172].

The Hybrid circuit breaker is also a potential topology, which is composed by the SSCB and a mechanical switch. It overcomes the drawbacks of the SSCB and mechanical circuit breaker, and has advantages including low power loss, fast reaction speed, long service life, high reliability and simple structure. The simpler control system and high power density result in the hybrid circuit breaker becom-

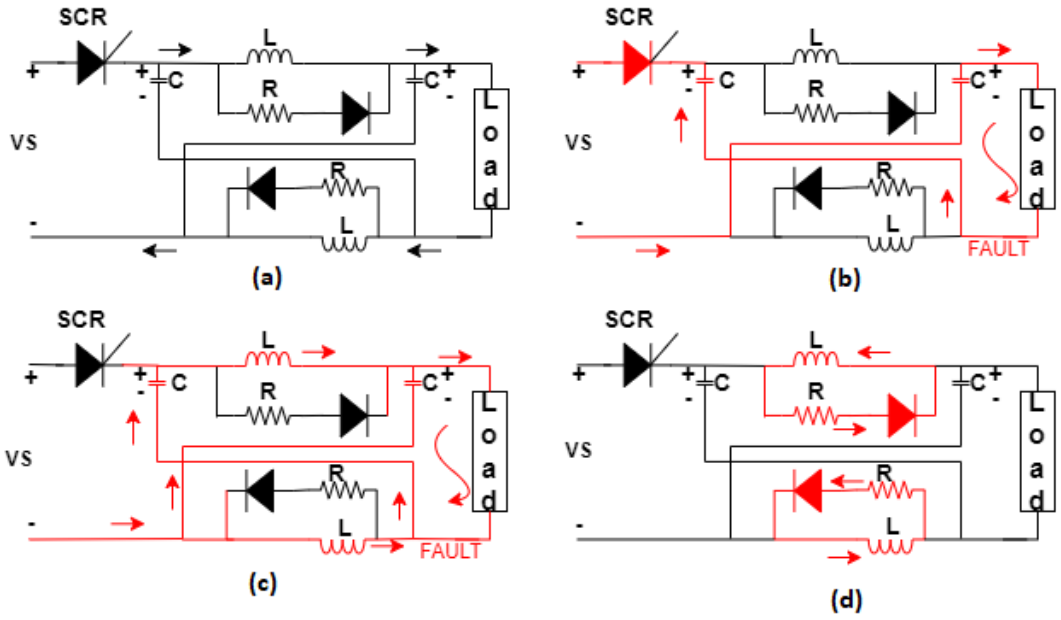

Figure 2.19: The diagram of the Z-Source SSCB

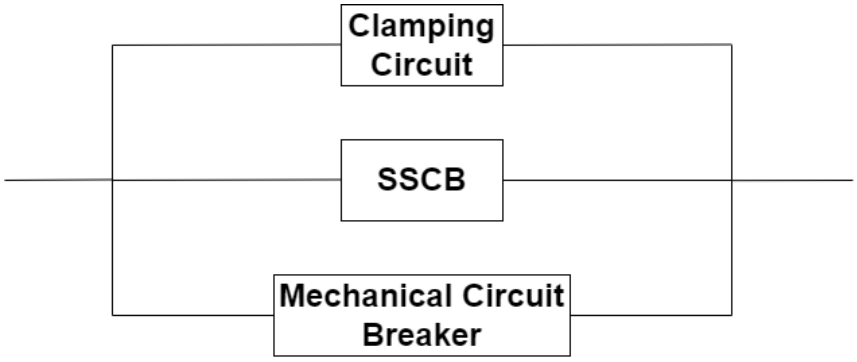

Figure 2.20: The diagram of the hybrid circuit breaker

ing a new research direction of the SSCB development [173]. The diagram of the hybrid circuit breaker is shown in Figure 2.20. When the circuit works in normal condition, the SSCB remains blocking and the current flows through the mechanical circuit breaker. Meanwhile, the clamping circuit maintains the high resistance state. When the fault occurs, the drive signal for the SSCB will turn on the SSCB and the contacts of the mechanical circuit breaker will be separated to shut down the mechanical circuit breaker. The arc voltage caused by the mechanical circuit breaker will rise until the rated voltage of the SSCB, during the turn on process of the SSCB and the main current will flow through the SSCB rather than the me-

chanical circuit breaker. The hybrid circuit breaker remains conducting. When the mechanical circuit breaker is fully blocked, the arc voltage disappears and the SSCB begins turning off. Because of the inductors in the circuit, the voltage across the SSCB rises sharply during the SSCB shut down process. When the voltage reaches the breakdown voltage of SSCB, the clamping circuit will limit the voltage value and transform to the low resistance state to conduct the current. The fault current will be absorbed by MOV in clamping circuit and drop to zero, as well as the hybrid circuit breaker finishes the blocking [174].

This Chapter introduced the research status and future challenges of the SSCB. SSCB can be widely used in low, medium and high power system protection circuit. To realise the zero carbon in the future, the development of renewable power system is significantly fast, which results in the more critical requirements in circuit protection circuit and more challenges for SSCB design. A number of technologies have been proposed to improve the performance of SSCB including the new semiconductor devices, new circuit topology and new digital and analog gate drive circuit for series connected switches. However, the improvement by using the drive signal, which is different with the pulse signal, is rarely mentioned. Therefore, this thesis proposed a novel drive signal to control the SSCB based on SiC MOSFET and compared the performance of the novel drive signal with the pulse signal in 270 V short circuit test. The novel drive signal is a new method to minimums the short circuit time of SiC MOSFET SSCB and the overcurrent flows through the main circuit during fault. Therefore, the weight and volume of the SSCB can be reduced by using the novel drive signal.

CHAPTER 3

MOSFET characteristics test

3.1 Introduction

In this Chapter, the short circuit characteristics of the SiC MOSFETs from the same family have been verified to obtain the fault reason of the MOSFET during the short circuit test. The MOSFET of the SSCB is used to determine the blocking and conducting behaviour of circuit, and protect the circuit from the short circuit fault. Therefore the short circuit withstand capability is the key character to be investigated, focusing on the maximum withstand short circuit time of the MOSFET. There are many situations that may result in the destruction of MOSFET during the short circuit fault, including the overvoltage and overcurrent, the junction overheating and the short circuit of the Gate [175] [176] [53]. The maximum safe operating range of the short circuit time for these failure modes are different, therefore, the maximum withstand short circuit time is determined by a combination of all reasons to ensure the reliable operation of the MOSFET.

Overvoltage and the overcurrent appear at the start of the short circuit event and may destroy the devices in circuit. These circuit characters can be measured by voltage and current probes. The maximum safe operating time of the circuit

can be determined according to the behaviour of the current and voltage. The condition of the Gate oxide is a critical characteristic to determine the reliability of the MOSFET and the threshold voltage is used to monitor any degradation arising from the overcurrent [177]. During the short circuit test, the oxide will be degraded by and can be observed by increases in the Gate-Source leakage current. This leads to the lifetime of oxide reducing and the threshold voltage will significantly increase [178] [179]. Once the oxide is damaged, the threshold voltage will permanently shift [177]. Therefore, the shift in the threshold voltage can be used to represent the condition of the Gate oxide. The safe operation time range for the Gate can be found from the relationship between the short circuit time and the threshold voltage shift, compared with a virgin device.

During the short circuit event, the large Drain-Source current causes the junction temperature to increase sharply and high junction temperature may also destroy the MOSFET. The junction temperature can be estimated by the thermal resistance from the datasheet and the power loss calculated from the short circuit test data. The thermal safe short circuit time can be subsequently determined from the data for the short circuit time and junction temperature.

After comparing the safe time of these three mechanisms, the shortest time is the maximum short circuit withstand time (T_{max}) of MOSFET in a system level application. To test these short circuit characteristic and measure the T_{max}, a test platform was developed. Normally, the short circuit test has two types, the Fault Under Load (FUL) test and the Hard Switching Fault (HSF) test [180]. The FUL test measures the characters of MOSFET, when the load has the short circuit, and the HSF measure the characters of MOSFET, when the MOSFET has the short circuit. This thesis focuses on the short circuit performance and action of SSCB when the load faults, therefore, the FUL test is selected for the test platform in this Chapter. Considering the MOSFET applied in SSCB is part of a half bridge topology, where the upper device and lower device could be the load for each, this Chapter will utilise the FUL test to represent the most likely fallure conditions of the half bridge. A FUL test platform was designed and used to generate the data in this Chapter. A range of commercial MOSFETs are evaluated for use in a SSCB

application in this Chapter and the device with the longest short circuit withstand time is selected for further evaluation.

3.2 Test platform

The first step to estimate the T_{max} of MOSFET is the creation of a validated test platform. The schematic diagram of the test platform is shown in Figure 3.1. The test platform circuit is composed of two capacitors, a silicon carbide power module and an under test MOSFET. A stable DC power source is used to provide 270 V DC-link voltage for the circuit which is an optimal option for future use in more electrical aircraft (MEA) or all electrical aircrift (AEA) [181]. The 270 V power system is also applied in solar Unmanned Aerial Vehicles (UAV) [182]. Therefore, the system will be designed and tested with aviation systems. L_{SC} is the parasitic inductance of the circuit, which from the internal inductance of devices in the circuit and the line inductance. C1 is a DC-link buffer capacitor. When the DC source is turned on, C1 will be charged first to reduce the high amplitude pulse voltage caused by high-voltage power supply start-up. C2 is a decoupling capacitor to maintain the DC voltage when the MOSFET and power module are conducting. To realise the FUL test, two controllable devices are required in the test platform to be the load and the device under test (DUT). The type of short circuit test is decided by the drive signals to the controllable device. A power module with a current handling capability that exceeds the DUT is used as the upper device, and the DUT is the MOSFET being evaluated. Because the power module has a lower on resistance than the MOSFET; during the FUL test, the majority of the DC voltage is applied across the MOSFET. Under the normal working condition, two device of the inverter will not conduct at the same time. When they conduct together, if the power module turns on first, the DUT has the HSF fault, otherwise, it has the FUL fault. However, the half bridge will have both types of fault during the short circuit. Therefore, the FUL short circuit characters of MOSFET have been selected to replace the state of the half bridge circuit in this thesis and the test platform will be used to test the FUL fault in this Chapter.

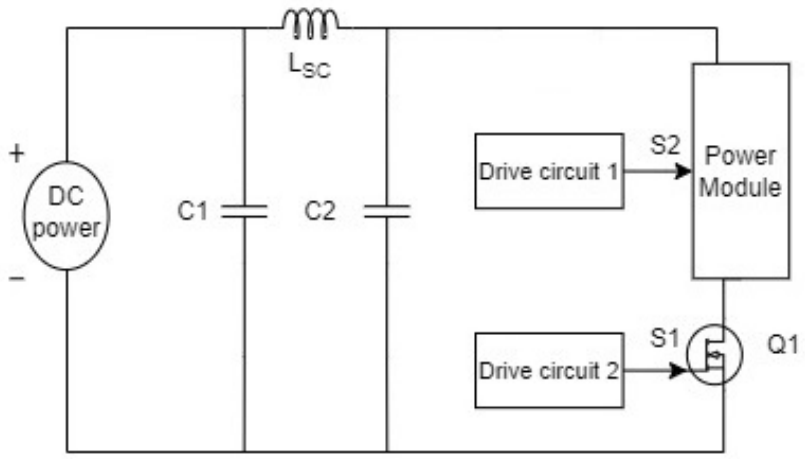

Figure 3.1: Test platform schematic diagram

The current through the circuit is expected to exceed 200 A during the short circuit test, with the total circuit resistance is approximately 1.5 Ohms. To facilitate the expected current, a copper bus bar is selected to replace the wire to connect the circuit. The value of capacitors is decided by the voltage of the DC power supply. In FUL test, the voltage of the DC power supply is blocked by both the MOSFET and the power module initially. MOSFET Q1 turns on first, and subsequently, the Drain Source voltage of Q1 drops rapidly and the voltage across the power module is equal to that of the capacitor C2, as the internal resistance of Q1 is far smaller than the resistance of the power module whilst in blocking. This voltage is the voltage of DC power supply and the lack of current flow in the circuit means that, the voltage induced across L_{SC} is zero. At the instant that power module turns on, the resistance reduces rapidly and current flows in the circuit. The current rises quickly resulting in a significant di/dt. The parasitic inductance, L_{SC} will induce an opposite electromotive force (EMF) to resist the increasing current and the voltage of C2 is now equal to the voltage of DC power supply minus the EMF of $L_{SC.}$ After the period of high di/dt, the voltage across the inductor decreases, the voltage of C2 will return to that of the DC power supply. Therefore, the voltage across the power module will observe a spike. This voltage spike may cause the damage to the devices and interfere with short circuit test result, especially in high voltage test. To reduce the spike, the capacitor C2 should be placed as close as possible to the DC

power supply to reduce the line inductance between these two devices. As C2 should supply the energy dissipated in the device and the energy stored in the inductance, the value of that could be estimated using equation 3.1 [183].

$$\Delta V_{\mathrm{DC}} = \frac{E_{\mathrm{loss}} + 0.5 L_{\mathrm{SC}} {I_{\mathrm{sat}}}^2}{C_2 V_{\mathrm{DC}}} \tag{3.1}$$

Where E_{loss} is the total energy loss during one short circuit test, and in this Chapter, 1 J is used as the maximum value, L_{SC} is the inductance in the test circuit which is around 1 µH [183], V_{DC} is the DC power supply voltage which is 270 V, I_{sat} is the saturation current of the MOSFET, Δ $\mathrm{V_{DC}}$ is the voltage drop at the time point when the short circuit test begins.

The $\mathrm{L_{SC}}$ is significantly small and has insignificant impact on Δ $\mathrm{V_{DC}}$. Therefore, to minimum the Δ $\mathrm{V_{DC}}$ two massive capacitors, C1 and C2, with the same capacitor value, which is 8000 µF are selected in this test. The Drain current and Drain Source voltage are measured using Tektronix TCPA 400 current probe with 750 A DC detection range, 50 MHz bandwidth and Tektronix THDP0200 voltage probe with 1200 V DC voltage detection range, 200 MHz bandwidth.

The MOSFETs used in this test are Infineon SiC MOSFETs from the same family with the different on resistance, including the 12M1H030, 12M1H045, 12M1H090. The information of these MOSFETs is shown in Table 3.1.

	12M1H030	12M1H045	12M1H090
$\mathrm{V_{DS}}$	1200 V	1200 V	1200 V
$\mathrm{I_D}$	56 A	47 A	26 A
$\mathrm{R_{on}}$	30 m/Ω	45 m/Ω	90 m/Ω
$\mathrm{V_{GS}}$	15-18 V	15-18 V	15-18 V
Total gate charge	63 nC	46 nC	21 nC

Table 3.1: The information of three MOSFETs

The drive signals for MOSFET and power module in FUL test are shown schematically in Figure 3.2, which are both square waves. Drive signal S1 is used to control the MOSFET and S2 is used to control the power module. Before time t0, both device are blocked and the DUT circuit has no current flow. The MOSFET turns on at time t0 and the power module turns on at time t1, which causes the FUL fault until the power module turns off at time t2. As the MOSFET is not an ideal

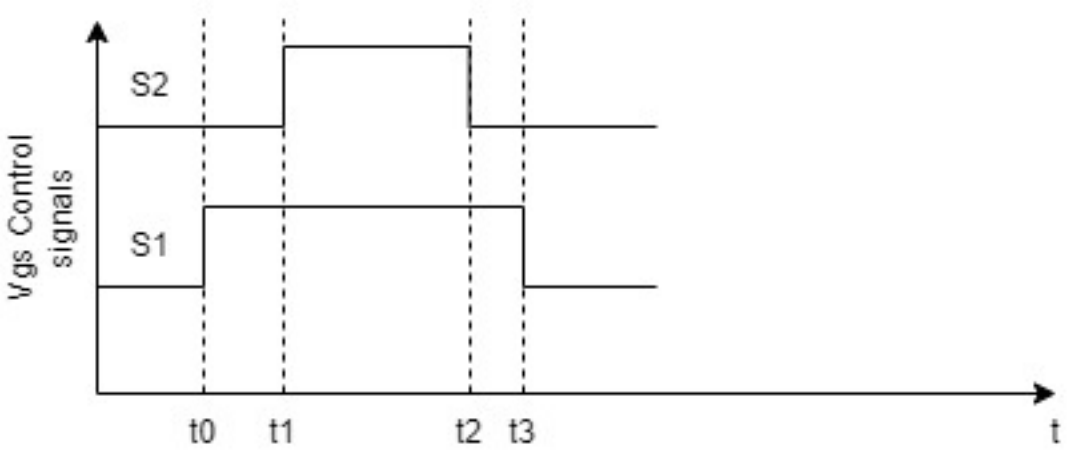

Figure 3.2: Control Signals S1 & S2 for FUL test

device, it takes several nanoseconds to fully turn on. Therefore, to ensure the FUL characteristics are only influenced by the condition of power module, time (t1-t0) should be sufficient to make sure the MOSFET is fully conducting before time t1. In this Chapter, time (t1-t0) is set as 1 µs, which is same as time (t3-t2), according to the 26 ns rising time and 30 ns fall time specified for the MOSFET [184]. The short circuit time is equal to (t2-t1) and controlled by the operation of the power module. This duration is increased to determine the MOSFET T_{max}. After power module turns off at time t2, the MOSFET shuts down at time t3. Furthermore, to collect the clear test result, the short circuit time (t2-t1) should longer than the response time of power module, which is 47 ns.

The drive signals are generated by a two channel synchronous pulse generator hp 8110A to ensure the synchronization of two drive signals. A gate drive circuit is used to generate the +24/-5 V levels to control the gates of the power devices. During the test, the MOSFET and power module are turned on every 10 seconds to ensure that the short circuit energy has been dissipated totally before the subsequent test.

In conclusion, a suitable test platform was constructed as described in this Chapter, and It will be used to test the short circuit characteristics of MOSFETs and obtain the fault reasons.

3.3 Result and analyse of the T_{max} of MOSFET

The target of this Chapter is to determine the T_{max} of different MOSFETs under FUL test conditions operating with a DC supply of 270 V. To find the T_{max} of the MOSFETs, three tests are performed using the test platform described previously, including the short current and voltage test, the Gate-Source threshold voltage test and the subsequent estimation of the junction temperature.

The short circuit current and Drain-Source voltage are used to directly show the state of the circuit and MOSFET. When the current or voltage change trend is different from the previous tests, the MOSFET can be considered to have failed, and the T_{max} of the devices is then determined from the test data. However, other reasons can result in the breakdown of MOSFET, and the T_{max} can be related to the characteristics of the short circuit current and voltage. The device thermal problems and the MOSFET Gate-Source breakdown must be considered. Although the internal resistance of MOSFET is typically around 80 mΩ in the on state, the overcurrent will cause a significant rise in the junction temperature and result in thermal failure of the MOSFET. Therefore, the short circuit time must be limited to reduce the rise of temperature and the maximum short circuit time, which could ensure the safe temperature of MOSFET, is the T_{max} defined by the thermal characteristics. Besides the overvoltage across the Drain-Source and overheating, the breakdown of the Gate is also a common reason for MOSFET failure. When the Gate of MOSFET suffers from overcurrent and overvoltage, the oxide layer will generally degrade, and the leakage current increases significantly, which will decrease the charge accumulated on the oxide layer and severely reduce the maximum electric field strength [185]. The insection of oxide charge in to the Gate capacitor causes the increase of the flatband voltage resulting in a noticeable short in the Gate-Source threshold voltage [186] When the overcurrent and overvoltage are over the maximum allowed value, the oxide layer will show evidence of breakdown, resulting in the MOSFET Gate-Source short circuit. Therefore, to ensure the safe operation of the MOSFET, the T_{max} of Gate-Source threshold voltage should be the maximum short circuit duration time that does not result in a significant shift. Furthermore, the T_{max} of the MOSFET is determined as the shortest of the three times described

above.

The short circuit current and the voltage of MOSFETs are tested first by the platform mentioned before. A 270 V DC power supply is selected to provide stable DC power. The short circuit test time is from 1 µs to 20 µs which approaches to the T_{max} of 1200 V SiC MOSFET driven by 24 V Gate-Source voltage [187]. A range of MOSFETs, including the 30 mΩ 12M1H030, the 45 mΩ 12M1045 and the 90 mΩ 12M1H090 were evaluated here to obtain the short circuit characteristics of the MOSFETs from the same family with different on resistance. The performance and test data for an Infineon 12M1H030 MOSFET, which has a rated blocking voltage 1200 V and 30 mΩ internal resistance, are shown in Figure 3.3 and Figure 3.4. The circuit characteristics T_{max} could also be determined from these two test results.

The data in Figure 3.3 show the Drain-Source current through the MOSFET during the FUL test. When the fault under load occurs, the fault current rises quickly from zero and reaches a peak, which is around 190 A, within 1 µs. During the turn off period, the current will drop to zero in a very short time, and it takes around 1.5 µs to release the energy. After the circuit dissipates the short circuit energy, the current through circuit will remain at zero. Two spikes appear in the data at the beginning of the circuit short and the end of the circuit short respectively. When the short circuit occurs, the V_{DS} of the MOSFET rises quickly, and dv/dt is approximately 270×10^6 V/s as shown by the data in Figure 3.4. This increase in the Drain-Source voltage results in the charging current for the internal capacitors of MOSFET and generates the 230 A current peak at the beginning of the test. When the power module is turned off, the V_{DS} of the MOSFET decreases sharply with a similar dv/dt to the rise at time 0.

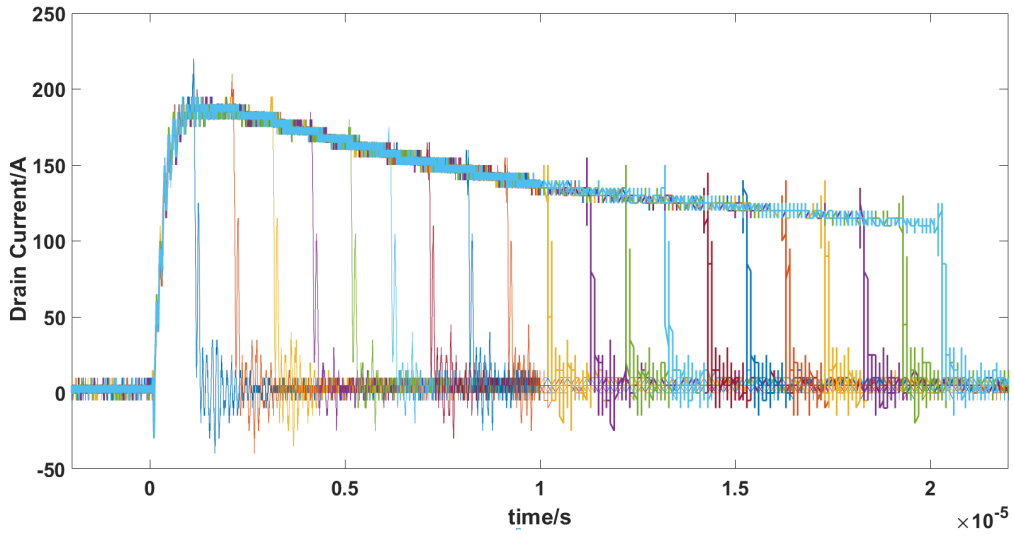

Figure 3.3: Drain current of 30mΩ MOSFET

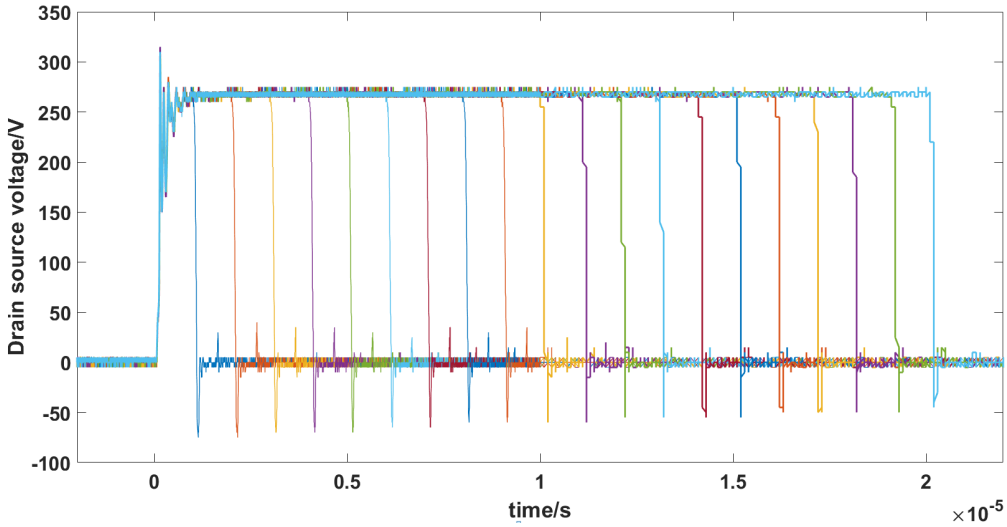

Figure 3.4: Drain-Source voltage across the 30mΩ MOSFET

At the conclusion of the FUL test, the internal capacitance of the MOSFET discharge and resulting in the current spike when the MOSFET begins to shut down, which is around 40 A. When the current drop to zero, the overcurrent during fault results in the oscillation which has around 50 A peak-to-peak value. With the increase of the short circuit time, the current presents a rapid rise and a gentle decline after reaching the peak. The high short current through the internal resistance of MOSFET resulting in an increase in the junction temperature. The higher temperature leads to a lower electron mobility and a higher internal resistance [177], and this results in the current through the MOSFET decreasing with time. The rate

of change of the Drain current decreases after 10 µs, because the rate of junction temperature increase slows, which causes the slope of the on resistance to decrease. As the Drain-source voltage is clamped at 270 V, the slope of the current follows that of the device resistance. The result shows that the short circuit time has a great impact on the Drain current and the on resistance of MOSFET.

The data in Figure 3.4 show the Drain-Source voltage across the MOSFET during the FUL test. When the fault occurs, the voltage across MOSFET rises rapidly and it stabilizes at 270 V. The oscillations observed in the waveform arise from the inductance in the circuit. At beginning of the test, the current through the circuit rises quickly, according to the Figure 3.3, and the high slope of the current speed causes the EMF across the inductance and the spike of the voltage reaches 320 V. With the short current reaches the peak, the slope of current decreases gradually and the EMF of inductance returns to zero which results in the voltage across MOSFET becommming stable at 270 V. When the circuit is operating in the blocking condition, the voltage drops to zero quickly and the current falls simultaneously. The EMF of the parasitic inductance has an opposite direction and results in a 70 V voltage spike at the conclusion of the 1 µs test. The spike at the end of test decreases with the increase in the short circuit test time, due to the decrease in Drain current as can be seen from the data in Figure 3.3. This decreases the di/dt during the turn off period, and hence a lower EMF due to the inductance.

The waveforms for the device during the short circuit test can be used to determine the state of circuit in the FUL test, but cannot show the internal state of the MOSFET. During the short circuit fault, the reliability of the MOSFET gate structure may permanently decrease because of the oxide degradation [177]. With the increase in the short circuit time, the current may destroy the internal structure of MOSFET first. When the internal parameter changes of the MOSFET degrades so that they fall outside the normal value range, it will be reflected in the current-voltage characteristics of the circuit. Therefore, before the current and voltage change, the MOSFET may already begin to show evidence of degradation. To ensure the safety of circuit and assess the degradation of the MOSFET, it is necessary to measure the internal parameters of the MOSFET after each short circuit test and get the T_{max} of MOSFET internal characteristics.

The Gate-Source threshold voltage (V_{th}) and the flatband voltage (V_{FB}) are selected to describe the internal condition of MOSFET as the gate oxide is often damaged during extreme operation conditions and resulting in a Gate-Source short fault during the test. The threshold voltage is defined as:

$$V_{\mathrm{th}} = V_{\mathrm{FB}} + 2\phi_{\mathrm{F}} + \frac{\sqrt{2qK_{\mathrm{s}}\varepsilon_0 N_{\mathrm{A}}(2\phi_{\mathrm{F}})}}{C_{\mathrm{OX}}} \tag{3.1}$$

Where V_{th} is the threshold voltage, V_{FB} the flatband voltage, C_{OX} the gate oxide capacitance, ϕ_F the Fermi potential, N_A the acceptor doping density, K_s the semiconductor dielectric constant, q the magnitude of electron charge, which is 1.6×10^{-19} C, and ε_0 the permittivity of free space, which is 8.8554×10^{-14} F/cm.

Threshold voltage is influenced by many factors, including the gate oxide capacitance (C_{OX}), the Fermi potential, flatband voltage, semiconductor dielectric constant and acceptor doping density according to equation 3.1. Among these factors, the Fermi potential is determined by the doping concentration of the polysilicon gate during production [188]; the acceptor doping density and semiconductor dielectric constant are determined by manufacturing processes and material; C_{OX} is decided by permittivity of oxide and physical oxide thickness [189]. These factors are generally not impacted by short circuit current, while the V_{FB} is greatly affected. Therefore, the flatband voltage becomes the main factor affecting the threshold voltage in short

circuit conduction and it is possible to monitor the condition of the gate oxide and test the T_{max} of the MOSFET Gate by examining the shift of V_{th}.

As the V_{FB} is the main factor which influences the threshold voltage and it is greatly impacted by the short circuit current, the shift in V_{FB} can be used to represent the gate oxide condition and verify the origin of the V_{th} shift. The V_{FB} is defined as [186]:

$$V_{FB} = \phi_{MS} - \frac{Q_F + Q_M + Q_{OT}}{C_{OX}} \tag{3.2}$$

Where the V_{FB} is the flatband voltage, ϕ_{MS} the metal-semiconductor work function difference, Q_{OT} the oxide trapped charge, Q_F the fixed charged and Q_M the mobile charge.

ϕ_{MS} depends on the metal and semiconductor material used in MOSFET and it has been decided during the manufacture but not influenced by the short circuit test [190]. Therefore, ϕ_{MS} is a constant value in the short circuit test. Q_{OT} is the oxide trapped charge and it contributes little to the flatband voltage or the threshold voltage shift during the short circuit test for a MOSFET with thin oxide layer [186]. As the 1200 V SiC MOSFET normally has a thin oxide thickness, which reaches 25nm in a 6 inch foundry [191], the impact of trapped charge on the reliability of gate structure could be ignored. Q_M is primarily decided by the ionic impurities in SiO_2 which is fixed during the manufacture [186]. Therefore, these three factors have little impact on the flatband voltage shift during the short circuit test. Q_F is determined by the flatband voltage shift, which is measured by comparing the voltage shift between the experimental virgin device C-V curve and the theoretical curve [186]. Normally, Q_F remains stable in normal working condition. However, too long short circuit time may break the gate oxide and permanently change the fixed charge and influence the flatband voltage further. Therefore, the flatband voltage can be used to describe the condition of the gate oxide, and according to equation 3.2, the result of flatband voltage shift can be correlated with the threshold voltage shift.

In this section, the threshold voltage is extracted using the linear region method based on the $\sqrt{I_{DS}}$-V_{GS} data [192] and the flatband voltage is measured according

to the C-V test curve [193]. A Keithley 4200A-SCS parameter analyser is used to test the current-voltage characteristics and the capacitor-voltage characteristics of the MOSFET after each short circuit test

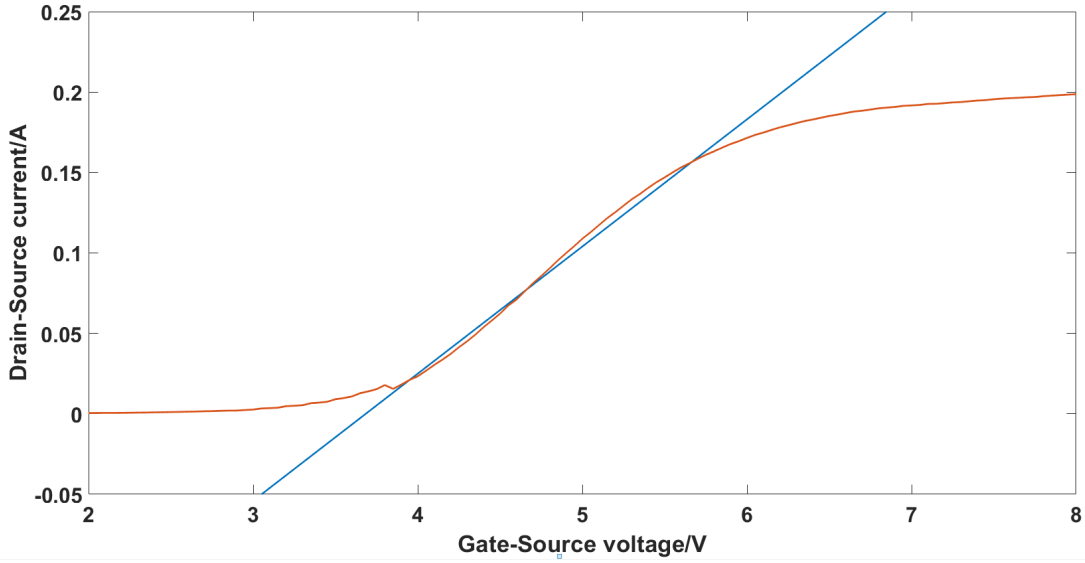

Figure 3.5: I-V test of 30mΩ MOSFET

The experimental $\sqrt{I_{DS}}$-V_{GS} data are shown in Figure 3.5. The data show the relationship between V_{GS} and the Drain current through the MOSFET. The red curve is the I-V character of the MOSFET and the blue line is the linear regression line which is used to determine V_{th}. When the V_{GS} is below the threshold, the MOSFET operates in the cut-off region and is blocking. The low Gate-Source voltage cannot form a sufficient electric field to form the channel. When the V_{GS} is greater than the threshold voltage, the Drain current through the MOSFET depends on the Drain-Source voltage. If V_{DS} is smaller than (V_{GS}-V_{th}), the MOSFET works in the linear region. In this region, when V_{GS} is constant, the increase of the V_{DS}, result in a linear increase of the Drain current in the circuit. If $V_{(DS)}$ is larger than (V_{GS}-V_{th}), the MOSFET operates in the saturated region. In this region, the Drain current shows a minor variation with V_{DS} for constant V_{GS}. In this operation condition, the Drain current is only a function of V_{GS}. According to the I-V characteristics of the MOSFET, the pitch off voltage is the boundary of the cut-off and linear regions, and it should meet the characteristics of two working states at the same time, which is no current and linear growth. The best method to

find the threshold voltage is finding the intersection point of a linear regression fit to the $\sqrt{I_{\mathrm{DS}}}$ data. The threshold voltage is the abscissa of intersection point of the blue line and zero current axis. The variation in the threshold voltage of 12M1H030 under the short circuit time from 1µs to 20 µs is shown by the data in Figure 3.6.

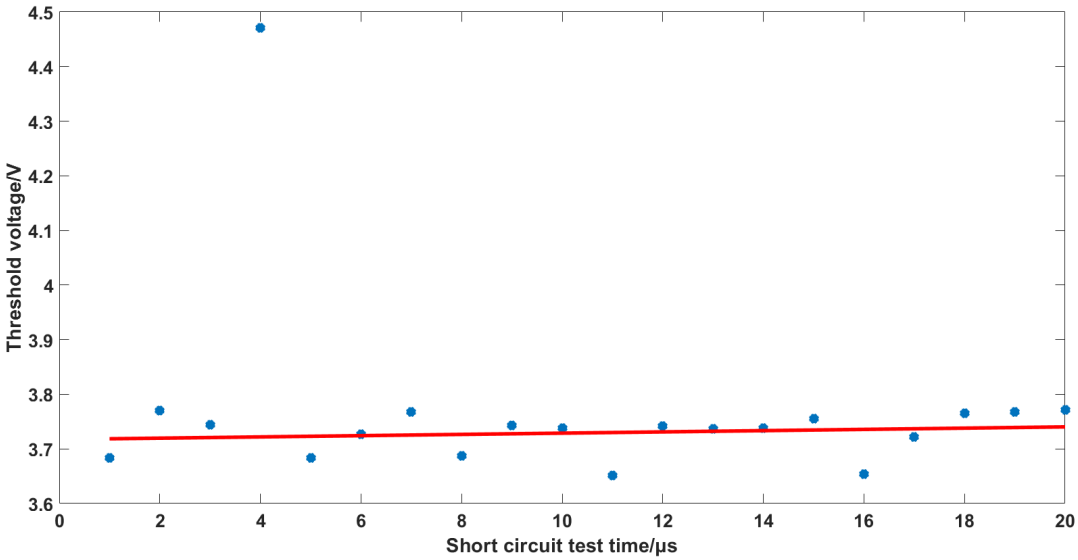

Figure 3.6: Threshold voltage of 12M1H030

The short circuit test time is varied between 1 µs and 20 µs, and the extracted threshold voltages are shown by the data in Figure 3.6. The red line is the linear fit line for threshold voltage data points and the masority of the threshold voltages are in the range between 3.6 V to 3.8 V, except the 4 µs threshold voltage, which is 4.48 V. According to the datasheet [184], the normal range of the threshold voltage is from 3.5 V to 5.7 V and there is no test data out of the normal range. Therefore, the threshold voltage does not show a permanent change after FUL tests, indicating that there is no significant damage to the Gate of the 12M1H030 transistor during the 20 µs short circuit test. However, the threshold at 4 µs has a significant difference with other data. It presented and thus has been considered as an anomalous point and must be considered further. The relationship between threshold voltage and Drain current is shown by the follow equation 3.3:

$$I_{\mathrm{DS}} = \frac{\mu \times W \times C_{\mathrm{OX}} \times (V_{\mathrm{GS}} - V_{\mathrm{th}})^2}{2 \times L} \tag{3.3}$$

Where μ is the electron mobility, W the gate wide, L the gate length, C_{OX} the Capacitance per unit area, V_{GS} the Gate-Source drive voltage, and V_{th} the threshold voltage.

According to the equation 3.3, when the threshold voltage has a positive shift, $\mathrm{I_{DS}}$ will decrease. Therefore, a significant shift in the threshold voltage will also be evident in the Drain current characteristics. If the Drain current characteristics show the degradation in comparison to those of a virgin device, the threshold voltage has permanently increased and there may be corresponding damage to the Gate of the MOSFET. According to the data in Figure 3.3, the Drain current of 4 µs pulse data follows the tracks of of the other tests, which indicates that threshold voltage has not shifted significantly and hence there is no damage to the Gate of the 12M1H030 as a result of the 4 µs short circuit test.

The C-V test results are used to extract the flatband voltage of the MOS capacitor that forms the gate of the MOSFET. As described earlier, the oxide trapped charge contributes little to the flatband voltage shift for MOSFETs containing a thin oxide [186] the C-V data focuses on the change in fixed and mobile charge, according to equation 3.2. The mobile charge shift is determined according to the conductance and voltage curve shown in Figure 3.7. The true flatband voltage value is between the two peaks in the conductance data and shown by a red dotted line. The flatband voltage during the charging and discharging, which is the value of the abscissa corresponding to the peak value of the conductance curve, is shown by two solid red lines. When the Gate voltage increases, the mobile charge shows a positive shift in comparison to the stable state resulting in a positive shift in $\mathrm{V_{FB}}$. When the Gate voltage decreases, the mobile charge will decrease and there is a corresponding negative shift $\mathrm{V_{FB}}$. Generally, the value of positive shift in $\mathrm{V_{FB}}$ is same as that of the corresponding negative shift $\mathrm{V_{FB}}$, therefore, to simplify the calculation, the mobile flatband voltage is the half of the sum of the absolute values of positive shift $\mathrm{V_{FB}}$ and negative shift $\mathrm{V_{FB}}$.

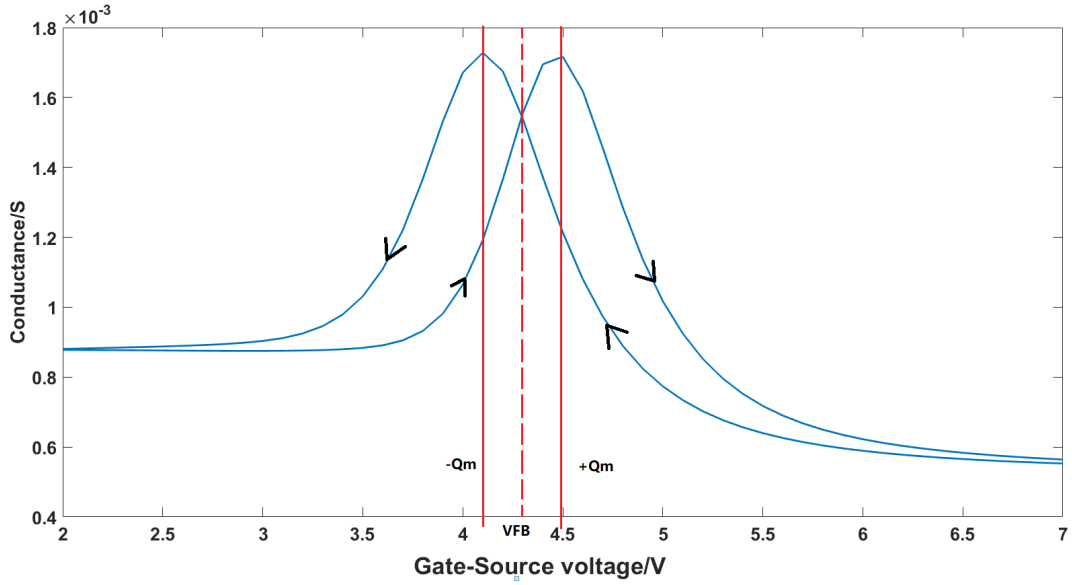

Figure 3.7: Conductance and voltage curve

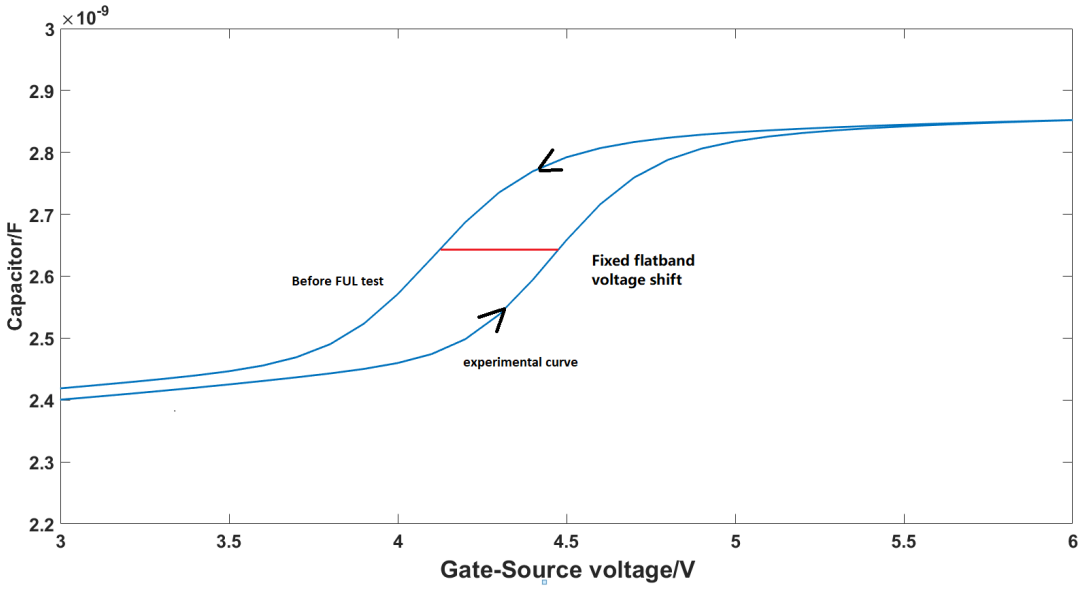

Figure 3.8: Capacitor and voltage curve

The fixed charge shift is estimated according to the capacitance-voltage curve which is shown in Figure 3.8. Following a method similar to that used with the conductance in Figure 3.7, the curve of the capacitor has charging process and discharging process. The charging process is the experimental curve. During this process, the V_{FB} is influenced by the fixed charge and $V_{FB} = \phi_{MS}$ - Q_F/C_{OX} considering the impact of fixed charge. The discharging process makes the condition of device return to the condition before the FUL test. Therefore, the $V_{FB} = \phi_{MS}$ during the discharging process. The difference of the flatband voltage between the two processes $\Delta V_{FB} = Q_F/C_{OX}$. As C_{OX} is a constant value, ΔV_{FB} is influenced by the fixed charge. Therefore, for a same capacitor value, the corresponding voltages between the charging process and discharging process are different, and the value of the difference in linear range is the fixed flatband voltage shift, which is shown by red line.

C-V test is applied after each short circuit test and the mobile flatband voltage result of 12M1H030 MOSFET, after the short circuit time from 1 µs to 20 µs, is shown in Figure 3.9. The range of the mobile flatband voltage shift is from 0.1 V to 0.2 V and the average value is 0.15 V which could be regarded as the flatband voltage shift under normal working conditions. The fluctuation of the mobile flatband voltage is ± 50 mV. The fixed flatband voltage result is shown in Figure 3.10. The range of the fixed flatband voltage is from 0.37 V to 0.4 V. The difference is very small and so the fixed flatband voltage remains stable during the test. The MOSFET tested in the this Chapter is the brand new device and after the first time conducting, the resistance increases insignificantly which results in the insignificant decrease of the flatband voltage [194]. Therefore the flatband voltage shows in Figure 3.9 and Figure 3.10 has the insignificantly decrease during the short circuit time between 1 µs to 3 µs. As the mobile flatband voltage does not have a permanent change and the fixed flatband voltage is stable, the gate oxide of 12M1H030 shows no damage during the test. Combining the results of flatband voltage and threshold voltage, it can be concluded that the maximum short circuit threshold withstand time of 12M1H030 exceeds 20 µs, and the maximum gate character withstand time of other MOSFETs will also be tested by the methods

mentioned above.

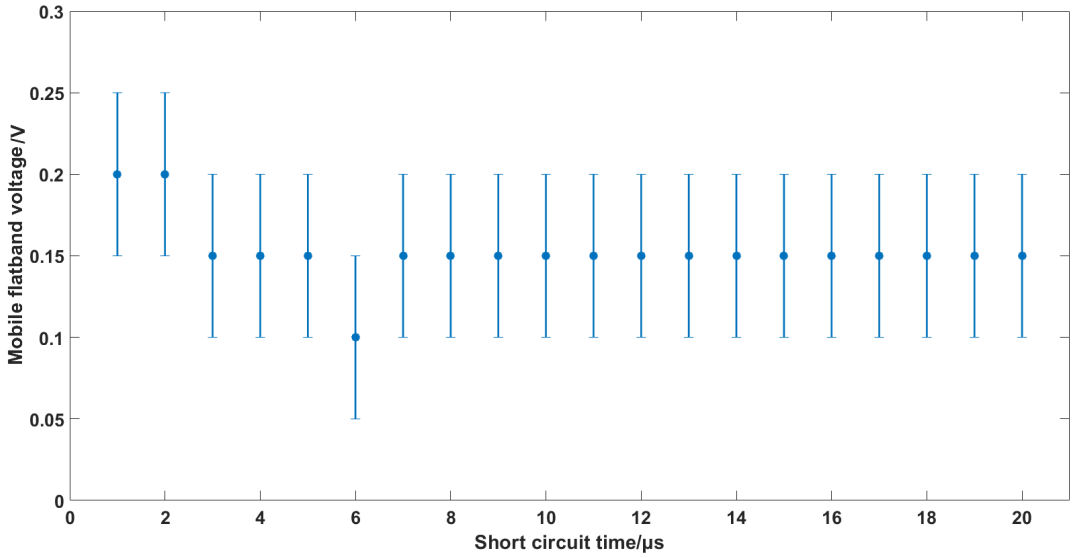

Figure 3.9: Mobile flatband voltage shift

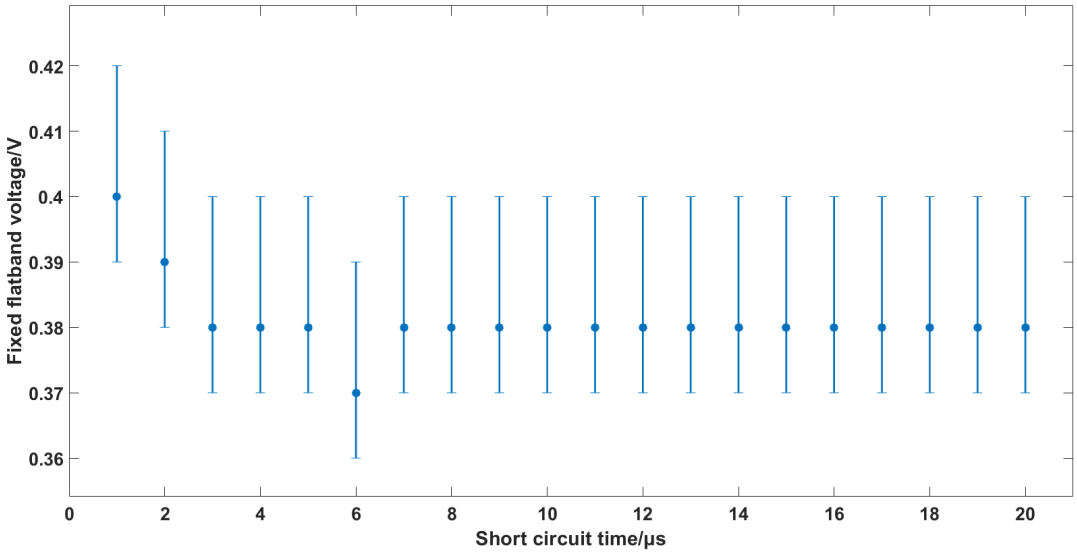

Figure 3.10: Fixed flatband voltage shift

The junction temperature is also an important parameter which must be considered in short circuit application to avoid thermal damage to the MOSFET. As it is not possible to directly measure the junction temperature. Equation 3.4 is used to estimate that:

$$R_{\mathrm{T(j\text{-}c)}} = \frac{T_{\mathrm{j}} - T_{\mathrm{c}}}{P} \tag{3.4}$$

Where $R_{T(j\text{-}c)}$ is the thermal resistance of junction-case, which can be determined from the datasheet [184], T_j the junction temperature of the MOSFET, T_c the case temperature, and P is the average power loss of the MOSFET during the test.

However, equation 3.4 is not suitable to be used in this study to estimate the junction temperature because the equation is used under steady-state conditions and does not reflect the rapid changes in device temperature experienced during a short circuit event [195]. When a MOSFET is operating normally, the heat generated by the current flowing through the MOSFET has sufficient time to dissipate from the junction to the case and the rise in temperature of the case which can be measured during operation. Meanwhile, the dissipated power remains stable, and the junction temperature can be estimated using the steady state experssion in equation 3.4. In contrast to the normal operating conditions, the short circuit condition is a rapid transient. The short circuit results in significant overcurrent and overvoltage conditions, which result in the huge transient power. However, as the short circuit time is limited to a number of microseconds, the total energy loss caused by transient power is very low, and is typically a fraction of a Joule. The low energy loss and the short fault time does not allow the heat to dissipate from junction to the case and cause the case temperature rise. Therefore, the case temperature in short circuit state was not measured and equation 3.4 is not suitable for the short circuit testing reported here.

The temperature dependence of the mobility for 4H-SiC at low doping concentrations, expressed in equation 3.5, is used to estimate the junction temperature during the short circuit test [196]. The equation is suitable for unipolar silicon carbide devices with n-type drift regions [197]:

$$\mu_{\mathrm{n(4H\text{-}SiC)}} = \mu_{\mathrm{n(300)}} \times \left(\frac{T}{300}\right)^{-2.7} \tag{3.5}$$

$\mu_{n(4H\text{-}SiC)}$ is the electron mobility of 4H-SiC at temperature T, $\mu_{n(300)}$ the electron mobility of 4H-SiC at 300K, and T the junction temperature. The relationship between the electron mobility and the conductivity is shown by equation 3.6:

$$\sigma = n \times q \times \mu_{\mathrm{n(4H\text{-}SiC)}} \tag{3.6}$$

Where σ is the conductivity, q the carrier charge, and n the carrier concentration.

Combining equations 3.5 and 3.6, the relationship between the junction temperature and conductivity is shown as:

$$\sigma_{(\mathrm{T})} = \sigma_{(300)} \times \frac{n_{(\mathrm{T})} \times q_{(\mathrm{T})}}{n_{(300)} \times q_{(300)}} \times \left(\frac{T}{300}\right)^{-2.7} \tag{3.7}$$

and so the resistance of the MOSFET can be expressed as:

$$R_{\mathrm{on(T)}} = R_{\mathrm{on(300)}} \times \frac{n_{(\mathrm{T})} \times q_{(\mathrm{T})}}{n_{(300)} \times q_{(300)}} \times \left(\frac{T}{300}\right)^{2.7} \tag{3.8}$$

$R_{on(T)}$ is the on resistance of MOSFET at temperature T, $R_{on(300)}$ the on resistance of MOSFET at 300K.

With the increase of the short circuit test time, the junction temperature rises significantly due to the significant overcurrent. However, the junction temperature mainly affects the channel, and the carrier concentration depends on the ionisation of the dopant in the drift region [198]. This fraction is close to 100% at room temperature and so $n_{(300)}$ can be considered to be the same as $n_{(T)}$ and so $\frac{n_{(\mathrm{T})} \times q_{(\mathrm{T})}}{n_{(300)} \times q_{(300)}}$ is approximately equal to one [199]. To simplify the following calculations, $\frac{n_{(\mathrm{T})} \times q_{(\mathrm{T})}}{n_{(300)} \times q_{(300)}}$ is set as one in this Chapter. Hence the simplified equation for the resistance is shown follow:

$$R_{\mathrm{on(T)}} = R_{\mathrm{on(300)}} \times \left(\frac{T}{300}\right)^{2.7} \tag{3.9}$$

The total on state resistance of the MOSFET consists of a number of resistances, including the channel resistance, the drift resistance, the source contact resistance,

the Source resistance, the accumulation resistance, the substrate resistance and the Drain contact resistance [197]. Among these resistances, the channel resistance and the drift resistance occupy the largest proportion, and the increase of the junction temperature mainly influence the value of channel resistance. Therefore, using the channel resistance allows a more accurate estimate of the junction temperature [200] [201]. The equation 3.9 could be changed to:

$$R_{\text{on-channel(T)}} = R_{\text{on-channel(300)}} \times \left(\frac{T}{300}\right)^{2.7} \tag{3.10}$$

Calculating the $R_{on\text{-}channel(300)}$ is the first step to estimate the junction temperature by equation 3.10, and the method is described below.

Resistance	Value (mΩ-cm^2)	Percentage Contribution
Source Contact	0.05	8.2
Source	0.0005	0.0
Channel	0.229	37.4
Accumulation	0.055	9.0
Drift	0.209	34.1
Substrate	0.06	9.8
Drain Contact	0.01	1.6
Total	0.613	100

Table 3.2: On resistance components

During the short circuit test, the junction temperature rises and cause the on resistance of MOSFET to increase [202]. Therefore $R_{on(300)}$ should be the minimum resistance and appears at the beginning of the test. Transforming the $R_{on(300)}$ to the current by Ohm's law, $I_{(300)}$ is the largest current that occurs at the beginning of the test. However, according to the data in Figure 3.11, the maximum current does not appear at the beginning of the test as there is a process of current rising during turn-on, during which the junction temperature rises significantly. To find the $R_{on(300)}$, a current waveform is extrapolated to the time where the short circuit transient occurs and so $I_{(300)}$ is the value of the current at t=0. After that, the $R_{on(300)}$ could be calculated by Ohm's law. The $R_{on\text{-}channel(300)}$ is a part of the $R_{on(300)}$, and the on resistance components under 300 K is shown in Table 3.2 [197].

The data in Table 3.2 show the On-state-resistance components within the 50-V power U-MOSFET structure with 5 µm cell pitch. As the resistance of MOSFET

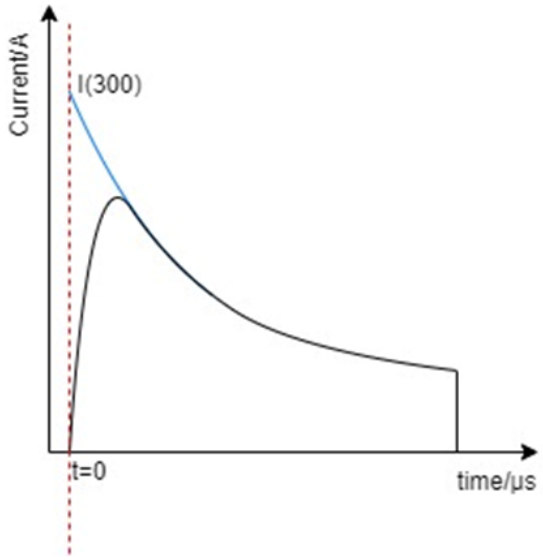

Figure 3.11: $R_{\text{on-channel(300)}}$ estimation method

is proportional to the square of the rated blocking voltage [203] [204], the total resistance of 1200 V MOSFET, which is used in this Chapter is much larger than that of the 50 V MOSFET, but the contributions from each of seven components are similar. Meanwhile, the manufacturing process of the 1200 V MOSFET used in this Chapter makes the cell pitch of that close to 5 μm. Therefore, the percentage contribution of on resistance in Table 3.2 could be used to estimate the on-channel resistance of 1200 V MOSFET. Furthermore, the data for 1200 V MOSFET is hard to find and the percentage contribution of 50 V MOSFET is used in this section. According to the Table 3.2, the $R_{on\text{-}channel(300)}$ could be calculated by equation 3.11, and the rest resistance $R_{on\text{-}rest(300)}$ could be calculated by equation 3.12.

$$R_{\text{on-channel(300)}} = R_{\text{on(300)}} \times 37.4\% \tag{3.11}$$

$$\begin{aligned} R_{\text{on-rest(300)}} &= R_{\text{on(300)}} - R_{\text{on-channel(300)}} \\ R_{\text{on-rest(T)}} &= R_{\text{on(T)}} - R_{\text{on-channel(T)}} \end{aligned} \tag{3.12}$$

As the channel resistance takes a large percentage of the on resistance and greatly affected by junction temperature rise, the change of the estimation on resistance is all

attributed to the change of the channel resistance and the remainder of the resistance described as $R_{on\text{-}rest(300)}$ in this Chapter. In fact, the change of the on resistance is attributed to both change of channel resistance and remainder resistance. Hence, by this method, the true change of the channel resistance is smaller than the change of the channel resistance used in estimation. In addition, because the time of short circuit test is very short and the temperature has no time to transform to case, the temperature rising just occurs in channel, and the change of channel resistance is all contributed by the junction temperature rising. Therefore, the true junction temperature rising is smaller than the estimated junction temperature rising, which ensures when the estimated junction temperature is smaller than the maximum junction temperature, the true junction temperature is smaller than the maximum junction temperature. This estimation gives more margin to ensure the safety of MOSFET during the short circuit fault.

The on resistance $R_{on(T)}$ could be calculated according to the Drain current and $V_{(DS)}$ data form Figure 3.3 and Figure 3.4. As the $R_{on\text{-}rest(T)}$ is a constant value, the $R_{on\text{-}channel(T)}$ could be calculated by equation 3.12. After calculating the $R_{on\text{-}channel(300)}$ and $R_{on\text{-}channel(T)}$, the junction temperature at each time point could be estimated by equation 3.10. As an example, the estimated junction temperature of 12M1H030 during the FUL short circuit test is shown in Figure 3.12. The results are calculated according to the experiment data.

Figure 3.12(a) shows the short circuit current of MOSFET at the time points from 1 μs to 20 μs. A quadratic rational fitting curve is produced according to the current data point to estimate $I_{(300)}$ of 12M1H030, which is 200 A, at time = 0, which is the beginning of the short circuit condition. The DC power supply of the test is 270 V and the on resistance $R_{on(300)}$ could be calculated by Ohm's law, which is 1.35 Ω. According to the equation 3.11 and 3.12, the $R_{on\text{-}channel(300)}$ is 0.5 Ω and $R_{on\text{-}rest}$ is 0.85 Ω. Furthermore, the on resistance under different short circuit time $R_{on(T)}$ can be calculated by the same method according to the voltage and current data at each short circuit time point, and the results are shown in Figure 3.12(b). After the calculation of the constant value $R_{on\text{-}rest}$ and $R_{on(T)}$, the on channel resistance at each short circuit time $R_{on\text{-}channel(T)}$ can be calculated according to equation 3.12 and

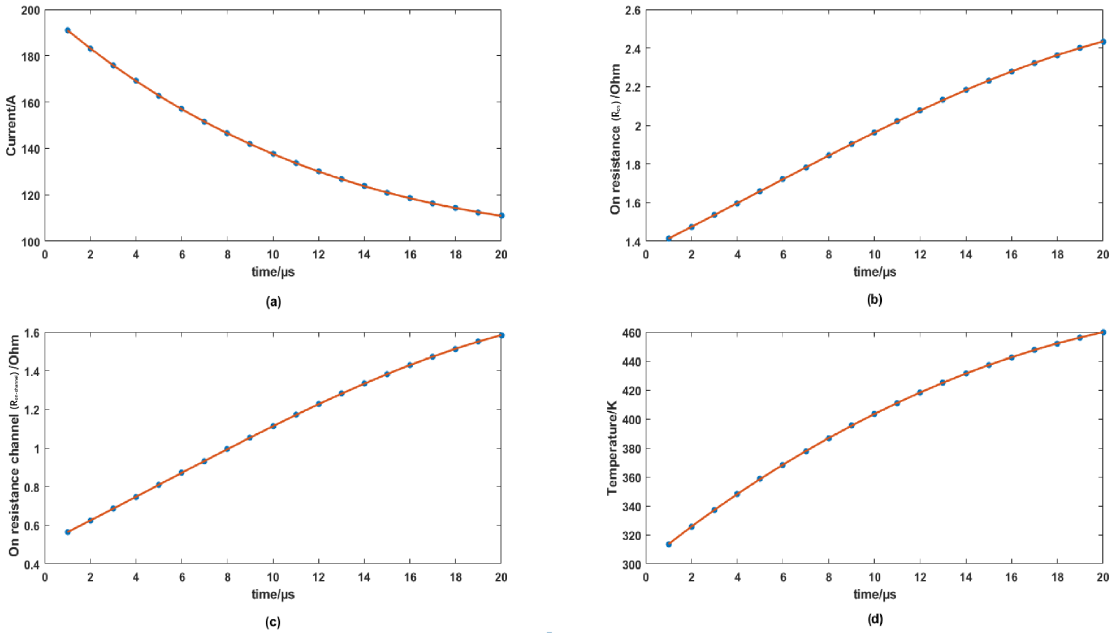

Figure 3.12: (a) Drain source current of 12M1H030, (b) total on resistance of 12M1H030, (c) Channel on resistance of 12M1H030, (d) Junction temperature of 12M1H030

the results are shown in Figure 3.12(c). The calculation of the junction temperature at each short circuit time is based on the $R_{on\text{-}channel(T)}$ and $R_{on\text{-}channel(300)}$, according to equation 3.10, and the results are shown in Figure 3.12(d).

The maximum junction temperature, that could be experienced by the 12M1H030 MOSFET is 448.15 K [184], which is close to the estimated junction temperature at 17 μs, according to the calculated results in Figure 3.12(d). To ensure the safety of MOSFET, the thermal T_{max} of 12M1H030 is considered to be 16 μs. In this Chapter, besides 12M1H030, the thermal T_{max} of other MOSFETs from the same family will also be estimated by the method mentioned above and the results will be shown later.

To estimate the T_{max} of MOSFET, a series of MOSFETs were evaluated by the methods mentioned above from three aspects, including the circuit characters, the Gate state and the thermal performance. These MOSFETs have the same rated V_{DS}, similar fall time which influences the shut down speed in SSCB applications and package, but are designed for different applications. For example, the 12M1H090 has a small Gate charge, 21 nC, which makes it suitable for the applications that require fast switching speed. Meanwhile, the 12M1H030 has the high rated I_D, which

is 56 A, and is suitable for the high power applications. The key internal parameters of the different tested MOSFETs are shown in Table 3.3.

The test has three steps. The first step is testing the circuit characters by the test platform. The short current and short voltage data are collected and the maximum circuit character withstand time determined by comparing the current and voltage characteristics during the short circuit event. Once the trend of current or voltage is different from the previous experimental results, the MOSFET may be broken and the maximum circuit character withstand time will be the time of last short circuit test. The second step is confirming the condition of the gate using I-V and C-V characteristics, and it could be represented by shifts in the threshold and flatband voltages. Once the threshold voltage and flatband voltage show permanent changes or the internal capacitors of MOSFET could not be charged anymore, the gate oxide of MOSFET is broken and the gate character withstand time will be the time of last short circuit test. Finally, the thermal performance is evaluated. The junction temperature is estimated from the on-state-resistance of MOSFET and the thermal withstand time will be the maximum time the junction temperature remains within a safe range.

After comparing the result of the three withstand times, the shortest one will be identified as the T_{max} of the MOSFET. In this section, the performance of 12M1H030, with 30mΩ resistance, is selected as an example to introduce the methods. Besides it, the performance of 12M1045 and 12M1H090 are also tested in this section to compare the short circuit characteristics of them. The test results are shown in Table 3.3 [205] [184] [206].

According to the Table 3.3, the circuit character withstand time and Gate character withstand time of 12M1H030 and 12M1045 are same, which are both 20 µs. They are longer than them of 12M1H090 and the performance of 12M1H030 and 12M1045 is better than 12M1H090. The thermal withstand time of 12M1H030 and 12M1045 is less than the circuit character withstand time and the Gate withstand time of them separately, while the thermal withstand time of 12M1H030 is longer than that of 12M1045. Combining the test results above, the 12M1H030 has the longest T_{max}, which is 16 µs.

	12M1H030	12M1045	12M1H090
Circuit character withstand time	20µs	20µs	18µs
Gate character withstand time	20µs	20µs	15µs
Thermal withstand time	16µs	12µs	9µs
T_{max}	16µs	12µs	9µs
On resistance	30mΩ	45mΩ	90mΩ
Rated Drain-Source voltage	1200V	1200V	1200V
Rated Drain current	56A	52A	26A
Total Gate charge	63nC	52nC	21nC
Rise time	19ns	18ns	4ns
Fall time	13ns	13ns	12.6ns

Table 3.3: The internal parameters of MOSFETs

In conclusion, this section introduces the method to estimate the T_{max} of MOSFET from three different circuit characters and test three MOSFETs with different on resistance, including 12M1H030, 12M1045 and 12M1H090. The fall time of three MOSFETs are almost identical, that means they have the similar shut down time which is an important characteristic when designing the SSCB circuit. According to the test result, the 12M1H030 has the longest short circuit withstand time of three MOSFETs, which is 16 µs, followed by 12M1H045 which is 12 µs, and the 12M1H090 is the shortest one, which is 9 µs. Meanwhile, 12M1H030 has the lowest on resistance which could reduce the power loss during the normally on working condition and highest rated Drain current which is benefit for high power applications.

3.4 Conclusion

In conclusion, the short circuit test for three SiC MOSFETs from the same family with different on resistance is introduced in this Chapter to obtain the short circuit characteristics of these MOSFETs. In addition, the method to obtain the fault reason and the maximum short circuit withstand time of the MOSFET is introduced which evaluate the MOSFET from three different aspects, including the overcurrent and overvoltage, the Gate state and the safety junction temperature.

CHAPTER 4

A design of the control system

4.1 Introduction

The main objective of this Chapter is the design of a control system, which can evaluate the operating conditions of the main power circuit according to the feedback signals and generate the corresponding drive signal to control the conducting or blocking operation of a MOSFET in solid-state circuit breakers (SSCB). As a part of the protection equipment in the circuit, the control system is required to have the fast reaction time and operation ability, when the short circuit fault occurs. Therefore, the close loop feedback, coupled with fast central processing units and execution devices are necessary in this control system design.

In this Chapter, two feedback signals are selected to describe the main circuit operating conditions. One is the Drain current (I_{DS}) through the MOSFET, the other is the Drain-Source voltage (V_{DS}). The short circuit test results in Chapter 3 show that the change of I_{DS} and V_{DS} can accurately describe the main circuit working condition during the short circuit fault. When the fault occurs, the I_{DS} will increase sharply with a significant di/dt, while the V_{DS} also reaches a peak. When the MOSFET is in blocking mode operation, the I_{DS} and V_{DS} will drop to zero.

Besides the feedback signal, the control system is required to have the high sampling frequency, the ability to perform complex calculations and the flexible designed ability, which requires a high performance central processing chip. Therefore, a high performance Field Programmable Gate Array (FPGA) is used as the central processing unit for the control system to calculate, compare the feedback data and generate the corresponding drive signal for MOSFET. The FPGA has a number of advantages for real time control system design, including high flexibility, lower cost compared with Application Specific Integrated Circuit (ASIC) and fast data processing speed. Those advantages make the FPGA meet the requirement of control system design in this Chapter. As the FPGA is a digital device but the feedback signal and drive signal are analog signals, one Analog-to-Digital Converter (ADC) and a Digital-to-Analog Converter (DAC) are required to connect the FPGA to the analog circuit, to collect the feedback signals and output the control signal. Although these devices both have high accuracy and high sampling speed, they cannot directly be used to drive the MOSFET as the range of the DAC output is from -5 V to 5 V, however the voltage range required for the Gate-Source voltage of the MOSFET should be -5 V to 15 V [184], and the drive signal from the DAC is easily influenced by the large current flowing through the main circuit during the fault. Therefore, an isolation circuit and an amplifier circuit are necessary between the DAC and the MOSFET. The drive circuit applied in this control system needs to transform the continuously changing drive signal when the control system is operating under the transform condition and isolate the main circuit and control circuit at the same time. Because of that, the isolation chips based on Transistor-Transistor Logic (TTL) could not be used in this drive circuit and a chip which is capable of generating an analog signal is selected. The control system schematic is shown in Figure 4.1.

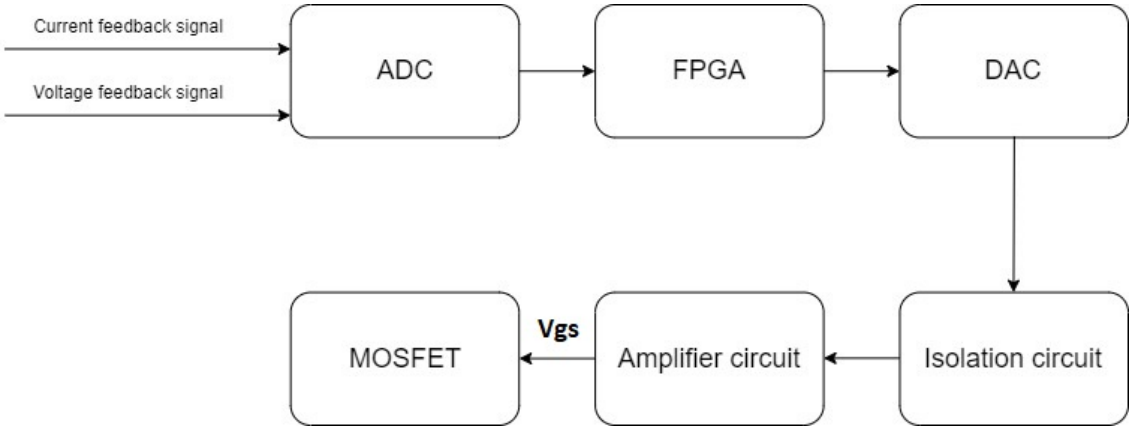

Figure 4.1: Control system flow chart

A special control system which could output the continuously changing control signal is designed and verified in this Chapter. It is composed of five blocks, including the ADC, the FPGA, the DAC, the isolation circuit and the amplifier circuit. The ADC is used to collect the feedback signals and transform them to digital signals for FPGA which will process the data and generate the correct drive signal according to the control requirement. The DAC is used to transform the drive signal to analog. The isolation circuit will isolate the main circuit and the control system to reduce the interference, and the amplifier circuit ensures the voltage of drive signal is enough to drive the MOSFET. More details of the control system design will be introduced in the remainder of this Chapter.

4.2 FPGA development

The FPGA development is divided into two parts, including the hardware program and the software program. In general, the complex calculation will be realized by hardware program in FPGA design as the speed of the programmable logic (PL) to process the large amount of data is faster than that of the processing system (PS). The hardware is capable of identifying the fault condition of the circuit and react in a time that will protect the circuit and reduce the overcurrent and power loss. Therefore, in this Chapter, the calculation and comparison to normal operation are achieved by hardware program. PS is also a necessary part of the design because PL is not capable of all the required operations and is normally selected to store data,

expand the external design ports, initialize the system and realize the bus interconnection for different modules. Human-computer interaction and system control are realized by the processing system. The powerful software Vivado is selected to program and debug the FPGA in this design. PL is programmed using the Verilog language and PS programming is based on C++.

After comparing the products available commercially, including SKU89, SKU110 and ECLYPSE Z7, the FPGA development board ECLYPSE Z7, with Xilinx Zynq-7000 ARM, is selected as the core device to design the control system because the performance of this FPGA developmernt board can meet the requirement of design with a reasonable 300 £ price. In addition, Xilinx has great technology support which is helpful for beginner to use the FPGA. Furthermore, to reduce the cost, selecting the Zynq-7000 ARM to build the circuit but not the development board costs less, around 100 £. Redesign the board with Zynq-7000 ARM can reduce the devices which are not useful in this thesis but used on development board, including the network port and flowing lights, and improve the integration rate to reduce the volume of the board. Zynq-7000 is a 667 MHz dual-core Cortex-A9 processor based on advanced system on chip (SoC) architecture. The advantages of this architecture are lower price and faster internal communication speed on chip with lower delay, as the architecture integrates both the PS and PL on a single die. Dual-core and high clock speed enables the processor to have the ability to process complex calculations in parallel which is a significant technical requirement of the control system, supporting the decision to select the Zynq-7000. Besides the processor, some external devices also needed. Digilent Zmod ADC 1410 module and Digilent Zmod DAC 1411 module are selected to collect the feedback signals and output the drive waveform. These two modules both have 100 MS/s pre-channel real-time sample rate and 2-channel 14-bit resolution, moreover the sufficient accuracy of ADC reaches $\pm 0.2\%$, which meets the high sampling frequency requirement and whilst maintaining high sampling accuracy. The high sampling accuracy is important to have the correct feedback signal and the result quickly when compare the feedback signal with the threshold. The ECLYPSE Z7 has interfaces specially designed for these two modules and diverse expansion devices, including DDR3 memory, QSPI flash, microSD card

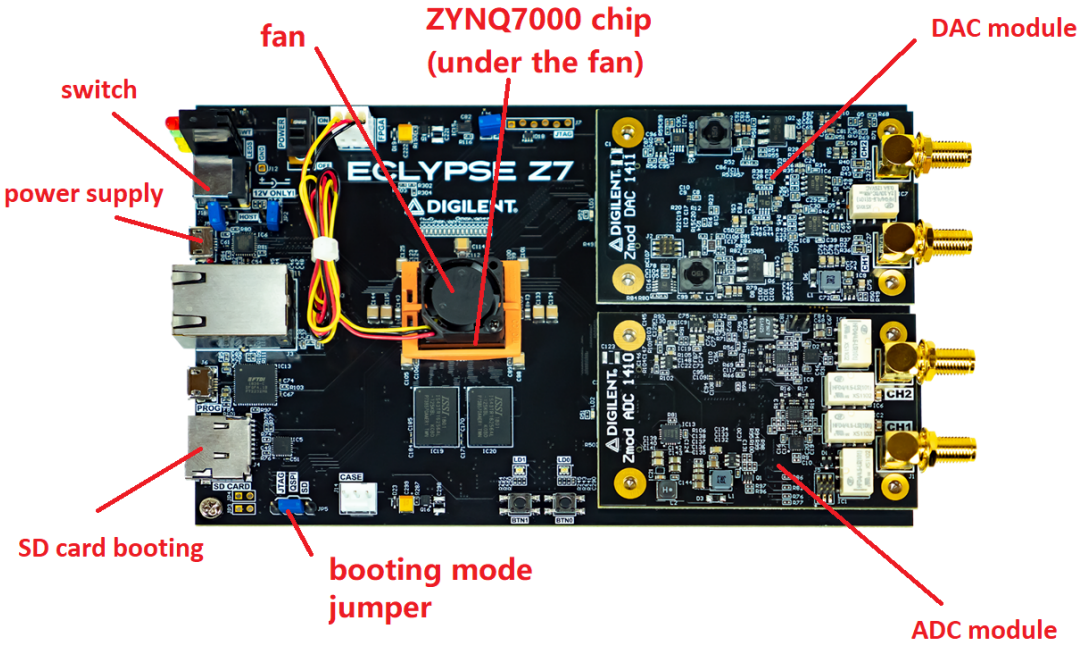

Figure 4.2: ECLYPSE Z7 development board top populated

connector and various USB interfaces to support the FPGA development. Therefore it is a smart choice for the control system design. The layout of the development board is shown in Figure 4.2.

The FPGA block diagram in shown in Figure 4.3. The ADC module collects the feedback signals and sends them to the PL and PS. PL is the significant block to compare the feedback data input and send the data of the drive signal to DAC module. PL also communicates with the PS as the registers in PS are necessary for PL when data needs to be saved or recalled. PS is mainly responsible for initializing other modules, like the ADC and DAC modules, which need the device ID and base address distributed by PS to communicate with other blocks. The communication between different devices in FPGA is based on the Bus. Therefore the AXI Bus and the I^2C Bus, which are integrated in the FPGA, are used in this design to transform the data between different blocks.

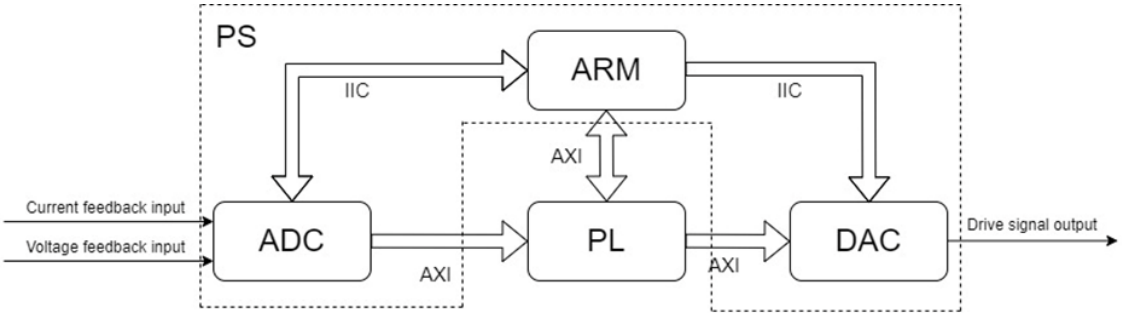

Figure 4.3: FPGA block diagram

To increase the response speed of the control system, it is necessary to select a rapid circuit condition judgment method for FPGA design. Several methods have been described in the literature and the most popular methods are threshold judgement and slope judgement [207]. Threshold judgement compares the measurement values with the threshold to evaluate the circuit condition. Normally, the measurement values are the transitor current and the voltage specify as I_{DS} and V_{DS}. Slope judgement compares the calculated slope of feedback signal with the threshold to evaluate the condition of the circuit. The short circuit protection process is shown schematically in Figure 4.4 as an example to introduce the concepts of threshold judgement and slope judgement.

According to the Figure 4.4, the circuit initially works normally when time $<$ t_0, and the current through the circuit is maintained at the rated value. When the fault occurs, the current begins to rise with di/dt limited by the inductance in the circuit. At t_1, the current reaches the specified current threshold, and the control system begins the decision making process that identifies a short circuit fault. However, the control system has a finite delay and the shut down starts at time t_2. This delay arises between the control system evaluating the short circuit and controlling the MOSFET to block the circuit. The response delay time between t_1 to t_2 depends on the control system hardware; therefore, it is a fixed value for the same control system. At t_2, the current reaches a peak and the MOSFET begins to block the circuit, so for $t > t_2$, the current decreases until reaching zero. Stability and reliability are the advantages of the threshold judgement technique, as there is no complex calculations required, just a comparison of the data point with a predetermined value which reduces the risk of system error.

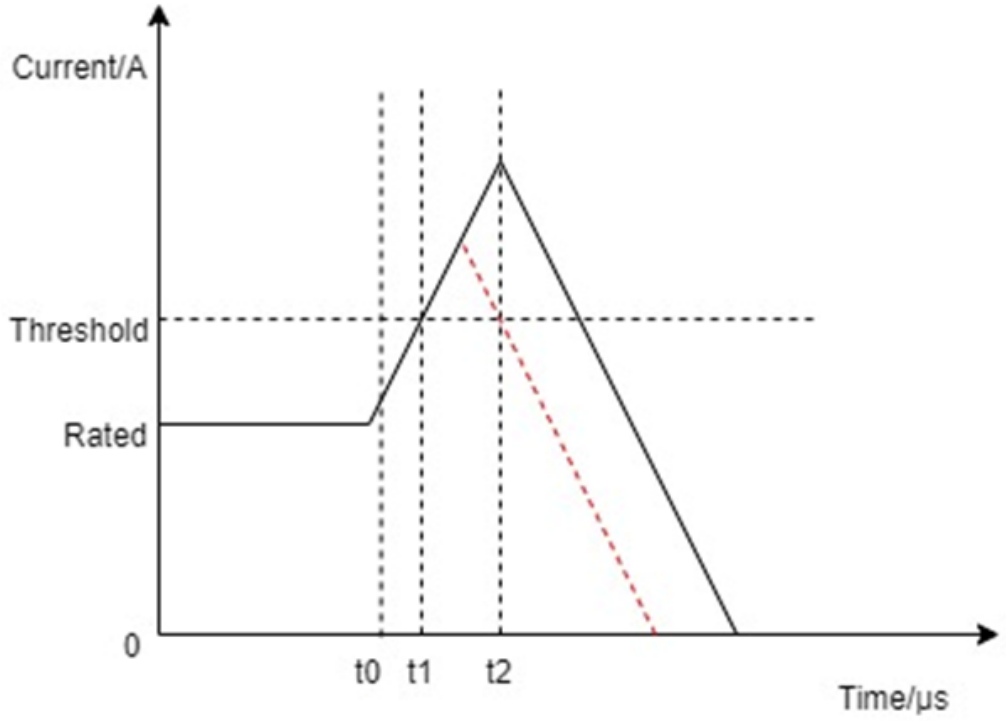

Figure 4.4: Short current and protection process

However, the response speed of the threshold judgement is not sufficient in high-speed system such as those formed using wide bandgap power electronic circuits. To increase the response speed, the delay time of the control system must be reduced. The delay time of the control system has two parts, one is the response delay time, another is the current rising delay time which is the time from the occurrence of the fault to the current reaching the threshold value. As the response delay time is fixed, the useful method is reducing the current rising delay. The slope judgment is a good choice to increase the reaction speed of the control system. The slope judgement technique compares the slope of the current with the specified resulting from slope threshold to determine the operating condition of the circuit. As the slope of a short current is very large, the delay in identifying the occurrence of a short circuit fault using slope judgement is much smaller than that of threshold judgment. Furthermore, the time at which the MOSFET starts to turn off can be reduced from t_1 to t_0 and the peak current is smaller than that for a system based on threshold judgement, as shown by the red line in the Figure 4.4. This technique reduces the impact of the short current and increases the short circuit withstand ability

of the circuit. However, the slope of current is not a directly measured parameter but a calculated value, which may introduce greater errors and hence reduce the reliability of the technique. As mentioned before, the threshold judgement has the better reliability and the slope judgement has the faster reaction speed. To ensure the reliability and reaction speed of the system, both of the judgement are used in this Chapter to design the control system.

4.2.1 Programmable logic development

The objective of the PL development is generating the corresponding drive signal for the MOSFET according to the operating conditions of the circuit. The PL system has three parts including the comparison and calculation, the controller and the output selector. The schematic of the PL development is shown in Figure 4.5.

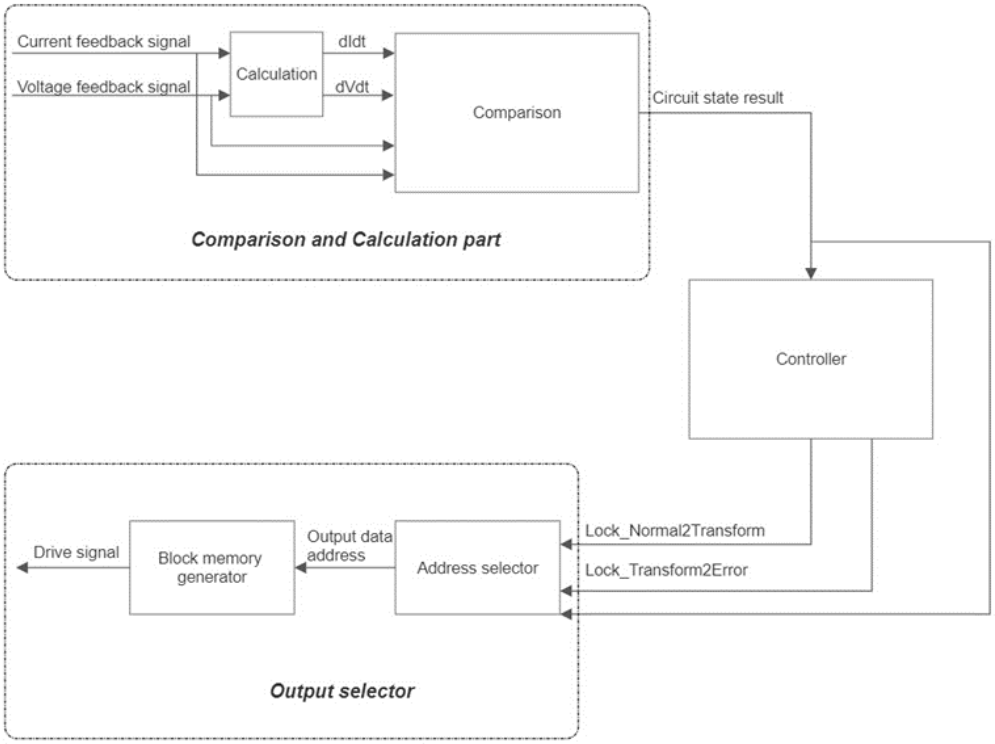

Figure 4.5: PL development schematic

The control signal generated by control system in this Chapter is different to those from traditional power electronic systems, which are normally based on a pulse width modulation (PWM) wave. There are three conditions in the new designed

control signal, including the normal condition, transform condition and the error condition. As the control signal output is generated by the DAC, the maximum and minimum voltage is limited to -5 V to 5 V, and the control signal design is based on this voltage range. When the circuit operates under normal conditions, the control signal generated by FPGA will be the normal condition and the DAC will output the maximum 5 V. Once the circuit has detected a fault, the control signal will be in the transform condition first and decrease the output voltage until it reaches the minimum, -5 V. After that, the control signal will be in the error condition and maintain the -5 V output. The diagram of the control signal is shown in Figure 4.6. The normal condition and the error condition both have a constant output voltage value, but that in the transform condition is required to be flexible as the rate of change of the voltage and the drive signal curve during the transform condition are required to be adjustable. Therefore, the control system must have the flexible design ability to freely change the output waveform and it is realised by PL development.

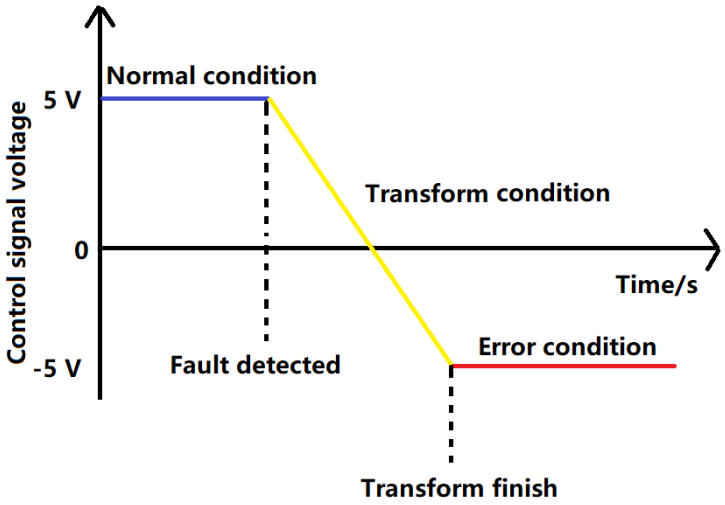

Figure 4.6: Control signal diagram

The task of the comparison and calculation part is generating the circuit condition result signal according to the feedback signals and transforming it to the controller and output selector. There are two blocks in this part. One is the calculation block which realizes the calculation of the current slope and voltage slope, which are represented by the di/dt and dv/dt separately. The second is the comparison block,

which compares the four signals, including the current value, the voltage value, the slope of the current and the slope of the voltage, with their corresponding thresholds and generate the circuit condition result signal. The most important function in the calculation block design is selecting the suitable method to calculate the slope of the feedback signals. The slope must have characteristics including small error and computationally simple calculation. As mentioned previously, the feedback signals are collected by the ADC, and the output of that operation is the conversion of the continuous-time signals to discrete-time [208]. Therefore, the method to calculate the slope of a continuous function such as differentiation could not be used in this block. The least squares method can be used to find the fitting function with the smallest square sum error for discrete data, and it is widely be used to predict the slope of discrete data [209]. The sampling error of ADC fits a normal distribution which supports the use of the least squares method. Therefore, the least squares method is selected to calculate the slope of feedback signals by linear regression and so the prediction function is given by the following function:

$$Y = bX + a \tag{4.1}$$

Where Y is the feedback signal and X is time. As the sampling speed of ADC is fixed at 100 MS/s, the difference between two adjacent sampling points is 10 ns. The variable a is the intercept and b is the regression coefficient. As the slope of the feedback signals is the output of the block, variable a is ignored and the equation to calculate b is shown below.

$$b = \frac{\sum_{i=1}^{n}(Y_{\mathrm{i}} - M_{\mathrm{Y}})(X_{\mathrm{i}} - M_{\mathrm{X}})}{\sum_{i=1}^{n}(X_{\mathrm{i}} - M_{\mathrm{X}})^2} \tag{4.2}$$

Where the M_Y is the average value of feedback signals and M_X is the average time. The sample should include a minimum of 2 points, but it is susceptible to excessive error due to accidental interference. Increasing the number of calculation data points can significantly reduce the impact of unintentional interference. However, increasing the number of samples involved in the calculation will not only increase the computational complexity, but also increase the system delay at start-

up. The feedback voltage and current are collected alternately, because the ADC is not able to enable two channels instantaneously [210] [211]. Hence, for each additional sampling point, the delay increases by 20 ns, and excessive delay will reduce the response speed of the control system. If increase the number of samples, the delay and computational complexity will increase, which results in the decrease of the slope judgement reaction speed. The advantage of slope judgement over threshold judgment will decrease, and the reaction speed of slope judgment may slower than that of threshold judgement when the number of sampling points is further increased. However, if the number of samples is 2, the calculated slope is susceptible to distortion due to extreme values. Considering the balance of calculation accuracy and the response speed, three data points of feedback signals are used to calculate slope. Therefore, the variable 'n' in the function outlined in equation 4.2 above is set as three.

A Cartesian coordinate system with time as the horizontal axis and sampling values as the vertical axis is established to simplify the calculation. The coordinates of the three sample data are (X0, Y0), (X1, Y1) and (X2, Y2). It is challenging to directly substitute these coordinates into the equation for the PL, as a large number of multiplications and divisions consume significant logic resources and slow down calculations. Therefore, a method to simplify the calculation is outlined in the equation 4.3. In the fixed coordinate system, all three coordinates are variable, and so that increases the complexity of the calculation. It is planned to set the first data coordinate of each set of data as the origin of the coordinate system, which reduces the number of variables to two, and the coordinates change to (0, 0), (X1-X0, Y1-Y0) and (X2-X0, Y2-Y0). Substituting the coordinates (0, 0), (A1, B1), and (A2, B2) into equation 4.2, After using the substitution method:

$$b = \frac{2A_1B_1 + 2A_2B_2 - A_1B_2 - A_2B_1}{2(A_1)^2 + 2(A_2)^2 - 2A_1A_2} \tag{4.3}$$

As the sample time is fixed, in the same coordinate system, the difference in the abscissa of two coordinate points is the same. Therefore, the following relationship can be obtained.

$$A_2 = 2A_1 \tag{4.4}$$

Substitute the equation 4.4 into 4.3:

$$b = \frac{B_2}{2A_1} = \frac{B_2}{A_2} = \frac{Y_2 - Y_0}{X_2 - X_0} \tag{4.5}$$

According to the equation 4.5, the linear regression result may be replaced by the slope of the line passing through the first data point and the third data point under the calculation conditions mentioned in this section, when the time difference between the data points is significantly small.

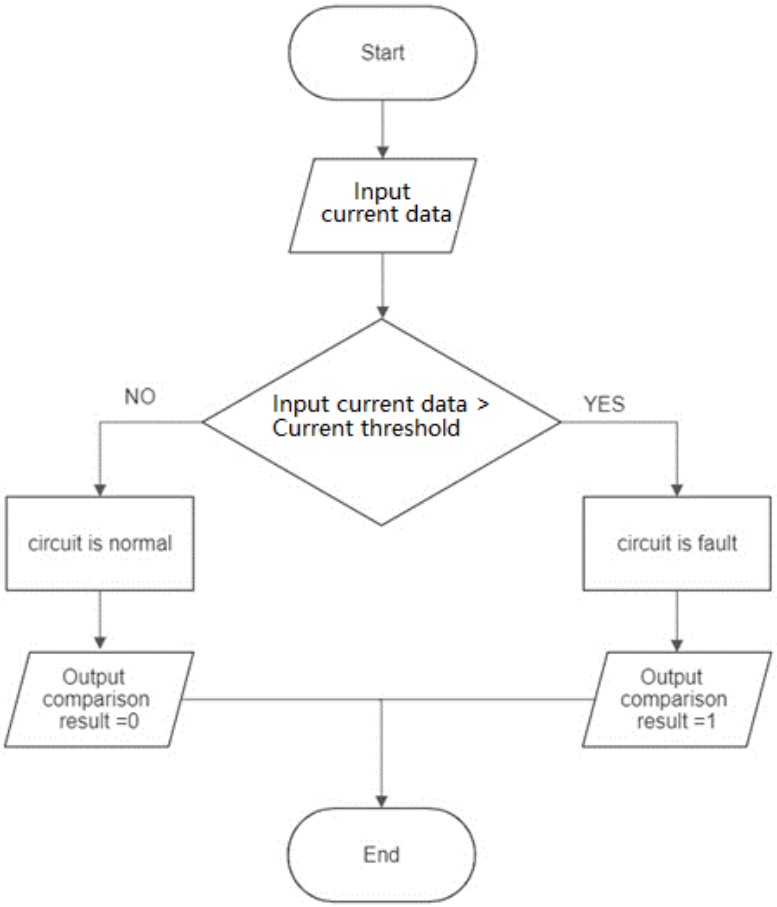

Figure 4.7: Comparison flow chart for current

The task of the comparison block is generating a circuit condition result according to the input signals to help selecting the correct output signal. There are four input values into the comparison block, and the comparison method for each signal is different. According to the test result in Chapter 3, when the fault occurs, the Drain-Source current will rise rapidly. Therefore, the current signal will be compared with the threshold directly and once the current is over the threshold, the circuit is believed to be in the short circuit condition, and the comparison result will be 1. In contrast, if the circuit works normally, the result will be 0. The current comparison flow chart is shown in Figure 4.7.

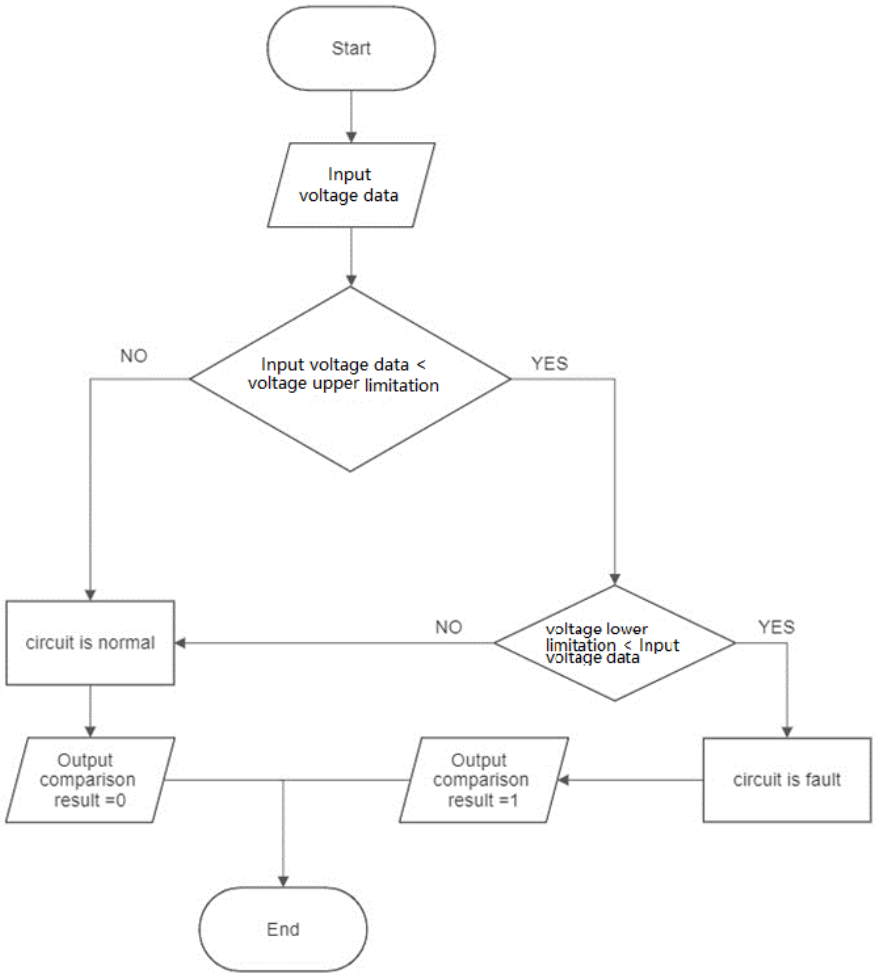

Figure 4.8: Comparison flow chart for voltage

In contrast to the Drain-Source current, V_{DS} will drop to a value that is close to but not zero at the beginning of the fault and return to rated voltage after the circuit has been totally blocked. Therefore, the threshold of the voltage signal is a range with an upper limit and a lower limit. If the voltage is in the range, the comparison result will be 1 to indicate the circuit is fault. If not, the comparison result will be 0. The voltage comparison flow chart is shown in Figure 4.8.

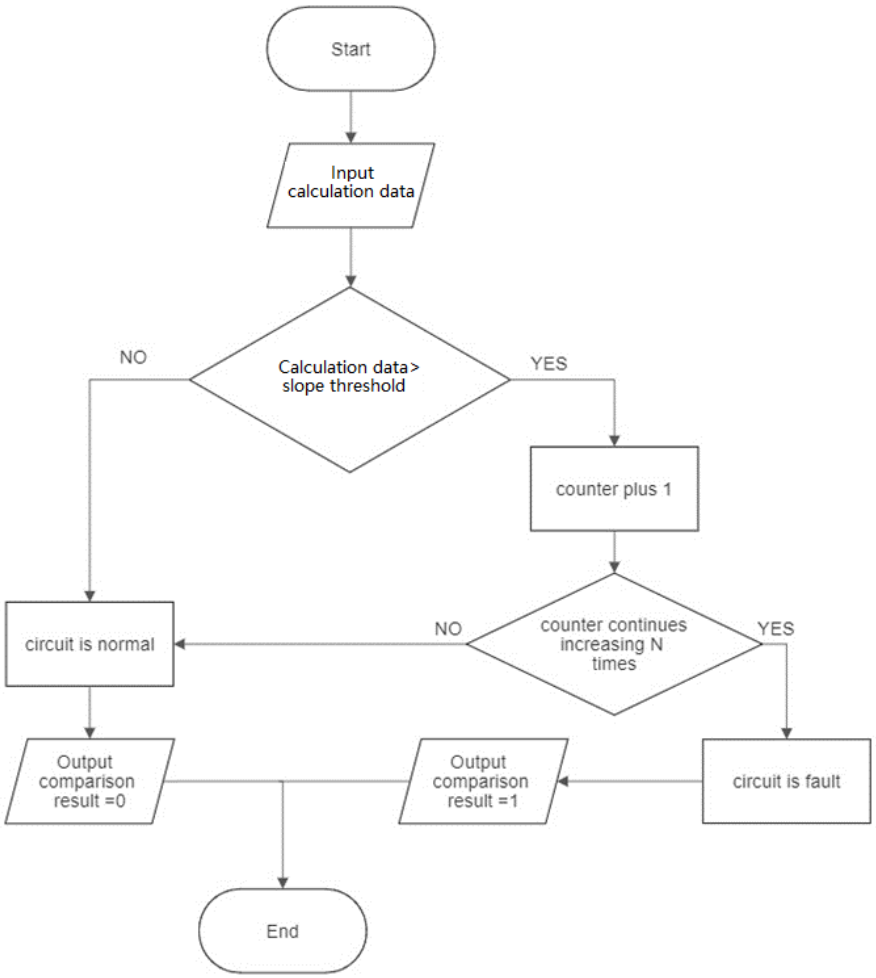

Figure 4.9: Comparison flow chart for calculated data

Voltage and current signals are the original collected signals from the ADC and so the calculation error does not exist with these signals. If there is a margin when setting the threshold, it can prevent misjudgement caused by voltage and current fluctuations, but this method is not suitable for calculated data, as it is easier to identify a significant change in the calculated data and it is difficult to make an accurate judgement based solely on the threshold. This results in the comparison flow chart of calculated data to be different as shown schematically in Figure 4.9.

In addition to the threshold, a counter is used to help assess the circuit condition. If the calculated data is over the threshold, the counter will be increased by one. When the counter increases above the certain value, the circuit is considered to be under a fault condition and the comparison result is 1. Otherwise, the counter will be reset as 0 and the comparison result is 0.

The circuit condition result is decided by these four comparison results. Only when the current, voltage, dI/dt and dV/dt are all lower than corresponding threshold, the circuit condition result agrees the circuit works normally and sends 0 to the controller. If not, the result collected by controller remain as 1. When the voltage or current value is higher than the corresponding threshold, the voltage or current compare result is 1 and the main circuit is considered having the short circuit. When the dV/dt or dI/dt exceeds the corresponding threshold continuously, the dV/dt or dI/dt compare result is 1 and the main circuit is considered having the short circuit. The truth table is shown in Table 4.1.

Voltage compare result	Current compare result	dV/dt compare result	dI/dt compare result	Circuit condition result
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Table 4.1: Comparison truth table

The Controller block is the significant part to realise the circuit blocking when the fault occurs. According to the test data shown in Chapter 3, when the circuit begins to be blocked, the current decreases from the peak value until reaching zero. During this process, the current is reduced below that at the moment when the fault is detected. Considering the logic of the comparison block, the circuit will turn on again when the current falls below the threshold, even though the fault has not been removed. Hence, the current will vary with values around the threshold and the circuit will not correctly enter the blocking condition. Therefore, the circuit condition result could not control the output drive signal alone and the controller is designed to generate two lock signals, Lock_Normal2Transform and Lock_Transform2Error, to help controlling the output drive signal. The logic of the controller is shown in Figure 4.10.

Lock_Normal2Transform is the switch to control the output signal changing between normal condition and the transform condition that blocks conduction in the circuit. It is triggered to change the value from 0 to 1, or from 1 to 0 by the rise edge of the circuit condition result. When the circuit condition result gets a rising edge, the Lock_Normal2Transform is set as 1 and the output signal works on transform condition. However, the output signal returns to normal condition requires the Lock_Normal2Transform and the circuit condition result to be 0 at the same time. Lock_Transform2Error is the switch, triggered by the counter, to control the output signal to change from the transform condition to the error condition when it changes from 0 to 1. As the design of the transform condition could change the shut down time of the MOSFET, the controller block must consider the impact of the circuit condition result to the transform processing in different shut down time.

There are two situations, one is when the shut down time is shorter than the time that circuit condition result is 1, and another is the shut down time is larger. Therefore, the solution to this problem is controlling the Lock_Transform2Error by a variable independent of the circuit condition result. That is the reason why a counter is used to control the Lock_Transform2Error. The counter is used to count the number of the data points generated by the DAC during the transform condition. Once the counter overflows, the Lock_Transform2Error is set to 1 and output drive

Figure 4.10: Logic of the controller

signal is set to -5 V to block the circuit. The counter is set as 2000 to ensure the Lock_Transform2Error remains as 1 for a period of when the current returns below the current threshold, to ensure the circuit remains in the blocking conduction. Otherwise, if counter has not reached the peak, the Lock_Transform2Error is set to 0.

A variable frequency word is used to adjust the transform time of the drive signal and the relationship between the frequency word and the transform time is defined in equation 4.6.

$$transform\ time = \frac{10\mu s}{frequency\ word} \tag{4.6}$$

The output control signal is saved by 1024 data points, and these points are saved in 1024 different addresses separately which is same with the look up table. As the time difference between the two output data points is fixed, which is 10 ns decided by the performance of the DAC, the total shut down time of the transform signal drops to -5 V is decided by the number of the output data points used to generate the waveform. For example, if the frequency word is set to 1, these data points will be output one by one, and the shut down time is 10230 ns; if the frequency word is set to 10, every tenth data points will be output and the total number of the output data points will be 102 which take 1010 ns to shut down the circuit. Therefore, a larger frequency word makes the output value drop more quickly to -5 V. To unify the time unit to µs, the constant is set as 10 µs in equation 4.6.

The output selector is the part to output the correct signal according to the control signals from the controller and the comparison block, which is shown in Figure 4.5. There are two blocks in this part, block memory generator and address selector. The block memory generator is an integrated module for storage functions, that is used as a single port Read-Only Memory (ROM) to save the discrete output waveform in this system. The look up table with 1024 data is saved as a COE document which can be generated by MATLAB. Each of these values has a corresponding address. Therefore and the address selector block is designed to control the output values through their addresses, and it is controlled by three signals, including the circuit condition result, Lock_Normal2Transform and Lock_Transform2Error. The

flow chart of the output selector operation is shown in Figure 4.11, and the truth value table of the output selector operation is shown in Table 4.2.

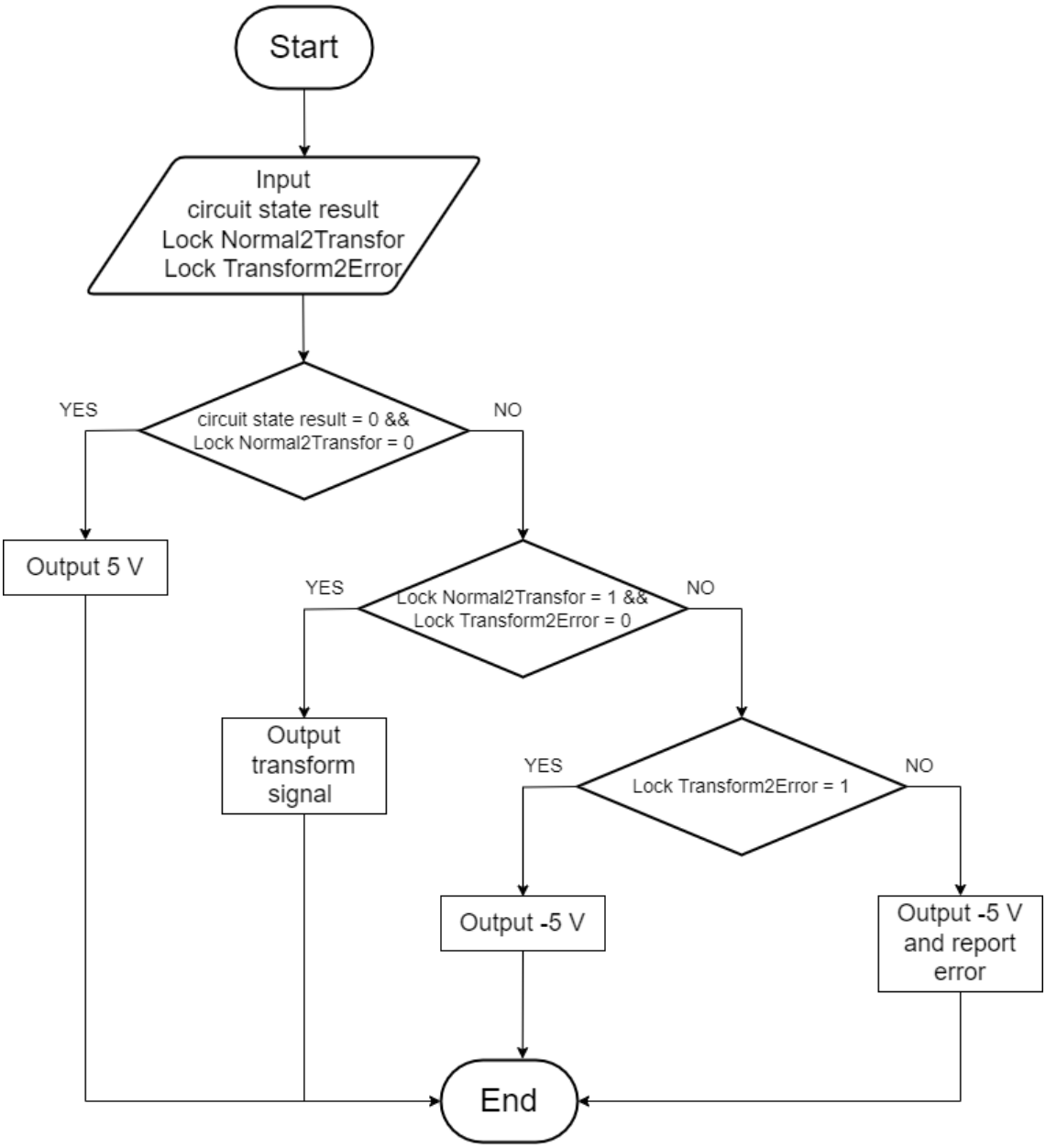

Figure 4.11: Output selector flow chart

Circuit state result	Lock Normal2Transform	Lock Transform2Error	Output result
0	0	0	5 V
0	0	1	5 V
0	1	0	Transform
0	1	1	-5 V
1	0	0	-5 V and error report
1	0	1	-5 V
1	1	0	Transform
1	1	1	-5 V

Table 4.2: Output selector operation truth value table

Besides correctly driving the MOSFET, the control system is also required to demonstrate the ability to restart the circuit once the fault has cleared. In this design, the manually controlled restart button is used to restart the control system. The shut down and restart process of the control system is shown in Figure 4.12. At t_0, the circuit operates normally, and three control signals are held at their default values. At t_1, the fault occurs and the feedback signals over the threshold and circuit condition result has a rising edge. Under this condition, the Lock_Normal2Transform changes to 1 from 0, which result in the counter begins to count the number of output data. Generated by the DAC and the circuit begins working on transform condition. At t_2, the counter reaches the peak value 1024 which is the number of the data points saved in memory and the counter is set to 2000 to ensure the counter is larger than 1024 until t_4 which results in the Lock_Transform2Error changing to 1 from 0. As the Lock_Normal2Transform and Lock_Transform2Error both remain at 1, the circuit operates in the error condition and the output drive signal remains at -5 V. At t_3, the main circuit is blocking, and the feedback signal lowes the threshold, therefore the circuit state result returns from 1 to 0. However, the Lock_Normal2Transform is triggered by the rising edge of the circuit state result and remains as 1, which results in the counter not being reset and remains as 2000. Therefore, the Lock_Normal2Transform and Lock_Transform2Error both remain as 1, and the circuit will remain in the blocking state. After the fault has been removed, the circuit state result rises to 1 again because the manually controlled restart button is pushed at t_4. The Lock_Normal2Transform is triggered by the rising edge of

the circuit state result and returns to 0. The counter is reset for the new counting cycle. At t_5, the manually controlled restart button is released and the control system is reset. The output drive signal will return to 5 V and the main circuit operates under the normal condition again. Moreover, if the fault reoccurs at t_6, the control system can realise the blocking function again to protect the circuit.

The design of the PL has multiple advantages, including the reliability of circuit blocking, button anti-shake and the convenient restart function. In contrast with the PWM wave, the transform process of the output drive signal increases the shut down time of the circuit, which may result in the condition that the control system stops the transform process and outputs the 5 V signal again because the feedback signals drop below the threshold during the transform process, if the output drive signal is just decided by the circuit state result. In this design, two condition locks are used to ensure the blocking process will not be interrupted and hence verify the the reliability of the control system. After the fault has been removed, the control system can be remotely restarted by the button or via the control computer. Furthermore, the restart signal is designed to be triggered by the release of the button, which prevents accidental touches caused by the button shake.

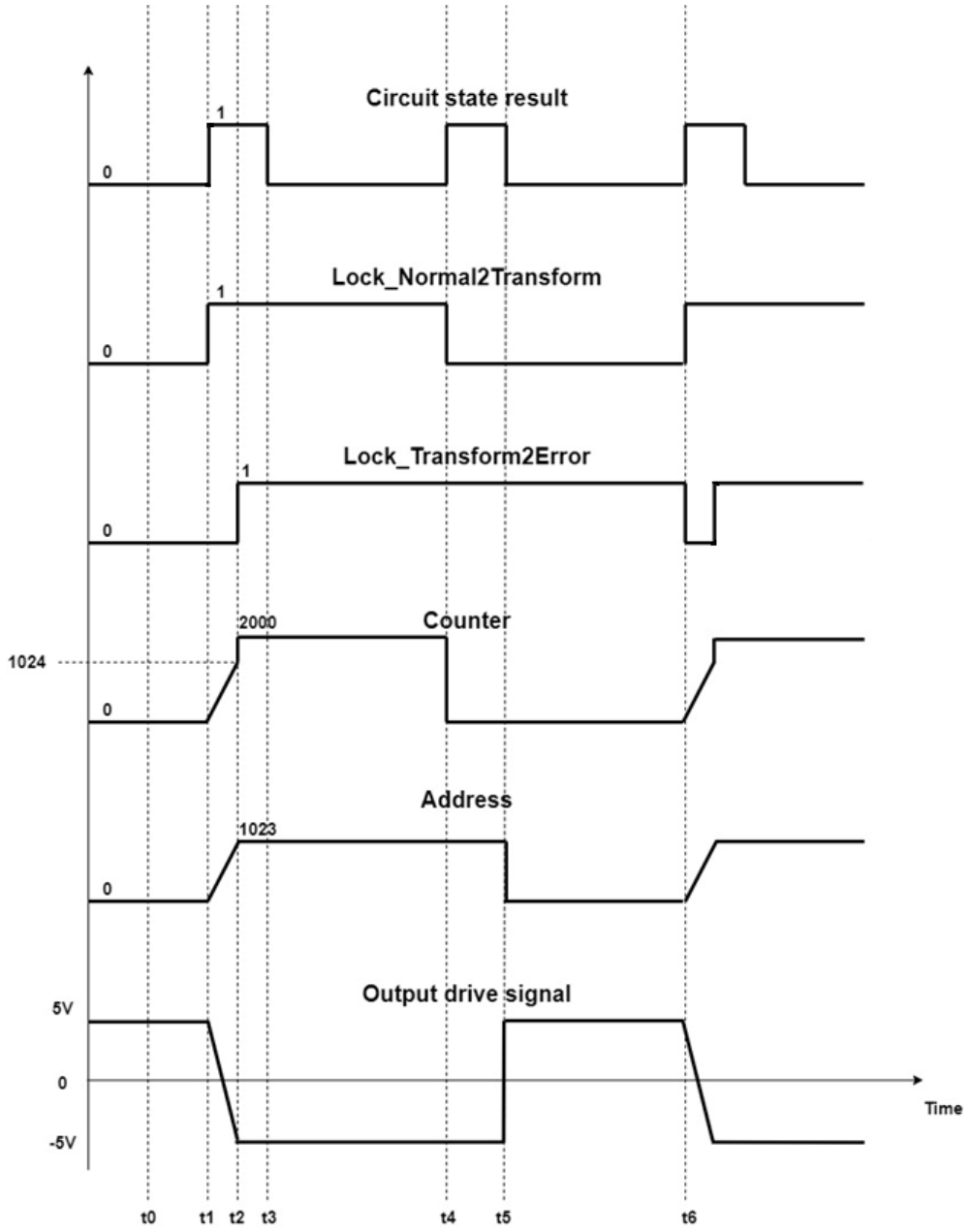

Figure 4.12: Circuit block and restart processing

4.2.2 Processing system development

The main objective of the PL system is to enable the communication between the subsystems in the control unit. The processing system consists of two ARM A9 chips, which form the CPU in the system, and the external devices, including the ADC and DAC modules, internal and external memory interfaces and Advanced Microcontroller Bus Architecture (AMBA). The ADC module is used to collect the feedback data which is transferred to the PL, and the DAC will output the drive circuit to control the circuit. The memory is used to save the data and support the communication between different devices. AMBA is mainly used to connect and manage the devices and blocks on chips, and in this section, the AXI Bus and IIC Bus are selected.

The first task of the PS is to enable the ADC and DAC to help collect and output data. The flow charts of ADC and DAC operation are shown in Figure 4.13. Before operation, the ADC and DAC need to be initialized. The Device ID is the identification code of the device in ARM. The Base address is the memory address assigned by ARM to save the data, which is required in all data operation. DMA allows the data from external devices to be send to flash memory directly, which increases the speed of data transformation and frees up the ARM. Traditionally, the ARM should copy the data to the registers first and sent to flash through the use of interrupts, causing the ARM to stop and answer the interrupt frequently, and resulting in poor ARM performance as during the interruption, other access requirements are not allowed. Otherwise, in DMA transformation, the ARM just needs initialize the DMA controller and data transfer in controlled by the DMA controller, allowing the ARM to respond to other access requirements, increasing the data processing speed. Another advantage of the DMA is that it allows devices with different frequencies to communicate with each other without the involvement of the ARM. Normally, the external devices in embedded systems operate different working frequencies, which results in the message sent by one device being different to the one received by another device. The DMA allows the data to flow between different devices using memory as a transfer station, which reduces potential restrictions on equipment selection. Therefore, DMA is important for high performance embedded

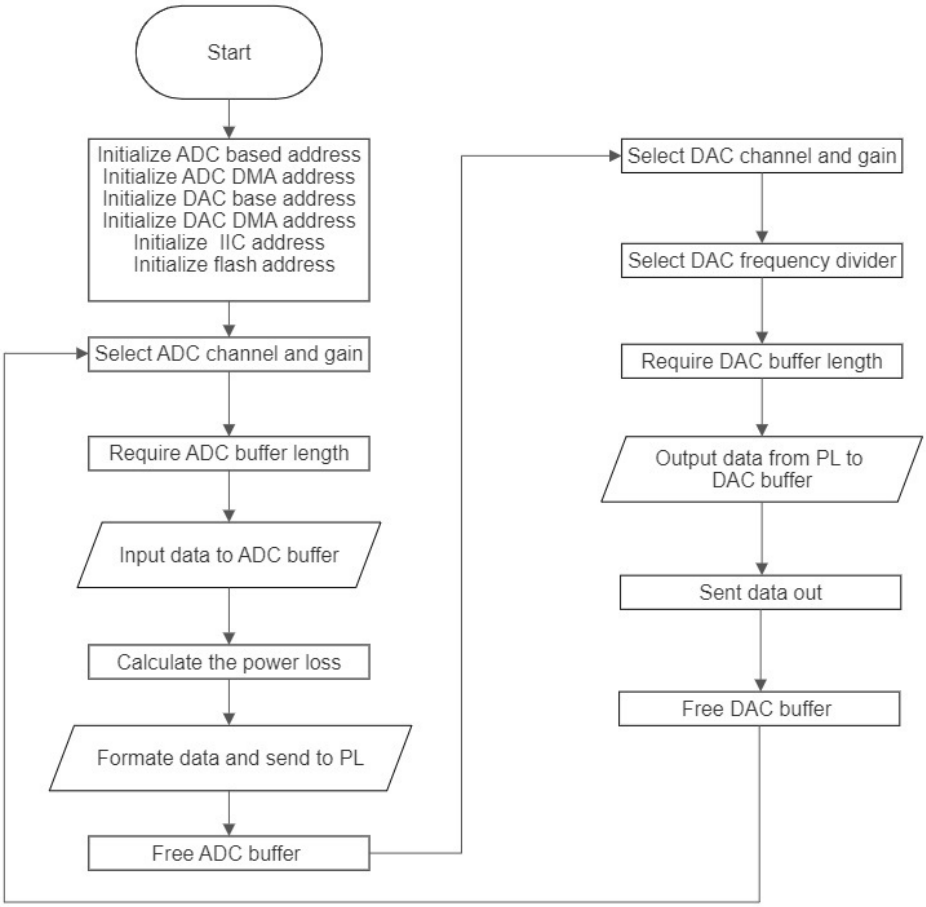

Figure 4.13: ADC and DAC operation flow chart

systems, and it is selected to transform the data in PS development.

After initialization, the ADC selects the channel and collects data. The ADC module has two channels enabling the collection of the feedback current and voltage separately. The power loss in the transistor is calculated by the ARM according to the feedback data collected and the data is sent to the PL to evaluate the condition of circuit. Subsequently, the DAC module is enabled to output the drive signal generated by the PL. As a real time control system, the process above is continually repeated to ensure the circuit can be shut down in time to protect the circuit from the fault.

Power loss in the transistor is a significant issue which should be considered when design the control system, and it is calculated by FPGA from the real time to feedback voltage and current data. Normally, the calculation of the power loss follows the equation 4.2.6 :

$$W = \int U \times I dt \tag{4.2.6}$$

Where the W is the power loss, U is the Drain-Source voltage and I is the current through the circuit. However, as mentioned above, the 2 channels of ADC could not be enabled simultaneously, therefore the feedback current and voltage data is not concurrent. The sampled value table is shown in Table 4.3. Where the value V_1, V_2, I_1 and I_2 are sampled data and $V_{1\text{-}2}$ and $I_{1\text{-}2}$ are interpolated values.

Time	t_0	t_1	t_2	t_3
Voltage	V_1	$V_{1\text{-}2}$	V_2	
Current		I_1	$I_{1\text{-}2}$	I_2

Table 4.3: ADC sampling data

As the sampled voltage and the current are not taken simultaneously, equation 4.2.6 cannot be directly used to calculate the power. As an alternative, the interpolated value will be used to replace the value which cannot be sampled, to calculate the power loss. For example, when calculating the power loss using equation 4.2.6 at t_1, the voltage and current data at t_1 are required. Whilst, the ADC sampled the current value, I_1, at the time t_1, the voltage ,V_1, is no longer the correct value. Hence, the voltage value at t_1 is replaced by the interpolated value, $V_{1\text{-}2}$, which is a linear interpolation of the sampled value V_1 at t_0 and V_2 at t_2. At time t_2, the voltage V_2 is the sampled value and the current $I_{1\text{-}2}$ is the interpolated value in a similar manner. The interpolated value as the instant of the calculation is the average value of the two sampled values.

As the interpolated value is not the value of the instant of the calculation, the accuracy of the power loss calculation should be considered. Normally, the more number of data points used in a calculation, results in higher accuracy. However, it results in a greater delay time and slows down the speed of the control algorithm because the calculated result can be generated until all data have been collected at

the beginning. The delay of the calculation result will increase the reaction time of the control system, which will decrease the advantage of faster reaction speed of slope judgement compared with the threshold judgement. Therefore, the calculation speed is important. In addition, the accuracy of two point interpolation method is evaluated. The slope between two discrete voltage points can be estimated by equation 4.2.7

$$V_2 - V_1 = (t_2 - t_1) \times \frac{dV}{dt} \tag{4.2.7}$$

Where V_2 - V_1 is the voltage difference between two data points and t_2 - t_1 is the time difference. The slope of current can also be estimated using an identical technique. The sampling frequency of the ADC is 100 MS/s, therefore, the time difference between two sampled data is 10 ns and that between two sampled voltage or two sampled current is 20 ns. The minimum voltage difference of the feedback signal is around 6 mV. Therefore, the minimum slope of the feedback signal can be determined by ADC is 3×10^5 V/s.

According to the results presented in Chapter 3, the maximum slope of voltage is around 2.7×10^8 V/s and according to the equation 4.2.7, the maximum difference between two adjacent voltage points is 5.4 V, which is 2% of the peak voltage value in the short circuit test. The maximum slope of current is 2.3×10^8 A/s and the maximum difference of two current points is 4.6 A, which is 2% of the peak current value in the short circuit test. Compared with the 230 A peak value of short circuit current and 270 V short circuit voltage, the calculation error is tolerable for the test in this thesis. Therefore, considering the balance between the accuracy and the complexity of the calculation method, the two point method is utilised to estimate the data and the time delay of the calculation is 10 ns.

4.2.3 FPGA output result

As mentioned in section 4.2, the drive signal for the MOSFET is generated by the combination of the PL and PS functions and the output result of the FPGA is described in this section. The impact of the different drive signals on the performance of the short circuit test is described in detail in Chapter 5 and the objective of this Chapter is the development of the control system to generate these signals, which are shown in Figure 4.14. The designed drive signal has three different shapes, including linear, convex and concave. Figure 4.14(b) shows the test of these three kinds of signals that arise from the same short circuit time, and Figures 4.14 (a), (c), (d) show the test of the signal performance with different short circuit time. The test result of FPGA output meets the requirement for the overall system in terms of the fast reaction and flexible output drive signals, and the control system will be applied in Chapter 5.

The basic requirements of the control system for the drive signal are the generation of the necessary voltage level to correctly drive the MOSFET according to circuit condition and protecting the circuit when faults occur. The FPGA development described in this Chapter meets these requirements and the result is shown in Figure 4.15. The yellow signal represents the circuit condition, when it is -5V, the circuit operates normally but when it changes to 5V, the circuit can be considered as being in the fault condition. The pink waveform is the output signal from FPGA that can be used to control the MOSFET after amplification. As the transition is too short to be clearly observed in this Figure, only the normal operation and error conditions can be observed. The result meets the requirement that when the circuit works normally the drive signal maintains the MOSFET in the conducting condition, once the fault occurs, the circuit transitions to the blocking condition. Once the drive signal goes to error condition, it prevents the circuit condition returning to normal which ensures the control system can block the circuit. After the problem is removed, the system can be manually restarted by the circuit condition trigger signals generated by the PS.

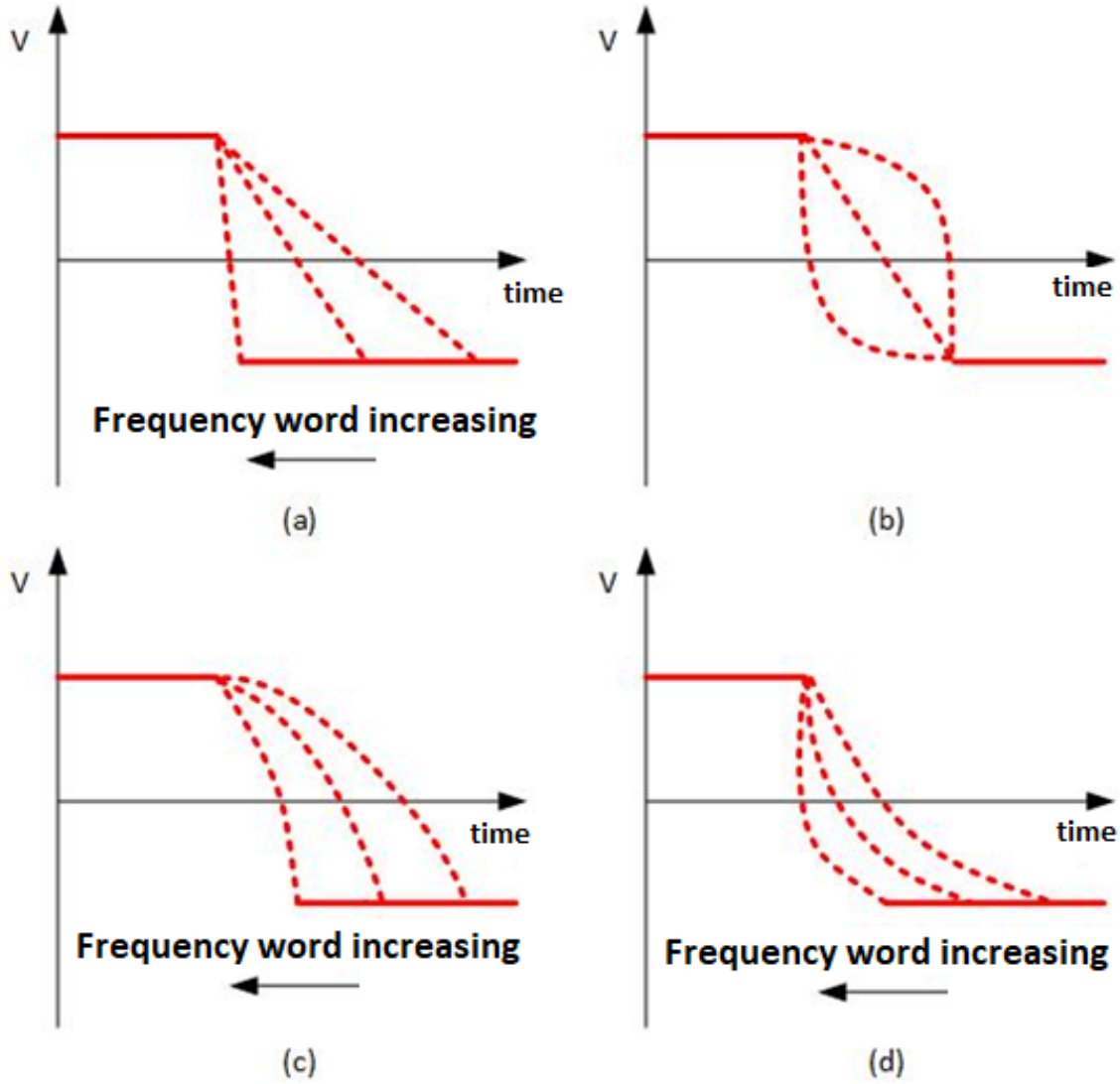

Figure 4.14: (a) Linear output with different frequency word, (b) Linear, convex and concave output with same frequency word, (c) Concave output with different frequency word, (d) Convex output with different frequency word

The control system requires the drive signal to show a rapid response to the short circuit and maintain blocking to protect the circuit. Therefore, the delay from the detection of the short circuit condition to initiating the shut down process must be minimised. The delay in this design may be reduced to 440 ns, which is reasonable for short circuit protection as generally, the short circuit withstand time of the circuit is several microseconds, according to the test result in Chapter 3. The delay of the drive signal is shown in Figure 4.16, where the yellow signal is the circuit condition, and the pink signal is the output drive signal.

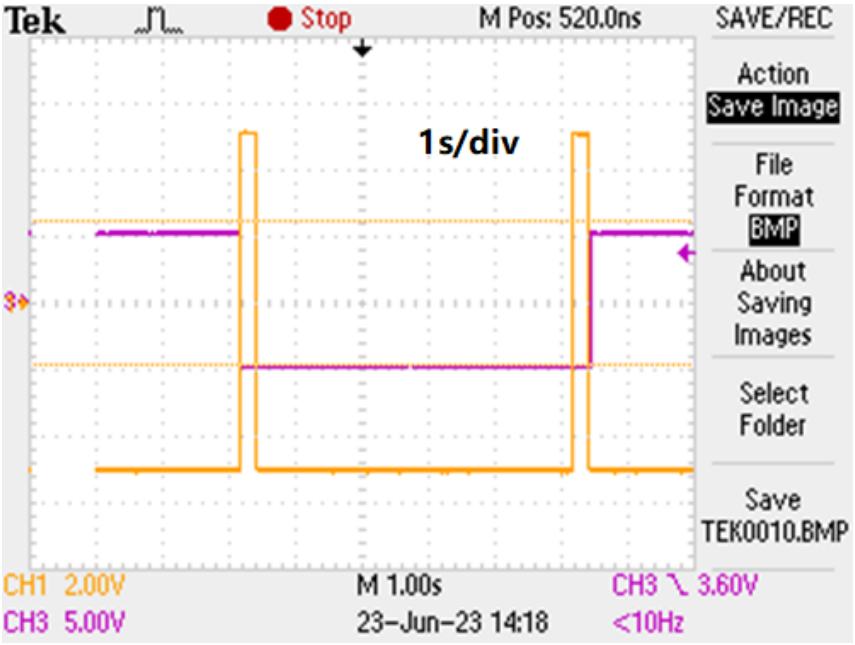

Figure 4.15: Overview of drive signal, yellow line is the fault trigger signal, pink line is the FPGA output signal

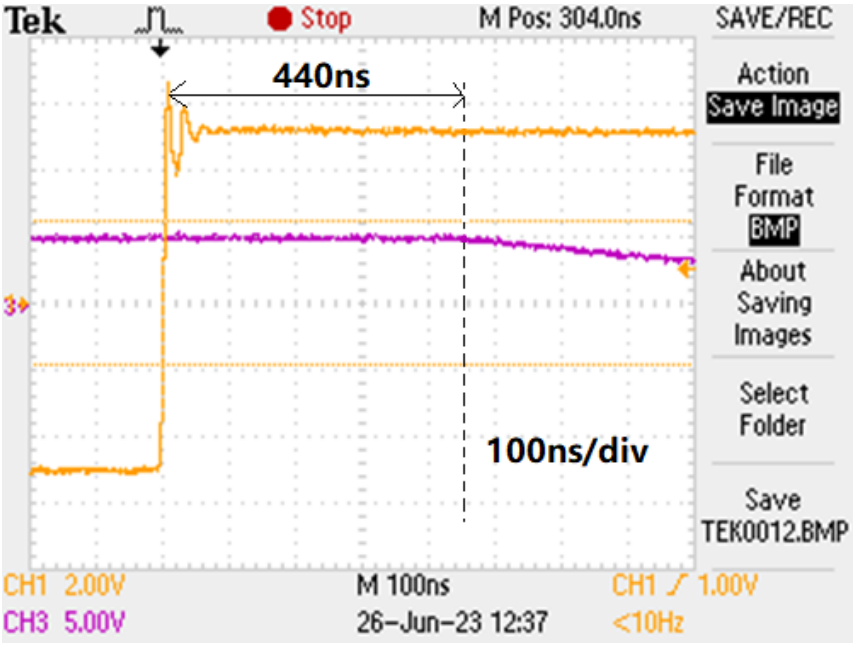

Figure 4.16: The delay of the drive signal, yellow line is the trigger signal, pink line is the FPGA output signal, black dotted line is the time point that the FPGA output signal begins decreasing

4.2.4 Conclusion

This section introduces the development of FPGA which include the PL and the PS parts, and realises the design of a controllable transition in the drive signal. The PL part realises the collection of two feedback signals, including the current and the voltage of the MOSFET, data calculation, circuit condition judgement and flexible drive signal generation. The application of high accuracy ADC and DAC improves the accuracy of the control system in circuit condition judgement, meanwhile the high speed FPGA and the slope judgement decreases the reaction time and increases operating speed of the control system. The main role of the PS is supporting the PL system, including the external devices initializing, data saving and the communication of the devices on chip. Furthermore, the IIC bus is applied in PS to transform the data from the FPGA to the control computer. As designed, with the cooperation of the PS and PL, the FPGA can generate flexible control signals, with the linear, convex and concave transform part, according to the requirement of the gate drive circuit. Meanwhile, the shut down time of these control signals can be adjusted by control of the frequency word. In conclusion, the design of the FPGA system enables the generation of the control signals which can be used to undertake the experimental verification tests in Chapter 5 to compare the performance of different control signals in MOSFET short circuit test.

4.3 Isolation and amplifier circuit

The main objective of this section is design of the isolation and amplifier circuits for the control signal from FPGA to protect the control system from high voltages in the power circuit and driving the MOSFET. The control signal generated by FPGA could not be directly used to drive the MOSFET for two main reasons. One is the current of the control signal is limited to below mA, which is much smaller than the 230 A overcurrent through the main circuit during the fault, and so an isolation circuit is required to protect the control signal and FPGA from interference and spikes. Another problem is the voltage of the control signal is determined by the DAC which is from -5 V to 5 V, which is insufficient to drive the MOSFET, as

the minimum drive voltage to turn on the MOSFET is 15 V, according to the datasheet [184]. Therefore an amplifier circuit is required to enable the control system design to be used to control the MOSFT behaviour.

The control signal for the MOSFET gate in this Chapter is a continuous signal to enable accurate control of the MOSFET, and so the traditional isolation circuit based on the TTL logic device cannot be used, because the logic output cannot realise the continuously changing of the signal because it is fundamentally limited to two states. Therefore, in this Chapter, the reinforced isolated amplifier AMC1301 is used to realise the isolation circuit. The maximum input analog signal voltage is from -250 mV to 250 mV, which matches the output voltage range of the DAC. There is a modulator in the chip to convert the analog input signal into a digital bitstream, and the bitstream is subsequently transformed across the isolation barrier that separates the input side and the output side. On the output side, the bitstream will be processed by a fourth-order analog filter and resulting in a differential analog signal. The bitstream transformation of AMC1301 ensures the continuous signal through the isolation barrier without any changes, which is a significantly advantage in comparison to a traditional TTL device and the main reason that the AMC1301 is selected to build the isolation circuit in this Chapter.

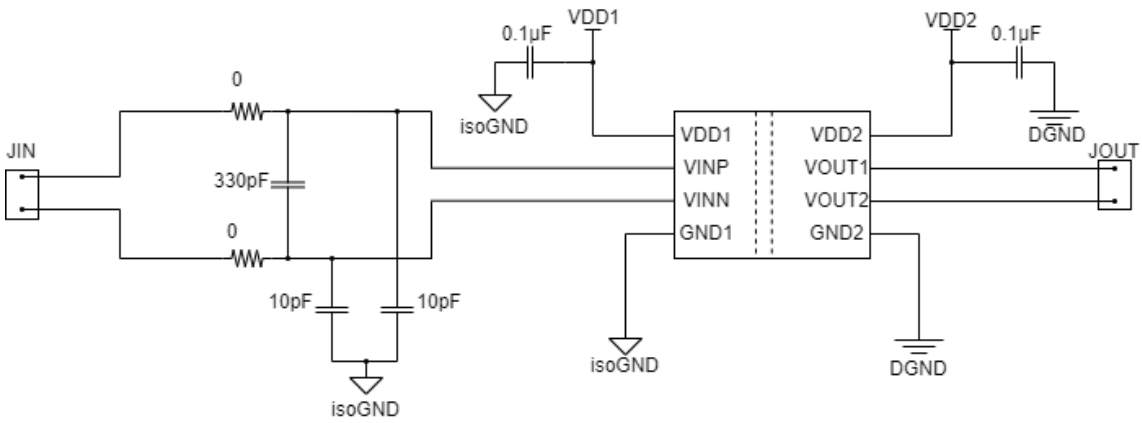

Figure 4.17: Schematic of AMC130xEVM

The schematic of AMC130xEVM is shown in Figure 4.17, where the VDD1 is the input side power supply and the VDD2 is the output side power supply. These two power supplies are supported by two isolated 5 V DC power supplies. The input signal will be connected to the differential input interfaces VINP and VINN after

filtering from the RC network in the Figure. The VOUT1 and VOUT2 are output interfaces and the differential output signal from these two interfaces is passed to the amplifier circuit. Besides the isolation, the AMC130xEVM also has a voltage gain, which is limited and the output current is insufficient to drive the MOSFET at high speed, which requires a minimum 2.5 A gate current according to the experimental results in Chapter 3. In addition the maximum voltage range of the differential output signal is from -2.05 V to 2.05 V, which is insufficient to drive the MOSFET. Therefore, a subsequent amplifier circuit is required to operate the system and will be designed based on this output voltage range.

The maximum range of drive voltage for the MOSFET is from -5 V to 24 V, therefore, the power supply range of the amplifier circuit is from -5 V to 30 V, to ensure the amplifier circuit can output the drive signal with sufficient voltage level. Considering the output voltage range of the isolation circuit, the DC gain of the amplifier circuit should be 12 and the output voltage from the isolation circuit will be from -0.42 V to 2 V. According to the datasheet, the gain of the isolation circuit is 8, therefore the output voltage of FPGA will be set as from -52.5 mV to 250 mV. The power operational amplifier MP111FD is selected to build the amplifier circuit. The MP111FD has multiple advantages, including the low cost, high voltage range, high drive ability, high slew rate and 500 kHz bandwidth [212]. The maximum voltage supply of MP111FD reaches 100 V and it supports the positive and negative dual power supply, which meet the voltage range requirement of the amplifier circuit from -5 V to 30 V. The maximum output continues current reaches 15 A, which is significantly high than the 2.5 A gate drive current requirement outlined previously and is sufficient to drive the MOSFET. To reduce the shut down time, normally the ramp rate of the drive signal of MOSFET will be very fast. The slew rate of MP111FD reaches 130 V/µs, which is higher than the 42 V/µs gate voltage slope of the MOSFET according to the experimental result and is sufficient to support the operation and changing of the drive signal in this study. The amplifier circuit is built based on the MP111FD and the schematic is shown in Figure 4.18.

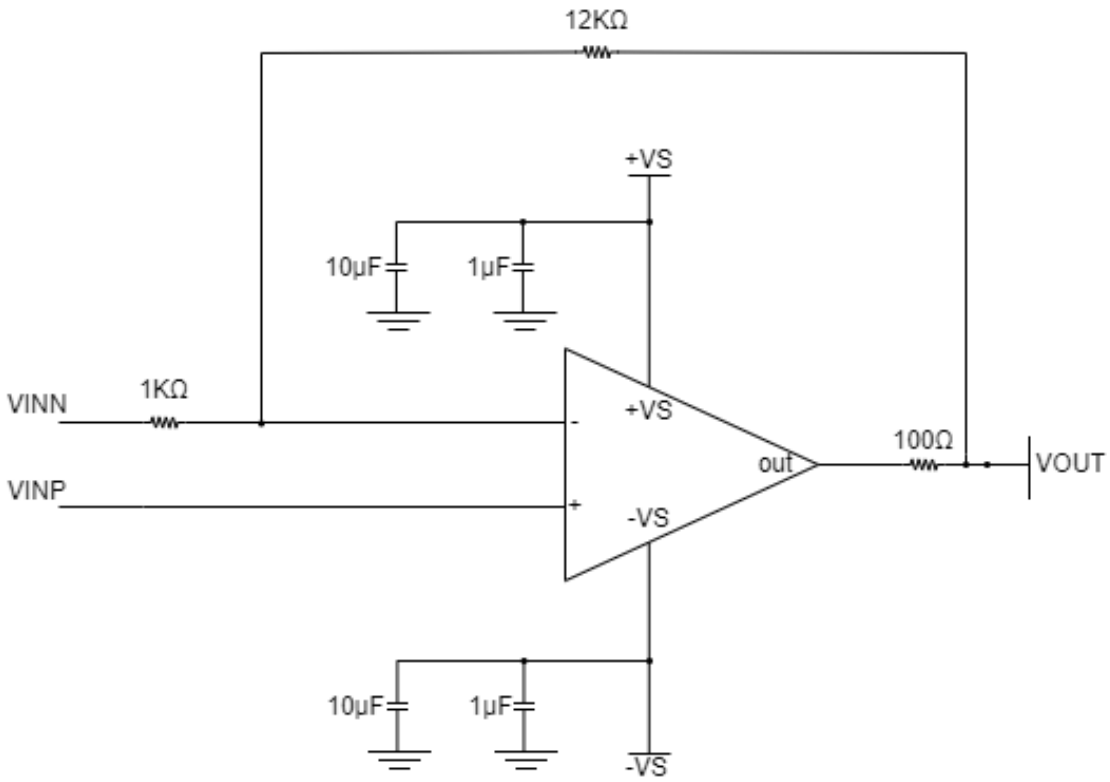

Figure 4.18: Schematic of amplifier circuit

As mentioned before, the drive signals generated by FPGA have three different types, including the linear curve, convex curve and the concave curve. Therefore, the output signals of the amplifier circuit are different and based on the signals from the FPGA. The drive signals of linear, convex and concave are shown in Figures 4.19, 4.20 and 4.21 separately.

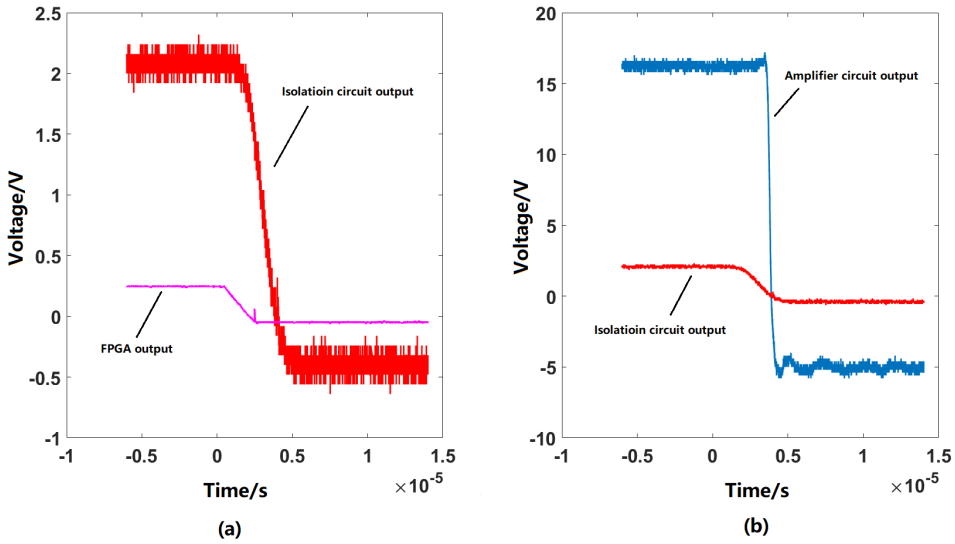

Figure 4.19: Amplifier linear output, (a) the FPGA output and the isolation circuit output, (b) the isolation circuit output and the amplifier circuit output

The waveforms in Figure 4.19 (a), 4.20 (a) and 4.21 (a) show the relationship between the FPGA output, which is denoted by the purple curve and the isolation circuit output, which is shown by the red curve. Meanwhile, Figures 4.19 (b), 4.20 (b) and 4.21 (b) show the relationship between the isolation circuit output, which is shown by the red curve and the amplifier circuit output, which is shown by the blue curve. The voltage of the amplifier circuit output changes from -5 V to 16 V, which is sufficient to drive the MOSFET correctly. The delay between the FPGA output and the isolation circuit output is around 1 μs and that between the isolation circuit output and the amplifier circuit output is around 1.5 μs, which are shown in Figure 4.22 (a) and (b) separately. Therefore, the total delay of the drive signal is less than 2.5 μs, which meets the design requirement that the delay of the control system has been less than 16 μs according to the short circuit test result in Chapter 3. In conclusion, in this section, the isolation circuit realises the isolation of the low voltage FPGA signal from the high voltage drive signal, and transforms the analog signal from the low voltage side to high voltage side, which is the key point to output the different drive signal curves. Meanwhile, the amplifier circuit ensures the voltage of the drive signals is sufficient to drive the MOSFET. The design of the isolation circuit and the amplifier circuit meet the requirement of the control system.

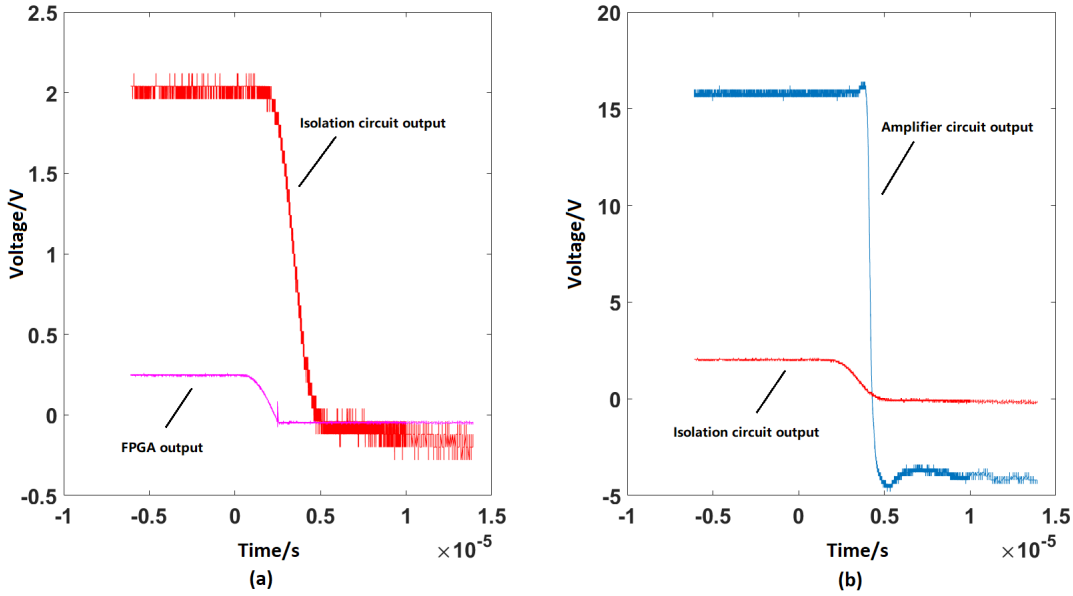

Figure 4.20: Amplifier convex output, (a) the FPGA output and the isolation circuit output, (b) the isolation circuit output and the amplifier circuit output

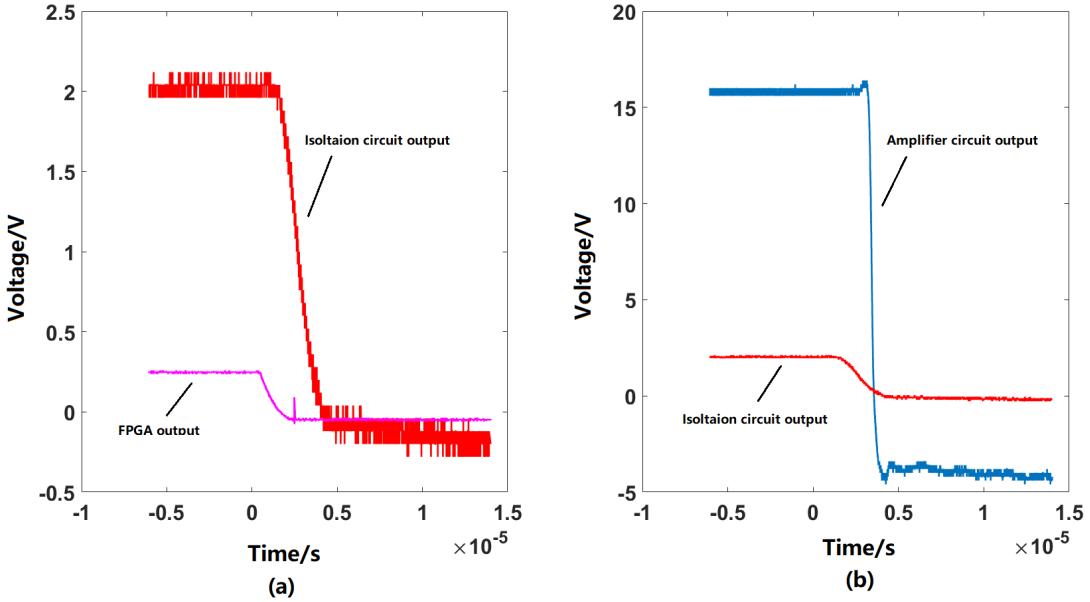

Figure 4.21: Amplifier concave output, (a) the FPGA output and the isolation circuit output, (b) the isolation circuit output and the amplifier circuit output

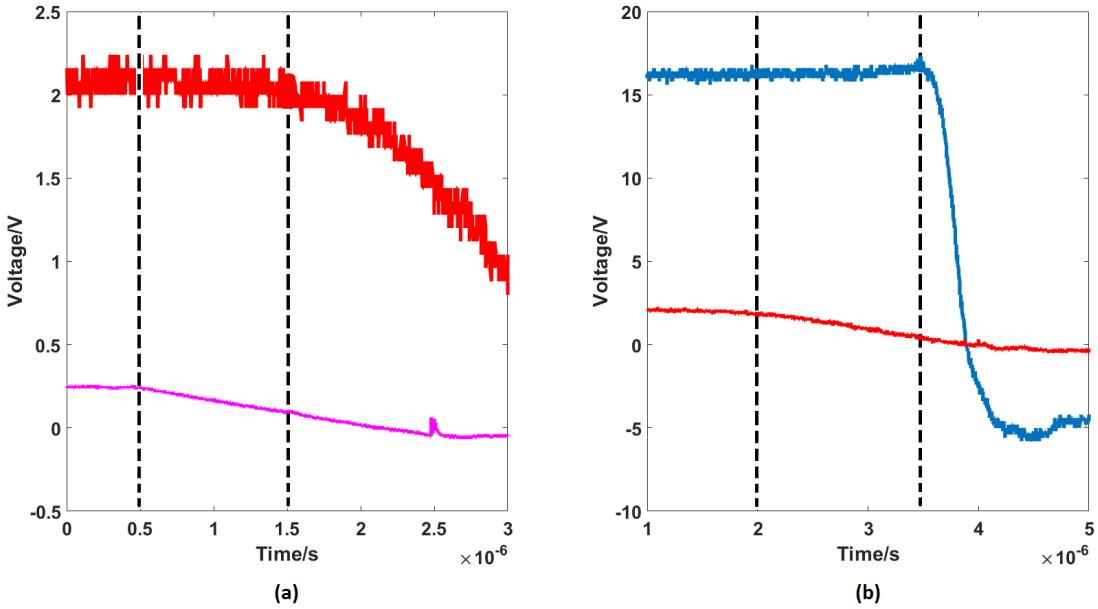

Figure 4.22: Amplifier output delay, (a) the FPGA output and the isolation circuit output delay, (b) the isolation circuit output and the amplifier circuit output delay

4.4 Experimental validation

As shown in Figure 4.14, the control system is designed to generate three different types of the control signals, including the linear, convex and concave, each of which can operate with different frequency word, which is used to control the transform time of the FPGA output. To minimum the short circuit time of the MOSFET, the maximum transform time of FPGA output is set to 2 µs. According to equation 4.6, the frequency word is 5, and the transform time of FPGA output can be decreased by increasing the frequency word. The FPGA output is amplified to drive the MOSFET and the amplifier circuit with large slew rate can further decrease the transform time. Therefore, the transform time of the amplifier circuit output is shorter than that of the FPGA output with the same frequency word. Experimental validation of amplifier circuit output drive signals will be described in this section.

The results of the linear drive signal are shown by the data in Figure 4.23. In the Figure, the blue curve is the linear drive signal with 5 frequency word; the red curve is the linear drive signal with 6 frequency word, and the yellow curve is the linear drive signal with 7 frequency word. The start time and the end time of the

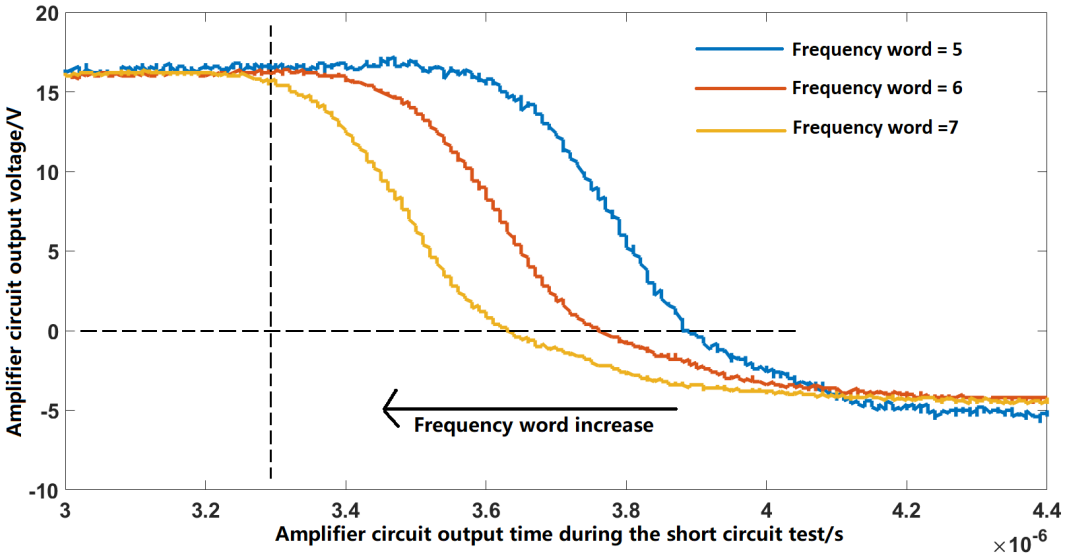

Figure 4.23: Linear amplifier circuit output with frequency word 5,6 and 7

transformation processing for three linear curves with different frequency word are almost identical, varying between 3.3 μs and 4.1 μs. The observed transformation time in the data is around 0.8 μs. Considering the control system has around 6 μs delay and the maximum short circuit withstand time of the MOSFET is 16 μs, according to previous experimental data, the 0.8 μs transform time of the drive signal is short enough to protect the circuit from the fault current. With the increase of the frequency word, the slope of the drive signal will rise and it can be seen from the data that the curve with 7 frequency word drops to 0 V more rapidly than the curve with 6 frequency word, while the curve with 5 frequency word is the slowest. The start time point of the curves begin to drop are all around 3.3 μs. The yellow curve with 7 frequency word takes 0.3 μs to drop to 0 and the red curve with 6 frequency word takes 0.5 μs to drop to 0. The slowest blue curve with 5 frequency word takes 0.6 μs to drop to 0.

The results of the convex drive signal are shown by the data in Figure 4.24. In the Figure the blue line is the convex drive signal with 5 frequency word; the red curve is the convex drive signal with 6 frequency word, and the yellow curve is the convex drive signal with 7 frequency word. The start time and the end time of different frequency word convex curves are different. For the curve with 5 frequency word, the start time is around 3.9 μs and the end time is around 4.6 μs, resulting

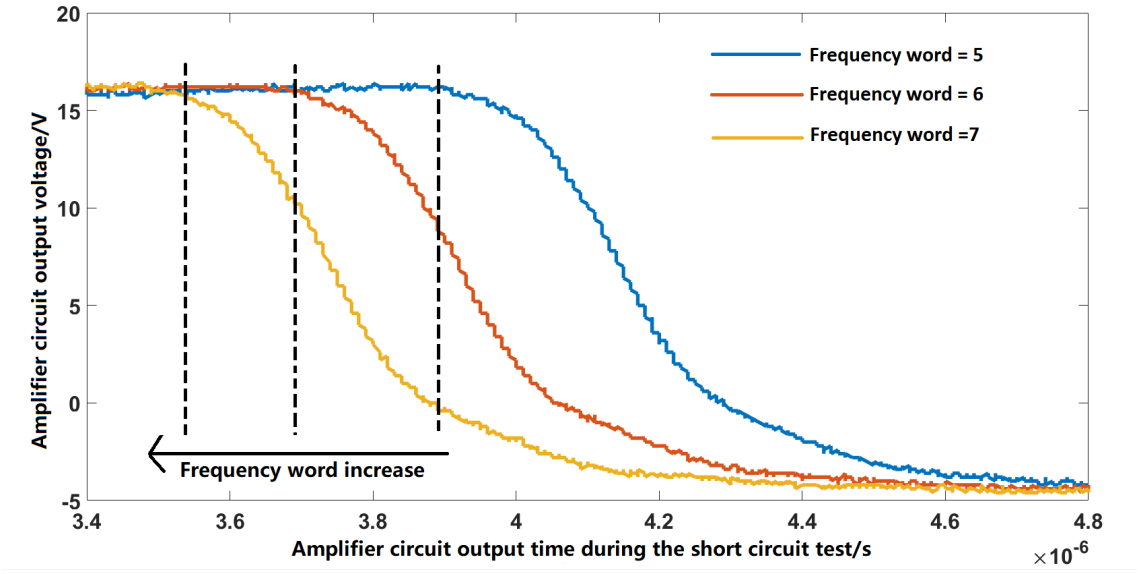

Figure 4.24: Convex amplifier circuit output with frequency word 5,6 and 7

in the transformation time for 5 frequency word curve of around 0.7 μs. For the curve with 6 frequency word, the start time is around 3.7 μs and the end time is around 4.3 μs, resulting in the transformation time for 6 frequency word is around 0.6 μs. For the curve with 7 frequency word, the start time is around 3.55 μs and the end time is around 4.1 μs, with a transformation time for the 7 frequency word curve being around 0.55 μs. The actual start time of these convex curves from the FPGA output are identical. However, at the beginning of the convex curve, the change in the voltage level is minor. Therefore, the change in the amplifier output is insignificant at the beginning of the transition. The larger frequency word results in a more rapid transition and the time of the 7 frequency word curve remaining at 16 V is shorter in comparison to that of other two curves. The curve with larger frequency word also reaches 0 V more rapidly.

The results of the concave drive signal are shown by the data in Figure 4.25. In the Figure the blue curve is the concave drive signal with 5 frequency word; the red curve is the concave drive signal with 6 frequency word, and the yellow curve is the concave drive signal with 7 frequency word. The start time of the transformation for the three curves are around 3.1 μs and the end time is around 3.8 μs. The transformation time is around 0.7 μs. Similar to the data for both the linear and convex curves, the concave curve with larger frequency word reaches 0 more rapidly.

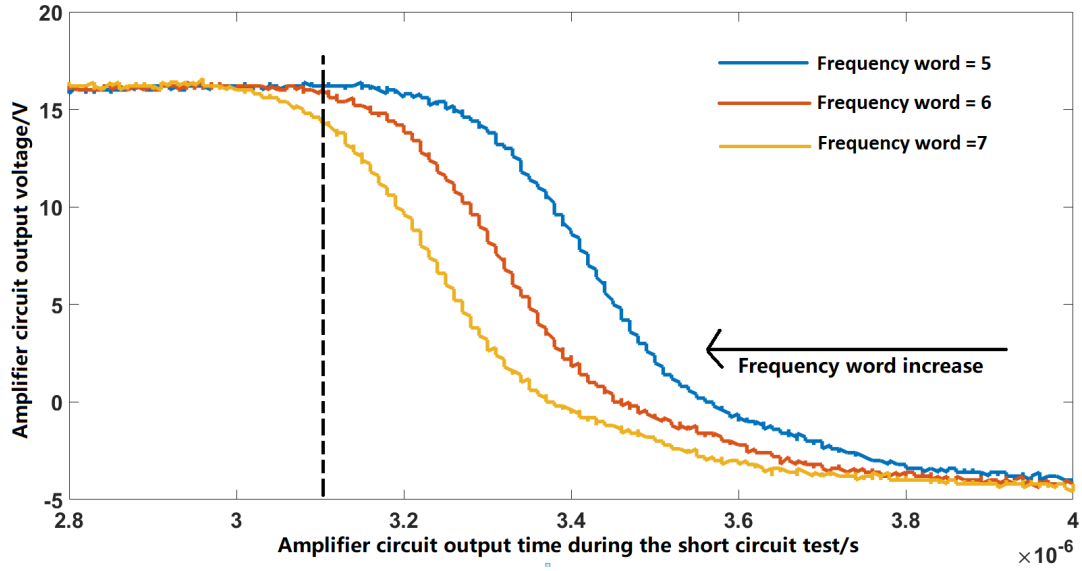

Figure 4.25: Concave amplifier circuit output with frequency word 5,6 and 7

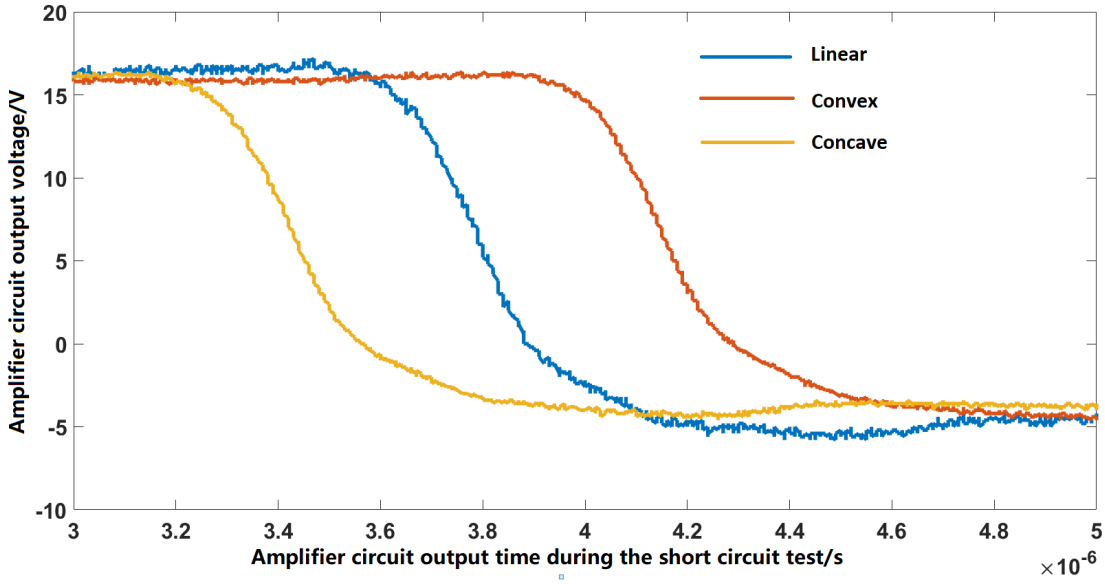

Figure 4.26: Direct comparison of linear, convex and concave drive signal with 5 frequency word

The differences for the same type of curve with different frequency word has been described in this section, and the comparison of three different types of curve with same frequency word is also important to show the impact of different types of curve to the transform drive signal. A direct comparison between the three waveforms is shown by the data in Figure 4.26. Because of the characteristics of the curve, the voltage change of the concave curve is the fastest, which is followed by the linear curve, and the convex is the slowest one. Therefore, the time of the linear curve remaining at 16 V is around 0.4 μs longer than that of the concave curve, and the time of the convex curve remaining at 16 V is around 0.4 μs longer than that of the linear curve. With the same frequency word, the slope of the concave curve is the largest and the concave curve reaches the 0 V faster than others; the slope of the convex curve is the slowest and it takes the longest time to reaches the 0 V.

In conclusion, the control signal from the amplifier circuit is clear and the voltage level is suitable to drive the MOSFET. For the same type of the curves, the curve with larger frequency word has a larger slope, however the total transformation time is similar. For the curves with the same frequency word, the concave curve changes faster than the linear curve and it is followed by the convex curve. Meanwhile, the curves remain the characteristics of the concave, linear and convex separately. According to the design, the transform time is controlled by frequency word, and the longest transform time of design is 2 μs when the frequency word is 1. In addition, a larger frequency word results in the shorter transform time and the transform time is equal to the calculation result of 2 μs divided by the frequency word.

4.5 Conclusion

In conclusion, the novel drive signal has been designed and verified in this Chapter. Meanwhile, the control system is introduced. The novel drive signal is generated by FPGA, and the shape and frequency word can be controlled by programming. To drive the MOSFET, the control system has the isolation circuit to protect the drive circuit from the fault in main circuit, and the amplifier circuit to amplify the voltage. To increase the reaction speed and reliability of the control system, both threshold

judgement and slope judgement are used in the control system. The performance and drive ability of the novel drive signal has been verified, and the it has a short delay which reaches 2.5 μs.

CHAPTER 5

The performance of the novel drive signals in short circuit test

5.1 Introduction

The main objective of this Chapter is the test and evaluation of the performance of the three different drive signals, to determine the optimum conditions for a range of different MOSFETs, and to identify the best drive signal to minimise the short circuit time and overcurrent in a SSCB circuit. Firstly, the short circuit test platform is similar to that described in Chapter 3, with the addition of a feedback control system to detect the main circuit working condition and control the blocking of the MOSFET. Two detection methods used here, including current shunt and voltage divider detection. The feedback signal is collected by the FPGA, which generates the correct drive signal, which is amplified by the operational amplifier circuit to control the Gate-Source voltage of the MOSFET.

To compare the performance of different drive signals and identify the optimum settings, multiple tests are described in this Chapter, which includes the evaluation of the different types of drive signals, including the linear, convex and concave, determination of the different transform time of the MOSFET controlled by frequency word, the test of two different detection methods, including the current shunt and

voltage divider, and the system performance when used with three different SiC MOSFETs from the same family, including 12M1H030 ,12M1H045 and 12M1H090. As mentioned in Chapter 4, the maximum FPGA output transform time is set to 2 μs, which corresponds the frequency word 5, according to equation 4.6. To obtain the short circuit performance of MOSFETs with the faster and slower FPGA output transform time, the frequency word used in this Chapter is between 4 and 10, corresponding the FPGA output transform time between 2.5 μs and 1 μs.

To evaluate the performance, the short circuit time, the impact of overcurrent and the reliability of control signal are the key parameters to compare and analyses, and these parameters can be obtained from the Drain current waveform during the shut down transient. The control system has a start time, which is the time after the short circuit event that the Drain current begins to drop. The end time, which is the time that the current drops to zero, and the shut down time, which is the whole time that the current takes to drop from the onset of the fault condition. Because the end time is equal to the short circuit time plus the delay of the IGBT drive signal, which is fixed 0.5 μs, and the short circuit time is required to be minimised in SSCB, the drive signal with the shortest end time will have the shortest short circuit time, resulting in a better short circuit performance. However, the shorter short circuit time results in a higher overcurrent. As introduced in Figure 3.3, when the MOSFET is driven by pulse, which has the shortest transform time and largest frequency word, the overcurrent results in the significant oscillation when the MOSFET shut down. Therefore, the novel drive signal introduced in this thesis which can minimum the short circuit time ,and the overcurrent to ensure the MOSFET Drain current has no oscillation when it is shut down. In addition, the reliability of the control system is also important, and variation in the end time for different drive signals with different frequency word is calculated to evaluate the reliability of the control system.

5.2 Test platform

The first step of the experiment is the optimisation of the short circuit test platform that was described in Chapter 3, the schematic for which is shown in Figure 5.1. The

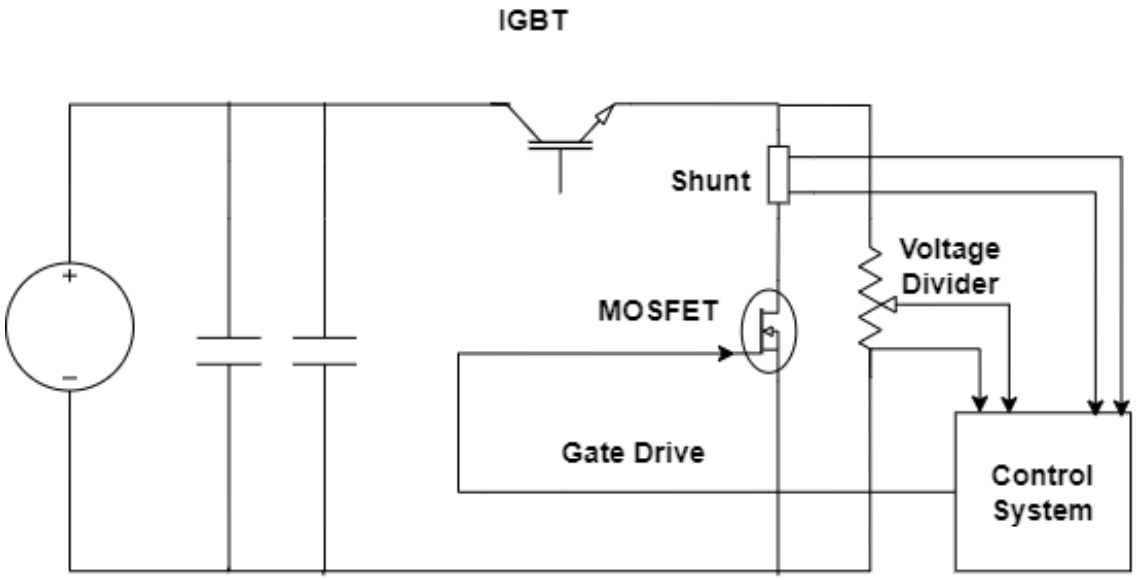

Figure 5.1: Short circuit test platform schematic

test platform is composed of the DC power supply, two capacitors, the MOSFET under test, an IGBT, current shunt, voltage divider and the control system designed in section 4.1. The DC power supply and the capacitors are identical to those in the test platform introduced in Chapter 3, and the SiC MOSFETs used in the initial testing are the 12M1H030, with 1200 V rated voltage and 30 mΩ on resistance, the 12M1H045, with 1200 V rated voltage and 45 mΩ on resistance, the 12M1H090, with 1200 V rated voltage and 90 mΩ on resistance. The IGBT is used as a switch to initiate the short circuit test. As mentioned in Chapter 4, the control system requires two feedback signals to detect the working conduction of the main circuit, therefore, in this Chapter, a current shunt is used to detect the Drain current through the MOSFET and a voltage divider is used to detect the Drain-Source voltage of the MOSFET. The control system will generate the corresponding drive signal to control the MOSFET gate, depending on the condition of the circuit. As shown in Figure 5.1, the current shunt is series connected with the MOSFET, and the voltage divider is paralleled with the MOSFET and current shunt. This topology has two advantages, one is the current detected by the current shunt is the current through the MOSFET, another is the ground of the MOSFET and the voltage divider are both connected to the negative point of the DC power supply, which increases the accuracy of the voltage and current detection and reduces the noise

when the MOSFET is blocked. However, the topology also has a drawback, which is the voltage detected by the voltage divider is not purely the voltage across the MOSFET. When the MOSFET is blocked, there is no current through the current shunt and the voltage detected by the voltage divider is the Drain-Source voltage of the MOSFET, which is equal to the voltage of the DC power source. When the MOSFET is conducting, the on resistance of the MOSFET is 30 mΩ and the resistance of the current shunt normally is 1 mΩ, therefore the error between the Drain-Source voltage and the voltage detected by the voltage divider is expected to be 3.33%. The DC power source is 270 V and the error voltage is 8.99 V. The error voltage collected by ADC is 0.8 V which is less than 1 V. Therefore, the limitation of this topology is acceptable and the advantages are significant as well have be described in this section, which are the reason why the topology is used in this Chapter.

5.2.1 Current shunt and voltage divider circuit

To detect the Drain-Source current, a current shunt is series connected with the MOSFET. According to the experimental results in Chapter 3, the peak value of the short circuit current is around 230 A. However, the stable short circuit current of the shunt used in this work is quoted to be 100 A and because the control system will shut down the MOSFET in several microseconds, the current shunt will withstand the short current current for this duration. Therefore, a 60 A 60 mV current shunt is selected to detect the Drain-Source current in this work. The output from the current shunt will be sent to the ADC and used to determine the working condition of the main circuit, therefore, the accuracy has to be considered. Because the maximum output voltage from the current shunt under rated conditions is 60 mV, which is difficult to detect by the ADC and calculations based on 1 mV changes in voltage, resulting from a 1 A current change in the main circuit, an amplifier circuit is used to improve the sensitivity of the current feedback signal. In addition, the short circuit current through the main circuit is significantly larger than that through the ADC and control circuits, therefore, the current shunt cannot be directly connected with the ADC and a isolation circuit is required for safety purposes. The schematic

of the current shunt circuit is shown in Figure 5.2.

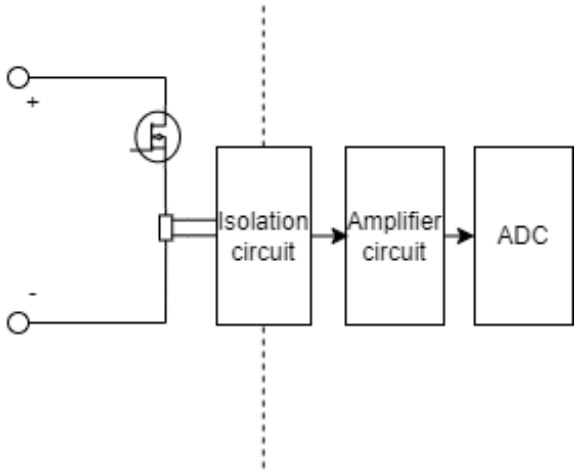

Figure 5.2: The schematic of the current shunt circuit

Because the input and output of the isolation circuit are both analog signals, the TTL digital isolation circuit cannot be applied in the current shunt circuit design, and the analog-to-analog isolation board AMC130xEVM is used to isolate the feedback current signal from main circuit, which has been introduced in Chapter 4. According to the short circuit test result in section 3.3, the maximum fault current is around 230 A, and the maximum output voltage from the current shunt will be 230 mV, which is lower than the 250 mV input voltage limit of the AMC130xEVM. Therefore, the AMC130xEVM is suitable for the current shunt isolation circuit. The gain of the AMC130xEVM is 8, therefore, the output voltage of the isolation circuit is 480 mV when the output voltage form the current shunt is 60 mV. However, 480 mV is challenging for the ADC to detect small current changes in the main circuit and the amplifier circuit is expected to amplify the voltage to the input voltage limitation of the ADC which is -25 V to 25 V. Therefore, the gain of the amplifier circuit is designed to be 50 and the output voltage from the amplifier circuit will be 24 V when the short circuit occurs and the Drain current increases sharply.

To increase the reaction speed, the slew rate of the operational amplifier should be large enough to limit the voltage rising time of current shunt circuit within 1 μs. In addition the gain bandwidth product should be also as large as possible to increase the voltage rising speed of the amplifier output. Therefore, OPA637AU is selected to build the amplifier circuit in this Chapter, which has 135 V/μs slew

rate and 80 MHz gain bandwidth product. The schematic of the amplifier circuit is shown in Figure 5.3. The amplifier circuit is supplied by a 24 V single DC power supply to limit the output voltage of amplifier circuit within the ADC input voltage range, which is 25 V. Two decoupling capacitors are used to ensure the stability of the power supply during operation.

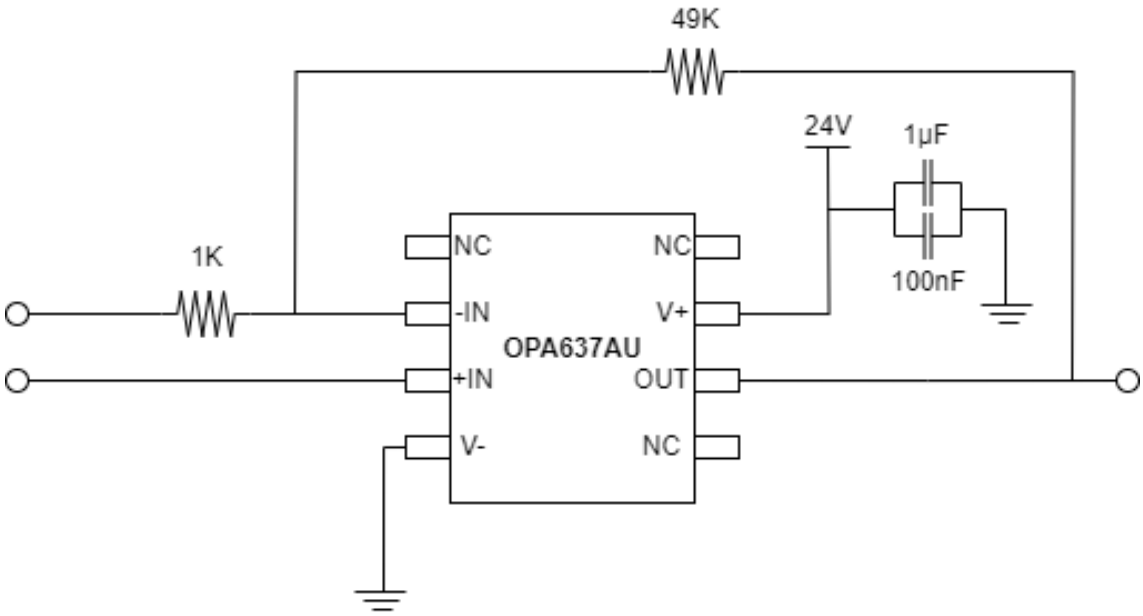

Figure 5.3: OPA637AU amplifier circuit

The voltage divider is used in this Chapter to detect the voltage across the MOSFET. To protect the test circuit when the MOSFET turns off and ensure the majority of current will flow through the MOSFET when it is turned on, the voltage divider must have a significantly large resistance value compared with the on resistance of the MOSFET and the current shunt resistance. Therefore, a Caddock 1776-C681 voltage divider which is specified as 1:999, with 10 MΩ total resistance value and 0.1 % absolute tolerance, is used in this Chapter to detect the Drain-Source voltage of the MOSFET. For safety and the stability of the control system, the voltage divider also requires an isolation circuit to isolate the ADC with the main circuit. However, the voltage divider with large resistance brings a large input impedance to the isolation circuit and this amplifies the drift voltage so that it exceeds the threshold voltage, which makes the feedback system cannot work correctly. Therefore, the voltage divider circuit does not incorporate an isolation circuit and

is directly to the amplifier circuit. Remove the isolation circuit results in the risk that the overcurrent from the main circuit may destroy the amplifier circuit. It is the compromise for the correct work of control system. The voltage divider will divide the 270 V Drain-Source voltage into 270 mV, and the feedback voltage will be amplified to 24 V by amplifier circuit before being sent to the ADC.

5.2.2 Power amplifier circuit

To protect the FPGA, there should be an isolation circuit between the FPGA and the power amplifier circuit, however, the isolation circuit significantly increased the noise which interferes with the detection of the short circuit event by the FPGA and hence interferes with the control of the MOSFET. Therefore, the isolation circuit between the FPGA and the power amplifier circuit is removed. The new power amplifier circuit is still based on the MP111FD and the revised schematic is shown in Figure 5.4.

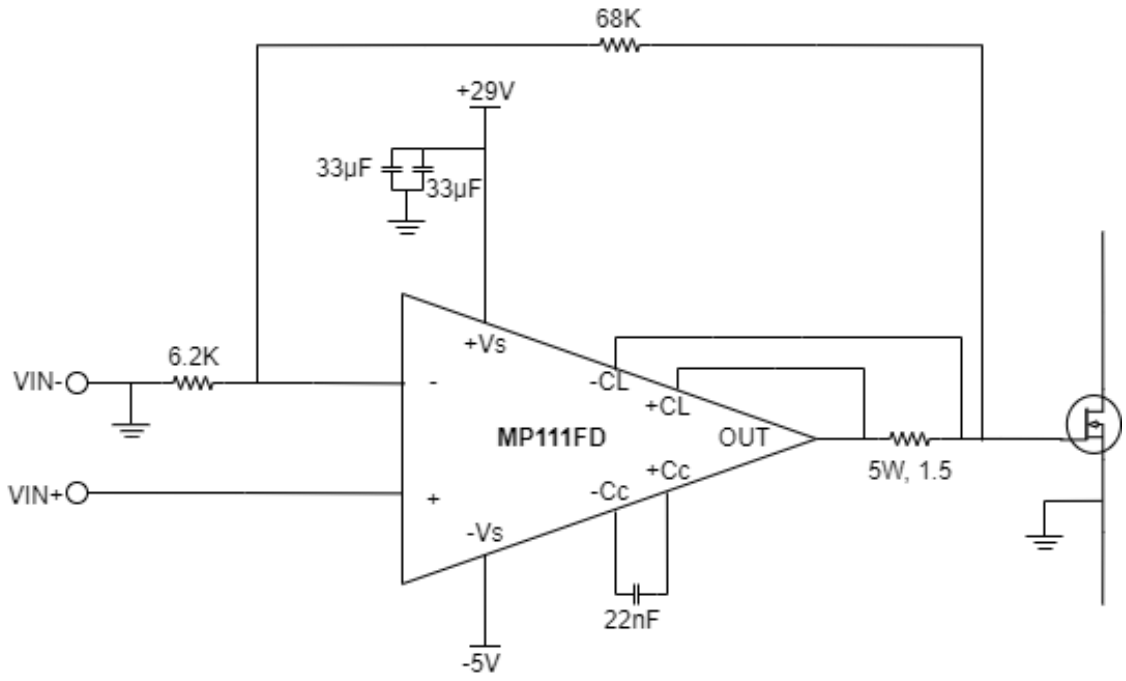

Figure 5.4: Power amplifier circuit

The power supply for the power amplifier circuit is -5 V and 29 V. Two 33 μF capacitors are used to decouple the power supply. A 5W, 1.5 Ω power resistor is used

to limit the output current and the 22 nF capacitor is used as the compensation capacitor. The gain of the power amplifier is designed to be 11 and the output voltage can be controlled by settings in the FPGA DAC. The output voltage from the FPGA is set to -0.4 V to 2.4 V to ensure the voltage of the drive signal reaches -5 V to 22 V, which is higher than the 18 V MOSFET threshold voltage [184], to conduct and block the MOSFET.

5.3 Result and analysis

Because the isolation circuit is required for the current shunt detection but cannot be used in the voltage divider detection, the test result of these two detection methods will be analysed separately in this section, and the analysis of the experimental waveforms from the short circuit test will be described. Because the power supply needs several seconds to charge the capacitor to 270 V and the rise time of the drive signal from power amplifier circuit is typically several milliseconds, the DC power supply and the MOSFET cannot be used to initiate the short circuit test. Therefore, the IGBT is used as a switch to start the short circuit test, which is similar to the conditions in a half-bridge inverter. The IGBT is the upper device and the MOSFET is the lower device. When both devices conduct at the same time, the short circuit fault occurs. Firstly, the DC power supply will be turned on to charge the capacitors and the feedback control system is initialed. Then the FPGA will generate the normal signal to set the Vgs to 22 V to ensure the MOSFET is operating in conducting mode. Finally the IGBT will be turned on by a 8 μs pulse, which is shorter than the maximum short circuit withstand time of the MOSFET according to the results in section 3.3, to start the short circuit test and protect the test platform should the control system fail to block the MOSFET within a reasonable time.

The test results show the effectiveness of two detection methods, including the current shunt detection and voltage divider detection, three different MOSFETs, including 12M1H030 (Ron=30 mΩ), 12M1H045 (Ron=45 mΩ), and 12M1H090 (Ron=90 mΩ), three different drive signals, including the linear, convex and concave

control, and different frequency word from 4 to 10.

5.3.1 Current shunt detection results

Overview of the current shunt detection

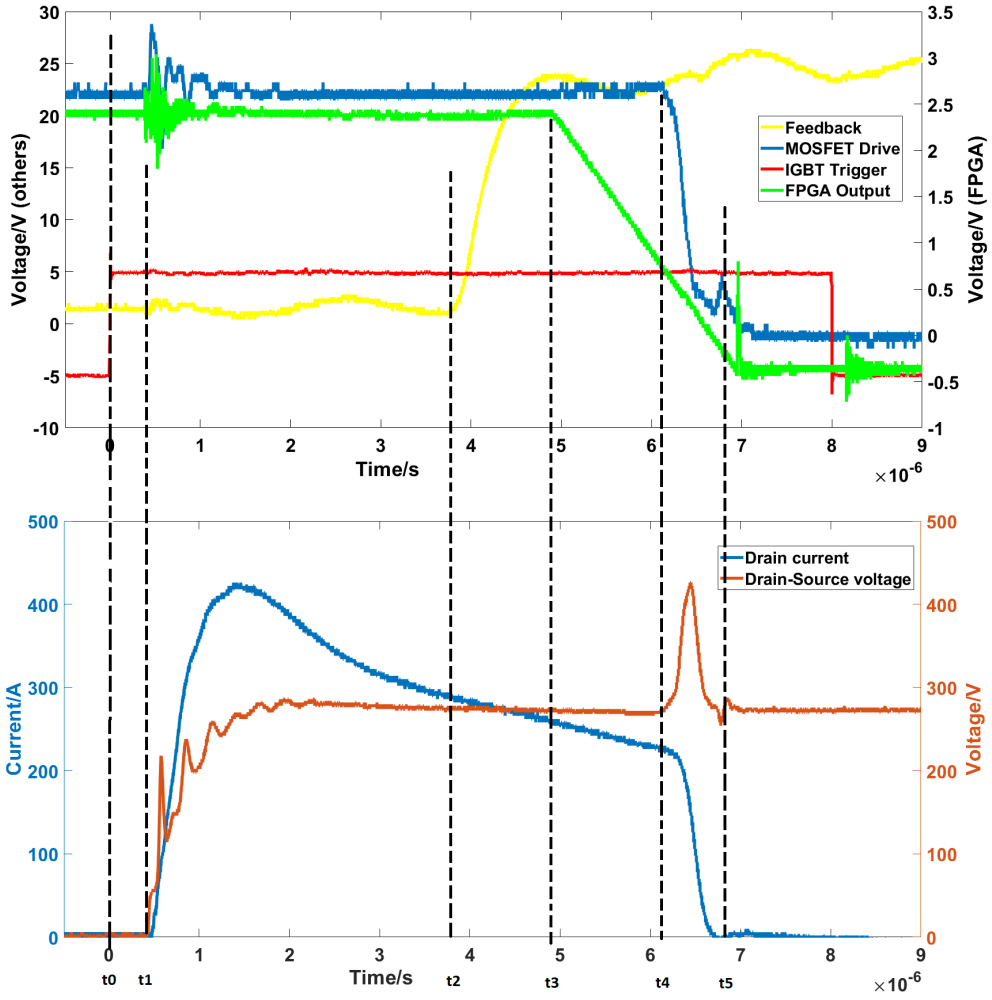

Figure 5.5: Short circuit test data for current shunt detection

The short circuit test data for current shunt detection and the performance of the control system is shown by the data in Figure 5.5. At t0, the IGBT trigger signal triggers the drive circuit of the IGBT. At t1, the IGBT starts to conduct and initiates the short circuit test. The time period t1-t0 is the delay caused by IGBT drive circuit, which is 0.5 μs. The short circuit test results in the significant rise of the Drain current and Drain-Source voltage of MOSFET. The Drain current reaches

430 A and Drain-Source voltage reaches 270 V, within 1 μs. Therefore, the voltage across the current shunt rises to allow determination of the working condition of the main circuit at time t2, and the feedback signal collected by ADC begins to rise. The voltage across the current shunt passes through the isolation board and the amplifier circuit, and the result in delay is large and reaches 3.3 μs as shown in Figure as t2-t1. At t3, the FPGA begins to generate the transform signal that will control the behaviour of the MOSFET. The time t3-t2 is the delay caused by the rise time of the amplifier output voltage and the delay of FPGA, which is around 1 μs, because the feedback signal requires time to reach the threshold which is used to judge the working condition of main circuit. At t4, the MOSFET drive signal generated by the power amplifier circuit begins drop and the time t4-t3 is the delay of the power amplifier circuit, which is around 1.2 μs. The Drain current through the MOSFET is blocked at t5 where the Drain current drops and remains 0 and the Drain-Source voltage remains 270 V because the IGBT is still conducting. The time t5-t4 is the shut down period of the MOSFET which is around 0.7 μs. The shut down time of the MOSFET is significantly larger than the data shown in datasheet, which is 13 ns [184], because the working condition is different. The Drain current begins blocking when the Gate-Source voltage of the MOSFET falls below the 18 V threshold voltage which occurs after t4, and the voltage waveform shows a spike at the same time which reaches 420 V caused by the internal inductance of the test platform. The total delay of the current shunt detection, from the time t1 to the time when the Drain current begins to drop, is around 6 μs.

Results of 12M1H030

The FPGA drive signal and Drain current of the 30 mΩ MOSFET driven by a linear control signal with different frequency word is shown by the data in Figure 5.6. The time that linear drive signal begins to drop is around 4.88 μs from the initiation of the short circuit test. The drive signals from the FPGA are all designed with an identical shut down start time, however, the Drain current will begin to drop significantly when the drive signal falls below the MOSFET threshold voltage, and different frequency words result in the drive signals that have different rate of decrease which

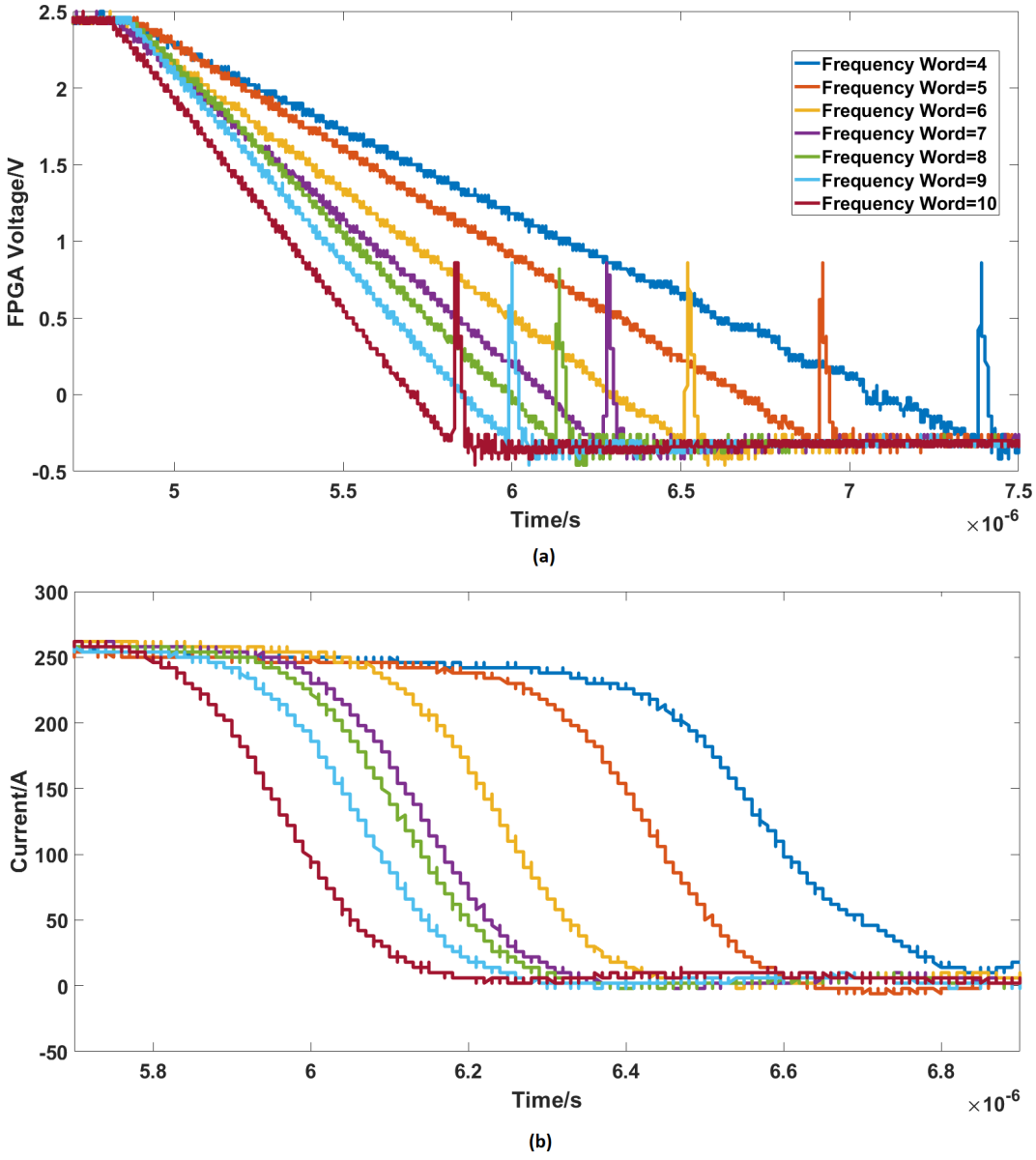

Figure 5.6: Test results of 12M1H030 driven by linear control signal with the frequency word from 4 to 10 and current shunt detection, (a) FPGA output, (b) Drain current

results in the time required for the drive signals drop to below the threshold voltage being different. Hence the shut down start time for the Drain current is different for different frequency words. Comparing with the short circuit test results shown in Chapter 3, Figure 3.3, the MOSFET driven by pulse signal, with the largest frequency word, has the huge overcurrent which results in the oscillation of Drain current when the MOSFET shut down. As shown in Figure 5.6, the MOSFET driven by novel drive signals, with the smaller frequency word compared with the pulse signal, has less overcurrent and there is no oscillation of Drain current when the MOSFET shut down. Therefore the larger frequency word results in the larger overcurrent.

A summary of the results for the 30 mΩ MOSFET shut down time under linear drive signal with different frequency word is shown in Table 5.1 and Figure 5.7. The start time is the time when the Drain current begin to drop and the end time is the time when the Drain current reaches zero. The shut down time is the difference between the initiation of the Drain current shut down to the end of the shut down time. The FPGA output has a spike when drop to -0.4 V because the FPGA takes a short time to transform the drive signal from transform state to error state. Before the drive signal state change finished, the FPGA output will remain as transform state. However, the last value saved in look up table has been output and the output starts from the first value automatically, which results in the spike. The spike can be removed by the isolation circuit and has no impact on the Drain current.

Frequency word	4	5	6	7	8	9	10
Start time	6.40 μs	6.25 μs	6.10 μs	6.00 μs	5.95 μs	5.90 μs	5.80 μs
End time	6.85 μs	6.60 μs	6.42 μs	6.35 μs	6.30 μs	6.25 μs	6.20 μs
Shut down time	0.45 μs	0.35 μs	0.32 μs	0.35 μs	0.35 μs	0.35 μs	0.40 μs

Table 5.1: Shut down time of 12M1H030 under linear drive signal with different frequency word and current shunt detection

According to the data, when the 30 mΩ MOSFET gate is driven by a linear signal, increasing the frequency word, results in the start time and end time of the shut down process both decreasing, and the decrease for frequency word below 6 is sharper than over 6, as the drop speed before frequency 6 is faster than 0.1 μs/frequency word, and the drop speed after frequency 6 is slower than 0.1 μs/frequency word.

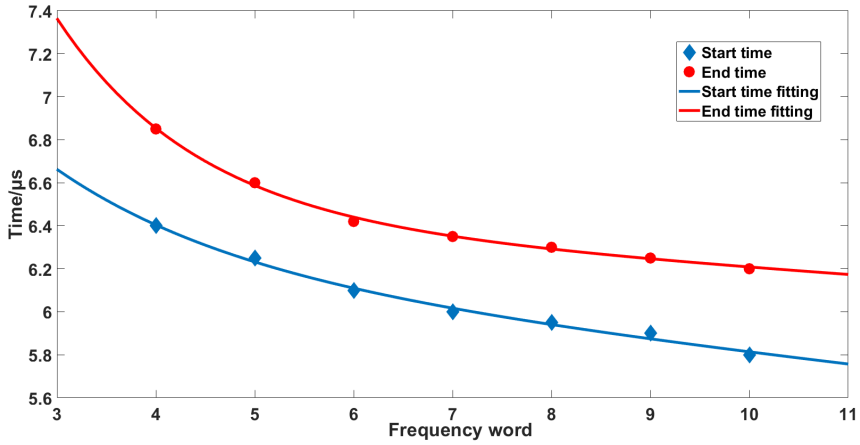

Figure 5.7: Comparison of 12M1H030 shut down time under linear drive signal with different frequency word and current shunt detection

Therefore, increasing the frequency word can improve the short circuit performance of 30 mΩ MOSFET under linear drive signal before the frequency word reaches 6 and has a little improvement after that. Meanwhile, as can be seen from the data, the average shut down time under linear control with different frequency word is 0.37 μs. The standard deviation can be calculated by equation 5.1, which is 0.04, and the coefficient of variation can be calculated by equation 5.2, which is 0.11. Because the standard deviation is small, the dispersion of the 30 mΩ MOSFET shut down time under linear drive signal with different frequency word is not significant and the frequency word has no impact on the 30 mΩ MOSFET shut down time under the linear drive signal control.

$$\sigma = \sqrt{\frac{\sum_{i=1}^{n}(T_{\mathrm{i}} - \mu)^2}{n}} \tag{5.1}$$

where σ is standard deviation, n is the number of shut down time, μ is the average shut down time and T is the shut down time.

$$C_{\mathrm{v}} = \frac{\sigma}{\mu} \tag{5.2}$$

where C_{v} is coefficient of variation, σ is standard deviation and μ is the average shut down time.

To compare the short circuit performance of three different drive signals, the same

test and evaluation of convex and concave drive signal are applied on 12M1H030.

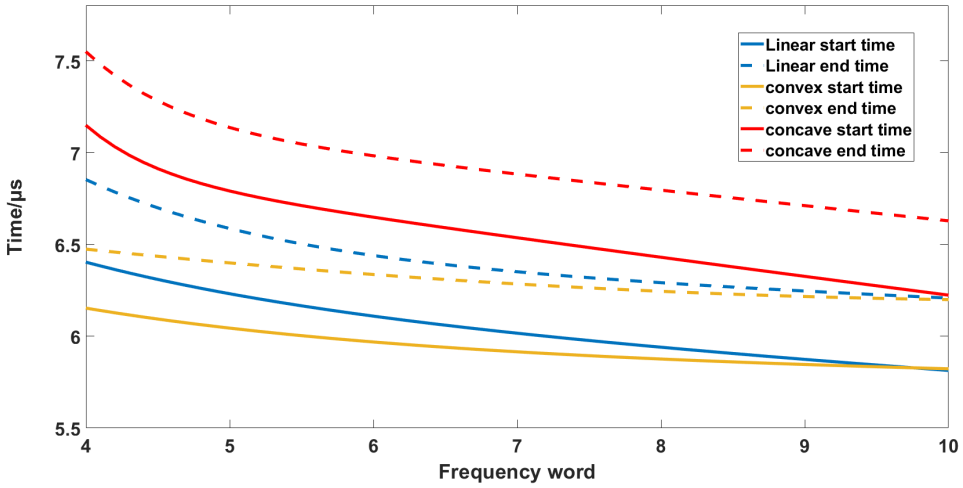

Figure 5.8: Fitting curve of 12M1H030 shut down time under linear, convex and concave drive signal with different frequency word and current shunt detection

The frequency word of the drive signals can be changed flexibly, however, the number of frequency word that can be utilised in the experiments reported in this Chapter is limited. Therefore, the fitting curve of 12M1H030 Drain current shut down time under three different drive signals, including linear, convex and concave, with different frequency word have been summarised in Figure 5.8 to predict the trend of Drain current shut time of the 12M1H030 MOSFET as a function of frequency word between 4 and 10, to directly compare the performance of three different drive signals. With the increase in the frequency word, the start time and end time of the shut down process decreases for all three waveforms, meanwhile, the shut down time remains stable under three drive signals. Therefore, the shut down time of the 12M1H030 will not be impacted by the change of frequency word and drive signal. The end time is proportional to the maximum time short circuit time which is an important parameter to evaluate the performance of SSCB based on SiC MOSFETs. When the frequency word below 6, the end time of linear, convex and concave are all significantly higher than that when the frequency word is higher. Meanwhile, the decrease in the start and end time driven by concave signal is faster than that driven by linear signal. That driven by convex signal is the slowest, when the frequency word below 6. Therefore, the frequency word below 6 is not

the optimum selection for the drive signal to control the blocking of the 12M1H030 MOSFET when used in SSCB applications. In contrast, the higher frequency word results in higher overcurrent when the MOSFET starts blocking, which will reduce the performance and long term reliability of SSCB. Therefore setting the frequency word to 6 is the optimum selection for 12M1H030 under all three drive signals when considering the balance of the overcurrent and the short circuit blocking time.

As for the drive signal, the time when the linear drive signal begins to drop is 4.88 μs, which is shorter than that for the convex drive signal, which is 5.00 μs, and the start time of concave drive signal is the longest, at 5.12 μs. However, because the speed of the voltage drop for the concave signal is slower than both the linear and convex signal at the beginning of the shut down, the concave drive signal takes longer to reach the MOSFET threshold voltage and the start time and end time of the Drain current characteristic, driven by concave drive signal is notably higher than those driven by either the linear or convex signal. When the frequency word is lower than 6, the start time and end time of the Drain current characteristic driven by the linear drive signal are higher than those driven by convex drive signal. However, with the increase in the frequency word, the difference between the start time of the drain current of the convex and linear drive signals and the difference between the end time of the drain current both decrease, and when the frequency word is higher than 9, the start time and end time of Drain current driven by linear and convex signal are almost identical. The average shut down time of Drain current driven by three different drive signals are similar which means that the shut down time of 12M1H030 will not be significantly impacted by the type of drive signal. However, the coefficient of variation of Drain current shut down time driven by convex drive signal, which is 0.05, is smaller than that driven by concave signal, which is 0.08, and the Drain current shut down time driven by linear drive signal has the largest coefficient of variation, 0.11, which is larger than the others studied here. Because the difference in the coefficient of variation between the convex and concave, and the small coefficient of variation values, the 30 mΩ MOSFET is more stable driven by either convex or concave signals in comparison to linear. Finally, considering the shut down time of Drain current driven by convex drive signal with

different frequency word has the smallest dispersion, the shorter start time and end time, the convex signal is the best choice to control the blocking of 12M1H030. In conclusion, to minimums the blocking time and overcurrent of MOSFET and increase the reliability of the control system, the convex drive signal with frequency word 6 is the best choice to control the blocking of SSCB based on the 30 mΩ SiC MOSFET. The novel drive signal can replace the MOV to minimum the impact of overcurrent on SSCB and shut down the circuit in a short time to protect the circuit, which reduces the weight and volume of the SSCB and remains the reliability.

Results of 12M1H045

To verify the short circuit performance of the novel drive signals when drive the MOSFET with different on resistance, the 12M1H045 and 12M1H090 are used to test in this Chapter. The test processing and evaluation are same with the 12M1H030.

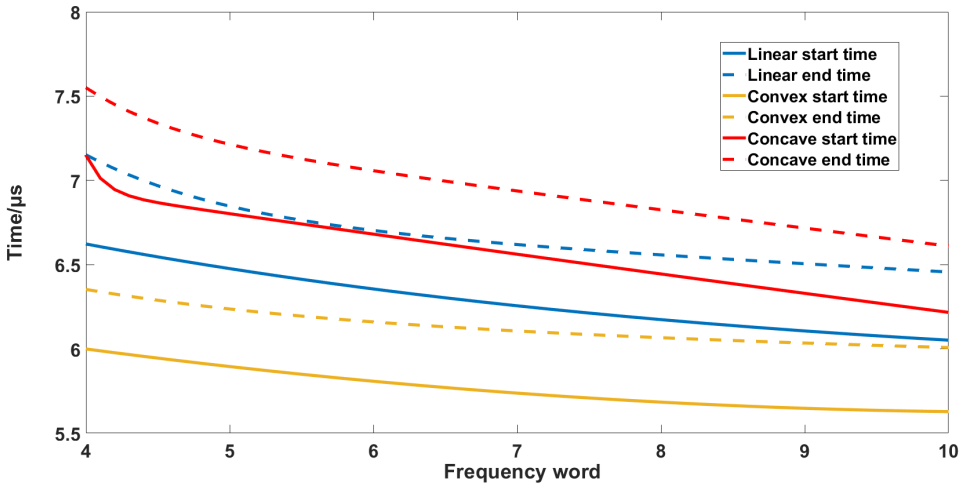

Figure 5.9: Fitting curve of 12M1H045 shut down time under linear, convex and concave drive signal with different frequency word and current shunt detection

The fitting curve of 12M1H045 Drain current shut down time under three different drive signals, including linear, convex and concave, with different frequency word has been shown in Figure 5.9 to predict the trend of Drain current shut time of 12M1H045 as a function of frequency word between 4 and 10, and compare the performance of three different drive signals with the same frequency word. According to the fitting curve, with the increase of the frequency word, the start time

and end time of the shut down processing decreases, however, the shut down time remains stable under three drive signals with different frequency word. Therefore, the shut down time of 12M1H045 will not be impacted by the change of frequency word and drive signal. Similar to the 30 mΩ MOSFET, the balance between the shut down speed and overcurrent is also considered in 45 mΩ MOSFET. According to the results, increasing the frequency word can reduce the shut down speed for the frequency words lower than 7 driven by three different drive signals, and after that, the improvement becomes less significant. Therefore, frequency word 7 is the best choice for linear, convex and concave drive signal to block the 12M1H045.

As for the drive signals, the time when the convex drive signal begins to drop, which is 4.80 μs, is earlier than the time of linear drive signal, which is 5.08 μs, and concave drive signal, which is 5.13 μs. In addition, the rate of decrease for the convex drive signal is also greater than that of the others at beginning. Therefore, the convex drive signal takes the shortest time to reach the MOSFET threshold voltage, and the start time and end time of Drain current driven by convex drive signal are shorter than those driven by Linear and concave signal. In addition, the start and end time of the Drain current driven by concave drive signal is the longest of those studied here. Variation in the frequency word from 4 to 10, the start and end time of Drain current driven by convex signal is consistently shorter than those driven by linear and concave signal. Meanwhile, with the increase in the frequency word, the difference between the start time and the difference between the end time of Drain current driven by any two drive signals both decrease. When frequency word reaches 10, the end time of Drain current driven by the concave signal is close to that driven by linear signal. The average shut down time of Drain current driven by three different drive signals are almost same which means that the shut down time of 12M1H045 will not be impacted by the type of drive signal. The coefficient of variation of Drain current shut down time driven by the linear drive signal, which is 0.14, is significantly larger than that driven by both the convex, concave signals, which are 0.05. Therefore, the 45 mΩ MOSFET shut down is more stable driven by convex and concave signal. Considering the reliability and the short short circuit performance of the MOSFET, the convex drive signal, with the highest

reliability and shortest short circuit time, is the best choice to control the blocking of 12M1H045. In conclusion, to minimums the blocking time and overcurrent of MOSFET and increase the reliability of the control system, the convex drive signal with frequency word 7 is the best choice to control the blocking of SSCB based on 12M1H045.

Results of 12M1H090

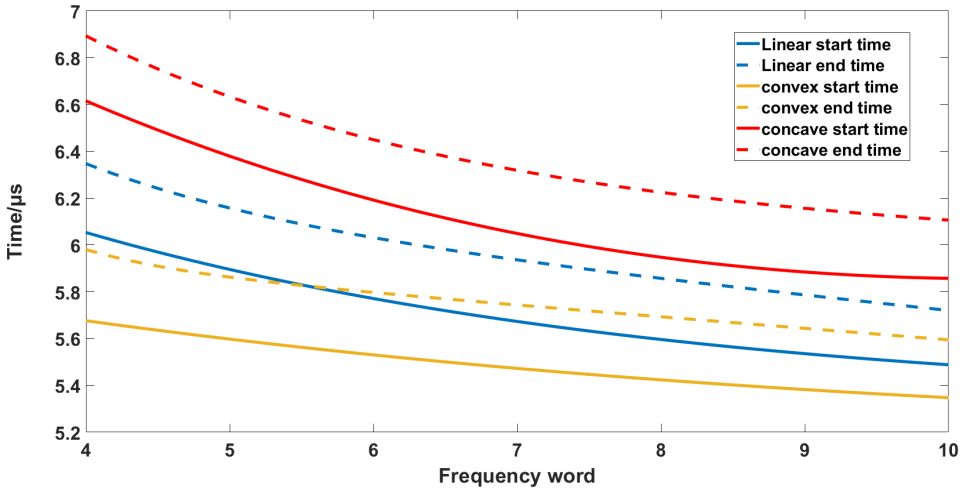

Figure 5.10: Fitting curve of 12M1H090 shut down time under linear, convex and concave drive signal with different frequency word and current shunt detection

The fitting curve of 12M1H090 Drain current shut down time under three different drive signals, including linear, convex and concave, with different frequency word has been shown in Figure 5.10 to predict the trend of Drain current shut time of 12M1H045 as a function of frequency word between 4 and 10, and compare the performance of three different drive signals with the same frequency word. According to the experimental results introduced before and the fitting curve, with the increase of the frequency word, the start time and end time of the shut down processing decrease, meanwhile, the shut down time remains stable when 12M1H090 is driven by three different drive signals with different frequency word. Therefore, the shut down time of 12M1H090 will not be impacted by the change of frequency word and drive signal. In addition, because the Drain current of the 12M1H090 is smaller than that of either the 12M1H030 or 12M1H045, the shut down time of 12M1H090

is shorter. According to the experimental results, increasing the frequency word can significantly reduce the shut down time when the frequency word lower than 8 driven by three different drive signals, and after that, the improvement reduces. Therefore, frequency word 8 is the optimum choice for linear, convex and concave drive signal to block the 12M1H090. In addition, decreases in the start and end times driven by concave signal is faster than the speed driven by linear signal, and the decrease speed driven by convex signal is the slowest, when the frequency word is lower than 8. Therefore, the start time and end time drive by concave signal have the most obviously improvement by increasing frequency word.

As for the drive signals, the time when the convex drive signal begins to drop, is 4.52 μs, is similar to the time for the linear drive signal, which is 4.50 μs, and the time of concave drive signal is the longest, which is 4.70 μs. The difference in the time when the drive signal starts to drop between the three different drive signals is insignificant, and the impact of the different drive signal start time can be ignored. It is obvious, that the start time and end time for the MOSFET driven by the convex drive signal is shorter than those driven by linear and concave drive signal, whilst the start time and end time when driven by concave drive signal is the longest. With increasing the frequency word, the end time driven by the linear signal is approaching the end time driven by the convex signal, but sill higher until frequency word reaches 10. Therefore, the MOSFET driven by convex signal has the shortest shut down time. The average shut down time of the Drain current driven by three different drive signals are similar which means that the shut down time of 12M1H090 will not be significantly impacted by the type of drive signal. The coefficient of variation of Drain current shut down time driven by linear drive signal is 0.08, by convex and concave is 0.07. Because the coefficient of variations are almost identical and the value is insignificant, the 90 mΩ MOSFET can be stably driven by linear, convex and concave drive signal. Considering reliability and the short circuit time requirement of MOSFET, the convex drive signal, with the high reliability and shortest short circuit time, is the best choice to control the blocking of 12M1H090. In conclusion, to minimums the blocking time and overcurrent of MOSFET and increase the reliability of the control system, the convex drive signal

with frequency word 8 is the best choice to control the blocking of SSCB based on 12M1H090.

According to the test results above, for the same MSOFET, the short circuit performance of the convex drive signal which has the shortest blocking time is better than the linear and concave. With the increase of the frequency word, the blocking time will decrease and the optimal frequency word to minimum the overcurrent and blocking time is between the frequency word 6 and 8.

Impact of different on MOSFET resistance to short circuit time

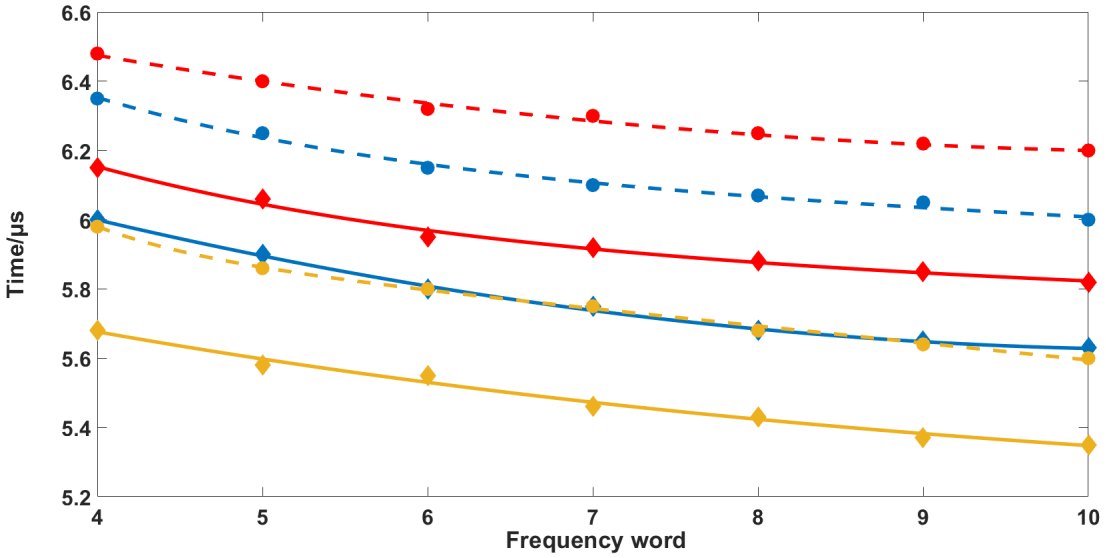

Figure 5.11: The comparison of start and end time of three different MOSFET Drain current driven by convex signal with different frequency word and current shunt detection

Three different MOSFETs have been tested in this section, and the main difference is the on-state resistance. Because the convex drive signal is shown to be the optimum choice for all three different MOSFETs with current shunt detection, the experimental results of convex signal are used to research the impact of different on-state resistance on the observed short circuit time. The comparison of the start and end times for the three different MOSFET Drain currents driven by convex signal with frequency word from 4 to 10 is shown in Figure 5.11. Where red diamond is 12M1H030 start time data, red line is 12M1H030 start time fitting,

red circle is 12M1H030 end time data, red dotted line is 12M1H030 end time fitting, blue diamond is 12M1H045 start time data, blue line is 12M1H045 start time fitting, blue circle is 12M1H045 end time data, blue dotted line is 12M1H045 end time fitting, yellow diamond is 12M1H090 start time data, yellow line is 12M1H090 start time fitting, yellow circle is 12M1H090 end time data, yellow dotted line is 12M1H090 end time fitting. According to the experimental results, increasing the on-state resistance, the end time of the Drain current decreases. The end time is determined by the sum of the start and shut down times. The feedback signal for the higher on-state resistance MOSFET results in more repaid rise and hence triggers the change of drive signal from the FPGA. Therefore, the start time of the higher on-state resistance MOSFET driven by convex drive signal is lower than that for linear or concave.

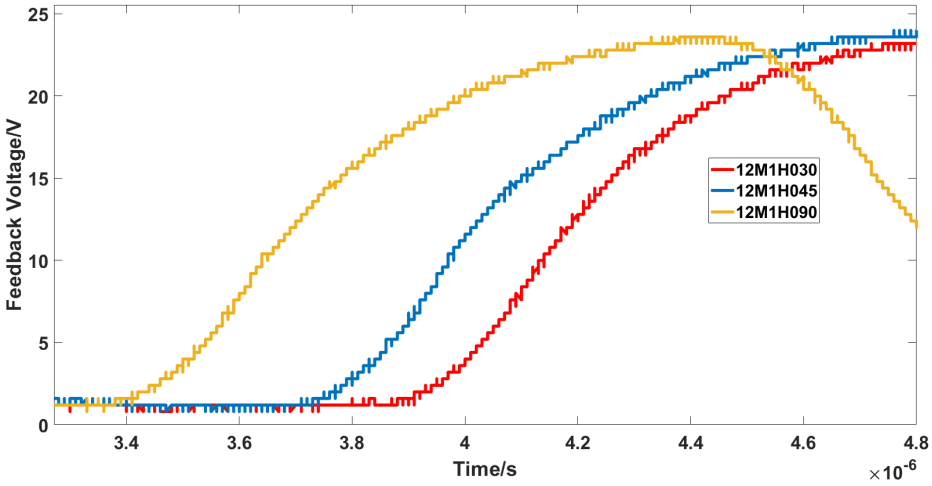

Figure 5.12: The comparison of feedback voltage of different MOSFETs driven by convex drive signal with frequency word 10 and current shunt detection

The comparison of feedback voltage for the different MOSFETs driven by convex drive signal with frequency word 10 is shown in Figure 5.12. Because the lower on-state resistance results in the higher Drain current when the short circuit occurs, and higher Drain current takes longer to be blocked, the shut down time decreases with increasing on-state resistance. The average shut down time driven by convex signal for 12M10H030 is 0.37 μs, 12M1H045 is 0.37 μs, and for the 12M1H090 is 0.27 μs. Because the MOSFET with higher on-state resistance has the earlier start

time and shorter shut down time, with the increase of the on-state resistance, the short circuit time will decrease when the MOSFET is controlled by convex drive signal with current shunt detection.

According to the test results, the optimal frequency word for MOSFETs with different on resistance is in the range between 6 and 8. It shows the on resistance of the MOSFET has little impact on the choice of frequency word. Therefore, it can be predicted that the MOSFET from the same family with lower on resistance will have a longer short circuit time, and the optimal frequency word will be in the range between 6 and 8. In addition, the advantage of the convex drive signal compared with liner signal is the faster drop speed. However, at the beginning of the drop, the drop speed of liner drive signal is similar with the convex. Therefore, if the voltage of MOSFET drive signal is close to the MOSFET threshold voltage, the start time of the current drop in main circuit will be similar when driven by the linear and convex drive signal, and the linear drive signal can also be a choice.

5.3.2 Voltage divider detection results

Overview of the voltage divider detection

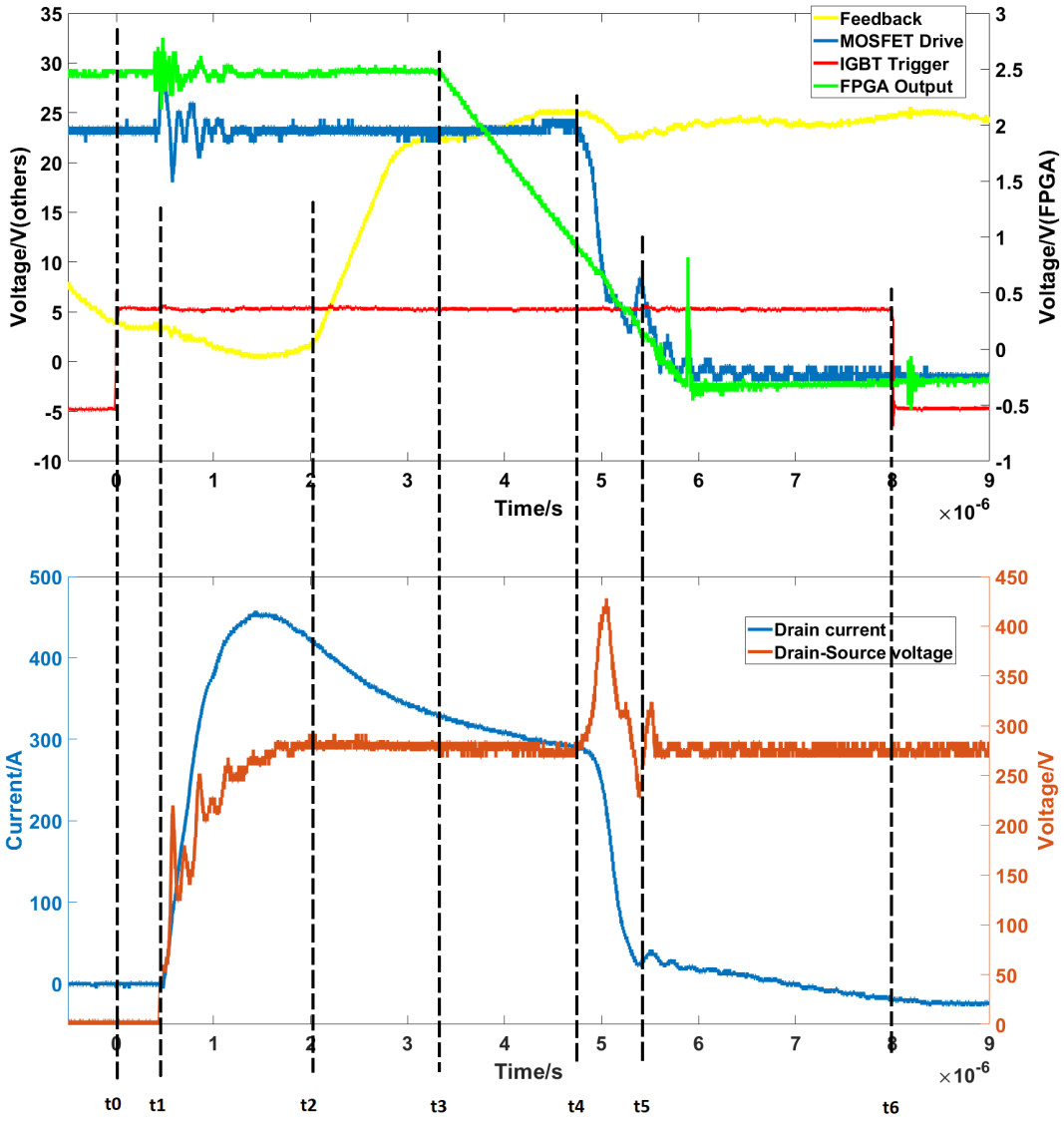

Figure 5.13: Short circuit test data for voltage divider detection

The short circuit test data for voltage detection and the performance of the control system is shown in Figure 5.13. In contrast to the current shunt detection, the voltage divider results in the larger input resistance for amplifier circuit. Therefore, the feedback shown in Figure 5.13 has a significant drift voltage, which is approximately 10 V. The drift voltage results in the feedback signal is not 0 but regular changing between 0 and 10 V when the circuit work normally. The drift voltage is

the main reason that the isolation circuit cannot be used with the voltage divider detection, because the isolation circuit will further amplify the voltage drift and the output remains at 24 V during the short circuit test, which results in the drive signal for MOSFET remaining at -5 V because the system triggers a false fault condition. The test data for voltage divider detection is similar to that with the current shunt detection. Before t0, the 270 V DC voltage supply will be turned on and the drive signal for MOSFET will remain at 24 V. At t0, the trigger signal for the IGBT rises to 5 V to place the IGBT in conduction and the short circuit test starts. Because of the delay between the trigger signal and drive signal for the IGBT, the IGBT will be conducting at t1 and the short circuit test starts. The delay of the IGBT drive signal is around 0.5 μs. At t2, the voltage divider detects the rise in Drain-Source voltage of the MOSFET, and the feedback signal begins to rise. The time t2-t1 is the delay of the amplifier circuit between the main circuit and FPGA, which is around 1.5 μs. The feedback reaches the threshold between t2 and t3, and because of the delay from amplifier circuit and FPGA, the FPGA output signal begins to drop at t3. The time t4-t3 is the delay of power amplifier circuit, which is around 1.7 μs, and at t4, the MOSFET drive signal begins to drop. As the drive signal takes time to reach the MOSFET threshold voltage, the Drain current begins to drop around 0.3 μs later than t4. Meanwhile, the significant change in Drain current results in a spike in Drain-Source voltage caused by the inductance in circuit. At t5, the MOSFET has been blocked, however the Drain current drops to around 30 A but not zero, because the voltage divider is paralleled with the MOSFET and when the MOSFET is blocked, the Drain current will through the voltage divider and the main circuit is still conducting. Meanwhile, the Drain-Source capacitor of the MOSFET discharge through the voltage divider because of the Drain-Source voltage drop at t5, which is around 200 V, and the discharge current flows through the voltage divider which results in the Drain current is drop to around 30 A but not zero. As the Drain current transforms from the blocked MOSFET to voltage divider, the performance of the main circuit is similar with the short circuit, and the Drain-Source voltage has an insignificant drop and is remained as 270 V by capacitors. After t5, the Drain current will keep decreasing until t6, when the IGBT is blocked. The total delay of

the voltage divider detection is around 4.2 μs.

The test processing and evaluation of voltage divider detection are same with the current shunt detection, and the short circuit performance of novel drive signals are introduced as follow.

Result of 12M1H030

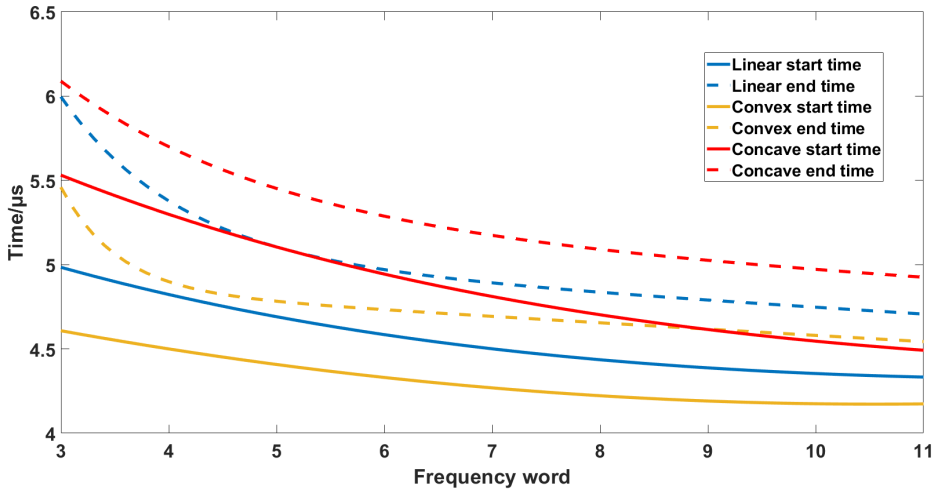

Figure 5.14: Fitting curve of 12M1H030 shut down time under linear, convex and concave drive signal with different frequency word and voltage divider detection

The fitting curve of 12M1H030 Drain current shut down time under three different drive signals, including linear, convex and concave, with different frequency word have been summarised in Figure 5.14 to predict the trend of Drain current shut time of the 12M1H030 MOSFET as a function of frequency word between 4 and 10, to directly compare the performance of three different drive signals with the same frequency word. With increasing frequency word, the start time and end time of the shut down process decreases for all three waveforms, meanwhile, the shut down time remains stable under three drive signals with different frequency word. Therefore, the shut down time of the 12M1H030 will not be impacted by the change of frequency word and drive signal. In contrast with the results of the current shunt detection method, the end time and start time of concave drive signal is closer to the time of convex and linear drive signal. Meanwhile, when the frequency word is higher than 7, the end time of three drive signals are similar and stable. As can

be seen from the data, increasing the frequency word can significantly reduce the shut down time of the linear drive signal before frequency word 6, and of convex and concave drive signal before frequency word 7. After that, the improvement is insignificant and higher frequency word results in higher overcurrent. Balancing the minimum the shut down time with the overcurrent, frequency word 6 is the optimum selection for linear drive signal, and frequency 7 is the optimum selection for convex and concave drive signal to block the 12M1H030.

As for the drive signal, in contrast with the current shunt detection method, the time when the drive signal begins to drop for three drive signals are similar, which is 3.33 μs for linear, 3.30 μs for convex and 3.34 μs for concave drive signal. Therefore, the difference in the start and end time for three drive signals with voltage divider detection is smaller than current shunt detection. In addition, the convex drive signal has the most significant decrease in drop time at the beginning of the shut down. Therefore the convex drive signal is faster to reach the MOSFET threshold voltage and the Drain current driven by convex signal decreases more rapidly than that driven by either the linear or concave signals. Furthermore, the rate of decrease for the convex drive signal is followed by linear drive signal, and the concave drive signal is the slowest. During the whole period, the start and end time of convex drive signal are the shortest, followed by the time of linear drive signal, and the time of concave drive signal are the longest. The average shut down time of the Drain current driven by three different drive signals are similar which means that the shut down time of 12M1H030 will not be significantly impacted by the type of drive signal. However, the coefficient of variation of Drain current shut down time driven by convex drive signal, which is 0.04, is smaller than that driven by concave signal, which is 0.08, and the Drain current shut down time driven by linear drive signal has the largest coefficient of variation, 0.13, which is significantly larger than the others studied here. Because the coefficient of shut down time driven by the convex drive signal is the smallest, the 30 mΩ MOSFET is more stable driven by the convex drive signal. Finally, considering the shut down time of Drain current driven by convex drive signal with different frequency word has the smallest dispersion, the shorter start time and end time, the convex signal is the best choice to control

the blocking of 12M1H030 MOSFET. In conclusion, to minimums the blocking time and overcurrent of MOSFET and increase the reliability of the control system, the convex drive signal with frequency word 7 is the best choice to control the blocking of SSCB based on 12M1H030 MOSFET.

Results of 12M1H045

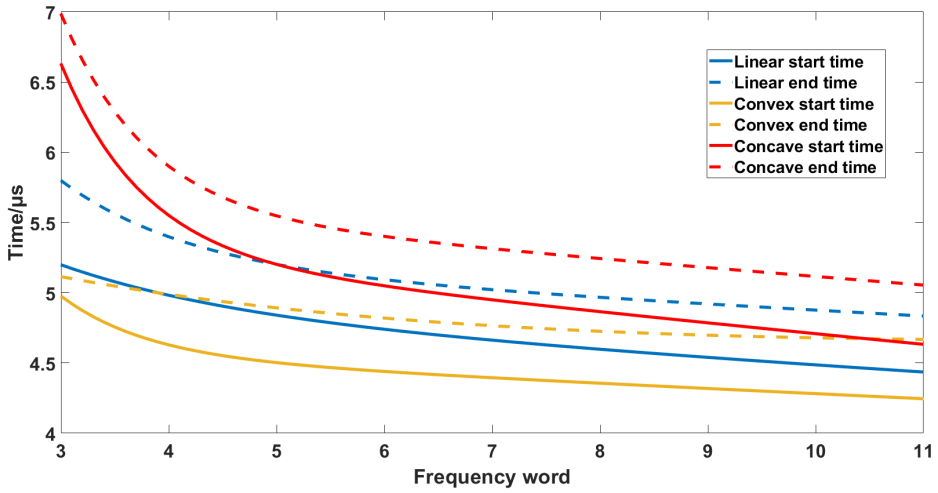

Figure 5.15: Fitting curve of 12M1H045 shut down time under linear, convex and concave drive signal with different frequency word and voltage divider detection

The fitting curve of 12M1H045 Drain current shut down time under three different drive signals, including linear, convex and concave, with different frequency word have been summarised in Figure 5.15 to predict the trend of Drain current shut time of the 12M1H045 MOSFET as a function of frequency word between 4 and 10, to directly compare the performance of three different drive signals with the same frequency word. With the increase of the frequency word, the start time and end time of the shut down process decreases for all three waveforms, meanwhile, the shut down time remains stable under three drive signals with different frequency word. Therefore, the shut down time of the 12M1H045 will not be impacted by the change of frequency word and drive signal. Comparing with the results of current shunt detection, the end time and start time of concave drive signal is closer to the time of convex and linear drive signal. Meanwhile, when the frequency word is higher than 6, the end time of three drive signals are paralleled and stable. As can be seen

from the data, increasing frequency word can obviously reduce the shut down speed of all three drive signals before frequency word 6. After that, the improvement is insignificant and higher frequency word results in the higher overcurrent. Considering to balance and minimum the shut down time and overcurrent, frequency word 6 is the optimum selection for all three drive signals to block the 12M1H045.

As for the drive signal, in contrast to the current shunt detection method, the time when the drive signal begins to drop for convex drive signal is the shortest, which is 3.39 μs, followed by linear drive signal which is 3.45 μs, and the time for concave is the longest, which is 3.52 μs. In comparison to the current shunt detection method, the difference in the start and end times for three drive signals with voltage divider detection is smaller. The convex drive signal has the largest rate of drop speed at the beginning of the shut down. Therefore the convex drive signal is faster to reach the MOSFET threshold voltage and the Drain current driven by convex signal drops earlier than driven by linear and concave signal. Furthermore, the rate of drop speed for convex drive signal is followed by linear drive signal, and the concave drive signal is the slowest. Therefore, during the whole period, the start and end time of convex drive signal are the shortest, followed by the time of linear drive signal, and the time of concave drive signal are the longest. The average shut down time of Drain current driven by three different drive signals are similar which means that the shut down time of 12M1H045 will not be significantly impacted by the type of drive signal. However, the coefficient of variation of Drain current shut down time driven by convex drive signal, which is 0.03, is smaller than that driven by linear signal, which is 0.06, and the Drain current shut down time driven by concave drive signal has the largest coefficient of variation, which is 0.07. Because the coefficient of shut down time driven by convex drive signal is the smallest, the 45 mΩ MOSFET is more stable driven by convex drive signal. Finally, considering the shut down time of Drain current driven by convex drive signal with different frequency word has the smallest dispersion, the shorter start time and end time, the convex signal is the best choice to control the blocking of 12M1H045 MOSFET. In conclusion, to minimums the blocking time and overcurrent of MOSFET and increase the reliability of the control system, the convex drive signal with frequency word 6 is the best choice to

control the blocking of SSCB based on 12M1H045 MOSFET.

Results of 12M1H090

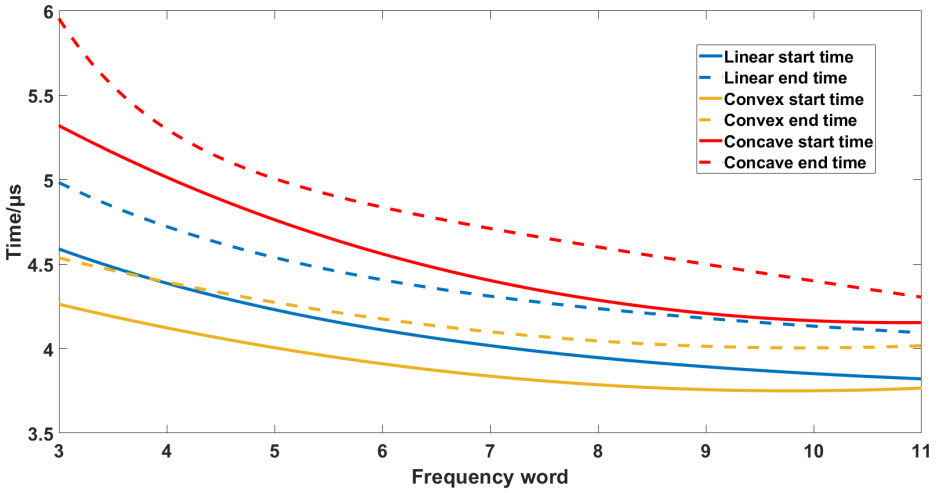

Figure 5.16: Fitting curve of 12M1H090 shut down time under linear, convex and concave drive signal with different frequency word and voltage divider detection

The fitting curve of 12M1H090 Drain current shut down time under three different drive signals, including linear, convex and concave, with different frequency word have been summarised in Figure 5.16 to predict the trend of Drain current shut time of the 12M1H090 MOSFET as a function of frequency word between 4 and 10, to directly compare the performance of three different drive signals with the same frequency word. With the increasing frequency word, the start time and end time of the shut down process decreases for all three waveforms. Meanwhile, the shut down time remains stable under three drive signals with different frequency word. Therefore, the shut down time of the 12M1H090 will not be impacted by the change of frequency word and drive signal. In comparison with the 30 and 45 mΩ MOSFET, the start and end time driven by the concave signal of 90 mΩ MOSFET is further higher than the time of linear and concave drive signal. When the frequency word is higher than 7, the end time of convex and linear drive signals are similar and stable, meanwhile, the rate of decrease for the concave drive signal start and end time is smaller than the frequency word below 7. As can be seen from the data, increasing the frequency word can significantly reduce the shut down speed of all three drive

signals for frequency word below 7. Above this, the improvement is insignificant and higher frequency word results in the higher overcurrent. Considering to balance and minimum the shut down time and overcurrent, frequency word 7 is the optimum selection for all three drive signals to block the 12M1H090.

As for the drive signal, be different with the current shunt detection, the time when the drive signal begins to drop for linear drive signal is the shortest, which is 2.70 μs, followed by convex drive signal which is 2.83 μs, and the time for concave is the longest, which is 3.00 μs. Comparing with the current shunt detection, the time when linear drive signal begins to drop is 0.63 μs shorter, the convex signal is 0.51 μs shorter and the concave signal is 0.34 μs shorter. The convex drive signal has the largest rate of drop speed at the beginning of the shut down. Therefore the convex drive signal is faster to reach the MOSFET threshold voltage and the Drain current driven by convex signal drops earlier than driven by linear and concave signal. Furthermore, the rate of drop speed for convex drive signal is followed by linear drive signal, and the concave drive signal is the slowest. Therefore, during the whole period, the start and end time of convex drive signal are the shortest, followed by the time of linear drive signal, and the time of concave drive signal are the longest. The average shut down time of the Drain current driven by three different drive signals are similar which means that the shut down time of 12M1H090 will not be significantly impacted by the type of drive signal. However, the coefficient of variation of Drain current shut down time driven by convex drive signal, which is 0.04, is smaller than that driven by linear signal, which is 0.06, and the Drain current shut down time driven by concave drive signal has the largest coefficient of variation, which is 0.10. Because the coefficient of shut down time driven by convex drive signal is the smallest, the 90 mΩ MOSFET is more stable driven by convex drive signal. Finally, considering the shut down time of Drain current driven by convex drive signal with different frequency word has the smallest dispersion, the shorter start time and end time, the convex signal is the best choice to control the blocking of 12M1H090 MOSFET. In conclusion, to minimums the blocking time and overcurrent of MOSFET and increase the reliability of the control system, the convex drive signal with frequency word 7 is the best choice to control the blocking

of SSCB based on 12M1H090 MOSFET.

Compared with the results of current shunt detection, the block time of MOSFETs, with voltage divider detection, driven by novel drive signals is shorter, because the voltage divider detection remove the isolation circuit between the ADC and voltage divider. However, it results in the higher safety risk. Be same with the results of current shunt detection, compared with the liner and concave drive signal, the convex drive signal with the shorter blocking time is the optimal drive signal to drive the MOSFETs. The frequency word range between 6 and 7 is the optimal frequency word to minimum the overcurrent and blocking time.

Impact of different on resistance to short circuit time

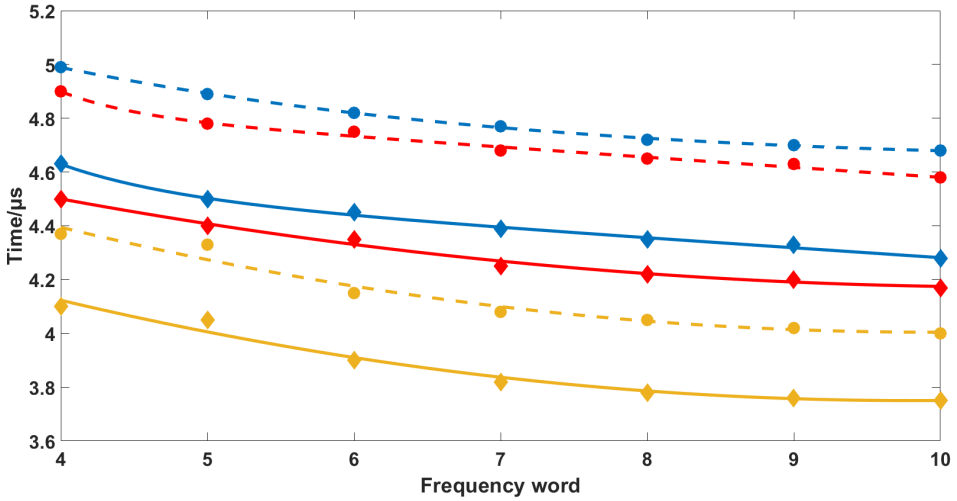

Figure 5.17: The comparison of start and end time of three different MOSFET Drain current driven by convex signal with different frequency word and voltage divider detection

The main difference between the three MOSFETs tested in this section is the on resistance. Because convex drive signal is the best choice for all three different MOSFETs with voltage divider detection, the experimental results of convex signal are used to research the impact of different on resistance to short circuit time. The comparison of start and end time of three different MOSFET Drain current driven by convex signal with frequency word from 4 to 10 is shown in Figure 5.17. where red diamond is 12M1H030 start time data, red line is 12M1H030 start time fitting, red

circle is 12M1H030 end time data, red dotted line is 12M1H030 end time fitting, blue diamond is 12M1H045 start time data, blue line is 12M1H045 start time fitting, blue circle is 12M1H045 end time data, blue dotted line is 12M1H045 end time fitting, yellow diamond is 12M1H090 start time data, yellow line is 12M1H090 start time fitting, yellow circle is 12M1H090 end time data, yellow dotted line is 12M1H090 end time fitting. The end time is the sum of the start and shut down times together. The comparison of feedback voltage of different MOSFETs driven by convex drive signal with frequency word 10 is shown in Figure 5.18.

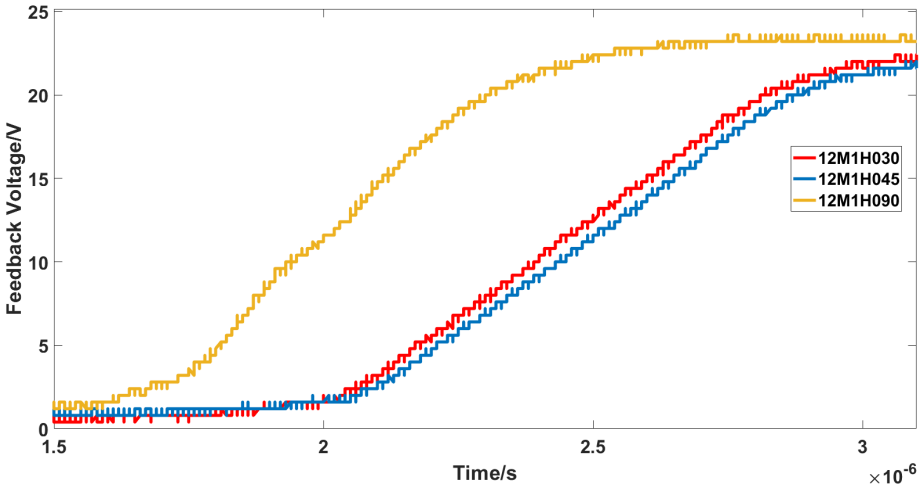

Figure 5.18: The comparison of feedback voltage of different MOSFETs driven by convex drive signal with frequency word 10 and voltage divider detection

As can be seen from the data, the feedback signal for 12M1H090 is the fastest, followed by the feedback for 12M1H030, and the feedback for 12M1H045 is the slowest. The feedback signal for 12M1H030 and 12M1H045 have an insignificant difference, but much slower than the feedback signal for 12M1H090. Therefore, the start time of 12M1H090 is earlier than the start time of 12M1H030 and 12M1H045, which are similar. As for the shunt down time, because the lower on resistance results in the higher Drain current when the short circuit occurs, and the higher Drain current takes longer time to be blocked, the shut down time will decrease with increasing on-state resistance. The average shut down time driven by convex signal of 12M10H030 is 0.41 μs, 12M1H045 is 0.38 μs, and the 12M1H090 is 0.26 μs. Because the 12M1H090 has the significantly small start time and shut down

time, comparing with other two MOSFETs, the end time and short circuit time of 12M1H090 is significantly lower than other two MOSFETs when the MOSFET is controlled by convex drive signal with voltage divider detection.

Comparing with the results of current shunt detection, the increase of the start time has no obvious dependence with the on-state resistance. However, the difference between the feedback signal of 12M1H030 and 12M1H045 is insignificant and the reliability of the feedback for voltage divider is lower than the current shunt because of the drift voltage. Therefore, it can be observed from the data that the start time of MOSFETs under convex drive signal with both current shunt and voltage divider detection decreases, with the increase of the MOSFET on resistance.

In conclusion, the short circuit performance of three different SiC MOSFETs, include 12M1H030, 12M1H045, 12M1H090 driven by different drive signals with frequency word from 4 to 10 and detected by current shunt and voltage divider separately has been verified in this Chapter. Although the test platform of current shunt detection is different with the voltage divider detection, there are still some common conclusions can be verified. Firstly, with the increase of the frequency word, the short circuit time will decrease. However, the rate of decrease speed also decreases and the improvement of the short circuit performance will be insignificant when the frequency word is very large. In addition, the higher frequency word results in more overcurrent which results in the noise of Drain current when the circuit is blocked. Therefore, to balance the short circuit time and the overcurrent, there is an optimal frequency word and for the all MOSFETs tested in the Chapter driven by all three drive signals, the optimal frequency word is in the range from frequency 6 to 7. As for the different drive signals, the time when the drive signal begins to drop are similar for the same MOSFET and because the rate of decrease for convex drive signal is larger than linear and concave, the convex drive signal takes shorter time to reaches the threshold voltage of MOSFET. Therefore, the MOSFET driven by convex drive signal is earlier to shut down and has less short circuit time compared with the MOSFET driven by linear and concave drive signal. According to the data shown in this Chapter, the convex drive signal with the frequency word in the range from 6 to 7 is the optimise drive signal to drive the SiC MOSFET in SSCB

applications.

The main reason that the different MOSFETs can impact the performance of short circuit test is the on resistance. As can be seen from the data in this Chapter, the MOSFET with higher on resistance has the earlier time when the Drain current begins to drop. In addition, the higher on resistance results in the lower Drain current during the short circuit, which reduces the shut down time of the Drain current. Therefore, the MOSFET with the higher on resistance has the shorter short circuit time. However, the difference of short circuit times is insignificant and higher on resistance results in more power loss during the normal operation, and the MOSFET with the Lower on resistance is the optimise choice for SSCB.

The different detection methods also have the impact on the performance of short circuit test. The current shunt detection is more stable compared with the voltage divider detection, and the Drain current has no noise when the circuit is blocked. However, the isolation circuit in current shunt detection results in more delay time and the short circuit time is longer. In contrary, the voltage divider detection has less short circuit time but the Drain current will not drop to zero when the MOSFET is blocked because the voltage divider is paralleled with the MOSFET and conduct the circuit before the IGBT is blocked. Meanwhile, no isolation circuit results in more risk compared with the current shunt detection.

5.4 Conclusion

In conclusion, the short circuit performance of the novel drive signals and FPGA control system is introduced in this Chapter. The current shunt and voltage divider are used to detect the working condition of the main circuit and send the feedback signal to FPGA. To reduce the risk of the test, the isolation circuit is used to isolate the control system with the main circuit, however, in voltage divider detection, the isolation circuit results in the large noise when the Drain current is blocked, because of the drift voltage. Therefore, the current shunt detection is more stable but has the longer shun down time, and the voltage divider detection has the shorter shut down time and potential risk. To ensure the drive signal generated by FPGA

can conducted the MOSFET, the power amplifier circuit is designed and the output voltage between -5 V and 22 V is sufficient to drive the MOSFET with 18 V threshold voltage. Because the convex drive signal drops faster when the faults occur, the MOSFET drive by convex drive signal has the shorter short circuit time compared with the linear and concave drive signal and the convex is the optimise choice the drive the SiC MOSFET. The short circuit time deceases with the frequency word increasing, however the higher frequency word results in more noise when the Drain current is blocked. Therefore, to minimise the short circuit time and noise, the frequency word range between 6 and 8 is the optimise choice. The main impact of different MOSFETs on the novel drive signals short circuit performance is the on resistance, and the MOSFET with higher on resistance has the shorter short circuit time. However, the difference of short circuit time is insignificant and the higher on resistance results in more power loss during the operation. Therefore, the MOSFET with lower on resistance is the optimise choice for SSCB. As can been seen from the data in this Chapter, the 12M1H030 SiC MOSFET driven by the control system with the current shunt detection, and convex drive signal with 6 frequency word is the optimise choice to design the SSCB.

The results in this Chapter verify the novel drive signal can replace the snubber circuit, including the MOV, to reduce the overcurrent, which can help reducing the volume and weight of SSCB. Meanwhile, the short shut down time ensure the reliability of SSCB in short circuit protection. In addition, the results prove the novel drive signal can be used to drive different MOSFETs from a same family, which makes the novel drive signal can be widely applied in SSCB design.

CHAPTER 6

Conclusions

6.1 Conclusion

A novel drive signal to minimise the overcurrent and short circuit time for SSCB based on SiC MOSFET is described in this thesis. The novel drive signal can replace the snubber circuit to reduce the impact of the overcurrent on the circuit. Therefore, the SSCB, driven by the novel drive signal, can remove snubber circuit to reduce the weight, volume and the number of devices used in SSCB. Meanwhile, the novel drive signal can shut down the circuit in a short time when the fault occurs, which ensures the reliability of the SSCB driven by novel drive signal. These advantages make the novel drive signal can be used in applications that have critical reliability and weight requirements, including the aviation system. According to the experiential results, the novel drive signal can drive the MSOFET with different on resistance, and it ensures the novel drive signal can be widely used in SSCB design.

In Chapter 2, the existing work in the literature describing a number of key technologies and applications of SSCB research were introduced. To improve the short circuit performance of the SSCB, a number of methods have been proposed to date, including using wide bandgap power semiconductor devices with increased voltage

ratings, novel topologies with lower power loss, the incorporation of snubber circuits to reduce overcurrent and absorb fault energy, novel fault detection method to increase the reaction speed, and novel drive circuits for series or paralleled connection SSCB in higher power applications. This work reported in this thesis focuses on the development of novel drive signals generated by a FPGA control system to minimize the overcurrent and short circuit time for SSCB based on SiC MOSFETs.

In Chapter 3, a 270 V short circuit test platform is described and the short circuit characteristics of three SiC MOSFETs from the same family are determined and compared. The maximum short circuit withstand time is a critical parameter to consider with considering the MOSFET short circuit ability, and in Chapter 3, this parameter is evaluated based on three different short circuit performance metrics, including the overcurrent and overvoltage, the condition of the Gate and the maximum junction temperature. As can be seen from the data presented, the 12M1H030 MOSFET has the longest short circuit time, at 16 μs, this maximum duration for 12M1H045 is 12 μs, and the time for 12M1H090 is 9 μs. The results are subsequently used to design the test facilities and operating parameters of the SSCB to verify the short circuit performance of the novel drive signal and FPGA control system that is reported in Chapter 5.

In Chapter 4, the design of the control system based on a FPGA, which is used to collect feedback signal that describe the operation of the circuit and subsequently generate the drive signal to the MOSFET, is introduced. The novel drive signal introduced in this Chapter has three parts, including the normal, transform and error. The FPGA can generate the corresponding signal according to the main circuit working condition. When the main circuit works under normal conditions, the FPGA generates the normal drive signal. Once the fault occurs, the FPGA generates the transform signal to transition the MOSFET from conducting to blocking modes. Subsequently the FPGA remains at error drive signal. In addition, the drive signal has three types during the transition period, including the linear, convex and concave signal, and different transform time, which is controlled by FPGA. The control system introduced in this Chapter can generate flexible drive signals and control the conducting and blocking characteristics of the MOSFET. The performance of

the control system and novel drive signals has been subsequently verified in Chapter 5.

In Chapter 5, the short circuit performance of the control system and drive signal introduced in Chapter 4 is verified. The tests performed to optimise includes three types of drive signals, including linear, convex and concave, and investigate the effects on three SiC MOSFET from the same family, including 12M1H030(Ron=30 mΩ), 12M1H045(Ron=45 mΩ) and 12M1H090(Ron=90 mΩ) with variation in the period of transition, described using different frequency words between 4 to 10, and two feedback detection methods, including the current shunt and voltage divider detection. As can be seen from the data, the convex drive signal is the optimum drive signal for SSCB applications, which has the shortest short circuit time whilst minimising the over current. With increasing frequency word, the short circuit time decreases. However, the higher frequency word results in increased overcurrent, therefore, to minimise the overcurrent and short circuit time, the optimisation of the frequency word is required, resulting in values in the range between 6 and 8. The data show that current shunt detection has the more stable feedback signal and reduced noise when the Drain-Source current in the MOSFET is blocked in comparison to operation based on the voltage divider detection technique. In addition, the isolation circuit between the FPGA and main power circuit that is required in the current shunt detection method ensures the safety of control system from high power transients. Therefore, the current shunt detection is the better technique for the detection of the SSCB operating condition. The MOSFET with higher on-state resistance and lower Gate charge is able to be turned off with a shorter short circuit time but shows higher power loss during the transition. To reduce the power loss of control system, 12M1H030 with the lowest on-state resistance is more suitable to be used in SSCB design for high power applications.

6.2 Future work

The novel drive signal introduced in this thesis can protect the power distribution system of aviation application by shut down the power system. However, it is not

an optimise solution when an airplane malfunctions in mid-air. In the future, the target of SSCB design can be ensuring that the power distribution system with the important functions, including the temperature system and oxygen supply system, can still be used during a short circuit fault, while ensuring that the components of the power supply system will not be damaged. The challenges can be the control logic of the SSCB and how to reduce the impact of short circuit current on power system. One solution might be useful is integrating the adjustable load in SSCB. When the power system works normal, the load will not be connected in the power system, and when the fault occurs, the adjustable load can be connected by the control system of SSCB to limit the short circuit current under a safe level.

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