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HIGH GAIN DC-DC CONVERTER TOPOLOGIES FOR POWER SYSTEMS

A thesis submitted for the degree of

Doctor of Philosophy

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Supervised by

Professor Alton Horsfall and Dr Mahmoud Shahbazi

Electrical Engineering

Durham University

United Kingdom

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Abstract

The voltage levels produced from renewable energy, particularly wave energy converters are relatively low and must be stepped up considerably to enable DC grid integration. This necessitates the use of high voltage gain DC-DC boost converters for power systems. These converters are designed for unidirectional power transfer and provide a high voltage gain (ten times or higher), supporting the high wave energy peak and low average power levels required for the integration of distribution networks. In theory, conventional boost converters are the common basic DC-DC step-up converters. However, these converters often operate with excessive duty cycles to obtain high voltage gain, causing severe voltage stress across devices. The main challenge of the high gain transformerless DC-DC converters is the requirement for an extreme (>80%) duty cycle to achieve the desired gain, resulting in poor efficiencies. This thesis presents the development, analysis, and design advanced high gain DC-DC converter topologies integrating magnetic and capacitive techniques and voltage multiplier circuits. The proposed converters could provide enhanced performance compared to currently available state-of-the-art converter topologies, the main advantages of which are the capability to achieve high voltage gain without the need for an extreme duty cycle, as well as low voltage stress on the switching device and self-balanced voltage levels at the output. In addition, the proposed converters require only a single switch, reducing the complexity of the control strategy. Four transformerless high gain DC-DC topologies are presented; Multilevel Boost Converter (MBC), Switched Inductor Multilevel Boost Converter (SIMBC), Voltage Lift Switched Inductor Multilevel Boost Converter (VLSIMBC) and Z-source Multilevel Boost Converter (ZSMBC), which could achieve the desired gains with

relatively high efficiencies. The operation principles, steady-state relations, and different input circuit strategies to further improve the voltage gain performance of the proposed converters are described. Furthermore, a theoretical analysis of power losses is provided. In addition, laboratory prototypes are developed to experimentally validate the given theories, simulation results and feasibility of the proposed topologies.

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List of Abbreviations

RESs	Renewable Energy Sources
WEC	Wave Energy Converter
MVDC	Medium Voltage Direct Current
$R_{DS,(ON)}$	Drain-Source Resistance On-State
CO_2	Carbon Dioxide
DPG	Distributed Power Generation
ESS	Energy Storage Systems
AC	Alternating Current
SST	Solid State Transformer
HFT	High Frequency Transformers
MBC	Multilevel Boost Converter
SIMBC	Switched Inductor Multilevel Boost Converter
VLSIMBC	Voltage Lift Switched Inductor Multilevel Boost Converter
ZSMBC	Z-Source Multilevel Boost Converter
VM	Voltage Multiplier
CBC	Conventional Boost Converter
MOSFET	Metal-oxide-semiconductor Field-effect-transistor
IGBT	Insulated-Gate Bipolar Transistors
PWM	Pulse Width Modulation
EMI	Electromagnetic Interference
PV	Photovoltaic
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
VMR	Voltage Multiplier Rectifier
$R_{ESR,L}$	Equivalent Series Resistance of the Inductor
ESR	Equivalent Series Resistance
SiC	Silicon-Carbide
Si	Silicon
RMS	Root Mean Square
ZSI	Z-Source Inverter

Publications

[1] A. Alsafrani, M. Parker, M. Shahbazi, and A. Horsfall, "High Gain DC-DC Multilevel Boost Converter to Enable Transformerless Grid Connection for Renewable Energy," in *2021 56th International Universities Power Engineering Conference (UPEC)*, 2021: IEEE, pp. 1-6.

[2] A. Alsafrani, M. Shahbazi, and A. Horsfall, "High gain DC-DC voltage lift switched-inductor multilevel boost converter for supporting grid connection of wave energy conversion," in *11th International Conference on Power Electronics, Machines and Drives (PEMD),* 2022: IEEE, pp. 1-5.

[3] A. Alsafrani, M. Shahbazi, and A. Horsfall, "High gain DC-DC switched inductor multilevel boost converter to enable transformer less grid connection for wave energy," *in 19th International Conference on AC and DC Power Transmission (ACDC 2023),* 2023: IET p. 102 – 107.

[4] A. Alsafrani, D. Blackhorse-Hull, N. Sarma, M. Shahbazi, and A. Horsfall, " Analysis of Transformerless, Single Switch, High Gain DC–DC Converters for Grid Connection of Wave Energy," has been submitted to IEEE Access Journal.

[5] D. Blackhorse-Hull, A. Alsafrani, N. Sarma, and A. Horsfall, " Multi-Level Dual Polarity DC-DC Converter," To submitted to IEEE Transactions on Power Systems.

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Chapter 1: Introduction

1.1 BACKGROUND AND MOTIVATION

Non-renewable energy sources have been experiencing significant challenges. Global warming, rising oil prices, and the growing energy crisis are the most compelling reasons to choose more sustainable sources and environmentally friendly electric power generation options. Thus, the primary focus in electrical supply revolves around the providing clean, cheap, and sustainable power supply to consumers via the distribution grid. The advantages of renewable energy generation include increased reliability, improved power quality, reduced power loss, and the integration of renewable energy sources (RESs) [1].

Renewable energy sources have been widely adopted as an alternative to conventional energy generations [2]. RESs include wave energy, wind, solar, tidal, and geothermal. Wave energy is considered one of the most promising, exploitable renewable energy sources due to its abundant potential and pollution-free nature. Compared to other renewable energy sources, the arrival pattern of waves is relatively predictable, and waves have a high power density due to the density of water [3]. Wave energy converters can also be located far enough away from the coast so that they are not visible [4]. Therefore, wave energy conversion technology has been increasingly utilised to convert wave power into electric power. However, since wave energy has a low-capacity factor, electrical power systems that can produce a stable DC output over a wide variety of input voltages are required. To solve this concern, power take-off systems with high voltage gain DC-DC converters are needed to boost the rectified output voltage from the wave energy converter (WEC). This would also allow a wave energy installation to use a medium voltage direct current (MVDC) collection network

for many WECs without the requirement for complex synchronisation. The voltage levels produced by wave energy converters are relatively low and must be stepped up considerably to enable DC grid integration, necessitating high voltage gain DC-DC boost converters.

Various DC-DC converter topologies have been discussed in the literature to offer high voltage gain. These topologies involve isolated and non-isolated converters. By adjusting the transformer's turn ratio, isolated converters can realise a high voltage gain [5]. Furthermore, isolated topologies that employ a high-frequency transformer can provide isolation between input and output terminals [5, 6]. However, the main drawback of the isolated DC-DC converters is that the transformer leakage inductance causes power transformer losses and stray inductance originating from the circuit's layout; thus, these isolated converters are not appropriate for obtaining high conversion ratios. Besides, the size and weight of these converters make it challenging to include them in a wave energy converter [6]. High voltage gain with increased efficiency can be achieved without a transformer in non-isolated topologies [7-15]. There are two broad classes of non-isolated step-up DC-DC converters: coupled-inductor-based [7-9] and non-coupled-inductor-based types such cascade boost, switched-capacitor and switched-inductor [10-15]. Coupled-inductor topologies improve efficiency and minimise voltage stress on the inductors, significantly increasing voltage gain. However, the linked inductor leakage issue creates a significant voltage spike on semiconductor components, and the circuits are challenging to design [7]. The dual-switch-based converters present high voltage conversion ratios with high input current ripple [11, 14]. Data published in the literature suggests that cascaded two-stage boost converters can achieve a high voltage gain [13]. In this converter, the switch experiences voltage stresses equal to the output

voltage, requiring a higher rated switch. Moreover, a switched-inductor structure has been proposed, which operates by charging two inductors in parallel and discharging them in series, increasing the voltage gain [14].

This thesis focuses on the design of high-gain DC-DC converters that demonstrate enhanced voltage gain, increased efficiency, and reduced voltage stresses across the active devices that are suitable for the integration of renewable energy, particularly wave energy, to the distribution grid in the UK via an MVDC collection network. Transferring energy from a wide range of input voltages requires a voltage gain that is significantly greater than what may be achieved with conventional boost converters, in particular, ten times or higher. Duty cycle operation is crucial in high step-up DC-DC converters since high duty cycle operation leads to limitations. The main drawback of operating converters with an extreme (>80%) duty cycle is the high voltage stress across the power devices, where the converters output voltage is equal to the power devices voltage of the conventional step-up converters. This results in the need for high rated devices. Power device rating is another concern associated with the performance of high step-up converters. For power MOSFETs, as the power rating rises, the on-state drain- source resistance ($R_{ds,on}$) likewise increases, causing conduction losses that further impair the efficiency. Therefore, there is substantial motivation to improve the performance of high-gain step-up DC-DC converters by reducing the voltage stress across the power devices so that switching loss can be significantly decreased.

1.2 POWER SYSTEM DISTRIBUTION

Classical electrical power systems have a vertical configuration that includes generation, transmission, and distribution [16]. Following the present arrangement,

power must be transferred from the transmission and distribution networks to the consumer. As a consequence of these transmission losses, efficiency degrades. In addition, thermal power plants' carbon dioxide (CO_2) emissions from consuming carbon-based fuels contribute to global warming. Hence, minimising generating power from conventional thermal power plants and increasing the penetration of distributed power generation (DPG) systems is one of the primary objectives in reducing global warming.

DPG systems are essential for future power grids because they generate energy and transmit it to numerous locations. Furthermore, DPGs can be used alongside renewable energy sources like solar energy, wave energy and wind power, as well as batteries and fuel cells to control, monitor, enhance power quality, find and isolate faults, and stabilise the grid [17]. DPG utilises microgrids that involve power networks and incorporate DPG systems and loads of varying types. Microgrids can function both independently and in conjunction with the larger power grid. Also, when properly controlled and operated, microgrids can improve the stability and quality of the power distribution system [16, 18].

Furthermore, the DPG system is an essential element of a microgrids, and various arrangements enable microgrids to function either independently or connected to the grid. The block diagram of the power system distribution is shown in Figure 1.1. It can be noticed from this figure that before the generated power can be connected to the utility grid or fed to DC consumer loads, it must be converted and regulated by certain power electronics converters [19, 20]. Utilising the locally generated power to fulfil the demands of the loads necessitates using DC-DC converters that operate at different power levels.

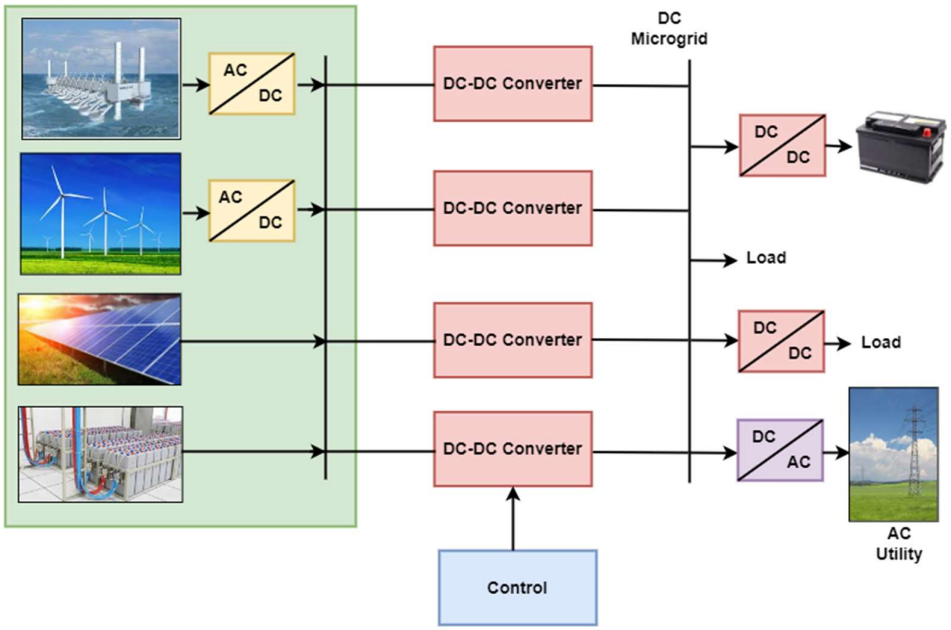

Figure 1.1: Power system distribution.

In addition, DC microgrid systems have gained significant interest in the current era enabling implementation with technologies including RESs, energy storage systems (ESS), electric vehicle charging, and residential applications. Therefore, DC distribution systems have recently gained increasing interest from developers owing to their benefits which are highlighted as follows.

- Environmental groups increasingly demand limiting CO_2 and other harmful emissions during power generation. Incorporating RESs on a substantial scale and enhancing the performance of power generation and transmission may contribute to accomplishing this goal. Hence, a DC grid system could be an effective approach to verify such feasibility [21].
- In the event of grid disturbances, the DC microgrid system maintains stability, reliability, control flexibility and power quality [22].
- Since RESs synchronisation with the grid system and reactive power control are unnecessary, the system's complexity can be minimised [22].

- In a DC grid system, the skin effect phenomena does not occur, enabling current to flow through the entire cable, unlike in AC grid system. Employing a smaller-gauge cable for the same amount of current enhances transmission efficiency and reduces the cost of transmission and distribution [23].

In consideration of these merits, the DC microgrid system has the potential to replace the traditional transmission system gradually. Moving to MVDC for many applications is a useful ideal, especially when considering distribution level. However, interfacing some sort of connected devices and generators to MVDC needs high gain step-up converters, which is a challenge that is discussed in this thesis. Examples are grid connected wave energy generation units that have a lot of potential and are discussed in the following.

1.3 HIGH STEP-UP DC-DC CONVERTER APPLICATIONS

1.3.1 Grid Connected Wave Energy Converter

Wave energy is an emerging technology that has the potential to provide a clean and sustainable source for the generation of renewable energy. The conversion of motion wave energy to electricity is considered one of the most environmentally friendly approaches to generating electricity, as it produces zero waste that must be kept or impacts the ecosystem [1]. It has the potential to fulfil up to 20% of the current UK electricity demand [24]. Compared to other renewable energy sources, the wave resource is highly predictable and possesses a significantly higher power density in comparison to wind [1, 3]. Additionally, it is one of the most affordable renewable energy sources due to its high-power density [1]. Wave energy systems can also be located offshore, hidden from public view [1, 4]. For wave energy to be viable, multiple spatially distributed converters need to be integrated into a power collection

network. The temporal variation of the energy that can be collected in such a network gives rise to challenges in synchronising and balancing a conventional AC system. DC collection networks can be utilised in place of these conventional AC systems, eliminating the need to synchronise different generation frequencies. For this to be feasible, the integration of a MVDC transmission system for multiple WECs offers significant advantages [25, 26]. The intermittent nature of the ocean waves results in irregular power produced by the wave energy converters (WECs). Accordingly, WECs have significant challenges in integrating with the grid. For instance, to efficiently convert continuous wave motion into electrical energy, the challenge of harnessing wave power generated at low speeds yet with significant force is challenging. This strong motion has no single direction and differs from the conventional operation of electric generators, which operate optimally with high speeds and require constant input [3]. The recently suggested undersea storage system can overcome this obstacle by smoothing the WEC output power oscillations [26]. However, wave energy has a low-capacity factor, necessitating the use of electrical power systems to produce a stable DC output to the collection network over a wide range of input voltages. Power take-off systems that may boost the rectified output voltage from a WEC and feed a grid-connected inverter with high conversion ratio DC-DC converters are required to enable this, as shown in Figure 1.2.

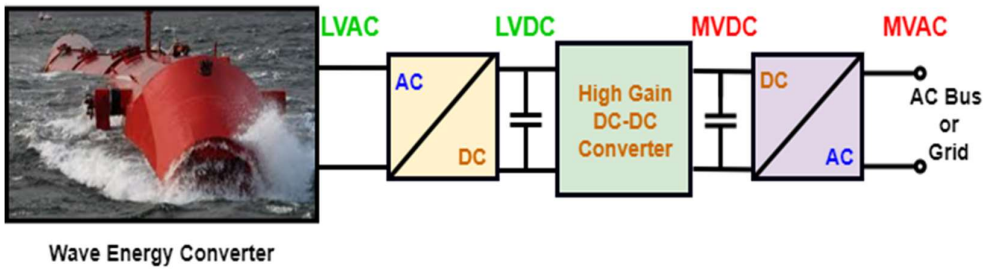

Figure 1.2: Schematic representation of a Wave Energy Converter (WEC) and Power Take Off (PTO) system.

DC networks are becoming increasingly significant in the marine energy environment due to their ability to handle the challenges associated with ocean wave power generation. Employing the MVDC system, they can effectively transfer wave-generated power from offshore wave sources to onshore networks while maintaining high efficiency for long-distance power transmission. Furthermore, DC networks enable the smooth integration of wave energy into onshore grids, facilitating bidirectional power flow for stability on the grid [28].

Publicly available data associating to existing output voltages in wave energy is very limited. [27] presented a system with the produced voltage up to $\pm$ 150 V, while in [28], the generated voltage was up to $\pm$ 300 V. As the wave energy source generates electricity with a linear generator, the output voltage displays oscillations in both amplitude and frequency as shown in Figure 1.3 [27]. Thus, it must first be rectified and then inverted before it can be integrated into the grid. Rectification is necessary for voltage regulations and a DC link. Furthermore, connecting multiple wave converters in parallel increases the power at the DC connection and becomes more stable [27].

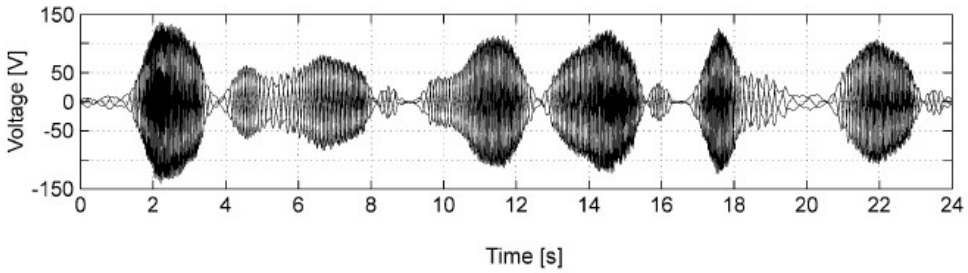

Figure 1.3: Output voltage from a WEC in Lysekil [27].

Furthermore, the output voltage of renewable energy, particularly wave energy, fluctuate due to its nature. To address this issue, a high step-up DC-DC boost converter is required to boost the voltage and interface it to the DC-link of the inverter with the

power grid, as displayed in Figure 1.2. A voltage gain in excess of 5 is difficult to attain with conventional DC-DC boost converter topologies due to the requirement for a duty cycle in excess of 80%. This thesis focuses on the design of high gain DC-DC converter topologies that demonstrate enhanced voltage gain (ten times or higher), increased efficiency, and reduced voltage stresses across the active devices that are suitable for the integration of wave energy to the distribution grid in the UK via a MVDC collection network.

1.3.2 Solid State Transformer

The Solid State Transformer (SST) is one of the state-of-the-art technologies that can contribute to the integration of renewable energy to the distribution grid by enabling the grid connection of renewable energy sources. SST technology is a rapidly evolving topic which is taking advantage of wide bandgap semiconductor devices and is not yet mature.

Significant research is being undertaken to assess the possibility of replacing the physically large line frequency magnetic transformer used in the distribution grid with SST circuits. SST topologies generally consist of multistage power electronics converters isolated with a high frequency transformer (HFT) which can control the input and output power, taking into account the voltage level using a number of switched electronic devices [29]. The primary function of the SST is to facilitate the increase or decrease of the voltage in a similar manner to the main function of a line frequency transformer.

A typical SST consists of an AC-DC rectifier, a DC-DC converter with HFT and a DC-AC inverter, as shown schematically in Figure 1.4 [30]. The fundamental operation of the SST is, at first, to rectify the 50 Hz AC voltage to DC. Then, this DC voltage is stepped up using a DC-AC inverter coupled to an HFT (with significantly

decreased volume and weight in comparison to a 50 Hz transformer) before being rectified to give a DC voltage. Finally, the DC voltage is converted into the desired 50Hz AC voltage, which connects to the distribution grid [31, 32]. The main advantage of SST over traditional LFT is the reduction in volume, which is dominated by the size of the transformer core and windings, which reduces as inverse of the cube of the operating frequency [33]. SST circuits have the ability to perform additional functionality with the help of semiconductor devices, including protection circuits to prevent power supply and load disturbances, allow bidirectional flow, realise voltage sag compensation, as well as controlling the output voltage. The input circuits offer the possibility of having a DC input or output, enhanced voltage regulation, and fault isolation [34-36], as well as the ability to integrate power storage at the low and high voltage DC links.

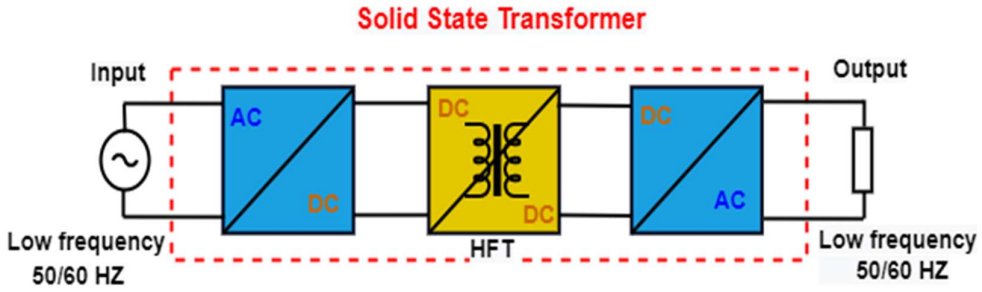

Figure 1.4: Schematic representation of the three stages SST.

The second stage of SST, which is identical in function to that of a high gain DC-DC converter, is the origin of the voltage boost. Thus, this is another motivation behind this thesis to focus on the design of a high gain DC-DC converter suitable for the integration of renewable energy sources to the distribution grid in the UK. The high gain DC-DC converters addressed in the following chapters can be considered as an alternative to traditional HFT and placed on the second stage of the SST.

1.4 THESIS OBJECTIVE

High voltage gain DC-DC converters are essential for efficiently converting low input voltages to significantly higher output voltages, enabling an efficient energy transfer in various applications. High voltage gain is theoretically feasible with conventional boost converters when the converters operate under excessive (>80%) duty cycles, resulting in substantially degraded efficiency. Since the high voltage conversion ratio requires a higher-rated device with large on-state resistance, the switch in the conventional boost converter has high voltage stress and conduction loss. Therefore, achieving a high voltage gain while avoiding severe duty cycle operation conditions is one of the primary challenges in converter design.

The research in this thesis aims to generate MVDC from renewable energy sources like wave energy. The main objective is to investigate, develop, design and test different connections of high gain DC-DC power conversion systems to achieve a high voltage conversion ratio (ten times or higher) that fulfils the condition of emerging distributed power generation systems, enabling the grid connection of renewable energy sources. The main objective and research contributions will be accomplished through the following specific objectives:

- To Study and design suitable high gain DC-DC converter topologies for WECs.
- To develop and prototype a 5 kV transformerless single switch- single inductor multilevel boost converter (MBC), which has the ability to realise high voltage gain without the need for an extreme (>80%) duty cycle, resulting in low voltage stress on the switching device and the creation of self-balanced voltage levels at the output.

- To develop and design a 5 kV transformerless switch inductor multilevel boost converter (SIMBC), which can achieve higher voltage gain with less duty cycle and low switch voltage stress and attain the output voltage balanced at all levels.
- To develop and build a 5 kV transformerless voltage lift switched multilevel boost converter (VLSIMBC), which can realise higher voltage gain with a lower duty cycle and less voltage stress on the components and self-balanced at the output voltage levels.
- To propose a novel Z-source multilevel boost converter (ZSMBC). The desired benefits include high voltage gain, less duty cycle and ensuring self-balanced voltage levels at the output.
- To validate and evaluate all the developed and proposed transformerless high gain DC-DC converter topologies through computer simulation using Pspice software and then build the prototype.
- To present a compression among the proposed high voltage gain topologies MBC, SIMBC, VLSIMBC and ZSMBC in terms of the number of devices, voltage gain, duty cycle, voltage stress across the switch and efficiency.

1.5 THESIS STRUCTURE

The thesis is organised as follows:

In Chapter 2, a comprehensive review of step-up DC-DC converter topologies with a high conversion ratio is presented. The categories of DC-DC boost converters, including isolated/non-isolated and unidirectional/bidirectional converters, are defined. Furthermore, various topologies that have the potential to overcome the conventional boost converter's limitations and enhance the voltage gain are analysed.

The main features and limitations associated with each method topology are discussed, and a clear explanation of why transformerless high-gain DC-DC converters are preferred in this research is given.

Chapter 3 describes a transformerless DC-DC multilevel boost converter (MBC) topology, which integrates the circuit of a conventional boost converter with a switched capacitor technique to produce a high voltage gain of ten times or more and self-balancing outputs, thereby sustaining the same output voltage for all output levels. Besides, this topology only requires a single switching device, reducing the complexity of the control strategy. The circuit regulates the voltage through the use of pulse width modulation (PWM), which only requires a single switch, a single inductor, (2N-1) diodes, and (2N-1) capacitors to provide an output that is N times more than what would be produced by a traditional boost converter working under the same conditions. A 5 kV laboratory prototype of the three-level MBC was built to verify the theoretical study and simulation results. Simulation and experimental results with power loss analysis are presented to validate the effectiveness of this converter in a high step-up application.

In Chapter 4, since the transformerless DC-DC MBC topology discussed in Chapter 3 has been verified to be an effective topology for acquiring a high conversion ratio, further efforts have been made to develop and examine enhanced transformerless high gain topologies capable of achieving precise higher conversion ratios with a lower duty cycle. The transformerless DC-DC high voltage gain converter topologies explained in this chapter are development on the multilevel boost converter (MBC) concept; the switched inductor multilevel boost converter (SIMBC) and voltage lift switched inductor multilevel boost converter (VLSIMB) intending to realise a voltage gain of ten or higher with reduced voltage stress on devices. Simulation and hardware

results of 5 kV three-level SIMBC and VLSIMBC topologies justify the theoretical observations. In addition, an assessment evaluation and comparison of the three-level MBC, SIMBC, and VLSIMC topologies are discussed.

Chapter 5 proposes the Z-source multilevel boost converter (ZSMBC) as a novel transformerless DC-DC step-up converter. The Z-source network is incorporated into the multilevel boost converter to provide a high voltage gain with self-balancing outputs, thereby keeping the output voltage the same while ensuring that each level receives an equal amount of the overall voltage output. The proposed transformerless DC-DC high voltage gain converter explained in this chapter is based on a single, low-sided transistor to realise a ZSMBC, where the control strategy is identical to that of MBC, SIMBC and VLSIMBC topologies presented in previous chapters. In addition, a 3 kV laboratory prototype of the proposed three-level ZSMBC has been implemented. Simulation and experimental results with the power losses are provided to verify the converter's operation and theoretical analysis. The proposed topology is well-suited for use in various practical applications, including wave energy converters and solid-state transformers since it enables a high voltage conversion ratio with a lower duty cycle.

Chapter 6 summarises the work presented in this thesis and provides recommendations for future research.

Chapter 2: A Literature Review of High Step-Up DC-DC Converter Topologies

2.1 INTRODUCTION

High voltage gain DC-DC converters, particularly step-up DC-DC converters, have acquired significance recently due to their wide application in power conversion systems for MVDC and HVDC transmission. Step-up DC-DC converters have been widely employed in various modern applications, including high-intensity discharge lamps, electric vehicles, and grid-connected renewable energy sources, since their invention in the 1950s [37-39]. In order to boost the relatively low output voltage of renewable energy sources to the voltage level required, these applications necessitate converters with a high voltage gain, frequently ten times or higher. However, for this voltage step-up, conventional boost converters experience challenges such as high duty cycles, high switch voltage stress, and severe diode reverse recovery losses.

The basic principle of step-up DC-DC converters is transferring energy to passive components, including inductors and capacitors, followed by energy release to the load. Hence, these converters may efficiently boost voltages through various combinations. Nevertheless, the voltage rating of the semiconductor switching device increases as the output voltage rises, and high input currents occur due to low input voltages. This condition can significantly influence the system's performance due to the conduction losses of the semiconductor device. Additionally, the converter may exhibit an insufficient dynamic response due to the components and possible load variations when the duty cycle approaches unity [9, 40, 41].

A number of DC-DC converter topologies, which include both isolated and non-isolated designs, have been highlighted in the literature for achieving high voltage gain. High voltage conversion ratios can be attained in transformer-based DC-DC converters by modifying the turns ratio. However, a high turns ratio causes substantial leakage inductance besides the stray inductance emerging from the circuit's layout. Furthermore, high-rated switches with significant on-state resistance are also critical due to the high conduction loss caused by large voltage spikes [6, 42]. Other approaches for increasing the output voltage involve passive components including capacitors and inductors. Energy is transferred to the passive components from the input sources, leading to an increase in voltage across the components. Consequently, the passive components are directly connected to input sources to discharge the stored energy. The increased output voltage can then be defined as the sum of the input voltage and passive elements' voltages. Likewise, several approaches exist for obtaining higher voltage gains by integrating multiple converters. For example, it is possible to connect the first boost converter's output port to the next boost converter's input port to increase the voltage gain. Furthermore, the voltage multiplier (VM) structure can even further boost the voltage gain. Power conversion researchers and industries continue to make significant efforts to fulfil the high gain requirement in DC-DC converters, advancing semiconductor devices technology and designing new converter topologies. This thesis addresses the latest by proposing new high-gain DC-DC converter topologies utilising the most recent wide bandgap semiconductor devices.

In this chapter, an overview of methods for improving high conversion ratio DC-DC boost converters is presented. The first section of this chapter outlines the categories of DC-DC boost converters in terms of isolation and power flow direction.

The following section assesses various topologies to overcome the boost converter's limitations and enhance the voltage gain. The significant advantages and drawbacks concerning each technique are highlighted, and the motivation for preferring the transformerless high-gain DC-DC converters in this work is demonstrated clearly. Moreover, the classification of non-isolated DC-DC boost converters with and without a wide voltage conversion ratio is discussed.

2.2 CATEGORIES OF DC-DC BOOST CONVERTERS

Step-up DC-DC converters can be classified based on their topologies, operating principles, performances and applications [43]. Figure 2.1 demonstrates the generic classification of step-up DC-DC converters. According to whether transformers are employed, converters can be divided into two types: isolated and non-isolated converters. Additionally, unidirectional and bidirectional converters are distinguished by the presence or absence of bidirectional power flow through the converters. Furthermore, converters can be categorised as voltage-fed/current-fed and hard-switching/soft-switching converters based on their working principle and implementations.

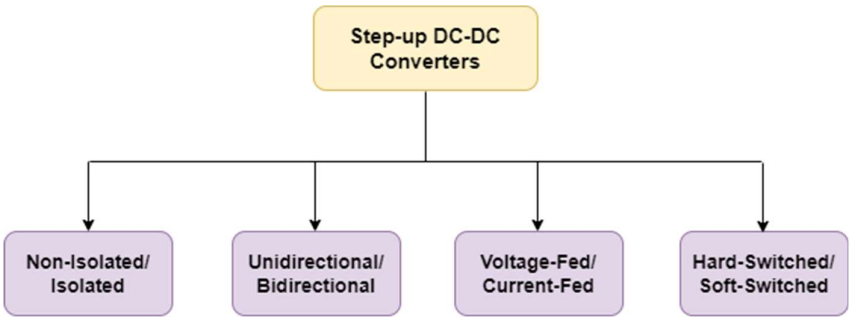

Figure 2.1: Categories of DC-DC boost converters.

2.2.1 Isolated/Non-Isolated Converters

Based on whether transformers supply galvanic isolation or not, DC-DC converters can be classified as isolated or non-isolated. The configurations of non-isolated and isolated DC-DC converters are presented in Figure 2.2. These figures indicate that the input side could be either voltage-fed or current-fed. Besides that, it can be noticed that the switched module includes active switches such as metal-oxide-semiconductor field-effect transistors (MOSFETs) or insulated-gate bipolar transistors (IGBTs) alongside passive components including inductors, capacitors, and diodes. Moreover, the output side load could also include inverters or grid-connected systems.

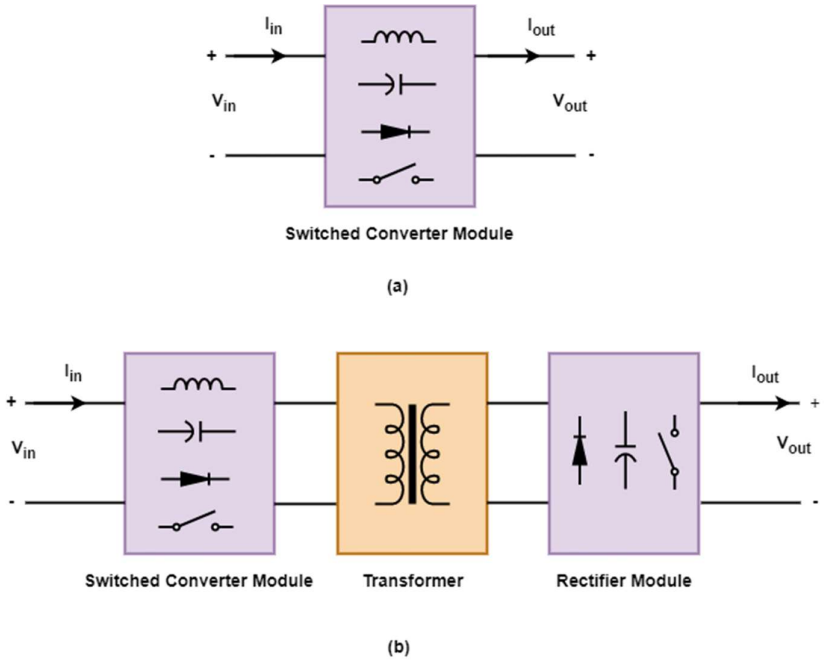

Figure 2.2: Circuit diagram of non-isolated and isolated DC-DC converters: (a) non-isolated; (b) isolated.

An effective technique to achieve galvanic isolation and impedance matching between the source and load is to use isolated DC-DC converters with high-frequency transformers. Isolated DC-DC converters work by first converting the DC input power into AC using a switching converter module and then transferring the AC power to the secondary side of the transformer from the primary side utilising electromagnetic fields. This allows the primary and secondary sides of the transformer to function independently. In most cases, the rectifier is essential for converting AC to DC to provide power to the load. The turns ratio of transformers, in addition to the voltage conversion ratio dependent on the active switches' duty cycles, can further increase the output voltage to a greater level [5, 6, 44]. Isolated boost converters can be operated as either current-fed [45, 46] or voltage-fed [47]. By merely altering the turns ratio, conventional converters that have galvanic isolation, like flyback converters [48] push-pull converters [49], and full bridge converters [50], are capable of acquiring high voltage gain. On the other hand, having a turns ratio that is very high results in a significant leakage inductance, which leads to a substantial voltage spike on the electronic devices. Furthermore, the structure of transformers would result in a considerable increase in both volume and weight, in addition to the rise in power losses. Therefore, the main drawbacks of using isolated DC-DC converters in embedded applications are their increased size, weight, and power losses.

Non-isolated topologies [7-15] can be employed to realise high conversion ratios and efficiencies without the use of a transformer. Accordingly, the high-frequency transformer's size, weight, and losses have significantly decreased. In addition, a transformerless topology is the most desirable option when the application involves high power, and the primary issue is the weight and size [9]. Therefore, utilising non-isolated converters is becoming a more viable solution as it can reduce the system's

cost and increase efficiency. Furthermore, knowing that the size and weight of the passive components in non-isolated converters exhibit an inverse relationship with the frequency, the components can function at converter switching frequencies in the range of tens of kilohertz (kHz) or higher. In brief, isolated DC-DC topologies are preferred for applications that demand isolation between the source and the load due to safety concerns, while, non-isolated DC-DC converters are more appropriate for high-power applications, in which the most crucial consideration is the volume or weight of the converters.

2.2.2 Unidirectional/Bidirectional Converters

Unidirectional DC-DC converters only transfer power from input to output. In contrast, bidirectional converters are capable of transferring power in both directions and are frequently employed in systems that contain batteries, such as electric vehicles (EVs) [43]. Typically, unidirectional DC-DC converters can be converted into more developed bidirectional DC-DC converters by adding additional active switches, as displayed in Figures 2.3 and 2.4. Figure 2.3 (a) depicts the conventional boost converter as a basic layout of a unidirectional DC-DC converter, often constructed using unidirectional semiconductor devices like power MOSFETs and diodes. This converter only allows for one power flow path due to employing a single-quadrant switch, which deters current from flowing in the opposite direction through the diodes. In contrast, Figure 2.3 (b) illustrates the bidirectional configuration of a non-isolated DC-DC converter. This structure can be realised by replacing the diode with current-bidirectional two-quadrant switch operated in unidirectional topologies [43]. Unidirectional converters are preferable over bidirectional converters due to the fewer controllable switches and, as a result, more straightforward control implementation

that unidirectional converters have. This is especially true when unidirectional power flow is needed.

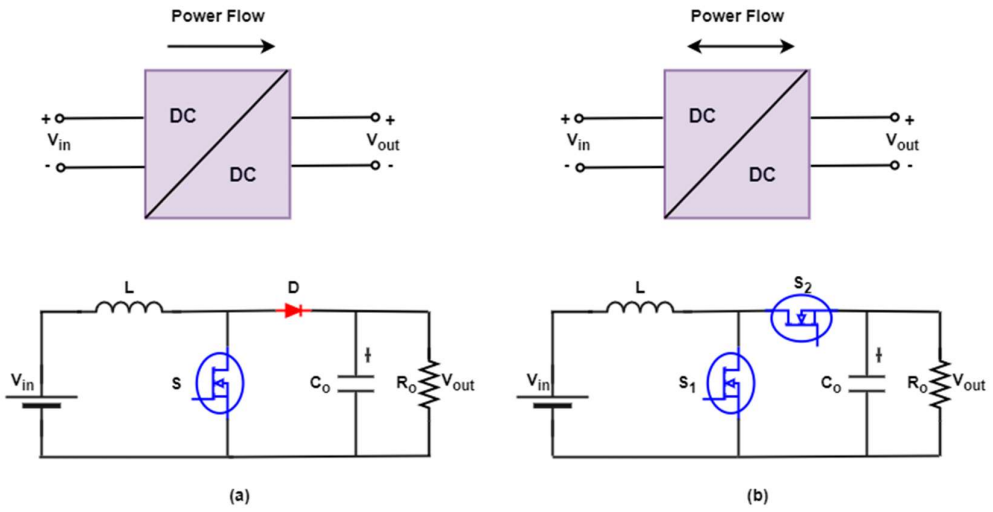

Figure 2.3: Circuit power flow of non-isolated unidirectional/bidirectional DC-DC converters: (a) unidirectional boost converter; (b) bidirectional boost converter.

Similarly, the isolated version of unidirectional/bidirectional DC-DC converters are shown in Figure 2.4. The isolated unidirectional design with a full-bridge DC-DC converter shown in Figure 2.4 (a) is a popular topology of this family [43]. This configuration also features a diode rectifier on the secondary end to restrict the current flow path. On the other hand, the isolated bidirectional converter features a symmetrical design that allows power to flow in either direction. A schematic of an isolated bidirectional converter is displayed in Figure 2.4 (b), along with a widely used instance of a bidirectional DC-DC converter known as a dual active bridge (DAB) derived from a unidirectional full-bridge DC-DC converter [51].

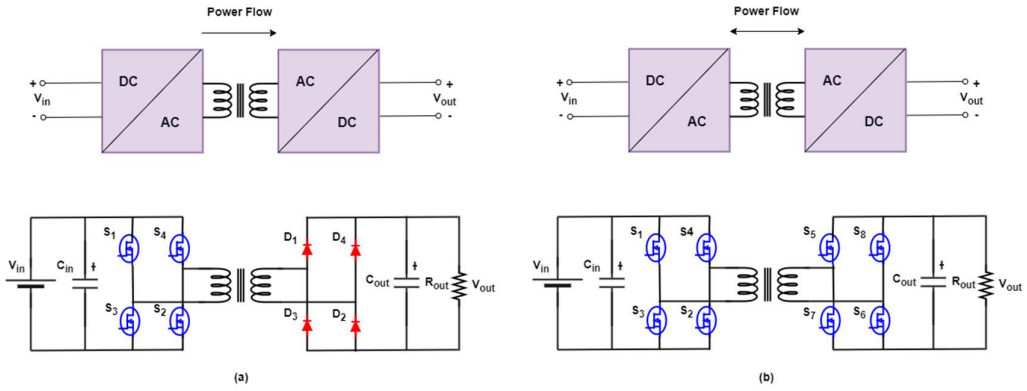

Figure 2.4: Circuit power flow of isolated unidirectional/bidirectional DC-DC converters: (a) unidirectional full bridge converter; (b) bidirectional dual active bridge converter.

2.3 TOPOLOGY EVALUATION OF THE STATE-OF-THE-ART HIGH GAIN DC-DC BOOST CONVERTERS

The main challenges preventing a high conversion ratio and enhancing the efficiency of basic DC-DC boost converters in high step-up applications are excessive duty ratio operation, conduction losses concerning high-rated power devices, and the output diode reverse recovery loss. This section briefly reviews the existing topologies of DC-DC boost converters and techniques suggested to overcome the limitations of basic converters and attain high gain voltage. Non-isolated converters, including cascade converters, quadratic converters, switched capacitors, switched inductors, voltage lift, voltage multiplier circuits, and Z-source converters, can increase the voltage boost ratios. Furthermore, transformers and non-isolated converters are typically combined to create isolated converters. The turn ratios of transformers would then be used to achieve high voltage conversion ratios.

2.3.1 Conventional Boost Converter

The simplest topology for a step-up DC-DC converter is the conventional boost converter, comprising a single inductor, low-side switch, diode and output capacitor, as shown in Figure 2.5 [43, 52-54]. The converter voltage gain is dependent on the MOSFET duty cycle d and is provided by

$$G = \frac{V_{out}}{V_{in}} = \frac{1}{1-d} \qquad 2.1$$

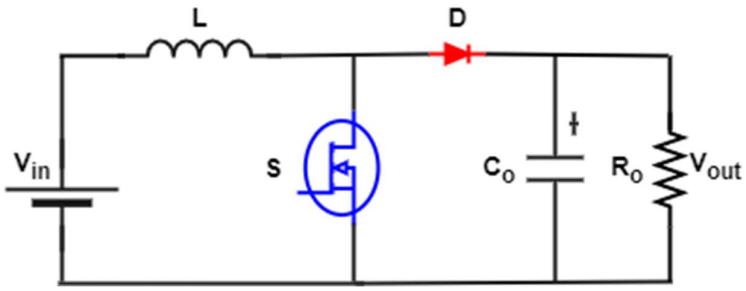

Figure 2.5: Conventional DC-DC boost converter circuit.

PWM signals control the ON/OFF state of the switch. The ratio of ON-time (t_{on}) to switching time (t_{sw}) is the duty cycle d. Increasing the duty cycle d of the active switch S would result in a greater output voltage, according to the equation 2.1. When the switch S is ON, the input source charges the inductor L since the output diode D is OFF. When the switch S is OFF, the output diode D conducts, and the power flows to the load from the input source and the inductor. The output voltage increases because the inductor is considered an equivalent voltage source resulting from the instantaneous voltage. In steady-state, the boost converters has two possible operation modes: continuous conduction mode (CCM), where the inductor conducts current continuously that never falls to zero, and discontinuous conduction mode (DCM), where the current drops to zero for a part of the switching period [43].

Theoretically, the conventional boost converter can achieve a high voltage gain at an exceedingly high-duty cycle. However, in practice, the traditional boost converter has a limited voltage-gain for several reasons. First and foremost, operating at excessively high duty cycles reduces the converter's efficiency and raises the voltage stress across passive and active components [55]. The voltage gain is drastically reduced, and the efficiency suffers due to the switches' conduction losses when the duty cycle is high. Furthermore, in high-power applications, the output diode's blocking of the output voltage may be compromised by the reverse recovery phenomenon [56]. Another drawback is that the converter's weight would rise due to the significant magnetic component needed to maintain continuous conduction mode (CCM) [57]. Therefore, a gain of ten is beyond the capabilities of this converter, which makes this design insufficient for high power applications.

2.3.2 Cascaded Boost Converters

Knowing that conventional boost converters have a limited voltage gain, a cascade structure is utilised to connect multiple converters in series to provide a higher output voltage [58, 59]. Increasing the voltage gain without operating at an excessive duty cycle can be accomplished by cascading two or more conventional boost converters [60]. A two-stage cascaded boost converter, displayed in Figure 2.6 (a), consists primarily of connecting the output stage of the first boost converter to the input of the second boost converter, creating an intermediate bus voltage across capacitor C_1. The two-stage cascaded boost converter's voltage gain can be expressed as follows.

$$G = \frac{V_{out}}{V_{in}} = \frac{1}{(1-d)^2} \qquad 2.2$$

Cascading more conventional boost converters is applicable, as Figure 2.6 (b) illustrates [61]. The cascade topology generates an output voltage which is a product of independent boost stages leading to an increased voltage gain and can be expressed as

$$G = \frac{V_{out}}{V_{in}} = \frac{1}{(1-d)^n} \tag{2.3}$$

where n is the number of the cascaded converters.

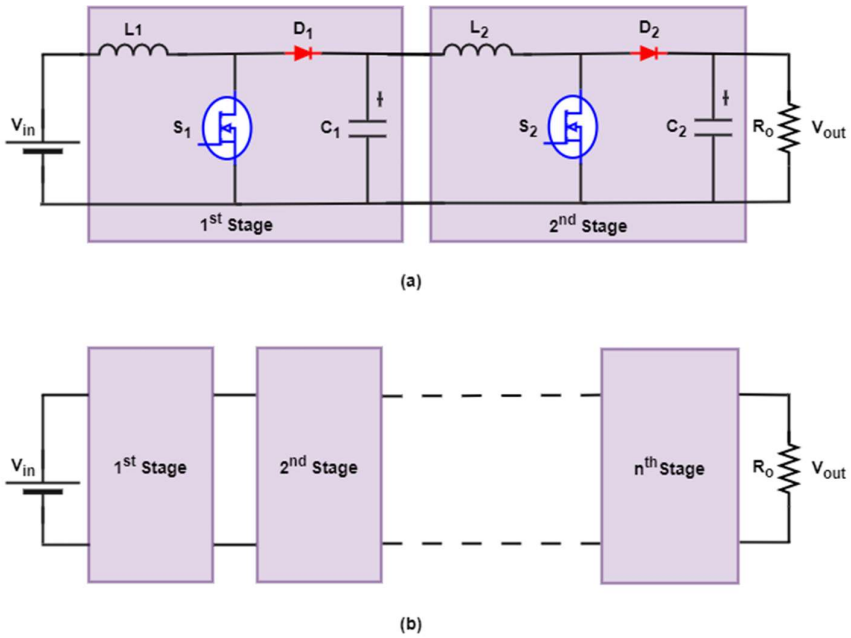

Figure 2.6: Cascade DC-DC conventional boost converter: (a) two stages; (b) n stages.

Every stage in the cascade converter can perform the step-up function without operating at an exceedingly high duty cycle, hence minimising the associated conduction and switching losses. However, the main drawback of cascading multiple boost converters is that the power is processed multiple times, which will reduce the overall efficiency. In addition, the n^{th} stage must employ a high voltage rated switch, which can also be constructed from a combination of switches. A further limitation is

that the output stage's active switch and diode still have to withstand voltages as high as those experienced in conventional boost converters. Three boost stages must be implemented at the lowest possible level to achieve a voltage gain of ten while maintaining the duty cycles below 80%. Unfortunately, this will require three times the amount of elements as a traditional boost converter, significantly increasing the design's size and weight [61].

2.3.3 Quadratic Boost Converter

A quadratic converter is suggested in [61-63] as a solution to the instability challenge experienced by the cascaded two-boost converters by replacing the switch S_1 shown in Figure 2.6 (a) with a diode D_3. Figure 2.7 shows the quadratic boost converter, which consists of two conventional boost converters connected in series by a single switch, with the voltage gain defined in the following equation.

$$G = \frac{V_{out}}{V_{in}} = \frac{1}{(1-d)^2} \qquad 2.4$$

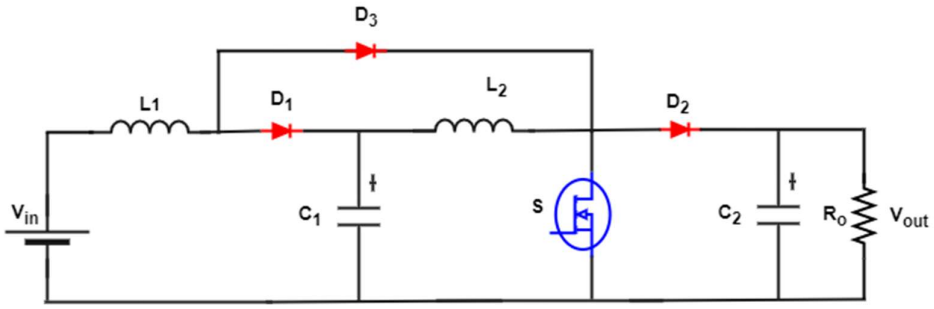

Figure 2.7: Quadratic DC-DC boost converter.

Like the cascaded converters, the overall voltage conversion ratio is the product of the gain of multiple stages; hence, the quadratic boost converter can obtain substantial voltage gain without exposing the switch to an excessive duty cycle. In

addition, taking advantage of a single switch mitigates the number of gate driver circuitry components demanded, reducing the cost. Nonetheless, unlike the cascaded boost converter, each stage cannot be individually controlled [43]. The main limitation of the quadratic boost converter is the reduced efficiency caused by twice conversion of energy. Furthermore, the voltage stress across the switch S and the output diode D_2 is the same as the output voltage; consequently, the converter requires high-rated devices, resulting in raised conduction losses.

2.3.4 Three-Level Boost Converter

The three-level boost was initially developed to minimise the voltage stress across the conventional boost converter's switch and decrease the magnetic components' size by increasing the operating frequency [64, 65]. The typical three-level boost converter is shown in Figure 2.8, including an inductor, two active switches, two diodes, and two output capacitors. This converter's main advantage is reducing the semiconductor devices' voltage stress, where voltage stress across the active switches equals half of the output voltage [64, 66]. Considering the benefits of devices' lower voltage stress, a high-performance MOSFET with low on-state resistance can reduce the conduction losses. The switching loss decreases proportionally as the device voltage stress reduces, and the electromagnetic interference (EMI) noise is dampened. In addition, this converter enables a sizeable reduction in the inductor's size [65]. Following these features, the three-level boost converter is more suitable than the traditional boost converter for applications requiring voltage step-up. However, the most significant disadvantage of this converter is that it is insufficient for applications demanding a wider voltage gain of ten times or higher, as the voltage gain is the same as a conventional boost converter. This implies

operating the converter with an excessive duty cycle to boost the conversion ratio, leading to additional challenges, such as the diodes reverse recovery losses.

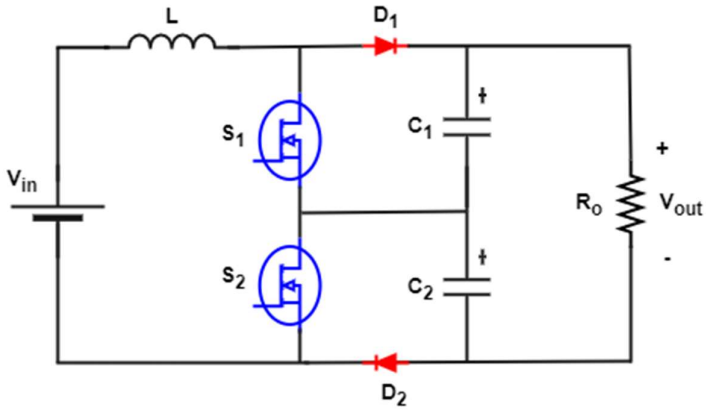

Figure 2.8: Three level DC-DC boost converter.

2.3.5 Switched Capacitor Converter

The switched capacitor is an effective topology for voltage step-up since it enables significant voltage gain over conventional converters [14]. This structure boosts the input voltage, employing charge transfer from capacitors. Traditional converters are connected with a switching cell of two capacitors C_1 and C_2 and two diodes D_1 and D_2 to obtain a high voltage gain. Structures can be either step-up or step-down depending on the cell design; however, only step-up topology is addressed in this section. Figure 2.9 demonstrates the schematic circuit of the switched capacitor converter. The capacitors C_1 and C_2 in the switch capacitor cell will be discharged in series when the main switch of the converter is ON, and the diodes D_1 and D_2 are turned OFF. In contrast, the two capacitors C_1 and C_2 will be charged in parallel by the converter's input voltage when the main switch is OFF, and the diodes D_1 and D_2 are turned ON. As a result, voltage gain can be improved, and voltage stress across the device can be minimised using a switched capacitor cell [67]. Therefore, when

integrated into conventional boost or buck-boost converters, the switched capacitor converter can boost input voltage by transferring charge from the capacitors [14, 68, 69].

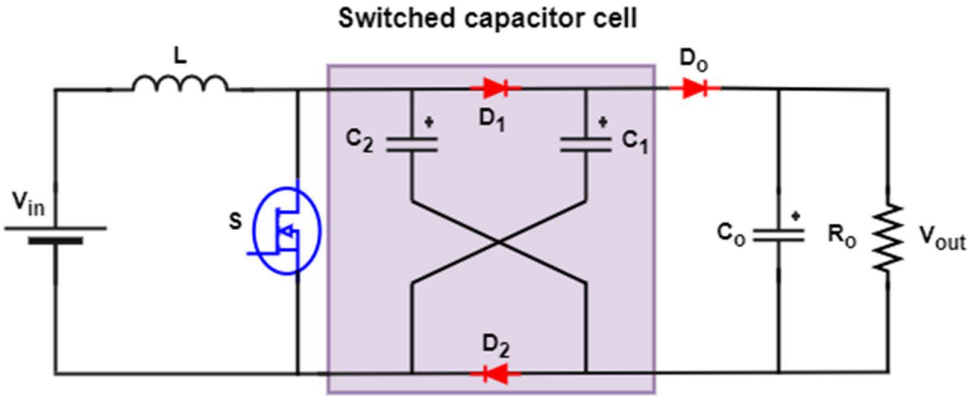

Figure 2.9: Switched capacitor boost converter.

The charge pump is an alternative topology involving switched capacitor circuits; it has been considerably utilised in DC-DC power conversion [69]. The inductors are unnecessary for the operation of the charge pump circuit and it relies only on the charge transfer between the capacitors [70, 71]. The duty ratio of the PWM controls the operation of the converter's power switches. The output voltage is proportional to the number of capacitors utilised, enabling switched capacitor technique to be suitable for creating small, lightweight converters. However, the converter's efficiency decreases dramatically while achieving regulated output voltage because of the high transient current emerging during switching transients and increasing the EMI noise [12, 72]. Furthermore, in high step-up applications, the converter evolves more complicated as the forward voltage drops of the diodes increase. Hence, the overall complexity and cost of the converter rise with the number of active devices and gate drives implemented, limiting its utilisation to applications with low power requirements.

2.3.6 Switched Inductor Converter

The switched inductor technique is suggested to step up the input voltage integrated with a conventional boost converter to develop a new power supply [14]. The design circuit of the switched inductor boost converter is displayed in Figure 2.10. Furthermore, the switched inductor cell comprises of two inductors L_1 and L_2 and three diodes D_1, D_2 and D_3.

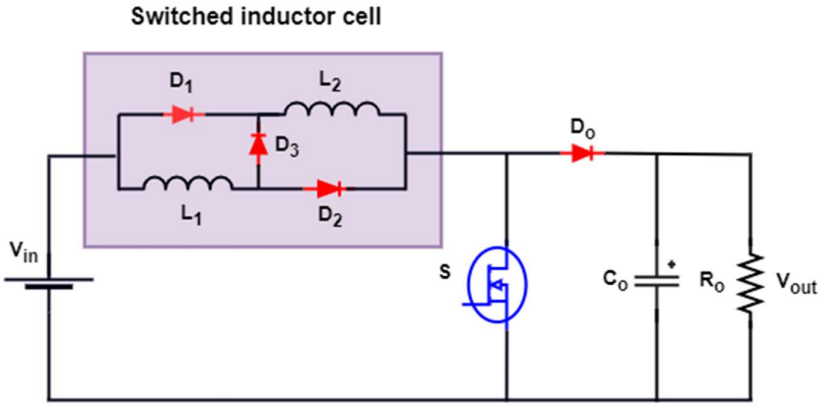

Figure 2.10: Switched inductor boost converter.

Like the operation principle of the switched capacitor converters discussed in the previous subsection, the switched inductor converters can realise high voltage gain, employing the input voltage and inductors charging in series connection [10, 14, 73-75]. While the switch is turned ON, the two inductors L_1 and L_2 are charged in parallel through diodes D_1 and D_2. While the switch is turned OFF, the two inductors L_1 and L_2 are discharged in series through diode D_3 and the power is transferred to the load from the input voltage and the inductors L_1 and L_2. Since the L_1 and L_2 are identical, they will experience the same voltage and an equal share of current flow. Therefore, the input and inductor voltage sum equal the output voltage. However, the main

drawback of the switched inductor converter is that high voltage stress across the active switch equals the output voltage [14]. As a result, switching inductor converter suffers from restricted voltage gain and cannot meet the demands of high-power applications.

Furthermore, if the two inductors are not identical, the values of two inductors currents will be different. A significant switch voltage spike is produced when switched inductors are discharged in series [73]. Overall, the voltage gain can be improved by integrating a switched inductor cell in conventional converters; nevertheless, voltage gains of ten times or more cannot be achieved without an extreme duty ratio. Besides, the substantial conduction losses and severe reverse recovery concerns caused by voltage stress across semiconductor devices restrict its utilisation to low-power applications.

2.3.7 Voltage Lift Converter

The voltage lift circuit cells can enhance the boost abilities of conventional DC-DC converters. Furthermore, they can be designed as integrated cells and connected to conventional converters. This makes them highly versatile. In [14, 68, 76-79], the switched capacitor/switched inductor cell is incorporated into the boost converter, also known as the voltage lift circuit. Figure 2.11 shows a schematic circuit of the voltage lift boost converter, where the voltage lift cell is added to the traditional boost converter leading to an increase in the voltage gain. The voltage lift cell contains two inductors L_1 and L_2, a charge pump capacitor C_v and two diodes D_1 and D_2. The two inductors L_1 and L_2 and the capacitor C_v are charged in parallel when the switch is turned ON through D_1 and D_2 and discharge in series when the switch is turned OFF to obtain a high output voltage. One of the significant advantages of a voltage lift converter is that the input and the output share the same grounding point. This implies

that there is no occurrence of a voltage floating, which further contributes to eliminating EMI [76]. In addition, the current ripple in the components can be mitigated due to the presence of the inductors. However, high duty cycle operation, high voltage stress across the active switch and higher switching losses are the main drawbacks of a voltage lift converter topology and are considered an obstacle to realising high voltage gain.

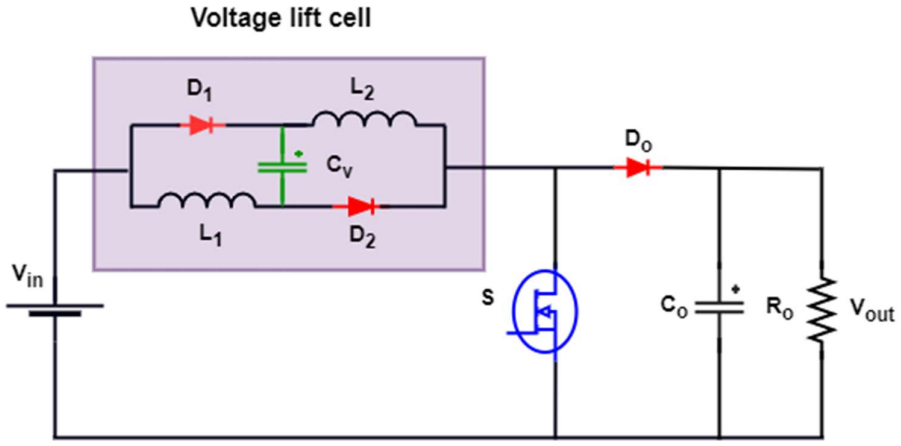

Figure 2.11: Voltage lift boost converter.

2.3.8 Voltage Multiplier Circuit

An alternative approach to overcome the limitations of conventional step-up DC-DC converters in achieving a high conversion ratio is by utilising a voltage multiplier circuit [9]. The voltage multiplier rectifier circuit (VMR) offers a compact and straightforward topology while attaining a higher DC voltage gain compared with the previous topologies discussed. Furthermore, voltage multiplier circuits employ capacitors and diodes to transform AC power into DC power at a significantly high voltage level [9, 80]. The structure of the VMR, particularly an n-stage Cockcroft Walton circuit, is shown in Figure 2.12. Similar to the AC-DC VMR, the multiplier can be operated in the DC-DC topology structure [43, 81]. The present topology

employs an AC source to charge capacitors marked with odd numbers during the first switching period, as illustrated in Figure 2.12. Once the AC source is inverted, the even capacitors will charge [40, 43]. One of the main advantages of this topology is that the output voltage is the sum of the stage voltages duo to the series connection of the capacitors while simultaneously being connected in parallel with the load. In addition, incorporating the voltage multiplier circuit mitigates the weight, size, and power losses arising from using high-voltage power transformers. The voltage gain of a n-stage Cockcroft Walton structure will be n. However, if the output voltage is measured on an odd capacitor, the gain will be n-1 [43]. Acquiring a high conversion ratio is possible by employing extra voltage multiplier stages, however; this can make the system more complicated and costly, coupled with significant voltage drops of capacitors impedance and diodes forward voltage that limit the gain [82].

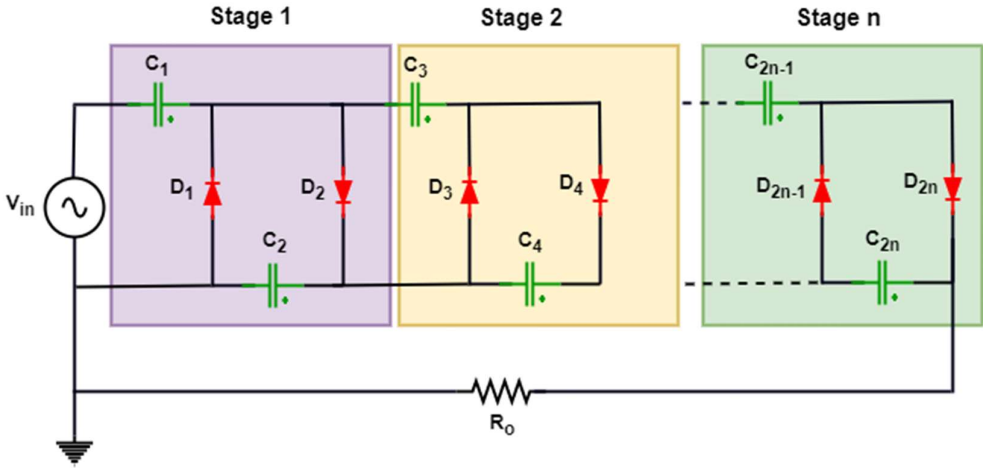

Figure 2.12: Cockcroft Walton voltage multiplier rectifier circuit.

2.3.9 Isolated Boost Converters

Isolated converters can achieve a high voltage gain by adjusting the transformer's turn ratio [6]. High frequency transformers offer isolation between input and output terminals [5]. Additionally, changing the transformer's turn ratio can prevent the semiconductor devices from operating at an excessive duty ratio. Therefore, applications requiring a step-up, wide-range voltage conversion ratio can utilise transformers combined with switching DC-DC converters.

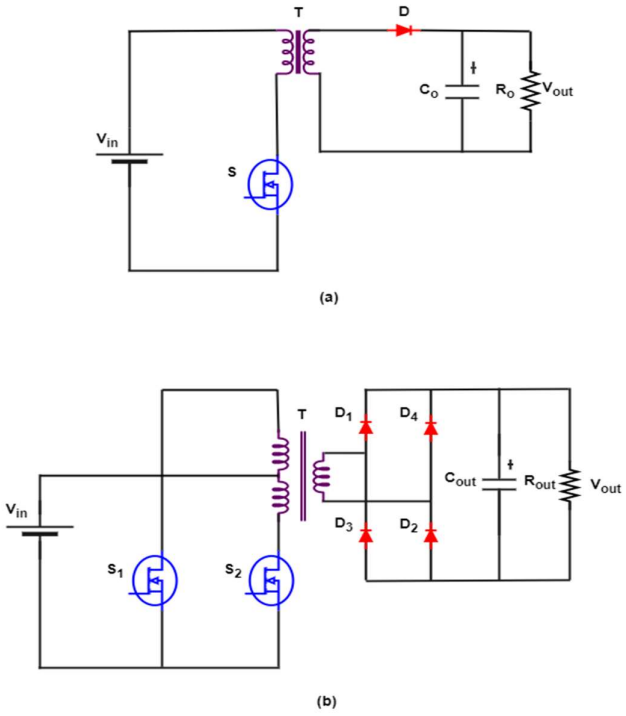

Figure 2.13: Typical isolated DC-DC boost converter topologies: (a) flyback converter; (b) Push pull converter.

Several classic isolated DC-DC converters are suggested to realise high voltage gains, such as the flyback and push-pull converters, as shown in Figure 2.13 [52, 83-85]. Although these converters have the characteristics of a simple circuit and a low

number of switches, they suffer from high voltage stress across the switches, a higher power loss, large current ripples requiring a large EMI filter and the size of transformers. These drawbacks make the isolated flyback and push-pull converters inappropriate for high-gain DC-DC converters.

Other topologies for the high conversion ratio of the DC-DC converters that might overcome these issues are the dual active bridge converter (DAB) and dual half bridge converter (DHB), as depicted in Figure 2.14 [86-88]. The DAB converter is a bidirectional and controllable DC-DC converter due to the symmetry of this converter with an identical primary and secondary bridge. As shown in Figure 2.14 (a), this converter is consisting of eight semiconductor devices, a high frequency transformer (HFT), and DC link capacitors. The DAB converter can be considered as a more common full bridge with a controllable rectifier. Compared to the push-pull converter, the DAB converter has lower voltage stress on the switches, equal to the output voltage.

In contrast, the dual half bridge (DHB) topology, shown in Figure 2.14 (b), requires half as many switching devices as the DAB. However, the main disadvantage of the DHB is that the split DC link capacitors have to deal with the full load of the current. The DHB DC-DC converters have only four switches, resulting in reduced on-state losses compared to DAB DC-DC converters. Even though the cost of the DHB is minimised due to the fewer active switches employed, the transformer's turns ratio will be doubled to achieve the same voltage gain.

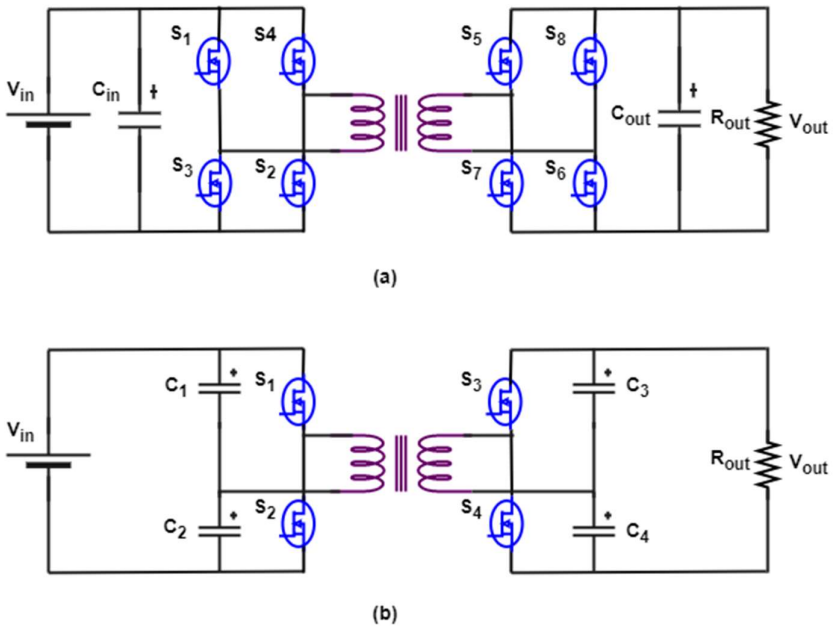

Figure 2.14: Isolated DC-DC boost converter topologies: (a) dual active bridge converter; (b) dual half bridge converter.

A high conversion ratio of ten or higher can be accomplished in isolated converters by modifying the turn ratio. Nevertheless, larger primary current, higher winding losses and volume are associated with a high turn ratio. In addition, the converter's efficiency decreases due to the switching losses. Moreover, the voltage stress across the output diodes is high, necessitating the usage of high-rated power diodes [38, 89].

2.3.10 Coupled Inductor Converters

Coupled inductor-based topologies can accomplish high voltage gain with improved efficiency and decreased inductors' voltage stress [7, 8, 90-92]. Figure 2.15 shows the coupled inductor boost converter, containing a single active switch S, coupled inductors L_1 and L_2, two diodes D_1 and D_o and two capacitors C_1 and C_o.

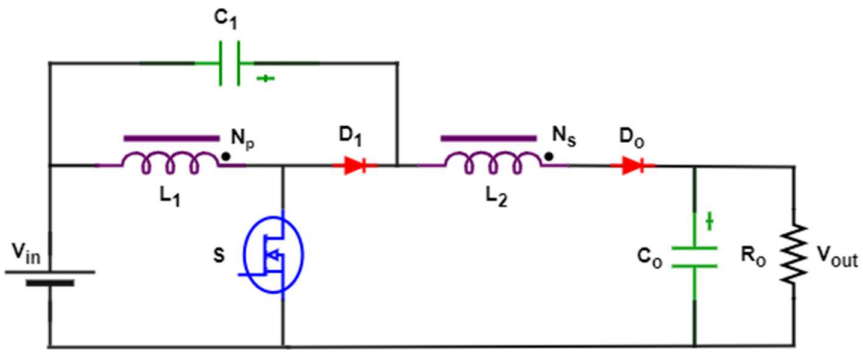

Figure 2.15: Coupled inductor boost converter.

The primary winding of the coupled inductor functions as an input filter inductor, and the secondary winding becomes the voltage source attached in series with the output load to attain high voltage gain. Modifying the turn ratio of the coupled inductor can help to achieve a voltage gain higher than the conventional non-isolated boost converter. Furthermore, a capacitor C_1 is employed to minimise the voltage stress across the active switch *S*, which may further reuse the energy held in the leakage inductance to improve the conversion efficiency. The fundamental operating principle of the coupled inductor boost converter is similar to the conventional boost converter. The energy is kept in the inductor L_1 when the switch is ON, and the energy is delivered to the output load when the switch is OFF. However, the major difference with the conventional boost converter is that the voltage is originated across inductor L_2 when the switch is OFF. As a result, the output voltage is raised due to the presence of L_2 in the main loop. Therefore, coupled inductor converter can realise a higher voltage conversion ratio. The main drawback of the coupled inductor boost converter is that the coupled inductor leakage induces a large voltage spike on semiconductor components, leading to essential energy regenerating methods to limit voltage spikes, which could improve power efficiency but come at a high cost and complex design [7, 91].

2.3.11 Z-source Converter

The Z-Source converter is a promising energy conversion approach that can overcome the obstacle of achieving a high voltage gain in conventional boost converters by employing a distinct impedance network defined as the Z-Source network [93-96]. As illustrated in Figure 2.16, this network consists of two inductors L_1 and L_2 and two capacitors C_1 and C_2 combined in an X configuration, offering an enhanced voltage boost.

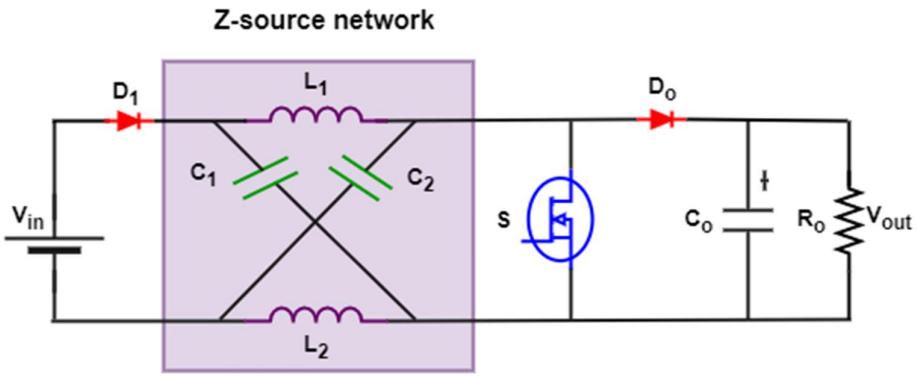

Figure 2.16: Z-source boost converter.

Applying the Z-source network to the conventional converter would give the converter a buck-boost function [93]. Further benefits of the Z-Source converter include enhanced power transfer efficiency, decreased EMI and improved reliability owing to the fewer components applied. Nevertheless, the Z-source converter has several limitations for acquiring the gain of ten or higher, involving extreme duty cycle operation, high voltage stress across the active switch, a significant inrush starting current and discontinuous input current [94, 95].

2.3.12 Integrated Converters

Based on the earlier discussion, a high voltage gain of ten or higher could not be obtained using the abovementioned approaches without any drawbacks. The switches' duty cycles in the conventional boost converter limit the voltage gain. In addition, the voltage gain of cascaded converters and quadratic boost converters can be enhanced by implementing several cells in a series connection; however, this requires many components and results in complicated control. Furthermore, the capacitor charge transfer process is implemented in switched capacitor converter, voltage lift converter and voltage multiplier circuit to increase the voltage conversion ratio. Besides that, the charged inductor technique is employed in the switched inductor converter to realise high voltage gain. Nevertheless, the main disadvantage of these methods and topologies is a substantial increment in the number of components associated with increasing the voltage gain. Additionally, isolated converters and coupled inductor converters can acquire high voltage gain by employing a high turn ratio of transformers. However, this increases size, weight, and power losses and decreases efficiency due to the transformer's core and winding loss.

Researchers interested in high step-up converters with high efficiency have proposed several methods and topologies. Integrating magnetic and capacitive approaches to achieve a high voltage gain in DC-DC step-up converters has been the main objective of most topologies. There have been many suggestions for high step-up converters employing magnetic and capacitive techniques. These methods involve integrated three-state switching cells and voltage multiplier circuits [97], coupled inductor and switched capacitor approaches [98-101], and coupled inductor and voltage multiplier circuits [102-105].

The following explains the most significant features of the integrated topologies. To begin with, a converter's duty cycle can be adjusted to achieve the demanded voltage gain with a suitable duty cycle. Second, the duty ratio can be modified to increase the output voltage, and the magnetic elements' transformation ratio enables appropriate duty ratio operation. Third, selecting a suitable duty cycle reduces the voltage stress across the components and is considerably lower than the output voltage, minimising the conduction losses even more for low-rated power semiconductor devices with low on-state resistance. Similarly, the efficiency of the power devices is increased by reducing the current stress. Finally, the converter's inductors and other passive elements can be designed to be smaller and lighter because they work at the converter's switching frequency.

2.4 CLASIFICATION OF STEP-UP DC-DC CONVERTERS WITH VOLTAGE GAIN

Various step-up DC-DC converters have been suggested to achieve a high voltage conversion ratio and presented in the literature with the evaluation of their advantages and disadvantages. As shown in Figure 2.17, these converters can be further categorised based on whether or not they have a wide voltage gain. Conventional boost, buck-boost and three-level boost converters cannot offer a wide conversion ratio. This is because they have a limited voltage gain and can only adjust one variable, the duty cycle, to increase the voltage conversion ratio. In contrast, step-up DC-DC converters with a wide conversion ratio can be attained using magnetic or capacitive techniques. Integrating switched capacitors, switched inductors, voltage lift circuits, voltage multiplier circuits and transformers into these converters increases the voltage gain.

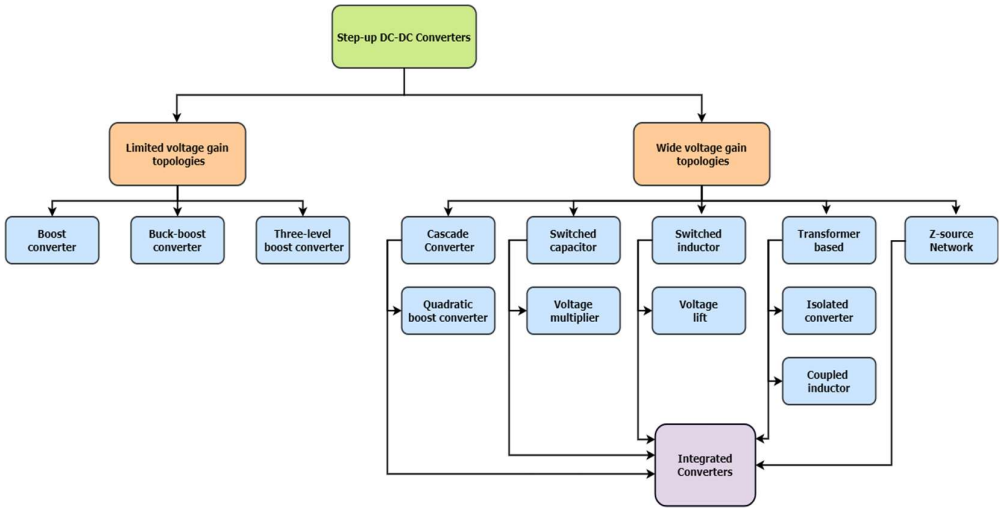

Figure 2.17: Classification of DC-DC step-up converter topologies with voltage gain.

2.5 SUMMARY

In high-step-up applications, excessive duty ratio operation is a significant obstacle to the efficiency of traditional non-isolated converters, including boost and buck-boost. This causes the semiconductor devices to be subjected to severe voltage and current stresses, reducing their performance. This chapter comprehensively analysed the most effective methods for obtaining high voltage gain in DC-DC step-up converters.

Several techniques have been discussed to realise a high conversion ratio without extreme duty cycle operation. For instance, cascade boost converter, quadratic boost converter and three-level converter can increase the voltage gain without excessive duty cycle. Nevertheless, ten times or more voltage boost is required in some high-power applications, such as wave energy, making these converters inefficient. Therefore, other topologies have been addressed to attain a high voltage gain, including switched capacitor converters, switched inductor converters, isolated boost

converters, coupled inductor converters and Z-source converters. Despite this, there are drawbacks to every converter, involving issues with leakage inductance, low power efficiency, complex design, and a high component count resulting in cost increase. Hence, many researchers are concentrating on developing topologies integrating the capacitive and magnetic techniques to address the abovementioned concerns. The concept of developing high gain DC-DC boost converters is reviewed. According to the literature review presented in this chapter, the significant challenges in high step-up DC-DC converter topologies are excessive duty cycle operation, high voltage stresses across the devices, and high-power losses. The research in the thesis is motivated by the limitations and drawbacks of the earlier discussed topologies. In the following chapters, four topologies are proposed to improve the existing topologies, achieve a gain of ten or higher and attain desirable features.

Chapter 3: High Gain Transformerless DC-DC Multilevel Boost Converter Analysis and Design

3.1 INTRODUCTION

A high step-up DC-DC converter can be developed by incorporating a boost stage with a voltage multiplier (VM) stage, as shown schematically in Figure 3.1. This topology is used to overcome the limitations of conventional topologies in high step-up converters. Depending on the configuration, the generic structure of the high gain converter has two stages. The first stage is a boost stage on the input side which integrates single inductor, switched inductor, or voltage lift switched inductor circuits. The second stage is a VM stage on the output side. This structure generally produces a gain of ten times or higher, which many emerging applications demand [106]. The use of a high switching frequency leads to a small size of the converter and suggests the use of wide bandgap semiconductor devices for the switch and diodes [75].

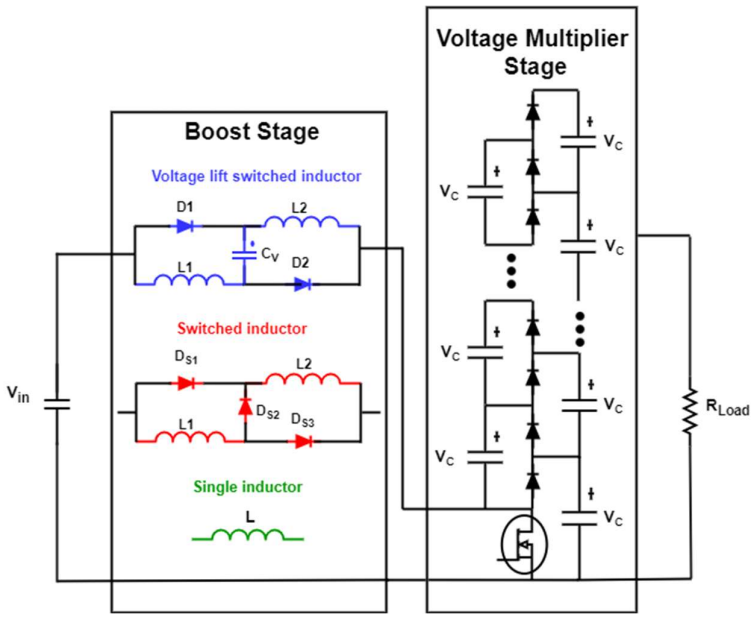

Figure 3.1: Generalized platform for high voltage gain DC-DC conversion.

A number of DC-DC converter topologies, which include both, isolated and non-isolated topologies, have been highlighted in the literature for achieving high voltage gain. Isolated topologies that utilize a high-frequency transformer [5, 6, 42] have the potential to provide isolation between input and output terminals. By adjusting the turns ratio of the transformer, isolated converters can offer a high voltage gain [5]. Nevertheless, isolated DC-DC converters are not a suitable for achieving high conversion ratios due to power transformer losses and the stray inductance arising from the circuit layout, in addition to the weight and large volume of the converter [6, 42]. Non-isolated topologies [7-15] can attain a high gains and efficiencies without the need of a transformer. Coupled-inductor-based [7-9] and non-coupled inductor-based types such as cascade boost, switched capacitor and switched-inductor [10-15] are two categories for the description of non-isolated step-up DC-DC converters. The coupled-inductor-based topologies offer a high voltage gain with enhanced efficiency and reduced voltage stress on the inductors in comparison to isolated converters. However, the linked inductor leakage issue creates a large voltage spike on semiconductor components, and the circuits are challenging to design due to the voltage spikes that can emerge at unexpected times and amplitude, making it difficult to design a circuit that can tolerate them. High voltage conversion ratios with high input current ripple can be achieved using dual-switch-based converters [11, 12]. In these topologies, a second active switch and gate drive are required. Research published in the literature suggests that the cascaded two-stage boost converters have the potential to realize high voltage gain [13]. In this converter, the voltage stress across the switch is equal to the output voltage, necessitating a higher rated switch, which leads to increased conduction losses. In addition, the inductor current ripple is similar to that found in a conventional boost converter (CBC).

This chapter presents a transformerless single-inductor DC-DC multilevel boost converter (MBC) with the aim of realizing a voltage gain of ten and low voltage stress on the semiconductor devices. The transformerless DC–DC MBC described in this chapter is a converter topology that combines the circuit of the conventional boost converter with a switched capacitor circuit to generate a high voltage gain coupled with self-balancing outputs, that maintain the same output voltage, where each level shares an equal portion of the total voltage output. This topology also, reduces the complexity of the control strategy by only requiring a single low side switching device, simplifying the gate drive requirements [107, 108]. The circuit controls the voltage by implementing pulse width modulation (PWM) using a single switch, one inductor, (2N-1) diodes and (2N-1) capacitors for obtaining an output which is the number of levels (N) times that for a conventional boost converter operating under the same conditions. The number of levels (N) in the circuit and hence the output voltage can be increased by the addition of capacitors and diodes to the fundamental boost converter topology. This enables the circuit to be used as a power converter in applications where multiple controlled voltage levels with self-balancing are required when operating in a unidirectional current flow application, such as PV system [107]. The converter operating principle along with the performance analysis and design consideration are described in detail. Simulation and experimental results with power losses analysis are included to verify the effectiveness of the presented converter in a high step-up application.

3.2 CONVERTER MODES OF OPERATION

3.2.1 Circuit Configuration and Description

Figure 3.2 shows a schematic of the three-level DC-DC MBC converter [107, 109], which comprises, one inductor, one switch, 5 diodes and 5 capacitors. In general,

the converter topology is defined as having three-levels. The boost converter is PWM controlled at the gate contact of the power MOSFET and has the potential to provide an equal voltage at all three output levels. The converter is based on a conventional DC-DC boost converter topology with the output voltage of the MBC is three times, that of the output voltage of the conventional converter. The other significant advantage of this topology for the realization of high voltages is that the voltage across each level is $\frac{V_o}{3}$, where V_o is the output voltage. This allows for significantly reduced voltages on other components compared to other high voltage topologies reducing the need for high performance components. Furthermore, the use of a high voltage topology designed for reduced voltage stress on semiconductor devices can contribute to higher efficiency by minimising circuit losses caused by component stress.

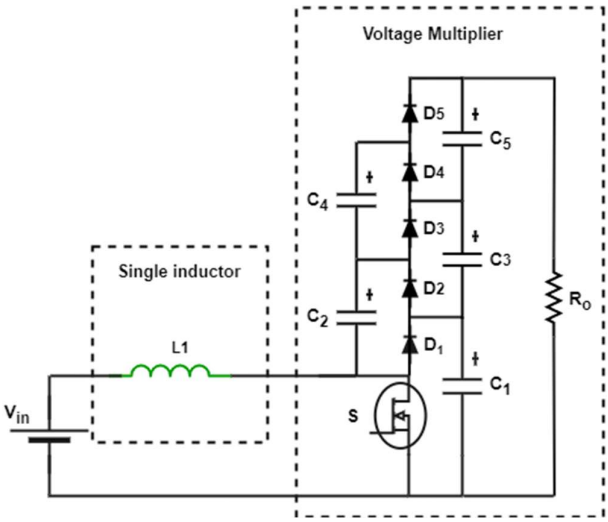

Figure 3.2: Circuit diagram of the three-level high gain DC-DC MBC.

Surge currents between the capacitors in a voltage multiplier circuit can significantly affect the performance and reliability. These surge currents arise during switching when rapid capacitor charging or discharging, resulting in voltage spikes and component stress [81]. Moreover, they can cause switching losses in diodes and MOSFET, reducing overall circuit efficiency and generating EMI. Thus, voltage

regulation may suffer, leading to output voltage instabilities. To address these concerns, careful component selection and proper circuit design are essential for ensuring reliable circuit operation.

3.2.2 Converter Operation Principle

The operating principle of the MBC can be described in terms of two operating modes; one when the switch is turned ON and the other when the switch is turned OFF. The converter has been designed to operate in continuous conduction mode (CCM) and throughout the entire range of duty ratio variation with resistive loads such operation is assured. To simplify the circuit analysis of the converter, all the components are initially considered to be ideal, and the inductor current is increased and decreased linearly. The steady state waveform of the MBC is shown in Figure 3.3.

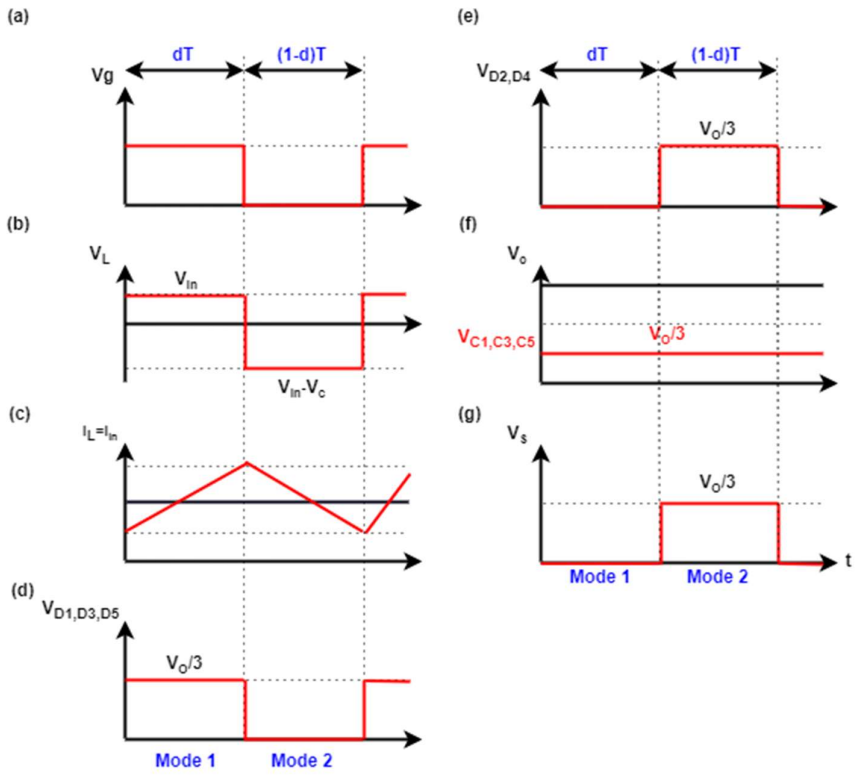

Figure 3.3: Main steady state waveforms of gate voltage, inductor voltage and current, output diodes voltages, output capacitors voltages and switch voltage for MBC.

The operating characteristics that occur during the two modes are described as:

In Mode 1, when the switch is turned ON as shown in Figure 3.4, the inductor is connected to the input voltage. If the voltage across C_2 is smaller than that across C_1, C_1 charges C_2 through the diode D_2 and the switch, as indicated in Figure 3.4 (b). At the same time, if the voltage across $C_2 + C_4$ is smaller than the voltage across $C_1 + C_3$, C_1 and C_3 charge C_2 and C_4 through the diode D_4 and the switch, as shown in Figure 3.4 (C) [107, 109].

In Mode 2, when the switch is turned OFF as shown in Figure 3.5, diode D_1 conducts allowing the energy stored in the magnetic field in the inductor to charge capacitor C_1 until the voltage on this capacitor is equal to the voltage which is the sum of the input voltage and the inductor voltage, as shown in Figure 3.5 (a). Then, diode D_3 conducts so the input voltage, the inductor and capacitor C_2 charges capacitors C_1 and C_3 as indicated in Figure 3.5 (b). When the voltage on $C_1 + C_3$ is equal to the total voltage of the input voltage, the inductor voltage and the voltage on the capacitor C_2, diode D_3 turns off and diode D_5 conducts, so that the inductor and capacitors C_2 and C_4 charge capacitors C_5, C_3, C_1 until the voltage is equal to the summation of the voltage on the input voltage, inductor and capacitors $C_2 + C_4$ as indicated in Figure 3.5 (c) [107, 109].

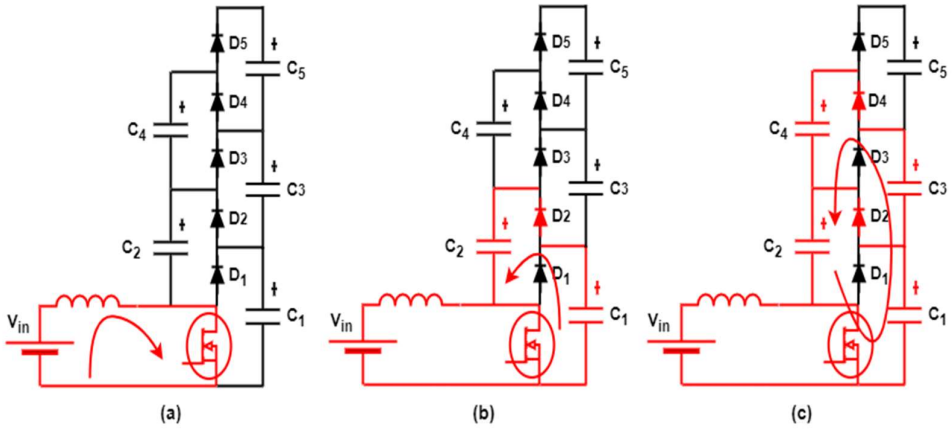

Figure 3.4: Operation of the three- level MBC when the switch is ON.

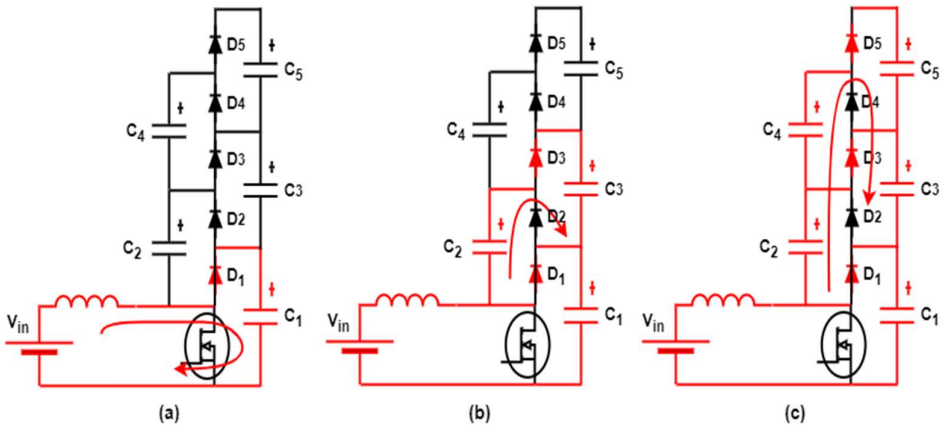

Figure 3.5: Operation of the three-level MBC when the switch is OFF.

3.3 STEADY STATE PERFORMANCE ANALYSIS

3.3.1 Voltage Gain

In the MBC circuit, the input power is transferred to the output by charging and discharging the switched-capacitor voltage doubler. In the analysis of the MBC, all the components are initially considered to be ideal, and the inductor current increases and decreases linearly with time. In Mode 1, when the switch is turned ON, as shown schematically in Figure 3.3; the time interval in this mode is dT, where d is the duty cycle of the switch, S, during one switching period T. Diodes D_2 and D_4 are forward-biased, and current begins to flow through the inductor. Thus, the inductor voltage is expressed as, $V_L = V_{in}$. In Mode 2, when the switch is turned OFF, as shown in Figure 3.3. This interval time is $(1-d)\,T$. Diodes D_1, D_3 and D_5 are forward-biased and the inductor delivers the stored energy to the load. This leads to,

$$V_L = V_{in} - V_{c1} \tag{3.1}$$

and

$$V_o = V_{c1} + V_{c3} + V_{c5} \tag{3.2}$$

The average inductor voltage V_L over one switching cycle is zero at steady-state operation and can be determined from

$$V_L = d\,(V_{in}) + (1-d)(V_{in} - V_{c1}) = 0 \qquad 3.3$$

Where V_{in} is the input voltage, V_o is the output voltage, and D is the duty cycle.

The voltage across C_1 is equal to that expected for a conventional boost converter topology and so when the converter is operating in the steady state, with identical output capacitors, the capacitor voltage and output voltage may be expressed as

$$V_o = 3V_C = \frac{3}{1-d}V_{in} \qquad 3.4$$

The three-dimensional view of the ideal voltage gain G is plotted as a function of duty cycle d and the number of levels N, as shown in Figure 3.6. The data shows that the voltage gain increases with the number of levels. The duty cycle increases as the voltage gain increases, and this relationship usually informs the choice of a certain voltage gain.

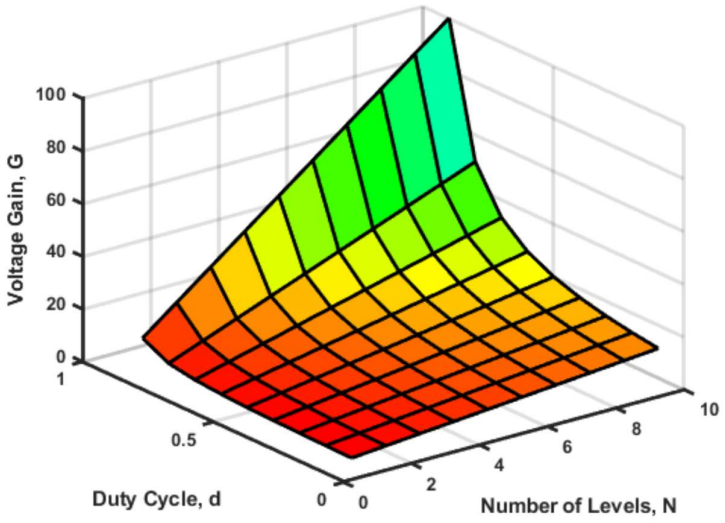

Figure 3.6: Ideal Voltage gain characteristic of the MBC as a function of d and N values.

The average inductor current I_L can be determined from the knowledge of output current and the input and output voltages. Assuming 100% efficiency for the converter, this results in

$$I_L = \frac{{V_o}^2}{V_{in} R_o} \tag{3.5}$$

Substituting the voltage gain from equations 3.4 and 3.5 enables the inductor current, I_L, in the MBC topology shown in Figure 3.2 to be expressed as:

$$I_L = \frac{3V_o}{(1-d)R_o} \tag{3.6}$$

In a practical circuit, the influence of the equivalent series resistance of the inductor ($R_{ESR,L}$) must be considered, therefore the voltage gain can be expressed as:

$$\frac{V_o}{V_{in}} = \frac{3(1-d)R_o}{(1-d)^2 R_o + 9R_{ESR,L}} \tag{3.7}$$

It can be observed from equation 3.7 that the presence of the inductor $R_{ESR,L}$ reduces the voltage gain of the MBC. Therefore, to attain the desired output voltage in a practical converter, the duty cycle must be increased.

The curve of the voltage gains of three-level MBC as a function of duty cycle demonstration the effect of the equivalent series resistance of the inductor ($R_{ESR,L}$) is shown in Figure 3.7. It can be seen from the data the effect of including the inductor equivalent series resistance (ESR) degrades the voltage gain and requires an increase in the duty cycle to achieve the required voltage conversion ratio. To achieve a gain of ten, MBC must operate at 0.75 with ESR is equal to 1 Ω. In contrast, the duty cycle of MBC with the ESR of 0.028 Ω is 0.72. Additionally, it can be noticed that the difference will be significantly increased when the MBC operates over 75% of the duty cycle.

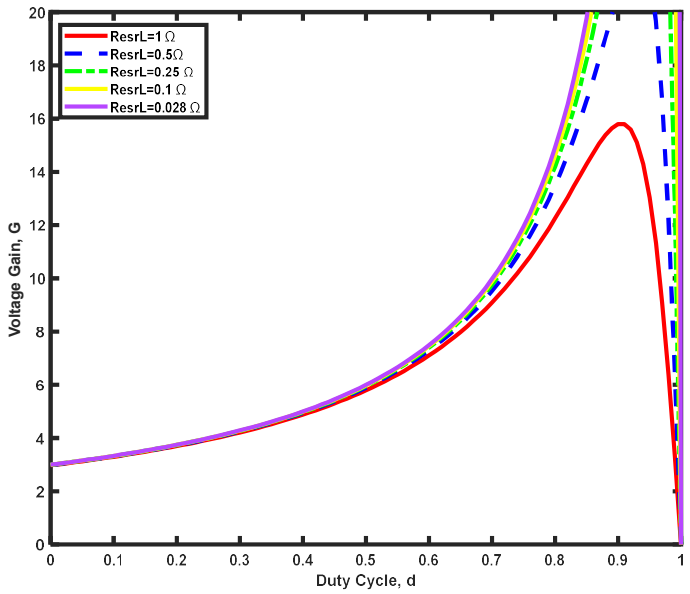

Figure 3.7: Voltage gain characteristic of the MBC as a function of duty cycle for different values of $R_{ESR,L}$.

3.3.2 Voltage Stress

Another key advantage of the MBC is the reduced voltage stress on the switch. According to the data shown in Figure 3.5 (a), the voltage on the switch V_S in the proposed converter can be expressed as:

$$V_S = V_{C1} \tag{3.8}$$

The voltage stress experienced by the switch in the three-level converter is observed to be lower than that for a single level converter with an equivalent output voltage and can be represented by substituting equation 3.4 into 3.8:

$$V_S = \frac{V_O}{3} = \frac{V_{in}}{1-d} \tag{3.9}$$

The data in Figure 3.8 illustrates the relationship between the normalised voltage stress across the MBC switch as a function of the duty cycle using equation 3.9. It is evident that an increase in duty cycle causes the voltage stress on the switch to increase. The voltage across the switch is one-third of the output voltage since each stage of the three-level MBC shares an equal portion of the total output voltage. Although a higher duty cycle can result in a larger output voltage, it can also increase switching losses in the switch and diodes. This can have an impact on the converter's efficiency. Utilizing higher-rated components, on the other hand, can improve performance and reduce losses, but it may also increase the cost. Therefore, the duty cycle and components rating are often chosen through a design trade-off to ensure that the converter meets the specific demands of its application.

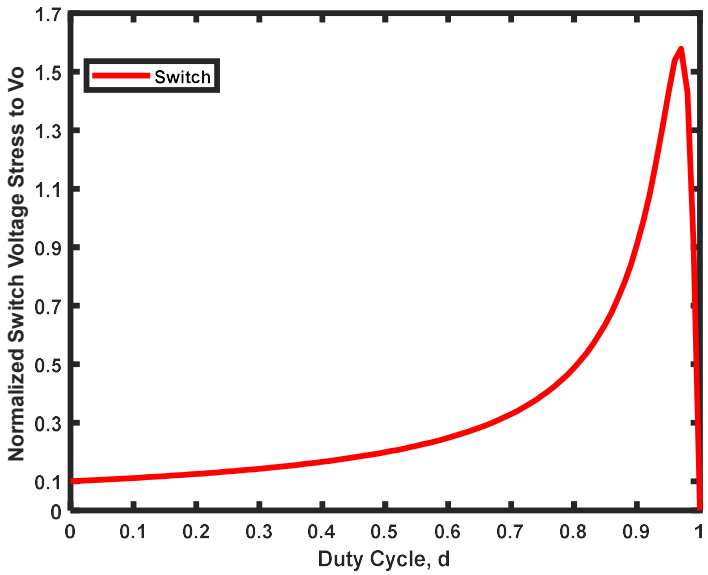

Figure 3.8: Normalized voltage stress of MBC versus d.

The voltage stress of all diodes in the MBC is the same and increases as the duty cycle increases. Nevertheless, it is always less than the output voltage and same the switch voltage, as shown in Figure 3.3 and conveyed in equation 3.9.

In the three-level MBC circuit, given that the capacitors are sufficiently large and have the same capacitance, all capacitors ideally maintain similar voltage. This means that the voltage stress experienced by each capacitor during operation is similar to voltage stress across the switch, as shown in Figure 3.3 and defined in equations 3.8 and 3.9, which depends on the duty cycle, the input voltage and output voltage of the converter.

3.4 DESIGN CONSIDERATION

When using MBC, it is important to consider that the number of diodes must increase to enhance the voltage gain by adding more levels. However, this can result in an increase in diode conduction loss, which could negatively impact the overall performance of the converter. On the other hand, a lower number of levels would require MOSFETs with higher voltage ratings and lead to an increase in MOSFET power loss. Thus, there needs to be a balance between MOSFET and diode power loss to determine the appropriate number of levels. Additionally, the converter's practical performance is affected by parasitic elements, which cause power losses and a reduction in output voltage compared to the ideal condition. The discussions given here are based on the three-level converter, as shown in Figure 3.2.

3.4.1 Inductor Design

For a three-level converter, the inductance of the inductors is calculated to maintain the appropriate current ripple so that $\Delta i_L = Y_L I_L$, where Y_L is generally in the range between 15 and 30%. For this, knowledge of the average current of the inductor is required. From equation 3.6, it can be observed that by adjusting the value of the duty cycle d applied to the switch, the inductor current can be regulated. As the duty cycle is raised, the switch remains turned ON for a more extended period, delivering

more energy to the inductor and resulting in a higher inductor current. To the contrary, when the duty cycle is reduced, the switch is ON for a shorter time, resulting in less energy supplied to the inductor and a lower inductor current [52]. As a result, the energy delivered to the inductor and hence the inductor current can be modified by controlling the duty cycle. Furthermore, a large current ripple in the inductor will result in large current stresses at the switch and diodes. Therefore, the inductor current ripple should be limited. The value of the inductance that allows the converters to operate in continuous conduction mode (CCM) is determined using the duty cycle and current ripple, where *f* is the switching frequency, as expressed below:

$$L = \frac{V_{in}\, d}{\Delta \mathrm{i}_L\, f} \tag{3.10}$$

3.4.2 Capacitor Design

The output voltage in this three-level MBC depends on the voltages of the three output capacitors, V_{C1}, V_{C3} and V_{C5}. Thus, with respect to equation 3.2, $V_o = 3V_C$. By selecting suitable capacitor values, it is possible to reduce the voltage ripple in the output of the three-level DC-DC MBC. Figure 3.4 and Figure 3.5 show the different operating modes for the three-level MBC.

The equations are derived utilising the following notations.

During the switch is turned ON:

- V_{1ac} and V_{3ac} define the voltage across capacitors C_1 and C_3 after the switch is closed, and these capacitors are discharging.
- V_{2ac} and V_{4ac} define the voltage across capacitors C_2 and C_4 after the switch is closed, and these capacitors are charging.
- Q_{1ac} and Q_{3ac} define the charge stored in capacitors C_1 and C_3 after the switch is closed.

- Q_{2ac} and Q_{4a} define the charge stored in capacitors C_2 and C_4 after the switch is closed.

During the switch is turned OFF:

- V_{1bc} and V_{3b} define the voltage across capacitors C_1 and C_3 before the switch is closed and, these capacitors are charging.
- V_{2b} and V_{4bc} define the voltage across capacitors C_2 and C_4 before the switch is closed and, these capacitors are discharging.
- Q_{1bc} and Q_{3bc} define the charge stored in capacitors C_1 and C_3 before the switch is closed.
- Q_{2b} and Q_{4b} define the charge stored in capacitors C_2 and C_4 before the switch is closed.

As shown in Figure 3.4 (c), when the switch is turned ON, capacitors C_1 and C_3 have a higher voltage than capacitors C_2 and C_4. During this period, diodes D_2 and D_4 allow capacitors C_2 and C_4 to charge from capacitors C_1 and C_3, respectively. At the same time interval, capacitors C_1 and C_2 are connected in parallel and the equivalent capacitor with a value of $C = C_1 + C_2$. The total charge stored in capacitors C_1 and C_2 just before the switch is turned on can be as follows:

$$Q_{(12)bc} = Q_{1bc} + Q_{2bc} = C_1V_{1bc} + C_2V_{2bc} \quad 3.11$$

The $Q_{(12)bc}$ represents the sum of the charge stored in capacitors C_1 and C_2 at the moment before the switch is closed. The total charge stored before and after the complimentary charging and discharging of the two capacitors must be equal in order to adhere with the principle of the energy conservation [108].

$$Q_{(12)ac} = Q_{(12)bc} \quad 3.12$$

$$V_{1a} = V_{2ac} = \frac{C_1V_{1bc} + C_2V_{2bc}}{C_1 + C_2}$$

The $Q_{(12)ac}$ represents the sum of the charge stored in capacitors C_1 and C_2 at the moment after the switch is closed. A similar analysis is performed to determine the relationship between the stored energy before and after charging for capacitors C_3 and C_4, for the same time period. An equivalent capacitor, $C^* = C_3 + C_4$, is used in this analysis, and the total stored charge in capacitors C_3 and C_4 just before closing the switching will be in a similar manner as follows:

$$Q_{(34)bc} = Q_{3bc} + Q_{4bc} = C_3V_{3bc} + C_4V_{4bc} \quad 3.13$$

The $Q_{(34)bc}$ is the total charge stored in both capacitors, just before turning ON the switch. In line with the concept of energy conservation, the amount of energy in the capacitors both before and after the switch is closed must be equal [108].

$$Q_{(34)ac} = Q_{(34)bc} \quad 3.14$$

$$V_{3ac} = V_{4ac} = \frac{C_3V_{3bc} + C_4V_{4bc}}{C_3 + C_4}$$

The expression given represents the total energy stored in capacitors C_3 and C_4 as $Q_{(34)ac}$ after the switch is turned ON. The balanced voltages of C_3 and C_4 after the complete discharging and charging time process for the first half cycle are represented by $V_{3ac}\ and\ V_{4ac}$ in the equation 3.14. Once the charging process is complete, the diodes D_2 and D_4 are opened, and the capacitors C_2 and C_4 no longer transfer their stored energy to the load. Their voltages stay steady during the switch- ON condition, while the load is powered by the series-connected capacitors C_1, C_3 and C_5, causing their voltages to drop. Assuming all capacitors in the circuit have the same capacitance and voltage drops, denoted as Δv_1, during the discharge time interval Δt_1 of the first half cycle, the voltage drops across C_1, C_3 and C_5 and the corresponding current flow, represented as $i_{C1} = i_{C3} = i_{C5} = I_O$, are the same. Thus, $i_c = C\frac{dv_c}{dt}$ and the expression for the voltage drops can be rewritten as follows.

$$\Delta \mathrm{v}_c = \frac{1}{C} i_C \Delta \mathrm{t} \tag{3.15}$$

$$\Delta \mathrm{v}_1 = \Delta \mathrm{v}_{c1} = \Delta \mathrm{v}_{c3} = \Delta \mathrm{v}_{c5} = \frac{1}{C1} i_{C1} \Delta t_1 = \frac{1}{C3} i_{C3} \Delta t_1 = \frac{1}{C5} i_{C5} \Delta t_1$$

$$\Delta \mathrm{v}_1 = \frac{1}{C1} I_O \Delta t_1 = \frac{1}{C3} I_O \Delta t_1 = \frac{1}{C5} I_O \Delta t_1$$

The second stage of the conduction mode, when the switch is opened, is being observed in Figure 3.5 (c). The inductor current I_L activates the diode D_5 when the switch is switched OFF. The off state of the switch is divided into two-time intervals, namely, Δt_2 and Δt_3. At the beginning of the time interval Δt_2, the voltage of the capacitor C_4 exceeds that of capacitor C_5, so diode D_3 will turn OFF. Additionally, the total voltage of the capacitors C_2 and C_4 is greater than that of the capacitors C_3 and C_5, causing diode D_1 to turn OFF. The capacitors C_2 and C_4 are discharged by current I_L while capacitors C_1, C_3 and C_5 are charged by the current $I_L - I_O$ during the charging and discharging of time interval Δt_2. The time interval Δt_3 starts when diodes D_1 and D_3 are turned ON. The two diodes are forward-biased when the voltages of the complementary capacitors C_3 and C_2 and capacitors C_5 and C_4 are equal. The voltage drops of capacitors C_1, C_3 and C_5 increase by values of $\Delta \mathrm{v}_2$, $\Delta \mathrm{v}_3$, and $\Delta \mathrm{v}_4$ in the time interval Δt_2 if the charging currents are $i_{C1} = i_{C3} = i_{C5} = I_L - I_O$.

$$\Delta \mathrm{v}_2 = \Delta \mathrm{v}_3 = \Delta \mathrm{v}_4 = \frac{1}{C1} i_{C1} \Delta t_2 = \frac{1}{C3} i_{C3} \Delta t_2 = \frac{1}{C5} i_{C5} \Delta t_2 \tag{3.16}$$

$$\Delta \mathrm{v}_2 = \Delta \mathrm{v}_3 = \Delta \mathrm{v}_4 = \frac{1}{C1} (I_L - I_O) \Delta t_2 = \frac{1}{C3} (I_L - I_O) \Delta t_2$$

$$= \frac{1}{C5} (I_L - I_O) \Delta t_2$$

It can express the voltage drops across capacitors C_2 and C_4 during the time interval Δt_2, while they are discharging with currents $i_{C2} = i_{C4} = I_L$, respectively, as $\Delta \mathrm{v}_5$ and $\Delta \mathrm{v}_6$.

$$\Delta v_5 = \Delta v_6 = \frac{1}{C2} i_{C2} \Delta t_2 = \frac{1}{C4} i_{C4} \Delta t_2 \tag{3.17}$$

$$\Delta v_5 = \Delta v_6 = \frac{1}{C2} I_L \Delta t_2 = \frac{1}{C4} I_L \Delta t_2$$

During the final time interval of the OFF condition, denoted as Δt_3, the capacitors C_3 and C_2, and the capacitors C_5 with C_4 are connected in parallel and supply power to the load in series with capacitor C_1. The discharging current for this configuration is $\frac{I_O}{2}$. However, capacitor C_1 continues to charge with a current of $I_L - I_O$ until the end of the cycle. The following is an expression for the voltage drops, $\Delta v_7, \Delta v_8, \Delta v_9 \; and \; \Delta v_{10}$ across the capacitors $(C_3, C_2) \; and \; (C_5, C_4)$ throughout the time period Δt_3 for $i_{C3} = i_{C2} = i_{C5} = i_{C4} = \frac{I_O}{2}$:

$$\Delta v_7 = \Delta v_8 = \Delta v_9 = \Delta v_{10} = \frac{1}{C3} i_{C3} \Delta t_3 = \frac{1}{C2} i_{C2} \Delta t_3 = \frac{1}{C5} i_{C5} \Delta t_3 \tag{3.18}$$

$$= \frac{1}{C4} i_{C4} \Delta t_3$$

$$\Delta v_7 = \Delta v_8 = \Delta v_9 = \Delta v_{10} = \frac{1}{C3}\left(\frac{I_O}{2}\right)\Delta t_3 = \frac{1}{C2}\left(\frac{I_O}{2}\right)\Delta t_3 = \frac{1}{C5}\left(\frac{I_O}{2}\right)\Delta t_3$$

$$= \frac{1}{C4}\left(\frac{I_O}{2}\right)\Delta t_3$$

The voltage drops across the charging capacitors C_1 during the time interval Δt_3, for a charging current of $i_{C1} = I_L - I_O$, is represented by the value of Δv_{11}.

$$\Delta v_{11} = \frac{1}{C1} i_{C1} \Delta t_3 \tag{3.19}$$

$$\Delta v_{11} = \frac{1}{C1} (I_L - I_O) \Delta t_3$$

The voltage ripple at the output of the three-level DC-DC MBC is the combined voltage ripples of capacitors C_1, C_3 and C_5, given by $V_{C1} + V_{C3} + V_{C5}$. The voltage ripple of each capacitor, including C_2 and C_4, output voltage and drain source voltage are depicted in Figure 3.9 [108].

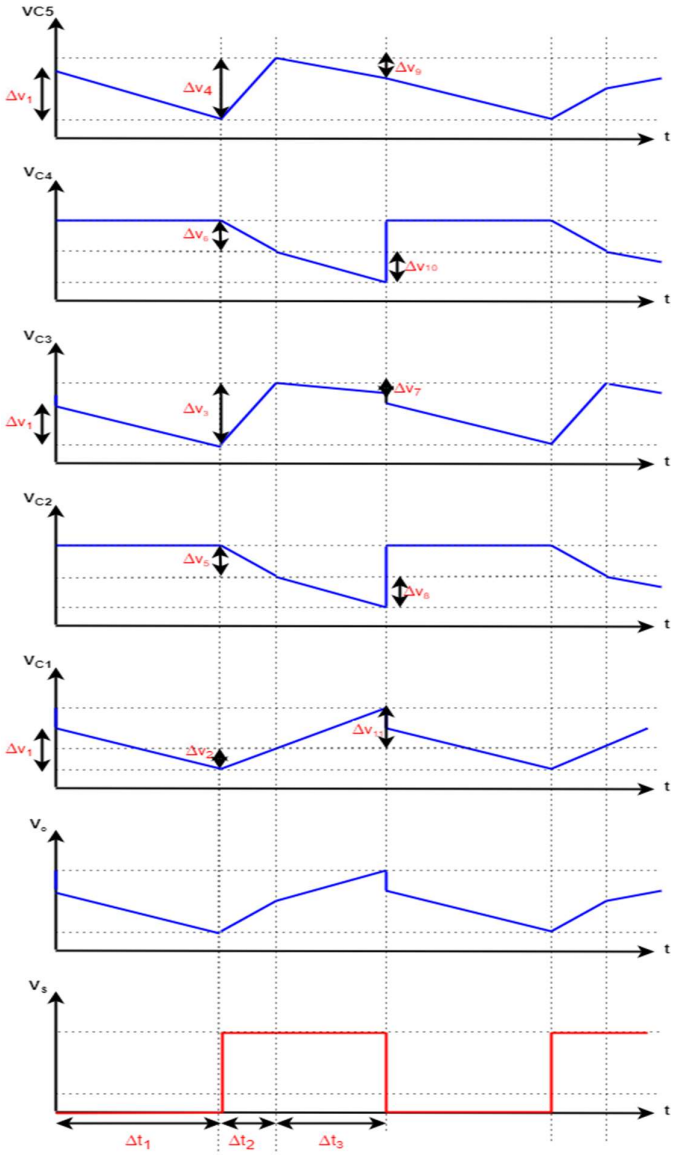

Figure 3.9: Voltage ripple waveforms for all five capacitors in MBC with output voltage and switch voltage.

One of the key advantages of the proposed topology is to maintain the same output voltage on each of the output capacitors C_1, C_3 and C_5. The output voltage across the load may be determined under the assumption that all capacitors have the same capacitances, resulting in $V_o = 3V_C$. The design criterion for the output capacitors is that the voltage ripple should not exceed 5% and so, the capacitance can be determined from ΔV_o, the voltage ripple of capacitor [82].

$$C = \frac{d}{R_o\left(\frac{\Delta V_o}{V_o}\right)f}\frac{N(N+1)}{2} \quad 3.20$$

Besides the current and voltage ratings, it is critical to use the smallest possible components, mainly inductors and capacitors, linked to the size of their respective capacitance and inductance values, to increase the power density of the circuit. To minimize these values, one factor that can be adjusted is the switching frequency of the converter's switch. Equations 3.10 and 3.20 illustrate that raising the switching frequency will result in decreased inductance and capacitance values needed for the circuit [110].

3.4.3 Selection of Power Devices

Selecting the appropriate power devices for a DC-DC MBC involves the consideration of voltage and current ratings and switching frequency. The power devices selected must be able to handle the voltage and current levels that will be present in the converter to avoid breakdown. In addition, the switching frequency of the converter plays a vital role in affecting the performance of the power devices selected. Generally, higher switching frequencies require devices with faster switching speeds to minimize power losses; however, faster devices may also be more expensive [110]. This concern can be mitigated by using wide-bandgap semiconductor devices, such as Silicon-Carbide (SiC) MOSFETs. Compared to silicon (Si) based MOSFETs, these devices offer shorter switching transients for charging and discharging the gate capacitor, which results in less power loss and enables higher switching frequencies, which can further improve efficiency and reduce the size of the converter.

Wide-bandgap materials also offer lower drain source ON-state resistance and better heat conduction properties, which slows the device's temperature rise [111]. In Figure 3.10, the specific on-resistance for the drift region in 4H-SiC devices is

compared with silicon as function of breakdown voltage between 100 V and 100 kV [112]. The data show that there are three orders of magnitude decrease in specific on-resistance between Si and 4H-SiC devices for the same breakdown voltage.

When selecting a diode, it is vital to consider the ability to withstand substantial OFF-state voltage stress, as well as the capacity to handle peak and average current. Fast switching capabilities, low reverse-recovery time, and a low forward voltage drop are also significant factors to consider [110].

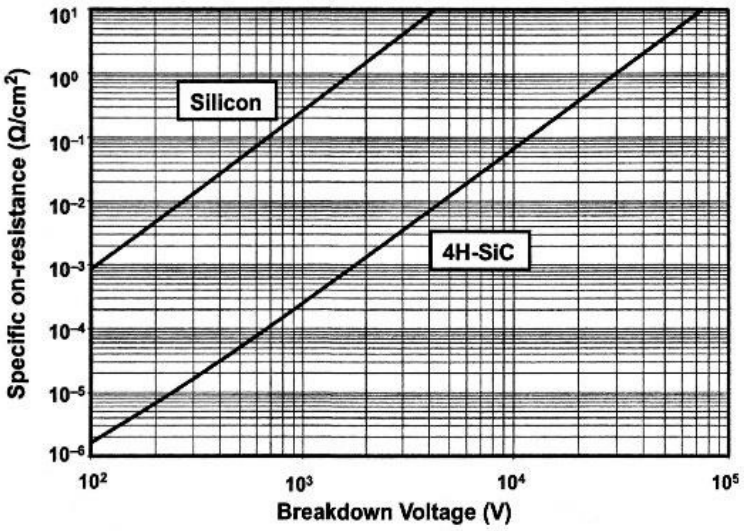

Figure 3.10: Specific on-resistance for 4H-SiC and Silicon in power devices [15].

3.5 SIMULATION AND EXPERIMENTAL VERIFICATION

The most significant characteristics to verify the operating characteristics and high voltage gain of the three-level MBC that has been designed to enable the connection of wave energy converters to an MVDC collection network are described. The performance of the proposed converter is validated through simulation and prototype results.

3.5.1 High Gain MBC Prototype

A hardware prototype of the three-level proposed converter was built to validate the theoretical analysis and simulation results. A commercial SiC MOSFET (GeneSiC Semiconductor part number G2R120MT33J) was chosen as the power switch, which has an on-state resistance $\left(R_{DS(ON)}\right)$ of 0.12 Ω and a blocking voltage of 3.3 kV. All the diodes in the circuits are SiC Schottky Diodes (GeneSiC Semiconductor part number GB05MPS33-263) and a blocking voltage of 3.3 kV with a forward voltage drop of 3 V. The inductor is toroidal power inductor (HF467-102M-26AH). The main circuit of the proposed three-level MBC and the experimental prototype are shown in Figure 3.11.

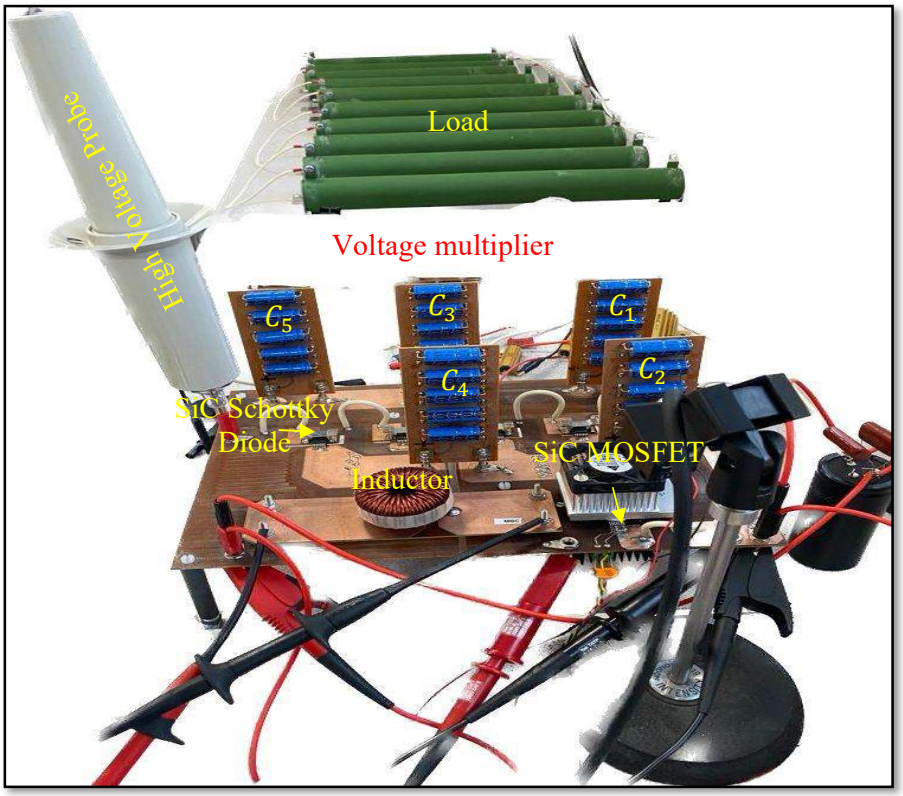

Figure 3.11: Three-level MBC experimental prototype.

3.5.2 Simulation and Measured Experimental Waveforms

The initial design has been simulated using LTSpice to validate the values for the passive components calculated using the analysis specified in sections 3.3 and 3.4 and to examine the switching transients in the circuit. The operating parameters of the converter and component ratings are listed in Table 3-1. The same parameters are used in both the simulation and experimental prototype to enable a comparison.

Table 3-1. Design Specification for Three-Level MBC.

Parameter	Symbol	Rating
Input Voltage	V_{in}	500 V
Output Voltage	V_o	5 kV
Output Load	R_o	10 kΩ
Switching Frequency	f	50 kHz
Inductor	L	1 mH, 26 A, ESR 28 mΩ
Capacitors	$C_1 - C_5$	1μF, 4.5 kV
Switch	S	G2R120MT33J
Diodes	$D_1 - D_5$	GB05MPS33-263

Simulated characteristics of a three-level boost converter have been used to boost a DC input voltage of 500 V to an output of 5 kV. To ensure an adequate portion of the operating period with the switch turned off, in order to avoid excessive voltage stress whilst achieving a gain factor of 10, the duty cycle was not allowed to exceed 75%. Following the analysis in the previous sections, a three-level MBC was investigated and a duty cycle of 71% found to give an output voltage of 5 kV with an output power of 2.5 kW. The efficiency of the proposed converter was evaluated as a function of the switching frequency between 25 and 200 kHz in order to determine the

maximum operating point and optimum efficiency for this converter topology. The efficiency is directly calculated by measuring the input and output powers. The data showed a maximum simulated efficiency of 94.5% when the converter was operated at 75 kHz with a duty cycle of 71%, as shown by the blue data set in Figure 3.12. However, compared to the simulation data, the performance of the experimental converter shows two distinct variations, as depicted by the red data set in Figure 3.12. Firstly, the efficiency of the converter is decreased by an average of 3.0% over the entire frequency range, from 93.7% to 90.7%. Secondly, instead of the peak efficiency being observed at 75 kHz, a smaller variation in frequency is observed, with the variation ranging between 91.7% and 92.4% over the frequency range between 50 and 150 kHz. This indicates that the switching frequencies in this range can be operated as though they are the maximum operating points. Additionally, it can be observed from the data that the efficiency decreases as the frequency exceeds 150 kHz.

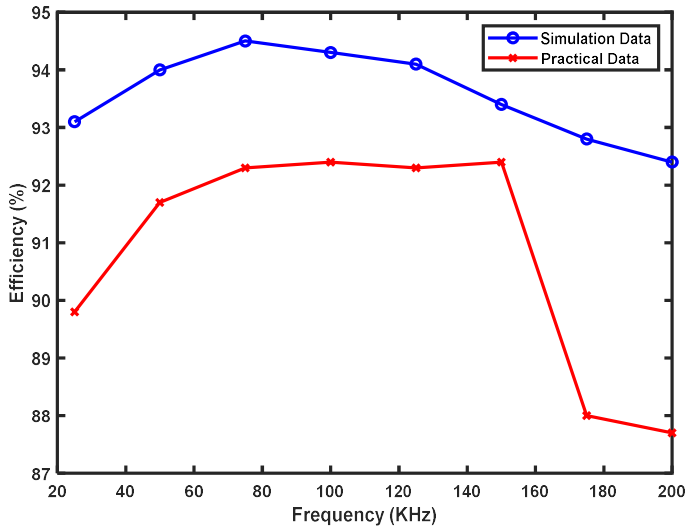

Figure 3.12: Simulation and practical efficiency with respect to the switching frequency of the three-level MBC.

To generate the required output voltage of 5 kV with gain of 10 using single switch, the duty cycle should be $d = 0.71$ according to equation 3.6. Due to the non-ideal conditions found in practical applications, $d = 0.73$ was required to achieve the desired gain. However, the duty cycle at the MOSFET is 0.72, observing that the gate drive introduces a delay, and this appears as a change in the duty cycle. The data in Figures 3.13, 3.14, 3.15, 3.16, 3.17 and 3.18 show the simulation and experimental waveforms for the converter operating at 50 kHz. In general, the experimental waveforms show a high level of agreement with the waveforms from the LTSPICE simulations.

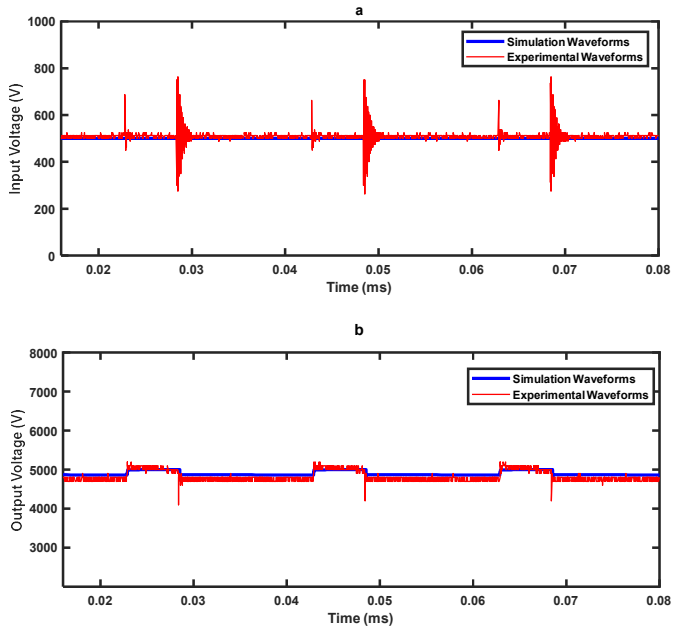

Figure 3.13: Input and output voltage waveforms of the three-level MBC.

The input voltage and output voltage waveforms are shown in Figure 3.13. The simulation and experimental results confirm the ability of the equations presented in section 3.3 and 3.4 to determine the voltage gain of the three level DC-DC MBC. The voltage gain values obtained from the practical and simulation three-level MBC are approximately 9.85 and 9.9, respectively. These values closely approximate to the

theoretical voltage gain defined in equation 3.7. Additionally, it can be observed from the data that the experimental waveforms show switching transients that are not evident in the simulation results. The input voltage transients, which occur at the turn on and turn off transients of the switch, originate in the parasitic capacitances and inductances in the circuit. The output voltage transients are related to the input transients being propagated through the circuit.

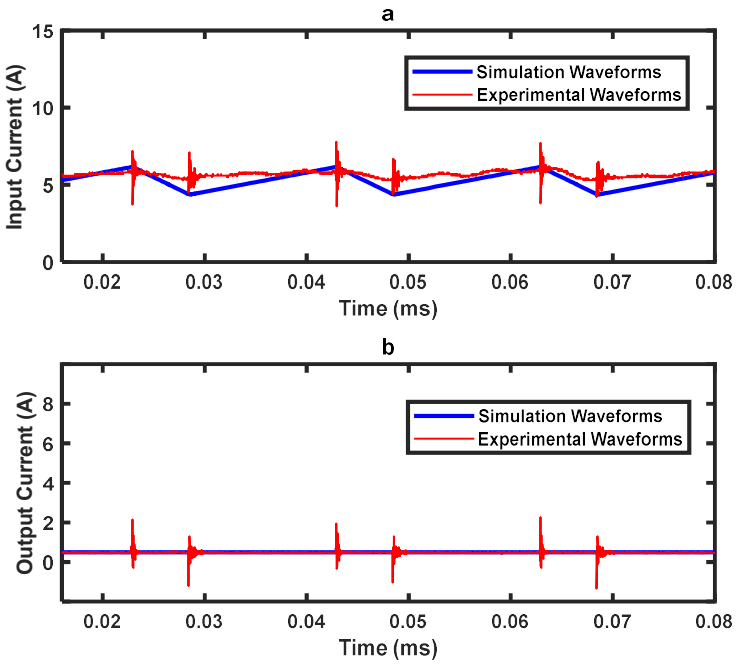

Figure 3.14: Input and output current waveforms of the three-level MBC.

The data in Figure 3.14 show the variation in the inductor current and output current. The observed output voltage from the converter is 5 kV, and the load current is 0.5 A. The data in the figure show that the inductor current I_L is continuous, confirming that the converter is operating in CCM. The current ripple in the inductor is equal to 10.71%. The measured average inductor current is 5.5 A, which is consistent with the theoretically estimated value of 5.36 A. It can be noticed from Figure 3.14 (a) that the simulation and experimental results slightly differ regarding the ripple current due to several causes. In practice, the manufacturing tolerances of components can

differ from ideal values, affecting the circuit's performance and resulting in different simulation ripple currents. Additionally, parasitic components like capacitance and inductance, which significantly impact circuit behaviour, may need to be adequately modelled in simulations. Furthermore, variations in stray inductance, capacitance, and resistance, which affect ripple current, might result from variances in circuit layout between practical and simulations.

The inductor voltage waveform is shown by the data in Figure 3.15. The measured value when the switch is ON is 500 V, which is equal to the input voltage of the converter and when the switch is OFF equals to -1275V, which is in agreement with the simulation and theoretical predictions using equation 3.3. The simulated and calculated values of $V_{L_{SON}}$ equals to 500 V, $V_{L_{SOFF}}$ equals to -1269 V and $V_{L_{SON}}$ equals to 500 V, $V_{L_{SOFF}}$ equals to -1255 V, respectively. This emphasizes the features of low voltage stress on the devices for this converter.

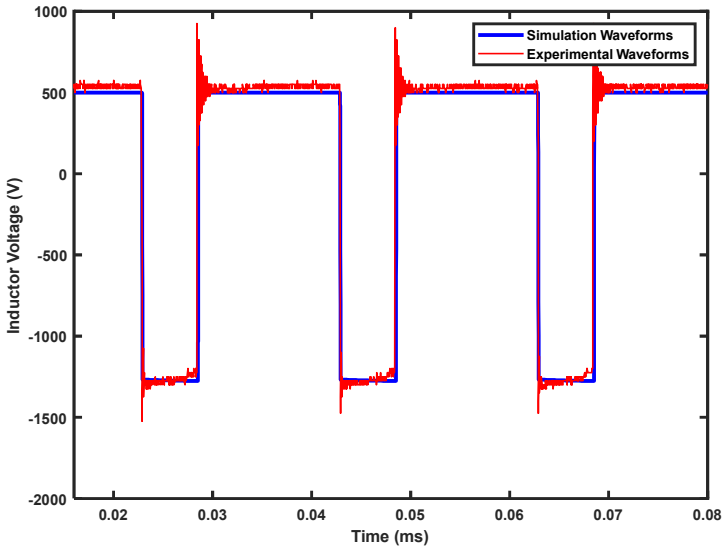

Figure 3.15: Voltage waveform across the inductor of the three-level MBC.

The data in Figure 3.16 show the drain-source voltage across the switch with its corresponding drain-source current for the three-level MBC. A significant advantage of the proposed converter in comparison to the conventional boost converters and the step-up converter topologies presented in the literature is to reduce the voltage stress on the switch. The data in Figure 3.16 show that the maximum drain-source voltage across the switch is 1800 V when the output voltage is 5 kV, which is in accordance with simulated and analytical predictions. This opens up opportunities for significantly higher output voltages without the need for high voltage FETs since lower voltage FETs can be utilized in conjunction with the voltage multiplier to attain the desired output voltage. Considering the theoretical analysis in equation 3.9, it is reasonable to draw the conclusion that the experimental findings closely verify the findings of the simulation and are consistent with the analysis. Equation 3.9 gives a predicted maximum drain-source, voltage across the switch of 1724 V when the output voltage is 5 kV. Hence, the experimental and simulation switching voltage of V_s = 1800V and V_s = 1775 V, respectively are closed to the estimated value. Similarly, the simulation and experiment's measured drain-source current nearly match each other.

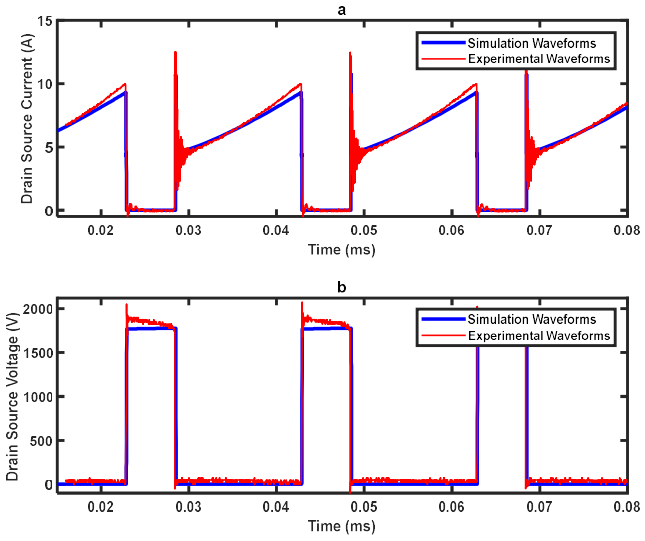

Figure 3.16: Drain-source voltage and current across the switch of the three-level MBC.

The data in Figure 3.17 show that the voltages across the three output capacitors, C_1, C_3 and C_5 are balanced with the minor difference observed being linked to the forward voltage drop across the diodes, losses in the parasitic components and the equivalent series resistance (ESR) of the capacitors used for C_1, C_3 and C_5. The simulation voltage difference between C_1 and C_3 is 11 V, and 4 V is between C_3 and C_5 with ideal capacitors. The measured voltage across capacitors C_1, C_3 and C_5 are 1800 V, 1637 V and 1563 V, respectively. Consequently, the voltage across the load is the algebraic sum of the voltages across the individual capacitors $V_{C1} + V_{C3} + V_{C5}$. Thus, each capacitor maintains approximately the same voltage levels and voltage balance is achieved across all capacitors as predicted by equation 3.4.

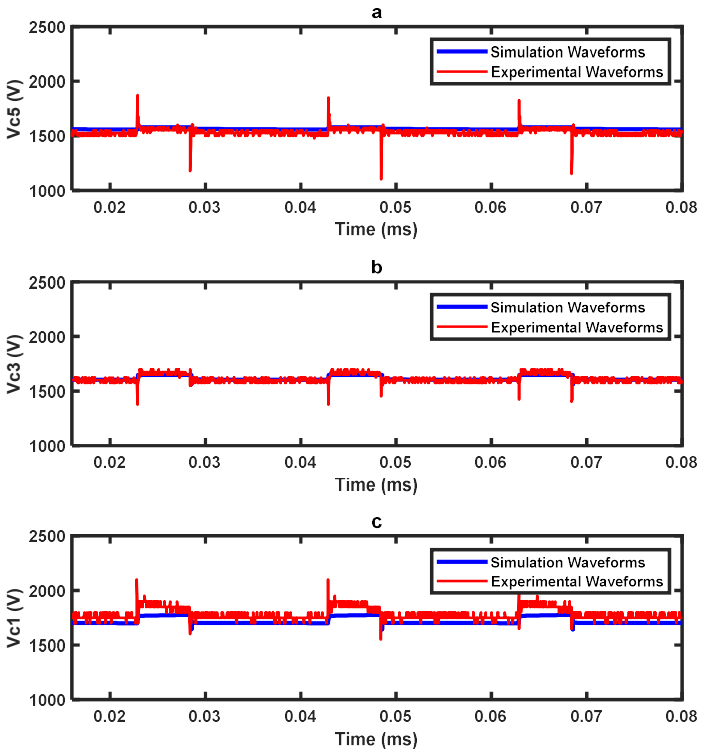

Figure 3.17: Voltage across the output capacitors C_1, C_3 and C_5 of the three-level MBC.

The data in Figure 3.18 show the drain-source voltage across the switch with voltage across all five diodes for the three-level MBC. It confirms the operating principle of MBC; when the switch is ON, $(0.028 \leq T < 0.043 \text{ ms})$, diodes D_2, D_4 are forward-biased and when the switch is OFF, $(0.043 \leq T \leq 0.048 \text{ ms})$, diodes D_1, D_3, D_5 are forward-biased.

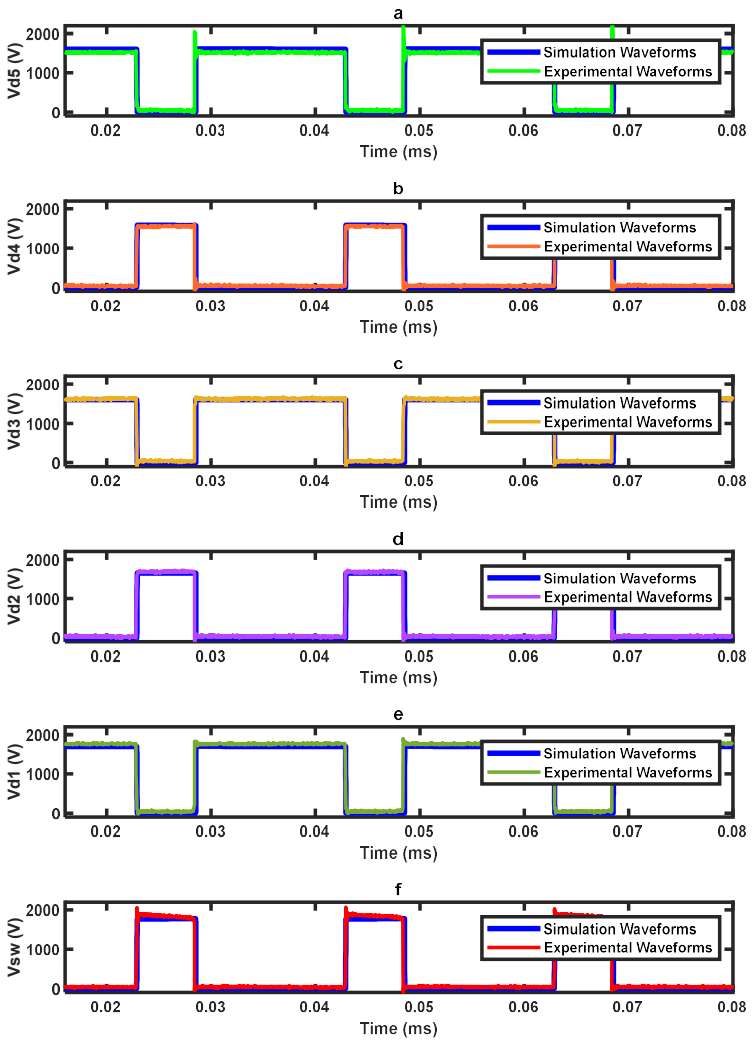

Figure 3.18: Drain-source voltage across the switch with voltage across D_1, D_2, D_3, D_4, D_5 of the three-level MBC.

3.6 POWER LOSS ANALYSIS AND EFFICIENCY MEASUREMENT

The internal characteristics of each component and device in the converter have an impact on the efficiency. The power loss caused by each component is discussed in this section.

3.6.1 Power Losses in Inductor

Core loss and copper loss are the two main sources of inductor loss. The average current of the inductor has a significant impact on the copper loss for the inductor. Thus, the power loss may be described as $P_L = I_L^2 R_{ESR,L}$, where $R_{ESR,L}$ is inductor equivalent series resistance. Therefore, the inductor copper loss P_L for three-level MBC can be expressed as

$$P_L = \left(\frac{3V_o}{(1-d)R_o}\right)^2 R_{ESR,L} \tag{3.21}$$

3.6.2 Power Losses in Capacitor

Based on the root mean square (RMS) current passing through the capacitor and its effective series resistance ($R_{ESR,C}$), the power loss in the capacitor is determined. The power loss in the capacitors for MBC can be calculated as

$$P_C = I_{C1}^2 R_{ESR,C1} + I_{C2}^2 R_{ESR,C2} + I_{C3}^2 R_{ESR,C3} + I_{C4}^2 R_{ESR,C4} + I_{C5}^2 R_{ESR,C5} \tag{3.22}$$

3.6.3 Power Losses in Switch

The practical power switch has conduction and switching losses. The switch conduction loss for the three-level MBC topology can be determined from the drain – source current and voltage characteristics, resulting in

$$P_{SC} = \left(\frac{3V_o}{(1-d)R_o}\right)^2 R_{DS,(ON)} \tag{3.23}$$

where $R_{DS,(ON)}$ represents the drain-source resistance.

The voltage across the switch, peak current, turn-on (t_{ON}) and turn-off (t_{OFF}) times, and switching frequency significantly affect switching power loss. Accordingly, the switches' switching loss can be expressed as:

$$P_{SW} = \frac{1}{2} I_{L,avg} V_s (t_{OFF} + t_{ON}) f_{sw} + \frac{1}{2} f_s C_{oss} V_S^2 \quad 3.24$$

where C_{oss} is output capacitance.

Total loss due to switch can be estimated as:

$$P_{S,total} = P_{SC} + P_{SW} \quad 3.25$$

3.6.4 Power Losses in Diodes

In general, there are two forms of diode loss: loss due to forward voltage drop (V_F) and conduction loss due to internal resistance (r_f). The loss due to forward voltage drop is based on the average current and the conduction loss is dependent on the RMS current of diodes. The average diode current $I_{D,avg}$ can be expressed as

$$P_{D,avg} = \frac{1}{T_S} \int_0^{(1-d)T_S} i_D(t) dt \quad 3.26$$

Taking into account that when the switch is OFF period $(1-d)T_S$, the diode is forward biased. The i_D represents the current passing through the diode.

Therefore, total loss in diodes for the three-level MBC will be as:

$$P_D = \sum_{i=1}^{5} I_{D,avg} V_F + \sum_{i=1}^{5} I_{D,rms}^2 r_f \quad 3.27$$

Hence, the total power loss in the converter is given as

$$P_{Losses} = P_L + P_C + P_{S,total} + P_D \quad 3.28$$

3.6.5 Estimating the Efficiency

The Efficiency (η) of the converter can be expressed as

$$\eta = \left(\frac{P_o}{P_o + P_{Losses}}\right) \qquad 3.29$$

The characteristics in Figure 3.19 show the simulation and experimentally measured efficiency of the there-level MBC topology with the respect to the output power ranging from 900 W to 2.5 kW. The data shows that the MBC has an adequate performance with maximum measured efficiency is 91.4% with an output power of 2.5 kW. At the same output power, the simulated efficiency is 94.7%. The core losses in the inductor are not included in the simulation efficiency, as well as contribution from parasitic capacitances and inductances in the circuit that cause the switching transients of input and output voltage, as shown in Figure 3.13. The losses can account for the difference between the simulation and experimental efficiency and hence can influence the experimental efficiency.

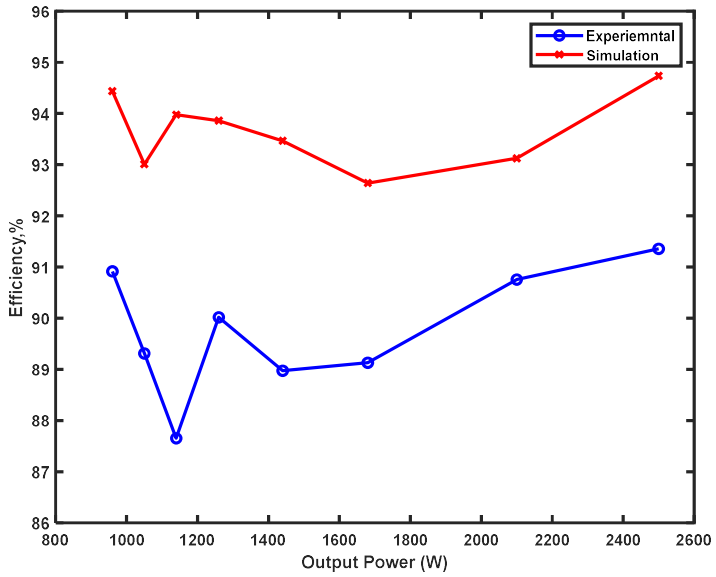

Figure 3.19: Simulation and practical efficiency with respect to the output power of the three-level MBC.

The power ratings of the selected components in the hardware prototype were used to conduct a loss analysis. The percentage distribution of losses in the proposed converters is shown in Figure 3.20. It is concluded that he major percent of losses occurs in the capacitors, due to the high ESR of the capacitors used, followed by the SiC MOSFET. The capacitors contribute to losses in a power converter due to their ESR that is present in series with its ideal capacitance. Note that the capacitors used in the demonstrator circuit are not optimally selected for efficiency consideration. The ESR generates power dissipation and heating when a capacitor is used in a power converter, which can result in losses. Therefore, the choice of capacitors with low ESR can contribute in reducing converter losses. Another major contribution of losses occurs in the MOSFET. Since the converter operates at high switching frequency with high voltage rating, the MOSFETs used in the converter can contribute significantly to the overall losses. Finally, carefully selecting components and optimising the converter design can help minimize losses and improve efficiency.

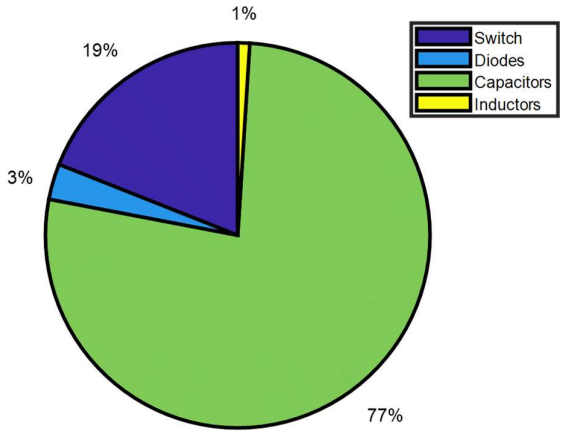

Figure 3.20: Percentage distribution of losses of the three-level MBC.

3.7 SUMMARY

This chapter comprehensively analyses a three-level DC-DC multilevel boost converter (MBC) for MVDC applications, including wave energy. The experimental results from the built prototype validate the converter's theory, operational characteristics, and simulation results. It is shown that the converter achieved the desired voltage gain ten times without the need for complex multi-switch control algorithms to enable the grid connection of renewable energy sources. Moreover, the voltage conversion ratio can be further increased not only by adjusting the duty cycle but also by increasing the level number N of the converter. The significant advantages of the proposed converter over other converter topologies, such as the conventional boost converter, cascaded converters, and quadratic boost converter, are that they offer low voltage stress across the devices, continuous input current, voltage balance across all output capacitors, and a high voltage gain without the need for an excessive duty cycle. In addition, the experimental data still show high efficiency, varying between 91.7% and 92.4% for the frequency range between 50 and 150 kHz. This implies that the suggested three-level MBC can operate effectively at various switching frequencies within this range without significantly impacting the overall efficiency. This is a valuable finding since it enables flexibility in the converter and optimization following specific demands, such as size, cost, and application. Unlike many power converters in the literature, the proposed topology offers low voltage stress on the switch, allowing higher output voltages without the need for high-voltage FETs. This could improve the system's overall efficiency, increasing energy production and reducing costs.

Notably, simulations of the circuits show a good level of match with the experimental data in terms of the trends in the operating conditions. The findings of

this study have considerable implications for developing efficient and high voltage DC-DC converters, particularly for wave energy applications, where high voltage and high power are desired. Additionally, the proposed converter's utilisation of high frequency SiC semiconductor devices is well suited for applications in which weight and power density are also crucial design criteria. The data presented in this chapter confirm the theoretical analysis developed for the circuit with parasitic components and identify that the transformerless DC-DC multilevel boost converters are suitable for wave energy integration.

Chapter 4: Analysis, Design, and Evaluation of High Gain Switched Inductor and Voltage Lift Switched Inductor Multilevel Boost Converters

4.1 INTRODUCTION

The transformerless DC-DC multilevel boost converter (MBC) topology presented in Chapter 3 has proven to be a successful solution for achieving high voltage gains. Nevertheless, a persistent demand for higher conversion ratio and improved efficiency exists. Accordingly, further efforts have been made to develop and test transformerless high gain topologies capable of attaining even higher conversion ratios with lower duty cycle. Hence, the switched inductor multilevel boost converter (SIMBC) and the voltage lift switched inductor multilevel boost converter (VLSIMBC) topologies have been designed, investigated, and tested. The merits of both converters are;

- transformer-less topology using a single, low side switch,
- low voltage stress across semiconductor devices,
- continuous input current,
- modularity,
- the creation of three self-balanced voltage levels at the output.

This chapter introduces a transformerless DC-DC switched inductor multilevel boost converter (SIMBC) and voltage lift switched inductor multilevel boost converter (VLSIMBC) intending to realize a voltage gain of ten with reduced voltage stress on devices. These converters combine the traditional boost converter with a self-balancing multi-stage voltage multiplier in the output stage to create a high voltage gain system, where each stage shares an equal portion of the total voltage output [11, 113-118]. Adding more capacitors and diodes to the fundamental boost converter

topology increases the number of levels in the circuit and, consequently, the output voltage. This enables the circuit to be utilized as a power converter in applications that require multiple controlled voltage levels with self-balancing when operating with unidirectional current flow [107]. The SIMBC regulates voltage through pulse width modulation (PWM) using a single switch, two inductors, (2N+2) diodes, and (2N-1) capacitors to produce a number of level (N) times the output of a conventional boost converter under identical conditions. On the other hand, the VLSIMB utilizes a single switch, two inductors, (2N+1) diodes, and (2N) capacitors to control voltage through PWM, resulting in an output N times larger than a traditional boost converter operating under similar conditions.

The converter operational analysis, performance analysis and design considerations are discussed in detail. Simulation, as well as laboratory prototypes are experimentally developed to validate the theoretical analysis and the feasibility of the proposed topologies in a high step-up application. Furthermore, the performance of both topologies is evaluated and compared to MBC under the same operating conditions. The results demonstrated that the SIMBC and VLSIMBC perform better, achieving higher voltage gain with lower duty cycle and higher efficiency.

4.2 CONVERTERS' OPERATIONAL ANALYSIS

4.2.1 Circuits Architecture Description

The circuit topologies for the proposed switched inductor multilevel boost converter (SIMBC) and voltage lift switched inductor multilevel boost converter (VLSIMBC) are shown in Figure 4.1 and Figure 4.2, with three-stage converters, (N = 3). The input portion is a boost stage that utilizes a switched inductor, and a voltage lift switched inductor. The subsequent stage is a voltage multiplier (VM) stage to increase the voltage gain and minimize the voltage stress on the semiconductor

devices. The voltage multiplier stage of each circuit for both converters is identical; however, the configuration of the input stage for each topology is different in the arrangement of the inductor. Both circuits comprise a PWM-controlled power MOSFET which has a blocking voltage to match the voltage across output capacitor C_1 rather than the entire output voltage as necessary in a conventional boost converter topology.

The schematic of the three-level SIMBC converter is shown in Figure 4.1. In the SIMBC, the inductor has been replaced by a switched inductor. The two inductors L_1 and L_2 are charged in parallel through D_{S1} and D_{S3} when the switch is turned ON and discharged in series through D_{S2} when the switch is turned OFF. The main advantage of the SIMBC is the voltage gain is increased by a factor of $(1 + D)$ compared the MBC, where D is the duty cycle.

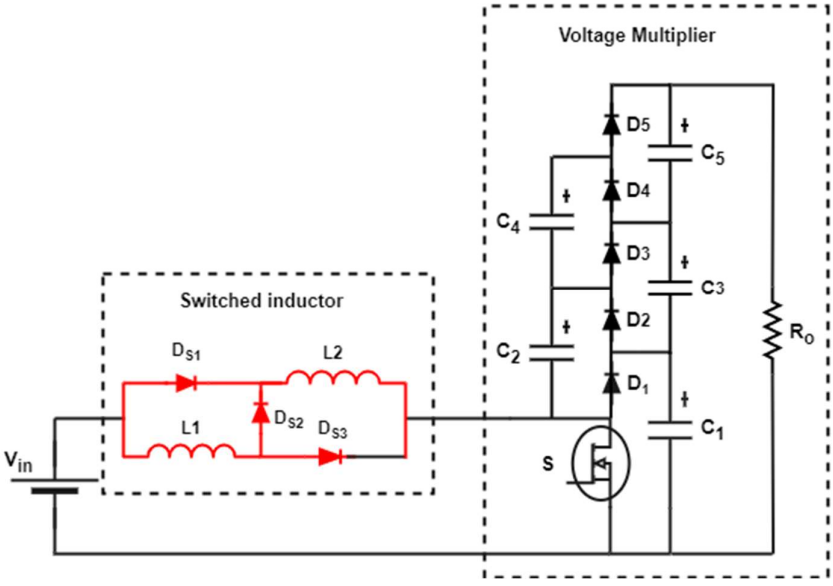

Figure 4.1: Circuit diagram of the three-level high gain DC-DC SIMBC.

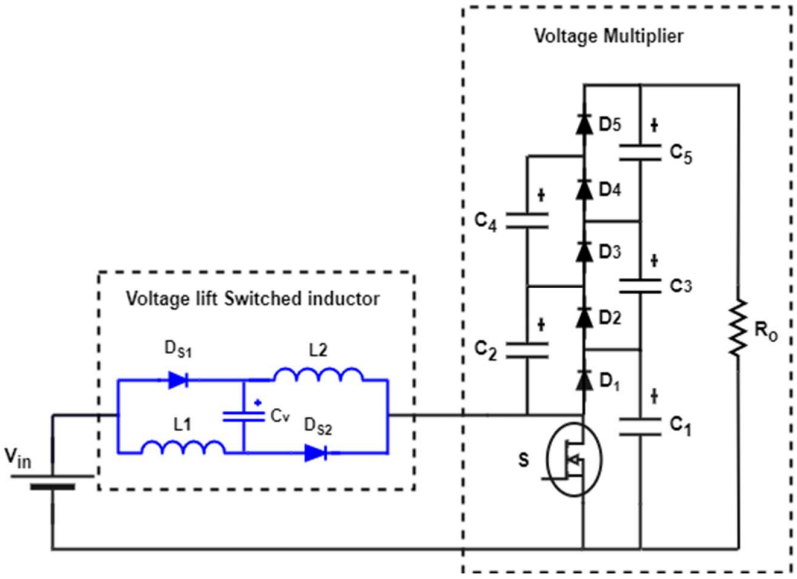

Figure 4.2: Circuit diagram of the three-level high gain DC-DC VLSIMBC.

Figure 4.2 shows a schematic of the three-level DC-DC VLSIMBC, where the input inductor has been replaced by two inductors, two diodes and a charge pump capacitor C_v. The two inductors L_1 and L_2 and the capacitor C_v are charged in parallel through D_{S1} and D_{S2} when the switch is turned ON and discharge in series when the switch is turned OFF. The main benefit of VLSIMBC is the voltage gain is increased by two times compared to the MBC and $\frac{2}{1+D}$ in comparison to the SIMBC.

4.2.2 Modes of Operation

The operating principle of the SIMBC can be explained on the basis of two operating modes, since it has been developed to operate in continuous conduction mode (CCM): Mode 1, when the switch is turned ON and Mode 2, when the switch is turned OFF, as described in Figure 4.3. All the components are initially considered ideal, simplifying the circuit analysis of the proposed converter. The steady-state waveforms of the SIMBC are shown in Figure 4.3.

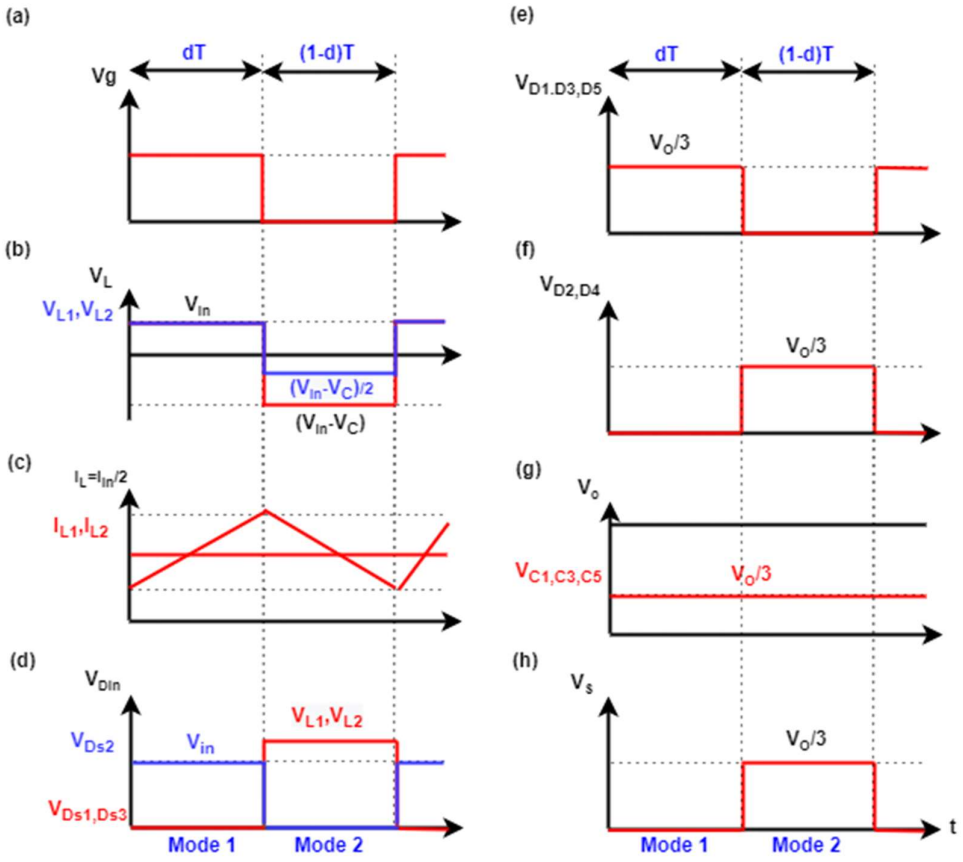

Figure 4.3: Main steady state waveforms of gate voltage, inductor voltage and current, input and output diodes voltages, output capacitors voltages and switch voltage for SIMBC.

The characteristics of the SIMBC that occur during the two modes of operation are explained as follows:

During Mode 1, when the switch is turned ON, the current flows as shown in Figure 4.4 (a). The inductors L_1 and L_2 are connected to the input voltage V_{in} and charged in parallel through diodes D_{s1}, D_{s3} and switch S. The load supplying capacitors C_1, C_3 and C_5 have higher voltages in this operation mode than the clamped capacitors C_2 and C_4. As a result, the diodes D_1, D_3 and D_5 are turned OFF, while D_2 and D_4 remain forward biased for transferring energy from capacitors C_1 and C_3 to

capacitors C_2 and C_4. The charging process continues until the voltage across all capacitors becomes equal [107, 113].

In Mode 2, when the switch is turned OFF, the current flow is illustrated in Figure 4.4 (b). The inductors L_1 and L_2 are connected to the input voltage V_{in} and discharged in series through diode D_{s2}. Diodes D_{s1} and D_{s3} are reversed bias, and diodes D_{s2} and D_1 conduct. Capacitor C_1 is charged by the two inductors until the voltage on the capacitor C_1 equals the total of the input voltage and the voltage on the two inductors. Then, the diode D_3 switches on, allowing the input voltage, two inductors and capacitor C_2 to charge the capacitors C_1+C_3. When the voltage on C_1+C_3 equals the sum of the input voltage, the voltage across the two inductors, and the voltage across the capacitor C_2, diode D_3 switches OFF and diode D_5 conducts. Consequently, as illustrated in Figure 4.4 (b), capacitors C_5, C_3 and C_1 are charged until their voltage equals the total of the input voltage, inductors' voltage and voltage across capacitors $C_2 + C_4$ [107, 113].

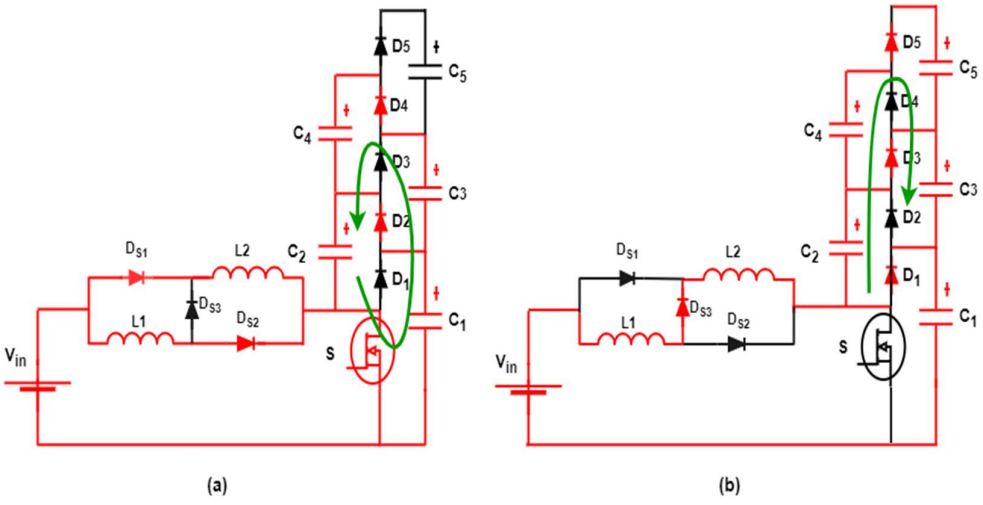

Figure 4.4: Operation modes of the three-level SIMBC (a) Mode 1, (b) Mode 2.

The operating principle of the VLSIMBC is approximately similar to SIMBC, except that charge pump capacitor C_v in the input circuit of VLSIMBC has a significant impact in the voltage gain. The steady-state waveforms of the VLSIMBC are shown in Figure 4.5.

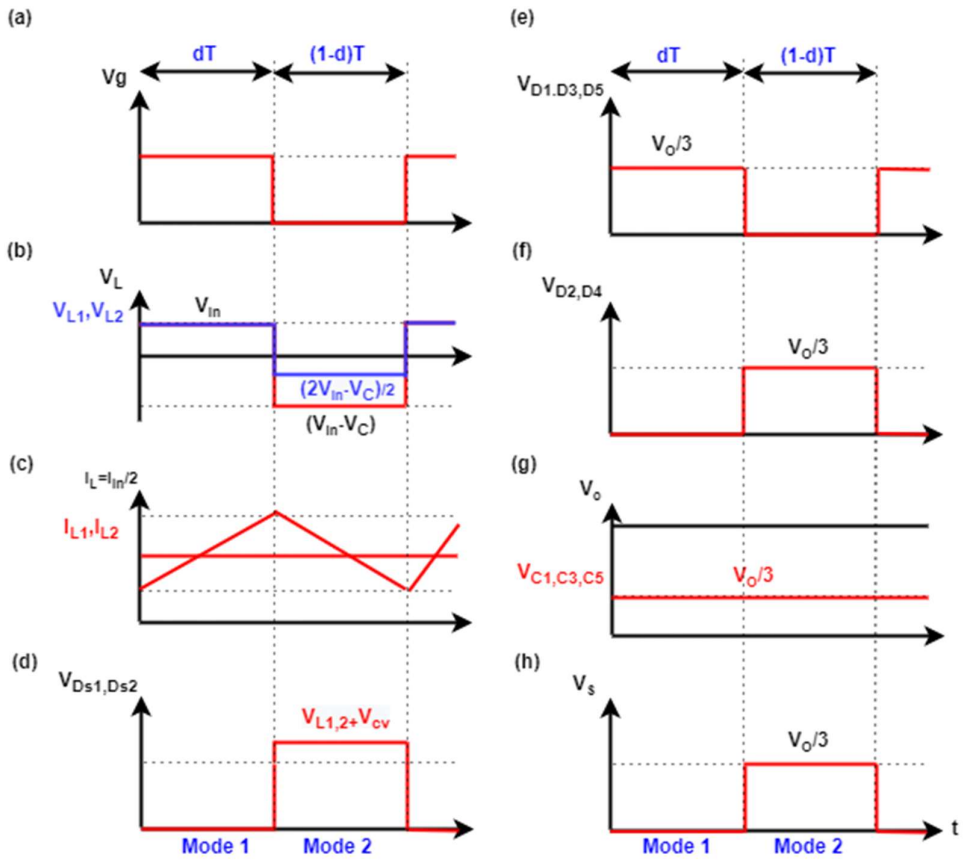

Figure 4.5: Main steady-state waveforms of gate voltage, inductor voltage and current, input and output diodes voltages, output capacitors voltages and switch voltage for VLSIMBC.

The behaviour of VLSIMBC in its two modes is discussed below as:

In Mode 1, the circuit operates with the switch turned ON, as shown in Figure 4.6 (a), and the current flows through inductors L_1 and L_2 and capacitor C_v, which are charged in parallel through diodes D_{s1} and D_{s2}. The output voltages at the load feeding capacitors C_1, C_3 and C_5 are higher than those of the clamping capacitors C_2 and C_4.

Therefore, diodes D_1, D_3 and D_5 are reversed bias, while diodes D_2 and D_4 remain forward biased, transferring energy from capacitors C_1 and C_3 to capacitors C_2 and C_4. This charging process is carried out until the voltage across all capacitors is equal [107, 114].

In Mode 2, the circuit operates with the switch turned OFF, as shown Figure 4.6 (b), and the current flows through inductors L_1 and L_2 and capacitor C_v, which are discharged in series. The two inductors and capacitor C_v charge capacitor C_1 until its voltage equals the total of the input voltage and the voltage on the two inductors and capacitor C_v. Diode D_3 then turns on, allowing the input voltage, two inductors, capacitor C_v and capacitor C_2 to charge capacitors C_1+C_3. When the voltage on C_1+C_3 equals the total of the input voltage, the voltage of the two inductors, voltage across capacitor C_v and the voltage across capacitor C_2, diode D_3 turns OFF and diode D_5 begins to conduct. The sum of the input voltage, inductors' voltage, capacitor C_v voltage and voltage across capacitors C_2 and C_4 charge capacitors C_5, C_3 and C_1 until their voltage equals the sum of the input voltage, inductors' voltage, capacitor C_v voltage and voltage across capacitors $C_2 + C_4$ [107, 114].

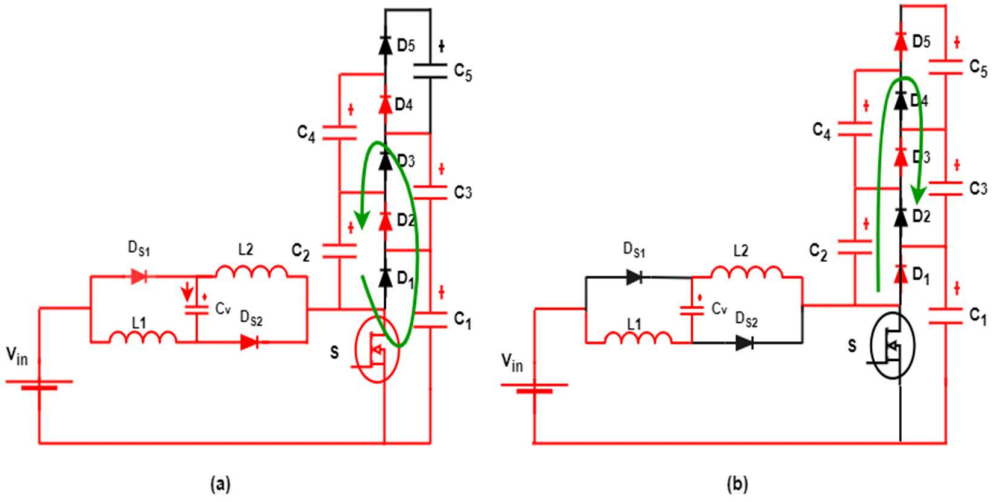

Figure 4.6: Operation modes of the three-level VLSIMBC (a) Mode 1, (b) Mode 2.

4.3 STEADY STATE PERFORMANCE ANALYSIS

4.3.1 Voltage Conversion Ratio

The initial development of voltage gain expressions of both SIMBC and VLSIMBC are evaluated under ideal conditions where the analysis does not take into account any parasitic components that may be present in the power devices and passive components.

In the SIMBC circuit, by charging and discharging the switched-inductor and switched-capacitor voltage doubler, the input power is transferred to the output. In Mode 1, as shown in Figure 4.3; the time interval is dT. During this operation mode, diodes D_{s1}, D_{s3}, D_2 and D_4 are forward-biased. Since the inductors L_1 and L_2 are connected in parallel, they exhibit a voltage drop equal to V_{in} under the assumption that the forward voltage drop of the diode can be neglected, and so

$$V_{in} = V_{L1} = V_{L2} \tag{4.1}$$

In Mode 2, as can be seen from Figure 4.3, the time interval is $(1-d)T$. During this mode, diodes D_{s2}, D_1, D_3 and D_5 are forward-biased. In this mode of operation, the input inductors L_1 and L_2 are connected in series so that

$$V_{in} = V_{L1} + V_{L2} + V_{C1} \tag{4.2}$$

Since L_1 and L_2 are identical, they will experience an equal share of the current flow. The average inductor voltage, which has to be zero over a complete switching cycle, can be expressed as

$$V_L = d\,(V_{in}) + (1-d)\left(\frac{V_{in} - V_{C1}}{2}\right) = 0 \tag{4.3}$$

In the steady state, the voltage across the output capacitors in a 3-stage converter can be expressed as:

$$V_C = V_{C1} = V_{C3} = V_{C5} = \frac{1+d}{1-d} V_{in} \tag{4.4}$$

and the output voltage of the converter is the sum of the voltages across the capacitors, so that

$$V_o = 3V_C = 3\frac{1+d}{1-d} V_{in} \tag{4.5}$$

The data in Figure 4.7 depict the three-dimensional view of the ideal voltage gain *G* of SIMBC as a function of duty cycle *d* for the varying number of levels, *N*. It can be observed that voltage gain increases with the number of levels and duty cycle. The voltage gain rises as the duty cycle rises, and this relationship frequently influences the realisation of a specific voltage gain.

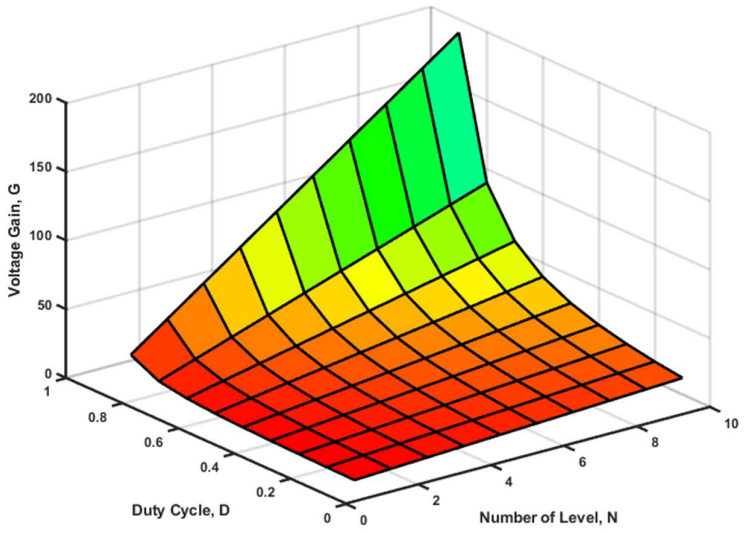

Figure 4.7: Ideal Voltage gain characteristic of the SIMBC as a function of *d* and *N* values.

The output current and the input and output voltages can be utilized to determine the average inductor current I_L, assuming that the converter operates at 100% efficiency, this leads to

$$I_L = \frac{{V_o}^2}{V_{in}R_o} \tag{4.6}$$

The inductor current in the SIMBC will result in the following equation by substituting the voltage gain expressed in equation 4.5 into equation 4.6.

$$I_{LSIMBC} = \frac{3V_o(1+d)}{(1-d)R_o} \tag{4.7}$$

In a practice, it is essential to take into account the inductor's equivalent series resistance ($R_{ESR,L}$). As a result, the voltage gain can be formulated as:

$$\frac{V_o}{V_{in}} = \frac{3(1-d^2)R_o}{(1-d)^2R_o + 9(1+d)R_{ESR,L}} \tag{4.8}$$

Equation 4.8 makes it clear that the inclusion of inductor $R_{ESR,L}$ in the circuit decreases the voltage gain of the SIMBC. Consequently, to achieve the desired output voltage in a practical converter, it is necessary to raise the duty cycle.

The data in Figure 4.8, depict the voltage gains of three-level SIMBC as a function of the duty cycle for different values of the equivalent series resistance (ESR) of the inductor. The data show that incorporating the inductor ESR reduces the voltage gain and necessitates increasing the duty cycle to reach the desired voltage conversion ratio. For instance, to achieve a gain of 20, the duty cycle needs to change from 0.74 to 0.81 as $R_{ESR,L}$ changes from 0.028 Ω to 1 Ω. In addition, it can be noticed that for a duty cycle greater than 0.9, the voltage gain collapses due to the effect of the inductor ESR. Therefore, selecting an appropriate inductor with low ESR becomes vital for high gain power converters. High ESR in an inductor result in higher power dissipation

and lower circuit efficiency. Additionally, it causes a voltage drop across the inductor that reduces the voltage available for the load, thus reducing the voltage gain.

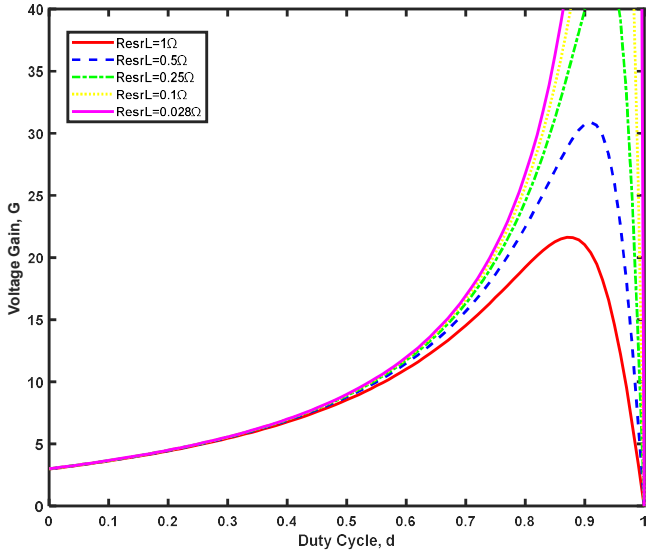

Figure 4.8: Voltage gain characteristic of the SIMBC versus duty cycle for different values of $R_{ESR,L}$.

In the VLSIMBC circuit, the transfer of input power to the output is accomplished by charging and discharging the switched-inductor, charge pump capacitor C_v, and the capacitors in the voltage multiplier. In Mode 1, as shown in Figure 4.5, diodes D_{s1}, D_{s2}, D_2 and D_4 are forward-biased. Since the inductors L_1 and L_2 have a parallel connection in this mode, they exhibit a voltage drop equal to V_{in}. At the same time, capacitor C_v is charged by V_{in} through diode D_1, so that

$$V_{Cv} = V_{in} \tag{4.9}$$

In Mode 2, as shown in Figure 4.5, diodes D_1, D_3 and D_5 are forward-biased whilst inductors L_1 and L_2 have a series connection, and so

$$V_{in} = V_{L1} - V_{Cv} + V_{L2} + V_{C1} \tag{4.10}$$

Since L_1 and L_2 are identical, they will be charged equally, and so the average inductor voltage can be expressed as

$$V_L = d\,(V_{in}) + (1-d)\left(\frac{(2V_{in} - V_{C1})}{2}\right) = 0 \qquad 4.11$$

In steady-state operation, the voltage across the output capacitors can be expressed as:

$$V_C = V_{C1} = V_{C3} = V_{C5} = \frac{2}{1-d}V_{in} \qquad 4.12$$

and the SIMBC output voltage is the total of the voltages across the capacitors, therefore

$$V_o = 3V_C = \frac{6}{1-d}V_{in} \qquad 4.13$$

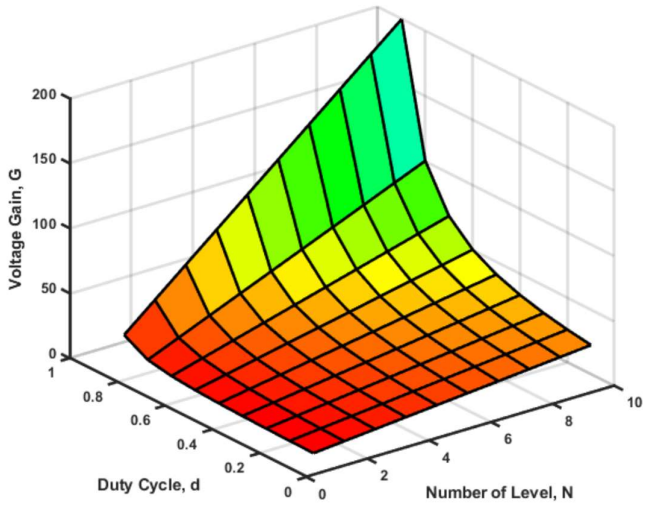

Figure 4.9: Ideal Voltage gain characteristic of the VLSIMBC as a function of *d* and *N* values.

Figure 4.9 shows the three-dimensional view of the ideal voltage gain *G* of VLSIMBC as a function of duty cycle *d* for different numbers of levels *N*. Increasing the number of levels results in a higher voltage gain. The duty cycle also increases with increasing voltage gain, and this relationship often guides the selection of a

particular voltage gain. Moreover, that data verifies that the VLSIMBC topology results in an enhancement of the voltage gain in comparison to the MBC and SIMBC.

As before, the average inductor current in the VLSIMBC can be expressed by substituting the voltage gain from equation 4.13 into equation 4.6, resulting in

$$I_{LVLSIMBC} = \frac{6V_o}{(1-d)R_o} \tag{4.14}$$

The voltage gain, considering the inclusion of the equivalent series resistance of the inductors, ($R_{ESR,L}$), can be expressed as

$$\frac{V_o}{V_{in}} = \frac{6(1-d)R_o}{(1-d)^2R_o + 18R_{ESR,L}} \tag{4.15}$$

Figure 4.10 displays the plot of voltage gains for three-level VLSIMBC as a function of the duty cycle for various equivalent series resistance (ESR) values of the inductor. The results indicate that incorporating the inductor ESR lowers the voltage gain and demands an increase in the duty cycle to achieve the desired voltage conversion ratio. To be specific, to achieve a gain of 20, the duty cycle needs to change from 0.7 to 0.78 as $R_{ESR,L}$ changes from 0.028 Ω to 0.5Ω. It can be seen from the data also that the proposed VLSIMBC offers a higher voltage gain in comparison to both the MBC presented in Chapter 3 and SIMBC, and this advantage increases as the duty cycle on the switch increases. For instance, a duty cycle of 43% in VLSIMBC achieves a desired gain of 10, whereas it takes duty cycles of 73% and 56% for MBC and SIMBC, respectively, to achieve the same gain.

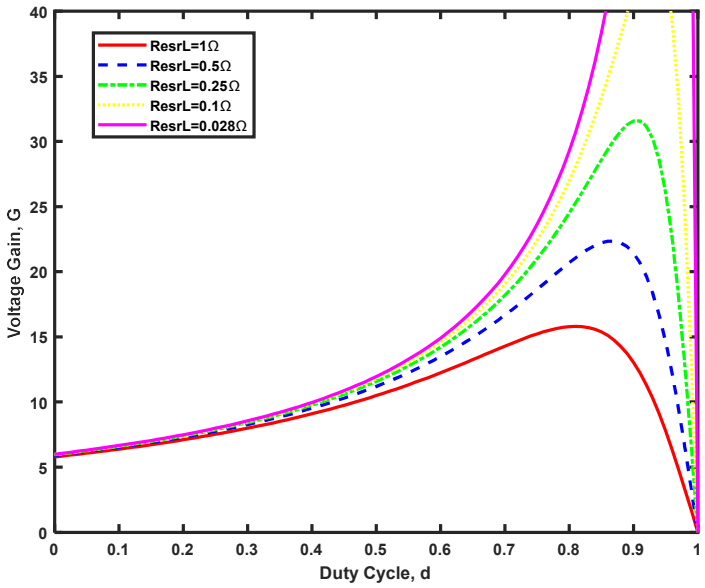

Figure 4.10: Voltage gain characteristic of the VLSIMBC versus d for different values of $R_{ESR,L}$.

4.3.2 Voltage Stress

The voltage stress experienced by the switch in the SIMBC and VLSIMBC is shown in Figure 4.3 (h) and Figure 4.5 (h). Notably, the voltage across the switch is lower than the output voltage, which differs from the behaviour of a conventional boost converter. The voltage stress reduction leads to another advantage of the SIMBC and VLSIMBC, which is the ability to select lower-rating semiconductor devices, resulting in reduced costs and lower losses for transistors. According to the data shown in Figure 4.4 (b) and Figure 4.6 (b), the voltage across the switch, V_S, in both proposed converters is equal to the voltage across capacitor 1 (V_{C1}). The voltage stress experienced by the switch in the three-level SIMBC can be expressed as

$$V_{S,SIMBC} = \frac{V_O}{3} = \frac{(1+d)V_{in}}{1-d} \qquad 4.16$$

While for the three-level VLSIMBC, the voltage stress across the switch can be estimated as

$$V_{S,VLSIMBC} = \frac{V_O}{3} = \frac{2V_{in}}{1-d} \qquad 4.17$$

It can be observed from equations 4.16 and 4.17, the switch blocking voltages can be defined as a function of the input voltage, output voltage, and duty cycle. Hence, the ability to express the voltage across the switch in this manner is a useful feature, as it allows for the optimization of the converter performance based on the desired input and output voltage requirements.

In accordance with equations 4.16 and 4.17, Figure 4.11 displays the relationship between the duty cycle and the normalized voltage stress across the switch in SIMBC and VLSIMBC. As the duty cycle rises, the voltage stress on the switches also increases for both topologies. Additionally, VLSIMBC has a higher normalized voltage stress across the switch than SIMBC due to its higher voltage gain.

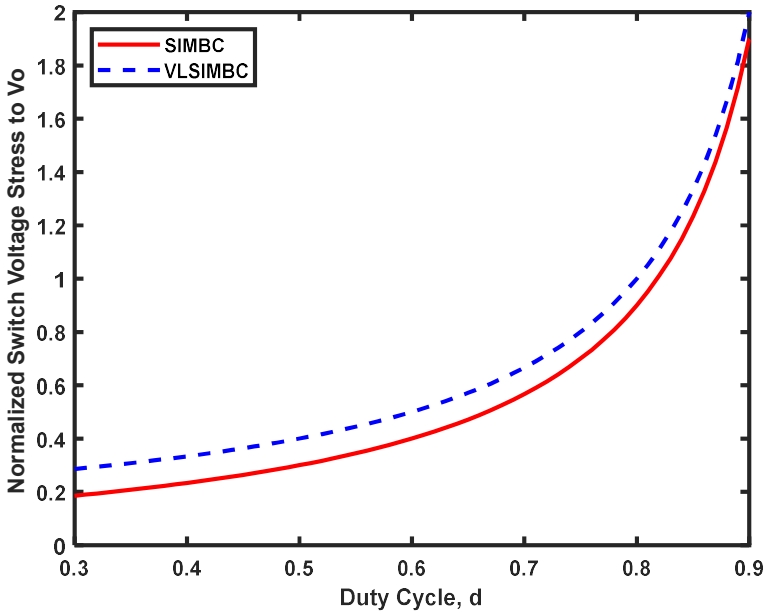

Figure 4.11: Normalized voltage stress of SIMBC and VLSIMBC versus *d*.

The voltage stress of the voltage multiplier diodes $V_{d1} - V_{d5}$ in the SIMBC is equal to the voltage across the switch and increases as the duty cycle increases. As equation 4.16 stated, the value is consistently lower than the output voltage and the same switch voltages. Whereas the voltage stress of the input diodes V_{ds1}, V_{ds2} and V_{ds3} can be expressed as

$$V_{ds1} = V_{ds3} = V_{L1} = V_{L2} = \frac{dV_{in}}{1-d} \quad 4.18$$

$$V_{ds2} = V_{in} \quad 4.19$$

For the VLSIMBC topology, the voltage stress of the voltage multiplier diodes $V_{d1} - V_{d5}$ is the same to the voltage across the switch and increases as the duty cycle increases, as presented in equation 4.17. However, the voltage stress of the input diodes V_{ds1} and V_{ds2} can be expressed as

$$V_{ds1} = V_{ds2} = V_{L1,L2} + V_{cv} = \frac{V_{in}}{1-d} \quad 4.20$$

The capacitors have a capacitance value sufficient to fulfil the circuit requirements in the three-level SIMBC and VLSIMBC topologies, ideally maintaining a similar voltage level. This implies that each capacitor will experience voltage stress similar to the voltage stress across the switch, as defined in equations 4.16 and 4.17.

4.4 SIMULATION AND EXPERIMENTAL VERIFICATION

In this work, the essential features required to validate the operating characteristics and high voltage gain of the three-level SIMBC and VLSIMBC topologies have been highlighted. These topologies have been specifically developed in order to facilitate the integration of renewable energy converters into an MVDC collection network. The simulation and prototype results confirm that these converters perform effectively.

4.4.1 High Gain SIMBC and VLSIMBC Prototype

A prototype has been implemented in the laboratory and tested to verify the operation and evaluate the performance of the three-level SIMBC and VLSIMBC topologies. The parameters of the converters, along with the component ratings, are the same as the MBC parameters in Chapter 3 and derived from analysis described in sections 4.3 and 3.4. The photograph of the prototype power converters is shown in Figure 4.12 and Figure 4.13. As can be seen, the only difference is in the input circuit. The experimental setup is the same as that of MBC described in section 3.5.1. The second inductor in the SIMBC and VLSIMB is the same toroidal power inductor (HF467-102M-26AH) used in Chapter 3. Additionally, the input diodes for both topologies are the same as the output diodes of SiC Schottky Diodes (GeneSiC Semiconductor part number GB05MPS33-263) utilised in Chapter 3.

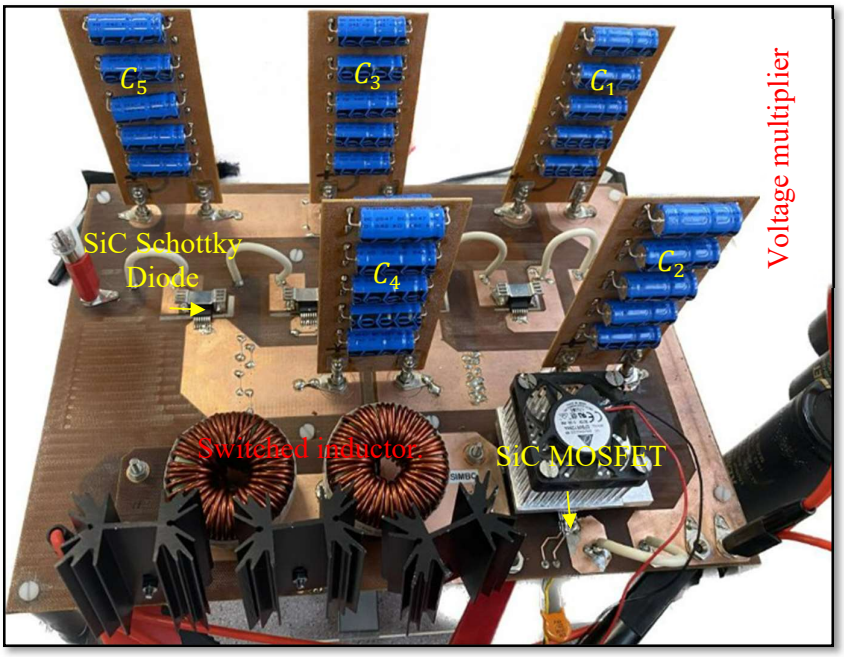

Figure 4.12: Three-level SIMBC experimental prototype.

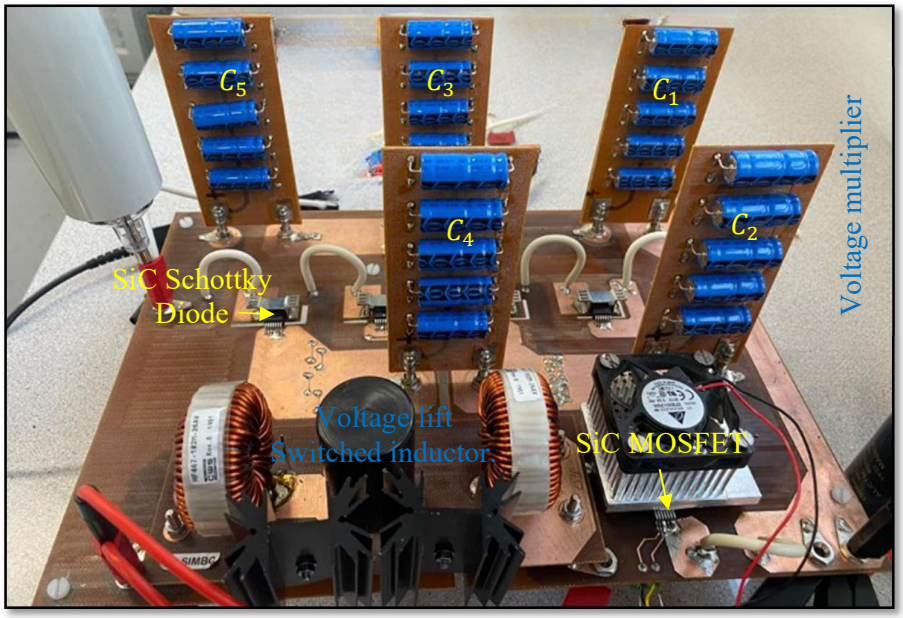

Figure 4.13: Three-level VLSIMBC experimental prototype.

4.4.2 Simulation and Measured Experiment Results

LTSpice was used to determine the performance of the proposed converters and to validate the analytical analysis. Table 4-1 summarises the operating parameters of the converters and component ratings. The same parameters are employed in both the simulation and experimental prototype to facilitate a comparison.

Table 4-1. Design Specification for Three-Level SIMBC and VLSIMBC.

Parameter	Symbol	Rating
Input Voltage	V_{in}	500 V
Output Voltage	V_o	5 kV
Output Load	R_o	10 kΩ
Switching Frequency	f	50 kHz
Inductor	$L_1 and\ L_2$	1 mH, 26 A, ESR 28 mΩ
Capacitors	$C_1 - C_5$	1μF, 4.5 kV
Switch	S	G2R120MT33J
Diodes	$(D_1 - D_5)\ and\ D_{s1} - D_{s3}$	GB05MPS33-263

The simulated features of a three-level SIMBC and VLSIMBC are used to boost a 500 V DC input voltage to a 5 kV output voltage. Based on the analysis discussed in section 4.3, the duty cycle was not allowed to exceed 56% for the SIMBC and 43% for the VLSIMBC in order to ensure an adequate amount of the operating period with the switch switched off and to avoid severe voltage stress across the switch while reaching a gain factor of 10.

4.4.2.1 Switched Inductor Multilevel Boost Converter

A three-level SIMBC was examined, and it was determined that a duty cycle of 54% would produce an output voltage of 5 kV and an output power of 2.5 kW. To attain a gain of 10 with a single switch and generate the required output voltage of 5 kV, equation 4.5 indicates that a duty cycle of d = 0.54 is needed. While due to non-ideal conditions often present in practical applications, a duty cycle of d = 0.56 was necessary to achieve the desired gain. However, since the gate drive produces a delay, which reflects a change in the duty cycle, the MOSFET's duty cycle is 0.55. Simulation and experimental waveforms for the converter operating at 50 kHz are presented in Figure 4.14 through 4.20. Overall, the experimental waveforms closely match those obtained from the SPICE simulations.

The data in Figure 4.14 display the input and output voltage waveforms. The simulation and experimental outcomes validate the accuracy of the equations introduced in section 4.3 for determining the voltage gain of the three-level DC-DC SIMBC. The voltage gain values attained from the practical and simulation are 9.89 and 9.97, respectively. Notably, the experimental waveforms display switching transients that are absent in the simulation results. The input voltage transients, which materialize during the turn-on and turn-off transients, arise from the parasitic capacitances and inductances in the circuit. The output voltage transients are

associated with the propagation of input transients through the circuit. Therefore, input transients can influence the circuit components, resulting in changes in the output voltage until the circuit stabilizes. Hence, by applying a sudden voltage change to the circuit and monitoring the result for any transients, output voltage transients can be observed to be certainly associated with the propagation of the input transients through the circuit.

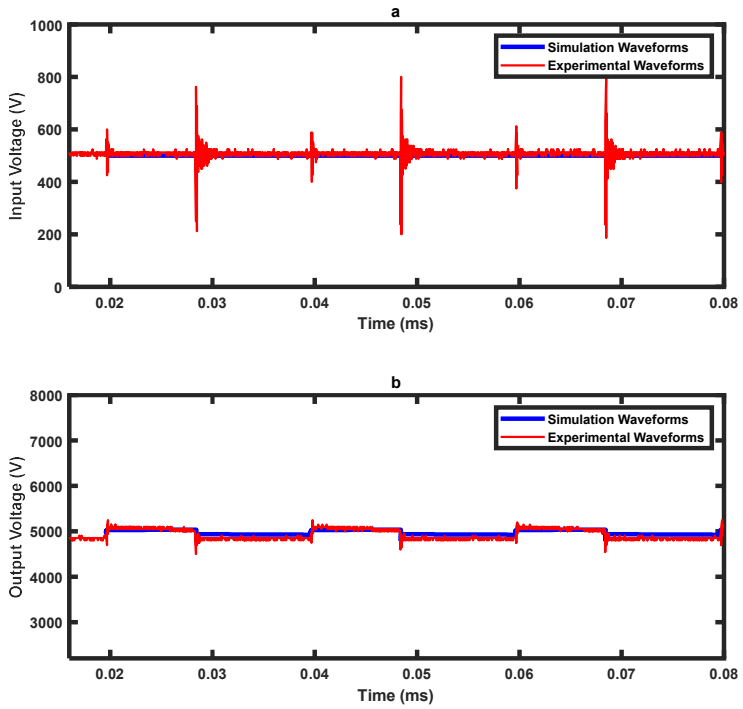

Figure 4.14: Input and output voltage waveforms of the three-level SIMBC.

The input and output currents are also shown by the waveforms in Figure 4.15. The inductor current I_L is continuous demonstrating that the converter is operating in CCM as predicted using equation 4.7. The current ripple in the inductor is equal to 8.33%. The average of inductor current is 5.45 A, which matches the value of 5.32 A predicted using equation 4.7. At the output, an average voltage 5 kV is obtained with an output current of 0.5 A through the load as shown by the data in Figure 4.15. Based on these values, the power output achieved is 2.5 kW. It can be observed from Figure

4.15 (a) that the simulation and experimental results slightly differ in terms of the ripple current due to the inclusion of the parasitic components, including capacitance and inductance, in the practical. In addition, the stray inductance arising from circuit layout leads to variance between practical and simulations.

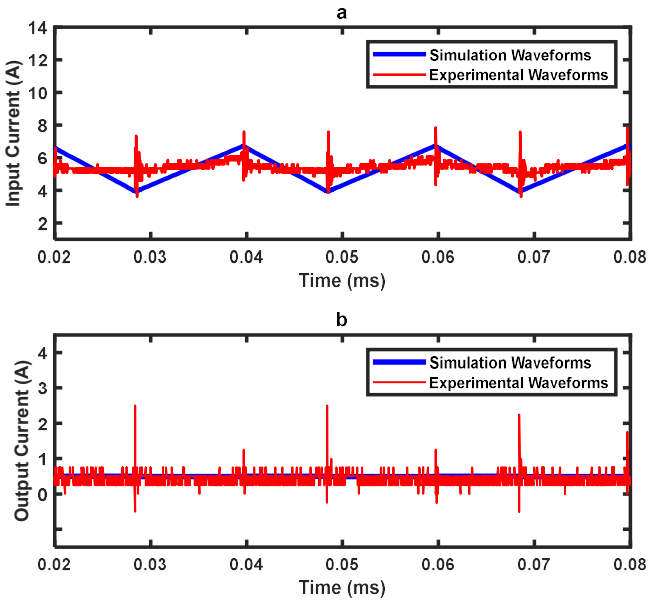

Figure 4.15: Input and output current waveforms of the three-level SIMBC.

The voltage across the inductors V_{L1}, V_{L2} and the overall input inductor V_L are shown by the data in Figure 4.16. The experimental values of V_{L1} and V_{L2} when the switch is ON equal 500 V and when the switch is OFF equals -655 V, which matches the simulation result shown in Figure 4.16 (b) and theoretical predictions based on equation 4.3. The simulated and calculated values of V_{L1} and V_{L2} when the switch is ON equal 500 V and when the switch is OFF equals -625 V and -610 V, respectively. It can be observed from the data that the experimental value of V_L when the switch is ON equals 500 V and when the switch is OFF equals -1275 V, which matches the simulation result shown in Figure 4.16 (a) and theoretical analysis shows in Figure 4.3.

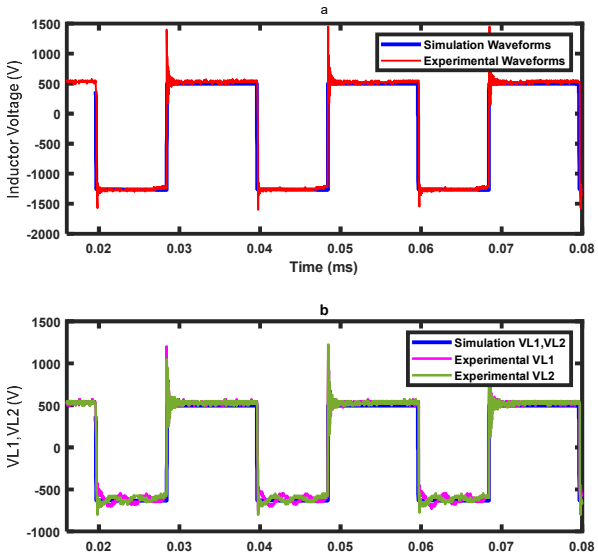

Figure 4.16: Voltage across L_1, L_2 and the effective inductor L for the SIMBC.

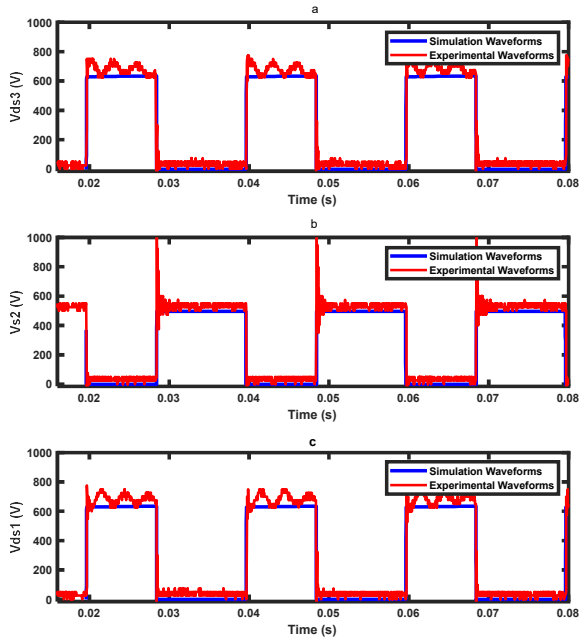

Figure 4.17: Voltage across D_{s1}, D_{s2} and D_{s3} for the three-level SIMBC.

The waveforms of the input diodes during the switching cycle are shown by the data in Figure 4.17. As described in section 4.3, diodes D_{s1} and D_{s3} are forward biased during charging while D_{s2} is forward biased during discharging. The diodes D_{s1} and D_{s3} voltage show ringing due to resonance of intrinsic inductance and capacitance.

It occurs as a result of the inductor's stored energy being discharged and charged periodically, resulting in ringing around the desired value.

The data in Figure 4.18 show the drain-source voltage and corresponding drain-source current of the MOSFET in the three-level SIMBC. The data highlight a significant benefit of the proposed converter, which is the reduction of voltage stress on the switch. The maximum drain-source voltage across the switch is 1800 V at an output voltage of 5 kV, as theoretically predicted based on equation 4.16. This finding suggests the possibility of achieving higher output voltages without using high voltage FETs. There is a sufficient match between the experimental and simulation results, as shown by the agreement between the measured and simulated drain-source currents, with measured and simulation average drain-source current values of 5.53 A and 5.41A, respectively. These findings support the theoretical analysis in equation 4.16 and demonstrate consistency between the experimental and simulated results.

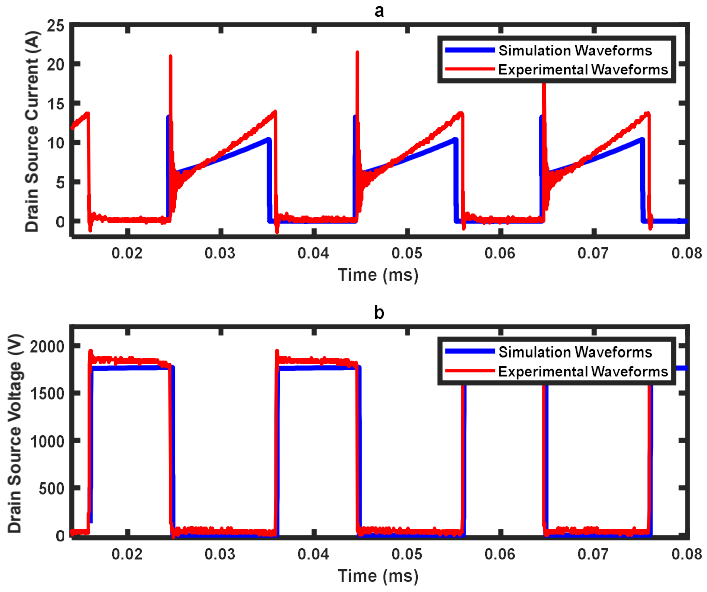

Figure 4.18: Drain-source voltage and current across the switch of the three-level SIMBC.

The data in Figure 4.19 show that the voltage across the three output capacitors, C_1, C_3 and C_5 are equal, except for the forward voltage drop over the diodes, losses in the parasitic components and the equivalent series resistance of the capacitors utilized for C_1, C_3 and C_5. With ideal capacitors, the simulation voltage difference between C_1 and C_3 is 22 V, while 18 V is between C_3 and C_5. The measured voltage on the output capacitors C_1, C_3 and C_5 are 1800 V, 1650 V and 1550 V. Hence, each capacitor maintains the same voltage levels and voltage balance is obtained across all capacitors. The voltage transients observed in the output capacitors are a result of the parasitic effects present at the circuit's input, as well as the turn-on and turn-off transients of the MOSFET. During the turn-on and turn-off changes of the MOSFET, there is a short time during which the voltage across the MOSFET changes rapidly. Consequently, this voltage change can lead to a transient voltage spike in the circuit, affecting the output capacitors.

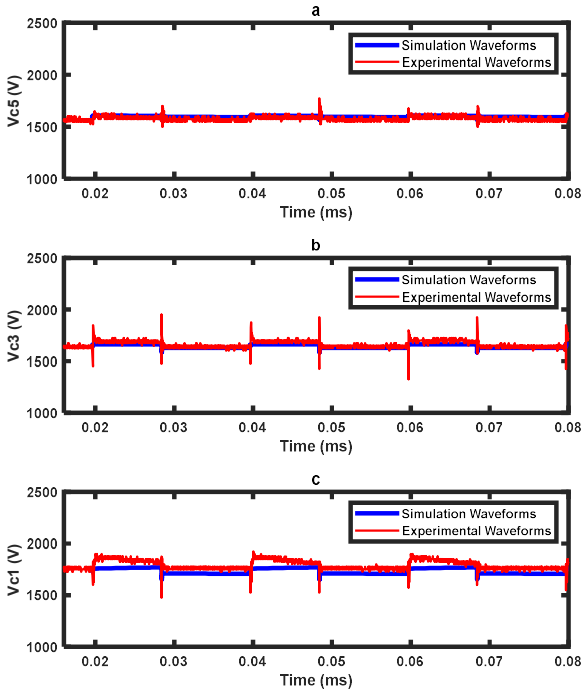

Figure 4.19: Voltage across the output capacitors C_1, C_3 and C_5 of the three-level SIMBC.

The drain-source voltage across the switch and the voltage across all five diodes for the SIMBC topology are displayed in Figure 4.20. The data confirms the operating principle of SIMBC: diodes D_2 and D_4 are forward-biased when the switch is ON, $(0.028 \leq T < 0.039 \text{ ms})$ and diodes D_1, D_3, and D_5 are forward-biased when the switch is OFF, $(0.039 \leq T \leq 0.048 \text{ ms})$. Additionally, one of the substantial advantages of the proposed converter is a reduction in the voltage stress on the switch and diodes.

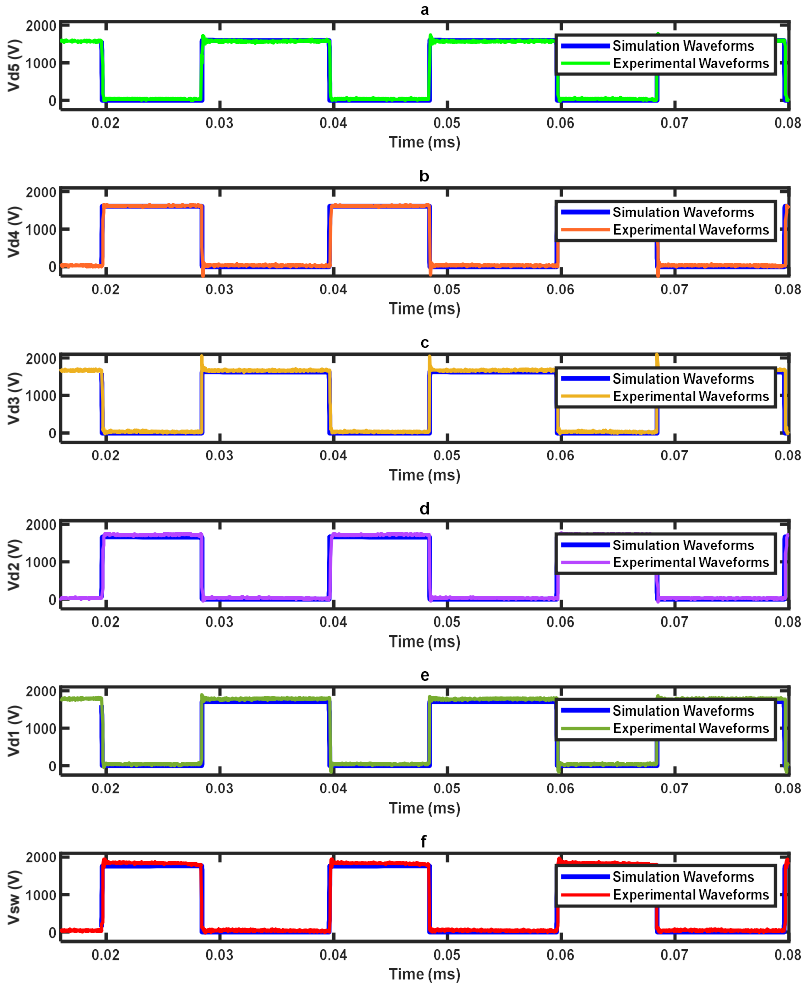

Figure 4.20: Drain-source voltage across the switch with voltage across D_1, D_2, D_3, D_4, D_5 of the three-level SIMBC.

4.4.2.2 Voltage Lift Switched Inductor Multilevel Boost Converter

In this topology, to generate the needed output voltage of 5 kV with a gain of 10, the working duty cycle is 0.41. In this instance, the duty cycle of the switch is adjusted to operate at 0.43 in order to take into consideration the non-ideal parameters as described by equation 4.15. Due to the gate drive causing a delay, the MOSFET's duty cycle is 0.42. The input voltage and output voltage waveforms of the VLSIMBC are shown in Figure 4.21. The simulation and experimental results confirm the ability of the proposed converter to achieve high voltage gain. The voltage gain values achieved from the practical and simulation are 9.9 and 10, respectively.

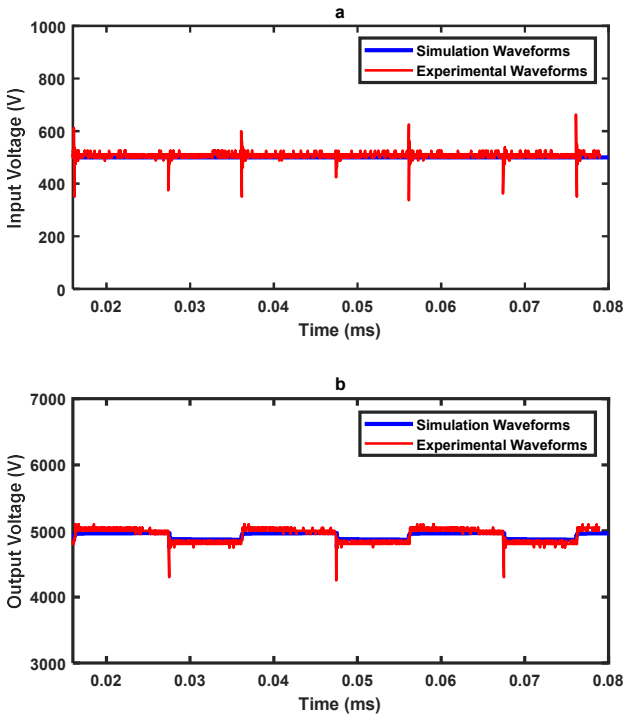

Figure 4.21: Input and output voltage waveforms of the three-level VLSIMBC.

The data in Figure 4.22 show the input and output currents waveforms for the VLSIMBC. The output of 5 kV is obtained with a 0.5 A current flow through the load as shown by the waveforms in Figure 4.22 (b). The inductor current (I_L) is continuous,

confirming operation in CCM as predicted by equation 4.14. The percentage of ripple in the inductor is equal to 4.55%, which is lower than that observed for both the MBC and SIMBC topologies described earlier when operating under identical conditions. The average of inductor current is 5.36 A which matches the theoretical predictions from equation 4.14, which is 5.26 A. The data in Figure 4.22 (a) show similar observations to MBC and SIMBC of the difference between the simulations and experimental results regarding the ripple current for the same reasons.

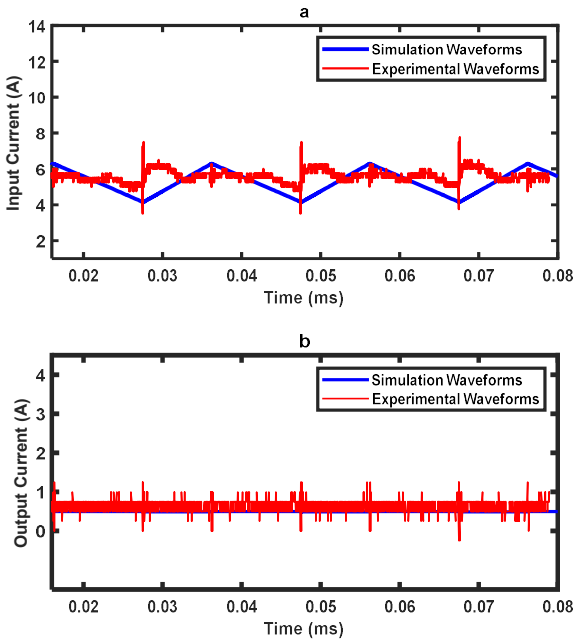

Figure 4.22: Input and output current waveforms of the three-level VLSIMBC.

The voltage across the inductors V_{L1} and V_{L2} and the overall input inductance, V_L, are shown by the waveforms in Figure 4.23. The experimentally measured value of V_{L1} and V_{L2} when the switch is ON is 500 V and when the switch is OFF equals - 376 V which is in accordance with predictions from the equation 4.11. The simulated and calculated values of V_{L1} and V_{L2} when the switch is ON equal 500 V and when the switch is OFF equals -371 V and -350, respectively. However, the measured value of V_L when the switch is ON equals 500 V and when the switch is OFF equals -1250V.

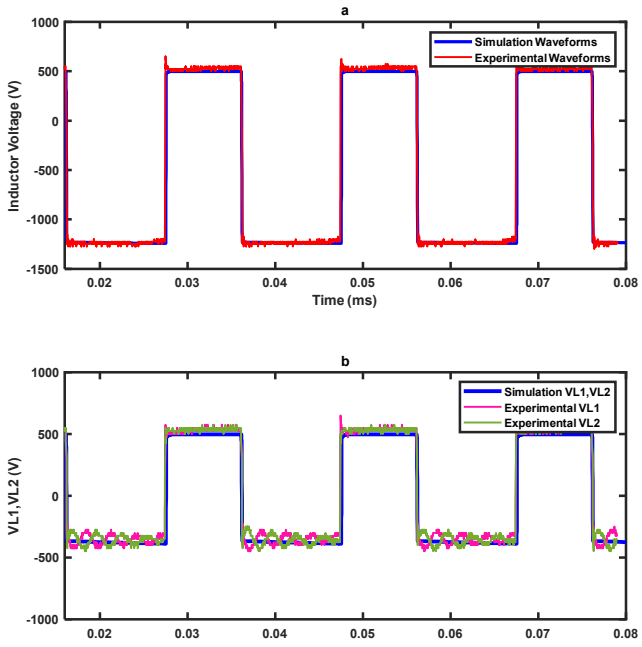

Figure 4.23: Voltage across L_1, L_2 and the effective inductor L for the VLSIMBC.

The voltage stress of the input side diodes and the voltage across the charge pump capacitor V_{cv} are shown by the data in Figure 4.24. Diodes D_{s1} and D_{s2} are forward biased during charging and the experimental voltages are 930 V, which are close to the simulation results and theoretical estimations as predicted from equation 4.20 which are 860 V and 850 V, respectively. The voltage across diodes D_{s1} and D_{s2} show ringing due to resonance of intrinsic inductance and capacitance of the circuit. This ringing is caused by the inductor's stored energy being discharged and charged regularly, which is the same as for the SIMBC. Moreover, the experimental value of the charge pump capacitor V_{cv} is equal 520 V, which is in agreement with the simulation and analytical results.

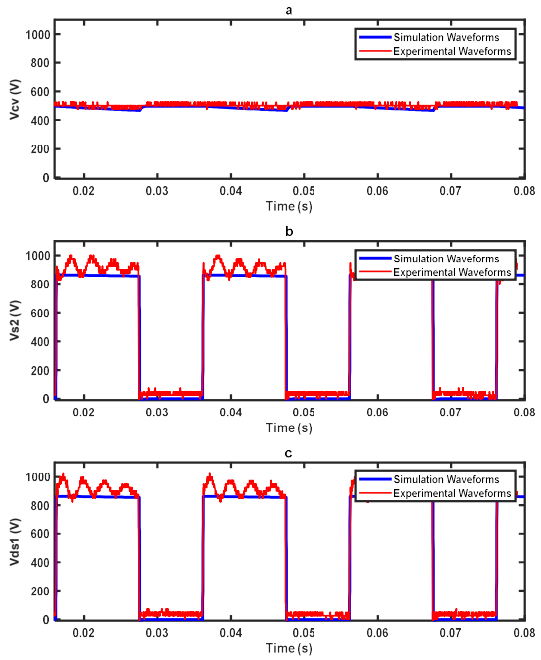

Figure 4.24: Voltage across D_{s1}, D_{s2} and V_{cv} for the three-level VLSIMBC.

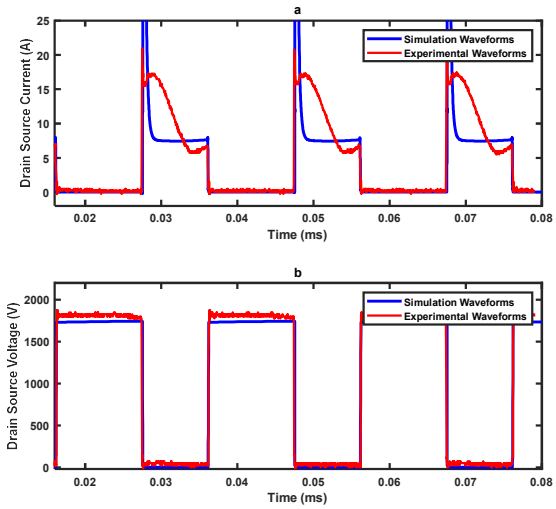

Figure 4.25: Drain-source voltage and current across the switch of the three-level VLSIMBC.

In Figure 4.25, the drain-source voltage and corresponding drain-source current for the MOSFET in three-level VLSIMBC are displayed. The results highlight a significant advantage of the proposed converter, which is the reduction of voltage

stress on the switch. The maximum drain-source voltage is 1770 V when the output voltage is 5 kV, as expected. This finding supports the theoretical analysis presented in equation 4.17. Furthermore, the measured drain-source current closely matches the simulation predictions, indicating consistency between the experimental and simulated results which are 5.43 A and 5.38 A, respectively.

The data in Figure 4.26 show similar behaviour to that for the SIMBC topology in that the voltage across the three output capacitors, C_1, C_3 and C_5 are almost similar, with a minor reduction that arises from the voltage drop forward across the diodes, losses in the parasitic elements and the equivalent series resistance of the capacitors. By considering the ideal capacitors, the simulation voltage difference between C_1 and C_3 is 15 V and 7 V between C_3 and C_5. The measured voltage on the output capacitors C_1, C_3 and C_5 are 1770 V, 1630 V and 1600V, respectively.

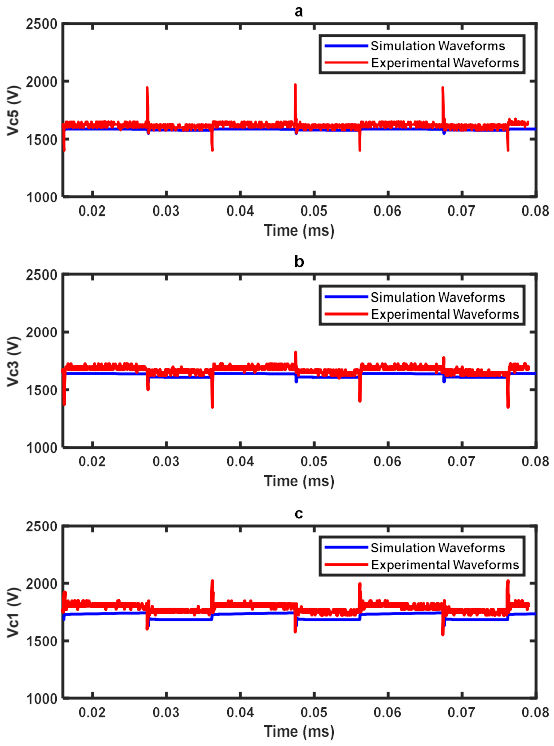

Figure 4.26: Voltage across the output capacitors C_1, C_3 and C_5 of the three-level VLSIMBC.

The data in Figure 4.27 illustrate the drain-source voltage across the switch with the voltage across the five diodes in the output stage of the VLSIMBC topology. The data confirm the operating principle of VLSIMBC; when the switch is ON, $(0.028 \leq T < 0.039 \text{ ms})$, diodes D_2 and D_4 are forward-biased and when the switch is OFF, $(0.039 \leq T \leq 0.048 \text{ ms})$, diodes D_1, D_3 and D_5 are forward-biased. The data in Figure 4.27 also show that the maximum drain-source voltage across the switch is 1770 V when the output voltage is 5 kV, in agreement with the predictions from equation 4.17.

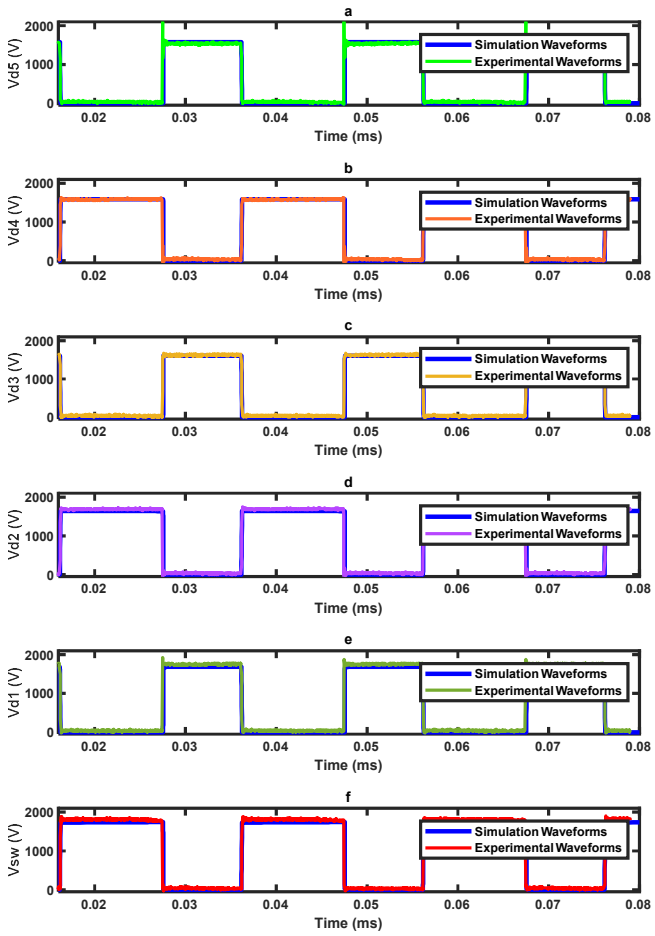

Figure 4.27: Drain-source voltage across the switch with voltage across D_1, D_2, D_3, D_4, D_5 of the three-level VLSIMBC.

4.5 POWER LOSS ANALYSIS AND EFFICIENCY MEASUREMENT

The efficiency of the SIMBC and VLSIMBC is affected by the internal properties of each component and device. This section outlines the power loss produced by each component.

4.5.1 Power Losses in Inductor

The average current of the inductor has a major influence on the copper loss for the inductor. Hence, the power loss can be described as $P_L = I_L^2 R_{ESR,L}$, where $R_{ESR,L}$ is inductor equivalent series resistance. Since the three-level SIMBC has two identical inductors, the inductor copper loss $P_{L,SIMBC}$ can be expressed as

$$P_{L,SIMBC} = 2\left(\left(\frac{3V_o(1+d)}{(1-d)R_o}\right)^2 R_{ESR,L}\right) \quad 4.21$$

While the VLSIMBC with two identical inductors, the inductor copper loss $P_{L,VLSIMBC}$ can be expressed as:

$$P_{L,VLSIMBC} = 2\left(\left(\frac{6V_o}{(1-d)R_o}\right)^2 R_{ESR,L}\right) \quad 4.22$$

A comparison of equations 4.21 and 4.22 leads to the observation that the inductor losses present in the VLSIMBC are less susceptible to changes in the duty cycle d and, so this indicates that this topology is more suitable for deployment in a renewable energy, like a wave energy system, where changes in duty cycle are required to maintain a constant output voltage for a range of input voltages. For example, the inductor losses for SIMBC at $d = 0.4$ and $d = 0.5$ are 0.69 W and 1.13 W, respectively. Hence, the percentage change in power will be 63.77%. In contrast, with the same change in duty cycles, the VLSIMBC inductor losses are 1.4 W and 2.02 W, respectively. Thus, the percentage change in power will be 44.29%. Accordingly,

comparing the percentage changes in power for the two converters indicates that the VLSIMBC is less sensitive to duty cycle D changes.

4.5.2 Power Losses in Capacitor

The power loss in the capacitor is derived using the RMS current flowing through the capacitor as well as its effective series resistance ($R_{ESR,C}$). The equation of power loss in the capacitors for three-level SIMBC is similar to the MBC topology in Chapter 3, as conveyed in equation 3.22. However, the VLSIMBC has one extra capacitor C_v in the input side, and thus the power loss in capacitors can be calculated as

$$P_{C,VLSIMBC} = I_{Cv}^2 R_{ESR,Cv} + I_{C1}^2 R_{ESR,C1} + I_{C2}^2 R_{ESR,C2} + I_{C3}^2 R_{ESR,C3} + I_{C4}^2 R_{ESR,C4} + I_{C5}^2 R_{ESR,C5} \quad (4.23)$$

4.5.3 Power Losses in Switch

The power switch used in practical applications experiences both conduction and switching losses. For three-level SIMBC and VLSIMBC topologies, the conduction loss of the switch can be derived by examining the current and voltage characteristics across the drain and source, and can be expressed as

$$P_{SC,SIMBC} = \left(\frac{3V_o(1+d)}{2(1-d)R_o}\right)^2 R_{DS,(ON)} \quad (4.24)$$

$$P_{SC,VLSIMBC} = \left(\frac{6V_o}{2(1-d)R_o}\right)^2 R_{DS,(ON)} \quad (4.25)$$

where $R_{DS,(ON)}$ represents the drain- source resistance.

The switching power loss of the switch is influenced by a number of factors, including the voltage across the switch, peak current, turn-on (t_{ON}) and turn-off (t_{OFF}) times, and switching frequency. The equation of switching loss for SIMBC and VLSIMBC

are similar to the switching loss equation of the MBC in Chapter 3, as presented in equation 3.20 since the same switch is utilised.

The switch total loss for SIMBC and VLSIMBC can be determined using

$$P_{S,SIMBC} = P_{SC,SIMBC} + P_{SW} \quad 4.26$$

$$P_{S,VLSIMBC} = P_{SC,VLSIMBC} + P_{SW} \quad 4.27$$

4.5.4 Power Losses in Diodes

Diode losses are classified as follows: loss caused by forward voltage drop (V_F) and conduction loss caused by internal resistance inducing conduction (r_f)[106]. The loss due to forward voltage drop is obtained using the average current, whereas the conduction loss relies on the RMS current of the diodes. The equation of diode's average current $I_{D,avg}$ for the SIMBC and VLSIMBC is same as the equation of MBC, as stated in equation 3.26. Therefore, total loss in diodes for the three-level SIMBC and VLSIMBC topologies can be expressed as:

$$P_{D,SIMBC} = \sum_{i=1}^{8} I_{D,avg} V_F + \sum_{i=1}^{8} I_{D,rms}^2 r_f \quad 4.28$$

$$P_{D,VLSIMBC} = \sum_{i=1}^{7} I_{D,avg} V_F + \sum_{i=1}^{7} I_{D,rms}^2 r_f \quad 4.29$$

Hence, the total power loss in the proposed converters is given as

$$P_{Losses,SIMBC} = P_{L,SIMBC} + P_{C,SIMBC} + P_{S,SIMBC} + P_{D,SIMBC} \quad 4.30$$

$$P_{Losses,VLSIMBC} = P_{L,VLSIMBC} + P_{C,VLSIMBC} + P_{S,VLSIMBC} + P_{D,VLSIMBC} \quad 4.31$$

4.5.5 Calculating the Efficiency

The Efficiency (η) of the proposed converters can be expressed as

$$\eta = \left(\frac{P_o}{P_o + P_{Losses}}\right) \tag{4.32}$$

Figure 4.28 and Figure 4.29 illustrate the efficiency of the three-level SIMBC and VLSIMBC topologies as a function of output power with changing the load resistances, as extracted from simulation and experimental data. The results demonstrate that SIMBC generally achieves a maximum measured efficiency of 92.1% at 2.5 kW output power, while its simulated efficiency is 95.5% at the same output power. On the other hand, the VLSIMBC has a better performance with a maximum measured efficiency is 93.2% with an output power of 2.5 kW and a simulated efficiency of 96.6% at the same output power, as shown in Figure 4.29. The difference between the simulated and experimental efficiency may be due to core losses in the inductor not being incorporated in the simulation efficiency and parasitic capacitances and inductances in the circuit leading to switching transients of input and output voltage, as shown by the data in Figure 4.14 and Figure 4.21.

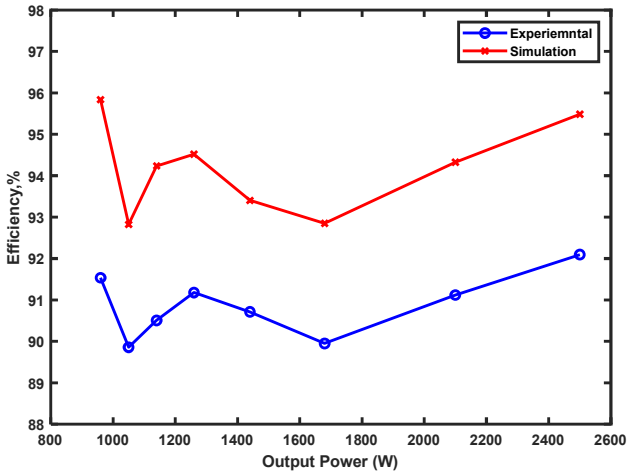

Figure 4.28: Simulation and practical efficiency with respect to the output power of the three-level SIMBC.

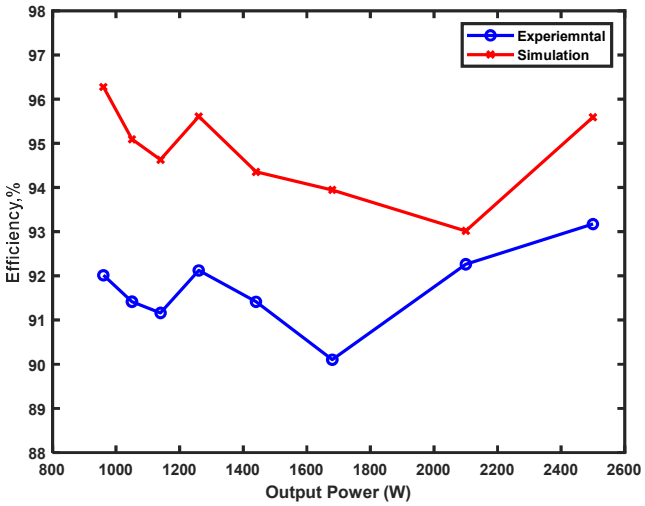

Figure 4.29: Simulation and practical efficiency with respect to the output power of the three-level VLSIMBC.

Furthermore, the power ratings of the chosen parts in the hardware prototype were employed for a loss analysis based on the experimental data and practical values. The distribution of losses in the proposed converters SIMBC and VLSIMBC is displayed in Figures 4.30 and 4.31. The data demonstrate that the most significant losses arise from the capacitors and the SiC MOSFET, which are same for the MBC presented in Chapter 3. In practice, capacitors add to the losses in a power converter due to their ESR, which is an equivalent series resistance present in series with their ideal capacitance. It should be noted that the capacitors utilized in the circuit were not optimally chosen for efficiency. The ESR generates heat and power dissipation when capacitors are used in a power converter, resulting in losses. Therefore, selecting capacitors with low ESR can assets in reducing converter losses. In addition, the MOSFET is another major contributor to losses since the converters operates at a high switching frequency and voltage rating. Therefore, the MOSFETs utilized in the converter can significantly add to the losses. Finally, carefully selecting components and optimizing the converter design can minimize losses and enhance the efficiency.

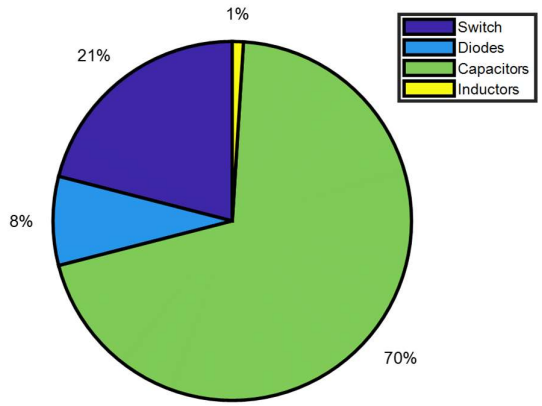

Figure 4.30: Percentage distribution of losses of the three-level SIMBC.

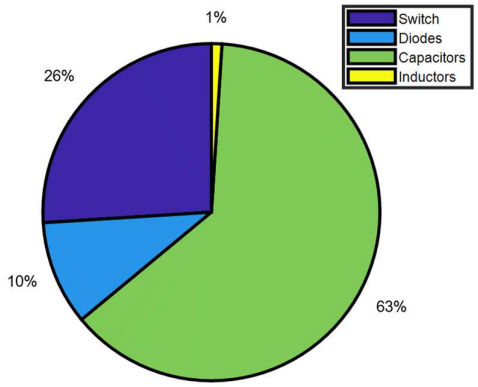

Figure 4.31: Percentage distribution of losses of the three-level VLSIMBC.

4.6 SUMMARY

Isolated DC-DC converters are unsuitable for achieving high conversion ratios due to power transformer losses and stray inductance resulting from the circuit layout. These converters also suffer from high weight and large volumes, which makes their integration within renewable energy, such as wave energy converters challenging. This chapter demonstrates that a transformerless DC-DC multilevel boost converter is a potential solution to the challenge of achieving a high voltage gain in a DC-DC

converter. The transformerless DC-DC high voltage gain converters presented in this chapter are improvements on the multilevel boost converter (MBC) design, including the switched inductor multilevel boost converter (SIMBC) and the voltage lift switched inductor multilevel boost converter (VLSIMB). These converters combine the circuit of the traditional boost converter with a switched capacitor technique to generate a high voltage gain coupled with self-balancing outputs that maintain the same output voltage for all output levels. This chapter presented the theoretical analysis of the proposed converters in detail, along with their advantages, including transformerless topologies using a single low side switch, low voltage stress across semiconductor devices, continuous input current, modularity, and the creation of three self-balanced voltage levels at the output. Both converters utilize a pulse width modulation (PWM) technique to regulate voltage and produce multiple levels by adding more capacitors and diodes to the fundamental boost converter topology. The simulation and the experimental results obtained via the two built prototype circuits validate each power converter's theory and operational characteristics, demonstrating that the converters can achieve a voltage gain of up to ten times without a higher excessive duty cycle and the need for complex control algorithms. This chapter also discussed the performance analysis of the converters, including efficiency analysis and power loss analysis. It is shown that the VLSIMBC has the advantage of achieving higher voltage gain with a lower duty cycle and attains 1.1% higher efficiency than SIMBC.

Overall, this chapter provided a comprehensive study of the design, analysis, and performance evaluation of two transformerless DC-DC high voltage gain topologies, the SIMBC and VLSIMBC, demonstrating their effectiveness in a high step-up application.

Chapter 5: A Novel High Gain Z-source Multilevel Boost Converter Analysis and Design

5.1 INTRODUCTION

As more renewable energy sources are utilised, the demand for more efficient and reliable components and converters becomes increasingly essential. This is due to renewable energy sources generally suffering from low voltage output and high reliance on weather conditions. As a result, a step-up converter with a high voltage gain ratio is required to ensure that the output voltage can be increased to an adequate level for transmission and distribution.

One successful solution to achieving high voltage gains is a transformerless high step-up DC-DC multilevel boost converter, which comprises a boost stage with a subsequent voltage multiplier stage. This approach has been developed and presented in Chapters 3 and 4 to overcome the limits imposed by conventional topologies in high step-up DC-DC conversion.

Another critical development in power conversions is the use of Z-source impedance networks. This converter was first proposed in 2002, and it has been widely applied in inverters to provide buck-boost conversion capability and significantly increase reliability [93]. This makes the Z-Source Inverter (ZSI) highly suitable for renewable energy systems that convert low DC voltage to high AC output voltage, such as wave energy and photovoltaic systems.

The Z-source impedance network is applicable not only in inverters but also to the other three types of power converters, including DC-DC, AC-AC, and AC-DC converters [93]. Figure 5.1 displays the general arrangement of the Z-source converter [93]. By incorporating the impedance network into a DC-DC converter, an increased

high voltage gain can be obtained while reducing the inductor current ripple due to the lower operating duty cycle. As shown in Figure 5.2, the Z-source network comprises two inductors and capacitors coupled in an X configuration. This structure mitigates concerns like shoot-through and limited voltage gain that are common in conventional DC-DC converters [119]. However, the DC-DC converter with the Z-source network in [119] has a few issues, including high voltage stress across capacitors, a large inrush starting current, discrete input current, high switch voltage stress, excessive duty cycle utilisation for high voltage gain, and the absence of a common ground for input and output. These challenges increase semiconductor device costs, complexity, and voltage stress [94-96].

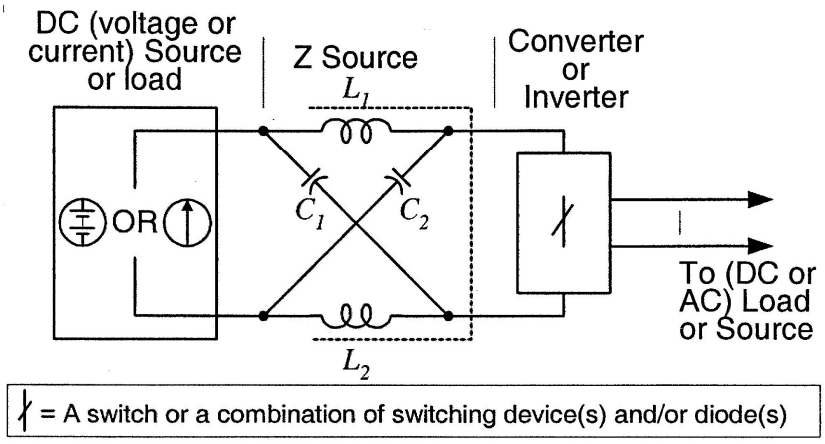

Figure 5.1: Z-source converter structure [28].

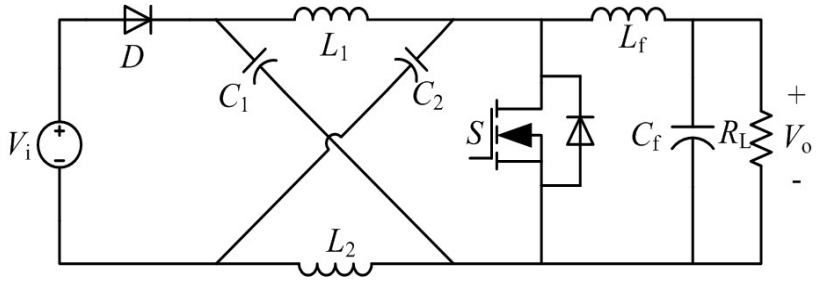

Figure 5.2: Conventional Z-source DC-DC converter [29].

This chapter proposes a new type of transformerless DC-DC boost converter called the Z-source multilevel boost converter (ZSMBC). The Z-source network is integrated into the multilevel boost converter to generate a high voltage gain with self-balancing outputs, maintaining the same output voltage where each level shares an equal portion of the total voltage output. The proposed topology allows for a high voltage conversion ratio with a smaller duty cycle in comparison to MBC, SIMBC and VLSIMBC while maintaining low voltage stress across the components and a common ground for input and output. This makes it suitable for use in a wide range of practical applications, such as in wave energy converters, DC microgrids, and solid-state transformer. The ZSMBC utilises pulse width modulation (PWM) to control the voltage, and it requires only a single switch, two inductors, (2N) diodes, and (2N+1) capacitors to obtain high voltage gain. The structure of the proposed high gain converter, circuit operation principle, steady-state characteristics, performance analysis and design consideration are discussed in detail. Furthermore, simulation and experimental results are provided, along with power loss analysis, to examine the operation of the converter.

5.2 PROPSED OVERVIEW

5.2.1 Circuit Topology Description

Figure 5.3 shows the circuit diagram of the proposed converter, which has a comparable structure to MBC, SIMBC, and VLSIMBC topologies. The proposed converter design is based on a modified Z-source network and voltage multiplier, allowing for high-voltage conversion while offering reduced voltage stress on the semiconductor components. The three-level DC-DC ZSMBC schematic in Figure 5.3 is a modified Z-source network integrated into a multilevel boost converter, which comprises 2 inductors, one switch, 6 diodes and 7 capacitors. The Z-source network

comprises two identical capacitors (C_a and C_b), two identical inductors (L_1 and L_2) and one diode (D_s), which are connected to form a distinct impedance network. The inductors and capacitors combine to create a second-order filter that suppresses voltage and current ripples more effectively than a first-order filter using only a single capacitor or inductor [120]. This network boosts the voltage at the input to the voltage multiplier stage while maintaining a common ground between the input and output [121].

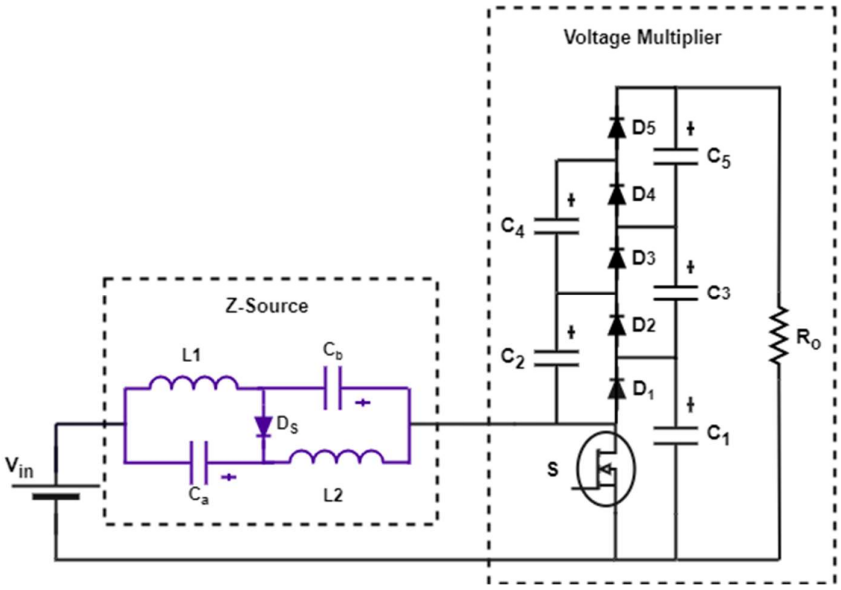

Figure 5.3: Circuit diagram of the three-level high gain DC-DC ZSMBC.

One of the significant advantages of the proposed converter topology is the ability to realise high voltages with reduced voltage stress on semiconductor devices. This is because the voltage across each converter level is $\frac{V_o}{3}$, where V_o is the output voltage. Compared to other high voltage topologies, such as conventional boost converters or conventional Z-source converters, the voltage stress on the components is significantly decreased. This means the converter can operate with lower voltage

tolerance components, resulting in less component stress and circuit losses. Consequently, this leads to higher efficiency, a significant advantage in applications where high efficiency is essential, such as in renewable energy systems.

5.2.2 Circuit Operational Principle

This section describes the steady-state operation of the proposed three-level ZSMBC, shown in Figure 5.3. The following assumptions have been made to study the converter's performance:

- Parasitic elements are ignored, and power devices are considered ideal.
- Since capacitors are large enough, their voltage is assumed as constant during one switching period.
- The converter operates in continuous conduction mode (CCM).

The Z-source DC-DC converter is comprised of two identical capacitors, $C_a = C_b = C$, two identical inductors, $L_1 = L_2 = L$ and an input diode D_s depicted in Figure 5.3. The symmetry of the component ensures that the inductor current, $i_{L1} = i_{L2} = i_L$ and voltage, $v_{L1} = v_{L2} = v_L$ are equal. Additionally, capacitor currents, $i_{Ca} = i_{Cb} = i_C$ and voltage, $v_{Ca} = v_{Cb} = v_C$ are also equal. On the other hand, the voltage multiplier contains a MOSFET active switch S, five diodes, D_1 to D_5 and five capacitors, C_1 to C_5. The operating principle of the three-level Z-source MBC can be divided into two modes: one when the switch is turned ON and another when the switch is turned OFF. The steady state waveforms of the proposed ZSMBC are shown in Figure 5.4.

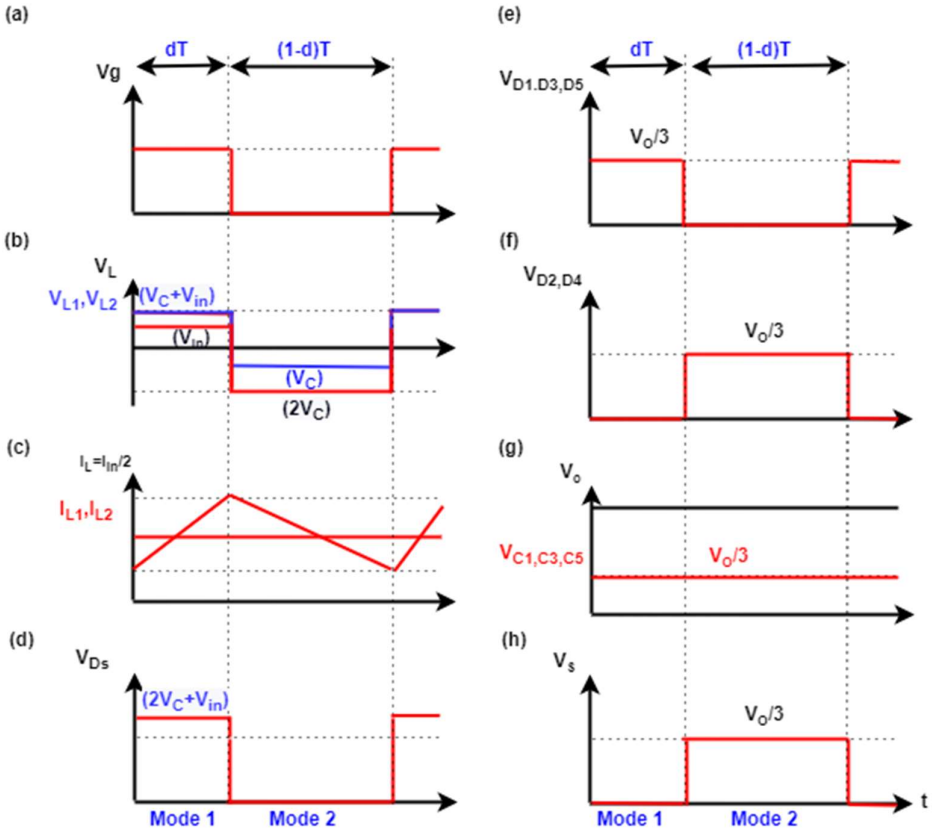

Figure 5.4: Main steady state waveforms of gate voltage, inductor voltage and current, input and output diodes voltages, output capacitors voltages and switch voltage for

The converter operates in CCM, and the following proceedings occur during the two modes:

In Mode 1, switch S is turned ON, and diodes D_s, D_1, D_3 and D_5 are turned OFF, as shown in Figure 5.5 (a). The inductor L_1 is charged by input voltage V_{in} and capacitor C_b. Similarly, the inductor L_2 is charged by input voltage V_{in} and capacitor C_a. As a result, the inductor current i_L increases linearly. Then, C_1 charges C_2 via the diode D_2 and the switch S while the voltage across capacitor C_2 is less than that across capacitor C_1. Simultaneously, C_1 and C_3 charge C_2 and C_4 through the diode D_4 and the switch S while the voltage across capacitors $C_2 + C_4$ is smaller than the voltage across $C_1 + C_3$, as shown in Figure 5.5 (a) [107].

In Mode 2, switch S is turned OFF and diode D_s, D_1, D_3 and D_5 are forward biased, as shown in Figure 5.5 (b). The capacitors C_a and C_b ae charged from inductors L_1 and L_2 , respectively. Then the inductor current i_L is decreasing linearly. As shown in Figure 5.5 (b), diode D_1 conducts, allowing the energy stored in the inductor to charge capacitor C_1 until its voltage is equal to the sum of the input voltage and the inductor voltage. After that, diode D_3 turns ON, enabling the input voltage, inductor L, input capacitor C and capacitor C_2 to charge capacitors C_1 and C_3. Once the voltage on capacitors $C_1 + C_3$ equals the sum of the input voltage, inductor voltage, input capacitor voltage and capacitor voltage C_2, diode D_3 switches OFF and diode D_5 conducts. Consequently, the inductor, input capacitor and capacitors C_2 and C_4 then charge capacitors C_1, C_3 and C_5 until the voltage equals the total of the voltage on the input voltage, inductor, and capacitors $C_2 + C_4$, as indicated in Figure 5.5 (b) [107].

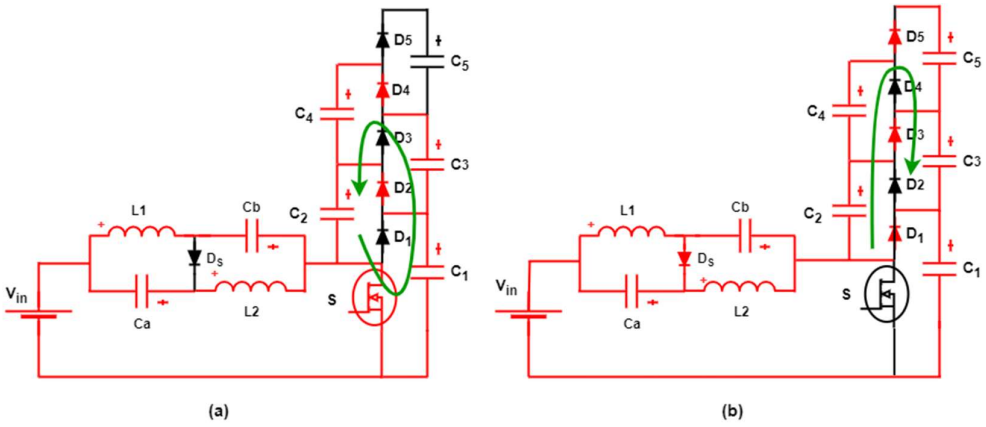

Figure 5.5: Operating modes of the three-level ZSMBC (a) S ON, (b) S OFF.

5.3 STEADY STATE ANALYSIS

5.3.1 Voltage Gain

This section presents the analysis of the voltage gain for the novel Z-source multilevel boost converter. The ZSMBC circuit transfers the input power to the output by charging and discharging the Z-source network and the switched-capacitor voltage multiplier. The capacitors in the circuit have a large capacitance, and the high switching frequency ensures that the voltage across the capacitor, v_C, can be assumed to be constant at V_C. The circuit operates in Mode 1, as displayed in Figure 5.4, with a time interval of dT. In this Mode, diodes D_2 and D_4 become forward-biased. Consequently, the Z-source impedance network is symmetrical, and so

$$V_{in} = V_L - V_C \tag{5.1}$$

Mode 2, as shown in Figure 5.5 (b), has a time interval of $(1 - d)\ T$. During this mode, diodes D_s, D_1, D_3 and D_5 are forward-biased, and the inductor supplies the stored energy to the load. This results in

$$V_{in} = V_L - V_C + V_{C1} \tag{5.2}$$

And

$$V_{C1} = V_{in} + 2V_C \tag{5.3}$$

where the V_{C1} is the voltage across the output capacitor C_1.

The average inductor voltage must be zero over a complete switching cycle and can be expressed as

$$V_L = d\ (V_{in} + V_C) + (1 - d)(V_{in} + V_C - V_{C1}) = 0 \tag{5.4}$$

The voltage across capacitor C_1 is the same as predicted for a conventional Z-source DC-DC converter topology. Therefore, in steady-state operation with identical output

capacitors, V_{Co}, the capacitor voltage can be expressed by combining equations 5.3 and 5.4 as follows:

$$V_{Co} = V_{C1} = V_{C3} = V_{C5} = \frac{1}{(1-2d)} V_{in} \quad 5.5$$

The output voltage of the three-level ZSMBC converter is the sum of the voltages across the output capacitors, which leads to this expression.

$$V_o = 3V_{Co} = \frac{3}{(1-2d)} V_{in} \quad 5.6$$

The proposed converter has two modes of operation, but it can also enter a transient mode, where the switch experiences higher voltage spikes, leading to increased power losses. To prevent this, snubber circuits can be utilised, as discussed in [122]. Furthermore, equation 5.6 shows that the proposed converter has a higher boost ability of $\frac{3}{(1-2d)}$ than other converters in the literature. However, from equation 5.6, it is essential to note that d should not exceed 0.5 to avoid the instability caused by inductor saturation and singularity issues.

Figure 5.6 displays a three-dimensional representation of the ideal voltage gain G, plotted as a function of the duty cycle *d* and the number levels N. The data indicate that increasing the number of levels results in a higher voltage gain. The duty cycle also increases with the voltage gain, and this relationship is typically employed to determine the desired voltage gain.

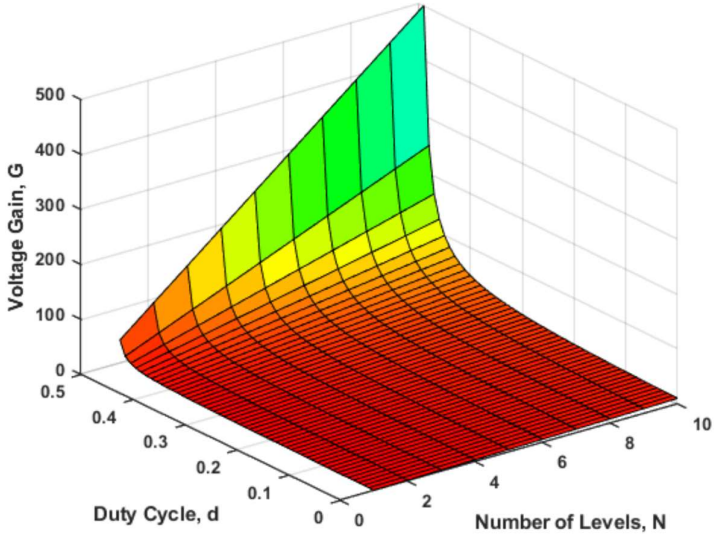

Figure 5.6: Ideal Voltage gain characteristic of the ZSMBC as a function of d and N values.

The average inductor current I_L is equal to the average source current I_{in} because the average current of the Z-source capacitor is zero within the switching period and the one-port impedance network is in series with the input voltage source. Therefore, the average inductor current, I_L, can be determined from the knowledge of the output current and the input and output voltages. Assuming that the converter operates at 100% efficiency, the following equation can be derived.

$$I_L = \frac{{V_o}^2}{V_{in} R_o} \tag{5.7}$$

Using equations 5.6 and 5.7, the inductor current, I_L, in the three-level ZSMBC topology shown in Figure 5.3 can be expressed as:

$$I_L = \frac{3V_o}{(1-2d)R_o} \tag{5.8}$$

In a practical circuit, the equivalent series resistance of the inductor, $R_{ESR,L}$ must be taken into account. As a result, the voltage gain in realistic circuit can be expressed as:

$$\frac{V_o}{V_{in}} = \frac{3(1-2d)R_o}{(1-2d)^2 R_o + 9R_{ESR,L}} \tag{5.9}$$

Equation 5.9 indicates that the presence of the inductor $R_{ESR,L}$ decreases the voltage gain of the ZSMBC. Consequently, increasing the duty cycle is required to achieve the desired output voltage in a practical converter.

Figure 5.7 shows the curve of voltage gains of a three-level ZSMBC as a function of the duty cycle, demonstrating the impact of the inductor's $R_{ESR,L}$. The data reveal that the inductor's ESR degrades the voltage gain and necessitates an increase in the duty cycle to achieve the desired voltage conversion ratio. For a gain of ten, the ZSMBC must operate at 0.38 with ESR equals 1 Ω. On the other hand, the ZSMBC's duty cycle with an ESR of 0.028 Ω is 0.35. Furthermore, it can be observed that the difference will be significantly higher when the ZSMBC with the duty cycle in excess of 45%.

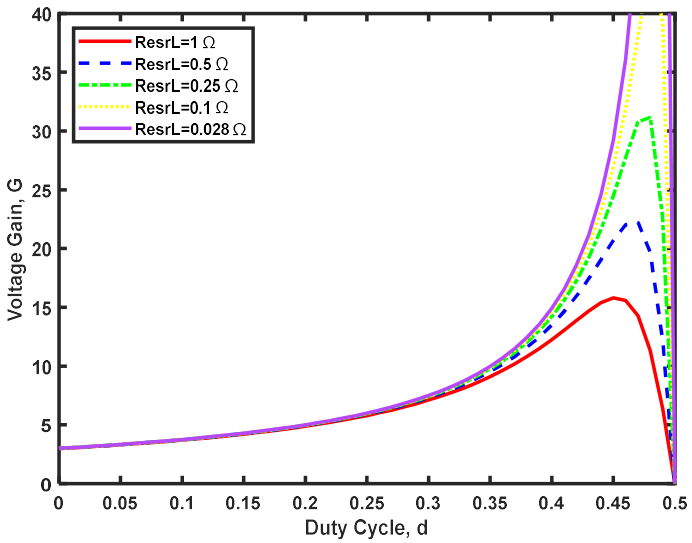

Figure 5.7: Voltage gain characteristic of the ZSMBC as a function of d for different values of $R_{ESR,L}$.

5.3.2 Power Semiconductor Voltage Stress

Figure 5.4 (h) shows the voltage stress experienced by the switch, V_s, in the proposed ZSMBC. As can be observed in the figure, the voltage across the switch is lower than the output voltage, unlike the behaviour of a conventional Z-source boost converter, where the voltage across the switch is equal to the output voltage. This reduction in voltage stress on the switch has the added advantage of allowing for the use of lower-rated semiconductor devices, ultimately reducing the overall cost of the circuit. Furthermore, the data in Figure 5.5 (b) confirm that the voltage on the switch, V_S, in the proposed converter is equal to the voltage across capacitor 1, V_{C1}. The voltage stress across the switch in the three-level ZSMBC can be defined as:

$$V_S = \frac{V_O}{3} = \frac{V_{in}}{(1-2d)} \qquad 5.10$$

The normalised voltage stress across the switch to the output voltage $\left(\frac{V_S}{V_O}\right)$ of the ZSMBC is plotted as a function of the duty cycle using equation 5.10, as shown in Figure 5.8. The data indicate that, as the duty cycle increases, the voltage stress on the switch also increases. Furthermore, the voltage across the switch is only one-third of the output voltage because each stage of the three-level ZSMBC conveys an equal portion of the total output voltage.

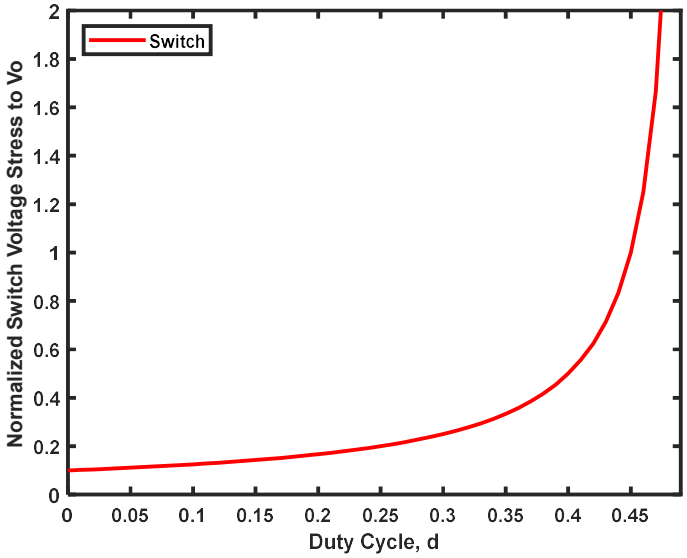

Figure 5.8: Normalized voltage stress of ZSMBC as a function of *d*.

The voltage stress across the input diode of Z-source network and voltage multiplier diodes in the ZSMBC, represented by $V_{ds}, V_{d1}, V_{d2}, V_{d3}, V_{d4}$ and V_{d5}, are equal to the voltage across the switch. The stress increased proportionally with the duty cycle. Equation 5.10 emphasise that this stress is equal to the switch voltage and consistently lower than the output voltage.

Furthermore, for the three-level ZSMBC circuit, assuming that all capacitors are sufficiently large and have equal capacitance, they should ideally maintain similar voltages during operation. As illustrated in Figure 5.3 and defined by equations 5.10, the voltage stress experienced by each capacitor of the voltage multiplier during operation is similar to the voltage stress across the switch. This voltage stress depends on the duty cycle, input voltage, and output voltage of the converter. In contrast, the voltage stress on the Z-source impedance network capacitor, V_C, can be expressed as

$$V_C = \frac{dV_{in}}{(1-2d)} \qquad 5.11$$

5.4 DESIGN CONSIDERATION

The component design of the proposed three-level ZSMBC is informed by the maximum permissible current and voltage stresses. Once the current and voltage stresses are known, the design principle of the elements can be analysed in detail. This section presents a detailed analysis of the design principles of these components.

5.4.1 Inductor Design

The equation provided can be used to determine the inductor voltage.

$$V_L = L\frac{\Delta \mathrm{i}_L}{dt} \tag{5.12}$$

where $\Delta \mathrm{i}_L$ is inductor current ripple.

Considering the inductor in operating Mode 1, equation 5.12 can be expressed as

$$\Delta \mathrm{i}_L = \frac{1}{L}\int_0^{dT} V_L\, dt \tag{5.13}$$

It can even be simplified as follows, with the assumption of ideal inductor:

$$\Delta \mathrm{i}_L = \frac{dV_L}{Lf} \tag{5.14}$$

Equation 5.1 can be substituted into equation 5.14 and simplified to obtain

$$\Delta \mathrm{i}_L = \frac{(1-d)DV_{in}}{(1-2d)Lf} \tag{5.15}$$

Limiting the current ripple in the inductor is crucial to avoid large current stresses on the switch and diodes. The following equation can define the inductor current ripple.

$$\Delta \mathrm{i}_L = Y_L I_L \tag{5.16}$$

where Y_L is the percentage inductor current ripple and generally in the range between 15 and 30% [96].

According to equations 5.8, 5.15 and 5.16, the inductance L can be expressed as

$$L_{min} \geq \frac{d(1-d)(1-2d)}{Y_L f} \tag{5.17}$$

5.4.2 Capacitor Design

The equation provided can be used to define the capacitor current.

$$I_C = C\frac{\Delta \mathrm{v}_C}{dt} \tag{5.18}$$

where $\Delta \mathrm{v}_C$ is capacitor voltage ripple.

Considering the capacitor in operating Mode 1, equation 5.18 can be expressed as

$$\Delta \mathrm{v}_C = \frac{1}{C}\int_0^{dT} I_C\, dt \tag{5.19}$$

It can be simplified as follows, assuming that the capacitor is ideal:

$$\Delta \mathrm{v}_C = \frac{dI_C}{Cf} \tag{5.20}$$

During the switch-ON period, the capacitor current I_C equals the inductor current I_L. Therefore, substituting the value of I_L into equation 5.20 will result in the expression for the voltage ripple of the one-port impedance network capacitor.

$$\Delta \mathrm{v}_C = \frac{dI_L}{Cf} \tag{5.21}$$

A larger voltage ripple in the capacitor reduces its lifetime and necessitates the utilisation of a higher capacitance value [96]. Thus, it is essential to minimise this value and the capacitor voltage ripple can be expressed as

$$\Delta \mathrm{v}_C = Y_C V_C \tag{5.22}$$

where Y_C is the percentage capacitor voltage ripple.

According to equations 5.10, 5.21 and 5.22, the capacitance C can be expressed as

$$C = \frac{(1-2d)I_L}{X_C f V_{in}} \tag{5.23}$$

Equation 5.23 can be used to determine the Z-source impedance capacitors C_a and C_b. The capacitance of the voltage multiplier capacitors is the same as the capacitance of the MBC presented in Chapter 3 and defined in equation 3.20.

5.4.3 Selection of Power Devices

Selecting switches and diodes depends on their permissible maximum voltage and current stresses, which are discussed in section 5.3 for the proposed ZSMBC. The voltage stress on the switches is one-third of the output voltage, while the current stress varies with the duty cycle. Accordingly, the output voltage and current values must be considered when determining the switches and diodes' ratings.

5.4.4 Proposed CCM Converter Operation Conditions and the Permitted Load Range

This section presents the requirements for CCM operation and load range comparison between the proposed ZSMBC converter and a conventional Z-source DC-DC converter. In CCM operation, the inductor current must not reach zero in each switching cycle, and the proposed converter must fulfil the following conditions to operate continuously throughout the switching period.

$$I_L - \frac{1}{2}\Delta i_L \geq 0 \tag{5.24}$$

By substituting equations 5.8, 5.15 and 5.24, the load range during CCM operation can be expressed as follows:

$$R_o \leq \frac{18Lf}{d(1-d)(1-2d)} \tag{5.25}$$

It can be observed from equation 5.25 that R_o is directly proportional to L. Hence, increasing the value of L raises the load capacity range of the converter R_o. In addition, the proposed converter must meet the following condition to ensure operation in CCM.

$$R_o \leq R_{o,max} \tag{5.26}$$

where $R_{o,max}$ is the maximum load.

The comparison of the CCM load ranges of the proposed converter and the traditional Z-source DC-DC converter in [94], with a switching frequency of 50 kHz, is shown in Figure 5.9. It can be observed that the proposed converter has a significantly wider CCM load range compared to the traditional Z-source DC-DC converter with the same inductance in the impedance network.

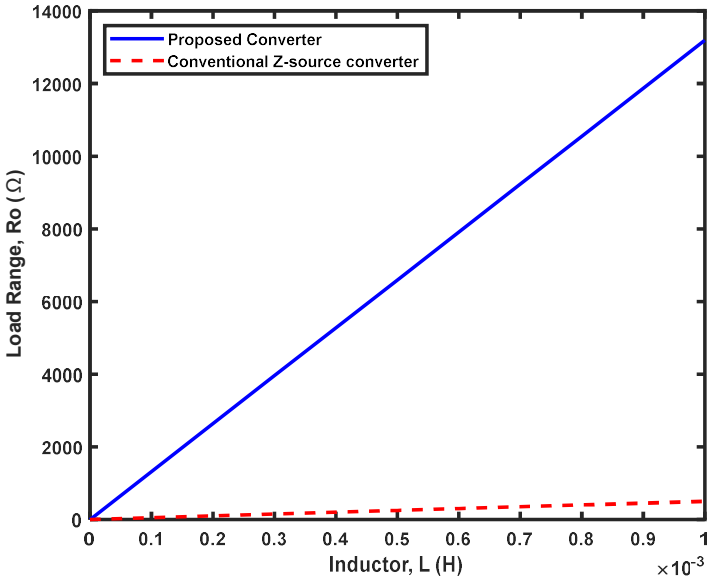

Figure 5.9: CCM load range for the proposed converter and conventional Z-source DC-DC converter.

5.5 SIMULATION AND EXPERIMENTAL VALIDATION

This section presents a comprehensive analysis of the proposed ZSMBC topology simulation and experimental verification, with an overview of the simulation and experimental setups provided. A detailed description of the simulation and practical results follows, analyzing the converter's performance. The three-level ZSMBC was designed with high voltage gain and specific features to verify its

operating characteristics and enable the connection of wave energy converters to an MVDC collection network. In addition, the performance of the topology is validated through simulations and prototype results.

5.5.1 High Gain Proposed Prototype

To verify the boosting capability and perform a theoretical analysis of the proposed converter, an experimental prototype was built with all power converter components, including power semiconductor devices, Z-source impedance diode, capacitors and inductors, and output capacitors, placed on a single board. The feasibility of the proposed three-level ZSMBC was tested by developing a prototype in the laboratory, with the circuit design and experimental setup shown in Figure 5.10.

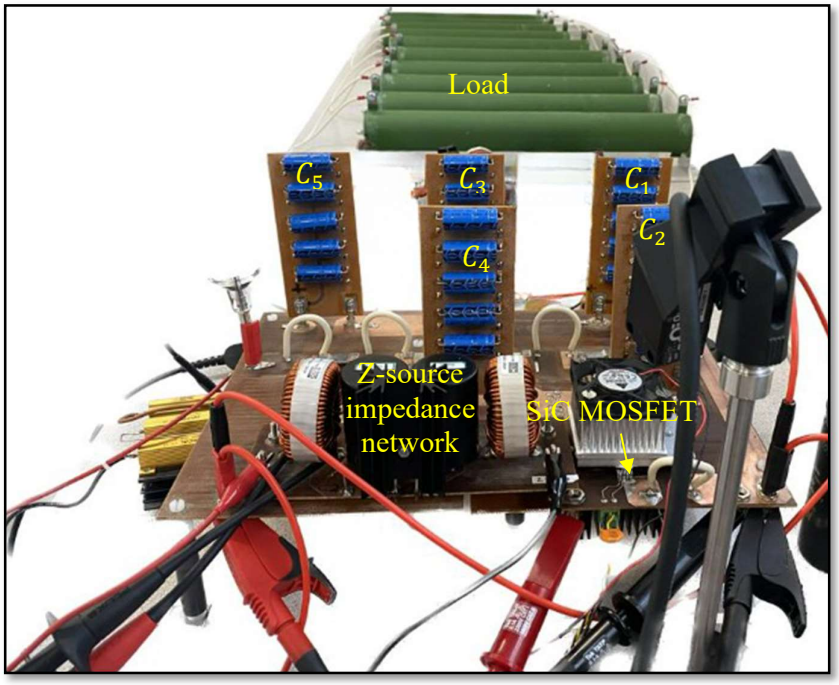

Figure 5.10: Three-level ZSMBC experimental prototype.

The hardware prototype of the proposed converter was constructed using a commercial Silicon Carbide MOSFET (GeneSiC Semiconductor part number G2R120MT33J) as the power switch and Silicon Carbide Schottky Diodes (GeneSiC

Semiconductor part number GB05MPS33-263) in the circuit. The blocking voltage of the SiC MOSFET is 3.3 kV with on-state resistance $(R_{DS(ON)})$ of 0.12 Ω and the blocking voltage of all diodes was 3.3 kV with a forward voltage drop of 3 V. Figure 5.10 displays the main circuit of the proposed three-level ZSMBC and the experimental prototype, validating the theoretical analysis and simulation results.

5.5.2 Simulation and Measured Experimental Waveforms

Theoretical analysis of the proposed converter was validated by developing a simulation model using LTSpice. The simulation parameters, including parasitic values, were selected based on the analysis presented in sections 5.3 and 5.4. The simulation and experimental prototype used the same parameters and component ratings listed in Table 5-1.

Table 5-1. Design Specification for Three-Level ZSMBC.

Parameter	Symbol	Rating
Input Voltage	V_{in}	300 V
Output Voltage	V_o	3 kV
Output Load	R_o	10 kΩ
Switching Frequency	f	50 kHz
Z-source inductors	L_1 and L_2	1 mH, 26 A
Z-source capacitors	C_a and C_b	13.5μF, 1.2 kV
Capacitors	$C_1 - C_5$	1μF, 4.5 kV
Switch	S	G2R120MT33J
Diodes	D_s and $D_1 - D_5$	GB05MPS33-263

The proposed three-level ZSMBC has simulated characteristics that enable it to increase the DC input voltage from 300 V to 3 kV. However, to avoid excessive voltage stress and achieve a gain factor of 10, the duty cycle was limited to 37% to ensure an adequate portion of the operating period when the switch was turned OFF.

Further analysis led to the investigation of a three-level ZSMBC, which provided an output voltage of 3 kV, an output power of 1.2 kW and a duty cycle of 37%.

To attain an output voltage of 3 kV with a gain of 10 using a Z-source network impedance along with a voltage multiplier, a duty cycle of d = 0.35 was required based on equation 5.6. However, non-ideal conditions in a practical circuit necessitate a duty cycle of d = 0.37 to achieve the intended gain of 10. The proposed converter's simulation and experimental waveforms operating at 50 kHz are depicted in Figures 5.11-5.17. The experimental waveforms corresponded nicely with those obtained from LTSPICE simulations.

The input voltage and output voltage waveforms are shown in Figure 5.11. Given a specified duty cycle of d = 0.36, the simulation values of the proposed converter's input and output voltage are 300 V and 3025 V, respectively. Correspondingly, the experimental input and output voltage, with a duty cycle of d = 0.37, is 304 V and 3050 V, respectively, yielding a gain factor of 10. As a result, the experimental results are consistent with the simulation results and theoretical analysis. Therefore, the simulation and experimental findings confirm the ability of the proposed three-level ZSMBC to achieve high voltage gain and demonstrate that the equations presented in sections 5.3 and 5.4 can be used to calculate the voltage gain. In addition, the data indicate that the experimental waveforms exhibit switching transients not observed in the simulation results. These transients arise from parasitic capacitances and inductances in the circuit and appear as input-voltage transients during switch turn-on and turn-off.

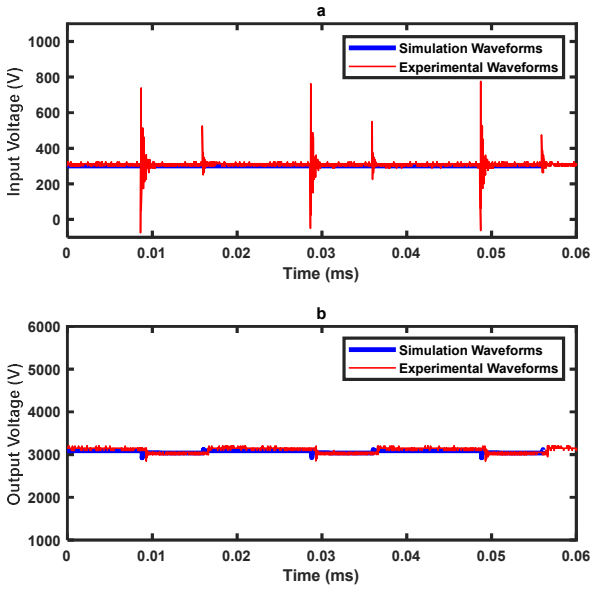

Figure 5.11: Input and output voltage waveforms of the three-level ZSMBC.

Figure 5.12 presents the inductor current and output current variations for an output voltage of 3.05 kV and a load current of 0.356 A. The data in this figure indicate that the inductor current I_L is continuous, confirming CCM operation. The measured average inductor current is 4 A, which aligns with the simulated value of 3.96 A.

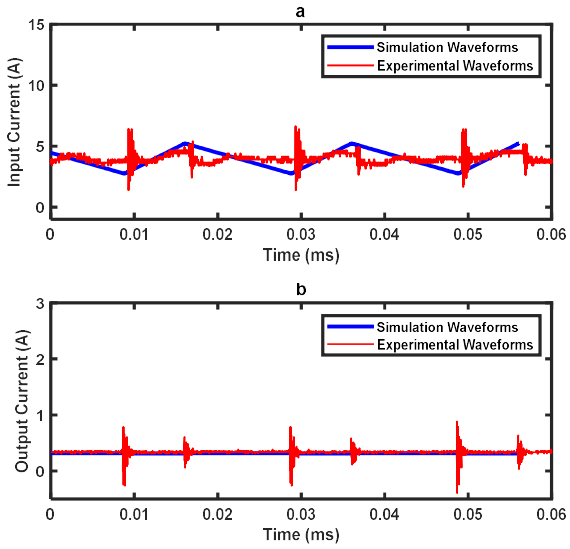

Figure 5.12: Input and output current waveforms of the three-level ZSMBC.

Figure 5.13 shows data on the voltage across the Z-source inductors V_{L1} and V_{L2}, as well as the overall input inductor V_L. The experimental values for both V_{L1} and V_{L2} are 712 V and -375 V when the switch is ON and OFF, respectively. In contrast, the simulated values for V_{L1} and V_{L2} are 687 V when the switch is ON and - 389 V when the switch is OFF. The experimental value for V_L is 300 V when the switch is ON and -800 V when the switch is OFF, whereas the simulated values are 300 V and -778 V for ON and OFF switch states, respectively. These results verify the performance of the proposed converter, as they indicate the agreement between the experimental and simulated values.

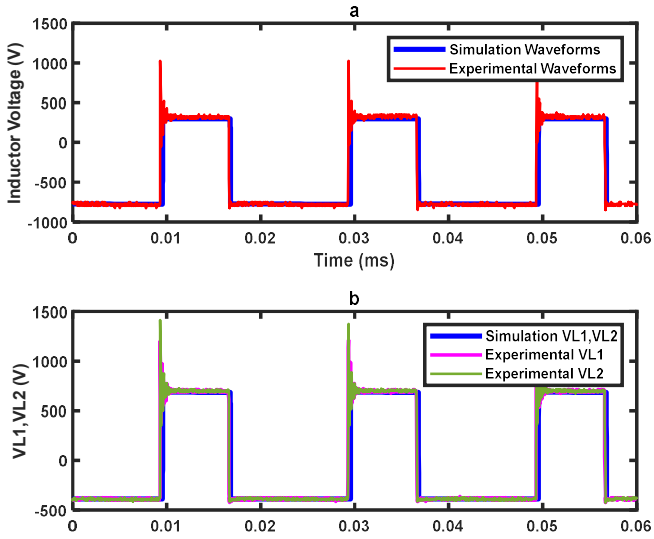

Figure 5.13: Voltage across L_1, L_2 and the effective inductor L for the ZSMBC.

Figure 5.14 displays data on the voltage stress across the Z-source diode D_s and capacitors V_{ca} and V_{cb}. During discharging, the diode D_s is reverse biased, and its experimental voltage value is 1050 V. This value is in close agreement with the simulation and theoretical estimation. Besides, the experimental voltage value of capacitors V_{ca} and V_{cb} are 400 V, which matches the results obtained from simulation and analytical calculations.

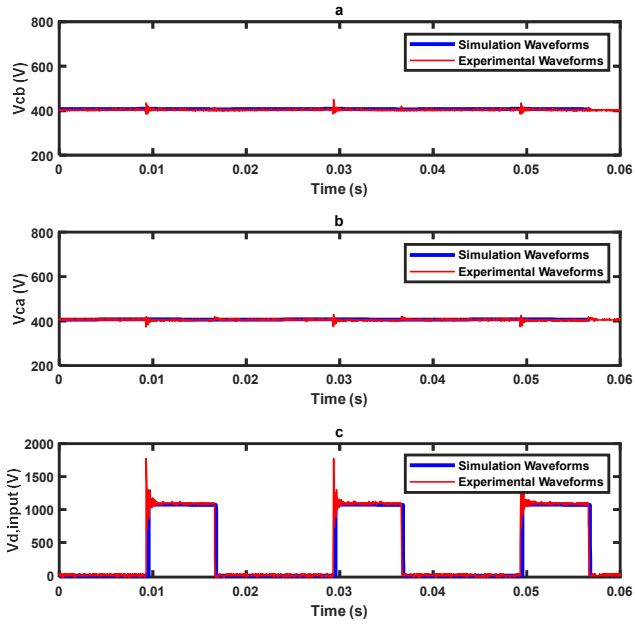

Figure 5.14: Voltage across D_S, V_{Ca} and V_{Cb} for the ZSMBC.

The drain-source voltage across the switch with its corresponding drain-source current for the proposed three-level ZSMBC is shown in Figure 5.15. The proposed converter has a significant advantage over traditional Z-source converters in reducing the voltage stress on the switch. The maximum drain-source voltage across the switch is 1.1 kV when the output voltage is 3 kV, according to the data in Figure 5.15, indicating that the switch is subjected to voltage stress, which is only one-third of the output voltage. This reduced voltage stress enables lower-rated power devices to be used while minimise conduction losses. The experimental findings closely match the simulation results. These results are consistent with the analysis presented in equation 5.10, which predicts a maximum drain-source voltage across the switch of 1 kV when the output voltage is 3 kV. In contrast, the experimental and simulated switching voltages of 1.1 kV and 1.05 kV, respectively, are close to the predicted value. Similarly, the measured drain-source current from the experiment and simulation nearly matches.

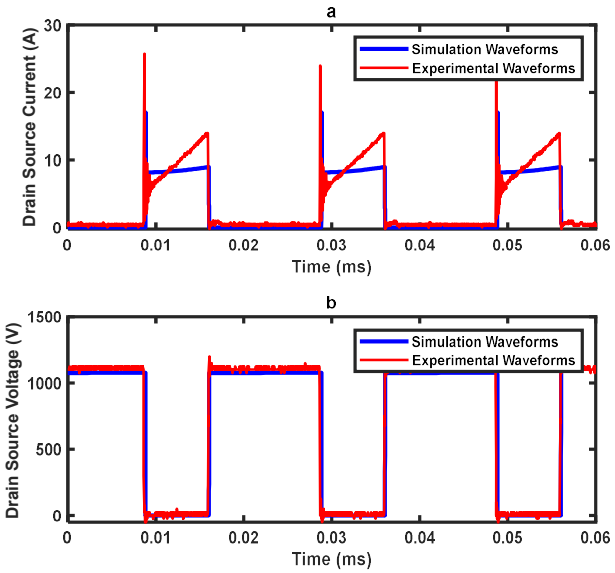

Figure 5.15: Drain-source voltage and current across the switch of the ZSMBC.

The data in Figure 5.16 indicate that the voltages across the three output capacitors, C_1, C_3 and C_5 are balanced. The slight variation in voltage can be accounted for by the forward voltage drop across the diodes, losses in parasitic components, and equivalent series resistance of the capacitors used. In a simulation using ideal capacitors, C_1 and C_3 have a simulation voltage difference of 7 V, whereas C_3 and C_5 have a difference of 2 V. Capacitors C_1, C_3 and C_5 have a measured voltage of 1050 V, 1005 V, and 995 V, respectively. Consequently, the output voltage of the proposed converter is the sum of individual capacitor voltages, $V_{C1} + V_{C3} + V_{C5}$. As a result, all the output capacitors maintain nearly equivalent voltage levels, resulting in voltage balance across all capacitors, as equation 5.5 predicted. In addition, it can be noticed that the experimental results of the output capacitors match well with the simulation results.

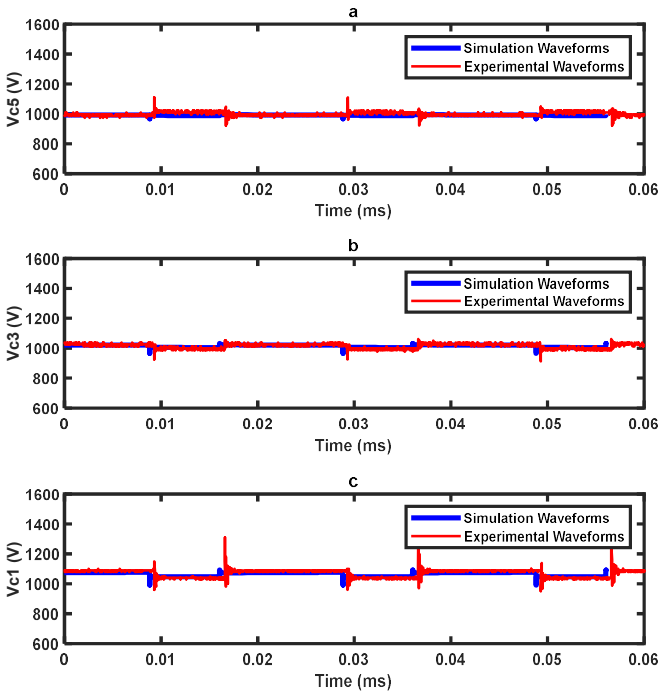

Figure 5.16: Voltage across the output capacitors C_1, C_3 and C_5 of the ZSMBC.

The data in Figure 5.17 display two vital parts of the proposed three-level ZSMBC operational principle. The data verify that when the switch is ON $(0.009 \leq T < 0.016 \text{ ms})$, diodes D_2 and D_4 are forward-biased. Accordingly, at this stage, the voltage across the switch is zero, and the voltages across diodes D_2 and D_4 are zero. However, when the switch is OFF $(0.016 \leq T \leq 0.029 \text{ ms})$, diodes D_s, D_1, D_3 and D_5 are forward-biased, and they allow the current to flow in the circuit; at this stage, the voltage across the switch is 1.1 kV, and the voltages across diodes D_s, D_1, D_3 and D_5 are zero. The data in Figure 5.17 highlight that the proposed ZSMBC operates as intended, switching between diodes dependent on the switch on/off state.

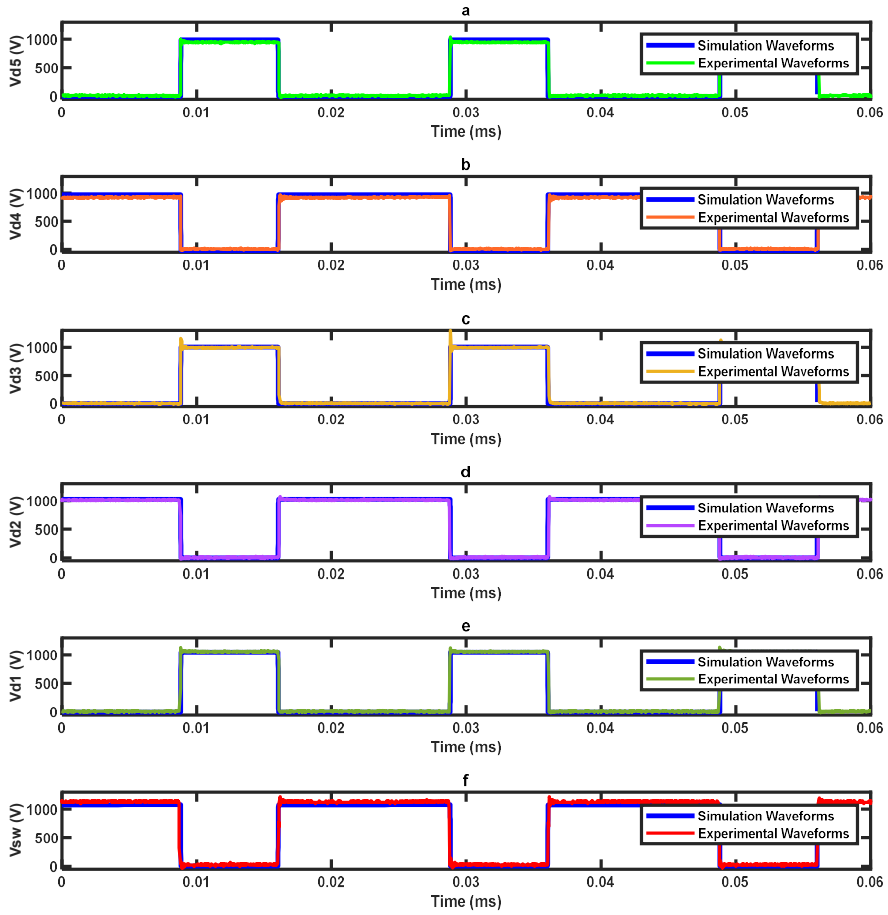

Figure 5.17: Drain-source voltage across the switch with voltage across D_1, D_2, D_3, D_4, D_5 of the ZSMBC.

5.6 POWER LOSS ANALYSIS AND EFFICIENCY MEASUREMENT

To estimate the efficiency of the proposed ZSMBC, the losses incurred by each component must be identified and evaluated. The losses mainly determine the efficiency due to the conduction and parasitic elements during the operation of the converter. The internal characteristics of each device and component in the converter also affect the efficiency. This section discusses the power losses associated with each parameter to provide a comprehensive evaluation of the efficiency of the proposed ZSMBC.

5.6.1 Power Losses in Inductor

The inductor power loss comprises core loss and copper loss, also known as conduction loss. The core loss is typically negligible. However, the average current of the inductor has a significant impact on the copper loss. Thus, the power loss can be computed as $P_L = I_L^2 R_{ESR,L}$, where $R_{ESR,L}$ is the equivalent series resistance of the inductor. Hence, the inductor copper loss P_L for a three-level ZSMBC with two identical inductors can be expressed as a function of the inductor current and internal resistance. The power loss analysis of the proposed ZSMBC presented in this chapter follows the same analyses as in the previous chapters.

$$P_L = 2\left(\left(\frac{3V_o}{(1-2d)R_o}\right)^2 R_{ESR,L}\right) \tag{5.27}$$

5.6.2 Power Losses in Capacitor

The power loss in a capacitor is determined based on the RMS current passing via the capacitor and its effective series resistance ($R_{ESR,C}$)Thus, the power loss in the capacitors for the proposed ZSMBC can be expressed as

$$P_C = I_{Ca}^2 R_{ESR,Ca} + I_{Cb}^2 R_{ESR,Cb} + I_{C1}^2 R_{ESR,C1} + I_{C2}^2 R_{ESR,C2} + I_{C3}^2 R_{ESR,C3} + I_{C4}^2 R_{ESR,C4} + I_{C5}^2 R_{ESR,C5} \tag{5.28}$$

5.6.3 Power Losses in Switch

The switch's power loss comprises two parts: conduction loss and switching loss. The value of conduction loss is defined by the switch's drain-source current and turn-on resistance ($R_{DS,(ON)}$). The following equation can determine the estimation of power conduction loss of the proposed ZSMBC:

$$P_{SC} = \left(\frac{3V_o}{(1-2d)R_o}\right)^2 R_{DS,(ON)} \tag{5.29}$$

Furthermore, switching power loss can be significantly influenced by the voltage across the switch, peak current, turn-on (t_{ON}) and turn-off (t_{OFF}) periods, and switching frequency. Consequently, the switching loss of the switches can be stated as follows:

$$P_{SW} = \frac{1}{2} I_{L,avg} V_s (t_{OFF} + t_{ON}) f_{sw} + \frac{1}{2} f_s C_{oss} V_S^2 \quad 5.30$$

where C_{oss} is output capacitance.

Total loss due to switch can be estimated as:

$$P_{S,total} = P_{SC} + P_{SW} \quad 5.31$$

5.6.4 Power Losses in Diodes

The diode power loss comprises conduction loss due to forward voltage drop (V_F) and internal resistance (r_f). The loss due to forward voltage drop is obtained using the average current, whereas the RMS current of the diodes determines the conduction loss. The average diode current $I_{D,avg}$ can be specified as

$$P_{D,avg} = \frac{1}{T} \int_0^T i_D(t) dt \quad 5.32$$

Moreover,

$$\begin{aligned} i_D &= 0, for\ (0 \le t \le dT) \\ i_D &= I_D, for\ (\ dT \le t \le T) \end{aligned} \quad 5.33$$

Substituting equation 5.33 into equation 5.32, it can be expressed as

$$P_{D,avg} = \frac{1}{T} \int_{dT}^T I_D(t) dt \quad 5.34$$

Considering that the diode is forward-biased when the switch is turned off for period $(1 - d)T$.

Hence, total loss in diodes for the proposed three-level ZSMBC will be :

$$P_D = \sum_{i=1}^{6} I_{D,avg} V_F + \sum_{i=1}^{6} I_{D,rms}^2 \, r_f \quad (5.35)$$

Then, the total power loss in the proposed converter is given as

$$P_{Losses} = P_L + P_C + P_{S,total} + P_D \quad (5.36)$$

5.6.5 Computing the Efficiency

The Efficiency (η) of the proposed ZSMBC can be expressed as

$$\eta = \left(\frac{P_o}{P_o + P_{Losses}} \right) \quad (5.37)$$

The data presented in Figure 5.18 outlines the efficiency of the proposed three-level ZSMBC topology through simulations and experiments. The efficiency was evaluated for output power levels varying between 1.2 kW and 1.6 kW. The results demonstrate that the ZSMBC performed sufficiently, achieving a maximum measured efficiency of 93.58% at an output power of 1.3 kW. The simulated efficiency at the same output power was slightly higher, 95.93%. However, it is worth noting that the simulation did not account for core losses in the inductor or the contribution of parasitic capacitances and inductances in the circuit, which can induce switching transients in the input and output voltages, as shown in Figure 5.11.

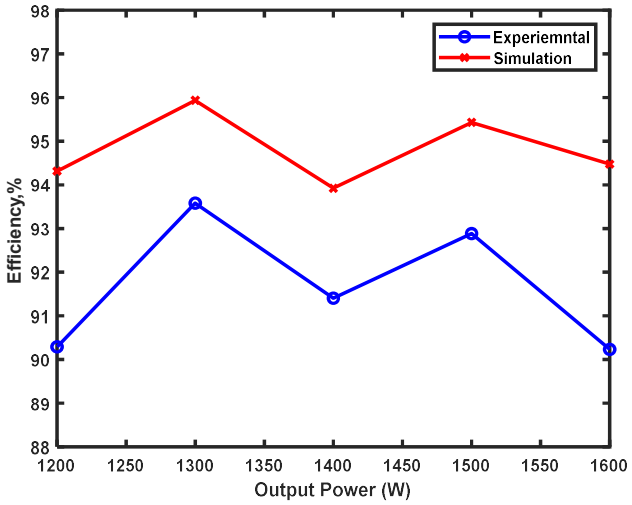

Figure 5.18: Simulation and practical efficiency with respect to the output power of the three-level ZSMBC.

Furthermore, the data in Figure 5.19 illustrate the distribution of losses among the different components, including inductors, capacitors, switch and diodes. The capacitors account for the highest losses at 64% due to their high ESR, which generates power dissipation and heating, whereas the losses assigned to other elements are much lower. Thus, selecting capacitors with a low ESR can minimize losses. Additionally, the MOSFETs employed in the converter can also contribute to significant losses. Therefore, by optimizing the converter design and carefully selecting the components, losses can be minimized, and efficiency can be improved.

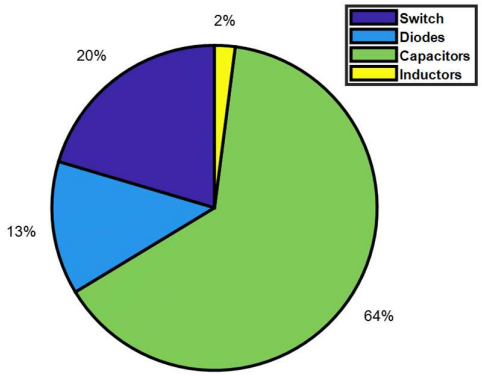

Figure 5.19: Percentage distribution of losses of the three-level ZSMBC.

5.7 SUMMARY

A novel high-gain transformerless DC-DC Z-source multilevel boost converter ZSMBC is proposed and verified using a 3 kV prototype. Integrating a Z-source impedance network into a multilevel boost converter is an effective solution for realising a high conversion ratio with a low duty cycle compared with MBC, SIMBC, and VLSIMBC presented in previous chapters, as well as other suggested converters depicted in the literature. This chapter clarifies the theoretical analysis, operating principle, design considerations, and simulation and experimental results of a new non-isolated ZSMBC based on integrating the Z-source and voltage multiplier approach. The proposed ZSMBC topology has remarkable achievements and offers significant advantages, such as reduced device voltage stress and higher output voltages without requiring high-voltage switches. Thus, the proposed converter provides a low voltage stress on the switch, one-third of the output voltage, significantly lower than the output voltage. Unlike many power converters in the literature, this distinctive characteristic indicates that lower-rated devices can minimise conduction loss.

The circuit is designed for applications requiring high voltage gain, and their demand is progressively growing. The experimental results acquired from the 3 kV prototype circuit verify the theory and operational characteristics of the ZSMBC topology and the simulation findings. Furthermore, these results indicate that the converter has attained a voltage gain of ten with three levels (N = 3). The assessment was performed using simulations and experiments. The practical and simulated results were in agreement with the equations presented in sections 5.3 and 5.4, with switching transients observed in the experimental results owing to the parasitic capacitances and inductances in the circuit. The results also demonstrate that the inductor current is

continuous, indicating that the converter operates in the continuous conduction mode (CCM).

Moreover, a voltage balance was attained across all output capacitors. Taking into consideration that the voltage transients visible in the output capacitors are associated with the turn-on and turn-off transients of the MOSFET and parasitic components. In addition, the experimental data still showed high efficiency, varying between 90.4% and 93.58% for the load range between 1.2 and 1.6 kW. This implies that the proposed three-level ZSMBC can operate effectively at various loads within this range without significantly affecting the overall efficiency. This is a valuable finding since it enables flexibility in the converter and optimisation following specific demands such as size, cost, and application. Finally, these findings provide valuable data on the performance of the proposed three-level ZSMBC, and these observations demonstrate the potential of the proposed converter for implementation in wave energy applications.

Chapter 6: Conclusion and Future Work

6.1 PROPOSED TOPOLOGIES COMPARISON

In order to comprehensively distinguish the capabilities of the high gain transformerless topologies discussed in Chapters 3, 4 and 5 and demonstrate the advantages of one topology over the other, performance evaluation and comparison are conducted between the three-level MBC, SIMBC, VLSIMC, ZSMBC topologies. A comparison between these topologies is shown in Table 6.1.

Table 6-1. Comparison of the Three-Level MBC, SIMBC, VLSIMBC and ZSMBC Topologies.

Topology	MBC	SIMBC	VLSIMBC	ZSMBC
Number of switches	1	1	1	1
Number of Diodes	5	8	7	6
Number of Inductors	1	2	2	2
Number of Capacitors	5	5	6	7
Duty Cycle	0.71	0.54	0.41	0.35
Voltage Gain	$\frac{3}{(1-d)}$	$\frac{3(1+d)}{(1-d)}$	$\frac{6}{(1-d)}$	$\frac{3}{(1-2d)}$
Switch Voltage Stress (V_s)	$\frac{1}{(1-d)}$	$\frac{(1+d)}{(1-d)}$	$\frac{2}{(1-d)}$	$\frac{1}{(1-2d)}$
Normalize Voltage Stress $\left(\frac{V_s}{V_o}\right)$	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{1}{3}$
Behavior of Input Current	Continuous	Continuous	Continuous	Continuous

In addition, the theoretical voltage gain of the proposed converters is compared as a function of the duty cycle, as shown in Figure 6.1. Moreover, Figure 6.2 illustrates the normalised voltage stress across the switch of the three-level converters with respect to the duty cycle. The data in Figure 6.1 helps to select a proper duty cycle that

achieves desired output voltage. To achieve a gain of 10, MBC needs to be run at 0.71 duty cycle, whereas the duty cycle of SIMBC must be 0.54. VLSIMBC and ZSMBC need to be operated at d = 0.41 and d=0.35, respectively to achieve a gain of 10. Generally speaking, the proposed converters have higher voltage gain, and this advantage increases as the duty cycle of the switch increases. For instant, for d=0.45, the voltage gains of MBC, SIMBC VLSIMBC and ZSMBC are 5, 8, 10 and 30, respectively. It can be concluded that ZSMBC can achieve a high voltage gain with a lower duty cycle and VLSIMBC can provide a double voltage gain compared to MBC at the same duty cycle. Also, it can be noticed that VLSIMBC can achieve high voltage gain with a low duty cycle, while MBC can realise high voltage gain with a slightly high duty cycle. SIMBC can reach high voltage gain without excessive duty cycle. Therefore, the proposed converters are more suitable than other high voltage gain converters of the boost coefficient.

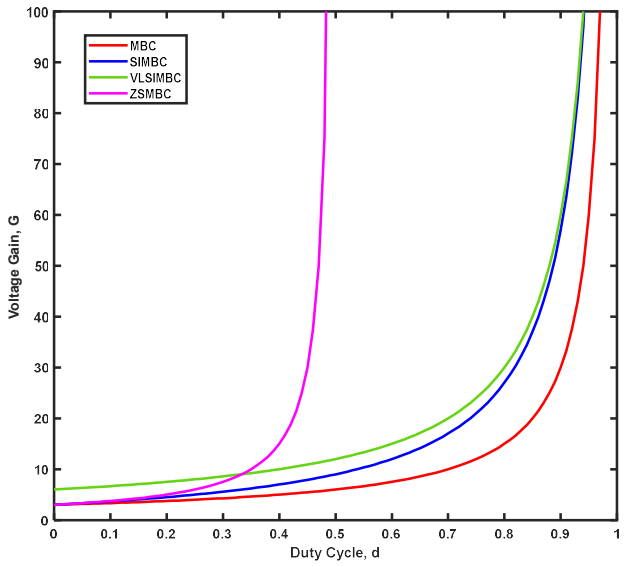

Figure 6.1: Voltage gains against the duty cycle for the proposed converters.

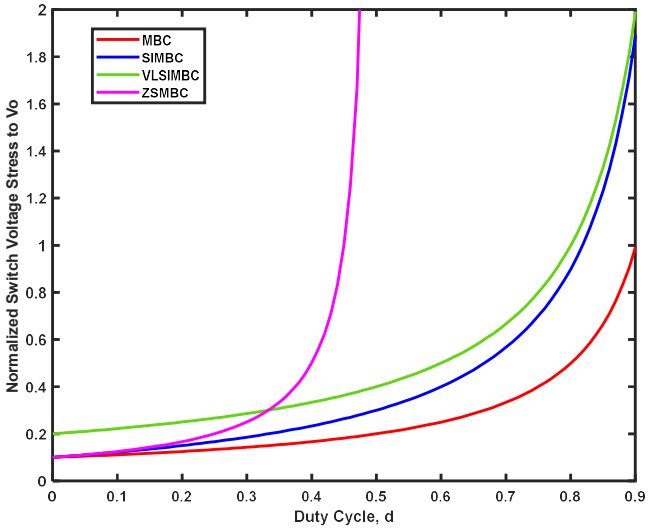

Figure 6.2: Normalized voltage stress of the high gain topologies.

Additionally, Figure 6.3 shows the measured efficiency of the MBC, SIMBC, and VLSIMBC with respect to the output power ranging from 900 W to 2.5 kW. The data shows that the VLSIMBC has better performance with maximum measured efficiency of 93.2% at 2.5 kW. Therefore, the efficiency of the proposed converters can be improved with the optimal selection of components.

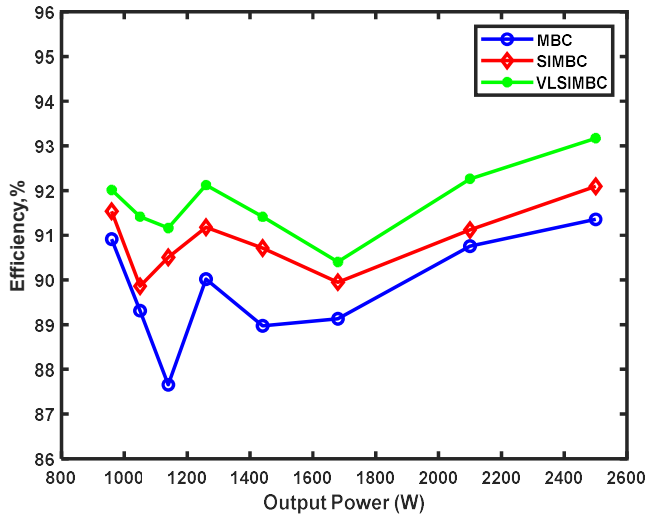

Figure 6.3: Converters efficiency at varying output powers.

6.2 SUMMARY

The most significant consideration in electrical supply is providing a clean, cheap, and sustainable power supply to consumers through the distribution grid. Renewable energy sources, such as wave energy and solar photovoltaic, are within the most environmentally friendly energy-generating systems and have the potential to supply a substantial amount of the world's future energy demands. According to this, pursuing further research and advancement in renewable energy sources has become increasingly significant. Nonetheless, the rising utilisation of renewable energy sources presents additional challenges to power conversion systems. For instance, devices that store or generate power can frequently be achieved by implementing multiple low-voltage storage cells, typically connected in series, to produce sufficient voltages for the required applications. These challenges might contribute to an obstacle to utilising renewable energy sources in high-power applications. Accordingly, multilevel converter topologies have the potential to overcome these challenges and are ideal for use in renewable energy generation systems.

Since the research in this thesis aims to generate MVDC from renewable energy sources like wave energy, transformerless high gain DC-DC converter topologies for power conversion systems have been proposed. Four converter topologies (MBC, SIMBC, VLSIMBC, and ZSMBC) have been studied, analysed, and implemented, adopting the increasing voltage conversion ratio techniques. In addition to the main objective of achieving a high voltage gain, the four converters share these advantages, including:

- The ability to realise high voltage gain without the need for an extreme duty cycle, resulting in low voltage stress on the switching device and the creation of three self-balanced voltage levels at the output.

- These topologies also reduce the complexity of the control strategy by only requiring a single switching device.
- Enabling high switching frequency.
- The capability of operating in the absence of magnetic components.
- They can be built in a modular way, and more levels can be added without changing the main circuit.

The most effective techniques for achieving high voltage gain in DC-DC step-up converters have been reviewed in Chapter 2. It can be concluded that conventional converters could not reach a gain of 10 times or higher, which is essential for high-power applications. Consequently, several topologies that can provide a high conversion ratio without requiring excessive duty cycle operation have been discussed. These topologies' advantages and disadvantages have been presented and analysed. Furthermore, integrating the capacitive and magnetic techniques is the optimal approach to attain a high voltage conversion ratio with less duty cycle and low voltage stress across the devices.

The results and discussions presented in Chapter 3 relate to the performance evaluation of a three-level DC-DC multilevel boost converter (MBC). The assessment was done through simulations and experimental tests. The MBC topology offered significant advantages, such as reduced device voltage stress and achieving higher output voltages without needing high-voltage FETs. The practical and simulated results were shown to be in agreement with the equations presented in this chapter, with switching transients observed in the experimental results due to the parasitic capacitances and inductances in the circuit. The results also demonstrated that the inductor current was continuous, indicating that the converter operated in continuous conduction mode (CCM). Moreover, the voltage balance was attained across all

capacitors. Taking into consideration that the voltage transients visible in the output capacitors were associated with the turn-on and turn-off transients of the MOSFET and parasitic components. Besides that, the experimental findings demonstrate high efficiency, with values ranging from 91.7% to 92.4% for the frequency range of 50 to 150 kHz. This suggests that the proposed three-level MBC can function effectively at various switching frequencies within this range without substantially influencing the entire system's efficiency. This is a significant achievement because it offers a way for the converter to be flexible and optimised in response to specific requirements, such as size, cost, and application. Overall, the findings provide valuable data on the performance of the proposed three-level MBC. These observations demonstrate the potential of the proposed converter to be implemented in wave energy.

Improvements in the design of the multilevel boost converter (MBC) are discussed in Chapter 4 in the form of transformerless high voltage gain DC-DC converters, including the switched inductor multilevel boost converter (SIMBC) and the voltage lift switched inductor multilevel boost converter (VLSIMB). Results from simulation and experiments with the two prototype circuits validate each power converter's theory and operational characteristics, indicating that the converters can achieve a voltage gain of ten times or higher without a higher excessive duty cycle or complex control algorithms. Analyses of the converters' performance, involving efficiency and power loss, have also been addressed in this chapter. It is demonstrated that the VLSIMBC has improved efficiency by 1.1% than the SIMBC and obtains higher voltage gain with a less duty cycle. Furthermore, the performance of the MBC was compared to that of the SIMBC and the VLSIMBC operating under identical conditions. The results showed that the SIMBC and VLSIMBC performed more efficiently and had a higher voltage gain at lower duty cycles. Notably, the voltage

stress across the switch in both proposed topologies in this chapter was about one-third of the converter output voltage, significantly improving over many of the power converters proposed in the literature. Conduction loss can be minimised in a high-performance device by keeping the voltage across the device to a minimum. Overall, this chapter comprehensively investigated the design, analysis, and performance assessment of two high gain DC-DC converter topologies, the SIMBC and VLSIMBC, confirming their practicality in a high step-up application.

Chapter 5 proposes a novel transformerless DC-DC Z-source multilevel boost converter (ZSMBC) that can achieve a high voltage gain of ten times or higher. It can be noted that the presented design is considered to be a step forward. When comparing the MBC, SIMBC, and VLSIMBC presented in previous chapters, as well as other recommended converters mentioned in the literature, integrating a Z-source impedance network into a multilevel boost converter is a viable approach for obtaining a high conversion ratio with a lower duty cycle ($D < 0.5\,\%$). Simulation and experimental findings of the proposed three-level ZSMBC are presented by combining the Z-source and voltage multiplier approaches, and the underlying theory, operation principle, and design concerns have been discussed in this chapter. Simulations of the circuit show a good level of match with the experimental data in terms of the trends in the operating conditions. In addition, the proposed converter has a small weight, size and a higher voltage gain with a lower duty cycle and voltage stress across the switch. This demonstrates the suitability of the proposed technology for the realization of a high gain DC-DC converter in a wave energy environment, where the excess heat from the electronics can be dissipated into the ocean.

6.3 FUTURE WORK

The following is an outline of several opportunities that have been highlighted as the potential future direction of study concerning this research work.

According to the literature review, state-of-the-art topologies for high step-up DC-DC converters use magnetic elements or capacitors with charge transference capabilities. One common approach is combining capacitive and magnetic techniques, mainly to increase voltage. Nevertheless, additional studies on voltage multiplier circuits may result in the development of new topologies that enhance efficiency.

The use of a high switching frequency leads to a small size of the converter and suggests wide bandgap semiconductor devices for the switch and diodes. However, the high switching frequency will contribute to a few drawbacks, including increased power loss. Therefore, there is an opportunity for further research on the restricted scope of switching frequency.

Due to the high equivalent series resistance (ESR) values of the capacitances, the voltage multiplier capacitors account for an overly major percent of total power losses in all four topologies, suggesting that optimising capacitors is a promising avenue for enhancing power efficiency.

The proposed converter topologies are operated in continuous conduction mode (CCM). Hence, future analysis of these topologies should be carried out in discontinuous conduction mode (DCM) for applications that demand such aspects.

One of the most critical considerations in high-power applications is the reasonable cost of power converters. However, the cost evaluation of the proposed high gain DC-DC converters has not been performed. Accordingly, future research could concentrate on practical approaches to develop low-cost converters.

Efficient thermal management is critical for the reliable operation of high gain DC-DC converters because of the high-power levels in which they operate. Therefore, further investigation of cooling methods should be performed to enhance the converters' thermal performance and reliability.

Consider the following essential recommendations for scaling the proposed converter topologies from the existing benchtop experimental set-up to higher power levels, such as 11 kV and 10 kW.

- Begin by carefully selecting higher-rated components corresponding to the desired output levels while reducing voltage stress on passive and active components. This comprises semiconductor devices, capacitors, and inductors, along with selecting appropriate voltage clamping devices or snubber circuits to regulate voltage spikes. Particularly, the suggested SiC MOSFET with drain-source resistance $\left(R_{DS(ON)}\right)$ of 0.12 Ω and a blocking voltage of 3.3 kV can be employed in stacked series configurations to attain the desired voltage rating while benefiting from the low $\left(R_{DS(ON)}\right)$. Besides, SiC Schottky diodes with a blocking voltage of 3.3 kV can be utilised in stacked series structures to achieve the needed voltage rating. The recommended inductor for this specification is a toroidal power inductor (HF467-102M-26AH).
- Ensure the selected components, converters' layout and traces on the printed circuit board (PCB) can manage rising currents without overheating or causing significant losses, maintaining the reliability and performance of the scaled-up converters. For instance, the maximum continuous current the proposed inductor can operate without overheating is 26 A.

- Employ advanced thermal modelling and heat management approaches that maintain component temperatures within acceptable limits to prevent overheating and enhance efficiency.
- Improve the protection assessed in the control system to handle larger voltage and power levels. This could imply improving control algorithms for better transient response and voltage regulation.
- Consider comprehensive testing, grid integration, and cost-effectiveness assessments.
- Seek regular optimisation possibilities concerning size, efficiency and control approaches for successful scaling.

It is highly recommended that the dynamic response of the proposed converters should be thoroughly investigated, taking into account the potential impact of parasitic components, including inductance, capacitance and resistance, since they can present unintended effects in electrical circuits. Assessing converters' dynamic response performance while accounting for parasitics is crucial, as these components impact response times, ringing, stability and efficiency. The converters must keep constant output voltage and current during load instabilities and respond fast enough to input voltage or load changes. Thus, control methodologies, such as loop gains and feedback, require further development, while parasitics tend to enhance dynamic response.

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