The Characterisation of CdTe-based Epitaxial Solar Cell structures fabricated by MOVPE

by

Michelle. Y. Simmons

A thesis submitted for the degree of Doctor of Philosophy

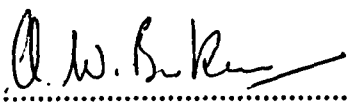
Department of Physics
The University of Durham

June 1992

This thesis is dedicated to
my Mum and Dad,
whom I love dearly.

Declaration

I declare that the work submitted in this thesis, unless otherwise stated, was carried out by the candidate, that it has not previously been submitted for any degree and that it is not currently being submitted for any other degree.



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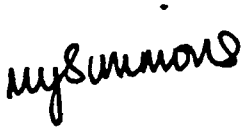
Dr. A. W. Brinkman
Supervisor



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M. Y. Simmons
Candidate

Abstract

This work has principally been concerned with the fabrication and characterisation of a number of CdTe-based p-n and p-i-n solar cells by MOVPE, namely: (i) the n-CdS/p-CdTe cell on {0001}CdS, (ii) the n-CdTe/p-ZnTe cell on {100}CdTe, (iii) the p-ZnTe/i-CdTe/n-CdS cell on {0001}CdS and (iv) the p-ZnTe/i-CdTe/n-GaAs cell on {100}GaAs.

The effects of substrate polishing on the quality of the epitaxial CdTe layers were investigated, and for CdS, a $CrO_3/HNO_3/H_2O$ polish was found to give the best surfaces for epitaxy. Doping studies proved ammonia gas unsuitable for the production of high conductivity p-type ZnTe and CdTe, but epilayers with conductivities of 10 Ωcm and 0.5 Ωcm respectively were obtained, however, using elemental arsenic heated to 250°C. Thin films of CdTe were then deposited by MOVPE at 325°C onto the opposite polar faces of {0001} and $\{01\bar{1}6\}$ oriented CdS single crystal substrates, the best morphologies being obtained on the non-metal or B faces of these planes. RHEED confirmed that the $\{111\}_{CdTe}\|\{000\bar{1}\}_{CdS}$ and $\{37\bar{5}\}_{CdTe}\|\{01\bar{1}\bar{6}\}_{CdS}$ epitaxial relationships were established whilst XTEM comfirmed that CdTe grown on both these planes contained a high density of lamellar twins lying parallel to the epilayer/substrate interface. Epitaxial n-CdS/p-CdTe cells were prepared on both (0001)A and $(000\bar{1})$B faces of CdS, where higher efficiencies were consistently found for A face devices despite better morphologies on B face devices, reasons for this remaining unclear.

Epitaxial ZnTe/CdTe/CdS and ZnTe/CdTe/GaAs p-i-n diode solar cells were also investigated, both devices giving similar conversion efficiencies. Analysis of current transport characteristics indicated that the current transport in the GaAs-based devices was dominated by a multistep tunneling process at all temperatures, whilst this mechanism was only important in the CdS-based devices at temperatures <250 K. Preliminary investigations into the growth of ZnTe/CdTe/ CdTe p-i-n cells on $\{\bar{1}\bar{1}\bar{1}\}$CdTe substrates and the growth of $Cd_{1-x}Zn_xTe$ alloys, for use in graded absorber layer structures are also presented.

Acknowledgements

Initially, and with sadness, I would like to thank the late Graham Russell for encouraging me to stay on at Durham. His enthusiasm for the subject was infectious and despite his loss I believe that this remains within all those he knew. I am very grateful to Andy Brinkman for taking me on with an already heavy workload and for being there throughout. Thanks also to Ken Durose for providing necessary support at some of the most difficult stages of the work and to Professor Woods for reading my thesis at such short notice.

I feel lucky to have worked with such an excellent group ..... thanks to Paul Clifton for teaching me the intricacies of MOVPE, Paul Brown for his invaluable help with TEM analysis and to James, Abdullah and Murat for providing moral support and making me laugh!! I wish them all the best. A special thanks to Haider whom I respect for his ability to try anything and everything-the mark of a true scientist.

Technical support within the department has been excellent thanks to Davy, John, Colin, Julie, Kay, Pauline and Sharon. I would especially like to thank Norman and Frank, who were not only good at their jobs but made me feel at home in Durham. Collaborative work with other groups has also been invaluable and I would like to thank Professor Tanner and John Hudson for helping with DCXRD measurements and Mrs.O.D. Dosser from RSRE for calibrated EDAX measurements. Thanks also to Peter Simmons (my Dad) for help printing the photographs ... its a day I'll never forget.

On a personal note I would like to take this opportunity to thank my friends: Arv. Barv, Alex, Pete and Jen, Alastair, Tony, Norman, J.A.K, Anth, John and Noreen, Harvey and Sonia; and my family (who have been superb), thanks to my brother, Gary and my Mum and Dad for their support and encouragement.

Finally an extra special thanks to Dan for help with the graphics and for going where no man has gone before ?!

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Chapter I

Introduction

As a source of energy the sun has many advantages over other coventional sources. Its energy is free, non-polluting, inexhaustible and is evenly distributed across the earth's surface. The energy from the sun which reaches the earth's surface each year is ten thousand times greater than the worlds annual production from other sources [1]. The direct conversion of this solar energy into electricity by terrestrial photovoltaic devices provides an important contribution towards meeting the increasing energy demands of the future and lessens the dependence on fossil fuels. The use of petroleum fuels is causing a number of serious problems that are degrading the global environment continually. Examples of the damage include the pollution created by burning petroleum fuels in rain, to form acid rain and the increasing CO_2 concentration, exacerbating the greenhouse effect.

Despite a drop in price by nearly a factor of ten in the last decade (from $\approx$£17 per watt in 1981 to $\approx$£2 per watt in 1992) solar cell power is still too expensive to compete with fossil fuel and nuclear power [2]. Current trends, however indicate that during the same time period the cost of fossil fuels and nuclear power has, and is continuing to increase. Thus the major objectives of research and development programmes within the photovoltaic industry have been to improve efficiency, stability, lifetime and reduce the costs of solar cell devices. In the 1970's the solar power industry was regarded with scepticism, the nuclear industry taking a leading role. Nuclear scientists even petitioned the White House to step up the use of coal and nuclear energy as "the only hope for achieving energy independence in the foreseeable future". Alternative energy sources were believed to be "flawed by geographical and technological limitations" [3]. It was the oil crisis in the 1970's that changed the picture, causing investment in the solar cell industry which has since made impressive technological advances and has experienced dramatic price reductions. As energy prices have risen photovoltaic systems have become a competitive energy source for a variety of applications.

1.1 Solar Cell Devices

Initial efforts concentrated on improving the cell efficiency, thus bettering the cost to performance ratio of the photovoltaic systems. Most of the photovoltaic products developed today use single crystal silicon cells, since amorphous silicon, GaAs and polycrystalline thin films are still being perfected. Of these the GaAs cells lead the field in efficiency, but are confined to laboratory development, single crystal silicon maintaining the lead in commercial products.

The efficiency of industrial crystalline silicon solar cells ranges from 10-15%, however laboratory type cells have efficiencies exceeding 24% [4]. This efficiency gap is caused by the usage of two different qualities of silicon substrate material, and by different cell processing. Laboratory cells are often made with techniques borrowed from microelectronics technology, while industrial cells are made using high throughput non-vacuum techniques. Advances in gettering and passivation have made it possible to obtain reasonable efficiencies using lower grade materials and it is expected that the two technologies will soon coexist.

The high production costs of III-V solar cells has meant that development efforts have focussed on space and concentrator applications. If these production costs can be brought down the high efficiency potential of III-V solar cells may make them an attractive option for terrestrial flat plate applications in countries with relatively low irradiation levels. Much of the interest in GaAs is attributed to the potential for use in tandem cell structures with potential efficiencies of $\approx$ 30%. These structures are however, complex and employ a large number of component layers. GaAs/InGaP tandem cells of 27.3% have been reported using GaAs as the lower band gap cell which is lattice matched to the wide band gap InGaP top cell [5]. Epitaxial layers of GaAs grown directly on silicon substrates have the attractive potentiality of reducing both cost and weight of GaAs single band gap solar cells as well as enabling a III-V/Si monolithic two band gap technology. The large lattice mismatch of 4% gives rise to a large dislocation density in the epilayer but efficiencies of $\approx$12% have been reported [6].

Polycrystalline cells are made of compound semiconductors, most common of which are the so-called II-VI compounds such as CdTe and the I-III-VI compounds such as $CuInSe_2$ (CIS). Polycrystalline cells are easily and reliably produced with

thin film techniques, their greatest attribute being that they can be mass produced economically. Problems remain with the deposition of photovoltaic grade material over very large areas, since processing control can only be maintained with thin film areas at best of 0.4 m^2. Processing technologies are being scaled up in dimension but care is needed over control of process related parameters e.g choice of substrate, carrier concentration, grain boundaries and surface recombination which affect the efficiencies of thin films produced. The advantages of CIS technology include large area modules and the low cost production processing techniques. Single junction large area submodules (0.4 m^2) with efficiencies of 9.7% have been fabricated and are expected to exceed 10% in the near future [7]. Over smaller areas, efficiencies of 14.1% have been observed [8]. Stability results taken from modules subjected to continous outdoor exposure indicate that less than 5% power loss occurs over 18 months. CIS is also being considered as a low band gap candidate for tandem photovoltaic modules, using either an advanced amorphous silicon alloy or a large band gap polycrystalline thin film material such as $CuGaSe_2$ or $CuInS_2$ to give module efficiencies of up to $\approx$17%. Despite showing promise, problems related to the reproducibility and stoichiometry of the CIS remain and the cell offers no advantages over CdTe cells (discussed in section 1.3). Not only are CIS cells less stable but they contain indium which is a rare, expensive and toxic metal.

The first amorphous silicon cells were fabricated in the early 1970's and by 1983 constituted 25% of all photovoltaic cells produced [9]. Problems with the trapping of current carrying electrons and holes within the amorphous atomic structure has however, caused a decrease in the electric current and hence cell efficiencies. When light shines on these structures the recombination of these electron-hole pairs has led to the incorporation of atomic impurities and microcracks within the atomic structure. This instability problem has been alleviated to some extent by passivating the films with hydrogen, but even these passivated layers contain voids and inhomogeneities [10]. The exact role that these light induced defects have in determining the performance and stability is still not fully resolved [11].

1.2 Solar Cell Applications

Once cells are produced they are generally joined to form conventional flat panels. These panels are then designed for use in either a fixed position or as

mechanically moveable units that track the moving sun. Cells are fitted with condensing lenses to form concentrators which operate much as magnifying lens to condense sunlight into a highly defined dense beam. Alternatively thin film cells are cut into smaller devices to power consumer products such as calculators.

Japanese industry improved and innovated photovoltaic devices and production methods by investing large sums of money in order to end the dependence on oil. Most of the Japanese market for photovoltaic devices is in consumer electronic applications including calculators, radios, watches, battery chargers etc.. and for domestic uses such as lighting, water heating and other stand alone applications. Photovoltaic power plants were not considered feasible due to limited availability of land in Japan, but investment was encouraged in roof mounted arrays. Recent advances in this field have been to produce solar cell roofing tiles, aimed at reducing costs by eliminating solar cell frames (thought to constitute 30-40% of total product costs) [2].

Crystalline silicon photovoltaic power technologies have demonstrated highly reliable performance with very low operating and maintenance costs. A 350 kW concentrator photovoltaic power system, the largest at the time was installed in 1981 in Riyadh, Saudi Arabia to provide power to remote villages to supply energy for lighting, air conditioning, water pumping and small appliances. The source consisted of 160 concentrator arrays with the energy stored in batteries with a diesel back-up generator. Recent analysis of the performance of these arrays found an 18% degradation over 9 years resulting mainly from solder delamination rather than cell damage [12]. Recent generators such as the ARCO 1 megawatt plant in Hesperia, California have now made photovoltaics a good option for future large-scale energy supply [13].

Whilst competitive with stand alone power systems such as diesel generators, photovoltaic systems are still too capital intensive to compete with utility supplied electricity or with fossil fuel boilers scaled for large industries. Small scale grid connected photovoltaic systems in residential applications are considered the most promising and cost effective way of introducing photovoltaics to wider use. Technological advances have permitted modules to be sold today that are 15-20 times less costly than they were in 1975, but this still needs to be reduced by

about 2.5 times again, before they can move more convincingly into the successful multibillion dollar market [14].

1.3 CdTe Solar Cells

Recent advances in CdTe thin film technology are demonstrating the prospect for significant cost reduction for photovoltaic power compared to conventional crystalline silicon solar cells. This thin film technology offers excellent potential for future developments towards a high yield, low cost manufacturing process. Thin film CdTe solar cells have been produced since the 1960's when Vodakov produced a homojunction cell of 4% efficiency [15]. Since then CdTe based cells have been produced by a variety of techniques e.g precipitation, evaporation, chemical vapour deposition, spray pyrolysis, close spaced vapour transport, and screen printing and with different junctions e.g homojunction, CdTe/Cu_2Te, CdTe/CdS, ZnCdS/CdTe, ITO/CdTe, and ZnO/CdTe cells.

The highest predicted theoretical efficiency of these systems lies with the CdTe/CdS heterojunction, with an efficiency of $\approx$ 25% [16]. The highest practical efficiency has however been 14.1% [17], whilst BP Solar are producing 0.4 m^2 modules with an efficiency of 10% which are stable over 18 months [16]. One of the major advantages of these cells is that they seem to suffer from significantly small degradation. Cells after 10 years of storage in an uncapsulated state have shown unimpaired device values, and additional irradiation over 4 months did not lead to any degradation [18].

In order to determine the optimum device performance of CdTe-based solar cells a fabrication technique capable of reducing defect content within the cell structure is necessary to be able to monitor device parameters in the absence of polycrystalline grain boundaries. These defects affect current-transport mechanisms across the junction and are known to severly degrade device performance. The use of metal organic vapour phase epitaxy (MOVPE) to grow epitaxial device structures allows investigation into the potential of these CdTe-based cells.

1.4 The present study

The primary motivation behind the present study was to develop the various

stages of the device fabrication procedure in order to be able to make preliminary investigations into MOVPE-grown CdTe-based solar cells. Chapter 2 introduces the relevant background in CdTe based cells and discusses the general characteristics of solar cell devices. More detailed theory on current-transport mechanisms and principles of operation are also presented. The details of the experimental set-ups used for the structural and electrical characterisation of the epilayers and devices are outlined in chapter 3.

The experimental results obtained during the course of this study are contained within chapters 4 to 8; chapters 4 and 5 describing the development of the various fabrication stages in the production of MOVPE-grown devices, and chapters 6, 7 and 8 presenting preliminary device measurements. Chapter 4 discusses the methods of substrate preparation employed to obtain optimum surfaces for epitaxy. A detailed study of the effects of various chemical polishes on the substrate surfaces is also presented. Chapter 5 describes the MOVPE growth process, including the optimisation of the growth of the binaries, CdTe and ZnTe, and of the ternary, $Cd_{1-x}Zn_xTe$. Studies on the p-type doping of CdTe and ZnTe for incorporation in device structures is also discussed.

Chapter 6 details the electrical and optical properties of the CdS/CdTe cells grown on single crystal CdS substrates, including findings on substrate orientation, polarity and current-transport mechanisms. The results of measurements of the electrical and optical properties of n-CdTe/p-ZnTe cells are given in chapter 7. Chapter 8 decribes the results of epitaxial p-i-n structures based on n- type substrates with epitaxial i-CdTe/p-ZnTe, where the substrate was either n-CdS, n-GaAs or n-CdTe respectively. Preliminary results as to the effects of grading the i-layer are also produced and a comparison of these p-i-n devices with conventional p-n structures is discussed. Chapter 9 concludes the experimental findings indicating the major objectives achieved whilst providing suggestions for future work in the field of MOVPE-grown solar cell devices.

1.5 References

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Chapter II

Solar cell and heterojunction theory

2.1 The solar cell

2.1.1 The junction

When solar radiation falls on a semiconducting material and is absorbed, electron-hole pairs are generated. The minimum energy that a photon must have to create an electron-hole pair is the band gap energy, E_g of the absorbing material. A photon with energy less than E_g cannot create these electron-hole pairs and in principle is not therefore absorbed, whilst a photon with an energy greater than E_g still contibutes only one electron-hole pair, the excess energy being wasted as heat. In order for these electron-hole pairs to contribute to a current in an external circuit they must be separated from each other. The p-n junction is ideally suited for this purpose and provides the cornerstone for photovoltaic technology. Used in this way, a p-n junction is generally referred to as a photovoltaic solar cell. Figure 2.1 describes the energy band diagram of a p-n junction heterojunction solar cell where an incoming photon has created an electron-hole pair (in this case in the p-side, close to the junction). The built-in potential at the junction has then separated the electron and hole, sweeping the electron across the barrier into the n-side, while repelling the hole.

Figure 2.2 illustrates one type of schematic diagram for a p-n junction solar cell, comprising of a top "window" layer, generally a semiconductor with a large band gap through which the light can pass to the absorber layer to create electron-hole pairs. A contact grid structure is applied to the window layer and the absorber layer is covered by another contact, both of which are ohmic. If the incident light passes though a grid on the larger band gap window layer it is termed "backwall illumination", but if the illumination occurs through the absorber layer it is called "frontwall illumination".

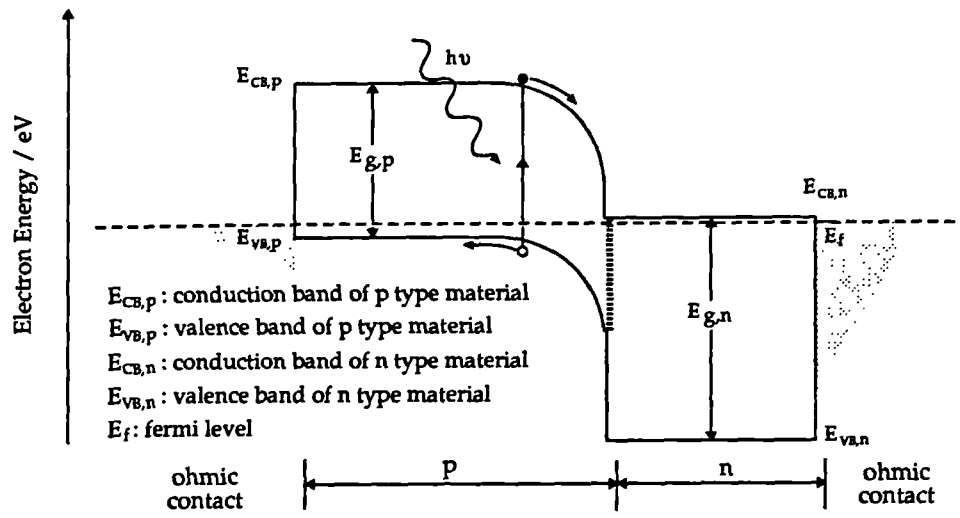

Figure 2.1 — Energy band diagram of a p-n heterojunction solar cell illustrating how the electron hole pair is separated by the internal field across the junction

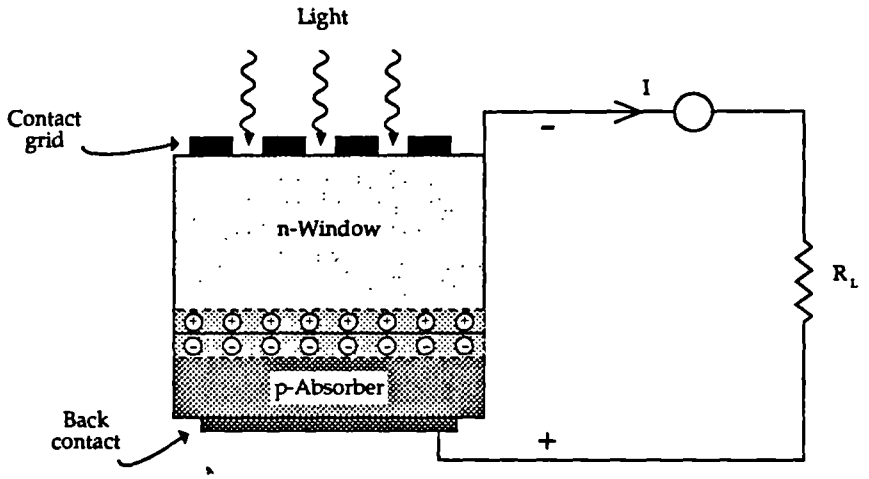

Figure 2.2 — A schematic diagram of a heterojunction solar cell

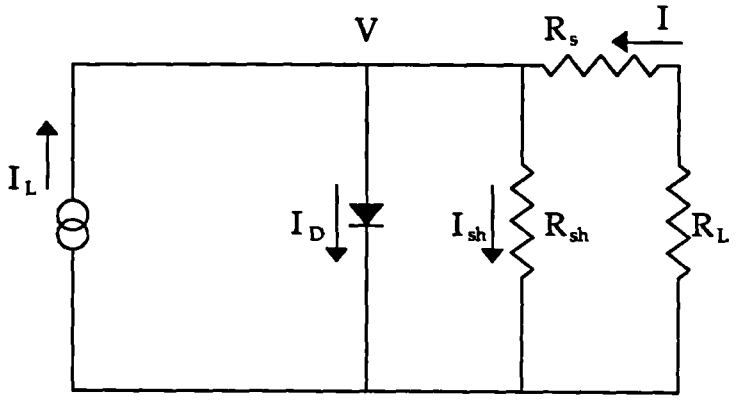

Figure 2.3 — The equivalent circuit for a solar cell

Various electronic processes occur within the solar cell, and these can be divided into 6 separate regions existing within the device itself.

(1) the metal contact to the absorbing (in this case the p-type) semiconductor, introducing a contact resistance.
(2) the bulk of the absorber region where electron-hole pairs are generated by the absorption of light and where the minority carriers are transported by diffusion to the junction and partially lost by recombination.
(3) the junction region itself where interface states arising from the difference in the lattice parameters of the two materials leads to recombination. Across the junction is the built-in electric field which separates the carriers.
(4) the bulk (n-type) window layer which, although essential to the operation of the cell nevertheless, constitutes added internal resistance.
(5) the contact to the n-type semiconductor introducing a second contact resistance and
(6) the front surface, where surface recombination loss of minority carriers can occur.

The corresponding equivalent circuit for such a solar cell device under illumination is shown in figure 2.3. The p-n junction (assumed to be ideal) is in parallel with a light dependent current generator, I_L, and a resistance, R_{sh}. The current to the external load, R_L, encounters an internal series resistance, R_s and is given by

$$I_L - I_D - I_{sh} + I = 0 \qquad [2.1]$$

These loss mechanisms can be lumped together in an electrical equivalent circuit as shunt and series resistive elements.

$$I_D = I_o\left\{ exp\left[\frac{q(V - IR_s)}{nkT}\right] - 1\right\} \qquad [2.2]$$

$$I_{sh} = \frac{V - IR_s}{R_{sh}} \qquad [2.3]$$

Thus combining equations 2.2 and 2.3 gives

$$I = I_o\left\{ exp\left[\frac{q(V - IR_s)}{nkT}\right] - 1\right\} + \frac{V - IR_s}{R_{sh}} - I_L \qquad [2.4]$$

The shunt resistance, R_{sh} accounts for all leakage currents such as those associated with localised states near the interface of the heterojunction and within the junction itself, that act as additional recombination pathways. The series resistance element represents internal resistive and dissipative losses such as bulk and contact resistances. The equivalent circuit response can also be considered as consisting of two diodes rather than one. As the temperature of the device changes, the dark I-V behaviour can be dominated by either space-charge recombination (one diode) or by a tunneling mechanism (the other diode). For an ideal cell, I_o and n are not functions of illumination and any parallel shunting resistance across the junction is effectively infinite.

In choosing the semiconductors for a solar cell application there are a number of material parameters that need to be considered, including the band gap, absorption coefficient, diffusion lengths, minority carrier lifetimes, doping, lattice parameters and surface recombination states. These parameters are discussed in detail below.

As the band gap of the absorbing region increases the diode parameter, I_o decreases strongly which in turn increases the voltage obtainable from the cell. Increasing the band gap however, also decreases the photogenerated current available since a smaller fraction of the solar spectrum is absorbed. The compromise between these two effects produces a maximum in the solar efficiency at band gap energies of 1.4-1.5 eV, as illustrated in figure 2.4. The window layer should be a large band gap semiconductor that does not absorb any significant proportion of the incident photons, whilst forming the junction that yields the photovoltaic effect. For solar cell applications, the thickness of the absorber layer required to absorb all the photons incident at its surface is given by approximately $\frac{1}{\alpha}$ [1], where α is the absorption coefficient of the absorber material. Direct band gap semiconductors have higher absorption coefficients and as such thinner layers are necessary for the absorption of the same number of photons than with indirect semiconduc-

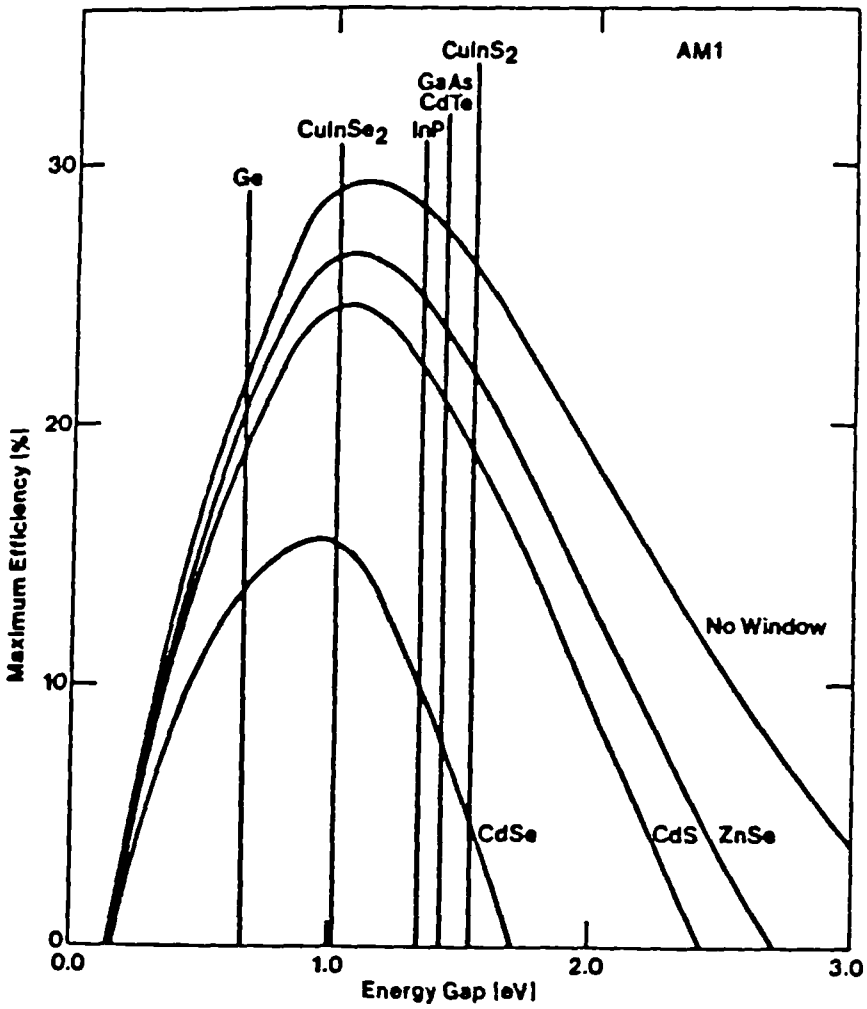

Figure 2.4 — Theoretical efficiencies of heterojunction solar cells as a function of energy gap for various absorber and window materials [1].

ultimately reduces the material costs and, as such, is favourable in the fabrication processes of solar cell devices.

Electron-hole pairs generated in the junction region are immediately separated by the built-in field. However, electron-hole pairs generated outside the depletion region have to be able to move across the absorption region to the junction, any that recombine before this stage do not contribute to the photocurrent. The minority carriers rely on diffusion to reach the junction and thus the minority carrier diffusion length, L (i.e the length the minority carriers are able to diffuse before recombining) is an important parameter in determining collection efficiency. This diffusion length is dependent on the crystallinity, defect content, and stoichiometry of the material involved. Similarly, large values of minority carrier lifetimes are desirable for efficient devices and the presence of a high density of localised states or deep impurity levels is known to seriously reduce these lifetimes.

The lattice parameter mismatch between the two different semiconductors can lead to the formation of misfit dislocations and interface states. These act as recombination centers, again reducing the photogenerated current reaching the junction. The source of these interface states created in the MOVPE growth of semiconductors is discussed in section 2.1.5

The incorporation of dopants has a profound effect on the absorption coefficient, diffusion length and energy band gap [2]. In order to obtain a high photovoltage high levels of doping are required, however excessive doping can lead to smaller lifetimes. Again a compromise has to be reached to ascertain the optimum doping levels within the device. Another less obvious problem that affects the solar efficiency is the surface states on the window material. Surface states arise from dangling bonds, oxide layers and chemical residues that lead to recombination of carriers thus limiting the cell performance. This results in an increase in contact resistance and various passivation techniques have been developed to minimise these losses [3].

2.1.2 The solar spectrum

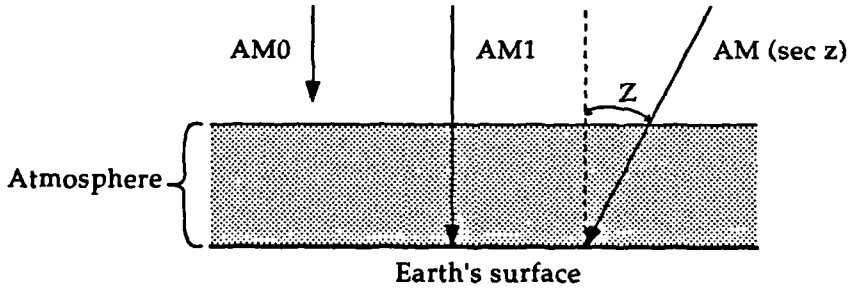

Figure 2.5 — Effect of the Solar Zenith Angle on Insolation at the surface of the Earth

The solar efficiency of a photovoltaic system depends critically on the spectral distribution arising at the surface from the earths atmosphere, which depends

not only on the composition of the atmosphere but the path length of the radiation through the atmosphere. Factors such as the water content, turbidity, ozone content, cloudiness, haziness, and ground reflections all affect the solar radiation reaching the Earth's surface. Another important parameter is the Sun's declination angle which varies the path length through the atmosphere. This geometric effect is described by specifying a zenith angle of the sun, z, the angle between the earth-sun radius and the normal to the Earth's surface, as illustrated in figure 2.5. The path length through the atmosphere is described in terms of an equivalent air mass, m_r. Thus specific solar spectra are labelled AMm_r, with AM0 corresponding to the solar spectrum at the outer edge of the Earth's atmosphere, AM1 to that at the Earth's surface for normal incidence and AMm_r is at the Earth's surface with m_r=sec z, i.e the deviation from normal incidence. All solar cells are tested under one of these standard air mass conditions for comparative purposes and the AM1.5 spectrum representing the sun at 45° to the zenith, with an incident power of $\approx$ 875 Wm^{-2}, is used for this thesis.

2.1.3 Solar cell device parameters

As described in section 2.1.1 electron-hole pairs are generated by illumination, which are separated by the electric field at the junction. In terms of the diode equation these charge movements constitute a generation of current. If the charge released by the illumination produces a current I_L, then the current that may be drawn from the solar cell in light is given in equation 2.4.

For an ideal junction, R_{sh} is infinite and R_s is negligible, giving

$$I \cong I_o \left[exp\left\{ \frac{qV}{nkT} \right\} - 1 \right] - I_L \qquad [2.5]$$

Under no load conditions the current supplied by the cell will, of course, be zero and the voltage will reach its maximum value, known as the open circuit voltage, V_{oc}. As the level is progressively increased (i.e the load resistance decreases) the current increases and the voltage drops until it approaches zero. The corresponding current is termed the short circuit current, I_{sc} and this is represented in figure 2.6.

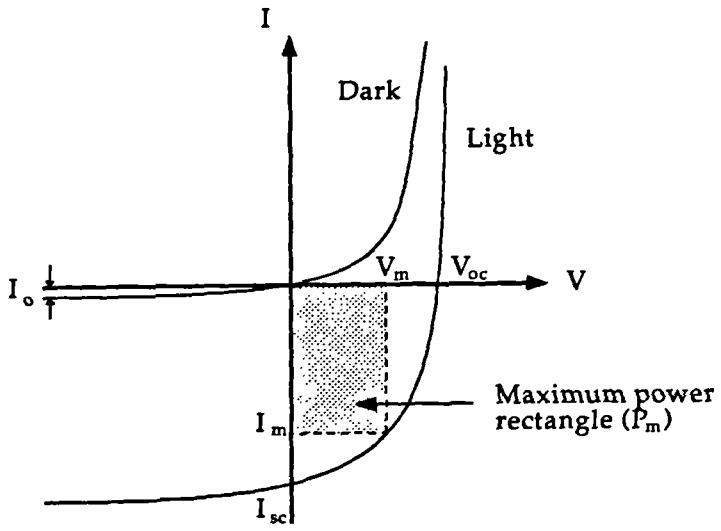

Figure 2.6 — Typical variation of the current, I as a function of the voltage, V for a solar cell in the dark and under illumination. The magnitude of I_o is exaggerated for clarity

At some intermediate value of voltage and current output, the product $I_m V_m$, reaches a maximum and it is at this point that the maximum electrical power is being taken from the source of illumination. The solar efficiency η, of the cell is defined as the ratio of this maximum power P_m ($I_m V_m$) to the solar power incident on the cell, P given by

$$\eta = \frac{P_m}{P} \qquad [2.6]$$

A quantity called the fill factor, ff, is commonly introduced to relate the value of P_m to the product $V_{oc} I_{sc}$,

$$ff = \frac{I_m V_m}{I_{sc} V_{oc}} = \frac{P_m}{I_{sc} V_{oc}} \qquad [2.7]$$

and the efficiency is given by

$$\eta = ff \frac{I_{sc} V_{oc}}{P_s} \qquad [2.8]$$

Typical values for a single cell are V_{oc}=0.4-0.8 V, I_{sc}=10-40 mAcm^{-2}, ff=0.3-0.8 and η=1-20%.

The maximum short circuit current obtainable for a semiconductor is determined by the spectrum of the light source and the spectral response of the device. Figure 2.7 shows 3 curves related to the solar flux density spectrum at different wavelengths where it can be seen that the spectrum of sunlight extends from the ultraviolet through the visible to the far infrared. The spectral response of a particular device gives the fraction of incident photons at that wavelength that contribute to a current in the external circuit. It is properly the spectral dependence of the quantum efficiency.

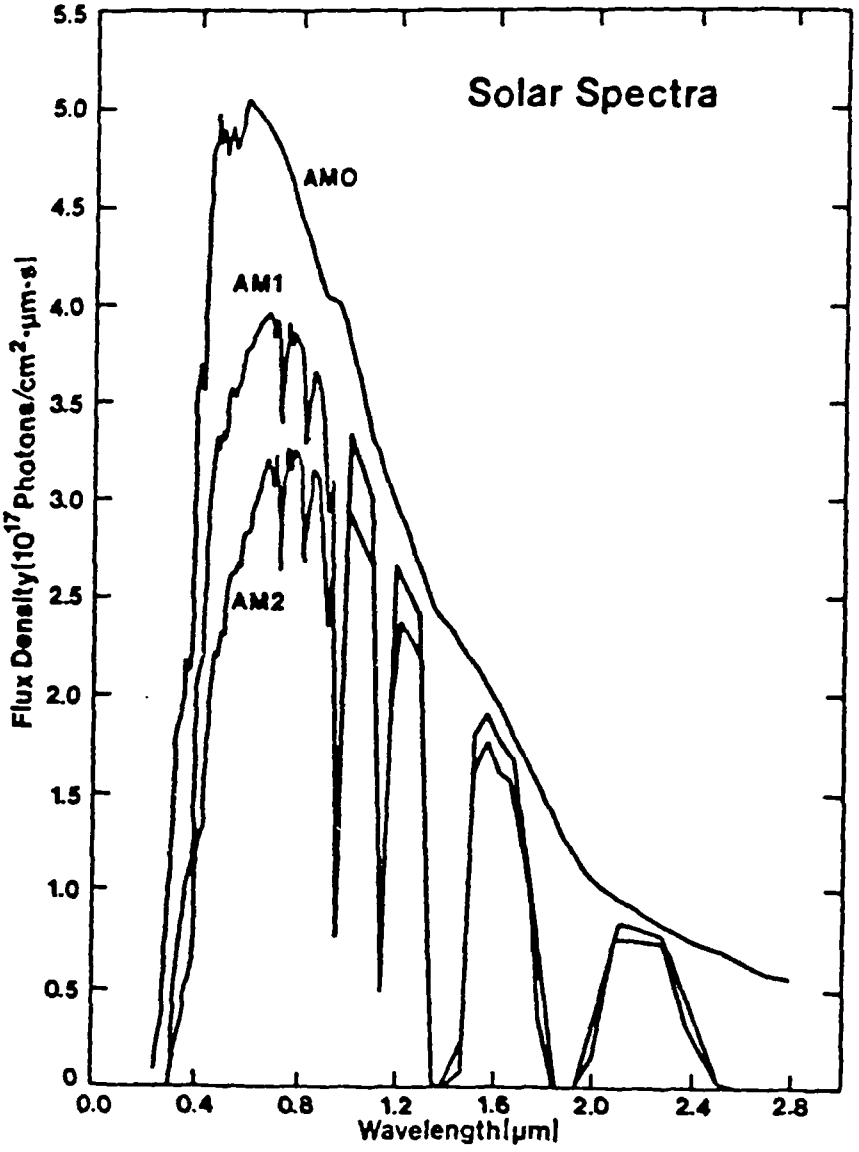

Figure 2.7 — Spectral distribution of solar radiation under AM0, AM1 and AM2 conditions [1].

The fill factor is strongly dependent on the series and shunt resistances within the device. The series resistance arises from the internal resistance within the device, e.g the contact resistances and the bulk resistances of the semiconducting layers and these should be as low as possible in order to have a high fill factor. Similarly the shunt resistance should be as high as possible to obtain high fill factors. The shunt resistance decreases due to the formation of defects and the presence of surface leakage along the edge of the cell which have to be minimised if the shunt resistance is to be large.

2.1.4 Defects in epitaxial solar cells

The use of MOVPE for the fabrication of solar cell devices has only recently been considered. Whilst producing epitaxial structures, the epilayers still contain defects which arise at the junction region due to the nature of the growth procedure. These defects fall into 5 categories and include :

(1) Propagation of defects from the substrates into the epitaxial layer. Substrates are chosen that do not generally contain dislocations which would propagate into the layer, however loops that intersect the surfaces of specially prepared substrates still result in the propagation of dislocations into the epilayer [4].

(2) Stacking faults occur due to the improper preparation of substrates. In many layers stacking faults form closed figures i.e triangles in (111) oriented layers and squares for (100) oriented layers. These are well known to propagate from the initial interface [5].

(3) Formation of low angle grain boundaries and twins due to rotation of islands. Islands of crystal nucleate in several orientations and when such misoriented islands meet and coalesce defects such as low angle grain boundaries or twins are formed. Some of these defects anneal out during the growth process, but often the defects propagate into the film.

(4) Formation of precipitates or dislocation loops caused by the supersaturation of either impurities, dopants or native defects during cooling.

(5) The formation of dislocations due to the lattice parameter mismatch between the substrate and epilayer. Frank and van der Merwe [6] predicted that with a

mismatch <12% the epilayer would initially grow pseudomorphically i.e the epilayer would be elastically strained to have the same interatomic spacing as the substrate. With increasing thickness the elastic energy increases until dislocations are generated to relieve the misfit strain. The thickness at which misfit dislocations are formed is called the "critical thickness". For systems with a lattice mismatch greater than 12%, a critical thickness of only a few atomic layers is observed, the interface comprising of a complex array of short misfit dislocations. Continued growth is considered homoepitaxial, where threading dislocations propagate, interact and annihilate one another.

The performance of most devices such as LED's, solar cells and photon detectors is severely degraded by the presence of misfit dislocations. Thus, in recent years research has concentrated on alloys lattice matched to the substrate, such that any abrupt changes in composition necessary for high performance solar cells [7] can be made without introducing undesirable dislocations at the interface.

2.2 Solar cell technologies

2.2.1 Solar cell structures

There are many solar cell configurations designed to achieve high conversion efficiencies and subsequently many ways of classifying them. Along with the materials used, leading broadly to group IV-IV, III-V, I-III-VI and II-VI semiconductor solar cells, they can also be classified by their crystalline quality, i.e amorphous, polycrystalline or epitaxial and finally by the type of cell produced, e.g homojunction, heterojunction or Schottky barrier type. Recent advances in solar technology have also led to the formation of new device structures such as tandem cells, multi-quantum well structures and "graded absorber" layer structures. With a few exceptions e.g the advent of organic solar cells [8] all solar cells will fit into one or more of these classification schemes. A comprehensive classification system is beyond the scope of this thesis, however a discussion of the various types is given below.

Homojunctions are p-n junctions within the same semiconductor material, e.g single crystal silicon cells utilising a 0.2μm thick n-type "window" region on a

thick p-type silicon absorber have been reported with efficiencies of $\approx 25\%$ [9].

Heterojunction cells are p-n junctions between two different semiconductor materials. There are however several criteria that limit the choice of the two semiconductors forming the heterojunction.

(i) there must be an absence of conduction or valence band spikes that could impede the photogenerated carrier transport.
(ii) ΔE_c for p-type absorbers must be as close to zero as possible to maximise the diffusion voltage, V_d and V_{oc} for the cell.
(iii) the absorber band gap should be close to 1.4-1.5 eV to take advantage of the maximum in solar efficiency.
(iv) the band gap of the window material must be large to prevent absorption of the solar spectrum before the photons arrive at the absorber layer whilst still retaining a low resistance.
(v) there should be a small lattice mismatch.
(vi) there should also be as small an expansion mismatch as possible since most junctions are prepared at high temperatures and used at room temperature.

Examples of common heterojunctions are GaAs/GaAlAs, $CuInSe_2$/CdS and CdTe/CdS.

Schottky barrier devices consist of metal-semiconductor (M-S), metal- insulator -semiconductor (M-I-S) and semiconductor-insulator-semiconductor (S-I-S) junctions. Their advantages lie in their simplicity and relatively inexpensive processing technology. Values of V_{oc} are lower for these devices, however, as a consequence of the large values of I_o due to the small potential barrier height. The advent of i-layers in these devices were shown to have an advantageous effect mainly by increasing the V_{oc} for the device, however very little work has been done on these structures intentionally. Following the improvement in metal-semiconductor structures by the insertion of an insulating layer, other researchers began to investigate whether a heterojunction structure could be improved in the same way. It was found [10] that the insulating layer was advantageous since it increased the effective barrier at the semiconductor surface, thus increasing the value of the diode

factor, and decreasing the dark diode current, I_o. The essential difference between M-I-S and S-I-S structures is that in the S-I-S case there is no large density of states within the forbidden gap of the bulk semiconductor and tunneling/recombination has to occur across the i-layer via interface states.

A single junction solar cell can only utilise photons of energy exceeding the band gap of the absorbing material and has a thermodynamically limited efficiency under unconcentrated sunlight of $\approx$ 30%. By positioning a second solar cell of smaller band gap to intercept the lower energy photons, which pass through a wider band gap solar cell, the total conversion efficiency can be increased. In the limit of an infinite stack of cells the efficiency was predicted theoretically to reach 68% [11]. The increase in the complexity of the device manufacture, weighed against the improvement in efficiency, practically limits the number of cells in a multijunction device to 2 or 3 in general [12]. An example of such a tandem cell is a InGaP top cell on a GaAs bottom cell giving an overall efficiency of 27.3% [13].

The V_{oc} of high efficiency cells is thought to be limited by interface and space-charge recombination. Recombination currents can be reduced by increasing the band gap of the absorber material, however this also leads to a corresponding loss in photocurrent. In order to reduce the recombination currents without loss of photocurrent, structures with a gradual increase of band gap towards the hetero-junction or "graded gap absorbers" have recently been investigated [14]. Cells with an efficiency of $\approx$ 9% were found to increase their efficiency to 10.2% under AM1 illumination, with such a graded absorber [15].

Quantum well structures could in principal offer higher efficiencies by stacking together several solar cells with different band gaps. In practice connecting these cells together optically and electrically has proved difficult. An alternative quantum well solar cell approach, utilises an intrinsic layer which includes the quantum wells (50 or more). The electron and holes which are created in the well can either escape from the well or they will be lost by recombination. In good material the escape processes have been seen to dominate [16].

Another classification scheme is to group the cells according to their crystallinity. Amorphous semiconductors have no long range order or periodicity in the arrangement of the atoms. Initial advantages in these types were thought to

arise from the wide range of compositions available and the versatility of the depostion process. Amorphous silicon solar cells have suffered problems with stability under long term illumination [17], due to the light induced defect creation that increases the recombination rate of the photogenerated carriers.

Polycrystalline semiconductors have crystalline order, but are comprised of small randomly oriented crystallites of varying size and orientation. The individual crystallites are generally of good quality, but are interrupted by numerous grain boundaries and occasional voids which are generally regions of increased recombination. Charge trapping at grain boundary energy levels can form potential barriers and impede carrier transport. The fabrication technology is however less expensive and, as such, these cells constitute the majority of commercial solar cell devices.

Single crystal materials have a high order of crystallinity and perfection, and subsequently lead to the highest efficiency cells. One set back of this is the production of high quality crystalline material is expensive. Most of the work in this field has been in the fabrication of crystalline silicon cells with efficiencies of $\approx$ 28% [18].

Presently there are 5 areas of solar cell technology that are receiving intensive study and these are summarised below

(i) amorphous silicon: efficiencies of $\approx$ 6% [17] are now being superseded by
(ii) single crystal silicon cells: improved techniques of surface preparation such as laser grooving which increases the number of reflections at the surface causing more light to go into the sample has led to efficiencies of up to 28% [18].
(iii) single crystal GaAs cells have been fabricated using LPE giving efficiencies of 21% [19], whilst InGaP has been used in a top cell GaAs tandem cell structure to give an efficiency of 27.3% [20].
(iv) $CuInSe_2$ has also been proposed as a low band gap absorber for tandem cells [21]. Modules of 0.4 m^2 having 10% efficiencies have been fabricated and were found to be stable over 18 months of operation.
(v) CdTe has also received considerable interest (see section 2.3 for a more detailed description of these cells) with British Petroleum (BP) reporting 3×3 m^2 devices with efficiencies of >9% and stable performances over 18 months [22].

Technique	Description
Vacuum evaporation (VE)	Materials from an evaporation source are sublimed under vacuum, and are then deposited on the substrate. Widely used and versatile, resulting in polycrystalline films.
Hot Wall epitaxy (HWE)	Vapours are transported through a heated cylindrical enclosure held at higher temperature than the substrate so that deposition of epitaxial films occurs.
Sputtering (S)	High energy ions are accelerated towards materials of interest which causes removal and subsequent condensation on a substrate.
Spray pyrolysis (SP)	An aqueous solution containing the soluble salts of desired compound is sprayed onto heated substrate where it undergoes pyrolytic decompostion and reacts with the substrate.
Screen printing (Sc.P)	Pastes containing the required materials are screen printed onto a substrate to define device patterns.
Chemical vapour deposition (CVD)	Vapourised precursor compounds are passed over heated substrate where reaction occurs and product condenses on surface.
Close-spaced vapour transport (CVST)	Source and substrate $\approx$ 1mm apart. Gas reacts with source to form volatile compound which decomposes on substrate to form film.
Plasma deposition (PD)	A glow discharge plasma breaks up vapours of required compounds which then react and deposit on substrate.
Electrodeposition (ED)	An electric current is passed through an electrolyte of required compound which deposits on substrate (electrode).
Liquid phase epitaxy (LPE)	Precipitation of material from a solution onto an underlying single crystal substrate.
Electroless deposition (ELD)	Substrate is dipped in appropriate solution containing desired compound to form film.

Table 2.1 — Summary of fabrication techniques

2.2.2 Fabrication technologies

Fabrication or deposition techniques have a characteristic effect on the nucleation and growth dominated microstructure of a thin film, and thereby its physical properties. Deposition techniques have been reviewed extensively in the literature [23] but table 2.1 summarises some of the more commonly used processes for thin film deposition. Until recently epitaxial techniques such as MOVPE and MBE were not applied to solar cell technologies due to their high cost, both in materials and equipment. However epitaxial devices produced in this way aid the investigation of current transport mechanisms and interfacial recombination in the absence of polycrystalline grain boundaries. The high degree of materials control with MOVPE and MBE will not only enable the study of graded or multicomposition $Cd_{1-x}Zn_xTe$ layers in the device to allow better use of the solar spectrum, but can lead to studies in low dimensional quantum well cells and high efficiency tandem cells. The techniques of MBE and MOVPE are discussed in detail in chapter 5, but have only recently been applied in the solar cell industry, and are mainly used as theoretical studies into the maximum efficiencies obtainable with near ideal heterojunctions.

2.3 CdTe-based solar cells

2.3.1 Introduction

Initial efforts with II-VI heterojunctions concentrated on the Cu_xS/CdS heterojunction with conversion efficiencies near 10% [24], until it was recognised that this junction did not possess the stability required of a commercial solar cell system. Several other II-VI heterojunctions have shown promise for photovoltaic conversion of solar energy including the n-ITO/p-CdTe [25], n-CdSe/p-ZnTe [26], n-CdS/p-CdTe [27], p-CdTe/n-ZnSe [26], n-ZnO/p-CdTe [28] and the p-ZnTe/i-CdTe/n-CdS [29] heterojunctions.

Cadmium telluride is a low cost, thin film photovoltaic absorber material with a band gap of 1.44 eV (at 300K) which coincides with the maximum in the theoretical

conversion efficiency of the solar spectrum [30]. The energy gap is direct with an optical absorption coefficient $>3\times10^4$ cm^{-1} at the band edge [31,32] which is large enough to require only one micron of material for quasi total absorption of light. CdTe can also be prepared in both n and p-type conductivity. Despite all these advantages there still remain some difficulties that have, in the past, made it undesirable as a solar cell component. For example, it is difficult to obtain low resistance ohmic contacts to p-type material as a result of the high electron affinity 4.5 eV [33], and correspondingly large work function of 5.95 eV. Problems are also encountered with the large concentration of uncontrollable residual acceptors, such as copper [34].

CdTe solar cells with efficiencies $\approx$ 10% or higher have been made as heterojunctions, homojunctions and M-I-S junctions prepared using a variety of deposition techniques to produce both single crystal and polycrystalline thin films.

The solar cell research in this thesis is principally on II-VI heterojunctions which use either p-type (chapter 6 and 7) or i-CdTe (chapter 8) as the absorber layers with n-CdS, n-GaAs or n-CdTe as the substrates. The relevant material parameters for all the II-VI and III-V semiconductors used in this thesis are summarised in table 2.2. Sections 2.3.2-4 go on to review the solar cells produced in this thesis, i.e n-CdS/p-CdTe, n-CdTe/p-ZnTe, n-CdS/i-CdTe/p-ZnTe, n-GaAs/i-CdTe/p-ZnTe and the n-CdTe/i-CdTe/p-ZnTe cell.

Material (300 K)	E_g (eV)	χ (eV)	μ_e ($cm^2V^{-1}s^{-1}$)	μ_h ($cm^2V^{-1}s^{-1}$)	Crystal structure	a (Å)	β (10^{-6} K^{-1})	p or n	ϕ (eV)
CdTe	1.44D	4.5	300	65	S	6.477	5.9	p/n	5.95
CdS	2.42D	4.5	400	15	W	a=4.14 c=6.72	4.0	n	4.79
ZnTe	2.26D	3.5	530	900	S	6.103	8.2	p	5.75
GaAs	1.42D	4.07	8500	420	S	5.65	5.8	p/n	4.8

where ϕ is the electron work function, a is the lattice parameter, β is the linear expansion coefficient, χ is the electron affinity, S=sphalerite and W=wurzite.

Table 2.2 — The material parameters for the compounds used in this thesis

Year	Cell	η (%)	V_{oc} (mV)	I_{sc} ($mAcm^{-2}$)	ff	Ref.
1972	CVD of CdS film onto CdTe thin film	5-6	0.51	1.5	0.4	[39]
1974	CSVT of thin film CdTe onto single crystal CdS	4	0.61	14	0.36	[42]
1976	CdTe thin film screen	8.1	0.69	11.4	0.51	[44]
1980	printed onto CdS thin film	12.8	0.73	11.4	0.51	[45]
1977	VPE of n-CdS onto	10.5	0.67	20.1	0.59	[43]
	p-CdTe single crystal	11.7	0.66	20.0	0.60	[46]
1977	Vacuum evap. of n-CdS onto single crystal p-CdTe	7.9	0.63	16.1	0.66	[40]
1977	Spray pyrolysis of n-CdS onto single crystal p-CdTe	6.5	0.53	16.4	0.63	[41]
1982	CSVT of p-CdTe onto Au/n-CdS on glass	10.5	0.75	17	0.62	[47]
1984	CdS and CdTe electroplated	9	0.75	20.6	0.60	[48]
1988	onto ITO/glass	10.3	0.73	21.2	0.67	[49]
1982	Screen-printed CdS/p-CdTe	12.8	0.73	28.5	0.52	[50]
1984	buried homo-junction	12.8	0.75	21.8	0.606	[51]
1987	Thermal evap. of CdTe onto CdS/glass	8.5	0.612	20.5	0.61	[52]
1987	CSVT of p-CdTe onto evaporated CdS/glass	10.5	0.75	22.2	0.63	[53]
1987	Electrodep. of p-CdTe onto spray dep. CdS/glass	10.4	0.74	22.0	-	[29]
1988	Spray pyrolysis of CdTe onto spray pyrolysed CdS/glass	8.7	0.75	17.3	0.67	[54]
1988	Screen printed CdTe onto sintered CdS/glass	12.8	0.75	28.2	0.61	[55]
1988	Spray pyrolysed CdS onto electroplated CdTe/glass	8.8	0.76	18.6	0.57	[56]
1989	Spray pyrolysed CdTe onto CdS/ITO/glass	12.3	0.782	24.98	0.63	[57]
1991	MOCVD CdTe onto spray pyrolysed CdS on ITO/glass	9.7	0.72	26.47	0.6	[58]
1991	Atomic layer epitaxy of CdTe onto CdS/ITO/glass	14	0.804	23.8	0.73	[59]

Table 2.3 — Current status of the n-CdS/p-CdTe solar cell

2.3.2 The n-CdS/p-CdTe solar cell

A summary of the solar cell fabrication techniques and solar efficiencies for the n-CdS/p-CdTe heterojunction is given in table 2.3. Early investigations of the n-CdS/p-CdTe heterojunctions focussed on their application as thin film diodes and optical detectors [35-38]. One of the first n-CdS/p-CdTe solar cells was made by Bonnet using a chemical vapour deposition technique to yield a cell with efficiency of 6% [39]. Subsequent n-CdS/p-CdTe cells generally involved the deposition of a polycrystalline layer of CdS onto single crystal CdTe substrates, using vacuum evaporation [40], spray pyrolysis [41], close spaced vapour transport [42], vapour phase deposition [43] or screen printing [44]. High deposition temperatures of $\approx$ 400°C meant that Cd diffusion into the CdS actually formed a n-CdS/n-CdTe/p-CdTe p-n homojunction with a CdS contact (which helped reduce the series resistance and surface recombination at the CdTe front surface). However high substrate temperatures also lead to unusually high growth rates resulting in poor quality films.

In order to meet goals for solar cell costs polycrystalline thin films have been extensively investigated, but future improvements in the solar efficiency of the n-CdS/p-CdTe heterojunction are expected to come primarily through improved fabrication techniques and materials.

2.3.3 The n-CdTe/p-ZnTe solar cell

Of the several II-VI heterpojunctions available for solar convertors the n-CdTe/p-ZnTe solar cell has received little interest. The n-CdTe/p-ZnTe junction itself however has been studied in more detail through general interest in II-VI superlattices (heterojunctions that are repeated to form a layered structure). Devices based on these structures will display properties and performances determined to a large extent by the degree to which grown-in stresses between multilayers of CdTe/ZnTe can be accommodated by elastic strain. CdTe and ZnTe possess bulk lattice constants differing by 6% from each other creating large internal stresses characteristic of II-VI superlattices. Deep level transient spectroscopy was used to

study the depletion region in the n-CdTe/p-ZnTe heterojunction [60] and revealed the presence of three hole trap levels due to

(i) Zn vacancies in the ZnTe epitaxial layer.
(ii) levels arising from interface states caused by lattice mismatch.
(iii) a deep level $\approx$ 0.98 eV above the conduction band due to trap states in the ZnTe side of the junction.

By forming a continuous series of $Cd_{1-x}Zn_xTe$ layers with compositions in the range $0< x <1$ between the two components of the heterojunction, the interface quality could be improved thus reducing recombination. Razykov et al [61] tried this "grading" technique in their n-CdTe/p-ZnTe solar cells prepared by a CVD fabrication process, and produced cells with an efficiency of 9.7%. Since then no further work has been reported on this heterojunction solar cell.

2.3.4 P-I-N solar cells based on CdTe as the absorber

P-I-N type solar cells based on CdTe as the absorber have only recently emerged in the solar cell market since the first paper published by Meyers [62]. Since this time a myriad of papers has resulted, diversifying into the many aspects of this p-i-n type of device. These advances are summarised in table 2.4. Initial interest was concerned with improving the efficiency of the n-CdS/i-CdTe/p-ZnTe device (an extension of the well studied n-CdS/p-CdTe device already studied) to 10%. The idea of using different absorber layers was introduced by Rohatgi et al [63], who replaced the i-CdTe layer with layers of i-CdZnTe and i-CdMnTe in order to create a wide gap cell (1.65-1.75 eV) for use in tandem cell structures.

CdZnTe and CdMnTe were thought to be the two most promising materials for top cell application since their band gaps could be tailored in the range 1.45-2.26 eV (CdTe-ZnTe) and 1.45-2.85 eV (CdTe-MnTe) respectively by controlling the film composition. The ultimate aim being to produce a top cell with $\approx$ 10% efficiency and 80% subgap transmission so that when it is coupled with a 15% bottom cell a combined efficiency of 15-20% could be achieved [65]. Initial difficulties with the

ternary cells of $\approx$ 6% efficiency were overcome by reducing the thickness of the i-layer so that the the depletion region did not extend into the bulk CdS or CdTe. Spectral response measurements on the ternary cells showed them to be suffering from recombination in the undepleted bulk. Photoluminescence measurements revealed broader luminescence peaks for the CdZnTe and the CdMnTe than for the CdTe films, and further improvements were expected by reducing the width of the ternary i-layer even further.

Device	Technique	η (%)	V_{oc} (mV)	I_{sc} ($mAcm^{-2}$)	ff
n-CdS/i-CdTe/p-ZnTe [62]	CdS-P, CdTe-EP ZnTe-VE	10.4	0.72	22.3	0.65
n-CdS/i-CdTe/p-ZnTe [56]	CdS-P, CdTe-EP ZnTe-VE	10.8	0.745	20.5	0.60
n-CdS/i-CdZnTe/p-ZnTe	i-CdZnTe:MBE	3.6	0.51	14.4	0.48
n-CdS/i-CdMnTe/p-ZnTe [63]	i-CdMnTe:MOCVD CdS-P, ZnTe-VE	6.0	0.68	20.6	0.44
n-CdS/i-CdMnTe/p-ZnTe [64]	i-CdMnTe:MOCVD CdS-P, ZnTe-VE	9.4	0.70	22.1	0.55

Table 2.4 — Summary of p-i-n solar cells

The use of MOVPE and MBE in these p-i-n devices has enabled the growth of ternary layers and the formation of more complex device structures. Further investigation into the different layers within these p-i-n structures should lead to even higher efficiencies, e.g the use of different n-type substrates with better lattice matching, the use of graded $Cd_{1-x}Zn_xTe$ and $Cd_{1-x}Mn_xTe$ layers and the possibility of using highly conducting p-ZnTe as the p-type window layer or even a thin layer of HgTe as a transparent contact [66]. Chapter 8 describes the investigation into some of these effects and the results they produced.

2.4 Heterojunction Theory

2.4.1 Introduction

This section describes the theoretical background required for understanding the operation of p-n and p-i-n heterojunctions and their applications as solar energy convertors. Detailed analysis of heterojunction theory and its historical background is not presented, unless necessary i.e in the case of current-transport mechanisms. This section attempts to develop a qualitative picture of the device concepts and junction characteristics involved whilst only using mathematical expression when necessary. Generally these expressions are only introduced when they will be used in the subsequent interpretation of results in later chapters.

Section 2.4.2 describes the formation of energy band diagrams for these heterojunctions and their interpretation in terms of interface states. Section 2.4.3 goes on to describe the detailed current-transport analysis for the interpretation of dark current-voltage characteristics at various temperatures, and subsequent sections describe the interpretation of C-V and spectral response data in terms of both p-n and p-i-n devices. Finally section 2.4.6 considers the formation of ohmic contacts to the p- and n-type semiconductors, and their importance in solar cell devices.

2.4.2 Formation of energy band diagrams

A heterojunction is an electrical contact between two different semiconducting materials. Junctions can either be abrupt (i.e where there is a sudden change in material properties across the interface) or graded where there is a gradual change in composition across the interface. If the semiconductors have the same type of conductivity then the junction is termed an isotype, otherwise it is referred to as an anisotype. Heterojunctions have been extensively reviewed by Milnes and Feucht [67], Sharma and Purhoit [68] and Chopra and Das [69]. The construction of the energy band diagram for the heterojunction proceeds by first drawing the energy diagrams of the two materials separately as in figure 2.8(a) for n-CdS/p-CdTe with the vacuum energy in common. As the materials are brought into

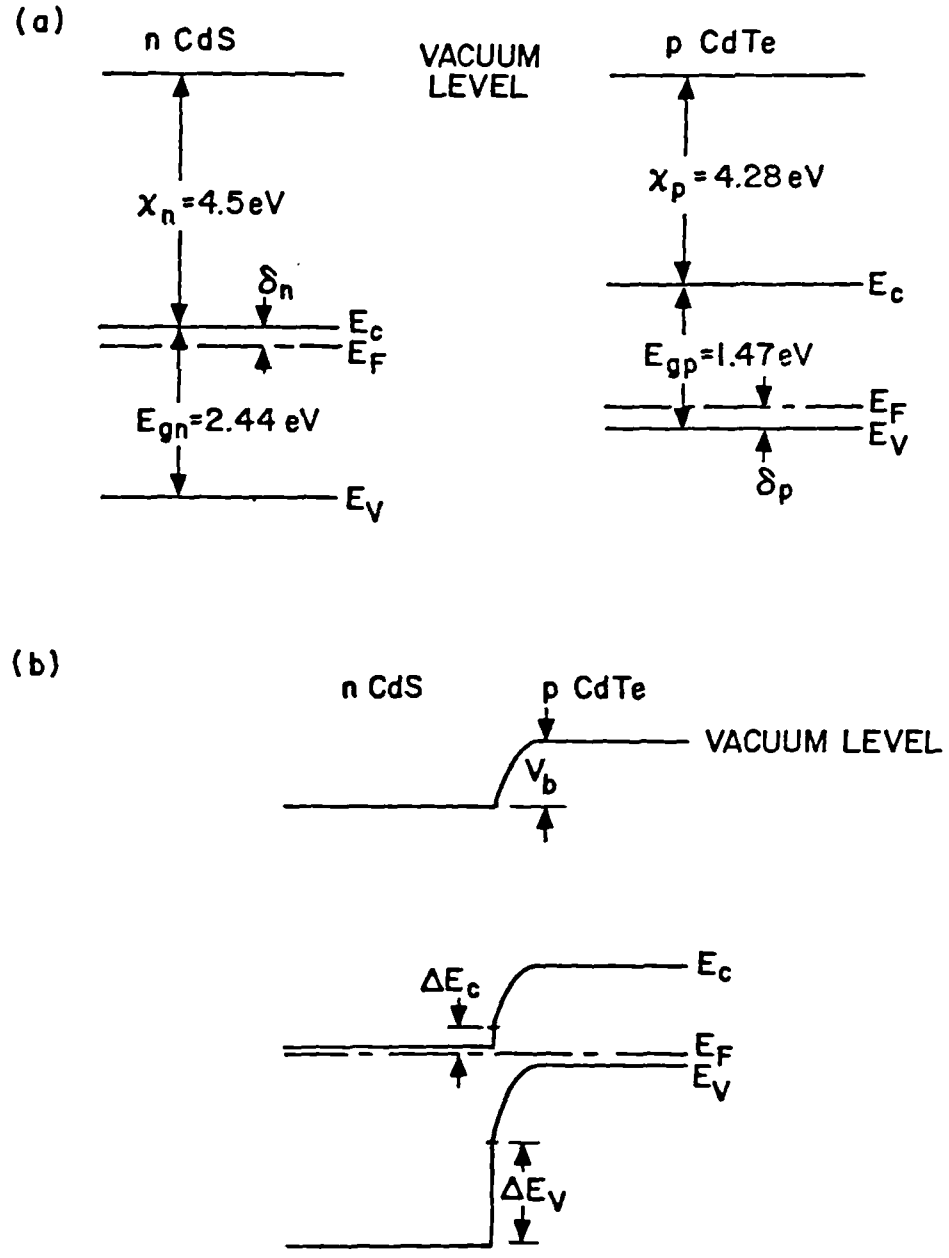

Figure 2.8 — Equilibrium energy band diagram for the CdS/CdTe heterojunction before (a) and after (b) the formation of an abrupt p-n junction

contact there is an equalisation of the Fermi level and it is necessary for a number of electrons to pass from the CdS to the CdTe (for the case where $\rho_{CdS} > \rho_{CdTe}$). This displacement of the electrons at the interface bends the E_c and E_v levels in the CdTe to give the formation of the abrupt heterojunction in figure 2.8(b). Each semiconductor is characterised by its electron affinity, χ, band gap, E_g and work fuction ϕ. For an ideal junction, i.e ignoring interface states and dipoles the barrier height, V_b to electron flow is given by [70,71].

$$V_b = E_{g,p} + \Delta E_c - \delta_n - \delta_p \qquad [2.9]$$

where ΔE_c is the conduction band discontinuity, $E_{g,p}$ is the band gap of the p-type material and δ_n,δ_p are the displacements of the Fermi level from the conduction band edge and valence band edges in the CdS and CdTe materials respectively.

$$\Delta E_c = \chi_p - \chi_n \qquad [2.10]$$

and

$$\Delta E_v = (E_{g,n} - E_{g,p}) - \Delta E_c \qquad [2.11]$$

Where $E_{g,n}$ is the band gap of the n-type material, and χ_n and χ_p are the electron affinities of the n and p-type materials respectively. The discontinuity in the value of ΔE_c, if large could limit the electron injection and allow recombination at the interface to dominate the current flow.

2.4.3 Current-transport mechanisms

In forward bias there are three mechanisms that give rise to current transport and these are represented as A, B and C in figure 2.9, where

A-injection : electrons are injected from the conduction band of the n-type material over the potential barrier to the p-type material where they diffuse/drift

away from the junction. Similarly there will be hole injection from the valence band of the p-type material into that of the n-type material.

B-space-charge recombination region : whilst injection is occurring carriers can recombine in the depletion region resulting in an increase in the dark current through the device. This space-charge region recombination current was first described by Sah et al [72].

C-tunneling : the third mechanism of dark current transport is a tunneling current caused by electrons or holes tunneling from the conduction or valence bands into energy levels within the band gap, accompanied either by further tunneling or by recombination into the opposite band.

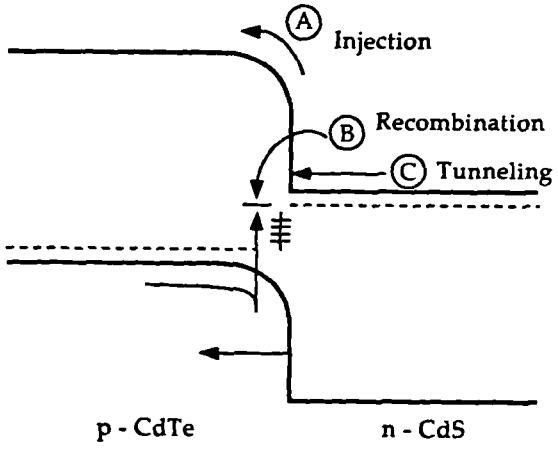

Figure 2.9 — Current-transport mechanisms in forward biased p-n junctions

The major differences between the injection and space-charge recombination currents lie in their voltage, temperature and band gap dependencies. The injection and space charge currents vary as $\exp\left(\frac{qV}{nKT}\right)$ and $\exp\left(\frac{qV}{2nKT}\right)$ respectively, whilst the dependance of I_o for the injection current is expressed as $\exp\left(\frac{E_g}{KT}\right)$ compared to $\exp\left(\frac{E_g}{2KT}\right)$.

The current-voltage relationship thus has to account for all three mechanisms, injection, space-charge and recombination, and tunneling. The contribution to the total current from the injection of holes into the wider band gap semiconductor is negligible because of the large energy barrier to hole injection arising from ΔE_v. When the n-type region is highly doped with respect to the p-type semiconductor the current-voltage equation simplifies to the standard diode equation (see section 2.1.3) given by

$$I_f = I_o \left[exp\left\{ \frac{q(V - IR_s)}{kT} \right\} - 1 \right] + \frac{V - IR_s}{R_{sh}} \qquad [2.4]$$

For an ideal diode $R_{sh} \rightarrow \infty$, $R_s \rightarrow 0$ and

$$I_f = I_o \left[exp\left\{ \frac{qV}{kT} \right\} - 1 \right] \qquad [2.12]$$

An expression for the recombination current was derived by Mitchell [70] and is given by

$$I_f = I_{oo} \left[exp\left\{ \frac{qV}{nkT} \right\} - 1 \right] \qquad [2.13]$$

The diode factor, n lies between 1 and 2 and is a function of the ratio of the densities of imperfections in the two semiconductors, whilst I_{oo} is a weak function of temperature.

The current-voltage characteristics of an abrupt heterojunction where tunneling is the dominant transport mechanism [73] are described by

$$I_f = I_{oo}(T)\ exp\ (BT)\ exp\ (AV) = I_o(T) exp\ (AV) \qquad [2.14]$$

where A is the tunneling constant and B gives the temperature dependence. The temperature and voltage dependence of I_f are separable, such that a plot of ℓn I_o with temperature gives a straight line relationship of slope B. I_o(T) is determined from the extrapolated intercept of the ℓn I_f-V characteristic and bears

an exponential dependence on the built-in potential, V_d (determined from C-V measurements) of the junction through

$$I_o\,(T) \;=\; I_t\; exp\;(-AV_d\;(T)) \qquad [2.15]$$

where I_t is a constant proportional to the density of traps of appropriate energy in the CdTe depletion region [74]. The values of A can be determined from the slopes of ℓn I_f-V curves. Thus by plotting I_f versus voltage characteristics at different temperatures the current transport mechanism can be determined. It has been found that the current transport across the heterojunction can be dominated by any one of these three mechanisms. If a plot of ℓn I_f versus temperature gives a constant value of n then the mechanism is either one of injection or space-charge recombination depending on the value of n, however if the value is variable but the value of A remains constant then this mechanism has been superseded by tunneling.

In the case where the carrier concentration is too low to allow simple tunneling ($\approx 10^{16}$ cm^{-3}) then a multistep tunneling model has to be considered [75]. Franz [75] proposed that, for this situation, the forward current density, J_f, could be expressed by the following equation

$$J_f \;=\; \tau\;\psi\;N_t\;exp\;(-\alpha R^{-(\frac{1}{2})}\;(V_d - KV)) \qquad [2.16]$$

where τ is a constant, $\alpha = \left(\frac{\pi}{4h}\right)\left(\frac{m_n^*\epsilon_p}{N_A}\right)^{\frac{1}{2}}$, N_t is the density of tunneling/ recombination centers in the space-charge region, ψ is the transmission coefficient for the electrons to cross the interface, $K = [1 + \left(\frac{\epsilon_p N_A}{\epsilon_n N_D}\right)]$, m_n^* is the electron effective mass, ϵ_p and ϵ_n are the dielectric constants of the CdTe and CdS respectively, N_A and N_D are the net ionised charge density on each side and R is the number of steps required to traverse the depletion region.

It can be seen that this equation is equivalent to equation 2.14, where B represents the temperature dependence introduced by the change of V_d with temperature. Combining these two equations and collecting like terms (see appendix A),

the value of the number of steps required to traverse the depletion region, R, is given by

$$R = \left(\frac{K\alpha}{A}\right)^2 \qquad [2.17]$$

and the fractional energy change for each step, S [74] is calculated from

$$A = \frac{d\ell n\, I_f}{dV} = \frac{4}{3h}\left(\frac{m^*\,\epsilon_p\,S}{N_A}\right)^{\frac{1}{2}} \qquad [2.18]$$

leading to a total barrier height of R.S to electron flow across the junction.

The reverse dark I-V characteristics can also be expressed in terms of a tunneling or multistep tunneling/recombination mechanism. The value of the reverse bias saturation current can be reformulated as

$$I_o(T) = I_{oo}\, exp\,(BT) \qquad [2.19]$$

where B is a measure of the variation of V_d with temperature. For multistep tunneling the reverse current density is given by

$$\ell n\left(\frac{J_r}{V}\right) = -\alpha[E_{gp} + \Delta E_V]\left(\frac{E_r}{V_d - V}\right)^{\frac{1}{2}} \qquad [2.20]$$

where J_r is the current density in the reverse direction, E_r is the effective barrier for one tunneling step, ΔE_V is the valence band offset and E_{gp} is the band gap of the CdTe. The gradient of $\ell n\left(\frac{J_r}{V}\right)$ versus $(V_d - V)^{-\frac{1}{2}}$ given by Γ is

$$\Gamma = -\alpha(E_{gp} + \Delta E_v)E_r^{\frac{1}{2}} \qquad [2.21]$$

Thus from the gradient Γ the value of E_r can be calculated which can then be used to calculate the number of steps required to traverse the depletion region, S_r where

$$S_r = \frac{(E_{gp} + \Delta E_v)}{E_r} \qquad [2.22]$$

Finally from the reverse bias characteristics and using the value of Γ the trap density, N_t can be determined which can aid explanation of interface state density.

$$J_r V^{-1} exp[\Gamma(V_d - V)^{\frac{1}{2}}] = q^2 a N_t h^{-1} \qquad [2.23]$$

Adirovich et al [76] found that there were generally two regions in most I-V characteristics with temperature, corresponding to two different transport mechanisms. At low temperatures and voltages a recombination/diffusion process dominated but at high temperatures this was superseded by multistep tunneling/ recombination. The occurrence of tunneling within these device structures confirms the presence of a high density of defects/traps in the depletion region that are effective tunneling centres.

2.4.4 Junction capacitance

There are two types of capacitance associated with a junction
(i) the junction capacitance due to the dipole in the transition region and
(ii) the charge stored capacitance arising from the lagging behind of the voltage as the current changes due to charge storage effects.

The junction capacitance is dominant under reverse bias conditions and vice versa, knowledge of both providing information about the structure of the p-n junction. By measuring the capacitance of the heterojunction as a function of the voltage, the value of the diffusion voltage, V_d can be found. The diffusion voltage is the difference in work functions of the two materials which in turn is equal to the sum of the partial built-in voltages V_{d1} and V_{d2} which represent the electrostatic potentials at equilibrium.

Instead of the common expression $C = |\frac{Q}{V}|$ which applies to capacitors in which charge is a linear function of the voltage a more general expression must be used

C=$|\frac{dQ}{dV}|$, since the charge, Q on each side of the transition region varies non-linearly with the applied voltage. The equilibrium value of W (the width of the depletion region) is found to be [77]

$$W = \sqrt{\frac{2\epsilon\,(V_d - V)}{q}\left(\frac{N_a + N_d}{N_a N_d}\right)} \qquad [2.24]$$

The capacitance is given by

$$C = |\frac{dQ}{d(V_d - V)}| = \frac{A}{2}\sqrt{\frac{2q\epsilon}{(V_d - V)}\frac{N_d N_a}{N_d + N_a}} \qquad [2.25]$$

where N_d and N_a are the donor and acceptor concentrations and ϵ is the dielectric constant of the p-type material. In the case of n-CdS/p-CdTe the CdTe is highly self-compensating and is difficult to obtain with a high doping concentration, the heterojunction is therefore more heavily doped on one side than the other such that $N_d >> N_a$ and equation 2.26 can be rewritten as

$$\frac{C}{A} = \sqrt{\frac{q\epsilon N_a}{2}\frac{1}{(V_d - V)}} \qquad [2.26]$$

Thus the net acceptor density, N_a can be calculated from the slope of the $\frac{C(V)}{A}^{-2}$ versus applied voltage. The depletion layer width of the heterojunction can be determined from

$$W(V_o) = \frac{\epsilon A}{C(V_o)} \qquad [2.27]$$

Donnelly and Milnes [78] however considered that the junction capacitance is affected by the inclusion of interface states and the presence of a dipole. The resulting junction capacitance is then expressed as

$$C = \sqrt{\frac{q\epsilon N_a N_d}{2N_a + N_d}}(V_d - V - \delta - BQ_1^2)^{-\frac{1}{2}} \qquad [2.28]$$

where B=$[2q\epsilon(N_a+N_d)]^{-1}$, Q_1 is the charge on the interface states (C/cm^2) and δ is the electric dipole moment.

The introduction of interface states and dipoles essentially gives the same slope of the $C(V)^{-2}$ versus applied voltage as before but the voltage intercept is shifted to a different value given by

$$V_i = V_d - \delta - \frac{Q_1^2}{2q\epsilon(N_a + N_d)} \qquad [2.29]$$

The occurence of a linear variation in plots of C^{-2} versus V at reverse bias confirms the formation of an abrupt junction, whilst the slope gives values of the doping concentration in the less doped sample. The measured value of the capacitance cut-off voltage will be different from the true diffusion potential, V_d by an amount which accounts for the electric dipole at the surface and the interface states.

2.4.5 Spectral response

Incident photons on the CdTe absorber layer create electron-hole pairs which are then separated by the internal potential in the solar cell. Only the carriers passing through the junction contribute to the light current in the external circuit. The collection of these photocarriers is however impeded by a recombination mechanism introduced by the junction interface states created by thermal or lattice mismatch or defects introduced during fabrication.

The absorption of light in the CdTe is described by

$$\Phi(x, \lambda) = \Phi_o(\lambda) exp[-\alpha(\lambda)x] \qquad [2.30]$$

where $\Phi(x, \lambda)$ is the photon flux available at a distance, x beneath the surface, $\Phi_o(\lambda)$ is the photon flux entering the CdTe (photons cm^{-2} sec^{-1}), and $\alpha(\lambda)$ is the optical absorption coefficient. Since Φ_o and α are functions of wavelength then so is Φ. Once created, the minority carriers have to travel through the bulk of

the CdTe, which has its characteristic minority carrier diffusion length, and the depletion region where the carriers are affected by the electric field and as such have a high diffusion length.

The total photocurrent arriving at the junction interface is the sum of the contributions from the depletion region and the bulk, giving

$$J_I(\lambda) = qa_o\Phi_o[1+\alpha(\lambda)L]^{-1}\ exp\ (-\alpha\ W(\lambda)) \qquad [2.31]$$

where a_o is the quantum efficiency for the absorbed light to produce electron-hole pairs (i.e one photon of light should generate one electron-hole pair). However interface states within the forbidden gap provide a recombination mechanism, described by

$$J_r = q\ C\ n_I \qquad [2.32]$$

where C is the interface recombination velocity and n_I is the density of minority carriers at the junction interface. Conservation of current at the interface means that J_I=J_r+J_L where J_L is the light current from the CdTe to the CdS, expressed as

$$J_L(\lambda) = qn_I(\lambda)\mu_e\epsilon \qquad [2.33]$$

where μ_e is the electron mobility and ϵ is the electric field at the junction interface. Thus

$$J_L(\lambda) = \left(1+\frac{C}{\mu_e\epsilon}\right)^{-1} J_I(\lambda) \qquad [2.34]$$

Thus the photogenerated minority carrier current reaching the CdS is given by

$$J_L(\lambda) = qa_o(\lambda)\Phi_o(\lambda)\left(1+\frac{C}{\mu_e\epsilon}\right)^{-1}[1+\alpha(\lambda)L]^{-1}\ exp\ (-\alpha(\lambda)\ W) \qquad [2.35]$$

which can be rewritten as

$$J_L(\nu) = q(\nu)a_o(\nu)\Phi_o(\nu)\ h(\nu)g(\nu) \qquad [2.36]$$

where

$$h(\nu) = \left(1 + \frac{C}{\mu_e \epsilon}\right)^{-1} \quad and \quad g(\nu) = [1 + \alpha(\nu)L]^{-1}\ exp\ (-\alpha(\nu)\ W) \qquad [2.37]$$

where g(ν) represents the fraction of photogenerated minority carriers arriving at the junction and h(ν) represents the fraction of photogenerated minority carriers that pass safetly through the junction on reaching it. The product of these two values is called the collection term. The collection of these photogenerated carriers can be described by the product of a generation term (the number of carriers produced by the absorption of light) and a carrier collection term (the fraction of carriers being transported). If the CdS is heavily doped compared to the CdTe then the depletion region exists almost entirely in the CdTe and

$$W = \sqrt{\frac{2\epsilon(V_d - V)}{qN_a}} \qquad [2.38]$$

For large values of the absorption coefficient g(ν)$\rightarrow$1.0 and is insensitive to the values of L and W.

A particular form of the spectral response Q(λ) of a solar cell is its quantum efficiency, the ratio of photocarriers collected at a given photon energy to the number of incident photons

$$Q(\lambda) = \frac{J_L(\lambda)}{q\Phi_o(\lambda)} \qquad [2.39]$$

$$Q(\lambda) = a_o H(\nu) \qquad [2.40]$$

where H(ν)=g(ν)h(ν) and $a_o(\nu)$ is the quantum efficiency of absorbed light to produce an electron-hole pair which is assumed to be 1. Thus

$$Q(\nu) = g(\nu)h(\nu) = \left(1 + \frac{C}{\mu_e \epsilon}\right)^{-1} [1 + \alpha(\nu)L]^{-1} \, exp\,(-\alpha(\nu)\, W) \qquad [2.41]$$

where

$$\Phi_o(\lambda) = \Phi_s(\lambda)(1 - R(\lambda)) \qquad [2.42]$$

and $\Phi_s(\lambda)$ is the photon flux to the cell and R(λ) is the overall reflection loss.

Thus the quantum efficiency is voltage dependent and the measured quantum efficiency versus applied voltage is useful in clarifying the details of photocarrier collection. For the CdS/CdTe solar cell the short wavelength cut-off of the spectral response is defined by the sharp absorption edge of the CdS and the shape of the long wavelength edge by the collection of photocarriers from the CdTe given by H(ν). The CdS is sufficiently thick that light absorbed within it does not contribute to the photocurrent.

2.4.6 Ohmic contacts

Ideal, ohmic metal semiconductor contacts occur when the charge induced in the semiconductor in aligning the Fermi levels is provided by the majority carriers. When a metal is brought into intimate contact with a semiconductor the type of electrical barrier that results is a function of the difference in work function, ϕ_m of the metal and ϕ_s of the semiconductor. For a metal contact to be ohmic to an n-type semiconductor (see figure 2.10) ϕ_m should be less than that of the semiconductor ϕ_s and for $\phi_m > \phi_s$ the barrier will increase linearly according to the work function difference. Conversely, for a metal contact to be ohmic to a p-type semiconductor $\phi_m > \phi_s$.

However, for most semiconductors ohmic contacts are not obtained even by the proper choice of work function due to interface states. For these cases a heavily doped semiconductor region between the metal and the bulk semiconductor is used.

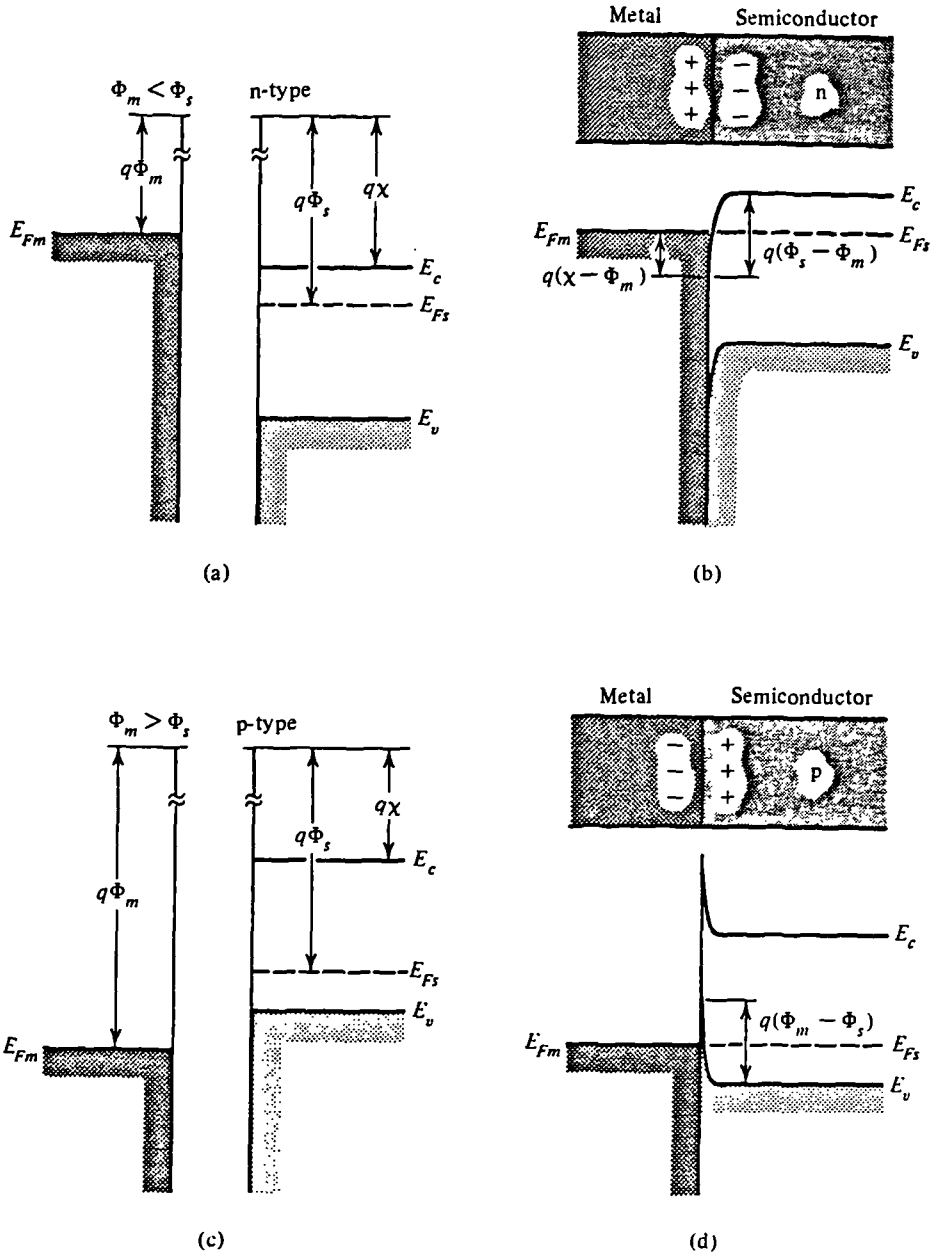

Figure 2.10 — Ohmic metal-semiconductor contacts for (a) n-type semiconductor and (b) p-type semiconductor showing equilibrium band diagrams before and after formation

This provides a thin depletion width through which quantum mechanical tunneling can easily take place. For a detailed analysis of ohmic contact formation see Milnes and Feucht [67]. In this thesis contacts were vacuum evaporated and then annealed in nitrogen. This annealing treatment encourages diffusion of the contact into the semiconductor, so providing a heavily doped surface through which tunneling can take place. The difficulties encountered in making contacts to p-CdTe and p-ZnTe, a major problem with the solar cell devices, is discussed in more detail in section 5.6.

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Chapter III

Characterisation of device structures

3.1 Introduction

The evolution of MOVPE growth technology has led to the production of high purity and complex devices structures. In turn this has created new challenges for the characterisation of materials and the evolution of new techniques to meet these challenges. This chapter describes the different characterisation techniques employed for the analysis of MOVPE grown epilayers and single crystal substrates. Section 3.2 discusses the various structural assessment techniques used including reflection high energy electron diffraction (RHEED), transmission electron microscopy (TEM), x-ray techniques and scanning electron microscopy (SEM) to analyse the surface morphology. SEM is considered important since the thicknesses of the epilayers are such that the conditions of the surfaces can easily influence or even dominate the current-transport properties.

Section 3.3 describes the electrical assessment techniques used to characterise the devices formed, including current-voltage (I-V), capacitance-voltage (C-V), spectral response, photocapacitance, photoluminescence, and Hall and resistivity measurements.

3.2 Structural Assessment

3.2.1 Reflection high energy electron diffraction (RHEED)

RHEED is a non-destructive technique which provides information on the crystal orientation and perfection of surfaces. It also enables the identification of surface films and has the ability to assess the degree of preferred orientation of any crystallites present at the surface. The technique employs a monoenergetic beam of electrons with an energy in the range 10-100 keV to obtain a diffraction pattern from the atomic planes at the surface of a crystalline specimen. The wavelength of

the electron beam, λ, corresponding to an accelerating voltage, V (given in volts), is given by the following expression [1]

$$\lambda = \sqrt{\frac{150}{V(1+10^{-6}V)}} \qquad [3.1]$$

where λ is in Angstroms. Thus for the given energy range 10-100 keV the associated wavelength of the electrons varies from 0.12-0.04 Å. Since the interplanar spacing in most semiconductors is $\approx$ 4Å only those crystal planes inclined at less than a few degrees to the surface of the specimen will diffract the electron beam (from Bragg's Law) and this is represented in figure 3.1.

An incident beam strikes the crystal plane $[h,k,l]$ at the Bragg angle, θ to form a diffraction spot, P on the photographic plate placed at a distance L from the sample. Thus from simple geometry,

$$R_{hkl} = L\ tan\ 2\theta \qquad [3.2]$$

$$R_{hkl} = 2L\ sin\ \theta \approx 2L\theta \qquad [3.3]$$

since sin $\theta \approx \theta$ for small angles. Combining these equations with the Bragg equation gives

$$\lambda \cong \frac{R_{hkl}d_{hkl}}{L} \qquad [3.4]$$

where d_{hkl} is the interplanar spacing and L is the camera length, and λ is the wavelength of electrons. The value of L is determined with reference to a standard specimen of known crystal structure and lattice parameter. RHEED can determine the amount of crystalline order, the crystal structure and interplanar spacing from the geometry of the pattern obtained. The nature of the specimen surface can be inferred from the shape of the diffraction spots, whilst the crystal quality of the surface layer can be assessed from the sharpness of the Kikuchi lines, described

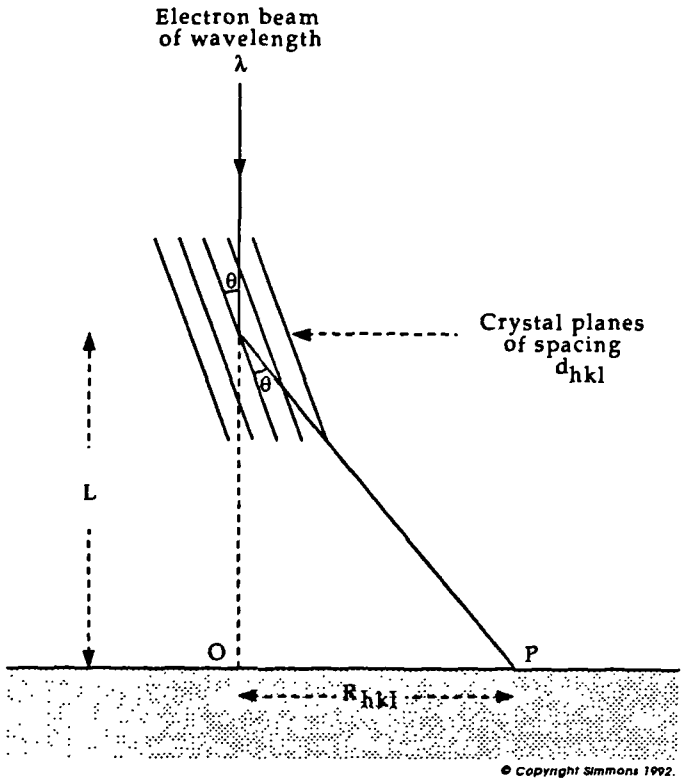

Figure 3.1 — Analysis of crystallinity using RHEED

later. By analysing the intensities of the diffracted beams the contents of the unit cell can be determined. The technique is versatile and easily performed and in all cases was used routinely to assess the surface quality. Where necessary detailed analysis of RHEED patterns was carried out to determine different crystalline structures (see section 4.4).

If the surface consisted of a large number of randomly oriented crystallites (i.e a polycrystalline sample) the diffraction spots became continuous rings. Measurement of the radii of these diffraction rings enabled the interplanar spacing for each ring to be calculated from equation 3.4, knowing the value of L. The next level of crystalline order occurs when crystallites or "grains" have a preferred common

orientation. This frequently occurs with single crystal surfaces that have been polished. In such cases the length of the arcs gives an indication of the misorientation of the grains. Single crystal samples give rise to spot patterns, the geometrical arrangement of which permits the evaluation of the crystal structure, whilst a quantitative assessment of the surface is inferred from other diffraction features such as the presence of Kikuchi and streak patterns.

Diffraction from reasonably flat single crystals with good lattice perfection gives rise to Kikuchi patterns. The origin of these patterns is fully discussed in a recent review article by G.J. Russell [1], but as with spot patterns they can be used for indexing crystal orientations by direct comparison with a reference pattern. The sharpness of the pattern provides a qualitative indication of the extent of crystalline perfection. Streaked patterns where the diffraction spots are elongated in a direction perpendicular to the sample surface are also obtained from very flat surfaces of single crystals. This is because a proportion of the beam striking the surface at grazing incidence will only penetrate to a depth of a few atomic layers resulting in poor resolution of the diffracted beam intensity perpendicular to the sample surface. This causes the reciprocal lattice points to be extended in this direction where the elongation is symmetrical about the position of the reciprocal lattice point.

Thin lamellar twins lying in a low index plane of a crystal lattice cause extension of the reciprocal lattice points in a direction perpendicular to the fault plane. The effect on the diffraction pattern is to produce more or less continuous streaks of intensity passing through the diffraction spots in these directions.

Thus it can be seen that RHEED is very dependent on the surface topography of the sample and whilst invaluable as an assessment technique is inferior to transmission electron diffraction (TED) due to the uncertainty in the camera length. In the case of TED the electron beam passes through a very thin specimen ($\approx$ 1000Å) leaving little uncertainty in camera length whereas the region contributing to the RHEED pattern may extend over several mm. The inherent problem with TED is that samples have to be thinned down to $\approx$1000Å both a costly and time consuming process.

3.2.2 Laue X-ray back reflection

Orientation of single crystals involves the determination of unknown orientations prior to setting the sample in the desired orientation. Laue back reflection allows the orientation determination of thick samples without requiring any special sample preparation. The experimental set up is shown in figure 3.2.

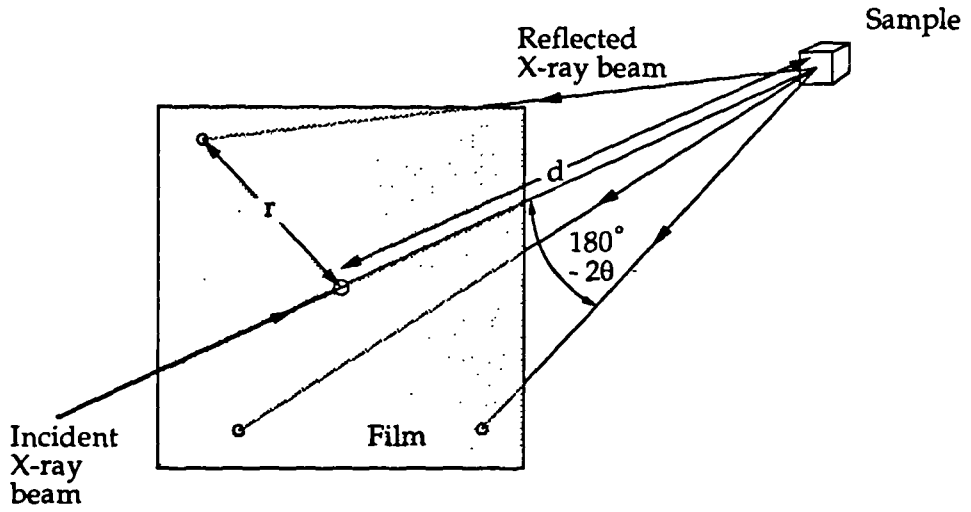

Figure 3.2 — Crystal orientation by Laue x-ray back reflection

The x-ray source produces a beam of x-rays with a wide range of wavelengths which are then collimated onto the sample surface using a filter of known wavelength. A flat photographic film is placed perpendicular to the incident beam between the source and the sample to record the reflected diffracted beam. After taking a Laue back reflection pattern from a sample a major spot on the pattern is located, corresponding to a strong reflection. The crystal is then tilted on its goniometer such that this reflection forms the centre of the next Laue pattern. From comparing the patterns with stereographic projections and calculating angles between unknown planes and low index planes the unknown orientation can be determined uniquely. Using the same process predefined orientations can be determined and aligned.

3.2.3 X-ray diffractometry

When a collimated, monochromatic beam of x-rays is incident on a crystalline material the resulting diffracted beams will follow directions given by Bragg's law. Thus if a narrow acceptance angle detector (i.e fitted with appropriate collimating slits) is used, the angle of a given diffracted beam can be measured directly. Scanning the detector over a range of angles wil map the diffracted rays in that region of angular space. A Geiger counter is driven at a constant angular velocity through increasing values of 2θ until the whole angular range is scanned. The counter and specimen are mechanically coupled so that a rotation of the counter through 2θ degrees is automatically accompanied by a rotation of the specimen through θ degrees. This coupling ensures that the angle of incidence and reflection from the flat single crystal surface will always be equal to one another and equal to half the total angle of diffraction, an arrangement necessary to preserve focusing conditions. The counter is connected to an automatic recorder which gives a record of intensity versus diffraction angle, 2θ. Diffractometers scan over two dimensions, giving in effect, a slice of the diffraction sphere. Thus for polycrystalline samples where diffraction is over concentric circles the slice will intersect every diffraction circle. For single crystal samples the diffraction is into narrow solid angles and only those diffracted rays that lie within the source-sample detector plane will be detected. Thus in these cases, the orientations of the sample with respect to the incident x-ray beam becomes important. Using x-rays of known wavelength the value of the lattice parameter, a, can be determined from the value of θ. For a cubic crystal

$$d^2 = \frac{a^2}{(h^2 + k^2 + l^2)} \qquad [3.5]$$

where d is the interplanar spacing. Thus, knowing d from the value of θ (using Bragg's Law) the value of a can be determined [2].

3.2.4 Double crystal x-ray diffraction

Double crystal x-ray diffractometry involves the sequential diffraction of x-rays from reference and specimen crystals. The wavelength of the x-rays is comparable to the interplanar spacings of the semiconductor and the penetration depth of the x-rays is much greater than that of the electron beam in RHEED. A reference crystal of extremely high quality is used, so that the diffraction from the specimen has a high angular resolution. A "rocking curve" of the specimen is recorded by rotating the specimen about an axis normal to the diffraction plane and the scattered intensity produced is recorded as a function of the specimen angular setting (see figure 3.3).

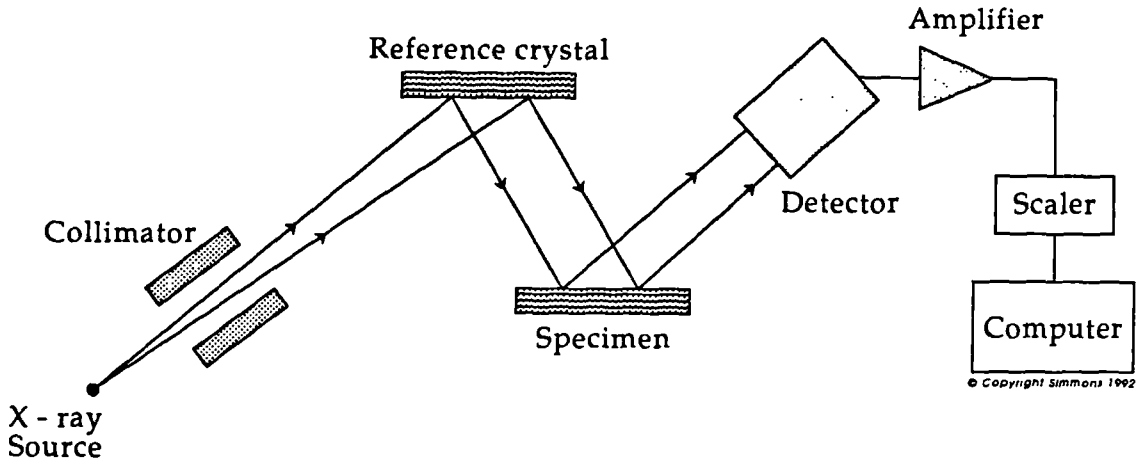

Figure 3.3 — Double crystal x-ray diffraction

The full width at half height maximum (FWHM) of the rocking curve provides a measure of the epilayer perfection. Any low angle grain boundary or dislocation will lead to variations in the lattice parameter and thus broadening of the diffraction pattern. More detailed analysis of the rocking curve data can provide information on the lattice mismatch and composition, layer thickness, wafer curvature and compositional variation across the epilayers [3]. For the most part in this thesis measurements were made to identify the layer perfection using FWHM measurements, since lattice mismatches were already known.

3.2.5 Scanning electron microscopy (SEM)

The surface morphologies of all layers was routinely assessed using a Cambridge Instruments scanning electron microscope S600. The two main components of the SEM are the electron optical column, including the gun, electromagnetic lenses and specimen chamber, and the display unit (see figure 3.4).

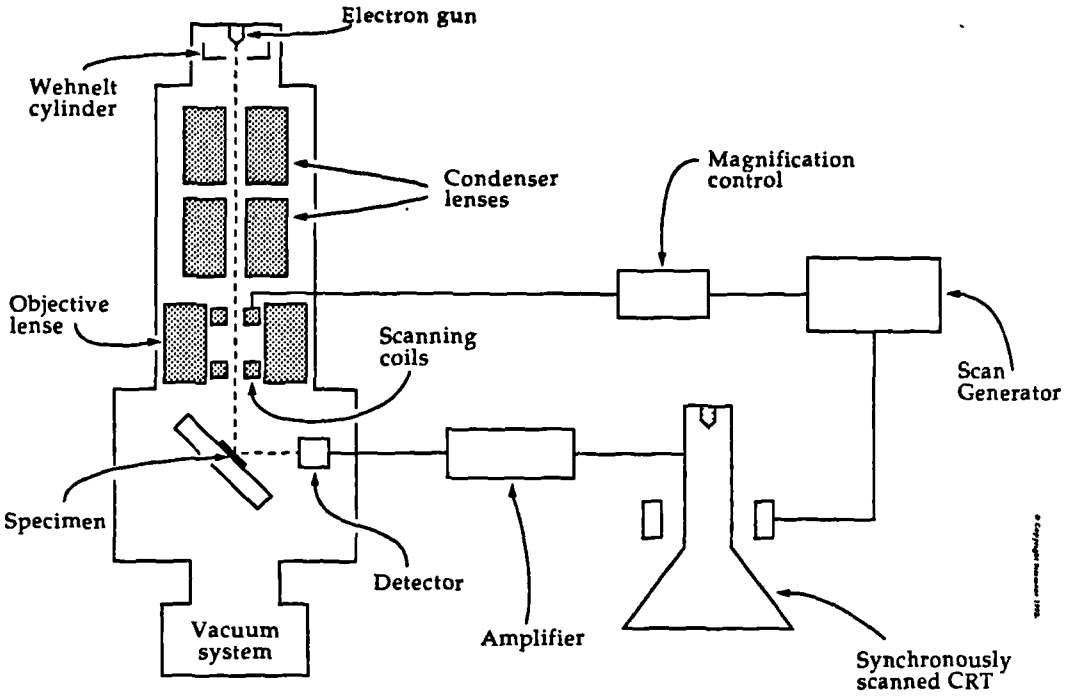

Figure 3.4 — Diagrammatic representation of the SEM

A heated tungsten cathode is maintained at a high negative potential, ≈1 KV to a Wehnelt cylinder. Two condenser and an objective lens are used to form a fine electron beam which is focussed on the specimen surface. A variety of signals are produced as a result of the dissipation of the electron beam energy in the sample into other forms of energy. These may then be detected and turned into electrical signals by means of suitable detectors. The electrical signals are amplified and fed to a grid of a synchronously scanned display cathode ray tube (CRT). The

raster scan of the electron spot over the specimen surface results in a one to one correspondence between the points on the display CRT screen and the points on the specimen. Thus the variation in the strength of the signal is recorded as a variation in brightness on the CRT screen and hence contrast on the micrographs. Different forms of physical energy from the electron bombardment of the samples are used as signals for the modes of operation of the SEM including

(1) Emitted electrons from the sample surface produce signals for the emissive mode. These secondary electrons have energies <50 eV and provide topographical contrast from within about 50Å of the surface.
(2) X-rays are emitted and form the basis of electron dispersive analysis by x-rays (EDAX). Here the presence of elements with a density of $>10^{18}$ cm^{-3} are detected within a spatial resolution of 1 μm. Quantitative analysis was not available on this machine, but was provided by Mrs. O.D. Dosser at RSRE, Malvern.
(3) Ultraviolet, visible and near infrared photons are the basis of the cathodoluminescence mode or
(4) The currents or voltages are the signals for the conductive, electron beam induced current (EBIC) mode. The EBIC mode of the SEM investigates the electrically active areas within the semiconductor. This technique can be used to measure transport properties such as minority carrier diffusion lengths, lifetimes and surface recombination velocities. In this mode the incident electron beam generates electron hole pairs which are separated by the internal electric fields within the sample. The electron beam is scanned across the sample and areas where preferential recombination takes place, such as the misfit dislocation region at the interface show a reduction in the short circuit current. The separated charge carriers are collected, amplified and applied to the z-modulation of the CRT display.

In the case of p-n junctions or Schottky diodes the EBIC mode of the SEM can thus be used to measure the minority carrier diffusion length by measuring the EBIC current as a function of beam distance, x, from the junction on both sides. The value of the current, I at a distance, d from the junction is given by

$$I(d) = A\, e^{-\frac{d}{L}} \qquad [3.6]$$

where L is the minority carrier diffusion length and A is a constant. Thus a plot of ℓn I(d) versus d will give a straight line of gradient $-\frac{1}{L}$.

3.2.6 Transmission electron microscopy

Routine assessment of epitaxial films by TEM whilst valuable was not possible due to the difficult and time consuming process of preparing specimens thin enough ($\approx$ 1000Å) for the transmitted electrons to be detected and analysed. Representative specimens of all samples were taken and analysed in a JEOL 100CX STEM microscope operating at 100kV.* In order to view the epilayer/substrate cross-section samples were mechanically polished parallel to the interface down to 50-70μm thickness. Samples were then thinned to transparency by iodine reactive ion sputtering [4].

TEM analysis provides an assessment of the microstructural defect content of the epitaxial layers. Due to the high resolution ($\approx$ 10Å), dislocations, stacking faults, grain boundaries, and twin boundaries may all be seen directly, the quality of the image being improved in dark imaging mode where only the diffracted beams from the particle of interest are allowed to recombine to form the image.

3.2.7 Photoluminescence

When a solid is supplied with an amount of energy it may emit photons in excess of any thermal radiation. This process is called luminescence the various types of luminescence are categorised depending on the source of excitation. Photoluminecsence (PL) employs photon excitation, whereas cathodoluminescence for example employs the excitation by energetic electrons or cathode rays. Luminescence in semiconductors is generally described in terms of the radiative recombination of electron-hole pairs often involving transitions between states in the conduction or valence band and other localised states within the band gap including donors and acceptors. Figure 3.5 describes a simplified set of radiative transitions that lead to emission in semiconductors containing impurities.

* Samples were analysed by Dr.P.D. Brown, University of Durham

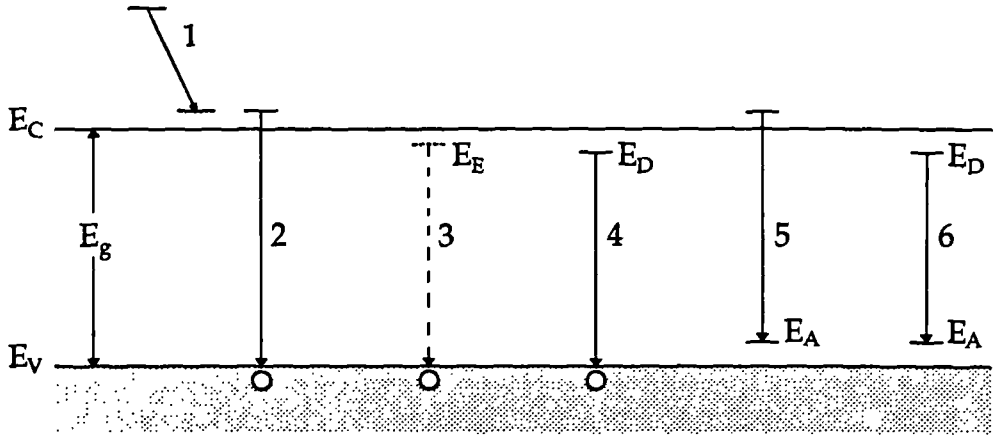

Figure 3.5 — Schematic diagram of radiative transitions between the conduction band (E_c), the valence band (E_v), and exciton(E_E), donor (E_D) and acceptor (E_A) levels in a semiconductor

Process 1 is an intraband transition, an excited electron well above the conduction band emits phonons in order to reach thermal equilibrium with the lattice.

Process 2 is an interband transition, giving intrinsic luminescence. A broad emission spectrum results however from the thermal distribution of carriers in states near the band edge.

Process 3 is the exciton decay where both free excitons (X) and excitons bound to an impurity undergo transitions. If it is the recombination of an exciton bound to a neutral donor it is denoted (D°,X), for an exciton bound at a neutral acceptor it is denoted (A°,X), whilst excitons bound to corresponding ionised impurities are (D^+,X) and (A^-,X).

Processes 4,5 and 6 arise from transitions involving impurity levels and are called extrinsic luminescence. The recombination processes between free carriers and trapped carriers of the opposite type are given by (D_o,h) for process 4, (e,A°) for process 5 and donor-acceptor pair (DAP) recombination for process 6. In order to distinguish between process 2 and processes 4 and 5 for shallow impurity transitions measurements are performed at liquid helium temperatures. Thus, PL studies allow the determination of the presence of impurity levels, especially deep levels which are known to affect device performance.

3.3 Electrical Assessment

3.3.1 I-V characterisation

The photovoltaic output characteristics of devices was measured under AM1.5 simulated illumination using a solar simulator experimental arrangement as described by Awan [5]. A 1.5 KW quartz halogen strip lamp with a parabolic reflector housing was mounted in a metal frame. The illumination passed through a 2 cm deep tray containing water, intended to simulate the infrared absorption due to water vapour of the atmosphere. A sample was mounted on a temperature controlled plate (25°C) where current-voltage characteristics were carried out using a high impedance Keithley voltage supply and an independent Hewlett-Packard ammeter. The solar simulator was calibrated to supply AM1.5 illumination, by adjusting the height of the sample below the light source, using a standard silicon PIN diode covering the wavelength range.

Detailed dark current-voltage measurements as a function of temperature were measured using the same circuitry, except that the sample was mounted in a DN1704 liquid nitrogen cryostat, maintaining temperatures between 77-500 K. Measurements were made at 0.05 V intervals in order to be able to observe any changes in the current transport mechanism with temperature. Independent voltage supplies were used to check the output voltage from the Keithley supply and an independent ammeter used to measure the absolute current. Samples were allowed time to establish equilibrium at different temperatures since the transport properties are known to be highly temperature dependent.

3.3.2 Capacitance-voltage measurements

Capacitance-voltage measurements not only enabled the determination of free carrier density but gave information on the interface state quality. Steady state photocapacitance was also used to provide information on the deep levels present in the devices.

Capacitance-voltage characteristics were measured manually with a Boonton 72B capacitance meter together with a Keithley voltage supply. Again the sample was mounted in a liquid nitrogen cryostat (type DN1704) to allow temperature dependent capacitance-voltage measurements to be made.

Steady state photocapacitance measurements were conducted at temperatures of 170 K to minimise thermal effects. The collimated light was provided by a tungsten light source and a Barr and Stroud double prism monochromator. The sample was left in the dark for a week to allow a steady state to occur before illumination. The monochromator was then changed from long to short wavelengths and the capacitance measured as a function of voltage at each wavelength.

3.3.3 Spectral Response

The spectral response of the solar cells produced was recorded over the wavelength range 0.4-2.0μm using a Barr and Stroud double prism monochromator. 'Spectrosil A' silica prisms were used to separate the light into its constituent wavelengths which were then collimated onto the sample surface. The light source consisted of a 250 W, 24 V quartz halogen lamp driven by a d.c stabilised power supply. An accurate recording of the spectral disribution of energy at the exit slit of the monochromator was made using a calibrated silicon PIN diode. A 50/50 beam splitter ensured that the light passing through the exit slit illuminated the same area of both the sample and the p-i-n diode, thus ensuring calibration of the photoresponse. The p-i-n diode response was amplified and passed through a comparator in a feedback loop where the current supply to the light source was readjusted to supply a constant photon flux at all wavelengths in the range 0.4-1.5μm (i.e within the p-i-n diode response). Measurements at longer wavelengths were made without the benefit of feedback control and therefore were not at constant flux. Figure 3.6 describes the experimental set-up where it can be seen that the device is mounted in a cryostat with a window for illumination. The solar cell was always illuminated in backwall mode and the temperature monitored.

A Keithley electrometer was used to measure the photovoltaic current and voltages, with an input impedance of 10^{14} ohms for the voltage measurements and

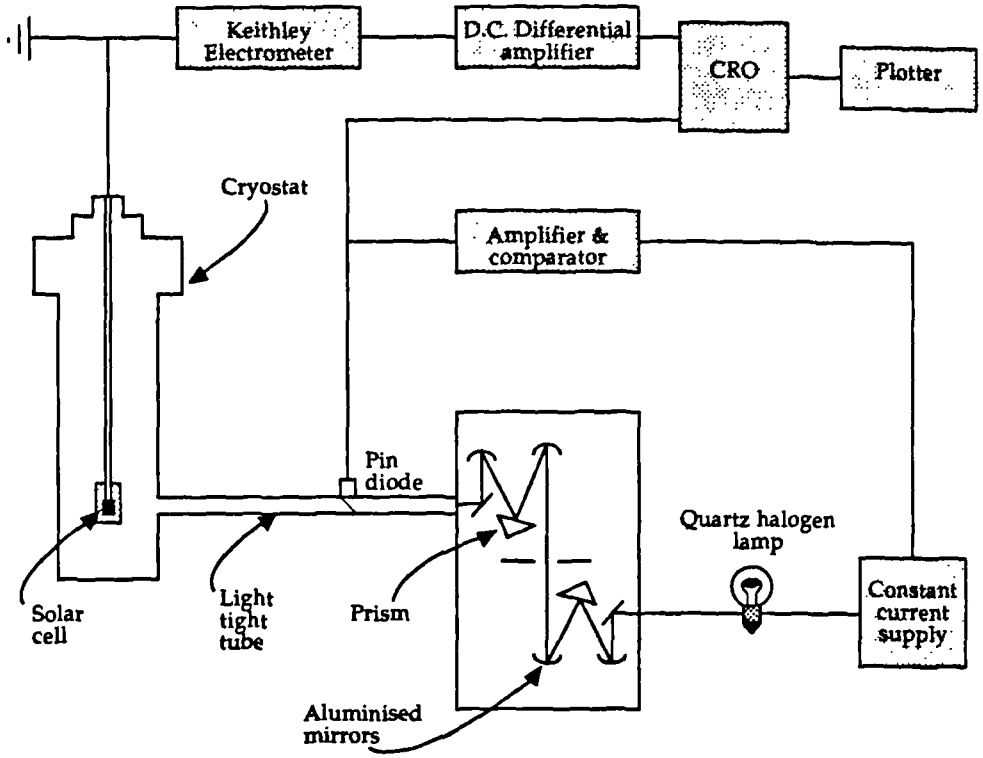

Figure 3.6 — Spectral response experimental set-up

very low impedance for current measurements. The outputs of the electrometer and the PIN diode were recorded on a LeCroy digital storage oscilloscope and downloaded where required to a Hewlett-Packard plotter. Quantum efficiencies were subsequently calculated from the light and sample responses, so that spectra were recorded as quantum efficiency versus energy. The same experimental set-up was also used to record photoconductivity spectra, used principally to characterise thin, resistive epitaxial layers. These spectra were used, mainly, as a means of determining the band gap energy in ternary $Cd_{1-x}Zn_xTe$ layers.

3.3.4 Hall effect and resistivity measurements

The measurement of the Hall effect (R_H) and resistivity (ρ) was necessary for all layers produced in order to be able to calculate carrier densities to aid the

interpretation of current transport and quantum efficiency measurements. Due to the different sizes of the substrates, and their subsequent layers, the Van der Pauw technique [6] was used to measure the values of R_H and ρ for layers of known thicknesses. Four point contacts labelled A,B,C and D of negligible size can be positioned (in principal) anywhere on the periphary of the sample enabling four different resistances to be measured, denoted by $R_{AB,CD}$ (where the current is applied between terminals A and B and the voltage measured across terminals C and D), $R_{BC,DA}$, $R_{CD,AB}$ and $R_{DA,CB}$ (see table 3.1). This has the advantage over the usual 4 point probe technique in that it is not necessary to know the other geometrical dimensions of the sample apart from the thickness which is generally easily measured. The resulting resistivity ρ, of the sample is given by any adjacent pair of resistances, i.e for $R_{AB,CD}$ and $R_{BC,DA}$

$$\rho = \frac{\pi\, d\,(R_{AB,CD} + R_{BC,DA})}{2\,\ell n 2}\, f\left(\frac{R_{AB,CD}}{R_{BC,DA}}\right) \qquad [3.7]$$

where d is the layer thickness and the function f satisfies the relationship

$$\frac{R_{AB,CD} - R_{BC,DA}}{R_{AB,CD} + R_{BC,DA}} = \frac{f}{\ell n\, 2}\, arccosh\left(\frac{exp\left(\frac{\ell n\, 2}{f}\right)}{2}\right) \qquad [3.8]$$

The function f is a function of the ratio of the two adjacent resistances and is close to 1 if the resistances are similar, see figure 3.7.

Van der Pauw Resistance	Current terminals	Voltage terminals
$R_{AB,CD}$	A,B	C,D
$R_{BC,DA}$	B,C	D,A
$R_{CD,AB}$	C,D	A,B
$R_{AD,BC}$	D,A	B,C

Table 3.1 — Van der Pauw Configurations

In practice the voltage measured between adjacent electrodes is small and comparable to errors arising in the circuitry. This error is eliminated by measuring the different values of I for different voltages and obtaining the resistance from the gradient of I-V graphs using the least squares method. The measurements were repeated with the current in the reverse direction to check the quality of the electrodes. At equilibrium the Hall Voltage, V_H is the potential required to exert a force on the current carriers equal and opposite to that exerted on them by the magnetic field. It is known that

$$\frac{V_H}{d} = R_H \, I \, B \qquad [3.9]$$

where B is the magnetic field, and R_H is the Hall coefficient given by

$$R_H = \frac{1}{n_c \, e} \qquad [3.10]$$

where n_c is the charge carrier concentration and e the electron charge. If the conductivity is known then the values of n_c and μ can be obtained from the measurement of R_H since

$$\sigma = n_c \, e \, \mu \qquad [3.11]$$

Another error is encountered if the voltage electrodes are not directly opposite one another and there will be a small offset potential due to the resistance of the sample. To allow for this the measurements were repeated with the magnetic fields reversed. The Hall voltage sign will be reversed but the offset will not and so will be eliminated (the two values of V_H are subtracted and divided by two).

The Hall coefficient R_H was determined from the change in resistances $R_{AC,BD}$ or $R_{DB,AC}$ with a change in the magnetic field ΔB perpendicular to the plane of the sample, using

$$R_H = \frac{d}{\Delta B} \Delta R_{AC,BD} \qquad [3.9]$$

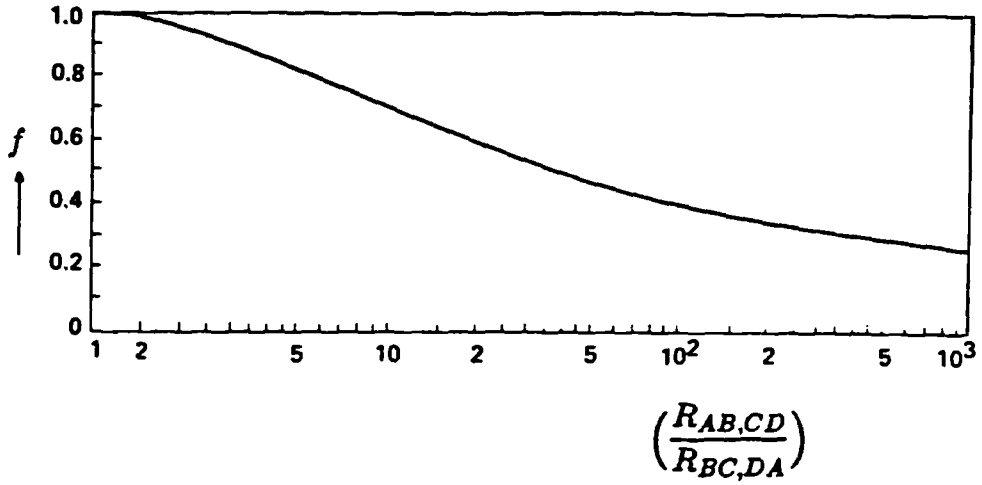

Figure 3.7 — The value of f plotted as a function of $\left(\frac{R_{AB,CD}}{R_{BC,DA}}\right)$

A Keithley electrometer was used as a current source and a Hewlett Packard HP3456a DVM with an input impedance of $> 10^{10}\Omega$ was used to measure the voltage. An electromagnet was provided with a constant current of 2 A and 200 V to give a magnetic flux density of 0.16 T at the centre of the pole gap. All parameters were controlled and data analysed by an Acorn Archimedes microcomputer, a detailed discussion of which has been previously reported [7].

3.4 References

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Chapter IV

Preparation of substrates for epitaxy

4.1 Introduction

Substrates play a crucial role in all high quality epitaxial deposition. The ideal substrate is one that is perfectly lattice matched to the epitaxial layer, as in homoepitaxy. In III-V compounds there are excellent quality substrates available for homoepitaxy, but amongst the II-VI compounds only CdTe and $Cd_{1-x}Zn_xTe$ are generally available as substrate materials. These crystals are very expensive and contain many imperfections that impair the epitaxial layer quality. The lack of suitable II-VI substrate materials has led to the investigation of alternative materials including ceramics [1,2], group IV and III-V semiconductors. However, it has been shown that even a mismatch of 0.1% in lattice constant leads to about 10^8 dislocations per cm^2 compared with $<10^5$ dislocations per cm^2 for homoepitaxial systems [3]. Moreover this mismatch also leads to strained layers that are sometimes bent to minimise the strain, causing difficulties in handling materials that will readily delaminate from the substrate.

In this thesis epitaxial layers of CdTe and ZnTe are grown by MOVPE onto n-type substrates of {0001} n-CdS, {100} n-GaAs and both {100} and $(\bar{1}\bar{1}\bar{1})$B n-CdTe. The lattice mismatch, m for these systems is calculated from equation 4.1

$$m = 2\,\frac{(a_1 - a_2)}{(a_1 + a_2)} \qquad [4.1]$$

where a_1 is the lattice parameter of crystal 1, and a_2 is the lattice parameter of crystal 2.

A summary of the lattice mismatches for the junctions encountered in this thesis are given in table 4.1, overleaf.

Substrate	Lattice Parameter/Å	Mismatch %	
	(300 K)	CdTe	ZnTe
{0001} CdS	a=4.135, c=6.713	9.7%	-
{100} GaAs	5.654	14.7%	7.6%
{100} CdTe	6.477	none	5.9%

Table 4.1 — Lattice mismatch for different semiconductor compounds at 300 K

It is important to note the orientation of the epilayer, since CdTe tends to grow in a {111} orientation on basal CdS, but can be either {111} or {100} oriented on {100} GaAs [4]. In this table the mismatches all refer to {100} oriented layers, except for the {0001}CdS substrate where the layer is {111}CdTe. For sphalerite systems the CdTe {100} orientation contains a 50:50 mixture of group II and group VI atoms. The {111} orientation however is polar and can be split into (111)A and $(\bar{1}\bar{1}\bar{1})$B orientations, the A face being composed of cadmium atoms and the B face of tellurium atoms. These different surface stoichiometries can lead to varying growth rates and epilayers with different defect microstructures. When semiconductors are etched in certain solutions it is found that some crystallographic planes etch faster than others. In the case of {0001} CdS, the two different types of faces, the A and the B face exhibit different etching properties. Large differences in the electronegativities exist between the Cd-component and the S-component and the difference in etching behaviour is attributed to this fact [5].

Even under good lattice matching conditions problems at the interface can still be encountered in systems with large mismatches in thermal expansion coefficients. Typically device structures are prepared at temperatures up to $\approx$400°C, but are subsequently used at room temperature. Differential contraction during cooling after fabrication will lead to strain at the interface, which is often taken up by the formation of dislocations. The physical properties of compounds used within these devices is described earlier in section 2.3.1.

However the first requirement for good epitaxy is to ensure that the initial stages of growth have a clean surface on which to "key". If this doesn't happen,

the growth will not recover no matter how thick a layer is grown. Generally [6] the thicker the film the better the structural [7,8], electrical [9] and photoluminescence properties are [10,11,12,13]. In order to ensure that growth starts with good crystal quality the substrate is prepared in a scrupulously clean environment.

Initially wafers are mechanically polished, using very fine abrasive particles of alumina suspended in a lubricant. Very high quality surface finishes can be produced in this way, the disadvantage being that the resulting surfaces are usually damaged (see section 4.3). Chemical polishing is one of the most commonly used techniques for epitaxial growth because it removes the damaged surface layer that has been left by mechanical cutting and polishing, and produces shiny, flat surfaces. If growth is conducted on substrates that have not been polished, the material grown is full of defects that can act as electron or hole traps and spoil the electrical properties of the layers [14]. In almost all semiconductor polishing processes the initial reaction is one in which the material is oxidised. In general the surface atoms will not pass into solution in this state and it is necessary to have another component in the etch that will react with the oxidised semiconductor to form a soluble complex. The complexing agent removes the oxidised species from the liquid-solid interface and prevents it from precipitating. Polishing solutions therefore contain an oxidising agent such as HNO_3, H_2O_2 or bromine and a complexing agent such as methanol, KCl etc... Many solutions also contain a constituent which simply dilutes the solution, this is often water. Thus it follows that more than one chemical reaction is involved in a typical polishing process, so the situation is far from simple. The etching leaves the substrate covered in a thin oxide layer on the surface. This oxide is removed in the first stage of the MOVPE process, the heat clean (see section 4.7). However, if the surface of the substrate is left stained by chemicals or is dirty in any way, the surface of the grown crystal will be full of defects which extend up through the layer from the substrate.

Chemical polishing produces a surface which is damage free, but often not flat. A combination of the two methods, chemo-mechanical polishing, can be used which gives a damage free surface of very high quality. The technique [15,16] is simply to polish the semiconductor slice on a polishing cloth, soaked in the etchant, using a polishing machine (see section 4.6.2). Reisman and Rohr [17] postulated that the effectiveness of this technique relied on the effect of the pile of the polishing

cloth on the flow of the etchant over the surface. Providing the pile is not too long turbulence occurs at any protrusions, which increases the etch rate. Stirring the solution is well known to encourage dissolution of reactants and thus aid the polishing process.

This chapter describes the substrate preparation studies on the n-CdS, n-GaAs and n-CdTe substrates. CdTe and GaAs are well known substrates for epitaxial growth and their surface treatment is well documented [18,19]. CdS, however has rarely been used as a single crystal substrate and a suitable preparation procedure had to be developed.

4.2 Review of the CdS substrate preparation

Generally CdS is not used as a substrate material due to its high cost, lack of availability and difficulty in handling (single crystal CdS is only commercially made by Eagle-Picher research laboratories in Miami, Oklahoma with an estimated cost of $120.00/gm). CdS has the wurzite structure, which is part of the hexagonal crystal system. The crystal faces perpendicular to the c-axis can either be terminated by Cd atoms or S atoms. The S surface atoms have three Cd atoms as nearest neighbours, whereas the surface Cd atom has only one sulphur atom, see figure 4.1. There is thus a difference in reactivity of the two different surfaces. The Cd-rich surface (0001) is commonly referred to as the A face and the opposite face $(000\bar{1})$ is rich in S and is referred to as the B face.

Sawing CdS with a diamond wheel is known to leave severely work damaged surfaces [20]. In order to prepare efficient devices it is necessary to polish the sawn faces mechanically to produce sufficiently flat surfaces before the chemical etch. Mechanical polishing, however, is known to produce cubic polycrystalline surface layers on the single crystal CdS surface [21,22]. Koba [21] showed that the wurzite-sphalerite polymorphous transformation took place by means of a slip on the close packed planes on the {0001} wurzite CdS to the formation of the {111}cubic planes of CdS (see figure 4.2). α represents the hexagonal system of stacking ABABA.., and β represents the cubic system of stacking ABCABCA... The fomation of the C layer from the hexagonal to cubic occurs by a small displacement of the atoms as shown in the diagram.

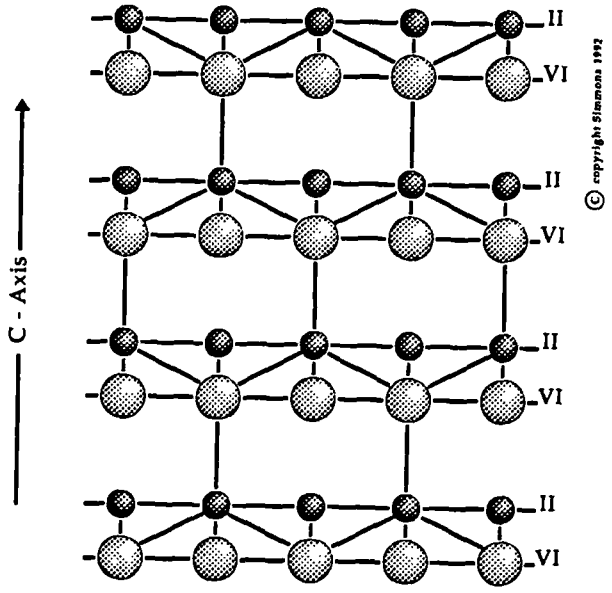

Figure 4.1 — Crystal lattice of CdS showing the layers of group II and group VI atoms perpendicular to the c-axis in basal CdS

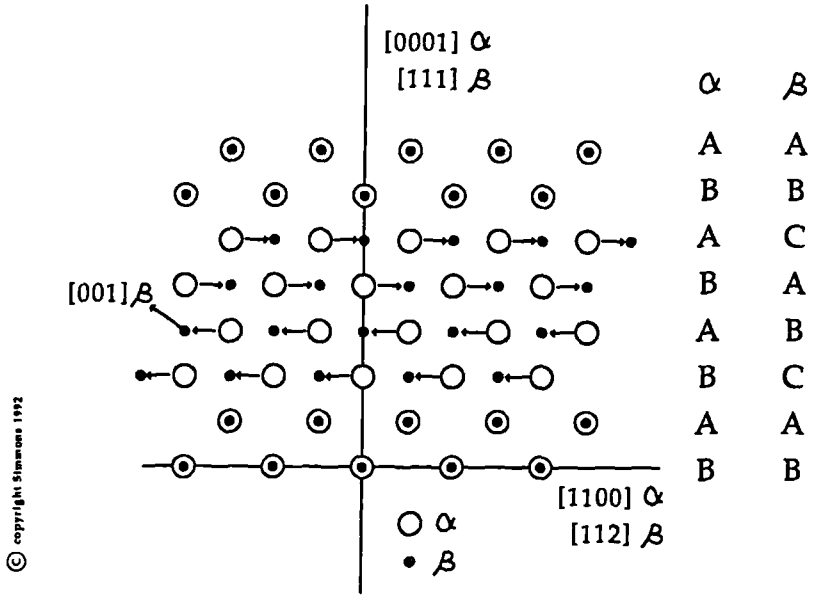

Figure 4.2 — α-β phase transformation [21]

Before epitaxial depostion can occur, this damaged surface layer has to be removed to leave a flat, stoichiometric and crystallographically perfect substrate

material. A HCl/H_2O etch has been shown not only to remove this polycrystalline layer but also acts as a revealing etch to distinguish between the A and B faces of CdS, which turn shiny and dull respectively [23]. Whilst removing the damaged layer, the HCl/H_2O etch also results in a rough surface with numerous large hillocks on the S face. Semiconductor laser screens fabricated on such a surface are invariably poor, having a low luminescence efficiency [24,25]. The significant differences in the chemical etching characteristics of the two polar faces of II-VI compounds has previously been observed [26], and an empirical relationship exists between the measured etch rates and the differences in electronegativities of the component elements [27]. The pronounced difference in the etching characteristic on the polar faces of most II-VI compounds is attributed to the higher amount of ionic character in the bonding.

Thus a distinction is made between chemical etching and polishing. Etching denotes the removal of material regardless of the final surface condition, whilst polishing denotes removal resulting in a smooth and shiny surface. A lot of etching studies were undertaken in the 1960's, when analytical techniques had lower resolutions. As a result some observations indicating polishing behaviour were not accurate, e.g Sullivan et al observed flat featureless surfaces on the S face using a 30% HCl etch, but the resolution was $\approx$70 μm.

Warekois et al [28,29] observed the differences in etching behaviour of the A and B faces of CdS, and concluded that the tendency for the S face to develop dislocation pits resulted from either the high electronegativity of the S or the large difference in electronegativities of the sulphide. Maeda [30] followed up Warekois work on the $K_2Cr_2O_7$/ H_2SO_4 polish replacing the sulphuric acid with phosphoric acid, giving a higher quality polish, that still had, however, a measurable dislocation etch pit density. A bromine in methanol etch has been found to be successful in the polishing of several II-VI compounds [31], but it was found unsatisfactory for CdS. Pickhardt and Smith [32] used a chemomechanical $HNO_3/AlCl_3$/silica polish which gave good LEED patterns after heat treatment in a vacuum, but his method was not continued. Any attempts to grow epitaxial layers on this polished substrate resulted in polycrystallinity [31].

Author	Etchant	Cd face	S face
E.P. Warekois [28]	$6CH_3CO_2$, $6HNO_3$ $1H_2O$	Hexagonal pits	discontinuos S film
	$1HCl$, $1HNO_3$	S deposits	conical pits
	0.5M $K_2Cr_2O_7$ 16N H_2SO_4	shallow dishes	polished with dislocation pits
M. Maeda [30]	0.5M $K_2Cr_2O_7$, HPO_3	clean surfaces, low density of surface states	
M.V. Sullivan [23]	30% HCl	Featureless down to 70μm, flat to within $\pm$2.5μm	
W.H.Strehlow [27]	10% Br_2/MeOH	no polish	no polish
V.Y. Pickhardt [33] D.L. Smith	90ml HNO_3, 10g $AlCl_3$, 100ml H_2O	Flat, good LEED after heat clean	Featureless under Normarski at 155×, 400×.
A. Pritchard [32]	HCl/KCl	Featureless under Normarski at 1000×	
I.V. Akimova [34]	HCl/C_2H_5OH	2.5μm disturbed layer as seen by PL	
S. Oktik [22]	HCl/H_2O	-	Surface hillocks
V.A. Zhuk [25]	33.3%CrO_3/HNO_3	Good single crystal RHEED	
E.S. Koba [21]	CrO_3/HCl	Good single crystal RHEED	

Table 4.2 — Effects of various etchants on the polar faces of CdS

In 1977 Pritchard et al reported a chemical polish for both the Cd and S faces of CdS. It comprised of an aqueous HCl/KCl mixture with a different pH for the two faces. The luminescent spectrum measured by photoluminescence (PL) confirmed the perfection of shallow surface layers [32]. PL was also used to measure the depth of the disturbed surface layer left after polishing [34]. A polish consisting of C_2H_5OH/HCl was shown to leave the thinnest damaged surface layer. Vasilisceva [24] confirmed, using PL, that complexes remained on the crystal after chemical interaction had taken place, and some method was needed to remove these complexes. S. Oktik et al [22] used a HCl/H_2O etch for 30 secs to remove

the polycrystalline damaged layer introduced by mechanical polishing, but this resulted in a severly hillocked surface. Subsequent solar cell devices formed were found to have a reduced solar efficiency due to the high interface recombination velocity.

RHEED studies were then performed on a CdS crystal polished in a CrO_3/ HNO_3 etch [25]. Following annealing treatments on these chromic acid polished surfaces at high temperatures (550 K) under vacuum, the surface layers were found to be "healed" restoring the matrix orientation in the substrate layer. Annealing has been shown previously to remove distortions introduced by polishing. A summary of all these etching/polishing treatments on single crystal CdS is presented in table 4.2.

4.3 Mechanical polishing of Cadmium Sulphide

4.3.1 Experimental

A boule of CdS was oriented using the Laue back reflection x-ray technique on the {0001} basal plane. Slices 1.5 mm thick were cut from the boule using a diamond saw, the maximum misorientation being less than 0.5°. After cutting the surfaces of the crystals appeared very rough and the edges were chamfered to prevent any crystallites breaking off during the mechanical polish. The CdS was then mechanically polished using 14, 6, 1, 0.25 μm diamond paste suspended in a lubricant. Each stage of the mechanical polish took $\approx$ 2 hours and was repeated for both sides of the wafer.

4.3.2 Results

After the mechanical polishing the surfaces of the CdS appeared to be uniformly covered in tiny microscratches when viewed in the SEM, see figure 4.3. A weak diffraction pattern with considerable blurring around the central spot was obtained using RHEED. The polishing had produced a microscopically smooth surface causing the definable rings of a polycrystalline surface to be smeared out as observed by Oktik et al [22]. Great care was taken to ensure that wafers of

CdS did not shatter during mechanical polishing. All wafers were initially greater than 1.5 mm thick before polishing to ensure greater strength during the polishing procedure.

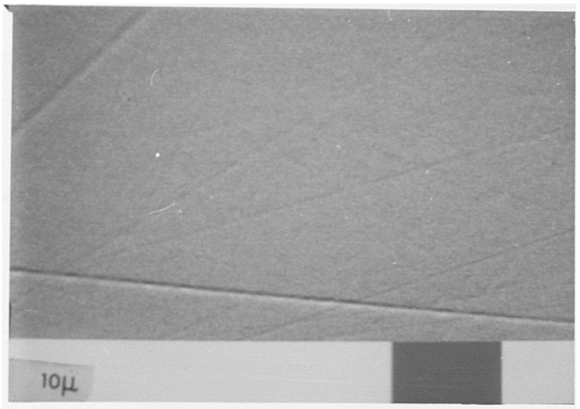

Figure 4.3 — An SEM micrograph of the effects of the mechanical polish on the surfaces of basal CdS

4.4 Chemical polishing of CdS

4.4.1 Experimental

Following the historical review of the chemical polishing of CdS given in table 4.2 it was decided to find a quick reliable method to produce a highly polished clean stoichiometric, damage-free surface of single crystal CdS for epitaxial purposes. The well studied chemical preparation of GaAs was considered as a basis for the same type of procedure for the CdS crystal. In the case of GaAs the mechanically polished wafers of GaAs are simply dipped into a solution of the etchant for 4 minutes which is maintained at a constant temperature and is stirred manually. The same procedure was thus adopted for each of the suitable etches described in table 4.2. After the etching procedure the wafers were rinsed in deionised water for 1 hour to quench the chemical reaction. Following this wafers were dried in a hot atmosphere of iso-propylalcohol (IPA), before being examined using SEM and RHEED.

4.4.2 Results

The effects the various polishing solutions had on the resulting surfaces of the A and B faces of basal CdS are summarised in table 4.3. Following these preliminary observations it was decided to concentrate further optimisation on the three most likely polishes, the CrO_3/HNO_3, $KCl/HCl/H_2O$ and HCl/H_2O polishes. The main reason for this being that they all gave single crystal surfaces when observed by RHEED.

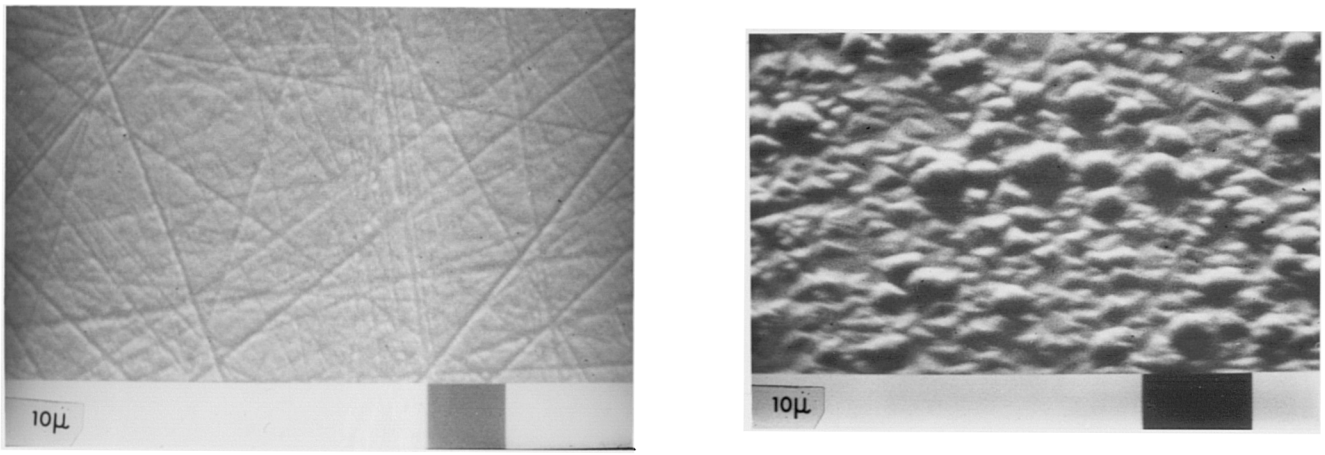

Figure 4.4 — SEM micrographs of the Cd and S faces of basal CdS after polishing in HCl/H_2O

Initially the HCl/H_2O polish was investigated. A 30% HCl/H_2O polish solution was made up and the CdS crystals etched in this solution at 30°C, whilst being stirred with a magnetic stirrer. The CdS crystals were etched for periods of 10 seconds at a time and then observed under SEM and RHEED to see the effects on the surface. For this etch it was found that etching for less than 20 seconds did not remove much of the polycrystalline damaged surface layer, whilst etching for longer resulted in a highly irregular surface. After 20 seconds, the S face was covered in etch pits $\approx 5\mu$m in diameter with a distinct triangular shape, whilst the Cd face was covered in microscratches, see figure 4.4. Left for even longer than 20 seconds the S surface became severly hillocked, and the scratches on the Cd face

became bigger until they resulted in a highly ridged surface as described in table 4.3.

Thus it appears that a compromise has to be accepted with this etch, either a reasonably flat surface is obtained which may still be partially damaged or a single crystal surface that is very irregular can be used for subsequent devices. Indeed the corresponding RHEED patterns for the surfaces after a 20 second etch are shown in figure 4.5. It can be seen that the pattern consists of features from both the polycrystalline layer and the underlying crystal. The arcing of the spots indicates that the hexagonal crystallites are only partially misoriented with respect to the substrate. Previous devices made on HCl/H_2O polished faces of CdS were however seen to be poor due to the high recombination velocity across the damaged interfaces [24,25].

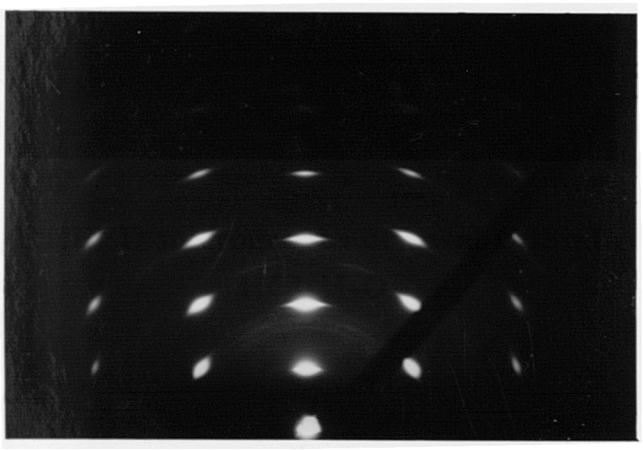

Figure 4.5 — RHEED micrographs of basal CdS after polishing in HCl/H_2O

The $HCl/KCl/H_2O$ etch proposed by Pritchard et al [32] was prepared using 0.5 ml HCl, 13.3 g KCl and 100 ml of deionised water and used for periods of 15-180 minutes. At 15 minute intervals the S face surface was observed by RHEED and SEM. For polishing times greater than 30 seconds a film having a milky appearance was observed on the surfaces. The incidence of this film was eliminated

by mechanical stirring during polishing, and this indicates that it may have been composed of reaction products. The temperature of the polish was then varied from 20°C to 60°C in steps of 10°C.

Polishing Solution	Physical Appearance	SEM	RHEED	Ref.
$K_2Cr_2O_7/H_3PO_4$	Both surfaces mirror finish	A face : etch pits 2-3μm B face : featureless	P P	[30]
CrO_3/HNO_3	Both surfaces mirror finish	A face : scratched B face : featureless	SC SC	[25]
CrO_3/HCl	Both surfaces mirror finish	A face : rectangular pits 4μm B face : shallow pits 4-5μm	P P	[21]
C_2H_5OH/HCl	A face : dull B face : shiny	A face : triangular pits 1μm B face : triangular pits 2μm	B B	[34]
HCl/H_2O	A face : dull B face : shiny	A face : ridged B face : hillocks 1-2μm	SC SC	[22]
$KCl/HCl/H_2O$	A face : dull B face : shiny	A face : hexagonal pits B face : scratched, deposits	SC SC	[32]

P = polycrystalline, SC = single crystal, B = blurred

Table 4.3 — The effects of various polishes on the A and B faces of single crystal CdS

Below 40°C a very sharp RHEED pattern was observed, see figure 4.6 indicating the presence of a single crystal surface. This pattern corresponds to a {0001} plane where the direction of the incident beam is along the <10$\bar{1}$0> direction in the hexagonal crystal. A complete analysis of the ring pattern (see table 4.4) revealed that both the cubic and hexagonal polycrystalline phases existed on the surface of the CdS. The first ring can be attributed to either the overlapping (100), (022)

and (101) planes in the hexagonal phase or the (111) planes in the cubic phase. The polish has thereby removed a very small surface layer. For longer polishing times the surface again became highly uneven, or hillocked as it did at higher temperatures.

Ring	d_{calc}/Å	$d_{tab(hex)}$/Å	(hkl)	$d_{tab(cubic)}$/Å	(hkl)
1	3.81	3.583	100		
2	3.27	3.357	002	3.36	111
		3.160_a	101		
3	2.46	2.450	102		
4	2.08	2.068	110	2.06	220
5	1.93	1.898	103		
		1.791_b	200	1.755	311
6	1.78	1.761	112		
7	1.72	1.731	201		

Rings *a* and *b* are not observed experimentally but are thought to be contained within the blurred rings. *hex* = hexagonal, *tab* = tabulated values taken from the ASTM index

Table 4.4 — Analysis of the RHEED pattern for CdS etched in HCl/KCl.

Finally to optimise the etch further, the composition was altered. It was considered that the KCl acted only to slow down the reaction at the surface, and it was the concentration of the acid that affected the surface structure. Thus the concentration of the acid was varied in the polish. If too small a volume of acid was used a milky appearance was observed probably due to the formation of $CdCl_2$ or $CdCO_3$ (the CO_2 being dissolved into the polish from the air). An electron dispersive analysis by x-rays (EDAX) trace was obtained from the surface covered with the thin film, see figure 4.7.

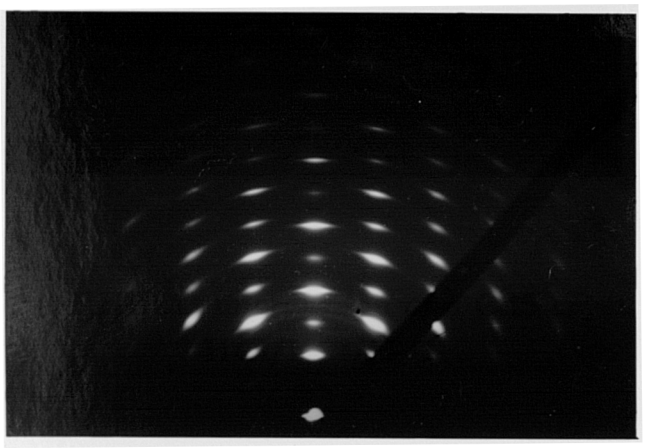

Figure 4.6 — A RHEED micrograph of a CdS crystal polished in $HCl/KCl/H_2O$

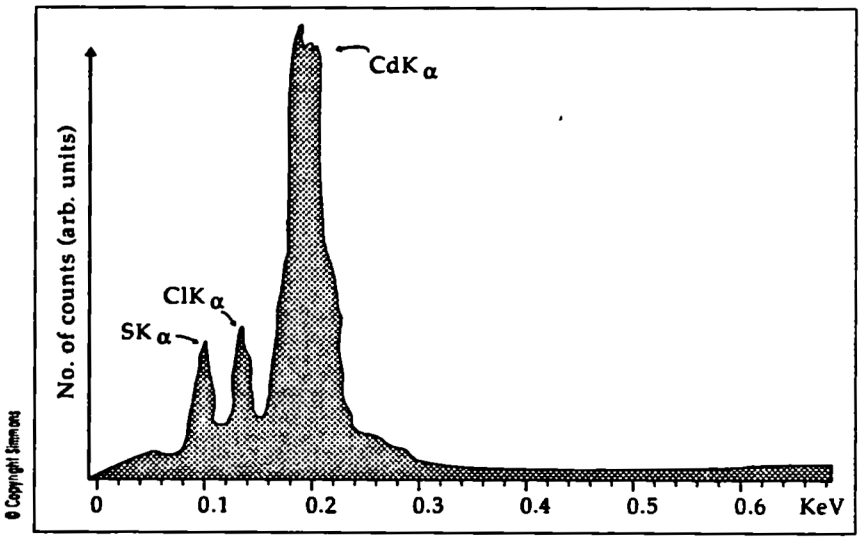

Figure 4.7 — EDAX trace of CdS surface etched in $HCl/KCl/H_2O$

A large chlorine peak was observed indicating the possible presence of $CdCl_2$. The corresponding RHEED pattern was blurred with no hint of a single crystal pattern. At higher concentrations of HCl a very rough surface resulted. The same optimisation procedure was performed on the Cd face where it was found

that the polishing resulted in etch pits approximately 2μm in diameter. RHEED analysis confirmed the presence of a single crystal pattern superimposed on faint polycrystalline rings. These rings corresponded to the cubic and hexagonal phases of CdS, indicating that the mechanically damaged surface layer had not been entirely removed from the highly ordered substrate below. At this stage it was decided to grow an epitaxial layer of CdTe (using the conditions described in section 5.4) on these surfaces of the CdS prepared using this polish. After growth it was observed that both the S and Cd faces were dull. On examination with the SEM both faces showed a high density of polycrystalline deposits, approximately 2-4μm in diameter, see figure 4.8. RHEED patterns also shown in figure 4.8 describe a (111) CdTe polycrystalline ring pattern. The rings however are not complete and smooth but remain spotted indicating the presence of a large number of oriented crystallites in the CdTe layer.

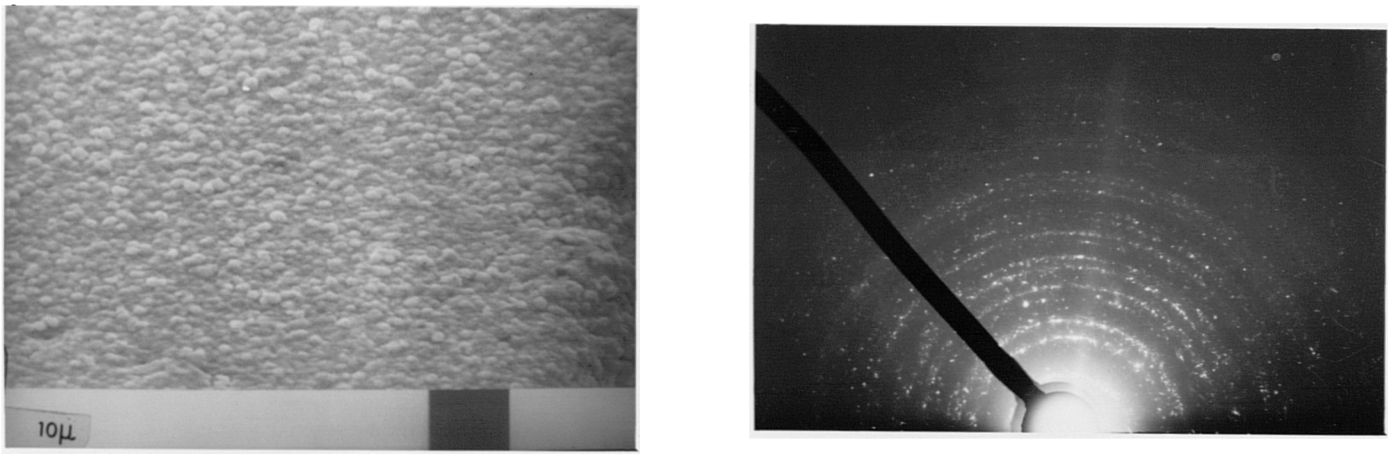

Figure 4.8 — The SEM and RHEED micrographs of a CdTe layer grown on a HCl/KCl/H_2O polished surface

If a good crystalline register of epitaxial CdTe is to be obtained, the substrate surface must show no signs of polycrystallinity. Thus another polish had to be found that completely removed the polycrystalline layer resulting from the mechanical polish.

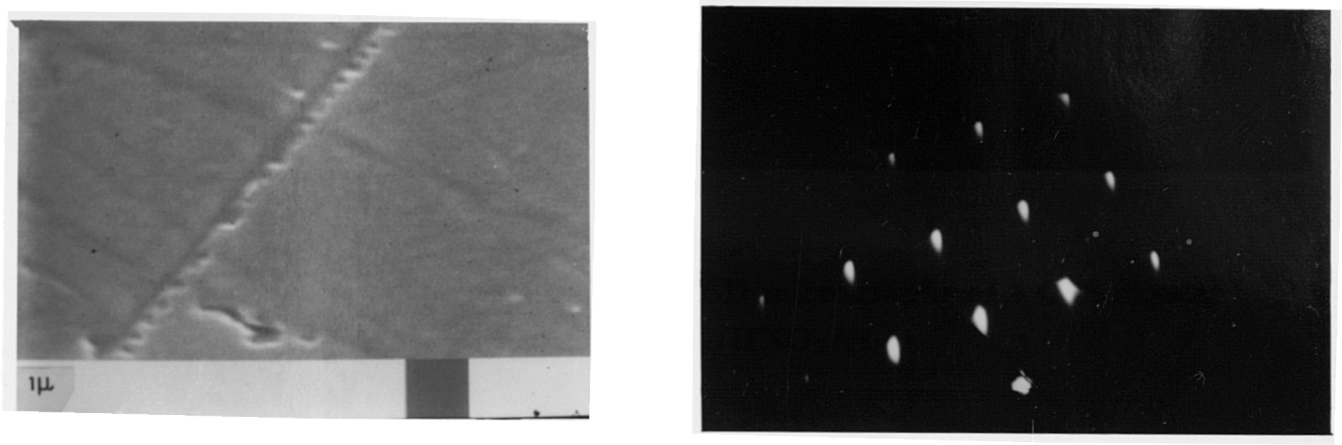

Figure 4.9 — The SEM and RHEED micrographs of a CdS crystal etched in $CrO_3/HNO_3/H_2O$

The best surface for epitaxy was obtained using a mixture of 4.8 g CrO_3, 9.1 g HNO_3 (70%) and 50 ml of deionised water, based on that used by Zhuk et al [25]. Oriented wafers were dipped into the solution at 30°C for ten minutes and the reaction was quenched by rinsing in deionised water. The resulting surfaces were mirror-like and free from mechanical polishing damage as evidenced by RHEED. However when viewed in the SEM the surfaces were seen to have a slightly undulating morphology with a network of microscratches, as shown in figure 4.9. These scratches were a consequence of the mechanical polish , but as with the $HCl/KCl/H_2O$ etch were revealed by the action of the chemical polish. With care in the mechanical polishing technique these scratches could be partially eliminated. Subsequent epilayers of CdTe were found to be crystalline on the S face, but twinned on the Cd face (see section 5.5); indicating the validity of the chromic acid polish.

4.5 GaAs substrate preparation

4.5.1 Review of the chemical polishing of GaAs

The chemical polishing of GaAs has been studied by several authors and the etches they proposed are outlined in table 4.5. Generally all etches were found

Author	Chemical solution	Technique	Results
M.V. Sullivan [23]	0.05% Br_2/MeOH	I.S	$\approx$ 25 Å roughness
	3:1:1 $H_2SO_4/H_2O_2/H_2O$	dipped	$\approx$ 200 Å roughness
A.Reisman [18]	NaOCl	dipped	smooth surfaces
S. Ida [41]	5:1:1 $H_2SO_4/H_2O_2/H_2O$	dipped	etch pits
	1000 CH_3OH:1 Br_2	dipped	etch pits
V.L.Rideout [17]	20:1 H_2O:NaOCl	CM	$\approx$ 250 Å roughness
T. Oda [42]	HNO_3/HF	dipped	smooth, flat
I. Shiota [43]	$NaOH/H_2O_2$	dipped	thin oxide layer
J.V. Gormley [44]	4:1 CH_3OH/	HP	optically flat,
	ethylene glycol		damage free
A. Munoz-Yague [37]	$H_2SO_4/H_2O_2/H_2O$	dipped	excellent surface
J.P. Contour [45]	Br_2/CH_3OH	CM	Ga rich surface
	$H_2SO_4/H_2O_2/H_2O$	dipped	As rich surface
H. Fronius [46]	$NaOCl/H_2SO_4$	CM	surface oxide
R. Sonnenfeld [47]	Br_2/CH_3OH	CM	surface strain
Z. Hang [39]	Br_2/CH_3OH	CM	not smooth

I.S = intensive stirring, CM = chemomechanical, HP = hydroplaning

Table 4.5 — A summary of the polishes for GaAs substrate

to leave a thin oxide layer on the GaAs surface. The morphology and thickness of this oxide was, however found to vary with different etches. Of all the etches studied only Br/CH_3OH, $H_2SO_4/H_2O_2/ H_2O$, HNO_3/HF and $NaOH/H_2O_2$ were found to leave thin homogeneous oxide layers. The need for an improved polishing technique came about in the need for a suitable surface for MBE [35].

The most common ways of etching GaAs are either chemical etching based

on a $H_2SO_4/H_2O_2/H_2O$ mixture [36,37] or a chemomechanical polish with a dilute bromine/methanol solution [38]. The polishing procedures may affect the quality of devices fabricated on processed substrates, but despite its significance relatively little work on this subject has appeared in the literature [39]. A surface prepared by a 0.05% bromine/methanol solution was analysed by nuclear backscattering and was found to be contaminated by carbon [40]. Deviations from stoichiometry were also observed, both effects possibly leading to unwanted electrical properties in the GaAs sample. Excellent surfaces were however obtained using a $H_2SO_4/H_2O_2/H_2O$ chemical etch as proposed by Munoz-Yague et al [37].

4.5.2 Experimental

Mechanically polished wafers of {100} oriented GaAs were supplied by MCP Electronic Materials Ltd. Following the review in section 4.5.1 a 4:1:1 solution of $H_2SO_4/H_2O_2/H_2O$, as used by Munoz-Yague [37] was considered the best polish for the {100} oriented GaAs. Immediately prior to growth the n-GaAs substrates were etched in this solution at 40°C for 4 minutes. This procedure removes any damage left by the mechanical polishing and results in a thin oxide layer protecting the GaAs surface [37]. This oxide layer is subsequently removed in the heat cleaning process (see section 4.7) to leave a clean, damage free surface of GaAs for growth.

The substrates were held in a specially designed silica "jig", which ensured no damage was introduced to the substrate by handling. Care was taken to ensure that the intended growth surface was maintained uppermost during the etch, since the dissolution process produced bubbling at the surface of the GaAs. Large amounts of GaAs are removed in their path as these bubbles escape to the surface, resulting in a highly ridged surface. This bubbling process has been observed with other etches [48] and is often thought, if controlled, to be useful as a natural stirring process.

4.6 Preparation of CdTe substrates

4.6.1 Review of the polishing of CdTe

CdTe is a material often used in the growth of epitaxial CdHgTe. It is soft (2.75 on Moh's hardness scale) and brittle with a strong tendency to cleave along

Author	Chemical solution	Technique	Results
M.H. Patterson [50]	Br_2/MeOH	dipped	stoichiometric, Br contam.
	$K_2Cr_2O_7/Ag^+$	dipped	TeO_2 surface $\approx$ 30 Å
	HNO_3	dipped	TeO_2, Te surface $\approx$30 Å
	NaCN	dipped	TeO_2, Te surface $\approx$ 30 Å
	cleaved face		only (110) planes
T.J. Magee [51]	Br_2/MeOH	HP	small density of dislocations
J.A.Mroczkowski [52]	diamond milling	cleaved	smooth, damage free
T. Myers [53]	Br_2/MeOH	HP	surface dislocation density $\approx 10^5/cm^2$
P.M. Amirtharaj [54]	Br_2/MeOH	CM	surface Te layer, 40 Å thick
D.F. Weirauch [55]	Br_2/MeOH	dipped	damage free, "orange peel" effect

HP = hydroplaning, CM = chemomechanical

Table 4.6 — A summary of the chemical polishing techniques on single crystal CdTe substrates

the (110) planes. Generally after mechanical polishing numerous microscratches exist on the surface due to the abrasive. Associated with these cracks will be strained material and dislocation arrays. The appearance of a surface can be misleading because x-ray or etching studies often reveal considerable damage in the form of scratches, or pits which are concealed by the surface flow of material being polished. The shearing of the surface has been observed for polished CdTe surfaces and is often referred to as the "Beilby layer" [49].

Table 4.6 summarises the findings of authors on the polishing of CdTe. It can be seen that only the Br_2/MeOH polish has been studied in any detail, since it is known to leave a damage free planar surface.

Initially experiments with the Br_2/MeOH etch confirmed the presence of a 10-40 Å thick CdTe layer [54] at the surface which was observed to have a slight "orange peel" appearance [55]. With the advent of hydroplane polishing techniques (see section 4.6.2) it became possible to eliminate this orange peel effect, and the subsurface damage introduced by chemomechanical polishing [53]. Hydroplane polishing was seen to reduce surface dislocation densities from 10^8-10^{10} cm^{-2} to 10^5-10^6 cm^{-2} (which is typical of bulk CdTe). The only other technique found to produce high quality surfaces was the cleaving of CdTe in air, followed by heat treatment in a vacuum [50]. However, this can only produce wafers of (110) oriented CdTe, its only principal cleavage plane.

4.6.2 Experimental

The Laue back reflection x-ray technique was used to orient a CdTe crystal boule to the (100) orientation. Wafers approximately 1.5 mm thick were cut from the boule with a diamond saw, with a maximum misalignment of 0.5°.

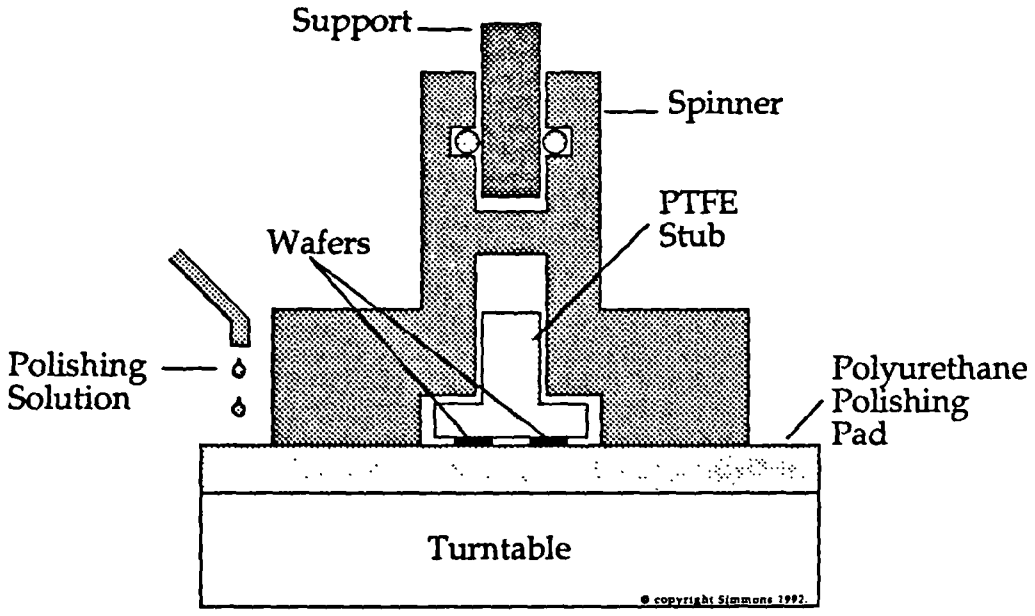

Figure 4.10 — The hydroplane polishing apparatus

Polishing was carried out using a hydroplane polisher as described in figure 4.10. This is similar to the one proposed by Gormley et al [44], but with a speed of 75 rev min^{-1}. In this method wafers of CdTe are mounted on a PTFE stub which is constrained horizontally by a spinner, as shown in the diagram. As the turntable moves the wafer hydroplanes on a thin layer of the polishing solution without contacting the pad. Thus no mechanical damage can occur to the wafer and a continual supply of fresh polishing solution ensures all waste reactants and products are removed by the rotational force. The solution was a 0.05% bromine in a 4:1 methanol:ethanediol mixture which has been shown to remove all surface damage [51].

After removal from the stub the wafers were degreased in 1,1,1 trichloroethane and given a brief dip $\approx$ 5 secs in 0.05% bromine/methanol and rinsed in aristar grade methanol. This has been shown by x-ray photoelectron spectroscopy (XPS) methods [55] to leave CdTe surfaces which are almost stoichiometric.

4.7 Heat cleaning of substrates

After chemical preparation all substrates were loaded immediately into the MOVPE reactor, which was flushed with hydrogen for 1 hour to ensure the removal of all oxygen from the system. The substrates were then heat cleaned in hydrogen for 10 minutes to reduce any native oxide present on the surface. For CdTe and CdS substrates this was carried out at a temperature of 410°C as prescribed by Hails et al [56], whilst for GaAs the heat clean temperature was 600°C. This heat cleaning procedure on GaAs has been found to reduce the native oxides and any carbonaceous deposits left as observed by XPS [57].

After this heat cleaning treatment the susceptor temperature is altered to the growth temperature and the growth initiated as described in chapter 5. In the case of the p-i-n structures on n-CdS and n-GaAs substrates the growths were carried out in the same run for comparative purposes and thus the n-GaAs was only heat cleaned at 410°C. At this temperature it is not suspected that the native oxide formed by the chemical treatment is entirely removed [37].

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Chapter V

Growth of epitaxial layers by MOVPE

5.1 Introduction

Several epitaxial techniques are currently available for the growth of semiconductor materials, including liquid phase epitaxy (LPE), molecular beam epitaxy (MBE), and vapour phase epitaxy (VPE). The VPE family includes chloride vapour phase epitaxy (ClVPE), hydride vapour phase epitaxy (HVPE), and metal organic vapour phase epitaxy (MOVPE). An overview of each technique, including the advantages and disadvantages is presented in table 5.1.

During the early 1980's the validity of the MOVPE process was in question due to problems with impurities and interface abruptness. These problems have now been overcome to the extent that the highest purity InP is now produced by MOVPE, and interface abruptness is known to be attainable down to atomic levels [1]. Indeed devices produced by MOVPE have been shown to have comparable performance characteristics to those produced by MBE. The major attractions of the MOVPE process are its capability for large scale production and its versatility. Virtually all III-V and II-VI compounds and alloys can be produced using the MOVPE technique.

Manasevit [2,3] first demonstrated that metal organics and hydrides could be used successfully in chemical vapour deposition (CVD) processes for the production of single crystal layers of III-V semiconductor compounds. MOVPE was then applied to the growth of various II-VI compounds and alloys [4,5,6]. Since then numerous review articles on MOVPE and specifically the MOVPE growth of II-VI compounds have been published [7,8,9,10,11].

The sections in this chapter describe the epitaxial growth of layers of CdTe, ZnTe and $Cd_{1-x}Zn_xTe$ for use in solar cell devices. The principles of MOVPE are

Technique	Process Details	Advantages	Disadvantages
LPE	Substrate is placed in a supersaturated solution containing required compound.	Simple apparatus, high purity metals.	Simple, inflexible, abrupt interfaces difficult, poor uniformity, difficulty with certain materials, no control of doping.
MBE	Molecular or atomic beams impinge on a substrate surface, where at suitable temperatures and particle flux epitaxial growth occurs.	Flexible, low temperature growth, use of foreign substrates in situ doping possible, well controlled growth rates, fast switching of fluxes, purity - high as elemental sources, in situ montoring.	Requires UHV, complex, expensive, low throughput, difficulty in growing P, As, compounds as they collect in vacuum pumps.
HVPE	Group V or Group VI is transported to growth interface using hydrides.	Large scale.	Hazadous sources, difficult to control, complex process, Al, Sb difficult to grow.
ClVPE	Group V or Group VI is transported to growth interface using chorides.	Simple, high purity.	No Al alloys available, large interface defects as layers passed between reactors.
MOVPE	The transport in the vapour phase of metal organics to the surface of a substrate where metalorganics pyrolyse to release component ions for growth.	Most flexible, abrupt interfaces, simple reactor, high purity, in situ doping, low temperatures, use of foreign substrates, controlled growth rates and switching possible.	Expensive reactants, most parameters need precise control, hazardous precursors, limited in situ monitoring.

Table 5.1 Comparison of Epitaxial Growth Techniques.

discussed in section 5.2 and the growth system used at Durham is described in section 5.3. The initial growth of CdTe onto {100}GaAs substrates in order to assess the influence of growth parameters on the layer quality is presented in section 5.4. Epitaxial growth of CdTe onto {0001} and {01$\bar{1}$6}CdS and {111} CdTe substrates with the same growth conditions as used in subsequent device fabrication is analysed in section 5.5. Section 5.6 goes on to describe the epitaxial growth of ZnTe onto {100}GaAs, again to optimise growth parameters for use in solar cells structures. The deposition of ZnTe onto {111}CdTe surfaces for production of p-i-n solar cell structures (see chapter 8) and the growth of ZnTe onto {100}CdTe for use in p-n devices (see chapter 7) is also described in section 5.6. The p-type doping of both CdTe and ZnTe using ammonia and elemental arsenic is discussed in section 5.7. The growth of the $Cd_{1-x}Zn_xTe$ alloy and its incorporation into graded p-i-n structures (described in chapter 8) is presented in section 5.8. Finally the formation of ohmic contacts to all surfaces for device fabrication is discussed in section 5.9.

5.2 Principles of MOVPE

Vapour phase epitaxy (VPE) growth techniques often make use of pyrolytic reactions occurring between the vapours of volatile chemical compounds A and B when they are heated together. These reactions produce chemically active species C and D which can either interact in the vapour phase or on a solid surface of a substrate, S to produce a corresponding epitaxial layer, E. This is illustrated in figure 5.1. MOVPE specifically utilises vapours from metal-organic compounds.

The mechanism of MOVPE single crystal growth is a matter of continuing conjecture. The main stages in the mechanism consist of the following steps:
(1) The transfer of reactants to the substrate surface
(2) adsorption of reactants
(3) surface reaction
(4) desorption
(5) transfer of products away from the surface
Thus it can be seen that thermodynamics determines the driving force for the overall growth process, but kinetics defines the rates at which various processes

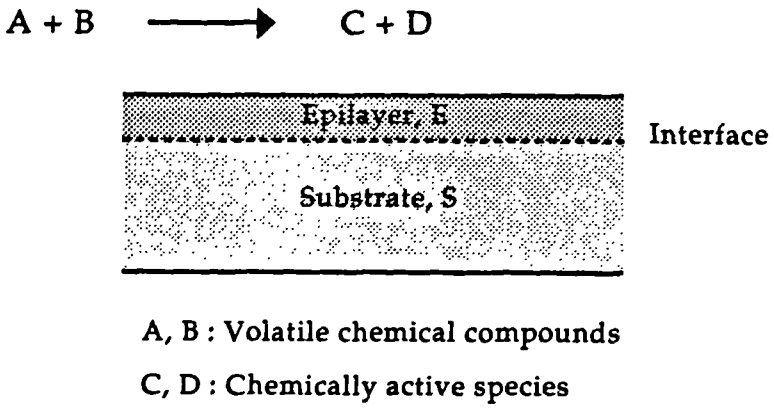

Figure 5.1 — The formation of an epitaxial layer by MOVPE

occur. Hydrodynamics and mass transport are also an integrated part of the process, controlling the rate of transport of the material to the growing solid/vapour interface. Each of these factors will dominate some aspect of the growth. The variation of growth rate with temperature generally gives an indication as to which one dominates the overall growth process. MOVPE is known to be an exothermic process, thus if the growth rate is thermodynamically limited, it is seen to decrease exponentially with increasing temperature. If the reaction rate limits the growth rate, termed the kinetically limited case the growth rate will be seen to increase with increasing temperature. Finally since diffusion is a much less temperature dependent process, the growth rate is nearly independent of substrate temperature in the mass-transport limited case. Other factors such as substrate orientation also help in determining the growth rate limiting process. The effects of substrate orientation only become important when the rate limiting step in the process is governed by the surface kinetics.

The provision of good quality epitaxial material is hampered by a crystal's ability to grow in alternative ways other than to produce a perfect lattice. These "side reactions" include the growth of a group II atom on a group VI lattice site (antisite defect), a lattice with atoms sitting between lattice sites rather than on them (interstitials) and lattices with atoms missing from their correct positions

(vacancies). Thus it can be seen that the chemistry of the decompositon of the metal organic precursors and the subsequent production of the epitaxial layer is very complicated and beyond the scope of this thesis. Detailed descriptions of the processes occurring during the growth of II-VI and III-V compounds by MOVPE are discussed in a detailed book by Stringfellow [1].

Initial research in the MOVPE of II-VI compounds involved the use of simple alkyls, such as R_2M, where R was either a methyl or ethyl radical and M was generally the group II or, less commonly, the group VI element (which was generally used as a hydride). However, the development of the MOVPE process has demanded the production of new organometallic sources with lower decomposition temperatures and higher purities. Generally low growth temperatures are desirable since they reduce solid state inter-diffusional processes, sharpening interfaces and decreasing the possibility of unwanted doping from a foreign substrate. At present the lower limit of the growth temperature of tellurium based binaries is determined by the decomposition temperature of the telluride precursor which, until recently, was diethyltelluride with a decomposition temperature of 400°C. With the advent of di-isopropyltelluride (DiPTe) the growth temperature of these binaries has been reduced to temperatures as low as 320°C [12]. Even more recent studies have seen the decomposition temperature of another Te-based precursor, diallyltelluride become as low as 180°C [13]. Table 5.2 describes the organometallic sources and their properties used in this thesis. The dimethylzinc (DMZn) source is a fairly high vapour pressure liquid at room temperature and is cooled to -12°C in a constant temperature bath to give a vapour pressure of 66.8 torr. The dimethylcadmium (DMCd) has a vapour pressure of 9.7 torr at 17°C and, as with the zinc precursor, is known to decompose at approximately 150°C. The choice of optimum growth conditions is an important part of the overall process design. Independent parameters such as the substrate temperature, II-VI ratio, and total flow rate have to be investigated to give the desired material properties. This optimisation process has to be determined empirically since conditions are not constant, even for a given reactor. For the tellurium based epitaxial layers grown in this thesis the various growth parameters are investigated in sections 5.4, 5.6 and 5.9.

Precursor	Melting pt. (°C)	Boiling pt. (°C)	Vapour pressure Torr at T(°C)	Comments
DMZn	-42	46	66.8 at -12°C [14]	Decomposes at 150°C sensitive to O_2 spontaneously flammable
DMCd	-2.4	106	9.7 at 0°C [15]	Decomposes at 150°C sensitive to O_2 inflammable
DiPTe	-	-	2.12 at 17°C [16]	Stable to air and water decomposes at 320°C

Table 5.2 — Properties of Organometallic Precursors used in this thesis

5.3 The MOVPE growth system

A schematic diagram of the growth system used in Durham is shown in figure 5.2. The metal organics chosen have high vapour pressures at or around room temperature so that they can be picked up by a carrier gas. The DMZn, DMCd, and DiPTe are all liquid sources contained in stainless steel bubblers. These bubblers are maintained in thermostat controlled baths to give the desired vapour pressure. Their vapours are carried to a gas switching manifold by hydrogen gas (the carrier gas) which has been purified by a palladium diffuser. The metalorganic components are then made to flow either into the reactor or are vented to an exhaust line. The reactor is comprised of a silica glass envelope containing a substrate heater (susceptor) made of stainless steel, see figure 5.3. The growth system was originally designed for the growth of $Cd_{1-x}Hg_xTe$ and therefore has a boat at the front of the reactor, specifically for the elemental Hg source. In the doping experiments discussed in section 5.7, this boat contains lumps of elemental arsenic, which are independently heated to give the required vapour pressure.

On entering the reactor the incoming hydrogen diluted metalorganic vapours (where appropriate passing over the boat and entraining vapour from the heated arsenic within it) pass over the stainless steel susceptor on which the substrate is

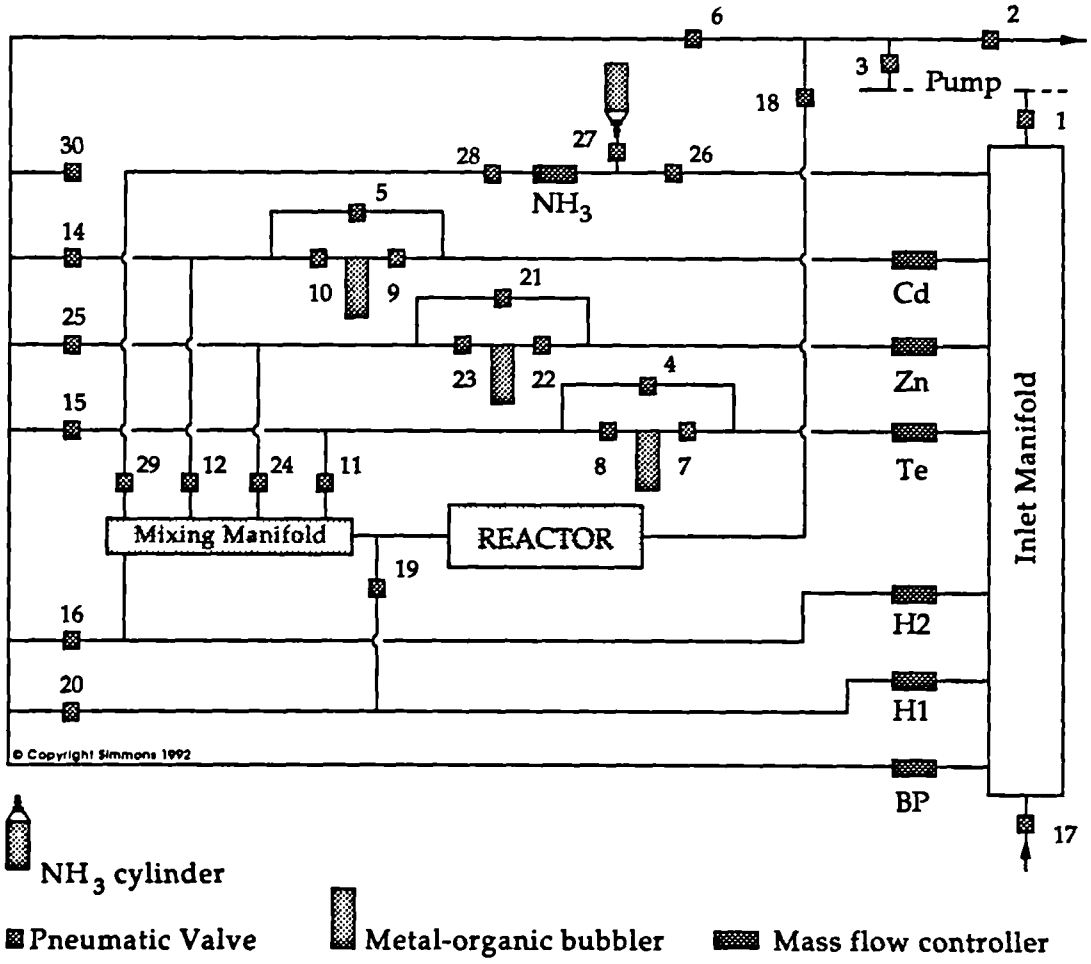

Figure 5.2 A schematic diagram of the MOVPE growth system.

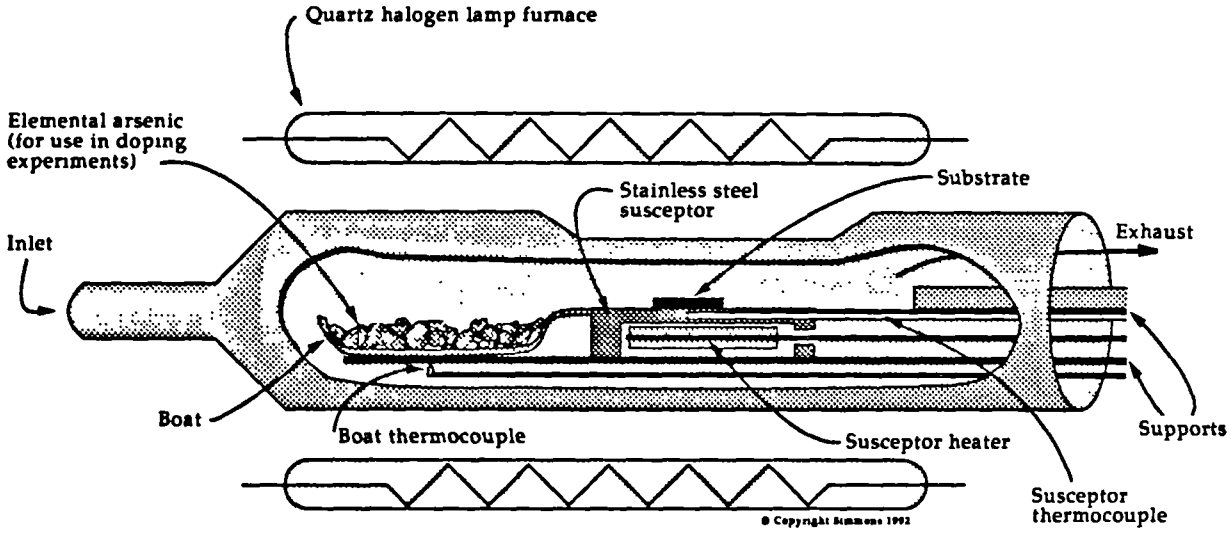

Figure 5.3 The MOVPE reactor.

located, decompose and deposit the epitaxial layer. The pyrolysis of the metalorganic compounds determines the growth temperature which must be significantly lower than the melting point of the material being grown. The susceptor is resistively heated, using a mica covered molybdenum wire, to the temperature necessary to crack the metalorganics and thus release the reactants for growth. A furnace consisting of four 750 W quartz halogen bulbs was used to heat the boat containing the elemental arsenic lumps through the reactor wall, to provide the required arsenic vapour pressure. Heating the reactor walls downstream and above the arsenic boat meant that no arsenic could condense prior to reaching the substrate. The reactor was fairly long in design ($\approx$70cm) with a silica liner incorporated at the end to condense out any involatile unreacted gases or reaction products. A compressed air cooling collar was incorporated for this purpose. The reactor was designed to provide laminar flow across the substrate by including a flat plate in the silica glass envelope immediately above the susceptor. This is known to improve the uniformity of the layers grown [9].

The gas handling system was fairly complicated, the purified hydrogen is passed through a series of mass flow controllers which regulate the flow rates passing through the different bubblers. The system utilises a vent-run system, where vapours are switched between the reactor inlet and the bypass by the switching manifold. It was possible to allow a hydrogen supply directly to the reactor via mass flow controllers H1 and H2, in order to provide a dilution flow during growth and for heat cleaning. A hydrogen flow was always maintained in the bypass (BP) to ensure that all residual metalorganics were flushed out of the system. The precursors used in this work were highly toxic and extreme care was taken at all times during the various procedures involved in the growth process. All waste vapours were passed through two sets of filters before being released into the fume extract. Firstly particulates were removed by a sub-micron dust filter, whilst an activated graphite filter was used to absorb any unreacted metalorganics and uncondensed arsenic. Regular helium leak testing was carried out by pressurising the growth system with helium via a separate inlet into the inlet manifold and thus using an Edwards helium leak detector to test for leaks.

Initial ammonia doping trials required the addition of a separate, independant doping line. A small ammonia gas bottle of 99.9999% purity was installed with its

own mass flow controller, into a line capable of being flushed by hydrogen from the inlet manifold as shown in figure 5.2. The flow rate of ammonia gas was regulated by the mass flow contoller, and at the end of doping experiments the gas bottle was closed and the dopant line flushed free of any residual or adsorbed ammonia.

The mass flow controllers, temperature controllers and pressure transducers were all interfaced to a microcomputer by a series of digital to analogue and analogue to digital convertors. The whole system had a manual overide, necesary in case of a fault or for the leak testing procedures. The status of all the temperatures, pressures and flow rates was monitored by a microcomputer and displayed instantaneously on the computer screen. It was thus possible with the control of all growth parameters to program any growth sequence required. For the p-i-n structure, for example, layers of ZnTe were grown onto layers of CdTe grown on different substrates. The ability to switch gases to obtain abrupt interfaces in these devices is vital in the quest for high efficiency in order to prevent cross-diffusion at the interfaces.

5.4 CdTe layers on {100}GaAs substrates

5.4.1 Introduction

The growth of CdTe onto GaAs as an alternative hybrid substrate for the epitaxial growth of $Cd_{1-x}Hg_xTe$ has generated significant interest, despite the large lattice mismatch encountered (14.6%). The crystal quality of CdTe layers produced in this way has been shown to be comparable to that of bulk CdTe. Moreover GaAs is a viable alternative substrate since high quality GaAs is readily available at a low cost and large area.

In both MBE and MOVPE of CdTe on (100)GaAs two different epitaxial relationships have been found : $(100)_{CdTe}\|(100)_{GaAs}$ [17-20] and $(111)_{CdTe}\|(100)_{GaAs}$ [21-24]. The (111)CdTe was thought to be the preferred orientation due to the smaller discrepancy in interatomic spacing of the parallel planes in the (111)CdTe on (100)GaAs i.e the $[211]_{CdTe}\|$ $[011]_{GaAs}$. In this configuration the spacing of the

Growth Technique	Growth temp./°C	Heat Clean temp./°C	CdTe layer observation	Reference
MBE	225	-	Te growth forces (111)CdTe	22
PLE	260	400	No oxide-(100)CdTe	30
MBE	325	550 582	O_2 on surface-(100)CdTe Ga-Te bonds, (111)CdTe	26
MOVPE	350-440	-	(100)CdTe	33
MBE	250	600	Both (100) and (111)CdTe no O_2 on either surface	27
MBE	300	300-480 > 580	O_2 on surface-(100)CdTe no O_2- (111)CdTe	25
MBE MOVPE	325 350-420	580 580	No oxide, initial Te growth forces (111)CdTe otherwise (100)CdTe	28
MOCVD	450-540	600	growth rate determines orientation, 2μm/hr.-(100) 4μm/hr.-(111)	31
MBE	275-325	582	Ga-rich surface-(111)CdTe Te-rich surface-(100)CdTe	21
MBE	300-450	600	(100)CdTe	32
HWE	400	600	(100)CdTe	35
MBE	300	<480 >480	(100)CdTe (111)CdTe	18
MOCVD	370	585	(111)CdTe (100)CdTe	23
MBE	275-300	580	As-rich surface - (100)CdTe Ga-rich surface - (111)CdTe	29
HWE	300	400-520 580-610	(100)CdTe (111)CdTe	13
Photo-MOVPE	165	600	(111)CdTe	34

Table 5.3 — Summary of the findings of CdTe growth on {100}GaAs

atoms in the parallel plane differ by 0.7%, compared to the 14.6% difference in the (100)CdTe on (100)GaAs [25]. Other authors [26] suggested that a thin residual oxide on the GaAs surface was necessary to permit growth of (100)CdTe. However, these observations were denied by other groups who nucleated (100)CdTe on oxide free (100)GaAs at elevated temperatures [21,25].

All experimental investigations agree that whether (111) or (100)CdTe epitaxy occurs on (100)GaAs is controlled by the substrate preheating temperature. At temperatures greater than 580°C in situ RHEED diffraction patterns indicated the existence of a Ga-rich surface on which (111)CdTe epitaxy was found [18,26]. For lower substrate preheating temperatures (100) epitaxy is observed, the role of oxygen however remains controversial. Feldman et al [28] found that not only oxygen but tellurium itself was present in excess on the (100)GaAs prior to (100)CdTe growth. Shirwana [29] et al confirmed the importance of the GaAs substrate preparation, proposing that if the surface was As-rich then (100)CdTe would result, and if Ga-rich (111)CdTe. Table 5.3 summarises the findings of these authors.

Other important controllable parameters affecting the epilayer quality are the substrate temperature, the II:VI ratio, the total flow rate and the partial pressure of the reactants. Extensive studies in the growth of epitaxial layers by MOVPE have shown that the purity of the semiconducting layer is often determined not only by the purity of the precursors, but also by the diffusion of substrate atoms at high growth temperatures [36]. The use of DiPTe with a lower growth temperature is thought to reduce these autodoping effects.

5.4.2 Growth Conditions

After loading into the MOVPE reactor, the polished {100}GaAs substrates were heat cleaned at 600°C for ten minutes to prepare the surfaces for epitaxy. A systematic study of the effects of temperature, II:VI precursor ratios, and dilution flow on the growth rate and layer properties were examined. CdTe epitaxial layers were grown under Cd-rich conditions at temperatures of 350°C, 325°C and 300°C. Following this layers of CdTe were grown at 325°C at different II:VI precursor ratios (3:1, 1:1 and 1:3 Cd:Te). The growth parameters of all CdTe epilayers are summarised in table 5.4.

Sample	Heat clean	T_{growth}	Dilution flow /SCCM	Cd/ moles /min	Te/ moles /min	II:VI ratio	Growth time	Thickness	Growth rate
CdTe/4	550°C for 10 mins	350°C	5000	1.64×10^{-4}	5.55×10^{-5}	3:1	1hr.	4 μm	$11.1 Å s^{-1}$
CdTe/11	550°C for 10 mins	325°C	5000	1.64×10^{-4}	5.55×10^{-5}	3:1	1hr.	2.5μm	$6.9 Å s^{-1}$
CdTe/5	550°C for 10 mins	300°C	5000	1.64×10^{-4}	5.55×10^{-5}	3:1	1hr.	1.43μm	$4.0 Å s^{-1}$
CdTe/M1	600°C for 10 mins	325°C	7000	5.33×10^{-5}	5.33×10^{-5}	1:1	1hr.	2.5μm	$6.9 Å s^{-1}$
CdTe/M2	600°C for 10 mins	325°C	7000	1.77×10^{-5}	5.33×10^{-5}	1:3	1hr.	1.5μm	$4.2 Å s^{-1}$
CdTe/M3	600°C for 10 mins	325°C	7000	5.33×10^{-5}	1.77×10^{-5}	3:1	1hr.	3.5μm	$9.7 Å s^{-1}$

Table 5.4 — CdTe growth parameters

All layers were analysed by RHEED to determine the crystallinity of the layers, and by SEM to observe the surface morphology. Cross sectional SEM micrographs were used to determine the thicknesses of layers grown, whilst double crystal x-ray diffraction (DCXRD) was used to study layer quality.

5.4.3 Properties of CdTe epilayers

Previous studies (see section 5.4.1) have suggested that a preheat treatment at 600°C would not only remove any oxides but would leave a Ga-rich {100} surface on which only a {111}CdTe layer would nucleate [29]. However, all CdTe layers grown on {100}GaAs in this laboratory have been (100) oriented. RHEED analysis of a <110> pattern at 90° to a <1$\bar{1}$0> pattern confirms a (100) oriented CdTe epilayer. The only possible explanation for this phenomenon is that somehow the surface produced after the heat treatment is rich in tellurium. Despite tellurium being known as a slow diffuser, relatively few studies have been considered with tellurium as a dopant [37], since it has been shown to adsorb to the reactor walls. This adsorption to the stainless steel reactor walls has been demonstrated by Y.S. Homg et al [38], who observed a doping memory effect. Indeed the smell of tellurium is frequently associated with telluride based MOVPE growth kits. After a few growth runs the walls of the silica reactor become coated in a thin metallic film. Analysis of the scrappings off the reactor walls by EDAX has confirmed that they were rich in tellurium. It could be possible that during the heat clean the tellurium adsorbed on the pipework and the reactor walls desorbs and coats the sample surface prior to growth. MBE studies of CdTe on {100}GaAs have confirmed that {100}CdTe oriented layers are always nucleated on a tellurium rich surface [28].

Table 5.5 summarises the results of varying the temperature, II:VI precursor ratios, and dilution flow on the nature of the CdTe epilayers obtained. It can be seen that the smoothest layers of CdTe with the best crystallinity were obtained at a growth temperature of 325°C. Higher temperatures produced layers with a rough pitted surface, and arcing of the spot patterns in RHEED. Lower temperatures produced highly crystalline layers as evidenced by RHEED, but with the presence of a large density of surface deposits. It can be seen that the growth rate of the

Sample	Temp.	II : VI ratio	RHEED	SEM
CdTe/4	350°C	3:1	Untwinned, arcing of spot pattern, scraggy.	Rough, pitted surface, 4μm thickness.
CdTe/11	325°C	3:1	Excellent, streaked, Kikuchi pattern, slight polycrystallinity.	Smooth, slight ridging, 2.5μm thickness.
CdTe/5	300°C	3:1	Excellent, streaked, Kikuchi pattern.	Very smooth, high density of deposits, 1.4μm thickness.
CdTe/M1	325°C	1:1	No polycrystallinity, streaked, no Kikuchi pattern.	Smooth, low density of deposits, 2.5μm thickness.
CdTe/M2	325°C	3:1	No polycrystallinity, strong Kikuchi pattern, highly streaked.	Slightly uneven surface, 1.5μm thickness.
CdTe/M3	325°C	1:3	Cross shaped distribution intensity on <110> axis, slight polycrystallinity.	Ridged surface, 4μm thickness.

Table 5.5 — The results of CdTe growth optimisation

layers decreases as the temperature decreases, indicating that the growth rate is kinetically limited.

The RHEED and SEM micrographs of layers produced at 325°C are given in figures 5.4(a) and 5.4(b) respectively. The <110> pattern reveals a good quality single crystal, with a smooth surface morphology as indicated by the streaks of diffracted intensity lying perpendicular to the shadow edge. The SEM image of this layer reveals a smooth surface morphology, on which a surface defect has been used to focus the image. The corresponding XTEM micrograph of this layer reveals a layer $\approx 1.4\mu$m thick with a high density of threading dislocations, see figure 5.5. This high density of dislocations is expected for a layer that has a lattice mismatch of 14.6% [39].

Varying the II:VI ratio has shown that layers rich in cadmium give a slightly streaked <110> zone RHEED pattern, but have a highly uneven surface. The tellurium rich CdTe was observed to have a thick layer ($\approx 4\mu$m) of highly ridged CdTe with numerous polycrystalline surface deposits. The 1:1 Cd:Te layer is shown to have a smooth surface, with a slight overall undulation. There was a low density of polycrystalline surface deposits and the layer was $\approx$ 2-3μm thick. The <110>

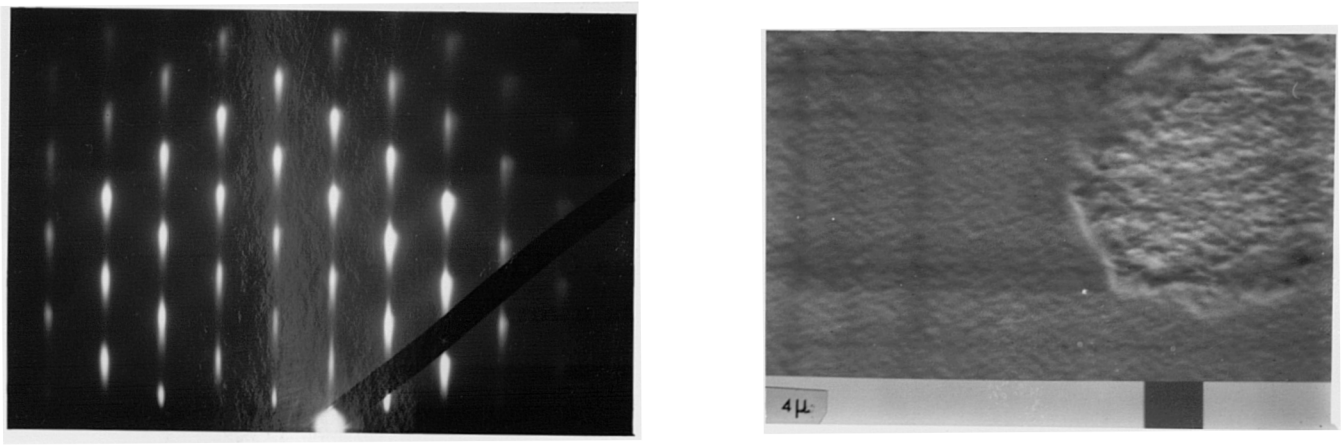

Figure 5.4 — (a)RHEED and (b)SEM micrographs of a layer of CdTe grown at 325°C on {100} GaAs

Figure 5.5 — An XTEM micrograph of a layer of CdTe grown at 325°C on {100} GaAs

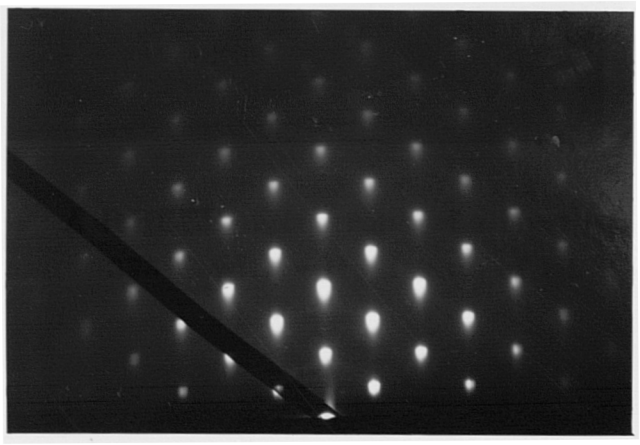

Figure 5.6 — A RHEED micrograph of a layer of CdTe grown at 325°C with a II:VI ratio of 1:1

RHEED pattern of this surface is shown in figure 5.6 and is seen to be highly streaked with strong Kikuchi lines. Analysis of the Te-rich RHEED pattern presented in figure 5.7(a) reveals a cross-shaped distribution of intensity in the spot pattern for an incident electron beam parallel to the <110> plane. If the pattern is rotated 90° about this zone axis to the <1$\bar{1}$0> axis this streaking is not observed, as seen in figure 5.7(b). Similar behaviour has been observed in layers of ZnTe grown at high temperatures [40]. Here reflections are occurring from (111) surfaces in a (100) oriented layer. The beam is perpendicular to a <110> zone axis but reflects off <111> oriented facets on the surface. The acute angle between the streaking in the spot pattern was $\approx 68° \pm 2°$ corresponding to the angle between two successive <111> planes. Figure 5.8 demonstrates the orientation of these defects within the (100) epilayer and it can be seen that when the beam is perpendicular to these defects it appears that they do not exist.

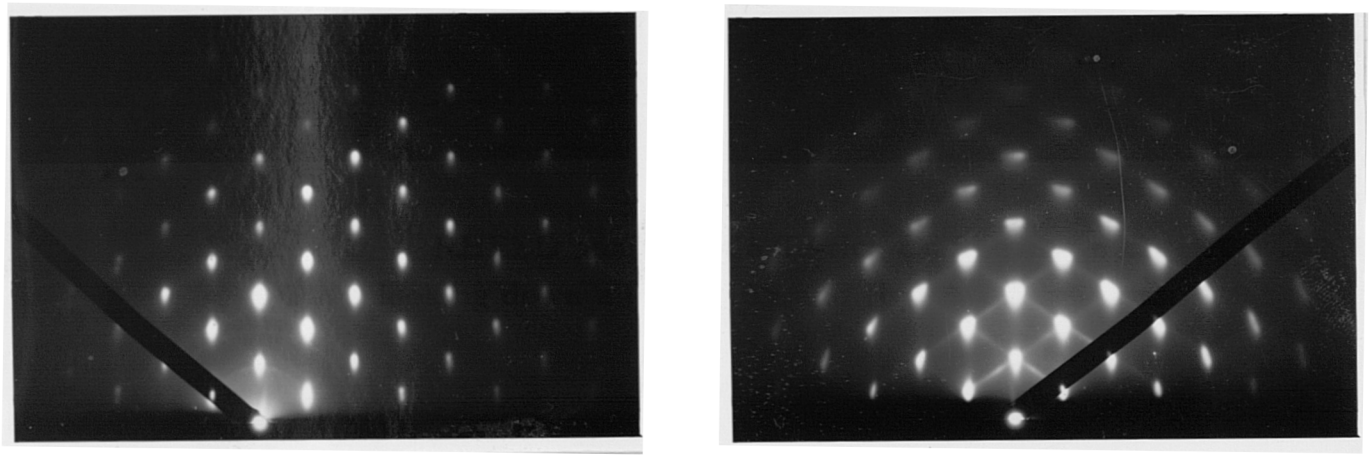

Figure 5.7 — RHEED analysis of a Te-rich CdTe epilayer on {100} GaAs looking down a (a) <110> and (b) <1$\bar{1}$0> zone axis

A double crystal rocking curve (DCXRD) obtained for a 2.5μm thick CdTe layer, grown at 325°C, with a II:VI ratio of 1:1 is shown in figure 5.9. The scan was made with the rocking axis parallel to a <100> crystal axis. The magnitude of the CdTe peak is a factor of $\approx$ 80 times smaller than the peak from the GaAs substrate. The full width half maximum (FWHM) of the CdTe peak is $\approx$ 3000 seconds of arc. Both of these observations indicate that the layer has a high density

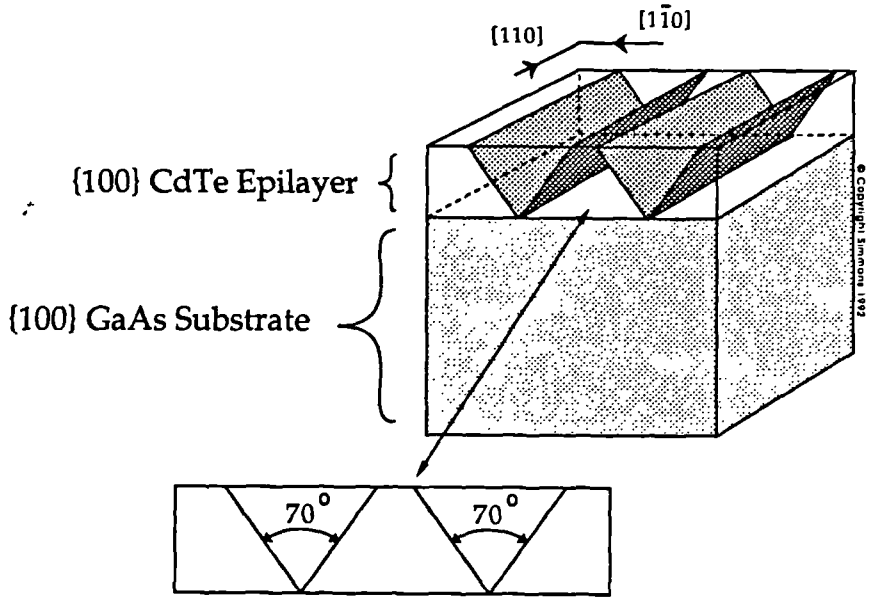

Figure 5.8 — Crystallographic orientation of defects within the {100} oriented CdTe epilayer

of dislocations at the interface as determined by DCXRD which gives a measure of the integrated quality of the surface. Previous studies on CdTe layers grown on {100} GaAs by MOVPE have shown that a 6μm thick layer of CdTe grown on {100} GaAs has a FWHM of 200 arc sec, with thinner layers giving values as high as 2000 arc sec [41]. Recent studies in our laboratories have further optimised the growth process and using the same conditions have achieved rocking curve widths with FWHM of $\approx$ 1200 seconds of arc for a 2μm thick layer [42].

Photoluminescence (PL) spectra of CdTe epilayers grown under Cd-rich conditions, as with CdTe/11, at Durham have been reported elsewhere [43]. The spectra showed a free exciton line at 1.595 eV with a relatively narrow acceptor line at 1.589 eV and a bound exciton at 1.593 eV. These results conform with similar spectra reported by Zanio et al [44]. Another shallow acceptor at 1.565 eV was observed but no deep emission centres were observed. The line at 1.565 eV could be related to weak donor-acceptor pair luminescence, as observed by Schikora et al [45], but its origin is not known. The (A°,X) line at 1.589 eV has also been reported for p-type CdTe films [46].

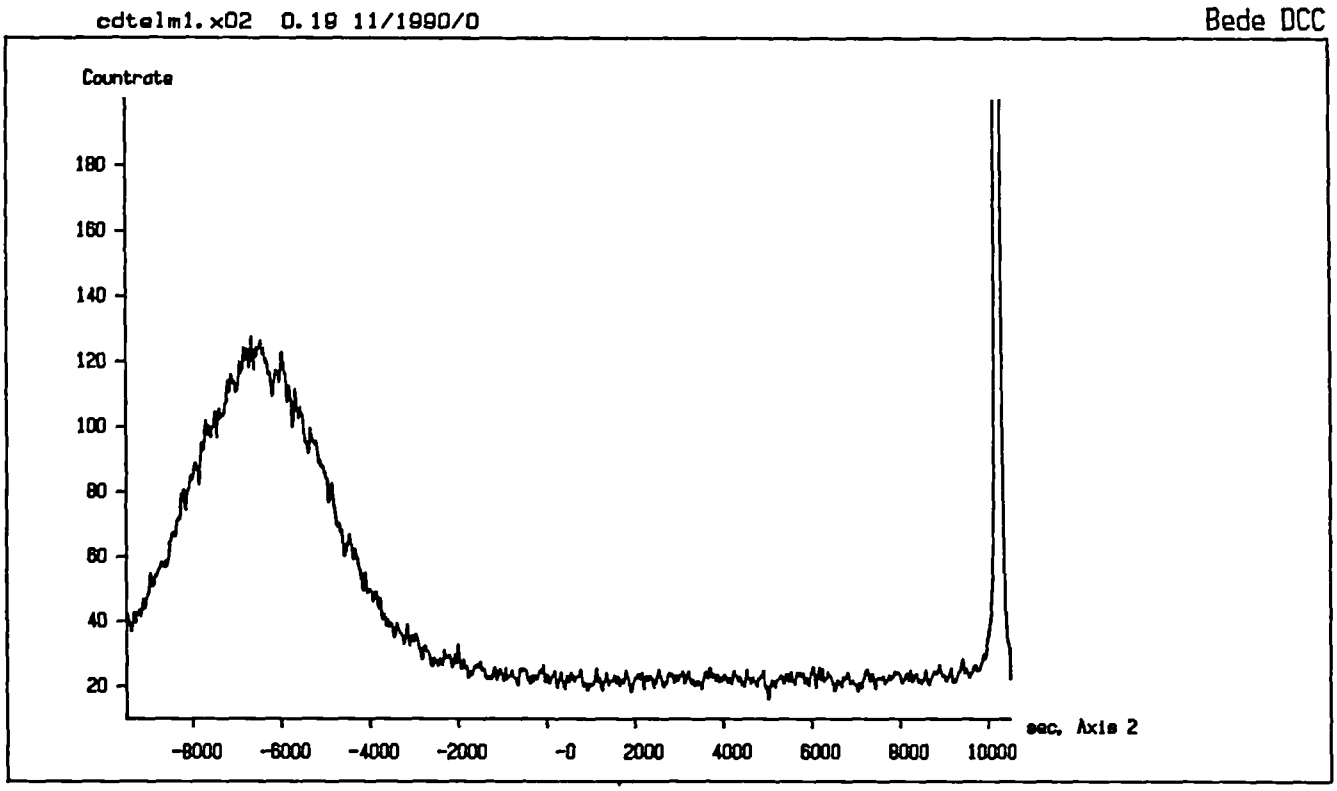

Figure 5.9 — A double crystal rocking curve of a CdTe layer grown on {100} GaAs

Single crystal {100} oriented layers of CdTe have been grown on {100} GaAs substrates by MOVPE. Layers were found to have a high density of threading dislocations leading to a large FWHM of 3000 arc sec as observed by DCXRD. This is to be expected for a system with a high lattice mismatch of 14.6%. Cd-rich or stoichiometric layers were found to support better crystallinity and smoother surface morphologies, whilst PL confirmed the lack of any deep emission centres.

5.5 CdTe on other substrates

5.5.1 Introduction

Following the study of CdTe on {100} GaAs conducted in section 5.4 epilayers of CdTe, using optimised growth conditions, were grown onto {0001} CdS, {01$\bar{1}$6} CdS and {111} CdTe single crystal substrates for the preparation of the solar cell devices discussed in chapters 6, 7 and 8. The epitaxial growth of CdTe onto

CdS single crystal had not been previously reported in the literature, however the reverse process of CdS epitaxy using vacuum evaporation of CdS on {111}CdTe was studied by Awan et al [53]. Awan observed that layers of {0001} oriented CdS approximately 5-8μm thick were found to deposit on these surfaces at 190°C for a growth time of between 10-25 minutes. The reverse process could in principle offer better quality solar cells due to the ability to be able to control the CdTe thickness and conductivity. Other findings indicated that $(01\bar{1}6)$ CdS epilayers grown on (221)CdTe did not contain surface cracks and were therefore thought to be advantageous for growth.

The presence of precipitates and other defects associated with the bulk CdTe which normally serve as dislocation nucleation sites are removed using hydroplane polishing thereby reducing the number of threading dislocations propagating into the epilayer. The homoepitaxial growth of CdTe could thus produce epilayers with a reduced density of defects compared to other substrates. Epitaxial films of CdTe deposited on CdTe substrates by MOVPE often exhibit crystallographic growth facets, typically referred to as hillocks [48-51]. Hails et al [50] noticed the formation of pyramidal facetted features in twin related orientation form on the surface of the (111)A homoepitaxial layers whilst lamellae twins were found parallel to the interface in homoepitaxial CdTe layers on the $(\bar{1}\bar{1}\bar{1})$B face.

5.5.2 Epitaxial growth of CdTe on {0001} and $\{01\bar{1}6\}$ CdS

Intrinsic, {0001} oriented, mechanically polished wafers of CdS, supplied by Eagle-Picher with resistivities in the order of 5-8 Ωcm were used, the polarity being identified by the suppliers. In addition, undoped CdS grown in our laboratories [52] with resistivities in the order of several kilo-ohm cm^{-1}, and oriented on the $\{01\bar{1}6\}$ planes were used. Awan [53] found that the best epitaxy, i.e. the best crystallinity and morphology were obtained on {221} surfaces of CdTe. The epitaxial relationship for this orientation was found to be $\{221\}_{CdTe}\|\{01\bar{1}6\}_{CdS}$. In order to obtain high quality CdTe it was decided to try the opposite process by the epitaxial growth of CdTe on the $\{01\bar{1}6\}$ surfaces of single crystal CdS, with the possibility of avoiding twinning in the epilayer. This unusual orientation was found, using equation 5.1 for a hexagonal crystal system to be 17° off the basal

for a hexagonal crystal system to be 17° off the basal plane, see figure 5.10. For the hexagonal system the angle, ϕ between two faces ($h_1k_1l_1$) and ($h_2k_2l_2$) is given by [54]

$$cos\phi = \frac{h_1h_2 + k_1k_2 + \frac{1}{2}(h_1k_2 + k_1h_2) + \frac{3}{4}(\frac{a^2}{c^2})l_1l_2}{\sqrt{[h_1^2 + k_1^2 + h_1k_1 + \frac{3}{4}(\frac{a^2}{c^2})l_1^2][h_2^2 + k_2^2 + h_2k_2 + \frac{3}{4}(\frac{a^2}{c^2})l_2^2]}} \qquad [5.1]$$

where a and c are the lattice parameters of the CdS hexagonal crystal system and h,k and l are the unit cell vectors. CdS single crystals were then oriented to the $\{01\bar{1}6\}$ planes (see figure 5.10) using Laue x-ray back reflection.

After polishing the substrates, as described in chapter 4 they were loaded into the MOVPE reactor and given a precautionary heat clean at 410°C for ten minutes under hydrogen. The growth temperatures and flow rates were selected on the basis of earlier experience with the deposition of CdTe onto GaAs substrates. Growth took place in a hydrogen carrier gas at 325°C using a II-VI ratio rich in cadmium and with a total flow rate of 5000 SCCM. The growth time was typically 60 minutes, during which layers of CdTe $\approx 1\mu$m thick were deposited. Layers were then assessed by RHEED, SEM and XTEM.

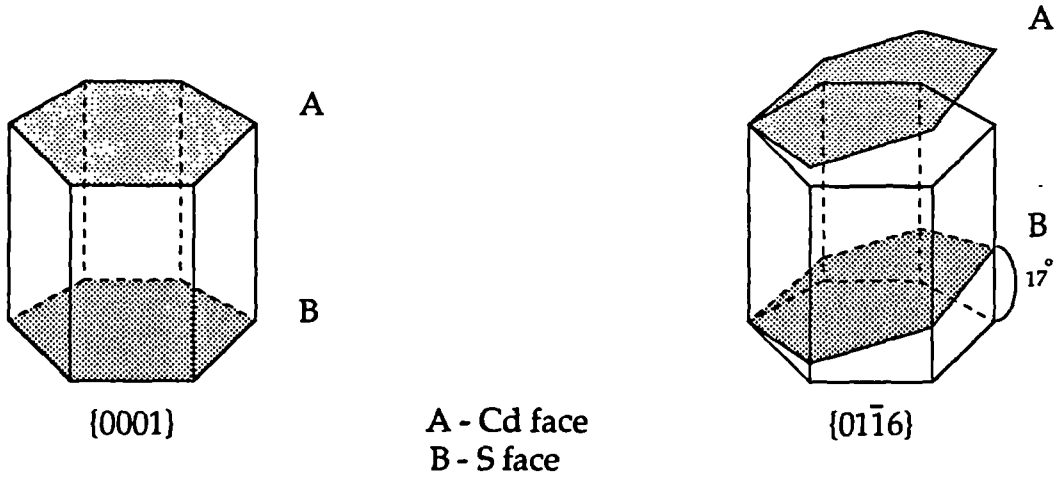

Figure 5.10 — The {0001} and {01$\bar{1}$6} planes in single crystal CdS

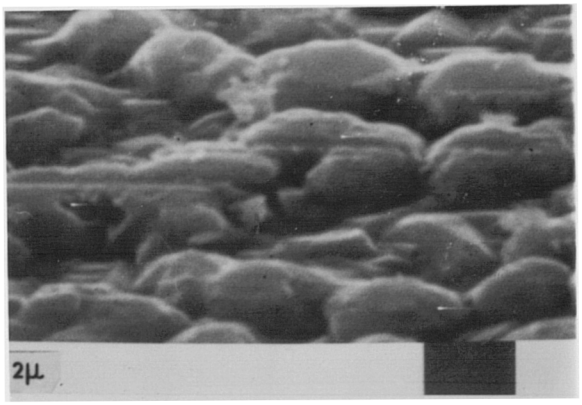

Figure 5.11 — An SEM micrograph of a CdTe epilayer on (0001)A CdS

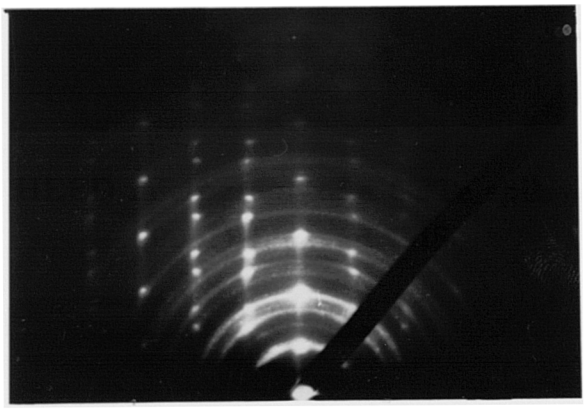

Figure 5.12 — RHEED micrograph of a CdTe epilayer formed on the $(000\bar{1})$B face of CdS

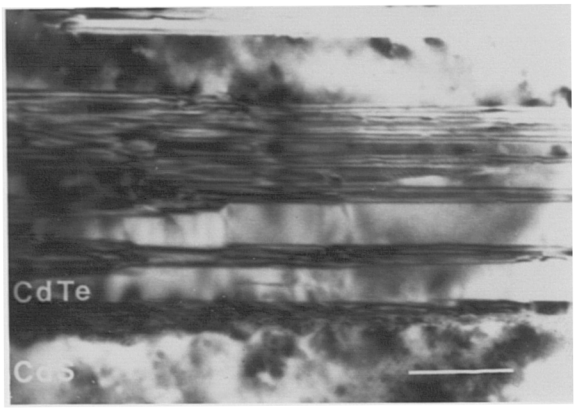

Figure 5.13 — XTEM micrograph of 0.75μm thick layer of CdTe grown on the $(000\bar{1})$B face of CdS

Layers of CdTe on (0001)A CdS were matt in appearance and uneven in texture. Examination of the films in the SEM revealed a high density of irregular hillocks superimposed on a background of triangular facetted features, as shown in figure 5.11. The latter indicate a <111> growth direction. Furthermore the two orientations of triangular features present indicate that the layers contain twin islands. Assessment of the films using RHEED showed them to have a random polycrystalline structure. Since RHEED is surface selective this demonstrates that the irregular hillocks are randomly oriented crystallites and the suggestion is that these are superimposed on a twinned layer of material.

Layers of CdTe grown on the $(000\bar{1})$B surface of CdS were shiny. However the SEM revealed a low density of hillocks similar to those observed on the (0001)A surface, these being superimposed on a smooth background. RHEED patterns confirmed that the epitaxial relationship was $\{111\}_{CdTe} \| (000\bar{1})B_{CdS}$. The pattern shown in figure 5.12 contains rings indicating the presence of polycrystalline surface deposits. Pairing of the spots reveals that the epilayer is twinned. Observation in cross sectional TEM demonstrated a film of thickness 0.75μm with a large number twin lamellae lying parallel to the epilayer/substrate interface (see figure 5.13). Transmission diffraction patterns taken from the same sample confirmed this and established that the $<110>_{CdTe} \| <1\bar{2}10>_{CdS}$ relationship existed.

From equation 5.1 it can be seen that the $\{01\bar{1}6\}$ plane is 17° off the {0001} basal plane of CdS and it is expected that this unusual orientation still retains polarity at its surfaces. In order to test this theory wafers of CdS oriented on the basal plane were oriented and cut from a single crystal boule. The polarity of these surfaces was then determined and the boule realigned to the $\{01\bar{1}6\}$ plane where two wafers were cut. It was necessary to cut two wafers from the crystal in order to obtain a wafer of uniform thickness, see figure 5.14. The original wafer predetermined the polarity direction, subsequent wafers following this convention. It was thus observed that the (0001)A face for the basal plane, which turned dull on etching was also the same polarity as the $(01\bar{1}6)$A face, which too turned dull on etching. It is impossible to conclude that this face is solely constructed of Cd atoms but it appears that this orientation still retains some degree of polarity. The polar surfaces of the $\{01\bar{1}6\}$ oriented layers are thus defined as the Cd-dominated $(01\bar{1}6)$A face and the S-dominated $(01\bar{1}\bar{6})$B face.

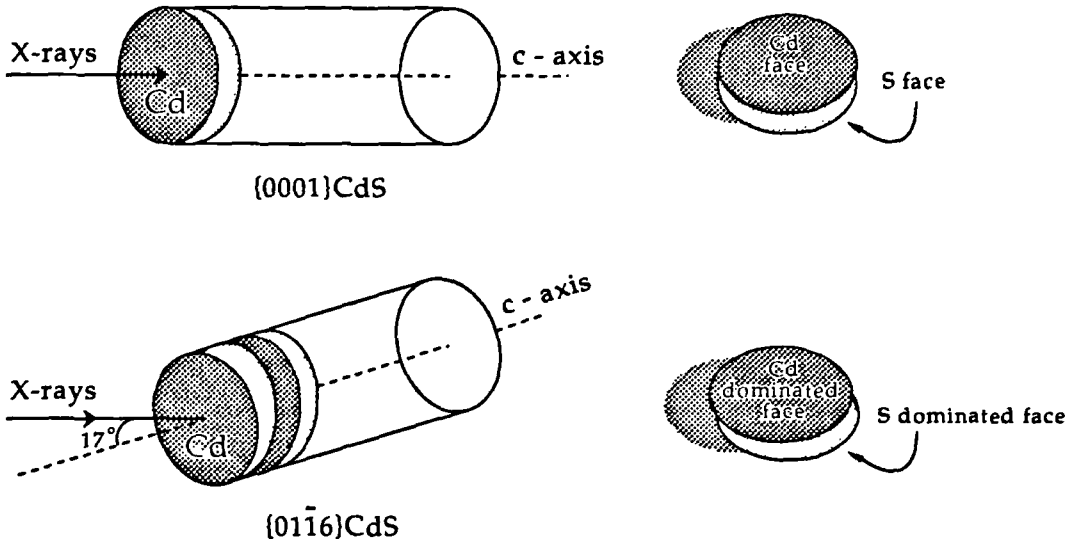

Figure 5.14 — The polarity of the {01$\bar{1}$6} CdS surfaces

CdTe growth on the two {01$\bar{1}$6} surfaces was highly sensitive to crystallographic polarity : one surface was matt and dull, whilst the other was mirror-like. Examination of the dull surface in the SEM revealed the presence of irregular hillocks on a smooth background see figure 5.15, the hillocks being similar to those observed on the {0001} surfaces. RHEED patterns taken from the CdTe layers consisted of smooth rings indicating a polycrystalline structure. The opposite shiny surface was characterised by an array of scratches as shown in figure 5.16(a), and exhibited only a low density of hillocks. The scratches corresponded to features which remained following the chemical and mechanical polishing procedures. A RHEED pattern taken from the same surface is shown in figure 5.16(b) which indicates that the film is epitaxial although there are some polycrystalline surface deposits. The spot pattern corresponds to a <112> zone axis and rotation of the sample enabled a <$\bar{3}\bar{2}\bar{1}$> pattern to be obtained. These indicate a {37$\bar{5}$} surface plane which is 8.9° off the nearest {221} plane. Cross sectional TEM micrographs of these layers grown on the S-dominated face revealed that these layers also contained a high density of lamellar twins inclined to the heterointerface as shown in figure 5.17(a). The beam direction is close to the <110> plane in the CdTe and to the <1$\bar{2}$10> in the CdS. The twin lamellae are at $\approx$ 17° to the basal plane

of CdS (i.e the same angle as the $\{01\bar{1}6\}$ plane is to the $\{0001\}$ plane). Figure 5.17(b) shows a selected area diffraction pattern for the corresponding layer. it can be seen that there is a small degree of misorientation ($\approx 2°$) between the close packed planes in the epilayer and the substrate, and this could be caused by a slight deviation of the substrate orientation from the exact $\{01\bar{1}6\}$ plane.

The finding that the best epitaxy was only achieved on non-metal close packed $(000\bar{1})$B and $(01\bar{1}\bar{6})$B surfaces by MOVPE is consistent with observations of CdTe epitaxy on other polar substrates. For example, layers having good morphology are only obtained on the non-metal surfaces of {111}GaAs [55] and CdTe [56]. Furthermore the presence of lamellar twins within {111} oriented CdTe layers grown on the $(000\bar{1})$B CdS substrates are similar to those observed in layers grown on GaAs and CdTe [57]. In all three cases the twin lamellae lie on the {111} planes parallel to the epilayer/substrate interface. The CdTe/sapphire system provides a further example for comparison [58]. In this case, growth on the {0001} sapphire planes also produced {111} oriented CdTe epilayers which were twinned in an identical manner to those shown for the CdS/CdTe layers. Twinning of this type in {111}oriented epilayers may be thought of as resulting from growth accidents on the low energy close packed surfaces. Aindow et al [58] also identified a hexagonal array of misfit dislocations at the CdTe/sapphire interface. Although no such array has yet been observed in the CdS/CdTe system it is likely that misfit will have to be accommodated in a similar manner.

The observation of inferior epitaxial growth on the (0001)A CdS surface is in accordance with the results of MOVPE growth on the {111}A surfaces of CdTe and GaAs [56,57]. However, an interesting feature of the layers grown on the (0001)A CdS is that there is an underlayer of epitaxial material interspaced with twin islands as shown in figure 5.11. These are similar to those observed on $Cd_{1-x}Hg_xTe$ epilayers on the $\{\bar{1}\bar{1}\bar{1}\}$B surface of CdTe [56]. This indicates that twinning in these layers is nucleated at the epilayer/substrate interface as opposed to being a result of post nucleation growth events within the bulk of the CdTe epilayer.

The polarity sensitive growth of CdTe on the $\{01\bar{1}6\}$ surfaces of CdS is in accordance with the results of growth on polar {0001} surfaces. The polarity of these surfaces was more difficult to define, but it is proposed that the surface

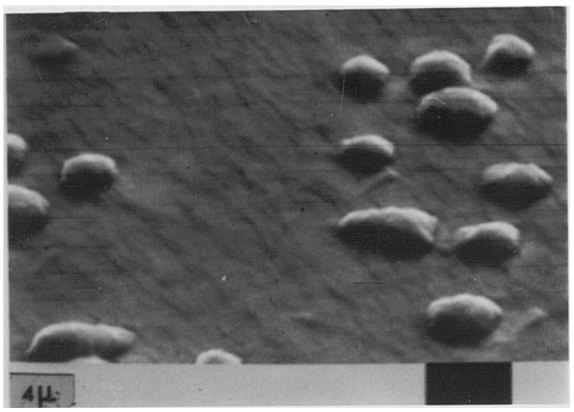

Figure 5.15 — An SEM micrograph of a CdTe epilayer on the $(01\bar{1}6)$A face of CdS

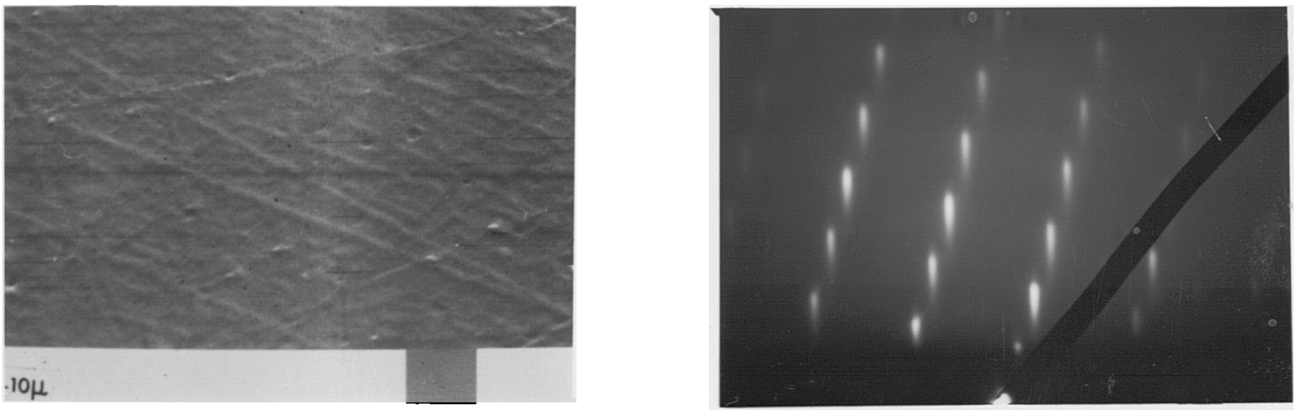

Figure 5.16 — The (a) SEM and (b) RHEED micrographs of a CdTe epilayer on the $(01\bar{1}\bar{6})$B face of CdS

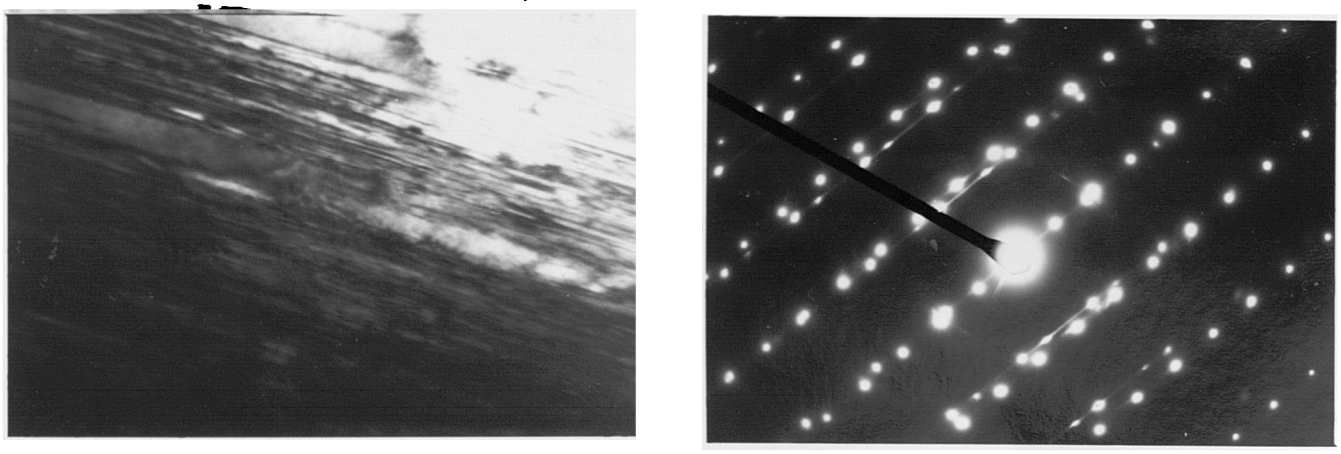

Figure 5.17 — (a) An XTEM micrograph and (b) selected area diffraction pattern of the CdTe epilayer on the $(01\bar{1}\bar{6})$B face of CdS

supporting best epitaxy is likely to be that dominated by S atoms i.e the $(01\bar{1}\bar{6})$B surfaces. The finding that the growth direction of CdTe on $(01\bar{1}\bar{6})B_{CdS}$ is <$37\bar{5}$> is not consistent with the epitaxial relationship of $\{01\bar{1}6\}_{CdS}\|\{221\}_{CdTe}$ reported by Awan et al [53] for the inverse case of CdS epitaxy on CdTe. This apparent discrepancy might be explained by the fact that the two epitaxial relationships differ by only 8.9°. XTEM results indicate that the CdS is misoriented from the $\{01\bar{1}6\}$ surface by as much as 2°, which could explain this unusual relationship. Twins observed in the CdTe grown on $\{01\bar{1}6\}$CdS are probably surface nucleated, the $\{01\bar{1}6\}$ surface being almost entirely made up of basal and prismatic plane segments. Clearly the use of this unusual orientation does not eliminate twinning in CdTe as was initially expected [59].

5.5.3 Homoepitaxial growth on $(\bar{1}\bar{1}\bar{1})$B CdTe

The homoepitaxial growth of CdTe has previously been investigated due to its use as a buffer layer in the growth of $Cd_{1-x}Hg_xTe$. The buffer layer has been shown to eliminate the effects of surface contaminants on the bulk CdTe and provide an atomically clean surface for subsequent growth [60]. The growth of CdTe onto (111)A and $(\bar{1}\bar{1}\bar{1})$B CdTe substrates by MOVPE has been demonstrated by Hails et al [56], however the polarity of the {111} surfaces was determined by the erroneous Warekois etch. The corrected configuration of this etch [61] has now shown that lamellar twins are now observed lying parallel to the substrate/epilayer interface on the $(\bar{1}\bar{1}\bar{1})$B surface. Layers grown on the A face were found to be matt in appearance and uneven in texture, due to the occurrence of triangular pyramidal facets on this surface. {111}CdTe single crystal wafers of unknown conductivity were supplied by Philips. These wafers were annealed for 48 hours in Cd at 600°C to produce n-type CdTe of resistivity 1.64×10^{-4} Ωcm. The wafers were then dipped in a solution of 1:1:1 HF, HNO_3 and CH_3CO_2H for 15 seconds to discriminate the A(Cd-rich) and B(S-rich) surfaces. This etch, named the "black and white etch" leaves the B face bright and reflecting and the A face dull. Epitaxial growth of CdTe on $(\bar{1}\bar{1}\bar{1})$B surfaces was considered for device purposes, since this orientation is known to offer a better surface for epitaxy. Layers of CdTe with a 1:1 Cd:Te ratio were grown for 1 hour at a temperature of 325°C to produce

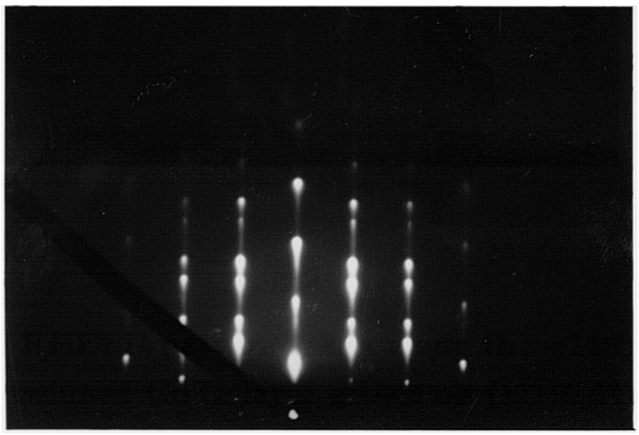

Figure 5.18 — RHEED pattern taken along the <110> zone axis of a twinned CdTe layer grown on $(\bar{1}\bar{1}\bar{1})$CdTe

a film of CdTe approximately 1-2μm thick.

The RHEED pattern of the CdTe epilayer taken along the <110> zone axis is shown in figure 5.18. The pattern consists of rows of single spots separated by 2 rows of double spots and is characteristic of {111} twinned face centered cubic structures. Similar patterns were obtained every 60° rotation about the substrate normal.The CdTe epilayer is thus twinned as with the CdS based heterojunctions. The surface appeared specular to the eye and featureless in SEM. In all the {111} CdTe epilayers examined this highly twinned structure was observed irrespective of the choice of substrate orientation. Its presence in homoepitaxially grown epilayers of {111}CdTe would indicate that the origin of the twinning is a phenomenon of the growth of CdTe on a {111} plane rather than being due to the accommodation of mismatch or to a nucleation process occurring at the interface. Finally in discussing {111} CdTe epilayers it should be mentioned that all samples when tilted in the TEM, such that the dislocations were out of contrast, revealed a high density of dislocations (except in the case of CdTe homoepitaxy).

5.6 Epitaxial growth of ZnTe

5.6.1 Introduction

The ZnTe acts as the window layer in the solar cell devices. For this reason the ZnTe should provide minimum series resistance to the cell, whilst being of sufficiently good quality to prevent excessive optical absorption across it. Thus a thin layer of ZnTe of good crystallinity and high conductivity is required. The thickness must be smaller than the inverse of the absorption coefficient otherwise most of the light will be absorbed across its length. The diffusion length must also be larger than the film thickness so that photogenerated carriers can be collected.

Initially layers of ZnTe were grown on to {100}GaAs in order to optimise growth conditions with the aim of achieving the above objectives. Previous studies of the growth of ZnTe onto {100}GaAs [62] at temperatures of 410°C, using diethyl telluride have shown that the surfaces were found to exhibit anisotropic facetting. Different growth rates on the {111}A and $\{\bar{1}\bar{1}\bar{1}\}$B planes of the sphalerite structure were observed by the formation of anisotropic ridges along only one particular <110> direction [63]. ZnTe layers were found to contain misfit dislocations that extended through the entire epilayer, in contrast with MBE grown samples where dislocations grew out within 0.3μm of the interface [64]. This result may have been related to the higher growth temperature in MOVPE (410°C) and possibly the higher growth rate.

Studies on the growth of ZnTe presented in sections 5.6.2 include the use of a different telluride source leading to a lower temperature growth. The results of this new growth are presented in section 5.6.3.

5.6.2 Growth conditions

A systematic study of growth temperature using the new DiPTe precursor was carried out with a total flow rate of 7000 SCCM and under Zn-rich conditions, at temperatures of 300°C, 325°C and 350°C. The growth conditions are summarised in table 5.6 below. All layers were analysed by RHEED and SEM to observe the

crystallinity and surface morphology respectively. XTEM was used to determine the thickness of the layers grown in order to determine the growth rate at different temperatures. DCXRD was used to assess the crystalline quality of the best layers and PL studies to determine the presence of any defect states.

Sample	Heat clean	T_{growth}	Dilution flow /SCCM	Zn/ moles /min	Te/ moles /min	II:VI ratio	Growth time	Thickness	Growth rate
ZnTe/28	550°C for 10 mins	350°C	5000	1.64×10^{-4}	5.2×10^{-5}	3:1	1hr.	0.89μm	$2.5 Å s^{-1}$
ZnTe/29	550°C for 10 mins	325°C	5000	1.64×10^{-4}	5.2×10^{-5}	3:1	1hr.	0.5μm	$1.39 Å s^{-1}$
ZnTe/30	550°C for 10 mins	300°C	5000	1.64×10^{-4}	5.2×10^{-5}	3:1	1hr.	0.1μm	$0.28 Å s^{-1}$

Table 5.6 — The growth conditions of ZnTe epilayers on {100} GaAs

5.6.3 Properties of ZnTe layers grown

A summary of the ZnTe growth properties is presented in table 5.7. The surfaces of layers grown using DiPTe at lower temperatures were essentially featureless and specular. No evidence of anisotropic ridging was found when the layers were examined in the SEM and generally the diffraction spots in RHEED patterns were found to be streaked in a direction perpendicular to the shadow edge, indicating the flatness of the surface. When grown at higher temperatures (≈350°C) the morphology was invariably less smooth. Figure 5.19(a) shows a RHEED pattern obtained from a ZnTe layer grown on {100} GaAs at 350°C, whilst 5.19(b) shows a SEM micrograph of a ZnTe layer grown at 325°C. As a result of the large lattice mismatch even relatively thin layers ($\approx 0.1 \mu m$) were found to be fully relaxed and therefore contained a large density of misfit dislocations (see figure 5.20). It can be seen that these dislocations extend all through the layer to the surface.

The array of features seen at the interface correspond to an interfacial array

Sample	Temp.	II : VI ratio	RHEED	SEM
ZnTe/28	350 °C	3:1	Strong, streaked <110> pattern.	Ridged surface.
ZnTe/29	325 °C	3:1	Small amount of polycrystallinity.	Smooth, low density of polycrystalline deposits, 1 μm diameter.
ZnTe/30	300 °C	3:1	Excellent spot pattern, slight polycrystallinity.	Smooth, undulating surface, difficult to focus on.

Table 5.7 — Summary of the ZnTe growth properties

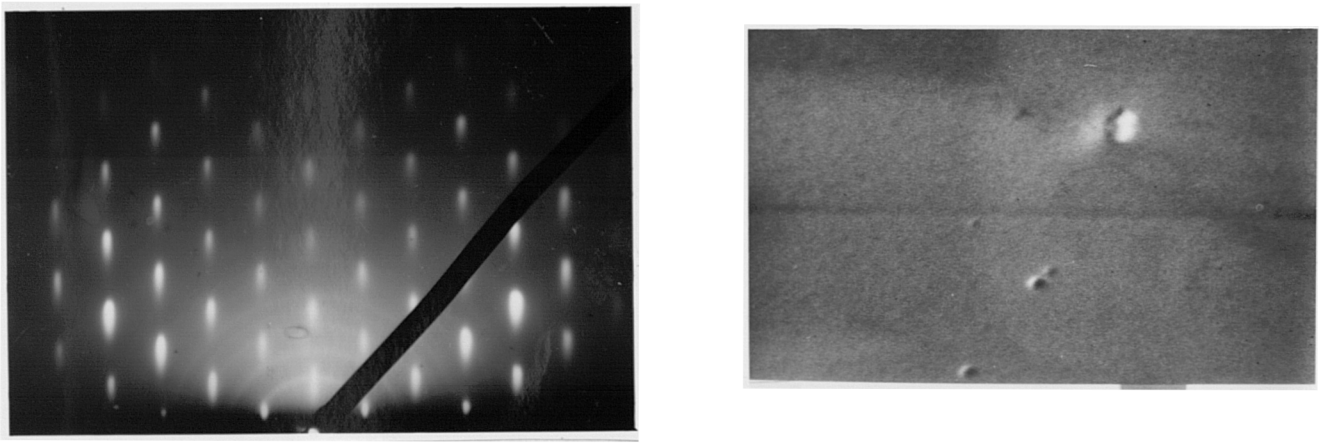

Figure 5.19 — (a) A RHEED and (b) SEM micrograph of a ZnTe layer grown on {100} GaAs

of misfit dislocations which accomodate the misfit strain. Analysis of this pattern using a calibrated electron microscope revealed that the separation of the misfit dislocations was 46±2Å. Assuming that all these dislocations are pure edge dislocations this value compares favourably with that obtained by Feuillet et al [64]. Feuillet found that the expected misfit separation of dislocations at the interface of this epitaxial system was ≈ 50Å.

Figure 5.21 shows an XTEM picture of ZnTe grown at 350°C. The layer was much thicker, ≈ 0.89μm and the system exhibits a high density of threading dislo-

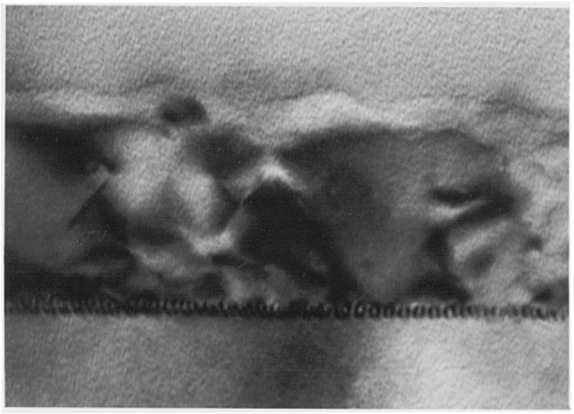

Figure 5.20 — A XTEM micrograph of a 0.1μm thick ZnTe layer on{100} GaAs grown at 325°C

Figure 5.21 — XTEM micrograph of a ZnTe layer grown on {100} GaAs at 350°C

cations ($\approx 6\times10^9$ cm^{-2}) from the mismatched epilayer. The difference in the TEM patterns of the two layers grown at 325 and 350°C confirms that the dislocations grow out to a significant extent through the thickness of the layers. This was also found in layers of CdTe grown on {100} GaAs substrates [65].

A DCXRD rocking curve obtained for a $\approx$ 0.6μm thick layer grown at 325°C revealed it to have a FWHM of 370.5 arc sec. The scan with the rocking curve parallel to a <100> zone axis is shown in figure 5.22 and reveals a misorientation of the ZnTe by $\approx$1° with respect to the GaAs substrate along the [110] axis as observed by Shtrikman et al [41]. The lower growth temperature has offered smaller values of the FWHM as evidenced by the value of >1200 arc sec obtained by Shtrikman for 1μm thick ZnTe layers grown at 410°C.

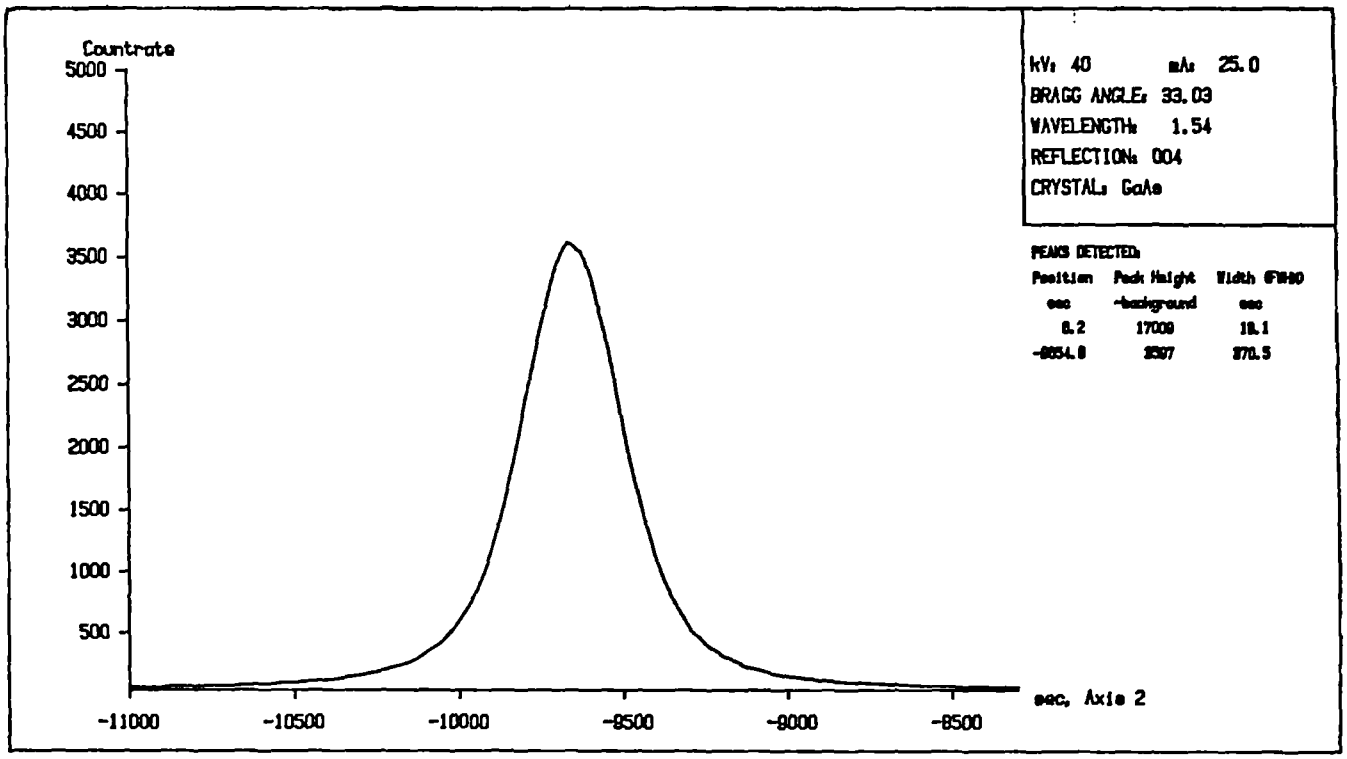

Figure 5.22 — DCXRD rocking curve for a layer of ZnTe grown on {100} GaAs at 325°C

Low temperature (1.2K) PL studies† of a layer of ZnTe grown at 325°C were performed and the corresponding spectra of the exciton region is shown in figure 5.23. A band at 2.147 eV (not shown) was attributed to self activated DAP emission probably involving Ga and As, which had probably diffused from the substrate. From figure 5.22 it can be seen that 5 lines are observed at energies of 2.356, 2.369, 2.347, 2.380 and 2.383 eV. The strongest emission line was at 2.369 eV and this was identified as being due to an acceptor bound exciton (A°,X) probably as a result of As in-diffusion from the substrate; analogous to the Al in-diffusion observed in GaAlAs substrates [66]. The emission at 2.347 eV could be due to either a donor bound exciton (D°,X), possibly Ga or free light hole exciton emission ($X_{1s\pm\frac{1}{2}}$) in which case the line at 2.383 eV would be the strain split heavy hole emission ($X_{1s\pm\frac{3}{2}}$). The line at 2.356 eV is believed to be related to some structural defect, probably the Zn vacancy. Kuhn et al [67] noticed that the intensity of this transition was related to the partial pressure of the Te/Zn. The

† PL measurements were performed by Dr.J.E. Nicholls of Hull University

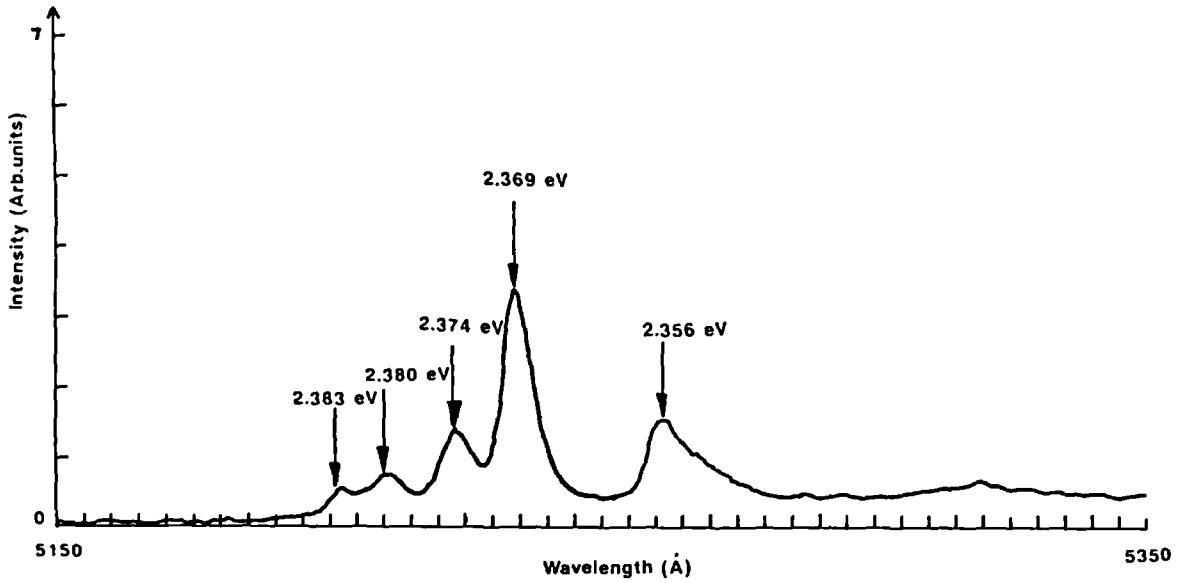

Figure 5.23 — Photoluminescence spectrum of a ZnTe layer grown at 325°C

origin of the 2.380 eV line is unclear, but may be related to gallium autodoping. Photoluminescence has shown that both Ga and As in-diffusion from the substrate was significant. This is consistent with results obtained by other authors [67] and is probably a consequence of the large threading dislocation networks that exist in such mismatched systems.

5.6.4 Growth of p-ZnTe on n-substrate/i-CdTe heterojunctions

It has been found that the morphology of CdTe:ZnTe superlattices was significantly better than either of the constituent binaries grown at the same temperature [68]. Matthews et al [69] found that the critical thickness for the relaxation to the free standing in plane lattice parameter was half the critical thickness of the constituent binary layers, thus it is possible that the growth of ZnTe onto CdTe can produce a higher quality crystal. The effects of the subsequent growth of ZnTe layers on the crystalline quality of layers of CdTe grown on CdS substrates were investigated. Layers of ZnTe were grown in-situ at 325°C, under a 1:1 II:VI ratio and high dilution flows onto epilayers of CdTe on single crystal CdS substrates.

Figure 5.24 confirms that the corresponding RHEED pattern shows no sign of polycrystallinty, but the ZnTe has followed the orientation of the CdTe underneath and is twinned. Surfaces were also shown to be specular as seen by optical and SEM micrographs of the surface.

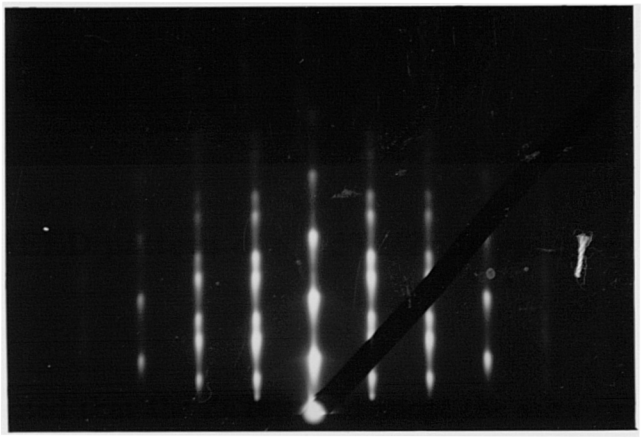

Figure 5.24 — RHEED pattern of a CdTe/ZnTe epilayer on {0001}CdS

It would be expected that the ZnTe would adopt the same orientation as the CdTe epilayer since they are both sphalerite structures. All samples investigated confirmed this, if the CdTe was twinned as in the case of growth on CdTe or CdS substrates then the subsequent ZnTe was also twinned. In the case of ZnTe growth on (100) CdTe for the p-n heterojunction the ZnTe was (100) oriented. It was not possible to observe the particular epilayers that were used for the electrical measurements since this would alter their electrical properties. In all cases the same growth conditions were used and samples were positioned identically on the susceptor. Reproducible growth was observed for all layers grown.

5.7 The doping of ZnTe and CdTe

5.7.1 Introduction

ZnTe and CdTe are the only II-VI semiconductors that can be made easily p-type. Ionisation energies of acceptor states within these materials have been

shown to be practically identical, ranging from 56<E_A <277 meV (see table 5.8). Eight different acceptor levels have been recorded using low temperature photoluminescence studies and all experiments performed on these high purity materials have shown these acceptors are related to substitutional impurities. The acceptor impurities of interest are the alkali metals Li, Na and the monovalent metals Cu, Ag, and Au which substitute for the cation (i.e Zn or Cd in ZnTe and CdTe respectively) and also the group V elements N, P and As which substitute for the anion (i.e Te). The different options for obtaining p-type CdTe/ZnTe are shown in the tree diagram in figure 5.25.

The electrical resistivity of the CdTe and ZnTe films is perhaps the most important property affecting the photovoltaic characteristics of the solar cells. The use of high resistivity CdTe and ZnTe results in low fill factors and low photocurrents, whilst excessive doping of CdTe films leads to low photovoltage as well as low photocurrents. However CdTe and ZnTe are difficult to achieve with the desired conductivity. The introduction of electrically active impurities into the host CdTe or ZnTe crystal induces the formation of electrically active natural defects (vacancies, interstitial atoms etc..) which tend to compensate the electrical activity of the impurity. This "self compensation" is common in all large band gap materials and in particular to partly covalent II-VI compounds such as CdTe and ZnTe [70].

	Li	Na	Cu	Ag	Au	N	P	As
ZnTe	60.5	62.8	148	121	277	-	63.5	79
CdTe	57.8	58.8	147	108	263	56	60	62

Table 5.8 — Acceptor levels in p-type ZnTe and CdTe (all values are in meV)

The introduction of p-type dopants into CdTe and ZnTe is thought to induce the formation of anion vacancies mostly in the doubly charged form. The introduction of such donors would thus reduce the hole density with one of the two anion vacancy electrons compensating the acceptor. With ZnTe two persistent shallow

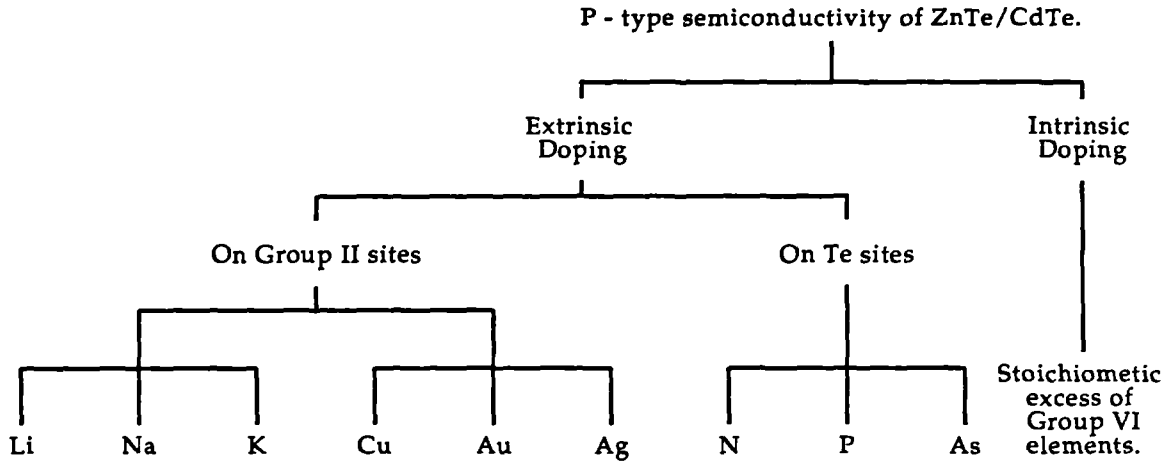

Figure 5.25 — A diagram illustrating the p-type semiconductivtiy of CdTe/ZnTe

acceptor levels at 60 and 150 meV above the valence band are attributed to cation vacancies [71]. Other authors have however attributed these acceptors levels to Cu and Li substitutional species contained within tellurium precipitates at growth [72,73]. Cu is known to diffuse rapidly as interstitials in II-VI compounds [74]. In order to obtain good control of electronic doping careful consideration of the chemical equilibria during crystal growth is paramount. II-VI compounds have a pronounced tendency for defects to agglomerate in the form of precipitates or associates during cooling from high temperature. Excess Te is well known to precipitate in the CdTe epilayer and any impurities contained within it diffuse out [75].

Enthalpy considerations confirm that the group I impurities Cu, Ag and Au can easily substitute into the ZnTe/CdTe lattice [76] but can lead to the formation of undesirable deep level impurities [77]. Group V elements are known to be slow diffusers [78] and are thus the most desirable for the controlled impurity p-type doping of ZnTe and CdTe. As yet a suitable, controllable p-type dopant for ZnTe

has not been found for MOVPE epitaxial growth.

One of the problems encountered in understanding the reproducible controlled doping of the wide band gap II-VI's is the need for low temperature, non equilibrium growth techniques. With the advent of growth methods such as MBE and MOVPE this problem of controlled doping may be overcome. Precursors play a key role in MOVPE and the properties that govern the choice of dopant precursors include safety and low growth temperatures. For safety reasons hydrides are not preferred, and for good crystallinity the growth temperatures should lie between 300 and 400°C. Doping studies for CdTe and ZnTe using metalorganic precursors are rare [67], due to the unavailability and cost of suitable precursors. Table 5.9 summarises the choice of metal organic precursors for p-type dopant purposes. It can be seen that both ammonia and elemental arsenic are fairly cheap and easy to incorporate.

The use of a nitrogen compound for the doping of ZnSe films grown by MOVPE using pure ammonia as the acceptor dopant source has been investigated [79]. Doping levels were controlled by the ammonia gas flow rate and the group II-VI ratio. Typical growth temperatures were approximately 350°C and photoluminescence studies of the layers formed confirmed the presence of nitrogen atoms. However film resistivities were high, approximately 10^3 Ωcm and this was explained by the formation of deep emission centres, resulting in considerable compensation. Among the group V elements nitrogen is expected to behave as a stable shallow acceptor with an ionisation energy of 100±15 meV [80]. MBE studies of N_2 plasma doping showed that growth temperatures of 400°C produced p-type ZnSe with resistivities as low as 3-7 Ω cm [81]. Initially nitrogen doping was considered a useful candidate for the p-type doping of ZnTe because both P and As were both found to form deep acceptor levels in ZnSe [82]. Stutius however showed that nitrogen could be incorporated as a shallow acceptor center in ZnSe by MOCVD [83].

This section examines the use of both arsenic and ammonia as dopant sources for the growth of both p-type ZnTe and CdTe.

	Name	Chemical formula	Bpt./°C	Vapour pressure	Toxicity	Supplier	Possibility as dopant
Nitrogen compounds	Ammonia	NH_3	-33.4 (gas)	7.5 bar at 20°C	-	BDH/BOC	Simple, decomposes at 132.4 °C.
	T-butylamine	$C_4H_9NH_2$	-	-	-	Epichem	Decomposition temperature too high (600 °C)
	Phenyl hydrazine	$C_6H_5NHNH_2$	-	10 torr at 115°C	Highly toxic	Epichem	Toxic
Phosphrous compounds	Trimethyl phosphorous	$(CH_3)_3P$	37.8	156 torr at 0°C	-	-	Needs low temperature bath
	Triethyl phosphorous	$(C_2H_5)_3P$	127	3.42 torr at 0°C	-	Cyanamid	Expensive
	Tertiary butyl phosphous	$(C_4H_9)_3P$	54	141 torr at 0°C	-	"	Needs low temperature bath
Arsenic compounds	Arsenic	As	-	10^{-2} mbar at 250 °C	-	BDH	Simple and cheap
	Ethyl arsenic	$C_2H_5AsH_2$	36	94 torr at -16°C	Toxic	Morton	Needs cooling
	Trimethyl arsine	$(CH_3)_3As$	51	97 torr at 0°C	Toxic	-	Needs cooling
	Tertiary butyl arsine	$(C_4H_9)_3As$	65	81 torr at 10°C	Toxic	Cyanamid	Needs cooling
Antimony compounds	Trimethyl antimony	$(CH_3)_3Sb$	80.6	30 torr at 0°C	-	Epichem	Needs cooling
	Triethyl antimony	$(C_2H_5)_3Sb$	160	107 torr at 75°C	-	Epichem	Expensive

Table 5.9 — Metalorganic precursors for p-type doping of CdTe/ZnTe

5.7.2 Doping of ZnTe using ammonia

Initial experiments concentrated on achieving high conducting p-type ZnTe using pure ammonia gas (5 nine purity) as the acceptor doping source. The ammonia gas was introduced into the reactor via a separate doping line, see figure 5.2 along with the hydrogen and metalorganic precursors. Ammonia is a thermally stable source and therefore high temperatures of 400°C were adopted in an attempt to crack the NH_3 molecule. PL measurements of ZnTe layers doped with ammonia confirmed that the incorporation of nitrogen can occur at temperatures as low as 250°C [81]. The important parameters in the growth of p-type ZnTe are temperature, II:VI ratio, NH_3:Te ratio, and the NH_3:H_2 ratio. Conflicting reports exist [79,81] as to the incorporation of N_2 under differing II:VI ratios, Ohki observing p-type behaviour with tellurium rich growth conditions and Taike reporting the reverse. Thus our experiments were conducted under both zinc rich and tellurium rich conditions. Taike also found that p-type conduction could only be found at NH_3:Se ratios greater than 100, whereas Ohki found that at below NH_3:Se ratios of 100 shallow nitrogen acceptor levels were formed, whereas at high NH_3:Se ratios deep emmision centres were formed. As a result Te:NH_3 ratios were varied from 1:14 to 1:200. Finally it was decided that since the large lattice mismatch at the ZnTe/GaAs interface creates a large number of misfit dislocations and trapping centres, buffered layers of ZnTe approximately 1μm thick would be grown on semi-insulating GaAs in order to relieve the stress caused by lattice mismatch onto which a doped ZnTe layer was grown.

All layers were found to be p-type as evidenced by the polarity of heated carriers between two probes but highly resistive (>$10^3\Omega$ cm). Layers were specular in appearance and retained their crystallinity as observed by RHEED. The resistivity of the ZnTe layers was too high however to be measured by the Van der Pauw method (see section 3.3.4).

5.7.3 Doping of ZnTe using elemental arsenic

Doping experiments were performed using elemental arsenic as a solid dopant source, heated to 250°C in a silica boat located just in front of the substrate holder,

see figure 5.3, following a procedure outlined by Kuhn et al [67]. The partial pressure of the arsenic above the substrate was calculated at this temperature to be 10^{-2} mbar. ZnTe layers were grown at 350°C for 1800 seconds with a total dilution flow of 7000 SCCM. The II:VI ratio was varied from 1:1 to 5:1, i.e layers were grown under stoichiometric or Zn-rich conditions, see table 5.10 below.

Sample	T_{growth} (°C)	T_{boat} (°C)	II:VI ratio	Growth time/s	ρ (Ωcm)
ZnTe/As1	350	250	1:1	1800	500
ZnTe/As2	350	250	2.3:1	1800	14
ZnTe/As6 (C)	350	250	5:1	1800	0.6
ZnTe/As6 (Au)	350	250	5:1	1800	0.2

Table 5.10 — The growth parameters for the As-doping of ZnTe

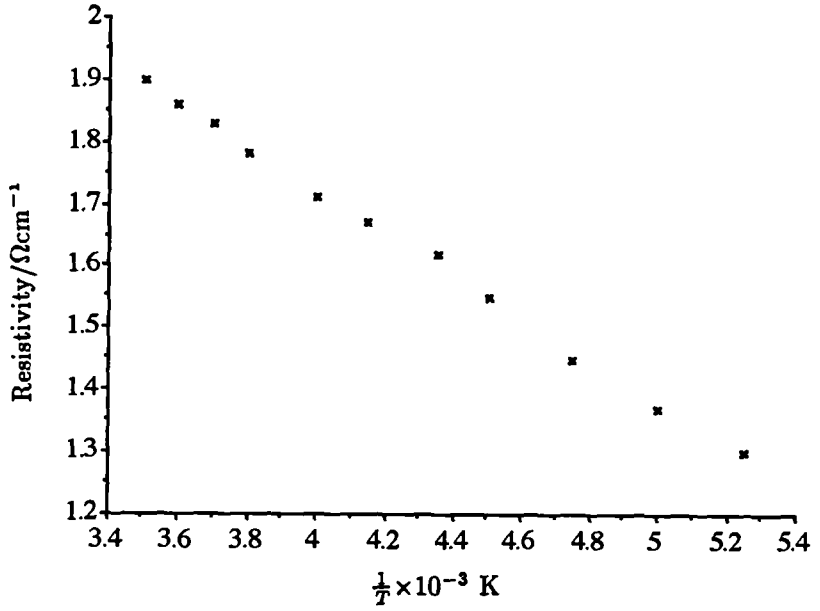

Figure 5.26 — Temperature-dependent carrier conductivity for p-ZnTe layers doped with arsenic

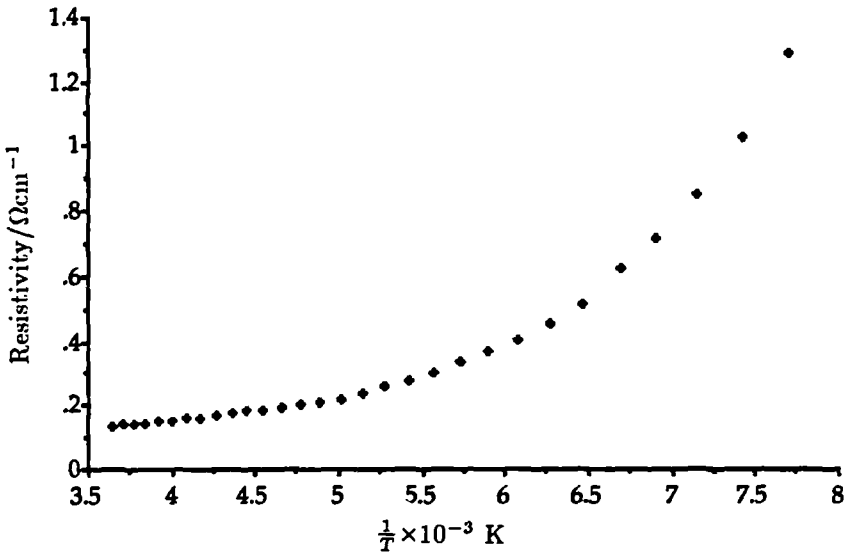

Figure 5.27 — Temperature-dependent carrier conductivity for p-CdTe layers doped with arsenic

Both carbon and gold contacts were made to the resulting epilayers. As the II:VI ratio was increased the layers of p-ZnTe became more conductive eventually giving layers of 0.2 Ωcm^{-1} conductivity. Hall effect measurements on this sample revealed a carrier concentration of 6.65×10^{17} cm^{-3} and a mobility of 52.2 $cm^2V^{-1}s^{-1}$, which compares favourably with that obtained by Aven and Prenner of 130 $cm^2V^{-1}s^{-1}$ [74]. RHEED measurements confirmed that the layers were still crystalline and their appearance was specular. Doping experiments were thus found to be reproducible and strongly dependent on the partial pressure ratios of the alkyls present. Using a similar process Kuhn et al [67] were able to achieve resistivities of 0.85 Ωcm^{-1}, carrier densities of 8.6×10^{17} cm^{-3} and mobilities of 8.5 $cm^2V^{-1}s^{-1}$ for layers of p-type ZnTe. The evaluation of temperature dependent carrier conductivity given in figure 5.26 revealed the presence of a level with an activation energy of 30 meV, which is smaller than the value of 76 meV [72] obtained by other authors for the arsenic doping of ZnTe.

5.7.4 The doping of CdTe using elemental arsenic

Following the successful growth of p-ZnTe layers using arsenic, layers of CdTe were fabricated in the same fashion. {100}GaAs substrates were polished and given a precautionary heat clean at 600°C for ten minutes. A Cd-rich environment was used with a growth temperature of 325°C. The Cd:Te ratio was kept at 3:1 and the arsenic boat temperature was 250°C. Again layers were grown with a total flow of 7000 SCCM and both gold and carbon contacts were made to the resulting epilayers. The growth conditions and conductivities of layers produced are shown in table 5.11.

Sample	T_{growth} (°C)	T_{growth} (°C)	II:VI ratio	Growth time/s	ρ (Ωcm)
CdTe/As4 (Au)	325	250	3:1	3600	35
CdTe/As5 (C)	325	250	3:1	3600	10
CdTe/As6 (Au)	325	250	3:1	3600	48

Table 5.11 — The growth parameters for the As-doping of CdTe

It was found that under Cd-rich conditions reproducible p-CdTe epilayers could be obtained using elemental arsenic. Hall effects measurements on samples revealed acceptor concentrations of 1.3×10^{16} cm^{-3} and mobility values of 48 $cm^2V^{-1}s^{-1}$. These values compare favourably to those found by other authors of 65 $cm^2V^{-1}s^{-1}$ [74]. A plot of $\ell n\rho$ versus $\frac{1}{T}$ shown in figure 5.27 revealed a straight line section from which a value of the activation energy of 63 meV was calculated for the acceptor. This compares favourably to those values shown in table 5.8.

5.7.5 Discussion

The use of elemental arsenic as a dopant has been successful in producing p-type layers of both ZnTe and CdTe. Resistivity and Hall effect measurements on these samples have found them to be suitable for the subsequent production of solar cell devices. Since the arsenic doped layers are highly conductive it can

be assumed that As substitutes for Te in the lattice. If the arsenic was associated with interstitial sites or on the Cd lattice it would be expected to form deep energy levels reducing the carrier concentration [84]. Photoluminescence studies on these arsenic doped samples would be able to confirm this since a peak at 1.511 eV, due to the arsenic acceptor on a tellurium site should be observed, but time did not permit.

5.8 The Growth of $Cd_{1-x}Zn_xTe$

5.8.1 Introduction

$Cd_{1-x}Zn_xTe$ (CZT) is a variable band gap (1.5-2.2 eV) II-VI compound semiconductor. By changing the value of x in the CZT ternary alloy the band gap and lattice parameter can be tuned for use in optical sources and detectors across the visible spectrum [85]. Bell and Sen have shown the ternary with x=0.04 can be used as a lattice matched substrate for the growth of $Cd_{1-x}Hg_xTe$ [86]. CZT alloys with band gaps in the region of 1.65-1.75 eV have been considered attractive for use in the top device in a high efficiency tandem solar cell structure [87]. Bulk lattice matched CZT has been used for some time as a substrate but epitaxial CZT is an attractive alternative for the development of CdTe/GaAs substrates currently in use [88]. It is also possible that CZT can be used as an inhomogeneous graded epitaxial absorber layer in the further development of the polycrystalline p-ZnTe/i-CdTe/n-CdS devices proposed by Meyers [89]. The growth of epitaxial structures on single crystal CdS having graded CdTe-ZnTe junctions will eliminate grain boundary recombination and, increase efficiency by making fuller use of the solar spectrum.

Initially CZT alloys of required composition were prepared by the growth of CdTe/ZnTe strained layer superlattices which were then interdiffused [62] as with the IMP (intermultilayer diffusion process) for $Cd_{1-x}Hg_xTe$ [94]. The advantage of this technique was that layers could be grown at a much reduced growth temperature, around 300°C using the same alkyls for direct alloy growth. However precise control of composition was difficult due to the complexity of the IMP process.

Other difficulties experienced with superlattice growth included the inhibition of the ZnTe growth due to the presence of Cd in the reactor. Flush times of around 15 seconds were required between successive superlattice layers in order to remove any residual Cd from the reactor. The CZT alloy has previously been grown by Ahlgren et al, using MOVPE on different orientations of GaAs [90]. The alkyls used were diethyl telluride and diethyl zinc with a growth temperature of 441°C. Growth at lower temperatures would however be advantageous since this would help reduce thermal strains and hence improve the structural quality of the material. This section reports on the epitaxial growth by MOVPE of CZT alloys of varying compostions on {100} GaAs substrates with a view to fabricating graded layers of CZT for p-i-n devices, described in chapter 8.

5.8.2 Growth conditions

Substrate temperatures of 325, 360, 380 and 400°C were investigated. A high total flow rate through the reactor of 7000 SCCM was used to prevent any pre-reaction of the diisopropyltelluride in the gas phase. Cd:Zn input molar ratios of between 1:1 to 1:30 were used in an attempt to control the Zn content of the layers. Grown layers were characterised by RHEED, SEM, XTEM and DCXRD to assess the structural quality and morphology of the layers. XRD measurements of lattice parameter were made with a Philips PW1130 diffractometer using Cobalt K_α radiation to determine the effects of alloy formation, and photoconductivity measurements were made to determine the band gap of the layers grown.

5.8.3 Results and discussion

At temperatures below 380°C no zinc was incorporated into the epilayers formed, as evidenced by EDAX. Single layers of CdTe were formed containing a large number of facets, see figure 5.28. RHEED analysis confirmed the presence of a {100} oriented layer with a small degree of polycrystallinity possibly resulting from surface contamination.

Epitaxial layers of CZT were grown at temperatures of 400°C , and they were

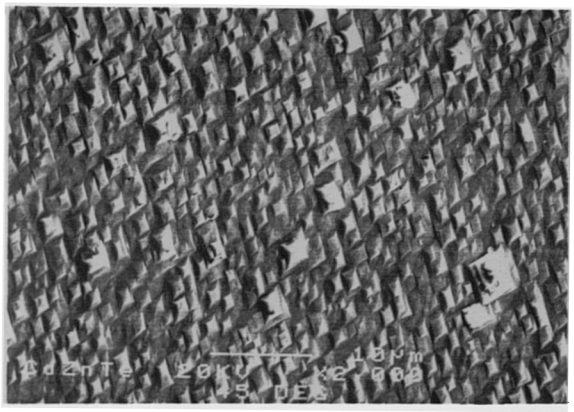

Figure 5.28 — An SEM micrograph of a CdTe epilayer grown at 380°C on {100}GaAs

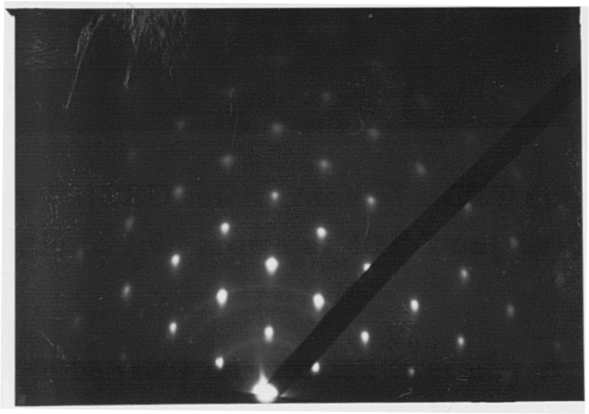

Figure 5.29 — A RHEED micrograph of a CZT epilayer, with a Cd:Zn ratio of 1:69 grown at 400°C on{100}GaAs

consistently found to be {100} oriented and to exhibit excellent crystallinity. A typical RHEED pattern of a layer where the Cd:Zn ratio in the epilayer is 1:69 is shown in figure 5.29. The electron beam lay along the <110> zone axis and when rotated by 90° gave an identical spot pattern confirming a (100) layer. The spot pattern is streaked perpendicular to the shadow edge a feature characteristic of a smooth surface. Table 5.12 summarises the growth conditions and features of CZT layers used in this study.

In all cases the II-VI ratio was kept constant at around 15, i.e operating in a tellurium limited regime. This limitation was imposed by the need to have a high partial pressure of zinc in order to get Zn incorporation into the lattice. The gas-solid distribution function is given in figure 5.30 as a function of the Cd mole

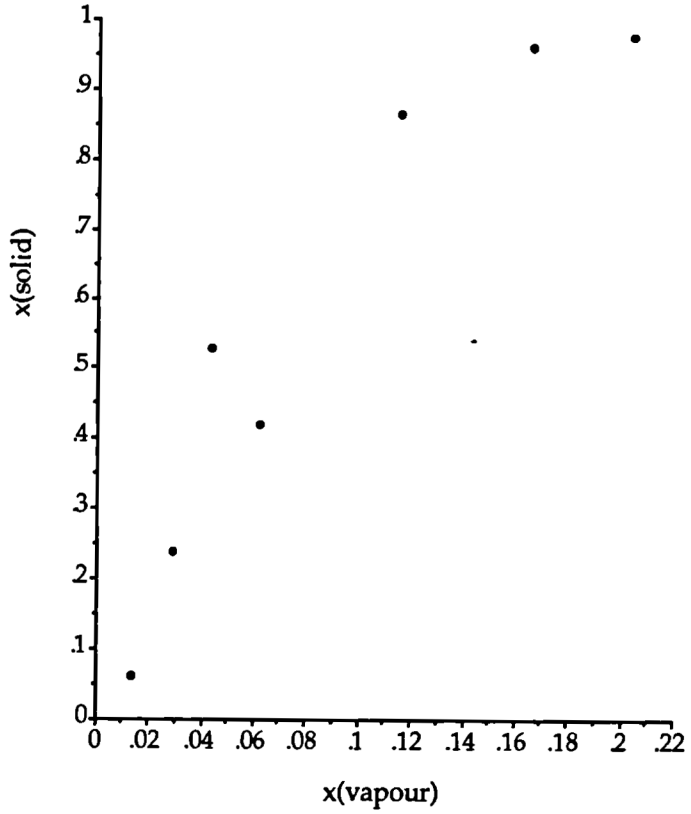

Figure 5.30 — The gas-solid distribution curve for the CZT alloy, where x is the Cd mole fraction

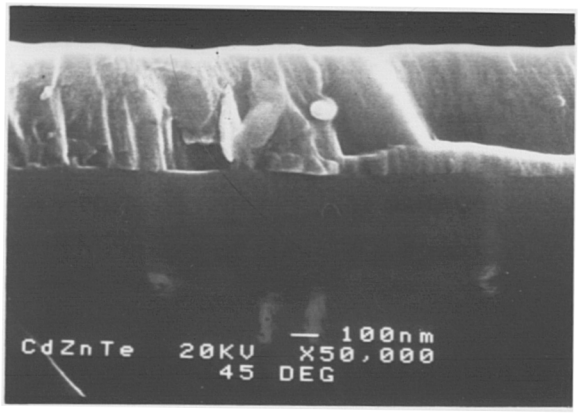

Figure 5.31 — A cross-sectional SEM micrograph illustrating the thickness of the CZT epilayer

fraction. The curve is bowed towards a larger Cd content in the solid phase. The degree of bowing is seen to be quite severe, and it is expected that this would reduce, if the tellurium mole fraction was made equal or greater than the Cd+Zn

Sample	Growth Temp.	Gas phase molar ratio Cd/Zn	Solid phase molar ratio Cd/Zn	Layer thickness	II/VI ratio	Lattice parameter	Growth rate	Band gap/eV
CdZnTe/4	400°C	0.015	0.061	0.9μm	17.5	6.123Å	5.0Ås^{-1}	2.181
CdZnTe/5	"	0.033	0.238	0.8μm	15.8	6.240Å	4.4Ås^{-1}	2.025
CdZnTe/6	"	0.051	0.532	0.6μm	16.0	6.313Å	3.3Ås^{-1}	1.745
CdZnTe/7	"	0.069	0.418	0.5μm	16.3	6.275Å	2.8Ås^{-1}	1.693
CdZnTe/9	"	0.142	0.804	0.9μm	17.3	6.405Å	5.0Ås^{-1}	1.500
CdZnTe/10	"	0.214	0.956	1.0μm	18.4	6.425Å	5.1Ås^{-1}	1.488
CdZnTe/11	"	0.287	0.974	0.7μm	19.4	6.475Å	3.9Ås^{-1}	1.511
CdZnTe/27	"	0.090	0.100	3.0μm	1.0	-	16.7Ås^{-1}	-

Table 5.12 — Growth conditions for the CZT epilayers of varying composition

mole fraction. It is interesting to note that Ahlgren et al [90] used theoretical computations to predict that the bowing observed in the gas-solid distribution curve would occur towards a higher zinc content in the solid phase. However, our experiments were conducted in a tellurium limited regime and it appears that Cd incorporation occurred at the suppression of Zn incorporation. Indeed previous experience suggests that ZnTe growth is inhibited in the presence of Cd, which will "mop up" the tellurium atoms. However to explain fully this discrepancy further experiments are needed to observe the effects of the II:VI ratio on the epilayers formed.

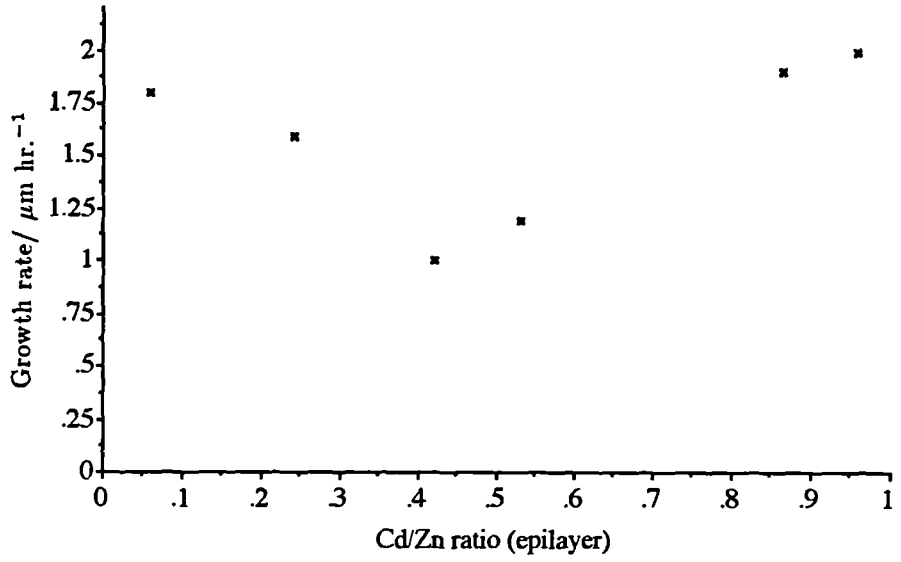

Figure 5.32 — Growth rate versus composition for the CZT epilayers

The growth rates of layers were determined from the value of the thicknesses obtained by cross-sectional SEM, see figure 5.31. The growth rate was seen to decrease to a minimum at a molar ratio in the solid of 0.5, see figure 5.32. Similarly the surface morphology of the binary materials was rough and facetted, becoming progressively smoother as the x=0.5 composition in the solid was approached. This is well illustrated by figures 5.33(a), (b) and (c) which correspond to layers having compositions of Cd of x=0.06, 0.24 and 0.5 respectively. The density and height of facets decreases as the x=0.5 composition is approached. It is interesting to note

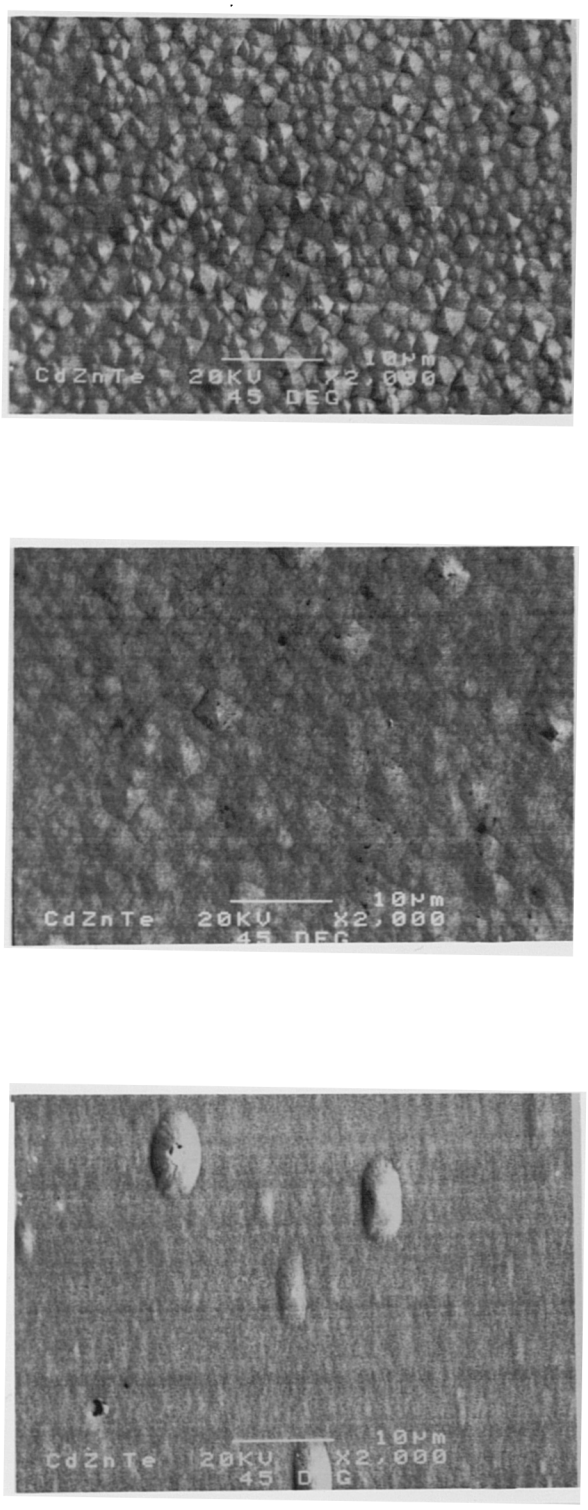

Figure 5.33 — SEM micrographs of CZT epilayers with (a) x=0.06, (b) x= 0.24, and (c) x=0.5, illustrating the change in surface morphology with composition

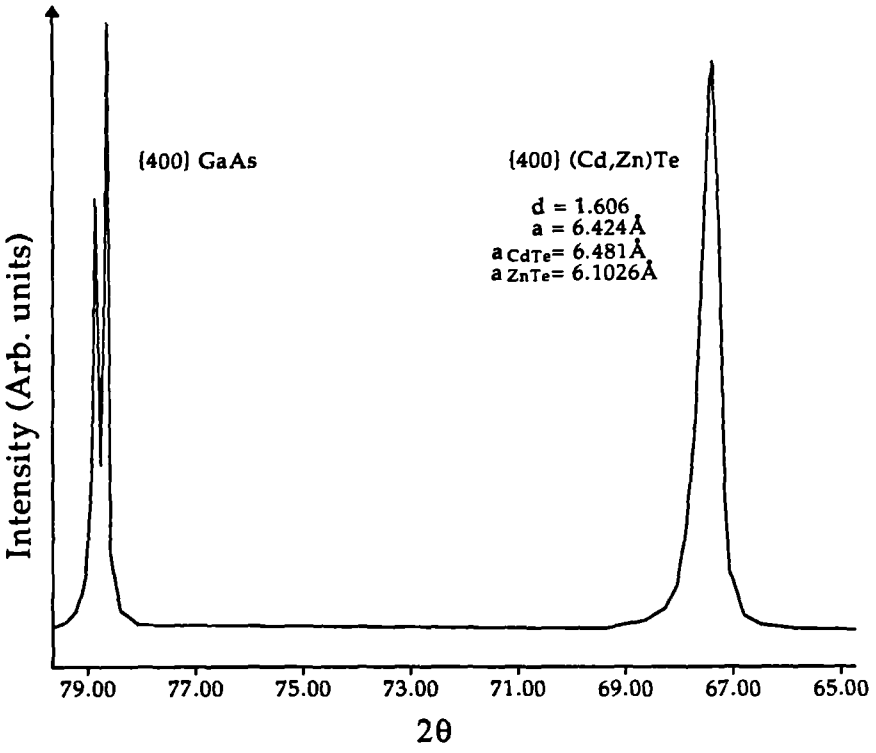

Figure 5.34 — X-ray diffraction data for a $Cd_{1-x}Zn_xTe$ epilayer where x=0.04

that better morphologies are attained at lower growth rates.

A typical plot of an XRD trace of the surface of one of the $Cd_{1-x}Zn_xTe$ epilayers where x=0.04 is shown in figure 5.34. It can be seen that there is a single discernible peak due to the {400} reflection of the CZT alloy. No other {400} reflections were observed, indicating the presence of a single phased alloy with no observable phase separation into the constituent binaries, as previously reported with the growth of CZT by MBE. In the MBE studies the layers grown underwent a phase separation, resulting in layers with very large rocking curve widths (>1700 arc s) [88].

From the trace in figure 5.34 it was possible to calculate the lattice parameter of the alloy to be 6.424 Å. If the variation of composition for the different epilayers varies linearly with lattice parameter the so-called Vegard's Law is obeyed. The variation in the lattice parameter with varying compostion of the CZT alloys is plotted in figure 5.34, where it is seen that the data does conform to Vegard's Law for a ternary alloy.

Figure 5.36 shows a typical example of a photoconductivity trace for a sample

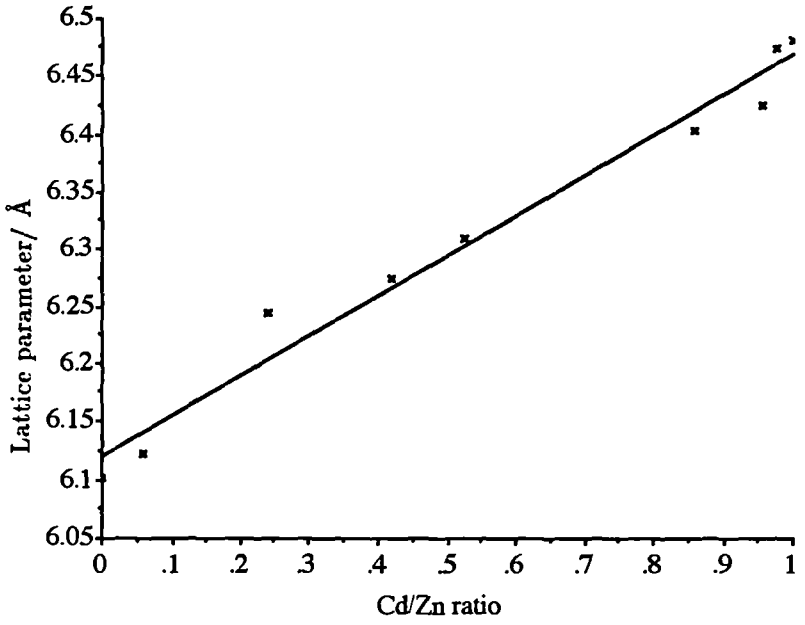

Figure 5.35 — The variation of the lattice parameter for CZT alloys with change in composition

where Cd/Zn=0.956. It can be seen that the band gap, taken as the threshold of the photocurrent, occurs at 1.475 eV, as would be expected for an alloy of this composition. Photoconductivity traces were recorded for all the alloys grown and the corresponding band gap versus Cd/Zn molar ratio in the epilayer is given in figure 5.37. The shape of the curve follows a quadratic equation, equation 5.2, previously predicted for ternary alloy semiconductors [91].

$$E_x = E_{g(ZnTe)} - [E_{g(ZnTe)} - (E_{g(CdTe)} - b)x - bx^2] \qquad [5.2]$$

where b is the bowing parameter, and x is the Zn molar fraction. From this equation the value of the bowing parameter, b, can be determined and was found to be 0.16. This compares favourably with the empirical value of 0.21.

XTEM micrographs from a sample of composition $Cd_{0.06}Zn_{0.94}Te$ revealed the presence of a dense tangle of dislocations about 0.2μm thick (see figure 5.38) above

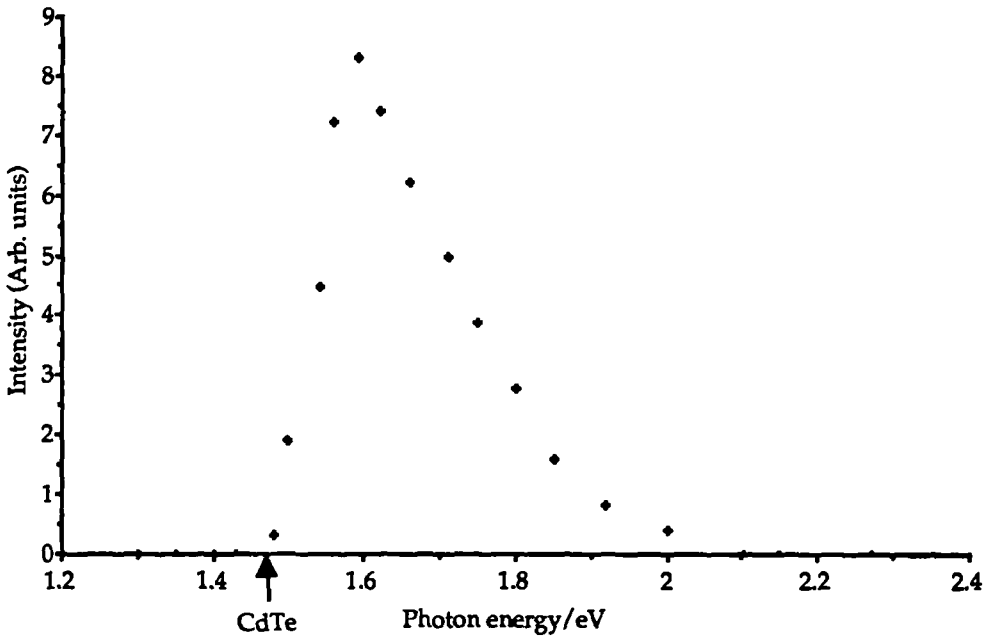

Figure 5.36 — A photoconductivity trace of a CZT alloy where the value of Cd/Zn=0.956

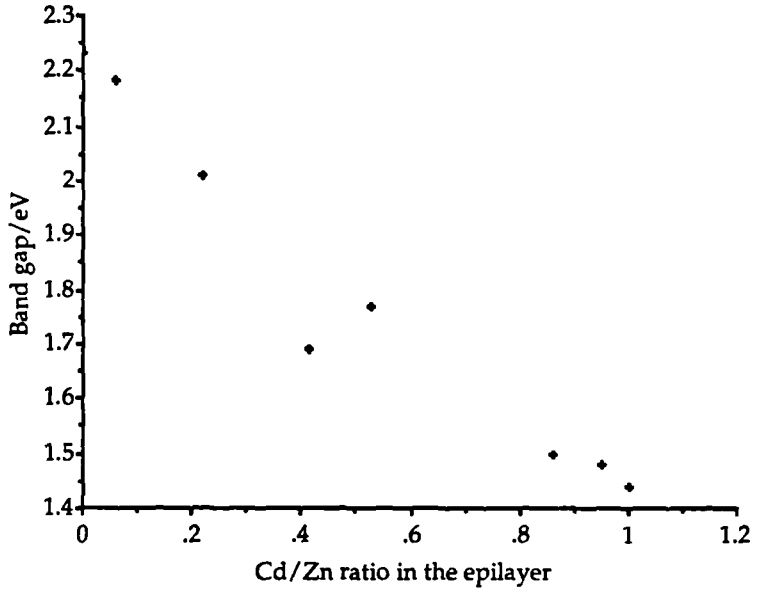

Figure 5.37 — The band gap versus Cd/Zn molar ratio for the CZT alloys of varying composition

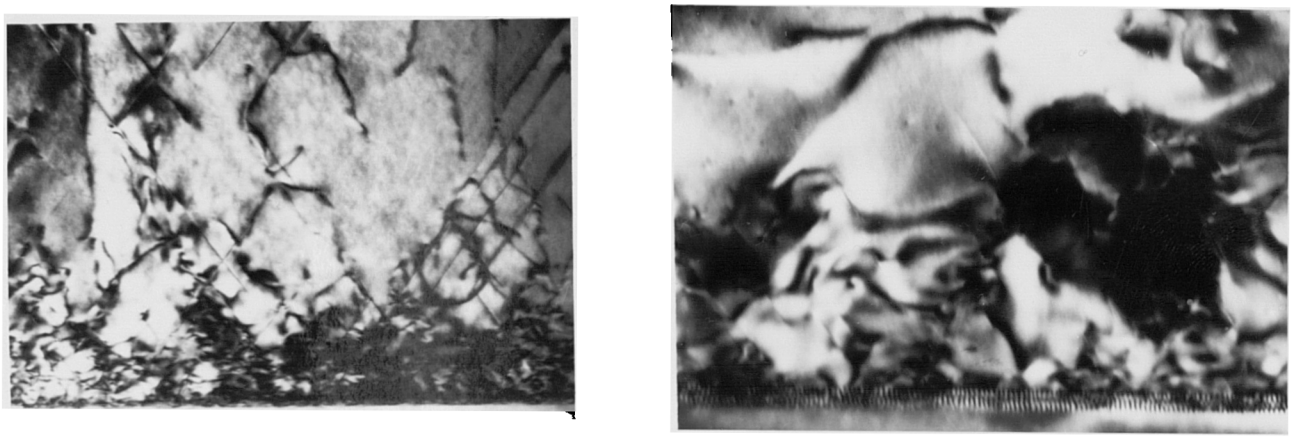

Figure 5.38 — An XTEM micrograph of a $Cd_{0.06}Zn_{0.94}Te$ epilayer illustrating the dense array of misfit dislocations at the interface

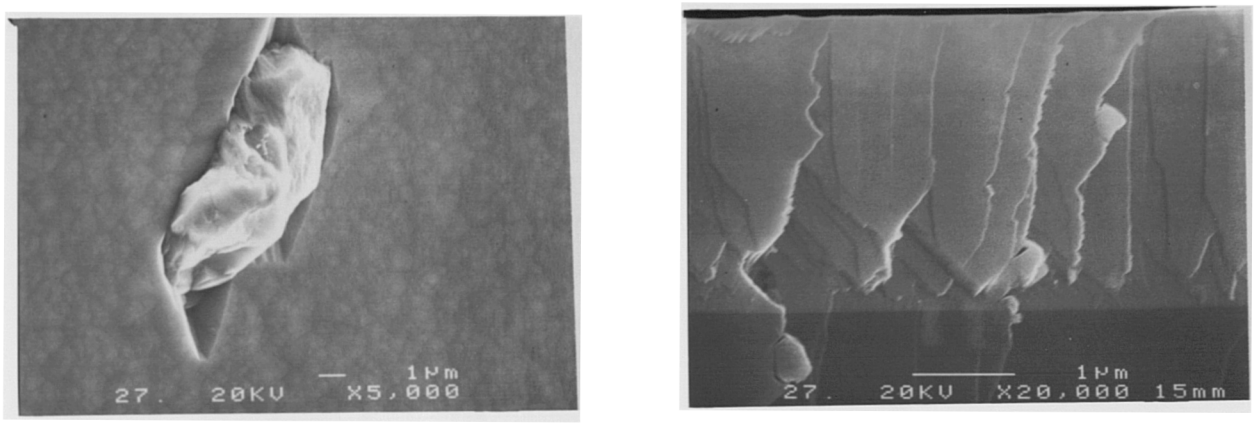

Figure 5.39 — (a) An SEM micrograph of a CZT epilayer where Cd/Zn=0.09 and (b) the corresponding XSEM micrograph illustrating the thickness of the layer

the interfacial array. A lower dislocation density of 10^{10} cm^{-2} was present at the surface. Similar dislocation densities have been observed in CdTe and ZnTe epilayers grown on {100} GaAs, see sections 5.4 and 5.6 and this is typical for systems with a large lattice mismatch. However, the surface dislocation density in the alloy is two orders of magnitude higher than seen in binaries of comparable thickness and is attributed to the relatively high growth temperature used in order to incorporate the zinc. No evidence of phase separation was found within this layer.

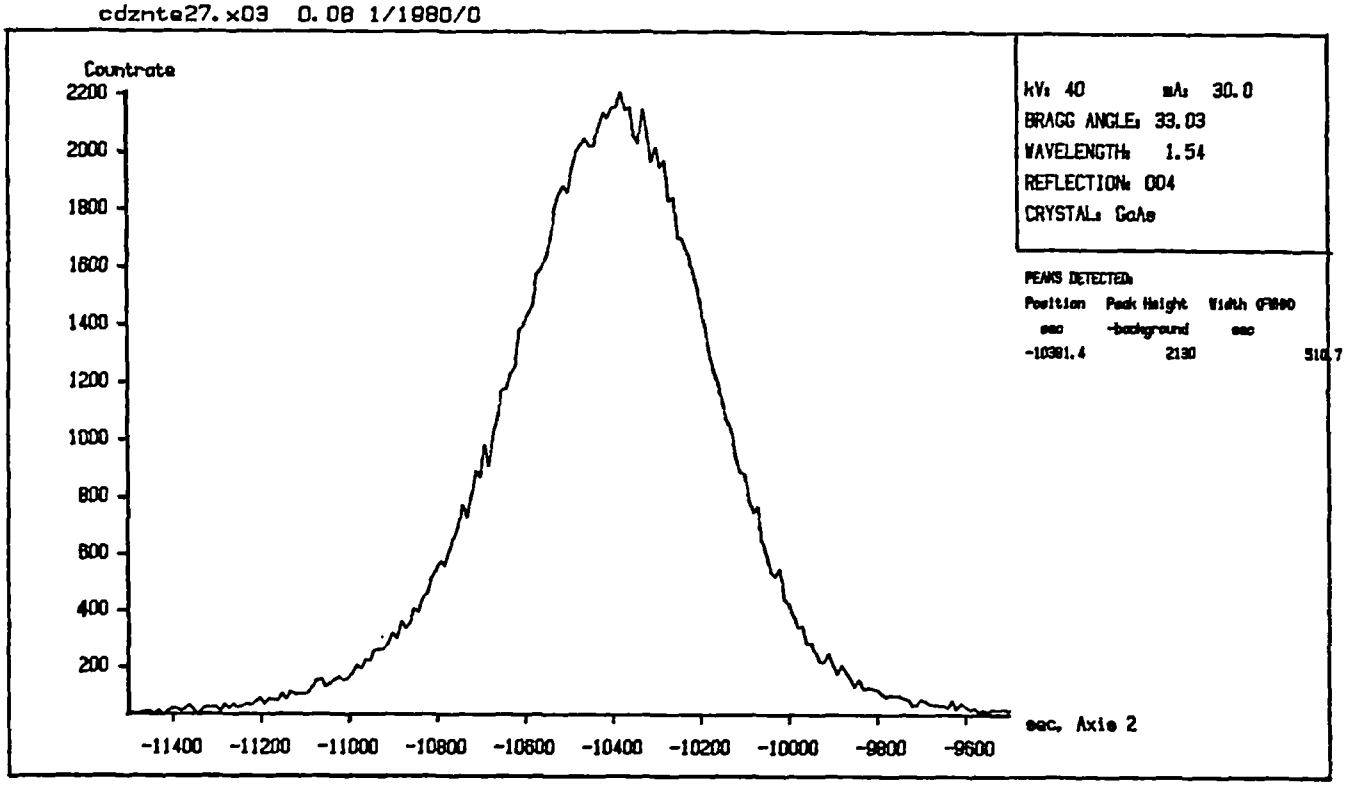

Figure 5.40 — A DCXRD trace of the CZT epilayer where Cd/Zn=0.09

Closer examination of the interface revealed an array of fringes of 33Å separation. Since this system is similar to ZnTe/GaAs in terms of lattice mismatch, this would indicate a higher proportion of inefficient 60° dislocations (approximately 70%) as opposed to 90° dislocations at the interface. This is indicative of a slightly rough GaAs surface used for growth, since 60° dislocations are more commonly associated with the substrate steps rather than pure edge dislocations [64].

Preliminary DCXRD measurements were made on an alloy where Cd/Zn=0.09. This layer was grown at 400°C with a II:VI ratio of 1:1. Figure 5.39(a) and (b) for this layer reveal the surface morphology as slightly ridged and with a thickness of $\approx 3\mu$m. The growth rate was seen to be much higher at this II:VI ratio i.e 17 Åsec^{-1} compared with 5 Åsec^{-1} for a II:VI ratio of 17:1. A possible explanation of this is that the excess Te present allows the Cd and the Zn atoms to compete for the Te atoms allowing both species i.e CdTe and ZnTe to grow. A DCXRD

trace (see figure 5.40) shows a FWHM of 511 arc sec. This value is much better than the values quoted by other authors for the CZT alloy of > 1700 arc secs [88]. Ahlgren et al [90] has found a FWHM of 83 arc sec for a very thick 15μm layer of composition $Cd_{0.96}Zn_{0.04}Te$ on GaAs/Si substrates. It is interesting to note that this value of FWHM is better than that for the corresponding binaries, again confirming the notion that the addition of Zn helps improve the CdTe layer quality, presumably as the presence of Zn slows down the CdTe growth rate by reducing the number of Te atoms available for growth.

5.8.4 Conclusions

Epitaxial layers of CZT of varying composition have been grown by MOVPE on {100} GaAs substrates at a temperature of 400°C with Zn to Cd molar ratios varying from 3 to 70. The band gap and lattice parameter have been shown to be tunable across the CdTe-ZnTe region and no phase separation has been observed in the layers grown, as confirmed by the presence of only single peaks for the alloys in the XRD data. All layers were shown to be {100} oriented and of good crystallinity. XTEM results also confirm the absence of phase separation which would be revealed by differently contrasted areas in the micrographs of the epitaxial layers. However XTEM results revealed the presence of a higher dislocation density at the interface of the GaAs substrate than experienced in binary growth. It is likely that better quality ternary layers would be obtained with a II:VI ratio of 1:1, as evidenced by the preliminary result of CZT/27. A reduction in growth rate at a molar ratio of 0.5 is accompanied by a reduction in surface roughness in the epilayer at this ratio. Further investigation is required into the effects of the II:VI ratio on the gas-solid distribution fuction. The growth of the CZT alloy of varying composition to grade the i-layer in p-i-n devices was performed and the preliminary results of this are presented in chapter 8.

5.9 Contacts to solar cell devices

5.9.1 Introduction

For all solar cell device structures high efficiency requires the formation of

stable, ohmic and low resistance contacts. An ohmic contact is one where the metal contact to the semiconductor surface has a linear I-V relationship in both directions. A good low resistance contact is one where the voltage dropped across the contact is negligible compared to that maintained across the device, i.e it does not affect the device characteristics. The choice of the metal contact to a semiconductor depends on its conductivity type and work function (see section 2.4.6).

For n-CdTe it is known that a thin oxide is present on the surface following a Br_2/MeOH etch [92] and that pinning of the Fermi energy by electron states at the CdTe surface gives rise to a surface depletion layer [93]. Thus a low resistance ohmic contact using a low work function group III metal such as indium is not expected to form initially, but with a subsequent heat treatment the enhanced inward diffusion of the evaporated metal would cause the surface region of the CdTe to become more strongly n-type than the bulk, resulting in an increase in probability of electrons tunneling as postulated by Kroger et al [94]. For n-CdS [95], n-CdTe [96] and n-GaAs [97] indium is well known to make a reproducible ohmic contact, if made onto clean surfaces.

The formation of stable ohmic contacts to p-ZnTe and p-CdTe has proved problematic due to the high electron affinity of these materials, 3.5 eV and 4.5 eV respectively. Generally for p-type material an ohmic contact is formed when the metallic work function is higher than the semiconductor electron affinity. Gold with a work function of 4.89 eV was initially considered the most likely metallic contact [98]. One method of overcoming this problem was to create a highly doped p-region when the metal is diffused into the semiconductor [99]. Aven et al [100] considered depositing a thin surface layer with acceptor impurities which are then diffused in by a heat treatment of the crystal at 350-800°C. However uncontrollable deviations in the basic bulk characteristics of the ZnTe were found using such heat treatments [101]. Thus a low temperature method of contact formation is required, and C-paste contacts seem to be the best alternative [102]. Here a carbon paste, as recommended by Awan et al, is painted onto the sample and given a low temperature anneal (250°C) to form a stable ohmic contact.

5.9.2 Experimental

In this study both gold and carbon paste contacts were made to the p-CdTe and p-ZnTe, whilst indium was used to make the ohmic contacts to the n- type substrate.

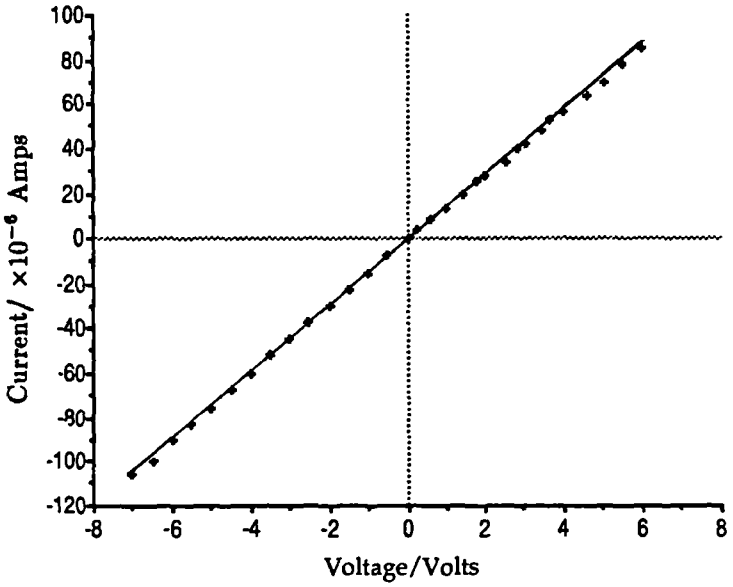

Figure 5.41 — I-V characteristic for a carbon paste contact on p-CdTe

After the growth of the p-type epilayer ohmic contacts were made to this freshly grown surface since, at this stage, it is relatively free from contaminants. Either gold contacts were evaporated onto the sample under high vacuum and then annealed in nitrogen for 1 minute at 500°C or carbon paste contacts were painted onto the surface and annealed in nitrogen for 20 minutes at 250°C. Samples were then coated in lacomit varnish and etched in a solution of the substrate polish solution, see chapter 4. Following this surfaces were rinsed and dried under IPA before ohmic contacts were made to the freshly etched n-type substrates.

5.9.3 Results

Thus for both p-ZnTe and p-CdTe carbon paste contacts were used to determine room temperature solar efficiencies although freeze out occurs at tempera-

tures below 250 K. Annealed gold contacts were used for detailed I-V and C-V characteristics at low temperatures.

In order to test the formation of ohmic contacts, I-V plots were made in both directions and a typical representation for the p-type CdTe with carbon paste contacts is shown in figure 5.41. The contacts were verified to be ohmic from the symmetric straight line I-V characteristic passing through the origin, giving a resistance of $1.4 \times 10^5 \Omega$.

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Chapter VI

The n-CdS/p-CdTe Solar Cell Grown by MOVPE

6.1 Introduction

Amongst the likely candidates for the photovoltaic conversion of solar energy the n-CdS/p-CdTe has been one of the most widely studied heterojunctions, with a high theoretical predicted conversion efficiency of 25% [1]. A band structure diagram of the n-CdS/p-CdTe cell at zero bias is given in figure 6.1. The Fermi energies coincide at the junction and it can be seen that there are no conduction or valence band spikes. Numerical values presented in the diagram are calculated for a typical cell. The values of ΔE_c and ΔE_v were calculated from equations 2.10 and 2.11 (see chapter 2), whilst δ_n and δ_p were calculated in appendix A. In section 6.4 the width of the space-charge region was found from C-V measurements to be 0.8μm wide. The carrier transport properties of the n-CdS/p-CdTe heterojunction are known to be dominated by phenomena at the interface region. The current-transport in the depletion layer is attributed to combinations of tunneling and recombination involving energy levels within the interface which are represented by a "ladder" of states in figure 6.1.

In an *ideal* substrate/epilayer relationship it is usual to expect the crystal structures to be compatible and the lattice parameters to be the same. For this reason the CdS/CdTe system has not been considered viable, CdS having the wurzite lattice and CdTe, the sphalerite. Furthermore the equivalent close-packed planes in these structures, the {0001} and {111} planes respectively have interatomic spacings differing by 9.7% [2]. Such a large mismatch invariably leads to extensive strains at the interface, which are relieved by dislocations and other defects [3]. Nevertheless good quality epitaxial layers of CdTe have been grown by MOVPE on GaAs, where the mismatch is even higher (14.7%) [4]. Indeed the epitaxial growth of CdS onto single crystal {111} CdTe by vacuum evaporation, and MOVPE has

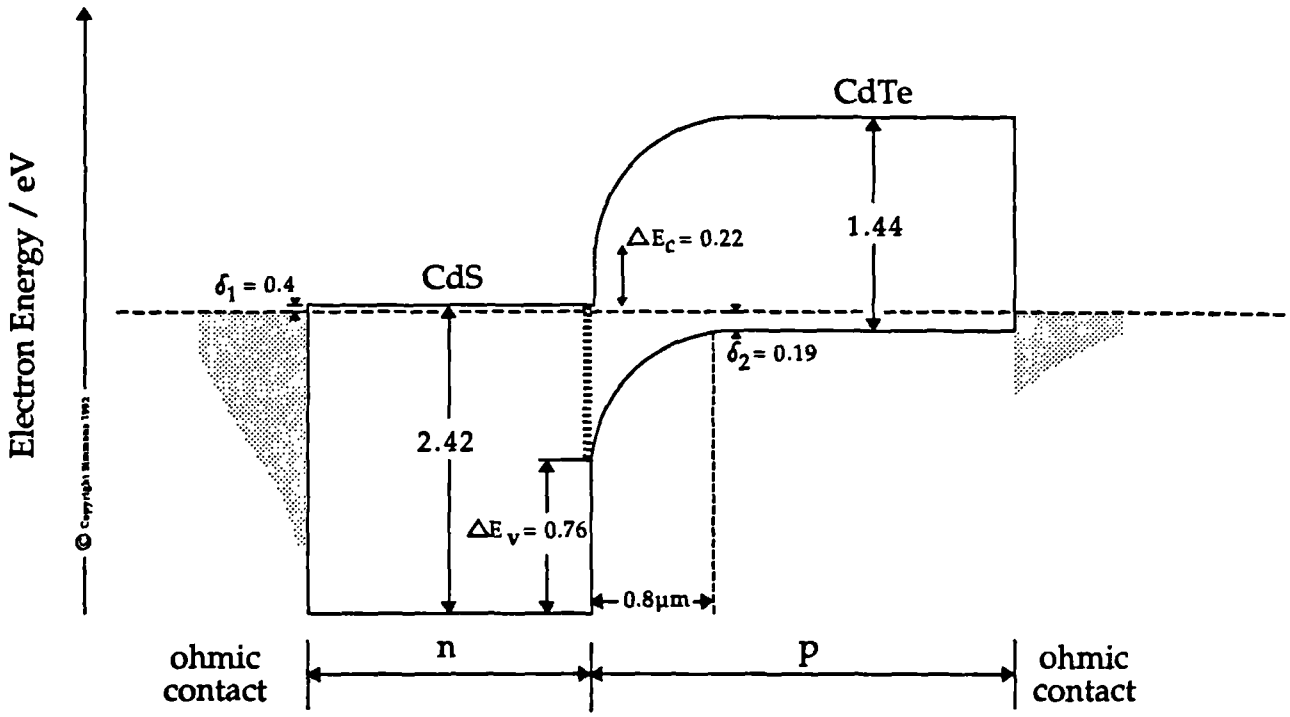

Figure 6.1 — The band structure diagram of the n-CdS/p-CdTe heterojunction

already been demonstrated [5,6,7]. However subsequent solar cell devices offered low efficiencies due to the high resistivities of the thick p-CdTe substrates. Nevertheless Yamaguchi et al [7] were able to produce a cell with a 10.5% efficiency. The inverse relationship (i.e. the growth of CdTe onto CdS) could lead to more highly conducting p-type CdTe by doping the CdTe layer during growth, thus reducing some of the contact difficulties experienced with this particular solar cell.

The work in this chapter includes a brief description of the fabrication of n-CdS/p-CdTe solar cells, using MOVPE to grow epitaxial layers of CdTe on the opposite polar faces of {0001}CdS single crystal substrates. The electrical properties of the cells are then described in detail including light and dark I-V measurements leading to current transport observations, spectral response, C-V and photocapacitance studies. The degree to which the polarity influences the device parameters of n-CdS/p-CdTe cells produced on polar {0001} CdS substrates is then discussed. The electrical properties of both types of devices are then correlated with the measured structural properties (previously described in section 5.5.2) giving an insight into the current transport mechanisms occuring within the cells.

6.2 Diode Characteristics

Oriented {0001} CdS substrates, approximately 1 mm thick, obtained from Eagle-Picher laboratories were etched in a CrO_3 acid etchant (as described in section 4.4.2) and rinsed in deionised water for 1 hour to obtain a damage free, mirror-like surface for epitaxy. The substrates were then loaded into the MOVPE reactor and given a precautionary heat clean at 400°C for 10 minutes to reduce the oxide on the surface. An epitaxial layer of CdTe doped with arsenic (see section 5.7.4), approximately 1-1.5 μm thick was then grown onto the CdS substrate. Immediately after cooling, the substrates were removed from the reactor and a semi-transparent dot of gold, 1 mm^2 in diameter, was evaporated onto the surface of the CdTe. The surface was then masked using lacomit varnish and the unwanted CdTe deposition around the edges and on the back of the device was etched off with a 1% Br_2/MeOH etch. Finally indium was evaporated onto the freshly etched CdS surface, again using a dot configuration. For comparison purposes each CdTe deposition was carried out simultaneously on both (0001)A and (000$\bar{1}$)B oriented CdS substrates.

6.2.1 Diodes prepared on the (0001)A face of CdS

Typical diode characteristics of a cell prepared on the Cd-face, under AM1.5 illumination are given in figure 6.2. For this particular device the V_{oc}, I_{sc} and ff were 0.42 V, 121 mA and 38.0% respectively. Both the values of the fill factor and open circuit voltage were disappointingly low compared to values of 60% and 0.7 V for polycrystalline cells (see section 2.3.2). The efficiency measurement is not absolute because of the contact geometry used. If the device area was taken as the junction area $\approx$0.9cm^2 (as is often done) the value of J_{sc} was calculated to be $\approx$149 $mAcm^{-2}$, which is unrealistically high. Using this value of J_{sc}, the calculated efficiency was 27.3%. In 1974 Fahrenbruch et al [8] predicted a maximum theoretical value of J_{sc} to be 19.8 $mAcm^{-2}$, assuming a solar input of 0.087 Wcm^{-2} for this cell. The highest published value of the short circuit current density is 28.20 $mAcm^{-2}$ by Ikegami et al [9]. It is the calculation of the actual active device area that causes this discrepancy, the contact area (7.85×10^{-3} cm^{-2}) apparently

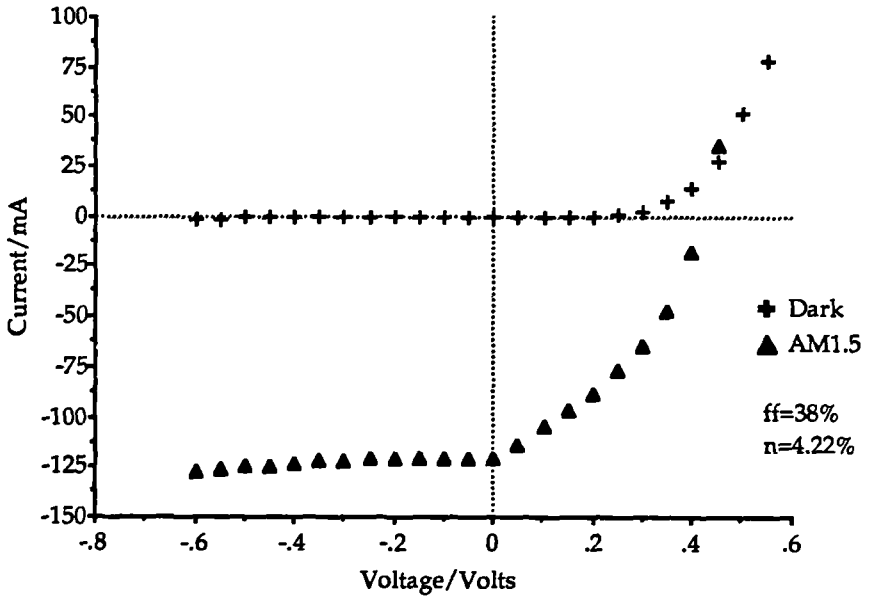

Figure 6.2 — Solar output characteristics of a n-CdS/p-CdTe solar cell grown on the Cd face of basal CdS under AM1.5 illumination

being a lot smaller than the effective junction area (0.81 cm^{-2}). Although the inaccuracies in the current density measurements are large, giving a value of J_{sc} five times greater than previously reported [5,7], it nevertheless seems that the current values measured are in reality large. Ikegami's cell [9] gave a short circuit current of 21.8 mA, whereas the cell described above gave the value of 121 mA. At the time of publishing their results Ikegami et al were concerned as to their value of the current density, being $\approx$8 $mAcm^{-2}$ higher than that predicted by Farenbruch et al [8]. The reason postulated for the difference being the formation of a CdS_xTe_{1-x} mixed crystal phase at the CdS/CdTe interface, causing a widening of the band gap in the absorber layer. This would lead to a increase in carrier density and thus the higher value of J_{sc}.

Since the values of J_{sc} reported here are anomalously high the magnitude was recalculated from the spectral response data (see figure 6.16). The short circuit current is defined by the relation of the light generated current density to the shunt and series resistance. For high quality cells with high shunt and low series resistance, the value of the the short circuit current is the same as the light generated current density. It is possible therefore to calculate the upper limit of the short circuit current obtainable from any selected solar cell material. Under ideal conditions each incident photon that has an energy greater than the bandgap gives

rise to one electron flowing in the external circuit. Thus using the solar spectrum, the maximum I_{sc} can be calculated. The light generated current is the integrated product of the photon current times the quantum efficiency. Figure 6.3 shows the theoretical photon current generated as a function of band gap energy for AM1.5 illumination [10]. From these values, assuming that the cell is behaving ideally the true values of the short circuit current density were extrapolated from spectral response data (presented in section 6.5). A more realistic value of the short circuit current density (23.0 $mAcm^{-2}$) was obtained. Using this value of I_{sc} the efficiency of the cell was found to be 4.22%, i.e a factor of six times lower. This confirms that the contact area was indeed much smaller than the actual junction area.

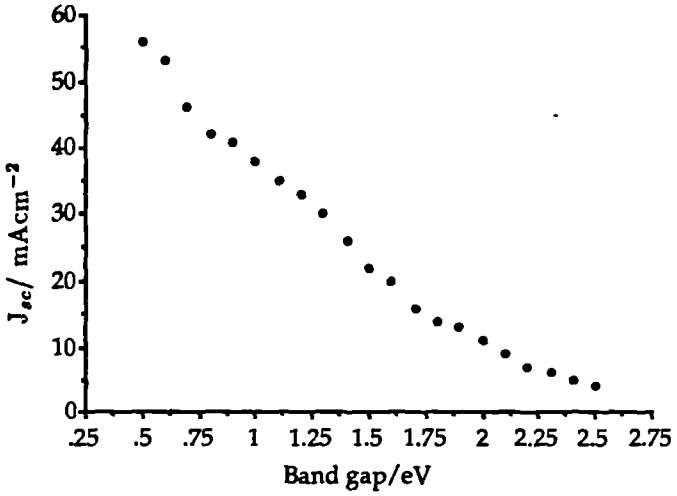

Figure 6.3 — Theoretical photon currents generated as a function of band gap energy for AM1.5 illumination [10]

6.2.2 Diodes prepared on the $(000\bar{1})$B face of CdS

The diode characteristics of a cell prepared on the sulphur face of {0001}CdS is given in figure 6.4. The shape of the curve is far from ideal, giving a very low fill factor of ≈16%. The open circuit voltage 0.52, is higher than that observed for the Cd face device, whilst the current 42.1 mA, is much lower. Again the contact area of the junction was much smaller than the effective junction area (0.81 cm^{-2}) and

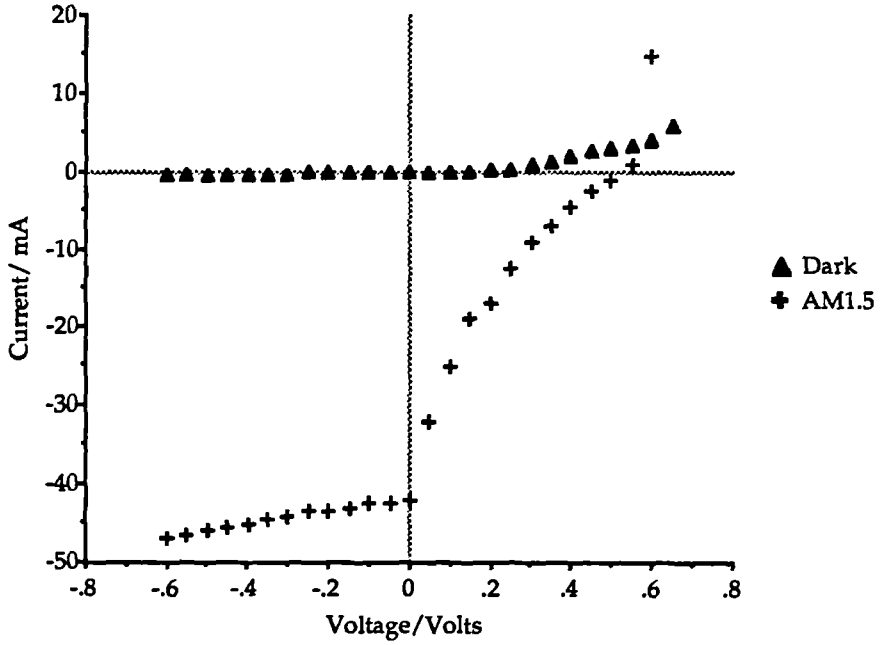

Figure 6.4 — Solar output characteristics of a n-CdS/p-CdTe solar cell grown on the S face of basal CdS under AM1.5 illumination

it is suspected that J_{sc} values of 53.48 $mAcm^{-2}$, giving nominal device efficiencies of 4.94%, were unreliable. Using spectral response data from section 6.5 a more realistic value of J_{sc} was calculated to be 15.60 $mAcm^{-2}$. The cell efficiency was recalculated to be 1.49%, using this corrected value of J_{sc}.

In both cells a cross-over of the dark and illuminated characteristics in the first quadrant was observed. The same cross over has been observed in Cu_2S/CdS [11] and CdS/CdTe cells [12,13], but not in silicon devices. The crossing of the light and dark I-V curves occurs because illumination shrinks the depletion layer due to the excitation of carriers across the direct band gap of CdTe, thus allowing an increased tunneling current to flow. Such effects are not observed for Si devices probably due to the nature of the indirect band gap where excitation requires a change in momentum as well.

6.3 Current transport mechanisms

Current-voltage characteristics of the n-CdS/p-CdTe heterojunction have been studied in an attempt to establish the dark conduction mechanisms in these devices. Measurements were carried out over the temperature range 70-350 K.

6.3.1 Diodes prepared on the (0001)A face of basal CdS

Figure 6.5 shows a semilogarithmic plot of the forward I_f-V characteristics in the dark for a polycrystalline CdS/CdTe diode grown on the Cd face of basal CdS. The forward bias current varies exponentially with voltage for several orders of magnitude of the current. The deviation from exponential behaviour at higher current levels (above 0.5 V) was due to the high series resistance of the bulk CdS. This effect became more pronounced as the temperature was lowered, since the resistivity of the CdS increases with decreasing temperature. Thus at temperatures below 250 K the characteristics became dominated by the series resistance of the CdS.

The slopes of the $\ell n(I_f)$-V characteristics in the regime where the series resistance was not dominant (10^{-8}-10^{-6} A) were found to be constant with temperature above 250 K indicating a temperature insensitive current-transport mechanism. Consequently, the $\ell n(I_f)$-V characteristics are not well described by the usual diode relation

$$I_f = I_o \left[exp\left\{ \frac{q(V - IR_s)}{nkT} \right\} - 1 \right] + \frac{V - IR_s}{R_{sh}} \qquad [6.1]$$

where R_s and R_{sh} are the series and shunt resistances respectively, since this would predict slopes in the $\ell n(I_f)$-V curves that varied with temperature.

Analysis of the data was carried out in the low voltage region of the characteristics where resistance effects could be neglected. Table 6.1 shows the values of A (see equation 6.4 below), I_o and n obtained by fitting the standard diode equation

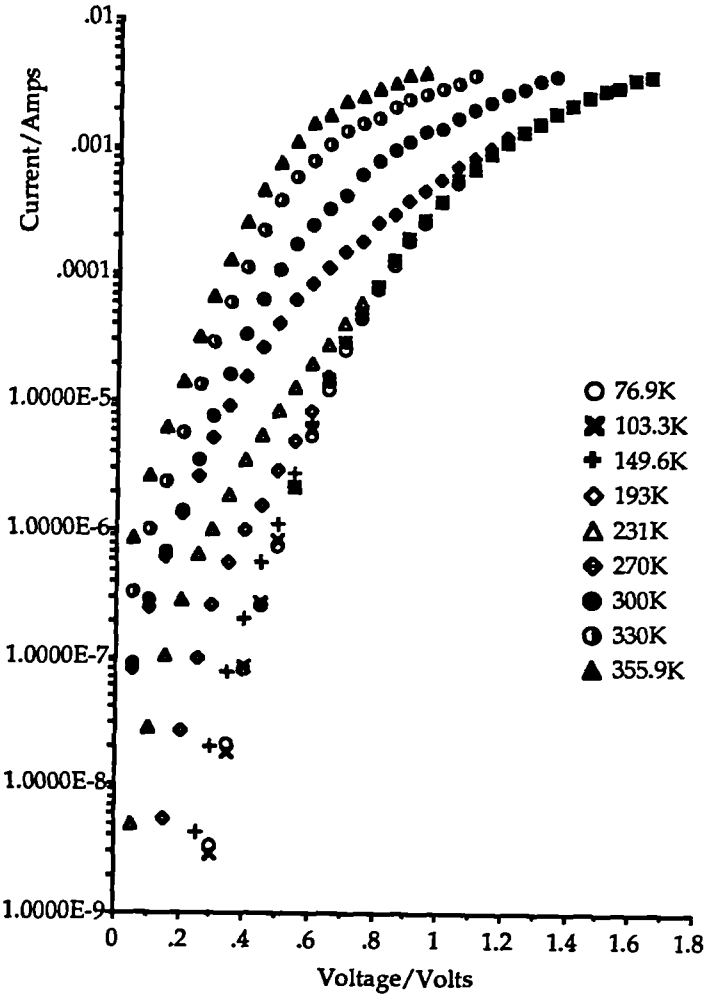

Figure 6.5 — Dark I_f-V characteristics of a n-CdS/p-CdTe diode grown on the Cd face of basal CdS at temperatures between 70-350 K

at different temperatures. It is observed that the diode factors n, required to fit the I_f-V data from equation 6.1 are close to or larger than 2 for the entire temperature range tested. Also there is a 65% change in n on going from 193-360 K. Diode factors of 2 or greater are indicative of recombination within the junction region since an ideal diffusion current mechanism would exhibit n=1. Thus both the magnitude of n and the fact that it is temperature dependent indicates that it is not a diffusion process that is occurring. The absence of any thermal activation in the $\ell n(I_f)$-V behaviour was confirmed by the failure of $\ell n(I_f)$ vs. $\frac{1}{T}$ plots to

display any straight lines.

Instead the forward I_f-V characteristics are reasonably well described by the tunneling expression given below

$$I_f = I_{oo}(T)\, exp\,(\,BT\,)\, exp\,(\,AV\,) \qquad [6.2]$$

where A is the tunneling constant and B gives the temperature dependence of the saturation current I_o. The temperature and voltage dependence of I_f are shown to be separable by the straight line relationship in the plot of $\ell n\ I_o$ with temperature, see figure 6.6. $I_o(T)$ can be determined by the extrapolated intercept and bears an exponential dependence on the built-in potential of the junction through

$$I_o\,(T) = I_t\, exp\,(-AV_d\,(T)) \qquad [6.3]$$

where I_t is a constant proportional to the density of traps of appropriate energy in the CdTe depletion region [14].

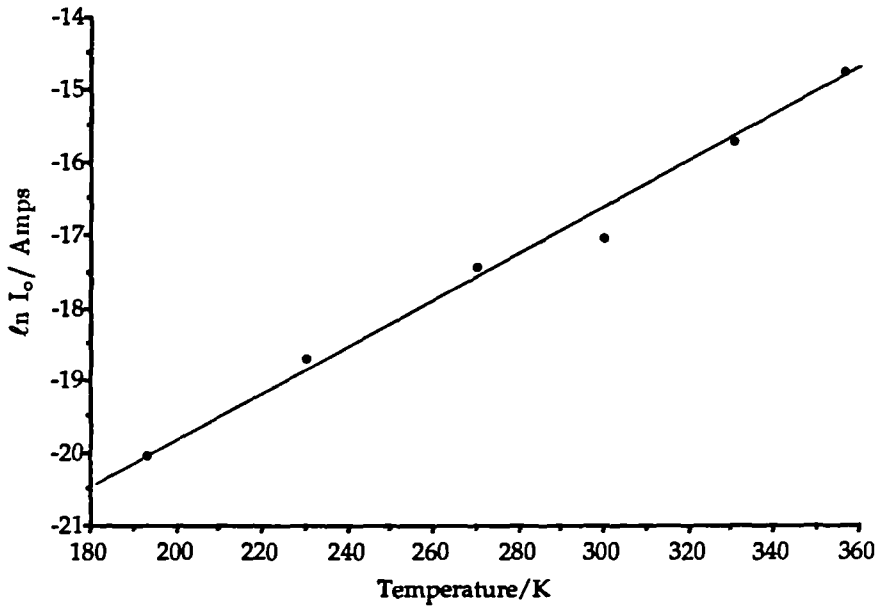

Figure 6.6 — A graph of $\ell n\ I_o$ versus temperature

Assuming a tunneling model, the values of A can be determined from the slopes of the ℓn (I_f)-V curves and are described by the following equation [14].

$$A = \frac{d\ell n\ I_f}{dV} = \frac{4}{3h}\left(\frac{m^*\ \epsilon_p\ S}{N_A}\right)^{\frac{1}{2}} \qquad [6.4]$$

where N_A is the acceptor density of the CdTe, ϵ_p is the dielectric constant of the CdTe and S is the fractional energy change at each step in the tunneling process. From table 6.1 it can be seen that the values of A are insensitive to temperature change, within experimental error, giving an average value of 17.8 V^{-1}.

Temperature/K	I_o/A	A/V^{-1}	n
193	2.7×10^{-9}	16.3	5.2
231	1.0×10^{-8}	18.7	3.0
270	3.0×10^{-8}	19.4	2.3
300	5.0×10^{-8}	17.1	2.3
330	1.6×10^{-8}	17.5	2.0
356	4.0×10^{-8}	17.8	1.8

Table 6.1 — Dark I_f-V characteristics for a diode grown on the Cd face

S.S. Ou et al [15] have shown that in order for band to band transitions to occur within this system a carrier concentration of 10^{18}-10^{19} cm^{-3} would be necessary. A room temperature value of N_A=1.3×10^{16} cm^{-3} was calculated from Hall measurements on the MOVPE grown p-type CdTe layers (see section 5.7.4). According to the criteria of S.S. Ou et al this value is two orders of magnitude below that required for simple tunneling, but perhaps multi-step tunneling could be possible. In this model proposed by Riben and Feucht [14], see section 2.4.3, the electrons are expected to tunnel stepwise from the conduction band of the CdS into empty interband states located in the CdTe and subsequently recombine through a staircase of closely spaced states in the depletion region. Franz [16] proposed that the forward current density, J_f, in the multistep tunneling/recombination model could be expressed by

$$J_f = \tau \psi N_t exp(-\alpha R^{-\frac{1}{2}}(V_d - KV)) \quad [6.5]$$

where τ is a constant, $\alpha = \left(\frac{\pi}{4h}\right)\left(\frac{m_n^* \epsilon_p}{N_A}\right)^{\frac{1}{2}}$, N_t is the density of tunneling/ recombination centers, ψ is the transmission coefficient for the electrons to cross the interface per unit time, $K = [1 + \left(\frac{\epsilon_p N_A}{\epsilon_n N_D}\right)]$, m_n^* is the electron effective mass, ϵ_p and ϵ_n are the dielectric constants of the CdTe and CdS respectively, N_A and N_D are the net ionised charge density on each side and R is the number of steps required to traverse the depletion region.

This equation is equivalent to equation 6.2 which considers the temperature dependence introduced by the change of V_d with temperature (see appendix B). For forward bias a value of 0.031 K^{-1} was obtained for the empirical coefficient, B, using figure 6.6. This is in reasonable agreement with values obtained by S.S. Ou et al [15] of 0.07 K^{-1} on a electrochemically deposited CdS/CdTe polycrystalline junction. The number of tunneling steps could be determined from combining like terms from equation 6.2 and from equation 6.6, giving

$$R = \left(\frac{K\alpha}{A}\right)^2 \quad [6.6]$$

Assuming $\epsilon = 9.6\epsilon_o$, and $m^* = 0.1m_e$ [15], the number of steps was calculated to be 104. This value is in reasonable agreement with values of 40-100 steps published by other authors [15,17,18] on the same heterojunction, although it is a little on the high side. The fractional energy change, S, can be calculated from equation 6.4 and was found to be 3.3×10^{-3} eV, for this junction. Thus the total barrier height to electron flow across the junction was 0.34 eV.

From equations 6.2 and 6.3 it follows that the only way the temperature dependence can enter the I_f relationship is through the term $I_o(T)$ i.e. through I_t or V_d. Since for $I_f \geq 10^{-6}$ A, $\ell n\ I_o$ varies linearly with T rather than T^{-1}, it can be concluded that it is the built-in potential that is temperature dependent. Whilst Donnelly and Milnes [19] investigated the effects of interface states on the transport mechanism, their results did not however, explain the effects of these interface states on V_d in terms of temperature. However it is well known that

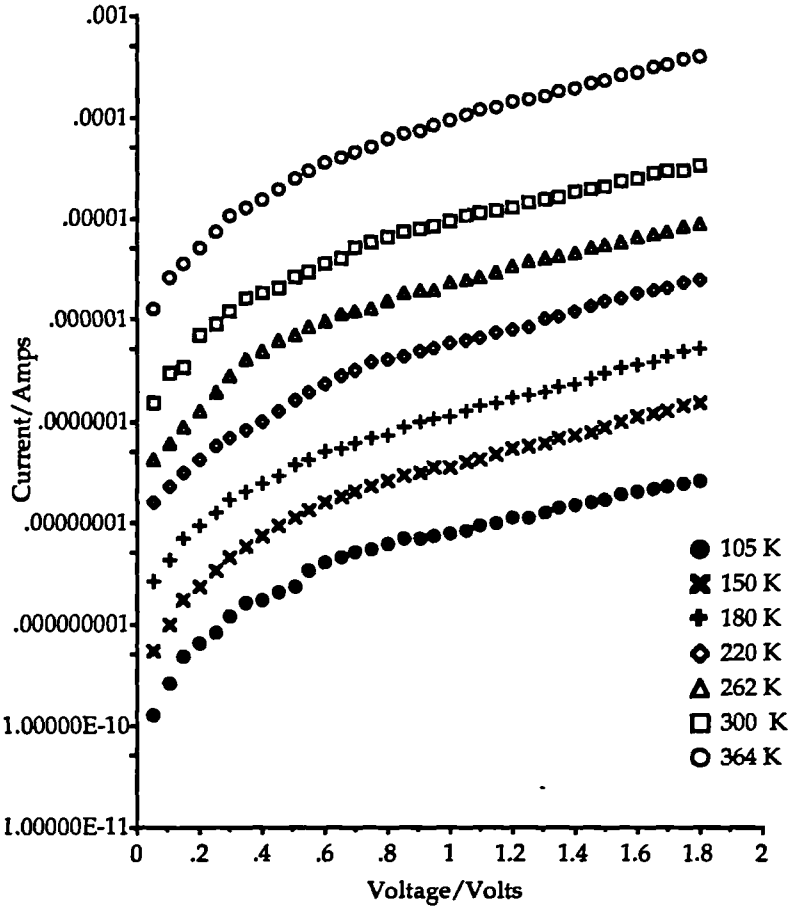

Figure 6.7 — Dark I_r-V characteristics for a n-CdS/p-CdTe diode grown on the Cd face of basal CdS at temperatures between 105-364 K

temperature affects the carrier concentration, the Fermi level and hence V_d.

The reverse, dark I_r-V characteristics for the n-CdS/p-CdTe junction grown on the Cd face of basal CdS, at temperatures between 105-364 K are shown in figure 6.7. As can be seen in comparison with figure 6.5 the junction is an excellent diode with a rectification ratio of 1500 : 1 at 0.6 V bias.

The reverse saturation current $I_o(T)$ can be reformulated as

$$I_o(T) = I_{oo}\, exp\,(\,BT\,) \qquad [6.7]$$

where B is a measure of the variation of V_d with temperature. Thus a plot of ℓn

I_o, obtained from the extrapolation of the linear region of figure 6.8, versus T gave the value of B from the slope. This was calculated to be 0.036 K^{-1} which is in good agreement with values obtained from forward I_f-V data. From figure 6.7 it can be seen that the ℓn I_r versus V plots are linear at low reverse bias, although there is some deviation at higher voltages probably due to the thermal excitation of carriers across the band gap. The rate at which the built in potential varies with temperature can therefore be calculated from equations 6.3 and 6.7, giving

$$\frac{dV_d}{dT} \cong \frac{B\,K}{A} \cong \frac{B}{A} \qquad [6.8]$$

since K≈1. The value of $\frac{dV_d}{dT}$ was calculated to be 2×10^{-3} VK^{-1}, which can be compared with values of 0.083 VK^{-1} obtained from C-V characteristics (see section 6.4.1). As with the forward bias current voltage relationship the characteristics are more aptly described by a multistep tunneling/recombination model [16]

$$\ell n\left(\frac{J_r}{V}\right) = -\alpha\,[E_{gp} + \Delta E_V]\left(\frac{E_r}{V_d - V}\right)^{\frac{1}{2}} \qquad [6.9]$$

where J_r is the current density in the reverse direction, E_r is the effective barrier for one tunneling step, ΔE_V is the valence band offset and E_{gp} is the band gap of the CdTe. A graph of $\ell n\left(\frac{J_r}{V}\right)$ versus $(V_d - V)^{-\frac{1}{2}}$ was found to be a straight line, indicating that the mechanism is indeed the tunneling of electrons from the valence band of the CdTe into the conduction band of the CdS. It can be seen from equation 6.9 that the value of the slope, Γ of the $\ell n\left(\frac{J_r}{V}\right)$ versus $(V_d - V)^{-\frac{1}{2}}$ graph is given by

$$\Gamma = \alpha\,(E_{gp} + \Delta E_v)\,E_r^{\frac{1}{2}} \qquad [6.10]$$

The gradient is temperature dependent, since α varies with N_A and E_{gp} changes linearly with temperature. N_A is temperature dependent at low temperatures up until the point where full ionisation occurs and then it becomes temperature independent. Thus at 300 K the value of the slope was 18.1 $V^{\frac{1}{2}}$. The number of steps required to traverse the depletion region, S_r, is given by

$$S_r = \frac{(E_{gp} + \Delta E_v)}{E_r} \qquad [6.11]$$

At 300 K the number of steps was found to be 2.6×10^3, whilst the height of the barriers, E_r, was found to be 1.4×10^{-3} eV. This gives the overall height of the barrier to current flow in the reverse direction as 3.6 eV. The density of traps, N_t required can also be calculated from the following equation [15]

$$J_r\, V^{-1}\, exp\, [\, \Gamma\, (V_d - V)^{\frac{1}{2}}\,] \;=\; q^2\, a\, N_t\, h^{-1} \qquad [6.12]$$

where a is the lattice parameter of the CdTe and Γ is given by equation 6.10. At 300 K a value of N_t was calculated to be 2.2×10^{11} cm^{-3}, compared with values of 2.1×10^7 cm^{-3} obtained by S.S. Ou et al [15]. The value quoted by S.S. Ou appears very small compared with densities of $\geq10^{10}$ cm^{-3} which are more common with such mismatched systems.

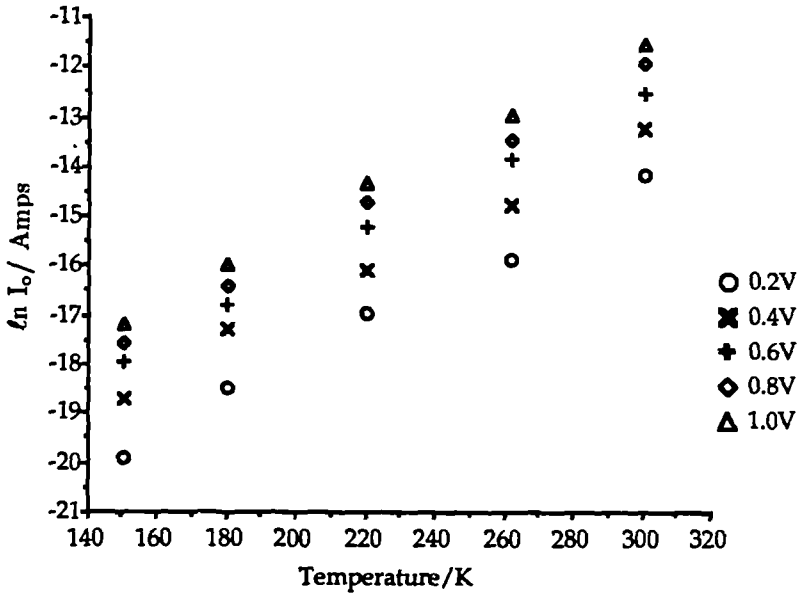

Figure 6.8 — The variation of $\ell n\ I_o$ with temperature

The experimental variation of $\ell n\ I_o$ with temperature is shown in figure 6.8. Assuming that the energy gaps of CdTe and CdS change linearly with temperature according to $E_g = E_{g,o}$-cT, N_A is fully ionised, and E_r is constant with temperature then

$$\frac{d\ell nJ_r}{dT} = -(V_d - V)^{-\frac{1}{2}}\ \alpha\ E_r^{\frac{1}{2}}\ c \qquad [6.13]$$

For CdTe, c = $4.5\times10^{-4} eV°C^{-1}$, thus a value for $\frac{d\ell nJ_r}{dT}$ was estimated from figure 6.8 to be $5.6\times10^{-6}\ V^{\frac{1}{2}}$ at a bias of -0.2 V. This value is small compared to the calculated value of 0.038 $V^{\frac{1}{2}}$ from equation 6.10. This suggests that the value of E_r is not constant with respect to temperature. The value of $\left(\frac{dE_r}{dT}\right)$ can be determined by calculating the values of E_r at different temperatures from equation 6.10. The variation in E_r with temperature is shown in table 6.2, giving a value of $\left(\frac{dE_r}{dT}\right)$ as 2.16 eVK^{-1}.

Temperature/K	E_r/eV
105	1.27×10^{-2}
150	1.33×10^{-2}
180	9.97×10^{-2}
220	3.80×10^{-1}

Table 6.2 — The change in E_r with temperature

Assuming E_r is a function of temperature then $\alpha(T)\ [E_{gp}(T)+\Delta E_r]\ \left(\frac{dE_r}{dT}\right) \approx 9.9\times10^{-3}\ V^{\frac{1}{2}}K^{-1}$, which is closer to the estimated value of the slope from figure 6.8 and similar to values obtained by Adirovich et al [17] of 0.017 $V^{\frac{1}{2}}K^{-1}$.

6.3.2 Diodes prepared on the (000$\bar{1}$)B face of CdS

Figure 6.9 shows a semilogarithmic plot of the forward I_f-V characteristics in the dark for a crystalline CdS/CdTe diode grown on the S face of the CdS at

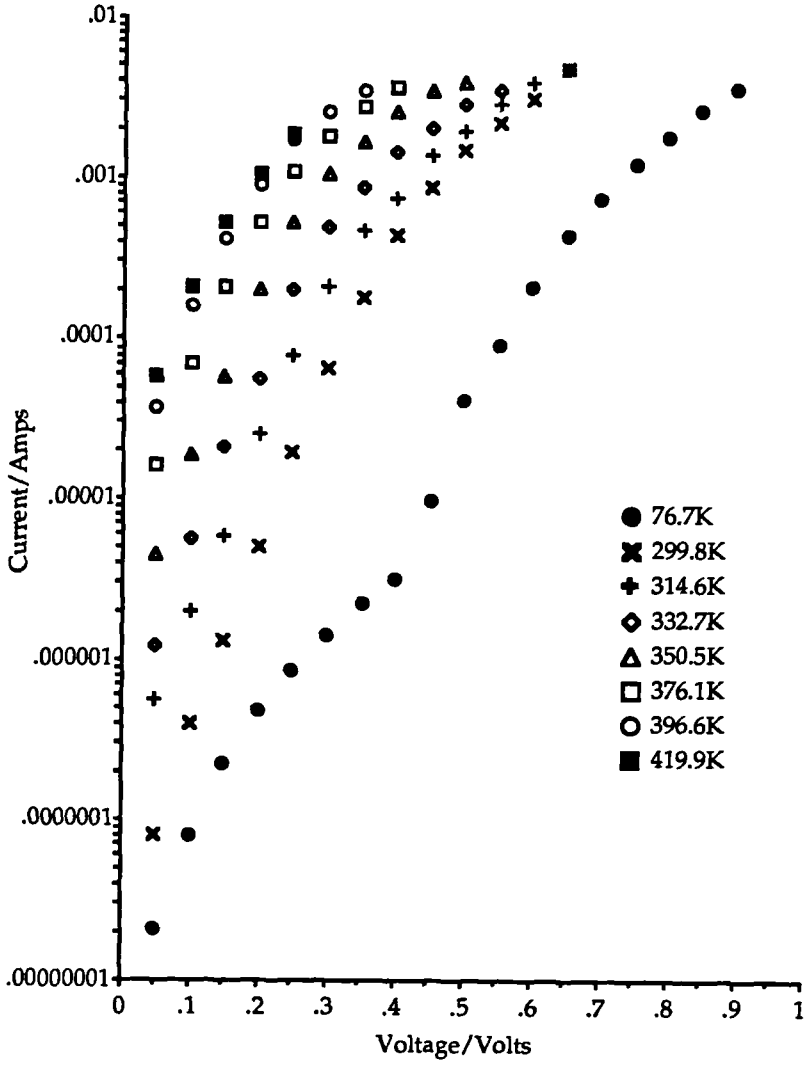

Figure 6.9 — Dark I_f-V characteristics for a n-CdS/p-CdTe diode grown on the S face of basal CdS at temperatures between 300-397 K

temperatures between 77-420 K. The plot initially appears to be very similar to that observed on the Cd face, although the current level is considerably higher. The junction rectification ratio at 0.6 V is 1200:1, approximately 20% smaller than that observed on the Cd face, however both junctions have high rectification ratios compared with 200:1 observed for crystalline CdS/CdTe junctions fabricated by Mancini et al [20] .

From figure 6.9 it can be seen that above 298 K only one current transport

mechanism exists. At low temperatures the current transport becomes dominated by the series resistance of the bulk CdS. The values of A, I_o, and n are given in table 6.3. From the table it can be seen that the value of A is constant, whilst the value of n experiences a 24% change over the temperature range 300-397 K. As with the junction formed on the Cd face of basal CdS the temperature insensitive values of A are indicative of a tunneling mechanism occurring in the diode. The value of I_o at room temperature is very low $\approx 5.8\times10^{-8}$ A, indicating a low density of defects at the CdS/CdTe interface. The value of I_o for the Cd face was 5.0×10^{-8} A, i.e very closely matched to that above.

Temperature/K	I_o/A	A/V^{-1}	n
299.8	5.8×10^{-8}	25.8	1.50
314.6	1.9×10^{-7}	25.5	1.46
332.7	4.0×10^{-7}	25.5	1.32
350.5	1.2×10^{-6}	25.5	1.25
376.1	4.0×10^{-6}	26.2	1.18
396.6	1.0×10^{-5}	25.6	1.14

Table 6.3 — Dark I-V Characteristics for n-CdS/p-CdTe diode grown on the S face of basal {0001}CdS

A plot of $\ell n\ I_f$ versus $\frac{1}{T}$ was non linear, confirming the absence of thermal activation within the junction. The value of B was calculated from the slope of the $\ell n\ I_o$ versus T graph shown in figure 6.10, and was found to be 0.058 K^{-1}.

As with the junction formed on the Cd face the measured ionised charge density can only support a multistep tunneling/recombination process across the junction. The number of tunneling steps, calculated from equation 6.12 was 49, and the mean value of each step was 7.1×10^{-3} eV. The total barrier height was thus found to be 0.347 eV. This value is almost identical to that observed for the Cd face junction.

The reverse dark I_r - V characteristics for the crystalline CdTe/CdS junction are shown in figure 6.11. A plot of $\ell n\ I_o$ versus temperature gives the value of B

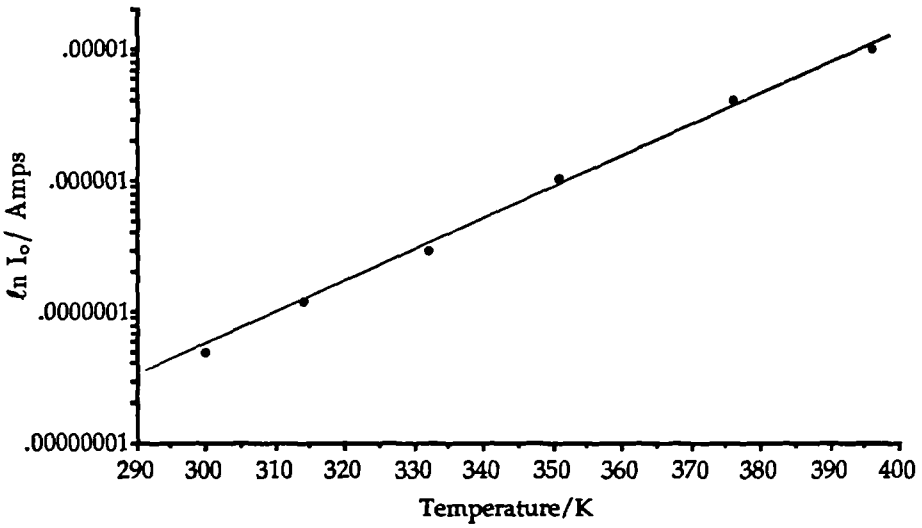

Figure 6.10 — The variation of $\ell n\ I_o$ with temperature

to be 0.0246 K^{-1}, which is smaller than that observed for the forward characteristics. The rate at which the built-in potential varies with temperature is therefore, using equation 6.8 calculated to be 2.23×10^{-3} VK^{-1}, which is in good agreement with that found from C-V data (see section 6.4.2). Again if the multistep tunneling/recombination mechanism applies a graph of $\ell n\left(\frac{J_r}{V}\right)$ versus $(V_d - V)^{-\frac{1}{2}}$ would give a straight line as observed in figure 6.12.

Using the gradient obtained from this graph, values for the number of steps S_r, and the height of each step E_r, were found to be 877 and 3.0×10^{-3} eV respectively. The total barrier height was found to be 2.64 eV. From equation 6.12 the number of traps required to support such a model was calculated to be 4.0×10^{7} cm^{-3}. As mentioned in section 6.3.1 this value is very small but is comparable with that found by S.S. Ou et al [15] on the same junction. The value of $\frac{d\ell n\ J_r}{dT}$ was found from figure 6.10 to be 0.104 $V^{\frac{1}{2}}$ at 0.2 V, whereas from equation 6.13 the value was 4.82×10^{-3} $V^{\frac{1}{2}}$. Since the value of $\frac{d\ell n\ J_r}{dT}$ is not constant, equation 6.13 was rewritten to take into account the derivatives of each variable giving

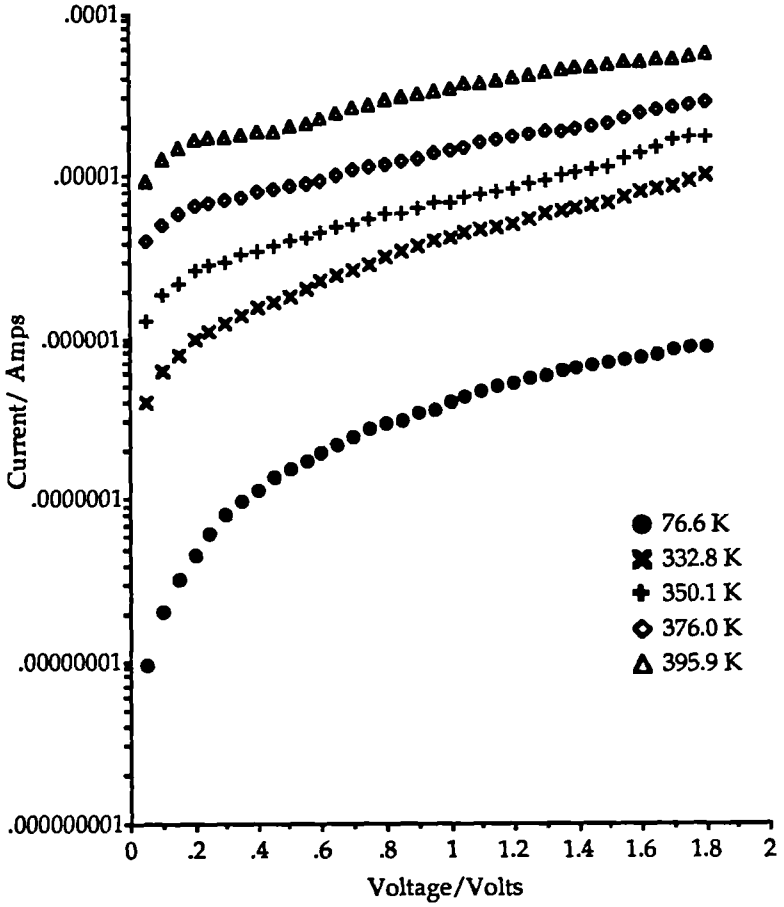

Figure 6.11 — Dark I_r-V characteristics of a n-CdS/p-CdTe diode grown on the S face of basal CdS at temperatures 77-400 K

$$\frac{d\ell n\ J_r}{dT} = \frac{-\alpha}{(V_D - V)^{\frac{1}{2}}} \left[E_r^{\frac{1}{2}} c + \frac{(E_{gp} + \Delta E_v) E_r^{-\frac{1}{2}}}{2} . \frac{dE_r}{dT} \right] \qquad [6.14]$$

A value of $\frac{dE_r}{dT}$ can be calculated from the value of E_r at different temperatures, as shown in table 6.4. The value of E_r was calculated at each temperature from the gradients of different graphs of $\ell n\left(\frac{J_r}{V}\right)$ versus $(V_d - V)^{-\frac{1}{2}}$ and using equation 6.10.

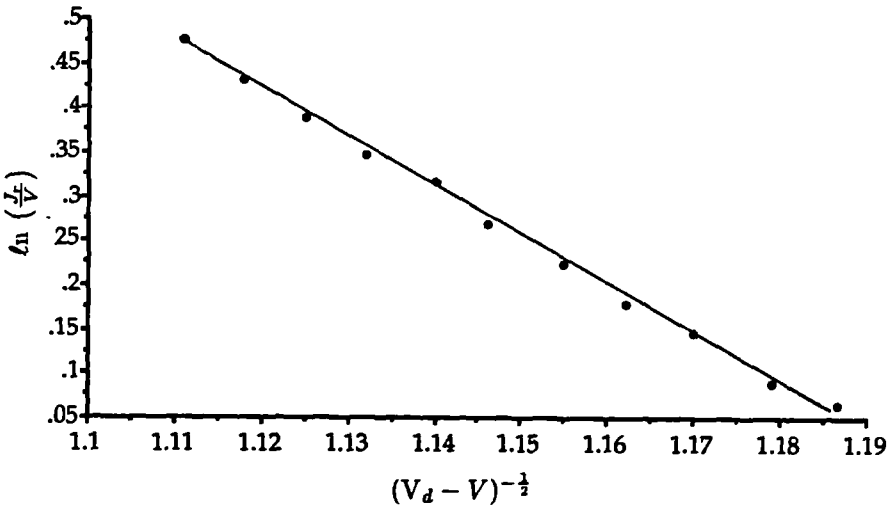

Figure 6.12 — A graph of $\ell n\left(\frac{J_T}{V}\right)$ versus $(V_d - V)^{-\frac{1}{2}}$

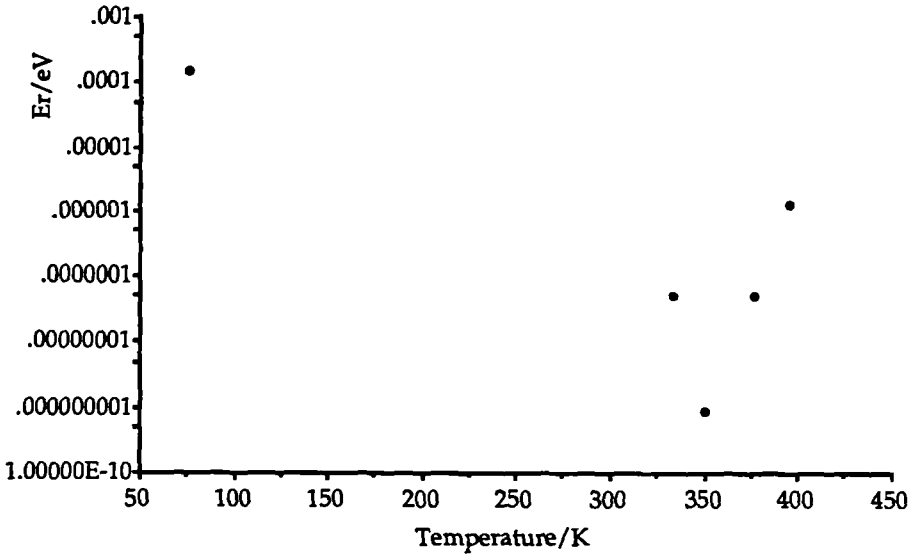

Figure 6.13 — A plot of E_r versus temperature

From figure 6.13 it can be seen that an exponential relationship exists between E_r and T. At low temperatures, N_A is not constant and thus α is not constant. As the temperature increases, N_A increases and the values of the gradients of the $\ell n\left(\frac{J_T}{V}\right)$ versus $(V_d - V)^{-\frac{1}{2}}$ curves are seen to increase, as expected from equation 6.10. At temperatures greater than 330 K, E_r increased monatomically with temperature and the gradient was found to be 1.1×10^{-7} eVK^{-1}. However, this value

is so small it does not bring the value of $\frac{d\ln J_r}{dT}$ any closer to its experimental value, for this to be the case the value of $\frac{dE_r}{dT}$ would have to be much larger. The reasons for the discrepancy are not known.

Temperature/K	Gradient/eVK^{-1}	E_r/eV
76.6	5.83	1.5×10^{-4}
332.8	0.11	5.2×10^{-8}
350.1	0.02	8.5×10^{-10}
395.9	0.54	1.3×10^{-6}

Table 6.4 — The change in E_r with temperature

6.4 Capacitance - Voltage Characteristics

6.4.1 Diodes prepared on the (0001)A face of CdS

Capacitance- voltage measurements of the samples were studied in order to gain further insight into the nature of the junction. Dark junction capacitance voltage characteristics of the n-CdS/p-CdTe grown on the Cd face were investigated in their as prepared states. Plots of C^{-2} versus applied reverse bias are shown in figure 6.14, for temperatures between 76-330 K. The plots yielded straight lines indicating the abrupt nature of the junction between the CdS and the CdTe. The change in slope at higher reverse bias can be attributed to either the uncovering of a deep level, or as a result of interdiffusion at the junction interface, which is thought to introduce a more highly compensated layer at the interface, or due to the lattice mismatch.

In order to understand the current transport mechanism it is important to measure the ionised charge densities from the C^{-2} versus V plots for a range of temperatures. Table 6.5 shows the net acceptor density, N_A - N_D, values obtained

from the slope of the straight lines, using the standard interpretation from section 2.4.4. The depletion region width inferred from the conventional formula,

$$\left(\frac{C}{A}\right)_{v=v_0} = \frac{\epsilon\,\epsilon_0}{W_{(V_0)}} \qquad [6.15]$$

at room temperature was found to be 0.7 μm. However, there is a degree of uncertainty in the area measurement and consequently values inferred from C-V measurements by the usual interpretation may not be reliable.

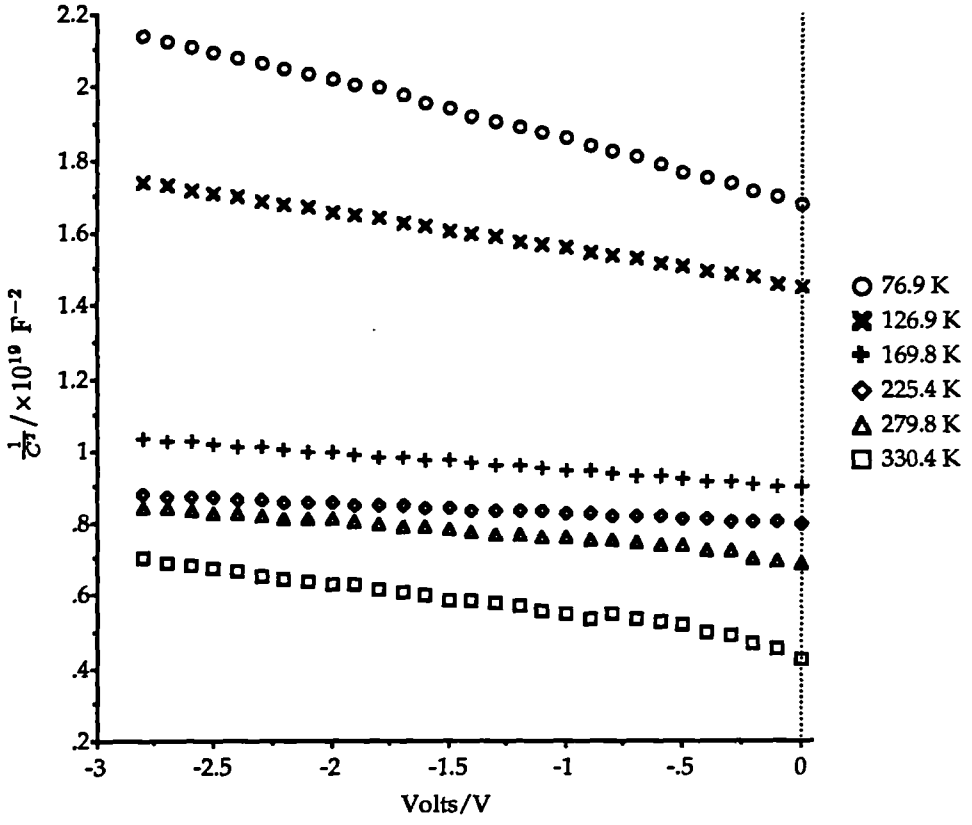

Figure 6.14 — C^{-2} versus reverse applied voltage for n-CdS/p-CdTe diode grown on the Cd face

A net free carrier concentration of $\approx 1.3\times10^{16}$ cm^{-3} was calculated from Hall measurements for a p-CdTe layer grown under the same conditions, which is in

good agreement with those obtained by C - V measurements. The values of zero bias dark capacitance varied significantly with temperature to give a corresponding range in depletion widths from 1.1 μm to 0.6 μm. Despite the ambiguity as to the effective junction area it can be seen that there is a factor of 2 change in the depletion width from 77-330 K. The values of N_A - N_D also changed from 8.8×10^{15} - 7.8×10^{16} cm^{-3}, suggesting that the density of positively charged levels in the depletion layer had decreased at low temperatures.

Thus the difference in the measured values of N_A - N_D at 279.8 and 76.9 K gave an indication of the density of carriers that could be ionised at room temperatures $\approx 2.3\times10^{16}$ cm^{-3}.

Temperature	N_A-N_D/cm^{-3}	V_d/V	W/μm
76.9	8.8×10^{15}	9.90	1.09
126.9	1.4×10^{16}	14.00	1.02
169.8	3.1×10^{16}	18.67	0.80
225.4	5.2×10^{16}	28.00	0.76
279.8	3.2×10^{16}	5.52	0.70
330.4	7.8×10^{16}	3.60	0.57

Table 6.5 — C-V data for n-CdS/p-CdTe cell grown on Cd face

As mentioned in section 6.3.1 the acceptor concentrations are sufficiently low that it is not expected that this would allow a simple tunneling/recombination process. As the voltage tends to zero the straight line observed in the C^{-2} versus V plot becomes curved, which could result from the interdiffusion at the junction or from the migration of defects introduced at the interface during fabrication into the bulk. However, the extrapolation of the slopes of the C^{-2} vs.V plot at low reverse bias gives a value of the voltage intercept of 5.52 eV at room temperature compared with the theoretical value of 1.13 eV given by K.W. Mitchell et al [21]. The large value observed experimentally indicates the presence of some interfacial layer or surface states which would act in series with the potential of the depletion region, also accounting for the curvature observed in the C^{-2} versus V plot.

The rate of change of the built-in potential with temperature is not constant throughout the whole temperature range. At low temperatures $\frac{dV_d}{dT}$ values increase with increasing temperature, but above room temperature the value saturates, giving a value of $\frac{dV}{dT}$ as 0.038 VK^{-1}.

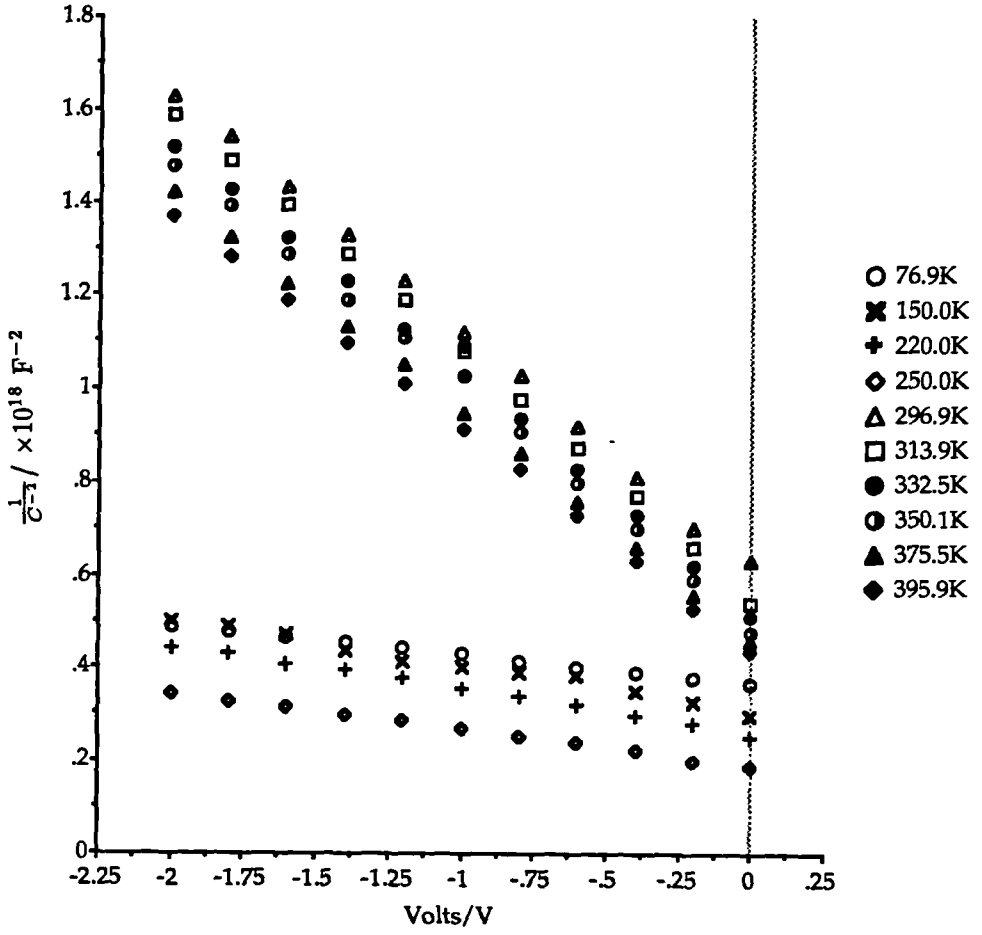

Figure 6.15 — C^{-2} versus reverse applied voltage for n-CdS/p-CdTe diode grown on the S face

6.4.2 Diodes prepared on the (000$\bar{1}$)B face of CdS

The dark junction capacitance voltage characteristics of the n-CdS/ p-CdTe

device grown on the S face at different temperatures are shown in figure 6.15. It can be seen that two different regions exist, one below room temperature where the gradients of the curves give rise to N_A - N_D values of $\approx 10^{17}$ cm^{-3} and above room temperature where N_A - N_D values of 5×10^{16} cm^{-3} are obtained. Again all plots revealed the abrupt nature of the junctions and the possible presence of deep levels due to the change in slope with temperature. The results obtained from detailed analysis of figure 6.15 are given in table 6.6.

Temperature	N_A - N_D/cm^{-3}	V_d/V	W/μm
78	2.18×10^{17}	5.44	0.23
150	1.55×10^{17}	3.00	0.21
220	1.59×10^{17}	2.81	0.19
250	1.89×10^{17}	2.45	0.16
297	2.77×10^{16}	1.07	0.29
314	2.83×10^{16}	0.98	0.28
333	2.91×10^{16}	0.91	0.27
350	2.94×10^{16}	0.87	0.26
376	3.06×10^{16}	0.83	0.25
396	3.16×10^{16}	0.79	0.24

Table 6.6 — C-V data for n-CdS/p-CdTe cell grown on the S face

At room temperature the depletion region was found to be 0.29 μm wide. This device was formed using a grid contact and thus the values inferred from C -V data are more accurate than those obtained with devices made on the Cd face. The width of the depletion region was found, again, to vary by a factor of 2 over the temperature range tested. The value of N_A - N_D also changed from 2×10^{17} to 2×10^{16} cm^{-3} as the temperature was raised, leading to the value for the ionised charge density at room temperature as 1.9×10^{17} cm^{-3}. There are two separable regions, one below room temperature where the depletion width is reduced as the temperature is raised as carriers are ionised. The depletion region then doubles in width at room temperature. Reasons for this are unclear, it could be that at low temperatures the device contacts are no longer injecting, since the carriers freeze out underneath causing the contacts to become rectifying.

The intercept value obtained by extrapolating the slope of the C - V curve at low bias was found to give 1.07 V at room temperature. This value is slightly lower than that expected theoretically. Donnelly and Milnes [19] considered that the junction capacitance was affected by the presence of interface states which would give rise to an additional charge per unit area, Q, and to electric dipoles, Ψ. The slopes of the C^{-2} versus applied voltage curves would be the same as before except the voltage intercept would be given by

$$V_{di} = V_d - \Psi - \left(\frac{Q^2}{2\,q\,(\epsilon_p N_A + \epsilon_n N_D)}\right) \qquad [6.16]$$

With the presence of traps in the space charge region the measured value of the capacitance cut off voltage V_{di} is always less than the true diffusion potential, V_d by an amount ΔV_d. The rate of change of built-in potential with temperature again is not constant over the temperature range considered. Above room temperature, however the value was found to be 2.83×10^{-3} VK^{-1}, which is in close agreement with 2.78×10^{-3} VK^{-1} obtained from forward I -V data.

6.5 Spectral response

The spectral response was measured for all devices in order to investigate the correlation between the spectral dependence of the quantum efficiency and the structural information obtained from RHEED studies. The spectral distribution of the quantum efficiency normalised to constant photon density, at room temperature for both the n-CdS/p-CdTe devices grown on the Cd face and S face are shown in figure 6.16.

The responses exhibit similar behaviour for the two types of device but with a slightly narrower response for the device grown on the S face and a lower quantum efficiency, $\approx$ 65% compared with 96% for those grown on the Cd face. In the devices the short and long wavelength cut-offs agree with the absorption edges of the CdS and CdTe respectively. The curves rise at 1.43 eV and decrease gradually with increasing energy. It can be seen that the spectral response of the S face

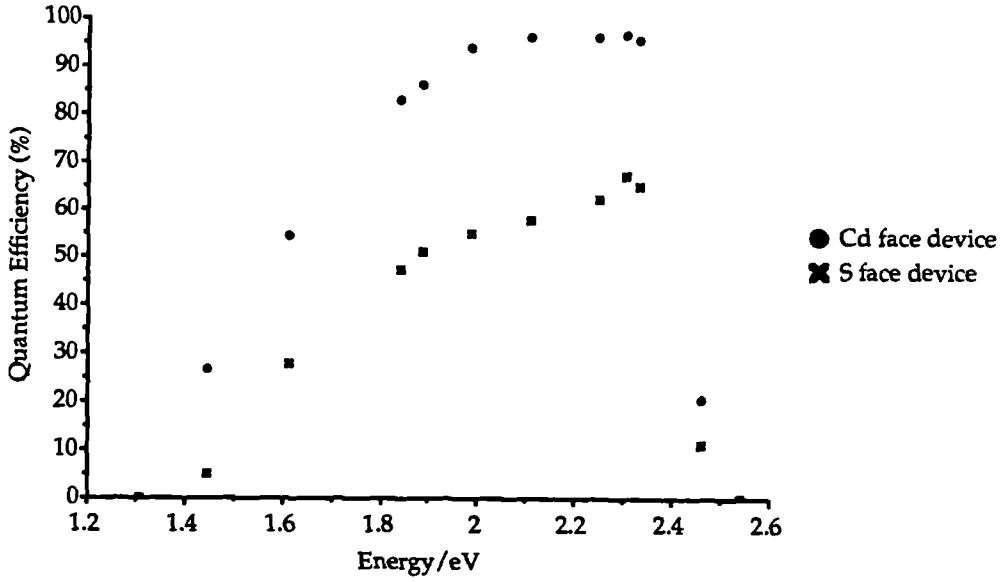

Figure 6.16 — The spectral response of n-CdS/p-CdTe diodes grown on the Cd and S faces of basal CdS

diode decreases more rapidly than that of the Cd face diode leading to a narrower response width. The high energy cut off of the spectral response is defined by the absorption edge of the CdS. The shape of the CdTe cut-off is defined by the collection of photocurrent from the CdTe, described by minority carrier transport equations. The CdS substrate is sufficiently thick that the light absorbed in the CdS does not contribute to the photocurrent. The light current, I_L is defined by

$$I_L(v,\lambda) = H(v,\lambda)\, q\, \Phi(\lambda) \qquad [6.17]$$

where $H(v,\lambda)$ is the voltage dependent collection function and $\Phi(\lambda)$ is the photon flux reaching the CdTe bulk (see section 2.4.5). $H(v,\lambda)$ is also represented by

$$H(v,\lambda) = h(v)\, g(v,\lambda) \qquad [6.18]$$

where $h(v)$ is the fraction of photogenerated minority carriers that pass through

the junction on reaching it and $g(v,\lambda)$ is the fraction of photogenerated minority carriers arriving at the junction interface. Thus any recombination at the junction interfaces, due to lattice mismatch will affect $h(v)$ and reduce it from unity. Thus

$$g(v,\lambda) = 1 - [1+\alpha(\lambda)L]^{-1} \, exp\,(-\alpha(\lambda)\, W) \qquad [6.19]$$

and

$$h(v) = \left(\frac{1 + C}{\mu_e \epsilon}\right)^{-1} \qquad [6.20]$$

where $\alpha(\lambda)$ is the absorption coefficient, L is the bulk minority carrier diffusion length, W is the depletion layer width in the CdTe, C is the interface recombination velocity, μ_e is the electron mobility and ϵ is the electric field at the junction.

At short wavelengths $\alpha(\lambda)$ is high and $g(v,\lambda) \rightarrow 1$. Thus $H(v,\lambda)$ is $\approx h(v)$. At zero bias the value of $h(v)$ for the Cd face device was calculated to be 0.96, from the spectral response data. As the photon energy approaches the band gap of CdTe, absorption occurs. The CdS is transparent to photons having energies less than the band gap of 2.42 eV. These photons will be transmitted to the interface and electron/hole pairs created by photons having an energy greater than the band gap of CdTe and, within one diffusion length of the depletion layer of CdTe, will start contributing to the photocurrent. As the energy of the photons increases the excitation of carriers continues until it reaches the CdS band gap, where additional electron/hole pairs are created and swept apart by the electric field existing in the CdS. As the photon energy increases further the photocurrent falls sharply due to the absorption of these photons occuring at the surface of the CdS. The relative contributions of the two sides to the total photocurrent depends on the relative band bending and the depletion layer width on both sides of the junction. These parameters depend on the doping concentrations of the semiconductors in either side of the junction. Usual heterojunction theory predicts that the band bending within semiconductors depends on their doping according to the relation

$$\frac{V_b^{CdS}}{V_b^{CdTe}} = \frac{N_D^{CdTe}\,\epsilon_{CdTe}}{N_A^{CdS}\,\epsilon_{CdS}} \qquad [6.21]$$

where V_b is the band bending and N_A and N_D are the doping levels and ϵ_{CdTe} and ϵ_{CdS} are the dielectric constants. Since $N_D >> N_A$ carrier photogeneration occurs almost entirely within the CdTe and the CdS acts entirely as a semitransparent collection electrode. A reason for the gradual increase in the CdTe absorption edge could be that band edge discontinuities and the recombination of the photocarriers at interface states impede collection of minority carriers. The blue-green photoresponse cut off limits the photocurrent density and is due to the thickness of the CdS substrate. Not only will a thick CdS layer reduce the photocurrent density but will also introduce reflection losses. The cell photoresponse could be extended into the blue region, if the CdS was replaced by $Cd_{1-x}Zn_xS$ in order to widen the window gap. The presence of zinc however is known to reduce the CdS electrical conductivity.

The photoresponses of devices with undoped or slightly doped films generally exhibit a cut-off at short wavelengths followed by a sharp maximum at 2.4 eV. In contrast devices with strongly conducting window layers the photocurrent signal increases regularly after the spectral cut off at 2.4 eV, without showing any peak in the visible region.

6.6 Photocapacitance Studies

The photocapacitance of the diodes grown on the Cd face was measured at liquid nitrogen temperatures and the spectra are given in figure 6.17.

The photon energy was scanned from 0.7 eV to 2.5 eV. There was an initial shallow decrease in capacitance on going to 0.9 eV, suggesting the existence of a negative going threshold at some photon energy less than 0.8 eV, however this was at the limit of the wavelength resolution of the photocapacitance technique. A shallow rise was then observed near 1.2 eV which dipped before a dramatic rise at 1.47 eV. Above 2.32 eV the photocapacitance started to decrease again slowly.

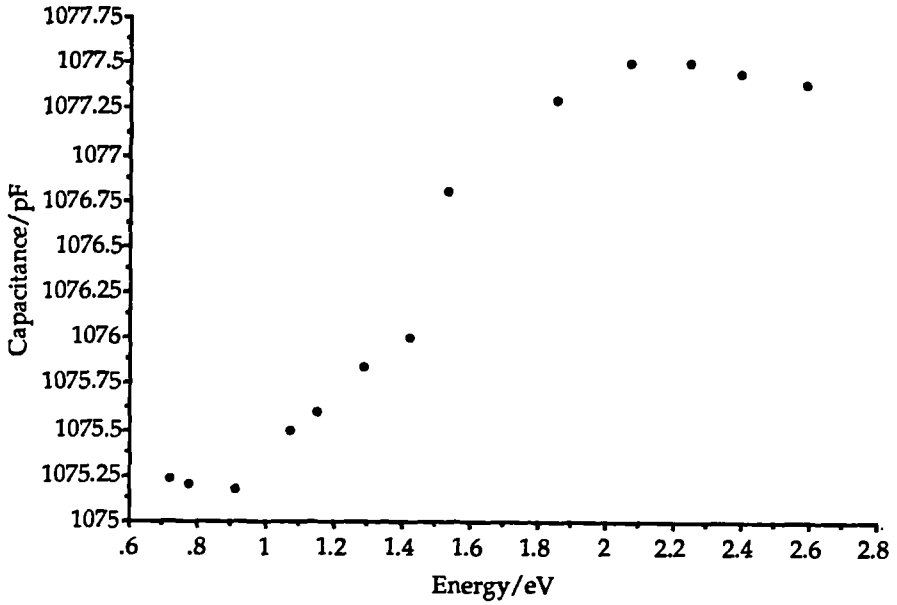

Figure 6.17 — The photocapacitance spectrum of a diode grown on the Cd face

The threshold and sign of the capacitance change identifies the process of emptying or filling of the impurity level. Generally a decrease in capacitance indicates a net increase in stored negative charge, possibly in the filling of acceptor like levels with electrons. Steady state photocapacitance allows an average picture of states in the depletion region, but capture cross sections cannot be evaluated. This can only be done by measuring the transient photocapacitance.

The positive going threshold observed around 0.9 eV is difficult to explain. The increase in photocapacitance is associated with the transition of electrons from filled levels to the conduction band, so this initial rise could be related to the emptying of a level with an ionisation energy $\approx$ 0.9 eV. Defect levels with energies between 0.6-0.9 eV have been reported by Zanio et al [22]. This shallow rise at 0.9 eV could indicate the presence of a level 0.60 eV above the valence band and these could be due to Cd vacancies present perhaps due to the presence of As becoming a substitutional impurity. This is often found in materials which are known to self compensate. The slight dip at 1.2 eV corresponds to the filling of the level that is responsible for the positive threshold at 1.47 eV i.e. the presence of a localised level existing 0.1 eV below the conduction band. The sharp rise in capacitance at 1.47 eV (at liquid nitrogen temperatures) is due to the optical excitation from a level 0.075 eV above the valence band to the conduction band. The band gap

of CdTe at 80 K is 1.60 eV [23]. Acceptor levels attributed to trace impurities of lithium and sodium are responsible for the well known donor-acceptor pair band edge emission in photoluminescence. Thus it is tempting to assign the positive change in ΔC to common alkali metal impurities. The negative threshold at 2.3 eV is attributed to a donor level lying 0.1 eV below the conduction band. The capacitance is reduced when the donor level is filled from electrons excited from the valence band.

6.7 Discussion

In this study the intention has been to investigate two different solar cell structures fabricated by MOVPE, one grown on the S face of CdS and one formed on the Cd face, to compare the effects polarity has on the operation of the device. Structural observations described in section 5.5.2 confirmed that devices grown on the S face of basal oriented CdS were superior in crystalline quality, those layers grown on the Cd face proving to be polycrystalline. This chapter compares the effect this structural difference has on the electrical phenomena occurring within the device. Table 6.7 compares the differences observed in the devices prepared under the same growth conditions and with similar device areas.

Initial predictions would expect the device grown on the S face to have a higher performance as there would be a fewer suspected number of dislocations, due to grain boudaries found within polycrystalline devices. Observation proved otherwise, devices formed on the S face of {0001}CdS consistently gave values of solar efficiency at least two times smaller than that observed on the Cd face devices.

The value of V_{oc} was higher for the single crystal device, as would be expected. The rough surface topography found in the polycrystalline devices would mean that the actual junction area would be much larger than the corresponding flat plane area. Since such a surface is not reflecting, the value of J_{sc} would be higher, as observed, causing V_{oc} to become lower. At high temperatures only one transport

The effects of polarity measured device characteristics			
Diode characteristics			
Cd-face (polycrystalline)		S-face (single crystal)	
$V_{oc} = 0.42V$ $I_{sc} = 121$ mA $ff = 38\%$ $\eta = 4.22\%$		$V_{oc} = 0.52V$ $J_{sc} = 42$ mA $ff = 16\%$ $\eta = 1.49\%$	
Current-transport characteristics			
I_o (300K) = 5.0×10^{-8} A A = 17.8 V^{-1} T$\geq$ 250K $n \approx 2$ B = 0.036 K^{-1} $N_t = 2.2\times10^{11}$ cm^{-3} $\frac{dV_d}{dT} = 2.0\times10^{-3}$ VK^{-1} Rectification ratio 1500 : 1 at 0.6V		I_o (300K) = 5.8×10^{-8} A A = 25.7 V^{-1} T$\geq$ 250K $n \approx 1.3$ B = 0.025 K^{-1} $N_t = 4.0\times10^{7}$ cm^{-3} $\frac{dV_d}{dT} = 2.2\times 10^{-3}$ VK^{-1} Rectification ratio 1200 : 1 at 0.6V	
Multistep tunneling data			
Forward bias	Reverse bias	Forward bias	Reverse bias
R = 104 S = 3.3×10^{-3} eV R.S = 0.34eV	$S_r = 2.6\times10^{3}$ $E_r = 1.4\times10^{-3}$ eV $\frac{dlnJ_r}{dT} = 0.038$	R = 49 S = 7.1×10^{-3} eV R.S = 0.35eV	$S_r = 877$ $E_r = 3.0\times10^{-3}$ eV $\frac{dln\ J_r}{dT} = 0.104$
Capacitance-voltage characteristics			
N_A - $N_D = 3.2\times10^{16}$ cm^{-3} $V_d = 5.52$ V W = 0.70μm T$\geq$ 300K $\frac{dV_d}{dT} = 0.038$ VK^{-1}		N_A - $N_D = 5.0\times10^{16}$ cm^{-3} $V_d = 1.07$ V W = 0.29μm T$\geq$ 300K $\frac{dV_d}{dT} = 2.83\times 10^{-3}$ VK^{-1}	

Table 6.7 — Summary of n-CdS/p-CdTe device characteristics

mechanism exists and V_{oc} can be expressed by

$$V_{oc} = \left(\frac{nkT}{q}\right) \ell n \left[\left(\frac{I_{sc}}{I}\right) + 1\right] \qquad [6.22]$$

From this equation it would be assumed that high values of n would be desirable in obtaining high open circuit voltage values. This, however, is not the case since a high value of n is usually associated with high values of I. In reality, V_{oc} for p-n junctions are always higher for low values of n (close to unity) [24] as observed with these devices.

The only discrepancy observed within these results is the very low fill factor observed for the crystalline device which has led to a lower efficiency. Generally the fill factor improves with increasing values of V_{oc} and decreasing values of n. The only possible explanation for the lowering of the fill factor can be due to resistive effects. Several devices were made to confirm that the low values of fill factor were not related to the contact resistance. In general, within the n-CdS/p-CdTe devices the metal-semiconductor contact resistance is known to be one of the major effects leading to a smaller efficiency than that predicted theoretically. The results obtained for the MOVPE grown devices however consistently confirmed the lower value of ff observed in the S face devices. The reason for this is as yet unclear. Other than resistive effects, the fill factor is also affected by the collection factor, the product of the fraction of photogenerated minority carriers arriving at the junction and the fraction of minority carriers that pass safely through the junction on reaching it. It is the transport across the interface that is important because it is here that carriers can be lost by recombination. Detailed RHEED studies presented in section 5.5.2, showed that whilst the S face growth is crystalline it did contain a high density of twin lamellae lying parallel to the substrate/epilayer interface. It could be postulated that this twinning actually increases the resistance of the CdTe epilayer since the twin boundaries are perpendicular to the current transport path, whereas misfit dislocations may actually enhance carrier movement.

Following the observation of defects in (111) HgTe it has been shown that twinning reduces Hall mobilities in layers grown on this orientation as opposed to layers grown on (100) oriented planes, which would already contain a high density

of misfit dislocations [25]. The presence of lateral twins would, therefore, reduce the current density and the fill factor, whilst still maintaining a high value of V_{oc}.

From the current transport analysis it can be seen that in both devices tunneling appears to be the dominant mechanism above room temperature, whereas below it is dominated by the series resistance of the bulk CdS. It is evident that a good junction is formed on the Cd face of the CdS crystal, characterised by a higher rectification ratio than that obtained on the S face of CdS. As mentioned earlier the better diode might have been expected to be the one prepared on the crystalline face, due to the better surface morphology observed. Again this unusual behaviour is not readily explainable. Mancini et al have also observed higher rectification ratios on the Cd face devices in their single crystal n-CdS/p-CdTe devices [20]. Their observations however also showed that the Cd face devices had a better surface morphology [26] reasoned by the fact that the S face devices were more disturbed at an atomic level due to the chemical etching effects on the thin elemental sulphur surface. Growth temperatures of the CdTe layer were however higher in Mancini's cells and the CdS substrates were etched in a HCl etch which is known to leave a high density of etch pits on the S face [27]. The CrO_3/HNO_3 etch used in this study has been shown to have the reverse effect, i.e. leaving the S face smooth and the Cd face with a high density of hillocks. The relatively smooth S face substrate has thus been prevented from forming an abrupt junction with the CdTe and this can only arise from surface effects. Prior to epitaxial growth the substrates are heated to 400°C for ten minutes under hydrogen. This heat treatment gets rid of adsorbed oxygen on the substrate surface, it may however have some effect on the surface structure. Generally annealing is known to improve the recrystallisation of surfaces [28,29], but the heat treatment has also been known to change the electrical properties of devices formed [30]. This can be explained by the production of single intrinsic defects, such as Cd or S vacancies or Cd interstitials or of partial evaporation of an over-stoichiometric component, usually Cd.

The current transport data has revealed a difference in the number and magnitude of tunneling steps necessary to surmount the barrier to current flow experienced in forward and reverse bias. The barrier height to current flow in the forward direction is the same for both S and Cd face devices. For the Cd face

(or A face), in forward bias the number of steps is greater and the height of each step smaller, giving a total height of 0.34 eV. For the S face or B face, in forward bias the number of steps is smaller probably due to the lower density of misfit dislocations but there are a greater number of them leading to a barrier height of 0.347 eV also. The barrier in reverse bias is however different as would be expected from the difference in the two rectification ratios for the junctions. The number of steps was again much smaller on the Cd face, but the overall height was smaller on the S face cell. Thus this explains the lower rectification ratio found on the S face and offers some explanation for the lower efficiencies found on this face.

Capacitance -voltage characteristics confirmed similar values of N_A-$N_D \approx 10^{16}$ cm^{-3}, but with differing values of V_d and W at room temperature. V_d is much greater for the Cd face device and so was the depletion width. The higher value of V_d is assosciated with a larger number of interface states which would be expected on the Cd face growth, giving a wider depletion width.

The spectral response data shows basically the same behaviour for the two types of device, but with a slightly narrower response for the S face growth and with a value of $h(v) \approx 0.65$ compared with 0.96 for the Cd face growth. This would suggest that the collection effeciency is much lower and again would explain the lower overall solar efficiency observed in the S face devices. The cut off at the CdTe band edge is much sharper for the Cd face response, thus giving a larger range of wavelengths over which the photons are absorbed. The spectral response is determined by the number of electron/hole pairs generated in the CdTe and the CdS and the interface collection factor. For these cells all the current is photo-generated in the CdTe, so the magnitude of light generated is determined by the intensity and wavelength of incident light and the properties of the CdTe layer, such as the thickness, the minority carrier diffusion length,and the absorption co-efficient. The thickness and absorption coefficients were the same for both devices and the spectral response recorded for both were of similar shape, although with a considerable difference in magnitude. The density of electron hole pairs created under defined illumination is the same for both A and B face devices, but there is an immense difference between their collection efficiencies and this is the root of the differences in their operational parameters. Thus the difference in cell performances between the Cd and S face devices must be attributed to the differences in

the recombination paths through the interface states. It is not easy to measure the interface parameters of the CdS/CdTe heterojunctions, but with Cd face devices it is expected that there is a high local interface state density, with a corresponding high interface recombination velocity which would affect the interface collection factor. This would lead to poor rectification,and the V_{oc} would be limited. The results have however shown fairly high rectification ratios, but confirm the low V_{oc} values.

The S face devices have twins which intersect the misfit dislocations, the combination of these two types of defects seems to provide further recombination pathways within the material, leading to poorer rectification behaviour, and a smaller collection factor. Thus Cd face devices provide better diodes, maintaining higher rectification ratios despite the polycrystalline nature of the device. This can only be attributed to the slight crystalline nature observed in the RHEED patterns. It is difficult to know, since RHEED is so surface sensitive whether the initial growth is singular and then perhaps the cooling effect of the reactants may lead to polycrystalline deposits falling on the surface after the end of the MOVPE growth, when the substrate has cooled but the reactants are still reacting. Indications are that the density of interface states on the Cd face growth are much lower.

The photocapacitance results indicate the existence of 3 levels, with energies of 0.10 eV below the conduction band, and 0.08 eV, 0.60 eV above the valence band. The temperature variation of the capacitance (figure 6.18), may be an indication of deep donor like levels (although a detailed study is not attempted, since this would require Deep Level Transient Spectroscopic analysis (DLTS)).

The presence of a large density of deep donor levels would give rise to a more abrupt band profile, as observed in the linear relations of the C^{-2} versus V data in figures 6.14 and 6.15. Donor concentrations obtained from the capacitance studies indicate that the tunneling probabilities from the conduction band of the CdS into interface states are fairly small, these deep levels would increase the tunneling probabilities considerably by narrowing the tunneling distances and increasing the electric fields near to the surface.

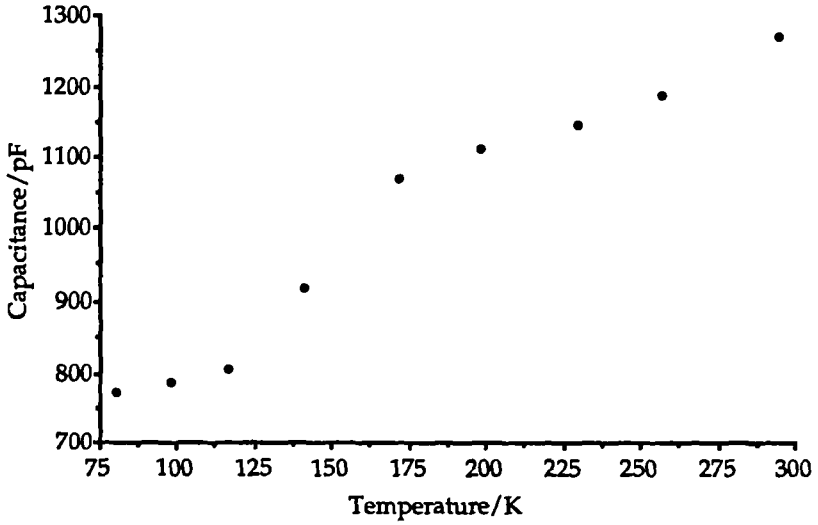

Figure 6.18 — The variation of capacitance with T for a Cd face device

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Chapter VII

The n-CdTe /p-ZnTe Solar Cell Grown by MOVPE

7.1 Introduction

Another II-VI heterojunction which has potential as a solar convertor is the p-ZnTe/n-CdTe system, having a theoretical efficiency of 14% [1]. This system has only a 5.8% difference in lattice spacings, but has quite a high diffusion voltage of 1.28 eV and a spike of 0.04 eV in the conduction band, which limits the quantum efficiency. Only two previous reports exist on the fabrication of this solar cell, one by close spaced vapour transport (CVST) of n-type CdTe onto a p-type {111} oriented ZnTe single crystal [2], and the other by chemical vapour deposition (CVD) of p-type ZnTe onto n-type CdTe single crystal platelets [3]. The highest efficiency reported has been 9.7% [3] but no work has been done to improve this junction or to make epitaxial cells by MOVPE.

The work in this chapter includes a brief description of the fabrication of the n-CdTe/p-ZnTe devices by MOVPE . The electrical properties of the cells are then described in detail including light and dark I-V measurements leading to current transport observations, spectral response, C-V and photocapacitance for the devices. A comparison of the experimental results can be utilised to suggest a band structure diagram for the n-CdTe/p-ZnTe device, which is discussed in section 7.7.

7.2 Diode Characteristics

The CdTe crystals used in this study were grown in our laboratories by a vapour phase technique originally described by Clark and Woods [4] for CdS crystals and recently adapted for CdTe. Slices of CdTe were oriented using Laue back reflection

x-ray diffraction to the {100} planes and cut using a diamond saw. The slices were annealed in Cd vapour for 48 hours to produce n-type CdTe substrates of resistivity $\approx 10^{-4}\ \Omega cm^{-1}$, which were then hydroplane polished using a 1% Bromine solution in (20:80) ethylene glycol:methanol mixture for 10 minutes, and washed thoroughly in IPA and trichloroethane. RHEED studies have shown it to be a good technique for producing exceptionally flat, strain free single crystal surfaces (see chapter 4). After etching the CdTe wafers were loaded into the MOVPE reactor and heat cleaned at 410°C for 10 minutes to reduce the oxide on the surface. Layers of p-type ZnTe $\approx 0.5\mu m$ thick were grown onto the n-CdTe surface using the conditions described in section 5.7. On removal from the reactor a gold point contact was evaporated onto the p-type ZnTe and the samples annealed in N_2 for 1 minute to produce a good ohmic contact (see section 5.9). Unwanted growth of ZnTe around the sides and edges was etched off using a 1% Br_2/MeOH mixture, and a back contact to the CdTe was made using evaporated indium.

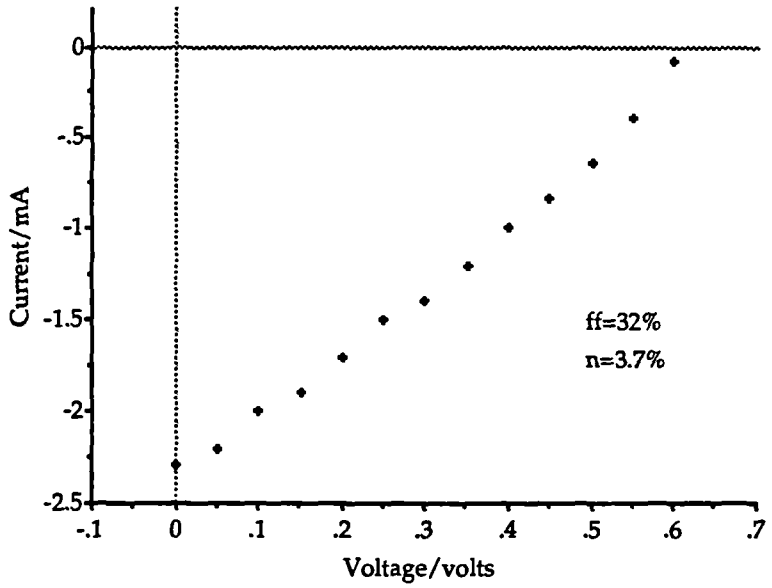

Figure 7.1 — The solar output of a n-CdTe/p-ZnTe diode under AM1.5 illumination

A typical diode characteristic of a cell illuminated through the ZnTe under AM1.5 illumination at 25°C is given in figure 7.1. The values of V_{oc}, I_{sc} and ff

are 0.61, 2.3 mA and 32% respectively. The short circuit current density J_{sc} was calculated, assuming the area of the device to be the contact area (a 1mm diameter dot) to be 292 $mAcm^{-2}$. This value is again unreasonably high as with values obtained for n-CdS/p-CdTe devices described in section 6.2. The contact area was a lot smaller than the junction area giving inaccuracies in the current density measurements. From spectral response data the value of J_{sc} was calculated to be 16.3 $mAcm^{-3}$, thus giving a value of the efficiency of 3.7%. This value seems in better agreement with that obtained by Razyhov [3].

7.3 Current-transport mechanisms

Current-voltage characteristics of the n-CdTe/p-ZnTe heterojunction were also studied to understand the dark conduction mechanisms operative within these devices. Figure 7.2 shows a semi-logarithmic plot of the forward I-V characteristics for a typical device at temperatures between 76-375 K.

Temperature	Region A			Region B			Region C		
	A	n	I_o/A	A	n	I_o/A	A	n	I_o/A
76.3	13.6	11.2	8.5×10^{-7}	1.6	96.8	8.0×10^{-6}	2.3	66.7	4.6×10^{-6}
94.4	13.1	9.4	1.1×10^{-6}	1.4	87.1	8.5×10^{-6}	2.4	52.3	5.2×10^{-6}
128.3	12.9	7.0	1.3×10^{-6}	1.6	55.8	1.0×10^{-5}	2.4	38.0	6.5×10^{-6}
179.5	12.7	5.1	1.7×10^{-6}	1.5	41.9	1.4×10^{-5}	2.1	31.5	1.7×10^{-5}
224.6	11.9	4.3	2×10^{-6}	1.5	34.2	1.7×10^{-5}	1.9	27.6	3.1×10^{-5}
289.3	12.2	3.3	2.4×10^{-6}	-	-	-	1.4	28.4	1.1×10^{-4}
375.0	12.1	2.6	2.7×10^{-6}	-	-	-	0.8	41.2	4.3×10^{-4}

Table 7.1 — Analysis of the dark I-V characteristics for the n-CdTe/p-ZnTe diode

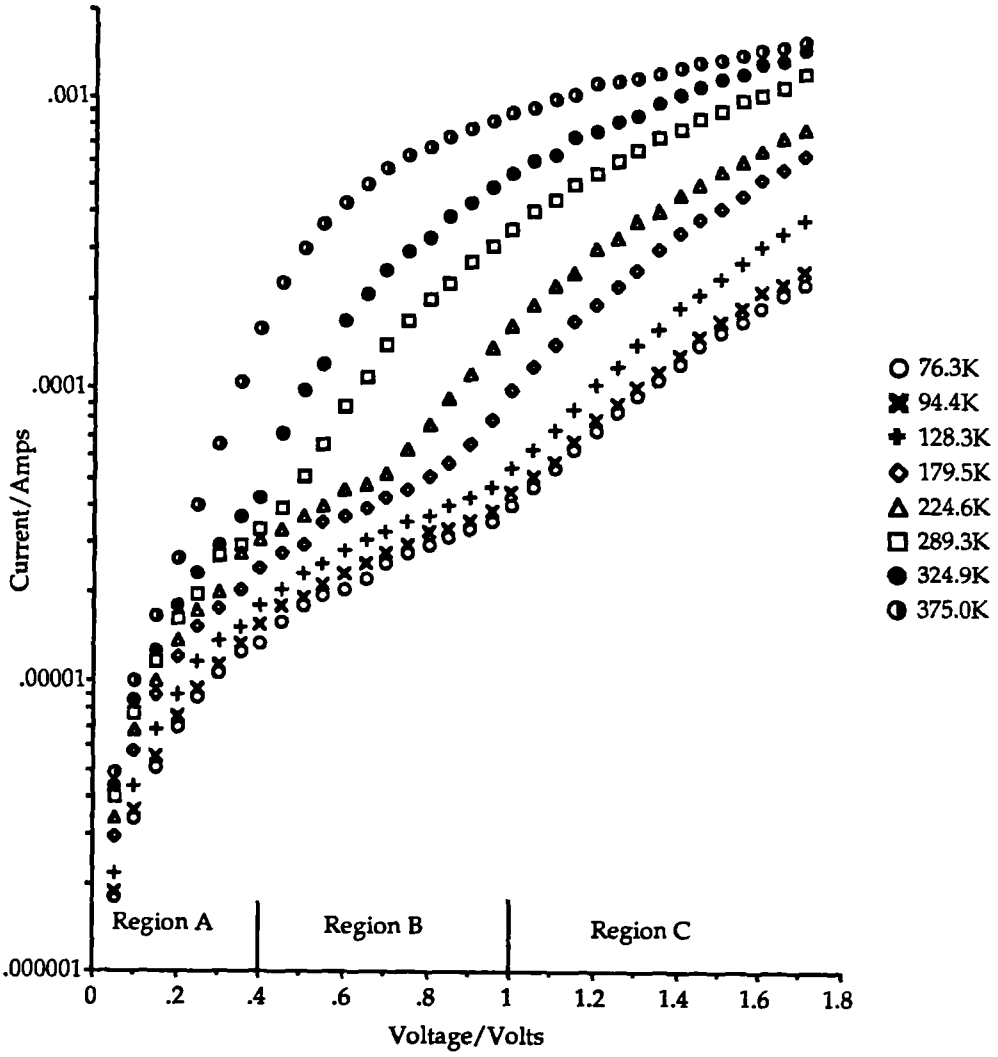

Figure 7.2 — The forward, dark I-V characteristics for the n-CdTe/p-ZnTe diode

Over the temperature range it can be seen that 3 separate regions exist, V<0.4V, 0.4<V<1.0V, and V>1.0V (described as regions A, B and C respectively). In region A the current rises sharply with a small change in voltage, whilst in region B a plateau is reached and the current appears to become saturated. As the voltage is again increased to region C, the current rises fairly sharply with voltage again. A breakdown of the values of the gradients existing within these three regions is given in table 7.1.

In the first region, A, the forward current behaves exponentially. In this voltage range the reverse characteristic (shown in figure 7.5) is very similar to that

measured in forward bias. With increasing forward bias, the forward current exhibits two distinct regions with different slopes which are relatively temperature insensitive. These curves are not well described by the usual diode equations, since the ℓn I_f vs. $\frac{1}{T}$ plots would display straight lines. It can be seen that from figure 7.3 that these plots are not linear.

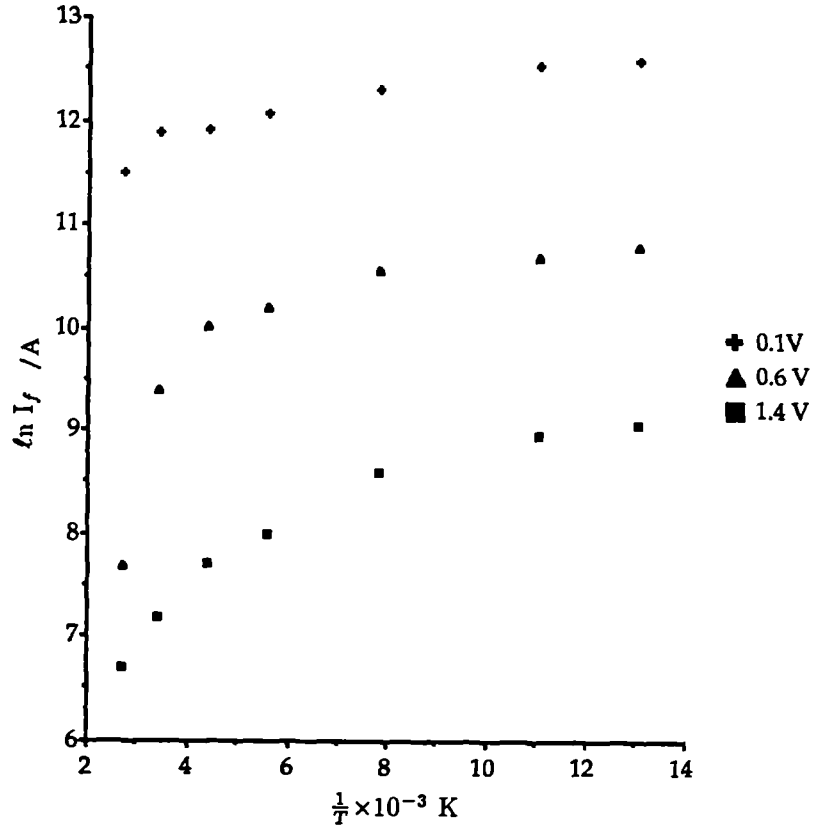

Figure 7.3 — A plot of ℓn I_f vs. $\frac{1}{T}$ for n-CdTe/pZnTe diode

The forward characteristics are better described by the tunneling expression discussed in section 6.3, equation 6.2.

$$I_f = I_o(T)\, exp\,(\,BT\,)\, exp\,(\,AV\,) \qquad [7.1]$$

giving average values of A as 12.6, 1.5, and 2.2 for regions A, B, and C respec-

tively. The values of n, from the standard diode equation are always >2 except for high voltages and high temperature values where it is suspected that thermionic emission will probably become the dominant current transport mechanism. This dual current transport mechanism has been observed by other authors [5] and is described in detail in section 2.1.1. The n-CdTe/p-ZnTe diode can be considered as having an equivalent circuit response consisting of two diodes in parallel with a shunt and series resistance. At low voltages, V< 1.0V and temperatures the I-V behaviour is dominated by one diode, where tunneling behaviour is prevalent. As the voltage is increased and at high temperatures (T>200K) the behaviour changes to a space charge recombination controlled transport mechanism described by the other diode. At low temperatures not only is tunneling important but there is also an increased series resistance. A plot of $\ell n\ I_o$, the reverse saturation current, with temperature gives a value of B as $5.3\times10^{-3}\ K^{-1}$ from figure 7.4.

	Region A	Region B	Region C
	V<0.4V	0.4<V<1.0V	V>1.0V
R	1	73	36
S/eV	0.325	4.77×10^{-3}	9.73×10^{-3}

Table 7.2 — The values of S and R from the forward I_f - V data

The value of I_o at room temperature was $2.4\times\ 10^{-6}$ A, and the device had a rectification ratio of 40 at 1.0 volt. These values indicate that the device is not very good, certainly not as good as the n-CdS/p-CdTe diode and a reason for this may be the quality of the single crystal substrate. CdS crystals were found, using double crystal x-ray rocking curve analysis, to have Full Widths at Half Maximum (FWHM) values of 55 arc secs, whereas the CdTe crystals grown in house were found to have widths of around 66 arc secs (see appendix C). The CdTe diffraction peak was split, indicating the occurrence of a grain boundary across the surface of the substrate. The presence of grain boundaries accounts for the reduced values of rectification ratios and device performance.

The measured ionised charge density, $4.0\times10^{15}cm^{-3}$ from C-V measurements (see section 7.4) was too low to support a simple tunneling mechanism across the

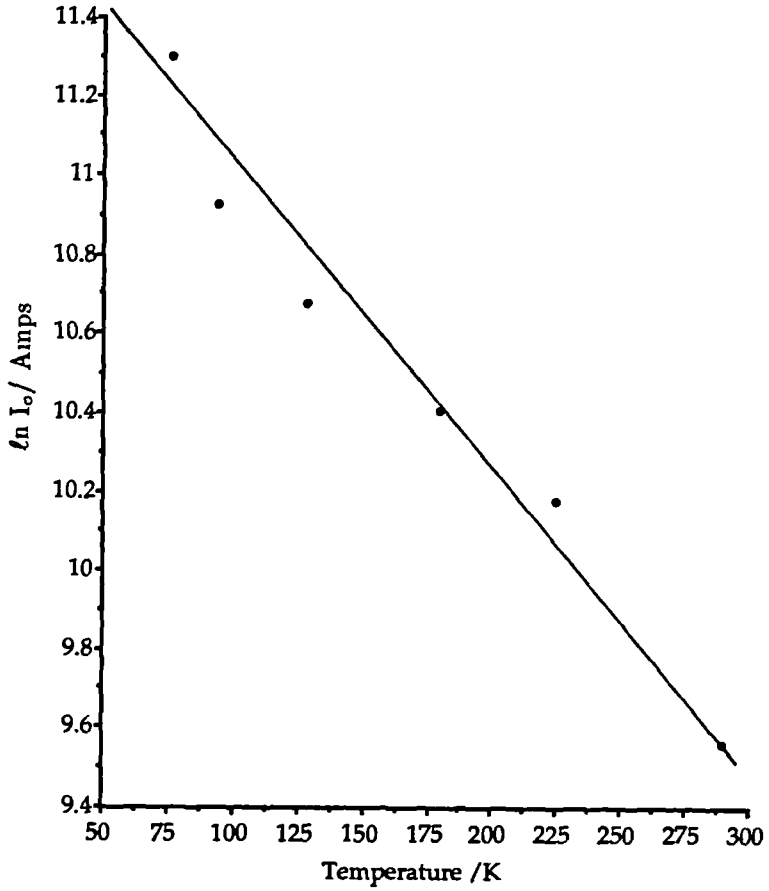

Figure 7.4 — A plot of $\ell n\ I_o$ versus temperature for the n-CdTe/p-ZnTe diode

potential barrier. Multi-step tunneling is therefore suspected to be the transport mechanism occurring. The number of tunneling steps, R, and height of each step, S, was calculated from analysis of the current transport characteristics as described in section 6.3 and these values are presented in table 7.2.

It is interesting to observe that analysis of the low voltage regions indicates a value of R to be 1 i.e. inferring a simple tunneling mechanism, however this cannot be the case since in this regime thermionic emission is prevalent. An explanation of this effect is probably due to the large inherent error as the current recorded is very small ($<10^{-6}$ A) at low voltage values. The total barrier height was calculated

for all three regions and found to be the same, 0.346eV. The diffusion voltage was estimated to be 1.38eV which agrees with the theoretical diffusion potential for this junction which was calculated to be 1.34eV. No other values have been published for this junction.

The behaviour of the reverse current can also be explained by a multi-step tunneling recombination model (see section 6.3.1). The dark reverse I_r-V characteristic for the n-CdTe/p-ZnTe diode is shown in figure 7.5. From this a graph of $\ell n\left(\frac{J_r}{V}\right)$ versus $(V_d\text{-}V)^{-\frac{1}{2}}$ should be a straight line, if multistep tunneling /recombination is the dominant current transport mechanism. The value of V_d was calculated from capacitance-voltage characteristics (see section 7.4) and was found to be 1.12 volts at room temperature. Figure 7.6 shows a plot of $\ell n\left(\frac{J_r}{V}\right)$ versus $(V_d\text{-}V)^{-\frac{1}{2}}$ and shows that the plot gives a straight line.

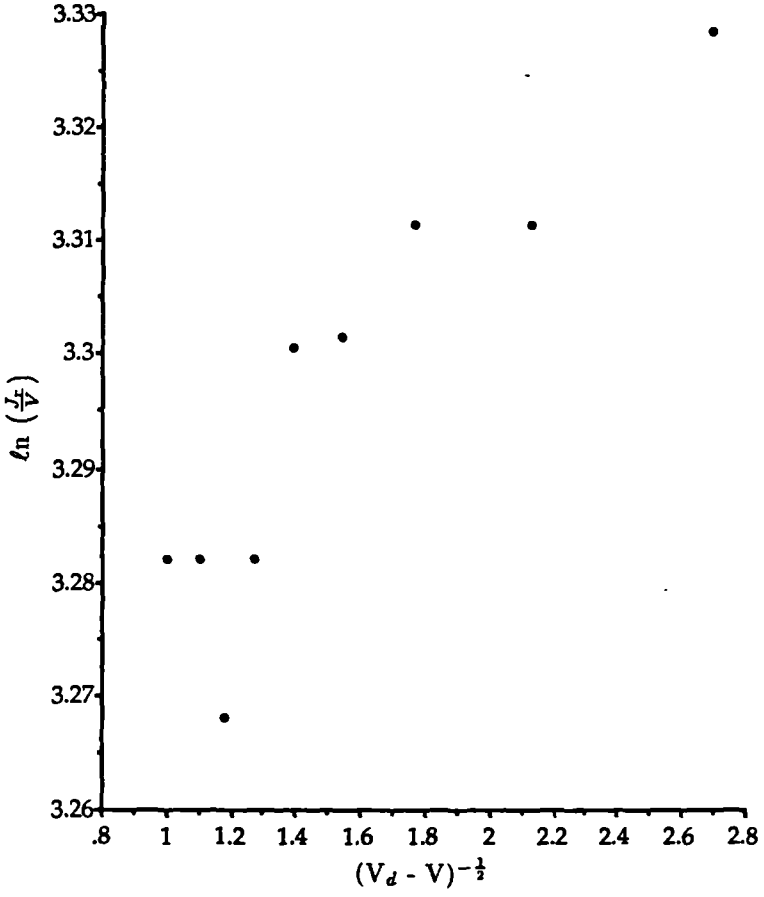

Figure 7.6 — A plot of $\ell n\left(\frac{J_R}{V}\right)$ versus $(V_d\text{-}V)^{-\frac{1}{2}}$ for the n-CdTe/p-ZnTe diode

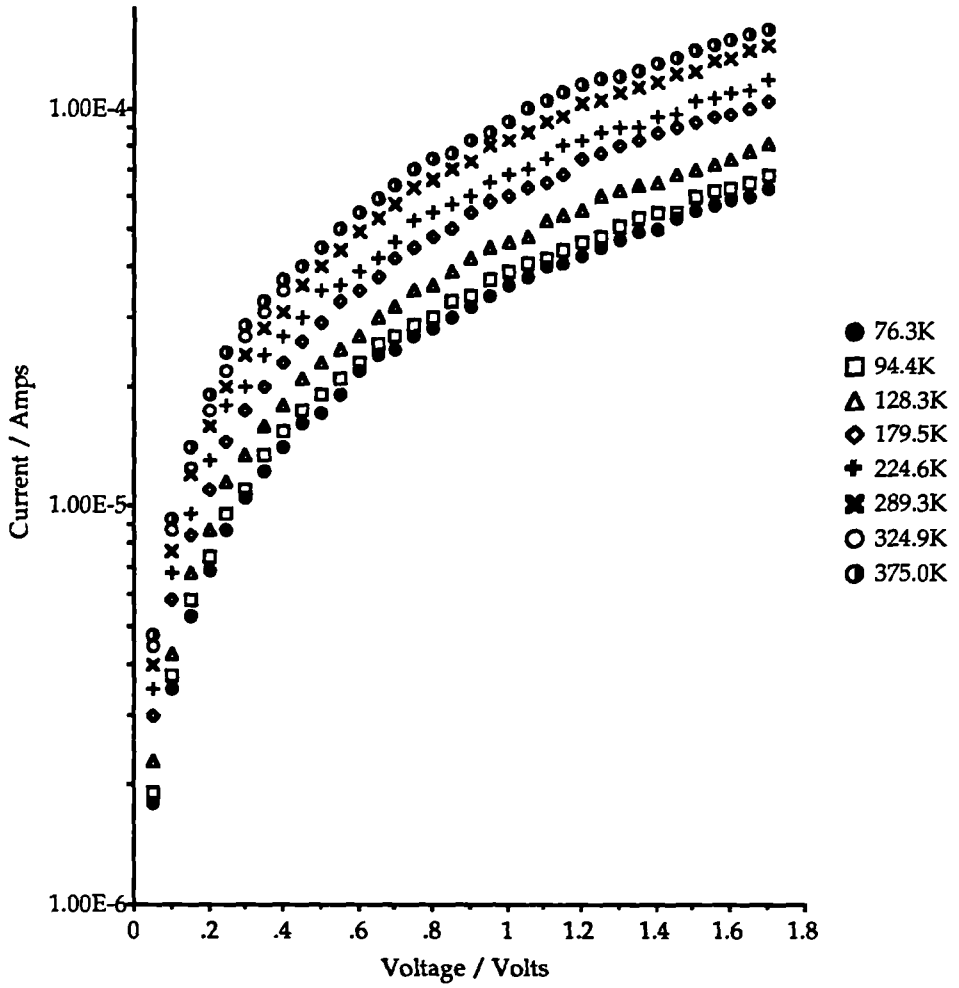

Figure 7.5 — The reverse dark I-V characteristics for the n-CdTe/p-ZnTe diode

The gradient was found to be 0.0283 $V^{\frac{1}{2}}$ and from this it is possible to calculate the values of the energy between each tunneling step. This was found to be 2×10^{-6} eV. The number of steps is given by $S_r = \left(\frac{E_g+\Delta E_v}{E_r}\right)$ and was found to be 1.25×10^{6}. This large number of steps was also found for the Cu_2S/CdS solar cells [6] and was thought to be so due to the high $\Delta E_{g,p} + \Delta E_v$ value. The trap density was calculated from

$$N_t = \frac{J\ h\ exp\ [\Gamma(V_d - V)^{\frac{1}{2}}]}{a\ q^2\ V^{-1}} \qquad [7.3]$$

where a is the lattice parameter of CdTe, V is the applied voltage and Γ is the slope of the $\ell n\left(\frac{J_r}{V}\right)$ versus $(V_d\text{-}V)^{-\frac{1}{2}}$ graph shown in figure 7.6. The value of N_t was found to be 1.23×10^9 cm^{-3}.

Assuming that the energy gap of CdTe changes linearly with temperature and E_r is constant with temperature then the gradient of the $\frac{d\ell nJ_r}{dT}$ versus $(V_d\text{-}V)^{-\frac{1}{2}}$ curve should be the same as that predicted from equation 7.4 (see section 6.3.1)

$$\frac{d\ell nJ_r}{dT} = -(V_d - V)^{\frac{1}{2}}\ \alpha\ E_r^{\frac{1}{2}}\ c \qquad [7.4]$$

From the graphs this value was found to be 0.043 $V^{\frac{1}{2}}$, whereas from equation 7.4 this value was calculated to be $1.15\times\ 10^{-5}$ $V^{\frac{1}{2}}$. It can be seen that E_r is not a constant with respect to temperature since these values would be similar. These results conform with those found for the n-CdS/p-CdTe junction where the change of the trap separation remains unaltered as the temperature is changed. Reasons for this are as yet unclear.

7.4 Capacitance - Voltage Measurements

Capacitance-voltage measurements were made on the n-CdTe/p-ZnTe junction in order to further investigate the nature of the junction. A plot of C^{-2} versus applied voltage at temperatures between 76-320 K is given in figure 7.7.

The plots yielded straight lines at high reverse bias indicating the abrupt nature of the junction. At low reverse bias the slope of the C-V line changes due to the presence of interface states at the junction. Table 7.3 shows the values of N_D-N_A, V_d and W. The depletion region at room temperature was found to be $\approx2.8\mu$m. The value of N_D-N_A was found to be 4×10^{15} cm^{-3}, which is different from that found from Hall measurements of $\approx6.7\times10^{17}$ cm^{-3}, see section 5.7.3.

The value of the depletion width changed slightly over the temperature range studied from 3.2-2.6μm from 77-321K, as would be expected due to the higher number of charge carriers at high temperatures. The values of N_D-N_A also changed

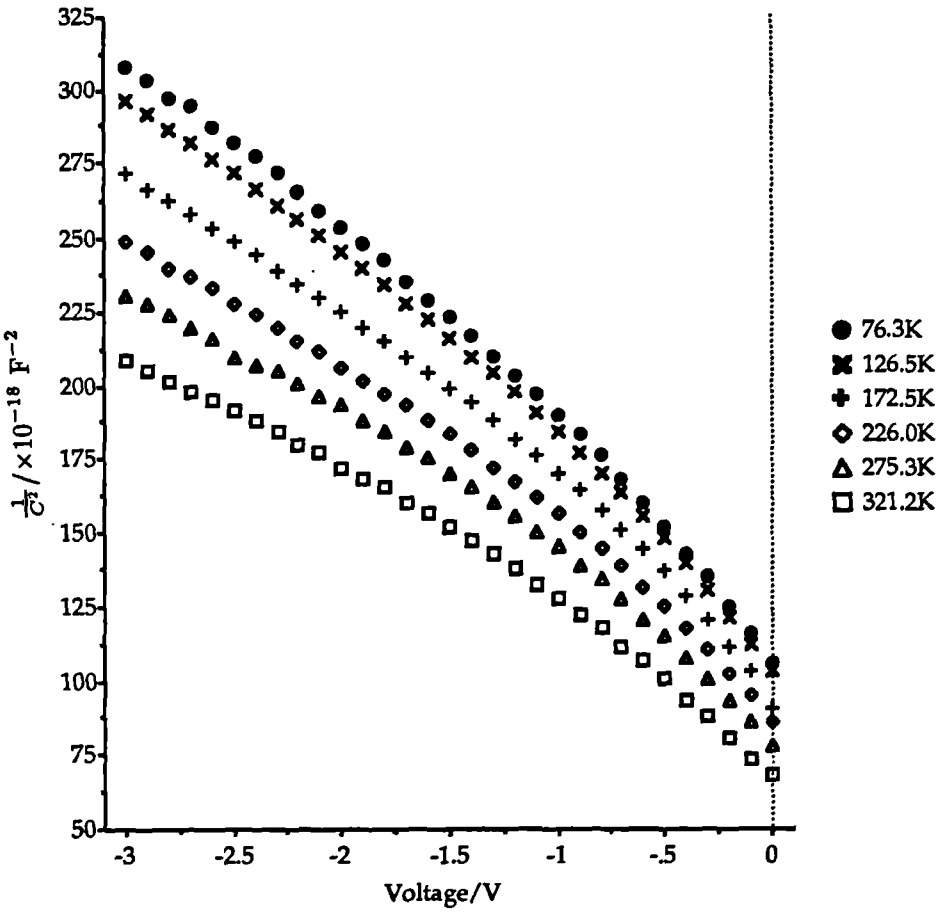

Figure 7.7 — The C^{-2} versus V curves for the n-CdTe/p-ZnTe diode at different temperatures

suggesting that the density of negatively charged levels in the depletion layer had decreased. The extrapolation of the curve at low bias gives a value of the voltage intercept as 1.12eV at 275 K. The measured diffusion potential obtained by Buch et al [2] gives V_d as 1.34eV. This value is in good agreement with that found by other authors. The rate of change of the built-in potential with temperature is not constant throughout the whole temperature range. Above room temperature the value of $\frac{dV_d}{dT}$ is given by 1.52×10^{-3} V K^{-1}. The value of $\frac{dV_d}{dT}$, from I_f - V measurements was found to be 4.2×10^{-4}V K^{-1}, for region A, 3.46×10^{-3}V K^{-1} for region B and 2.42×10^{-3}V K^{-1} for region C. Thus it can be seen that the values of $\frac{dV_d}{dT}$ are in close agreement with that found from C-V data.

Temperature	V_d/volts	N_D-N_A/cm^{-3}	W/μm
76.5	1.5	5.5×10^{15}	3.2
126.5	1.6	5.2×10^{15}	3.2
172.5	1.5	4.8×10^{15}	3.0
226.0	1.4	4.3×10^{15}	2.9
275.3	1.1	4.1×10^{15}	2.8
321.1	1.0	3.7×10^{15}	2.6

Table 7.3 — The analysis of the C-V data for the n-CdTe/p-ZnTe diode

7.5 Spectral Response

The spectral response of quantum efficiency of the n-CdTe/p-ZnTe junction, normalised to constant photon density, on illumination through the ZnTe window layer is given in figure 7.8. It can be seen that the short and long wavelength cut-offs agree well with the band gaps of ZnTe and CdTe respectively.

At zero bias the value of h(v) (described in section 6.5) was found to be 0.67 from the spectral response data. It can be seen that the maximum spectral sensitivity corresponded to an energy of 1.8 eV. The smooth form of the curve indicates the absorption of carriers at many wavelengths, possibly due to the formation of $Cd_{1-x}Zn_xTe$ at the interfaces of these two materials. The curves only indicate the presence of one broad peak corresponding to the absorption of light across the band gap of CdTe. The spectral distribution of V_{oc} and I_{sc} for this cell showed that the largest response occurred in the vicinity of the band gap of the CdTe and there was a relatively small broad response centered around the band gap of ZnTe. There is no evidence of any minor peaks from defect states or doping effects, as observed with the CdS - Cu_2S solar cell [7].

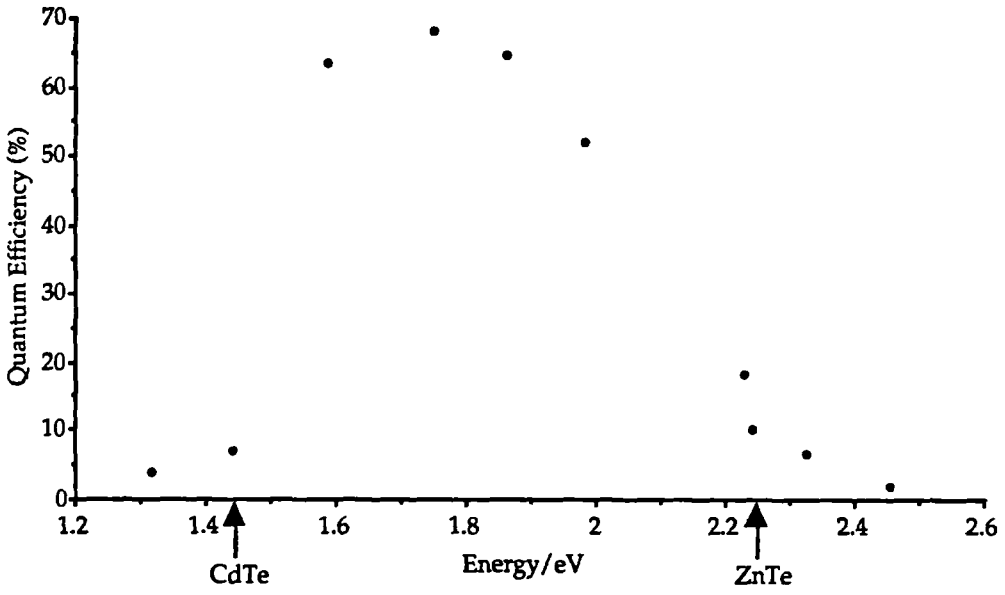

Figure 7.8 — The spectral response curve of the n-CdTe/p-ZnTe diode

7.6 Photocapacitance Studies

The photocapacitance of the n-CdTe/p-ZnTe diode was measured at 171.2 K over the energy range 0.6-2.8 eV and the response is plotted in figure 7.9.

It can be seen that the capacitance remains unchanged until 1.18eV, at which point it starts to rise until it peaks at 1.7 eV and then begins to drop off again at energies >1.7 eV. At 2.6 eV the capacitance again becomes steady. At 171.2 K the band gap of CdTe is 1.527 eV. The threshold occuring at 1.18 eV is not clear, but indicates the transition of electrons from filled levels to the conduction band.This level is either a deep level in the p-ZnTe, which would seem unlikely due to the high conductivity or implies the presence of a level with an energy of 0.35 eV below the conduction band of the CdTe. Several authors [8,9,10] have observed the presence of levels lying at energies of 0.22, 0.28 and 0.35 eV below the conduction band of n type CdTe. The other levels at 0.22 and 0.28 eV may have been difficult to observe since their presence is swamped by the strong CdTe band edge absorption at 1.53 eV. The sensitivity of the photocapacitance technique renders it a technique for observing shallow to middle gap trapping centers, with the possibility of viewing

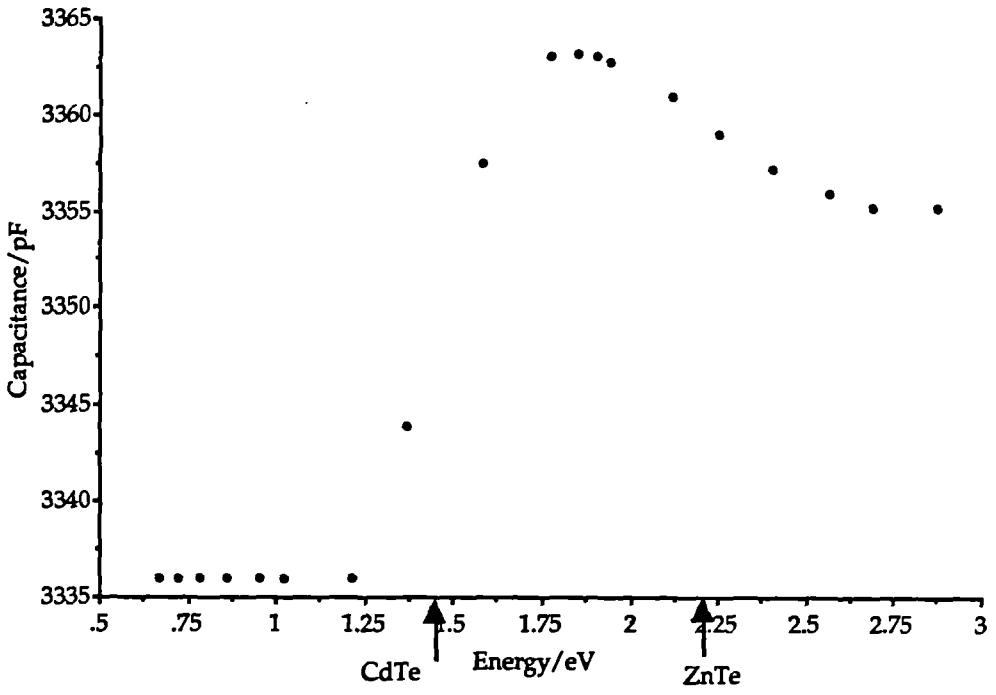

Figure 7.9 — The photocapacitance spectra of the n-CdTe/p-ZnTe diode

very shallow or deep centers unlikely.

The negative threshold at 1.9 eV is attributed to a level lying 0.36 eV below the conduction band of the ZnTe. In general, photoluminescence (PL) studies of As-doped ZnTe show that an acceptor level occurs at 80 meV below the conduction band edge of p-ZnTe [11]. Doping with arsenic thus produces a shallow acceptor, which would be difficult to detect in the photocapacitance spectrum. It is however possible that the arsenic becomes an interstitial anion species due to the high overpressure during the growth of the ZnTe (see section 5.7.3). This would lead to a deep acceptor in the range 0.3-1.0 eV as observed by Henry et al [12] in other II-VI compounds. Group V elements are known to be slow diffusers, and thus desirable to achieve impurity controlled p-type doping of II-VI compounds [13]. Berding et al [14] found that the energy of formation of an As atom on a Te site was 1.87 eV, and is therefore quite easy to form, no studies have however been conducted on interstitial As atoms.

Diode Characteristics			
V_{oc} = 0.61V		$I_o = 2.4\times10^{-6}$A	
J_{sc} 16.3 mAcm^{-2}		B = 5.3×10^{-3}K^{-1}	
ff = 32%		$N_t = 1.23\times10^{9}$ cm^{-3}	
η = 3.7%		Rectification Ratio 40 : 1 at 1.0V	
Current-transport characteristics			
Forward bias			
Parameter	Voltage Region		
	V< 0.4V	0.4V<V<1.0V	V>1.0V
A(V^{-1})	12.6	1.5	2.2
n	$\geq$2	$\geq$2	$\geq$2
$\frac{dV_d}{dT}$ (VK^{-1})	4.2×10^{-4}	3.5×10^{-3}	2.4×10^{-3}
R	1	73	36
S(eV)	0.345	4.8×10^{-3}	9.7×10^{-3}
R.S(eV)	0.345	0.346	0.346
Reverse bias			
$S_r = 1.25\times10^{6}$			
$E_r = 2.0\times10^{-6}$ eV			
$\frac{dlnJ_r}{dT} = 1.15\times10^{-5}$ VK^{-1}			
Capacitance - voltage characteristics			
N_D - $N_A = 4\times10^{15}$ cm^{-3}			
V_d = 1.12 eV			
W = 2.77μm			
$\frac{dV_d}{dT} = 1.52\times10^{-3}$ VK^{-1}			

Table 7.4 — A summary of the n-CdTe/p-ZnTe diode characteristics

7.7 Discussion

The emphasis in this chapter has been the fabrication and characterisation of an n-CdTe/p-ZnTe solar cell grown by MOVPE. Until now there have only been

two such reports of heterojunctions being fabricated for use as solar cells [2,3] and their device characteristics have not been fully explored. Table 7.4 gives a summary of the device characteristics observed for an n-CdTe/p-ZnTe diode prepared on conducting n-type {001} single crystal CdTe grown in this laboratory. The actual n-CdTe/p-ZnTe solar cell parameters are summarised in table 7.5, along with a comparison of the results obtained by other authors [2,3]. The cells produced by Buch et al [2] gave very low efficiences and this was due in the main to the highly resistive CdTe layers ($\rho \approx 10^7\ \Omega cm^{-3}$) used in the junction. The cells produced by Razykov et al [3] had high rectification ratios of $\approx 10^4$ at 2 volts, but were found to have fairly low J_{sc} values of 10-12 $mAcm^{-2}$, limiting their overall efficiency.

The current transport data confirms the presence of a multistep tunneling/ recombination mechanism occurring within the device. At high voltages and temperatures this mechanism is superseded by an emission mechanism. All the cells reported had high reverse saturation current, several orders of magnitude larger than expected for a recombination current transport mechanism. Thus more direct current paths must control the current transport mechanism including tunneling and thermal activation. From the characteristics of the junction a band diagram of the n-CdTe/p-ZnTe diode is shown in figure 7.10.

It can be seen that the holes tunnel from the valence band of the ZnTe into interface states, where they recombine with electrons from the conduction band of the CdTe that have previously tunnelled into these interface states. The motion of electrons is obstructed because of the large barrier of 0.77 eV in the conduction band as compared with the barrier of 0.02 eV in the valence band for the motion of holes. This barrier implies that emission would only occur at high voltages and temperatures, and thus tunneling into interface states appears the likely transport mechanism. Capacitance measurements indicate the wide nature of the junction 2.8μm at room temperature, compared with 2.99μm found by Buch et al [2]. Since $N_D > N_A$ most of the depletion region occurs within the ZnTe as shown in the diagram. Analysis of the I-V data confirmed that at moderate temperatures the current transport was dominated by interfaces at the junction, the number of tunneling states being very high indicating an inherently large density of interface states, as would be expected from a system with a lattice mismatch of 5.8%.

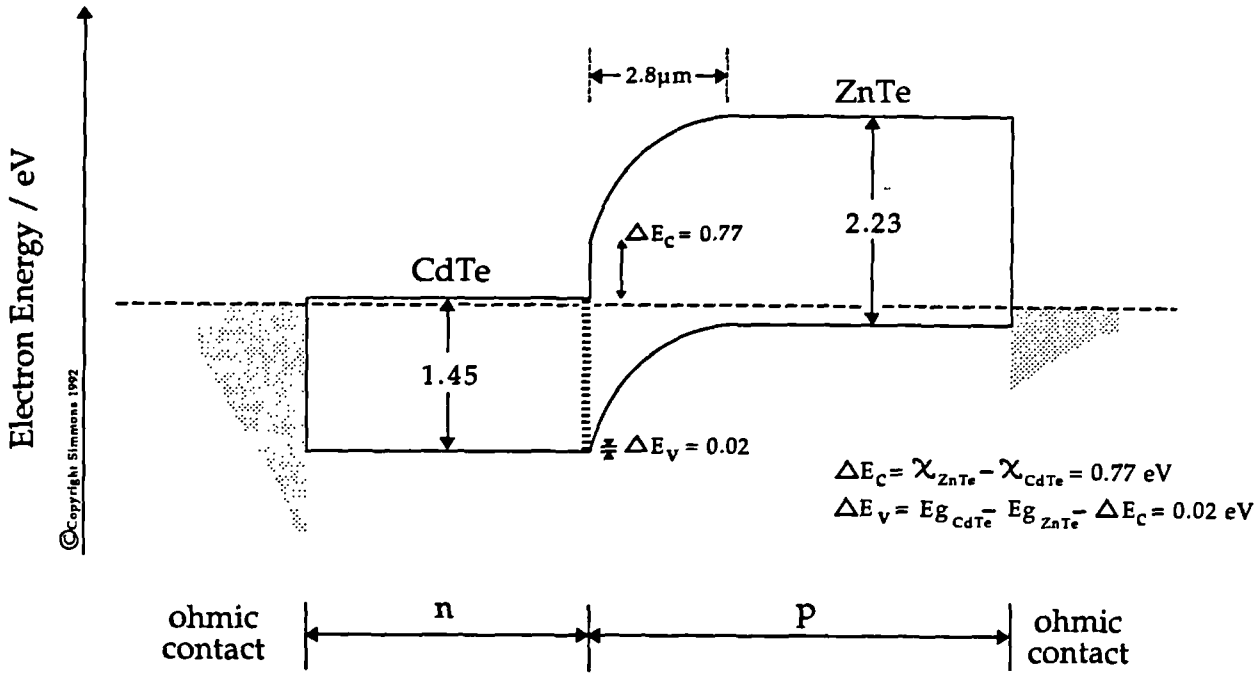

Figure 7.10 — The expected band structure diagram of the n-CdTe/p-ZnTe solar cell

The presence of defects in the substrate is particularly undesirable for epitaxy, since many of them can propagate into the growing layer with deleterious effects on device properties. The presence of twins is known to be a problem in the growth of boules of single crystal CdTe grown at Durham [15], and isolated dislocations and twins have been observed within the substrate material used (see chapter 4). Bulk grown crystals of CdTe have been shown to contain an unacceptably large defect concentration (e.g dislocations, sub-grain boundaries, precipitates and twins [15]) that result in epitaxial films of poor structural quality [16]. Single crystal CdTe is also mechanically very brittle and therefore difficult to work with.

As with all substrates used for MOVPE, the CdTe is exposed to a heat treatment of annealing in hydrogen at 410°C for 10 minutes, as recommended by Werthen et al [17]. Such a heat treatment has been shown to produce a decrease in carrier concentration near the surface and it is thought that this is caused by

the creation and in-diffusion of Cd vacancies at the surface, due to the different rates of evaporation of Cd and Te from CdTe [8-10]. As an acceptor species, when ionised the Cd vacancies can compensate donor impurities within the material. Heat treatments can improve the electronic properties of CdTe, however some heat treatments induce these native defects due to the deviation from stoichiometry. These native defects can either act as trap levels or recombination centres, which have a serious effect on the electronic properties. In addition, atoms near the surface interact strongly with the atmosphere, they may evaporate, migrate or precipitate during heat treatment. As a result the characteristics of electrical contacts of metal-CdTe may be seriously affected by annealing, whilst the electronic properties of the bulk can be improved.

Author	Technique	$\eta(\%)$	V_{oc}/V	$J_{sc}/mAcm^{-2}$	ff	V_d/V	n
F. Buch [2]	CVST	0.02	0.6	0.32	0.37	1.34	2.04
T.M. Razykov [3]	CVD	9.7	0.81	10-12	-	0.8	1.0
M.Y. Simmons	MOVPE	3.7	0.61	16.3	0.32	1.1	>2

Table 7.5 — Comparison of device characteristics for the n-CdTe/p-ZnTe diode

DLTS characterisation [8] of electron trap levels found in n-type CdTe crystals, subjected to a heat treatment at 400°C for 1 hour revealed the presence of levels at 0.22, 0.28, and 0.34 eV. In general, the concentration of trap levels was found to be reduced by the annealing. At temperatures above 350°C some defects were induced, which compensated the donors and reduced the concentration of trap levels near the surface. These defects could be Cd vacancies or Te interstitials. Isett et al [10] observed 5 levels in n-CdTe at 0.22, 0.37, 0.52, 0.62 and 0.85 eV. The level at 0.85 eV was found to increase with heat treatment where Cd vacancies thought to be responsible are produced by two mechanisms, the evaporation/condensation of Cd and the formation of oxide species. Cd vacancies are thought to be a highly mobile species [16] so that vacancies can easily penetrate into the bulk. The use of a pure hydrogen ambient during the anneal implies that the CdTe will try to provide the minimum Cd pressure required for its own phase stability. The loss of

Cd from the substrate results in the diffusion of Cd vacancies into the substrate. Other defects generated by the anneal are known to form deep levels in the energy gap of the semiconductor [19], at values between 0.7-0.8 eV below the conduction band edge [11].

Photocapacitance studies revealed the presence of a level at 1.18 eV above the valence band of the CdTe and this is thought to be due to the Cd vacancies described above. The presence of deep levels could not be detected using the photocapacitance technique since this would predict levels occuring at ≈0.6 eV, i.e at the limit of the techniques resolution. The presence of interface states is however observed in the curvature of the C-V data, causing a deviation from linearity as the levels are emptied. The C-V data agrees well with that obtained by Buch et al [2] and it gives a value of $\frac{dV_d}{dT}$ that is in close agreement with that observed from the forward I-V data.

Detailed current transport data has revealed the total number of tunneling steps required to surmount the barrier to current flow in forward bias ranged from 1-73 depending on the voltage, with the height of each step varying between 0.345-9.7×10^{-3} eV respectively. The total barrier height was found to be the same at 0.346 eV for all voltage regions. The barrier height in reverse bias was found to be much higher ≈2 eV as would be expected. It is surprising however that with such a large difference in the barrier heights for forward and reverse bias that the rectification ratio was not higher. This can only be accounted for by the low shunt resistance providing parallel paths for the current flow, possibly providing a current leakage path in reverse bias.

7.8 References

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Chapter VIII

The p-i-n Solar Cell Grown by MOVPE

8.1 Introduction

This chapter describes the fabrication and characterisation of different p-i-n solar cell structures based on CdTe as the intrinsic absorber layer. The incorporation of another layer into the more familiar p-n heterojunction to form a p-i-n heterostructure helps distribute the electric field over the entire thickness of the light absorbing i-CdTe layer, thus enabling drift collection of photogenerated carriers. The p-i-n design also overcomes the primary limitation encountered in the conventional CdTe heterojunction design i.e. difficulty in producing stable, low resistance back contacts, by replacing the back contact with a rectifying junction [1]. In practice CdTe p-i-n solar cells have been shown to be stable over 3000 hours of simulated solar illumination [2]. In order to realise even higher efficiencies tandem cell designs have been proposed in which a wide bandgap cell is stacked over a narrow bandgap cell [3]. The optimum band gap of the top cell is 1.7eV and that of the bottom cell is 1.1eV for a two cell arrangement. Alloys of CdTe (eg CdZnTe and CdMnTe) have been suggested as suitable materials for top cell applications [4].

Meyers [1] found that in order to produce high quality thin film CdTe, a heat treatment was required to anneal out any electrically active defects. But this same heat treatment has been shown to change the effective carrier concentration and even the dominant carrier type of the film [5]. This would account for the absence of high efficiencies in CdTe homojunction cells and suggests that thin film CdTe may be most appropriate when used in conjunction with other materials. It can, however also account for the reduction in efficiency found in CdTe heterojunctions, since improvements in crystallinity at junction interfaces require heat treatments which degrade the conductivity of the CdTe. Meyers found that highest efficiency cells were constructed of high resistivity CdTe, presumably because this was also

the highest quality CdTe. One attribute of CdTe is its ability to be produced as either n or p-type; however, its tendency to self compensation may be a contributory factor in the absence of high efficiencies.

Metal-insulator-semiconductor (M-I-S) devices incorporating an i-CdTe absorbing layer and a Ni contact metal were found to produce cells of 8.6% efficiency [6], however problems with limited built-in voltages (due to interface states) and reduced optical transmission (due to the slightly opaque Ni layer) meant that any further improvement in efficiency would be difficult. The p-i-n solar device was thus considered as a novel alternative with several potential advantages over the single heterojunction and M-I-S devices.

One of the advantages of the i-CdTe based p-i-n cell design is that different n type substrates can be incorporated to reduce the lattice mismatch at this n-substrate/i-CdTe junction, and thus reduce the density of interfacial misfit dislocations. The choice of n-type substrate is also restricted to materials that offer no spikes in the conduction or valence band of the heterojunction formed. The n-type substrates used in this thesis were {0001}CdS, {100}GaAs and {111}CdTe. CdS was considered because it naturally follows on from the p-n junction work described in chapter 6, epitaxial growth is known and it has no spikes in either the conduction or the valence bands. The system does however have a very large mismatch between $\{0001\}_{CdS}\|\{111\}_{CdTe}$ of $\approx 9.7\%$ which is undesirable for epitaxial growth and CdS is a relatively poor quality substrate. GaAs on the other hand is a high quality substrate which is readily available and relatively inexpensive. Again CdTe epitaxial growth is well known despite the large mismatch of 14.7%. The CdTe/GaAs system does, however, have 0.22 eV conduction and valence band spikes which may affect the device properties. The obvious choice for lattice matching conditions is CdTe since this would offer no conduction band spikes or mismatch and the homoepitaxial growth is well documented. Problems do exist however with expensive, relatively poor quality substrate material that is prone to contain defects such as twins. These three substrates were thus adopted into the p-i-n structures which were fabricated and analysed.

Finally in order to overcome the problem of mismatch and to improve absorption at all wavelengths it was decided to try and grade the intrinsic layer. Good

quality crystallinity is not generally obtainable if the heterojunction is a highly mismatched system (see section 2.1.4). In such cases, large densities of misfit dislocations are generated and these defects severely degrade the electronic properties of the solar cell. In the case of p-ZnTe/i-CdTe/n-CdTe, the grading from CdTe to ZnTe provides a changing template for the in-plane lattice, preparing for the ZnTe growth, thus minimising the generation of misfit dislocations. The effects of grading the intrinsic layer on the properties of the devices formed are then discussed.

8.2 The n-CdS/i-CdTe/p-ZnTe Solar Cell

8.2.1 Introduction

The p-i-n cell proposed by Meyers [1] addresses the two inherent problems in the n-CdS/p-CdTe cell of making highly conducting p-type CdTe, which is notoriously self compensating and of making good ohmic contacts to CdTe, which has an electron work function of 5.95eV [7]. The design of this new structure had several properties that made it almost ideal as a solar convertor. The CdS is always n-type, whereas ZnTe is generally p-type and CdTe notoriously self compensating and thus highly resistive. There are no spikes at the n-i and i-p interfaces which could inhibit the collection of photogenerated electrons and holes respectively. Finally at each interface there is a step which prevents collection of the unwanted charge carriers arising from reflections. These features are demonstrated in an idealised band diagram of this structure in figure 8.1.

The p-i-n device has now been grown by a number of laboratories in thin film polycrystalline form [8,9] with reported small area efficiencies of up to $\approx 10\%$. This section describes the fabrication of single crystal ZnTe/CdTe/CdS solar cells by MOVPE, which would, it was hoped, offer higher efficiencies than their single heterojunction counterparts and also allow the limiting aspects of the polycrystalline device performances to be investigated.

This section demonstrates the fabrication of p-i-n structures based on {0001} CdS n-type substrates. The epitaxial growth of CdTe onto {0001}CdS by MOVPE

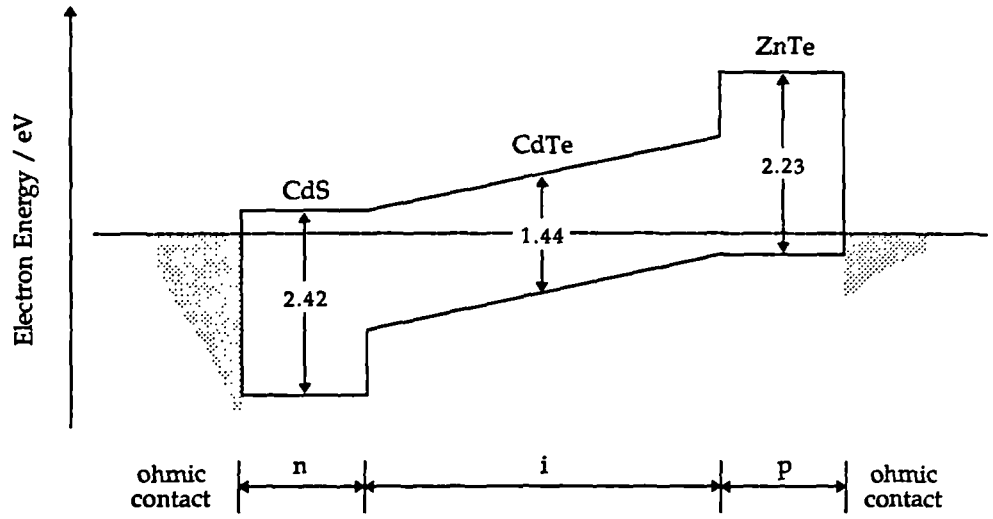

Figure 8.1 — The idealised band structure diagram of the n-CdS/i-CdTe/p-ZnTe solar cell

has been discussed in chapter 6. An undoped p-type ZnTe window layer was then grown onto a n-CdS/-CdTe heterojunction and the electrical properties and epi-layer microstructure investigated [11,12]. Finally doped p-i-n structures were fabricated in-situ in the MOVPE reactor in order to observe the effects p-type doping has on the device properties, and to investigate the current transport mechanisms and interfacial recombination in the absence of polycrystalline grain boundaries. These results were then compared with those obtained for the single crystal n-CdS/p-CdTe device.

8.2.2 Experimental

Intrinsic {0001} oriented CdS mechanically polished layers supplied by Eagle-Picher with resistivities in the region of 5-8 Ωcm were used as substrate material. The polarity of the CdS surfaces had been identified by the supplier. The oriented CdS wafers were initially boiled in C_2HCl_3 for 10 minutes to degrease the substrate surface. They were polished in a mixture of 4.8g CrO_3, 9.1g HNO_3 (70%) and 50ml of deionised water at 30°C for ten minutes as prescribed by Zhuk et al [13]. The reaction was quenched by rinsing the substrates in deionised water for 30 minutes.

The substrates were then loaded into the MOVPE reactor and given a heat clean at 410°C for ten minutes under hydrogen. The CdTe ($\approx 1\mu$m) and ZnTe ($\approx 0.6\mu$m) epitaxial layers were grown at 325°C on both (0001)Cd and (000$\bar{1}$)S faces of the CdS with a total flow rate of 7000 SCCM. Initially structures were grown with a highly resistive (10^3 Ωcm) p-ZnTe layer due to difficulties encountered with the production of high conductivity p-ZnTe. Following the success of doping experiments with elemental arsenic (see section 5.7) subsequent devices were fabricated with a highly conductive (2-10 Ωcm) p-ZnTe layer. Au and In point contacts were evaporated onto the ZnTe and CdS surfaces respectively for device fabrication.

8.2.3 Diode Characteristics

The epitaxial ZnTe/CdTe layers on the (000$\bar{1}$)B CdS surface were characterised by a smooth, flat morphology. The crystallinity of the CdTe and ZnTe layers were excellent as illustrated by the RHEED pattern in figure 5.23. Pairing of the spots however, revealed that the epilayer was twinned as expected from results achieved earlier with the epitaxial growth of CdTe onto (000$\bar{1}$)B CdS [11]. The slight streaking of the spots along a direction perpendicular to the shadow edge confirmed the flat surface morphology. Layers of CdTe/ZnTe on (0001)A CdS were highly facetted, having a polycrystalline structure as evidenced by RHEED. Growth on the S face was thus found to give superior crystallinity and was therefore adopted for device fabrication.

Typical photovoltaic output characteristics from an undoped epitaxial p-ZnTe/ i-CdTe/n-CdS device at 25°C under AM1.5 illumination through the ZnTe are shown in figure 8.2. The overall efficiency was low due to the high series resistance and contact resistance losses of the cells. These led to low values of the fill factor (≈ 0.33) and the short circuit current (6.3 mAcm^{-2}) and were predominantly the direct result of the high resistivity of the p-ZnTe layers.

The room temperature photovoltaic output characteristics for an As-doped ZnTe p-i-n device is shown in figure 8.3. The junction area was taken to be the area of the top contact. The device structure gave a relatively high *notional* device efficiency, (η) of 14.9%, mainly due to the high short circuit current 107 mA leading

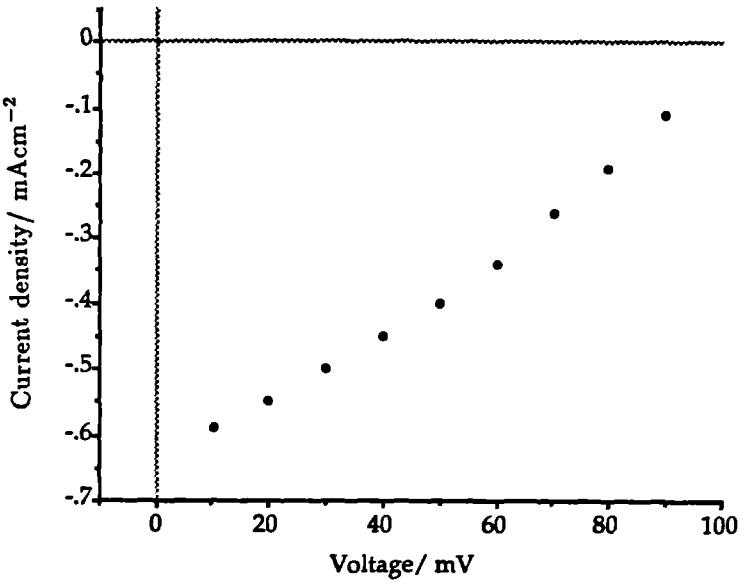

Figure 8.2 — Photovoltaic output characteristics for an undoped p-i-n device under AM1.5 illumination

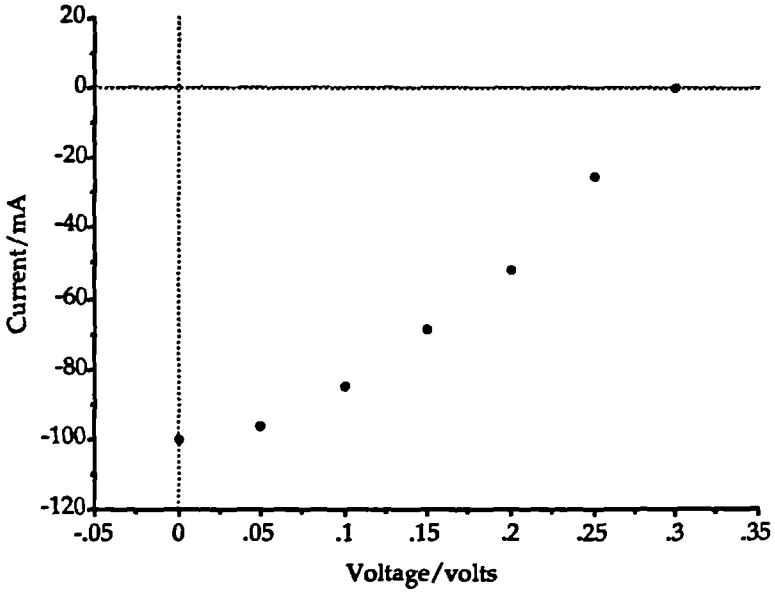

Figure 8.3 — Photovoltaic output characteristics for a doped p-i-n device under AM1.5 illumination

to a current density of 136 mAcm^{-2}. The value of J_{sc} is unrealistically high as with those found for the n-CdS/p-CdTe cells (see section 6.2) since the junction area is

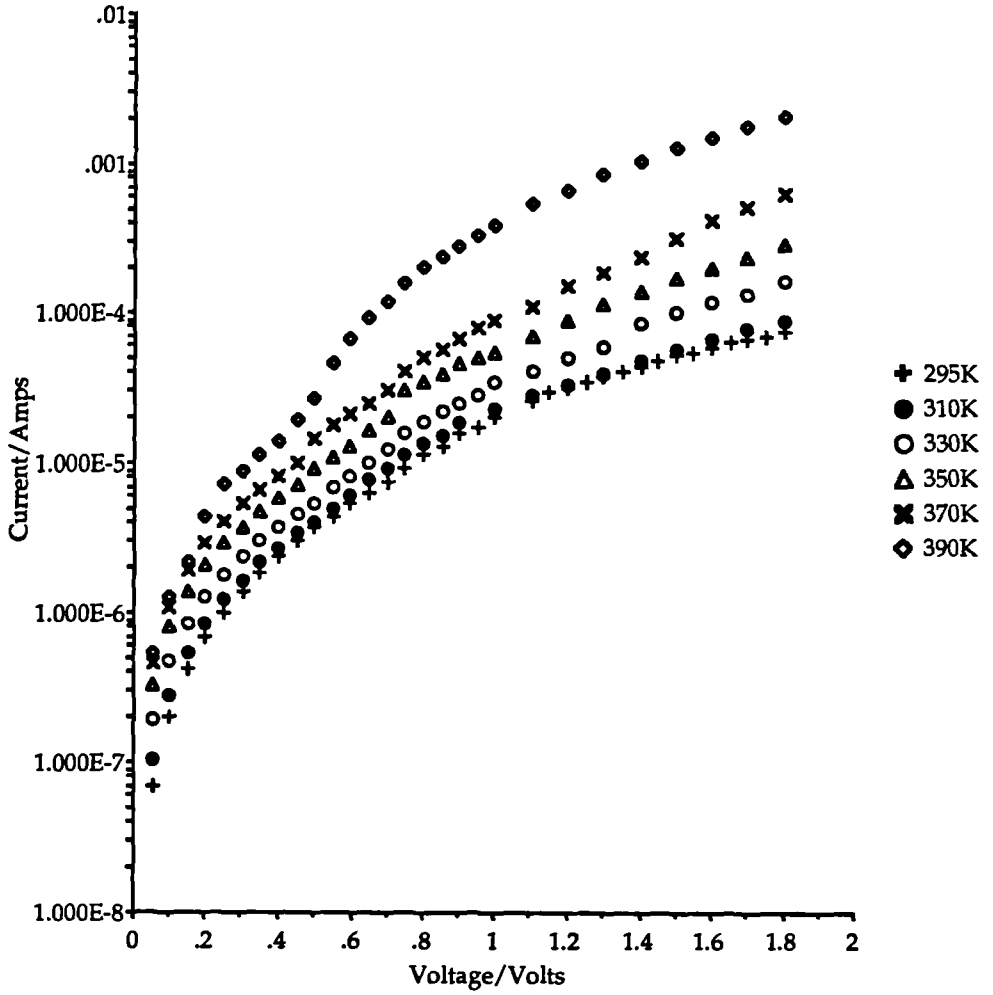

Figure 8.4 — The dark forward I_f - V characteristics for an undoped p-i-n diode

much larger than the contact area. A more realistic value of J_{sc} was recalculated from the spectral response data and found to be 24.2 $mAcm^{-2}$, leading to a device efficiency of 3.2%. The open circuit voltage of 0.37 and fill factor of 0.31, are paradoxically low for reasons that are not yet clear. It could be due to the fact that the CdTe layer thickness (1.5μm) was larger than the depletion width. The addition of the arsenic dopant has increased both the open circuit voltage from 0.1 to 0.37 V and the short circuit current from 6.3 to 24.2 $mAcm^{-2}$, increasing the

efficiency of the device. The fill factor was very similar for these two devices and is characteristically low, probably due to high contact resistances.

The forward and reverse current-voltage characteristics of the undoped structure for a range of temperatures between 290-400 K are given in figures 8.4 and 8.5 respectively. Rectification ratios were typically 50:1 at 0.9V bias. It can be seen that over the temperature range considered, there are three separate regions $V \leq 0.3V$, $0.3V \leq V \leq 1.0V$, and $V \geq 1.0V$ described as regions A, B and C respectively. In region A the current behaves exponentially and then rises sharply with a small change in voltage (over a broad range of forward current 10^{-6}-10^{-4} A) and beyond that ($I_f \geq 10^{-4}$ A) the curve deviates from this behaviour and rises less steeply. A breakdown of the gradients existing within these three regions is given in table 8.1.

Temperature/K	Region A			Region B			Region C		
	A	n	I_o/A	A	n	I_o/A	A	n	I_o/A
295.0	21.9	1.8	2.7×10^{-8}	3.9	10.0	4.8×10^{-7}	1.42	27.7	6.3×10^{-6}
330.0	20.6	1.7	9.5×10^{-8}	4.0	8.9	7.4×10^{-7}	1.6	22.0	4.3×10^{-6}
350.0	13.9	2.4	1.7×10^{-7}	4.0	8.2	1.2×10^{-6}	2.0	16.5	7.0×10^{-6}
370.0	14.7	2.1	2.5×10^{-7}	4.2	7.5	1.7×10^{-6}	9.4	3.3	6.8×10^{-6}
390.0	16.1	1.9	3.0×10^{-7}	-	-	2.5×10^{-6}	-	-	-

Table 8.1 — Analysis of the dark I-V characteristics for an undoped p-ZnTe/i-CdTe/n-CdS diode

In region A it can be seen that the forward current followed the normal diode equation with a value of n of 1.98±0.34 (i.e with an error of 17%). As the voltage is increased the forward current exhibits two distinguishable regions. The slopes of the forward $\ell n(I_f)$ - V characteristics in region B, were found to be constant for different temperatures. The deviation from this at high current levels was attributed to the high series resistance losses in the CdTe and the ZnTe. This became more pronounced as the temperature was lowered. In region B the current-voltage characteristics are not well described by the usual diode relation since this

would predict slopes of $\ell n\ I_f$ - V that varied with temperature. A plot of $\ell n\ I_o$, where I_o is the extrapolated intercept on the current axis with temperature is given in figure 8.6, describing a tunneling behaviour. A value for B was estimated from the slope to be 0.016 K^{-1}. No other values for this heterojunction have been published, but in general, values of B for similar II-VI junctions are in the region of 0.01- 0.08 K^{-1} [14].

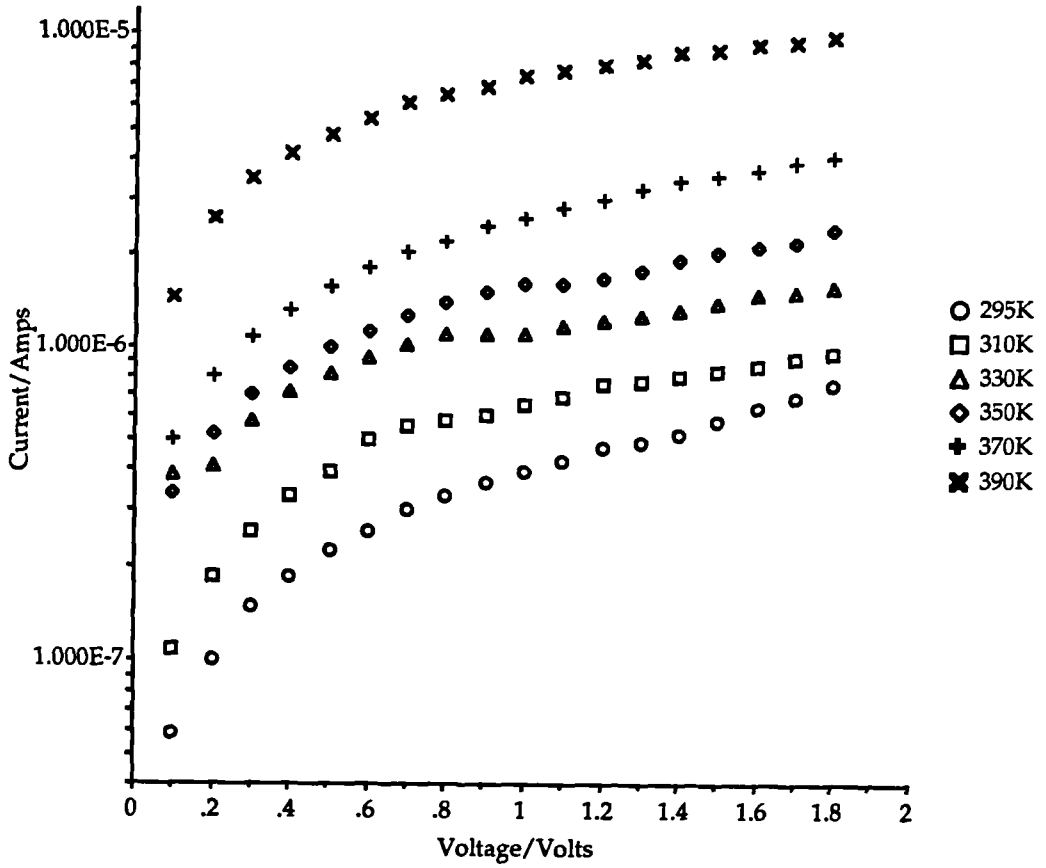

Figure 8.5 — The dark reverse I_r - V characteristics for an undoped p-i-n diode

The forward and reverse dark current voltage characteristics for the As-doped structure are given in figures 8.7 and 8.8 respectively, between temperatures of 82-300 K. The results clearly show that as the temperature is raised to between 200-291 K the current-transport mechanism changes from one type to another, see table 8.2.

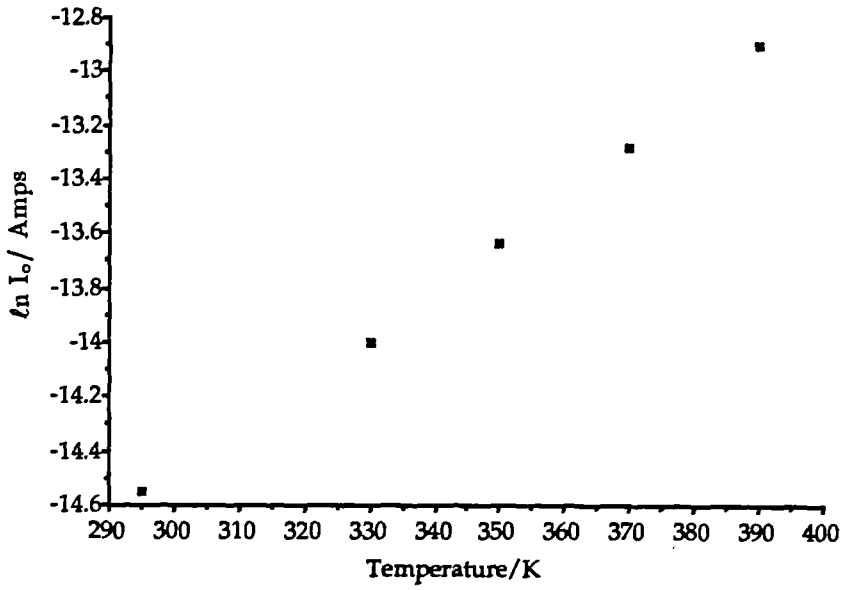

Figure 8.6 — A plot of ℓn I_o versus temperature

Temperature/K	Region A			Region B		
	A	n	I_o/A	A	n	I_o/A
82	-	-	-	2.8	50.3	1.15×10^{-10}
150.0	-	-	-	2.4	32.2	3.2×10^{-9}
200.0	-	-	-	2.2	26.4	1.7×10^{-8}
249.0	36.2	1.3	2.5×10^{-12}	2.2	21.6	4.2×10^{-8}
291.0	20.3	2.0	4.0×10^{-9}	1.6	25.2	3.3×10^{-6}
320	35.0	1.0	5.8×10^{-9}	1.5	23.7	5.3×10^{-6}

Table 8.2 — Analysis of the dark I-V characteristics for the As-doped p-ZnTe/i-CdTe/n-CdS diode

At high temperatures (T≥250 K) the current is well described by the usual diode equation, modified by the inclusion of series (R_s) and shunt resistances (R_{sh}) i.e

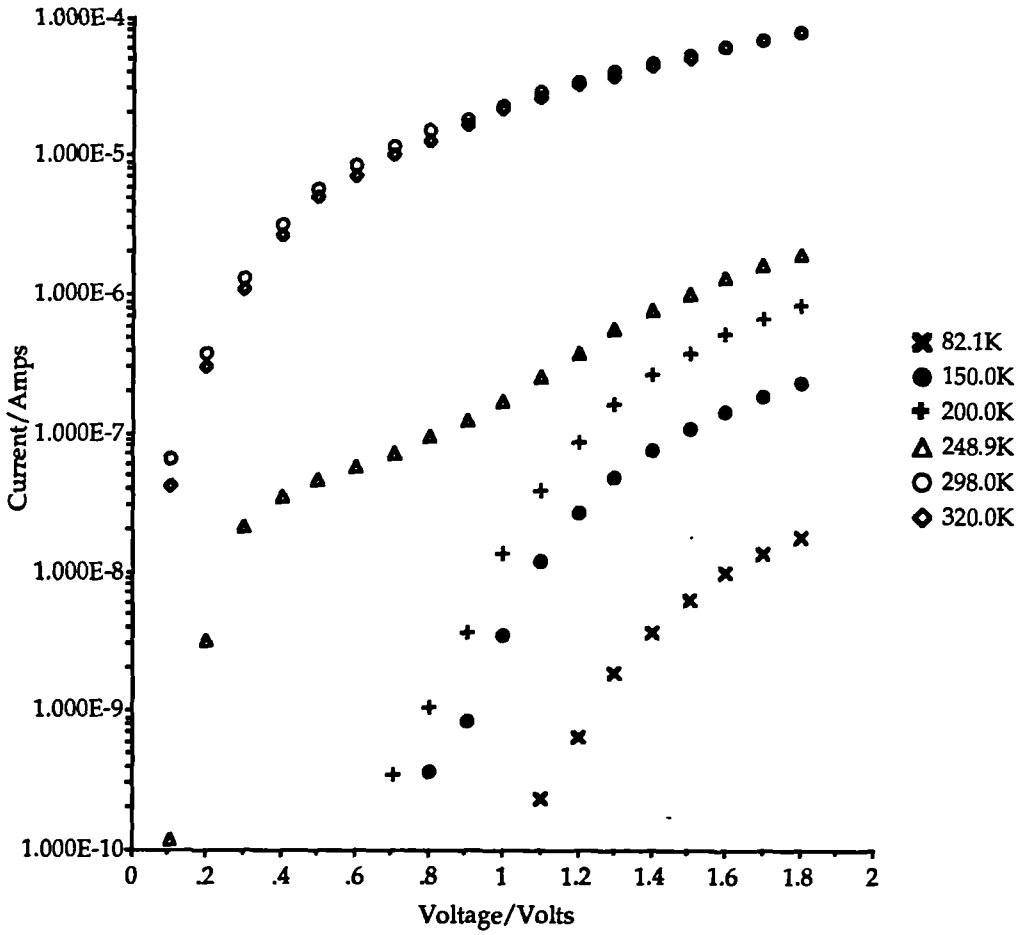

Figure 8.7 — The dark forward bias I_f - V characteristics for the As-doped p-i-n diode

$$I(V,T) = I_o\left[exp\left\{\frac{q(V-IR_s)}{nKT}\right\}-1\right]+\frac{V-IR_s}{R_{sh}} \qquad [8.1]$$

where I_o is the reverse saturation current. However as the temperature was lowered to below 200 K the curves were found to deviate from this behaviour. In particular the low temperature ℓn I_f - V curves display temperature independent slopes which are indicative of tunneling behaviour. A plot of ℓn I_o with temperature gave a straight line at T$\leq$250 K confirming the tunneling behaviour and giving a value of B as 0.026 K^{-1}, see figure 8.9.

Similar behaviour has been reported by Rohatgi et al [8] for polycrystalline ZnTe/CdTe/CdS p-i-n devices, with a space charge recombination transport mechanism becoming dominated by tunneling as the temperature is reduced below 250 K. Rohatgi et al [8] were able to use multivariable regressional analysis to fit the

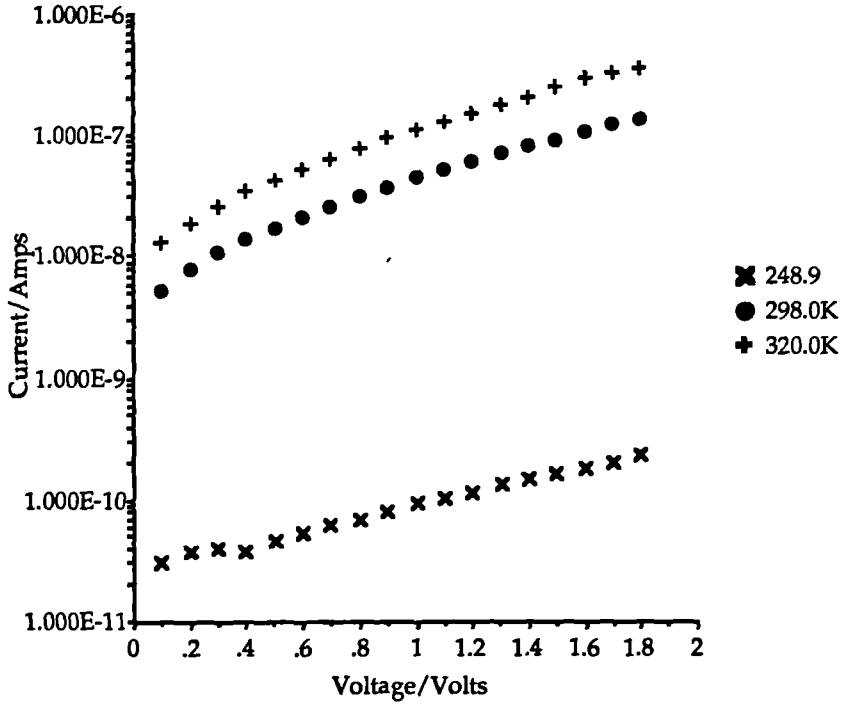

Figure 8.8 — The dark reverse I_r - V characteristics for the As-doped p-i-n diode

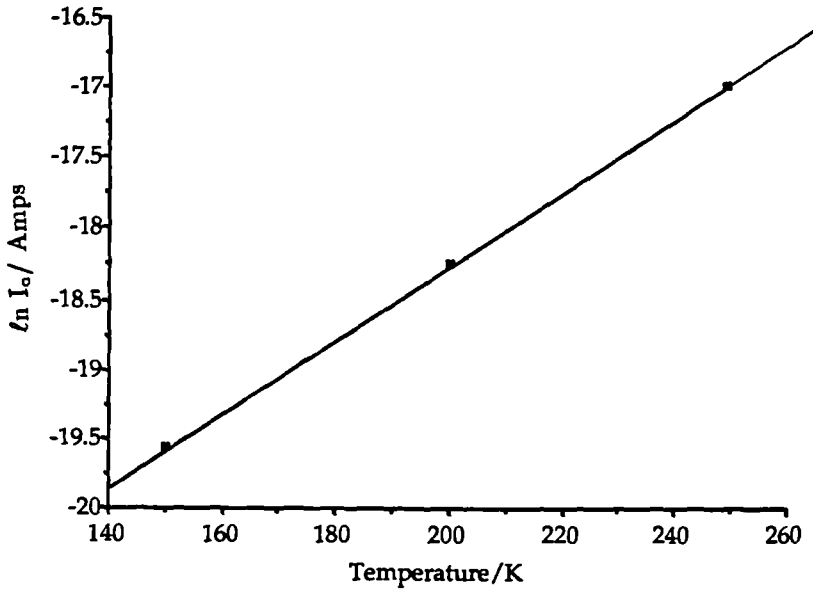

Figure 8.9 — A plot of $\ell n\ I_o$ with temperature

I-V curves to an equivalent circuit response consisting of two diodes with a shunt and series resistance. A detailed discussion of this analogy is given in section 2.1. At 310 K they found a value of n of 1.75, which is similar to the value found by us where an average value of n was calculated to be 1.43, indicating a space-charge recombination controlled transport mechanism. At T $\approx$250 K the other tunneling diode behaviour becomes predominant (see section 8.3). At high voltages the series resistance dominates and n is seen to diverge from a value of between 1-2.

As with the n-CdS/p-CdTe devices the low temperature transport mechanism was indicative of multistep tunneling/recombination via interface states [15]. This type of behaviour has been observed and analysed in detail in epitaxial CdTe/CdS devices [16] and in the *undoped* p-i-n structure discussed earlier. In both these cases the CdTe and/or ZnTe layers were resistive and this seems to be the common factor. As the temperature was reduced the carrier density in the various layers was reduced and so at low temperatures the doped p-i-n structure resembles the more resistive structures of previous studies. At 0.9 V bias the rectification ratio was found to be 74:1, i.e 50% greater than that of the undoped structure.

8.2.4 Capacitance - Voltage measurements

Theoretically, reverse bias C-V measurements are difficult to interpret, but are known to be sensitive to the presence of defects within the i-layer. Capacitance-voltage measurements have however been applied to p-i-n structures previously [20] and can be used to give indications of acceptor density within the CdTe epilayer and estimates of the width of the space-charge region. Dark junction capacitance-voltage characteristics of the doped p-i-n structure grown on the S face were investigated at 295 K, see figure 8.10. It can be seen that the $\frac{1}{C^2}$ versus V characteristic forms a straight line, giving an average acceptor density of $\approx 1.3 \times 10^{18}$ cm^{-3}. The width of the space-charge region was given by $\approx 1.3 \mu$m.

From our analysis of cross sectional TEM micrographs the thickness of the CdTe in this device should be around 1-1.5μm, i.e comparable to the value of the depletion width. Thus it would be expected that the interfaces in the heterojunction formed are playing an active role in the device characteristics, leading to the

observation of tunneling behaviour at low temperatures. A closer examination of the straight line reveals slight variations in the C-V data at 295 K corresponding to regions within the device with different carrier concentrations. The calculated net donor densities were greater near the junction tending to decrease further away from the junction. This may be an indication of the higher density of carriers in the p-ZnTe which become compensated for further into the CdTe depletion region.

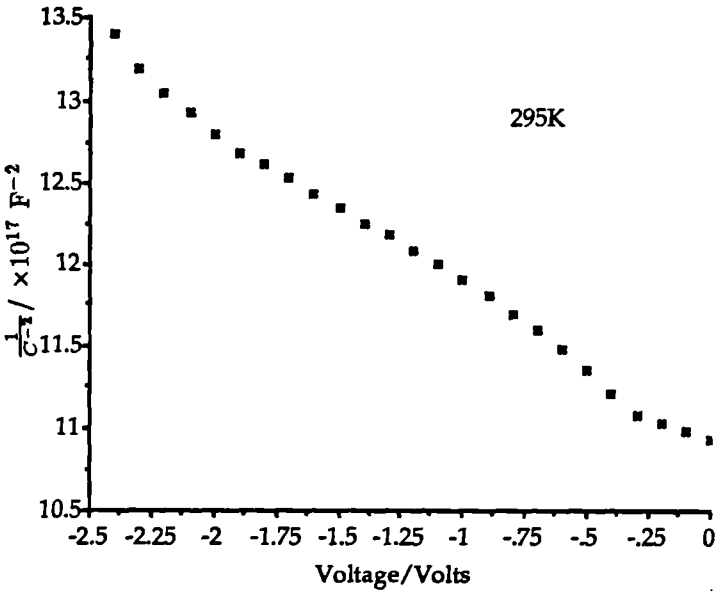

Figure 8.10 — The C-V characteristics for the As-doped p-i-n diode at 295.0 K

8.2.5 Spectral Response measurements

The spectral response of the doped device illuminated through the ZnTe is given in figure 8.11, and approximates quite closely to the ideal window response. Measurements on the undoped structure were not possible due to the high resistivity of the CdTe/ZnTe layers. However, for the doped sample the curve rises at the band gap of CdTe and remains fairly constant over the range 1.6-1.8 eV, when it starts to decrease until the absorption edge of the ZnTe. The CdTe threshold is very sharp but the roll-off in the spectral response at ≈2.0 eV or so is due to a decrease in the transmittance of the ZnTe absorption. The external quantum efficiency is high (≥90%) throughout the usable spectrum, which explains the high J_{sc} value. The broad plateau in the visible region shows a uniform response rather

than a sharp peak, and this is typical of devices made with strongly conducting window layers (as discussed in section 6.5).

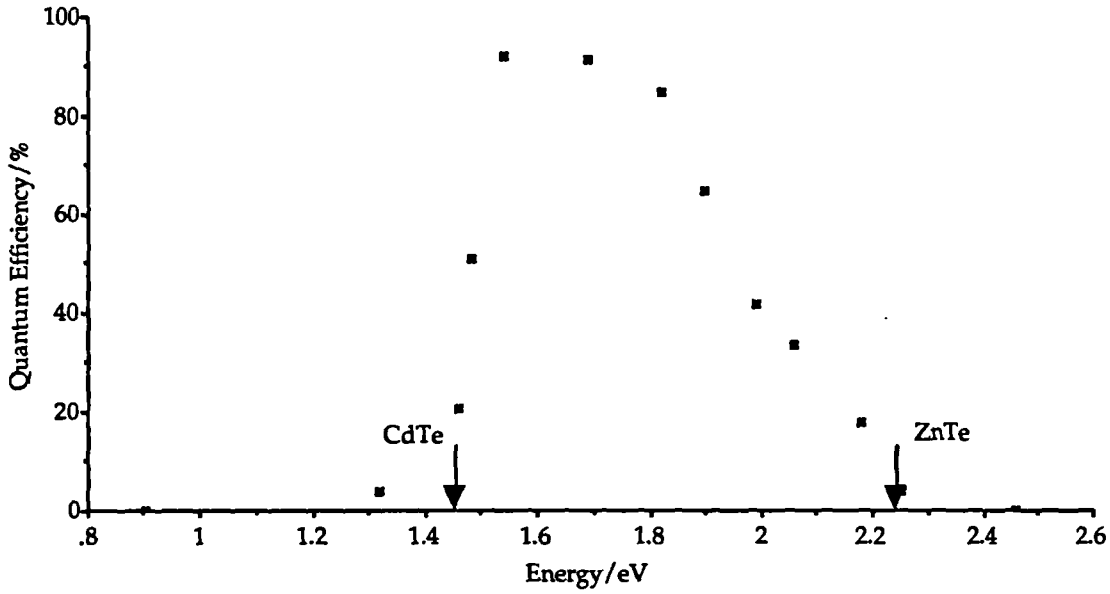

Figure 8.11 — The spectral response measurement of the As-doped p-i-n diode

8.2.6 EBIC measurements

A SEM EBIC line trace across the undoped junction is shown in figure 8.12. From the trace it can be seen that the maximum intensity occurs at the CdTe/ZnTe junction. This signal indicates that there is considerable recombination at the CdS/CdTe and CdTe/ZnTe interfaces since the signal does not decay to zero over the depletion region of the CdTe. The decay of the signal intensity from the CdTe/CdS interface progressing into the CdS can be used to calculate the minority carrier diffusion length in the CdS. However, this cannot be calculated at the ZnTe interface since the thicknesses of the CdTe and ZnTe layers are less than or comparable to their respective diffusion lengths. The intensity from the CdS/CdTe

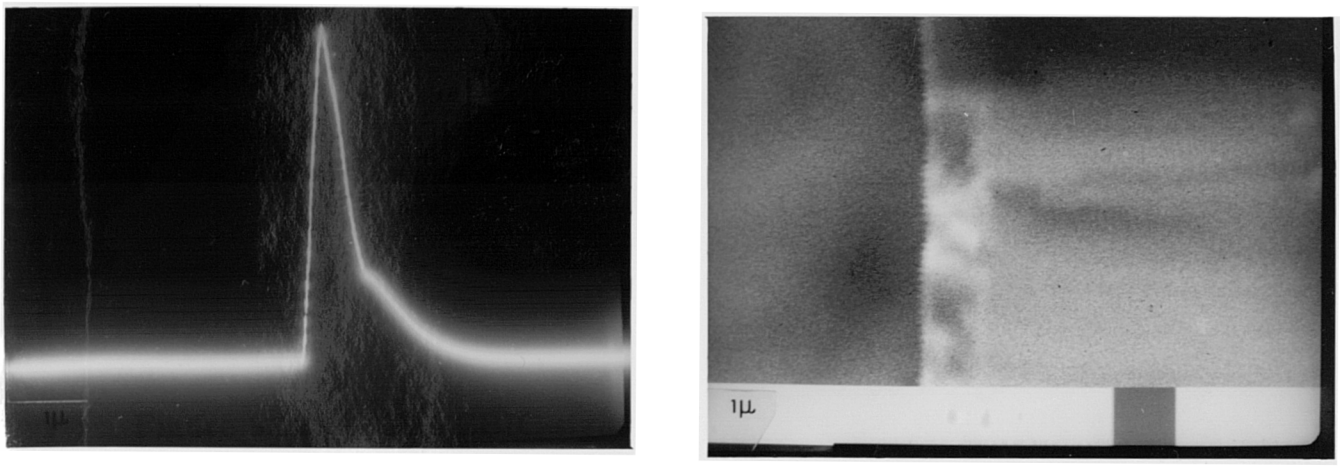

Figure 8.12 — The EBIC signal across the heterojuntion interface for the p-i-n diode

interface would be expected to be much smaller, due to the large lattice mismatch between the CdS/CdTe, and possibly as a result of the substrate polishing techniques leaving an imperfect surface for epitaxy. The value of the current I at a distance d, is given by

$$I(d) = Ae^{-\frac{d}{L}} \qquad [8.2]$$

where L is the minority carrier diffusion length and d is the distance from the junction. Figure 8.13 shows a plot of ℓn I(d) versus d from which the value of L, calculated from the gradient, was found to be 0.7μm. This is in good agreement with the values of L of between 0.6-0.8μm obtained by Awan et al [17] for the CdTe/CdS heterojunction, but is less than values normally obtained for bulk single crystal cells [18]. This reduced value of L may again be attributed to either the large lattice mismatch between the CdS/CdTe, which gives rise to a high dislocation density at the interface or the large contact resistances in the cell.

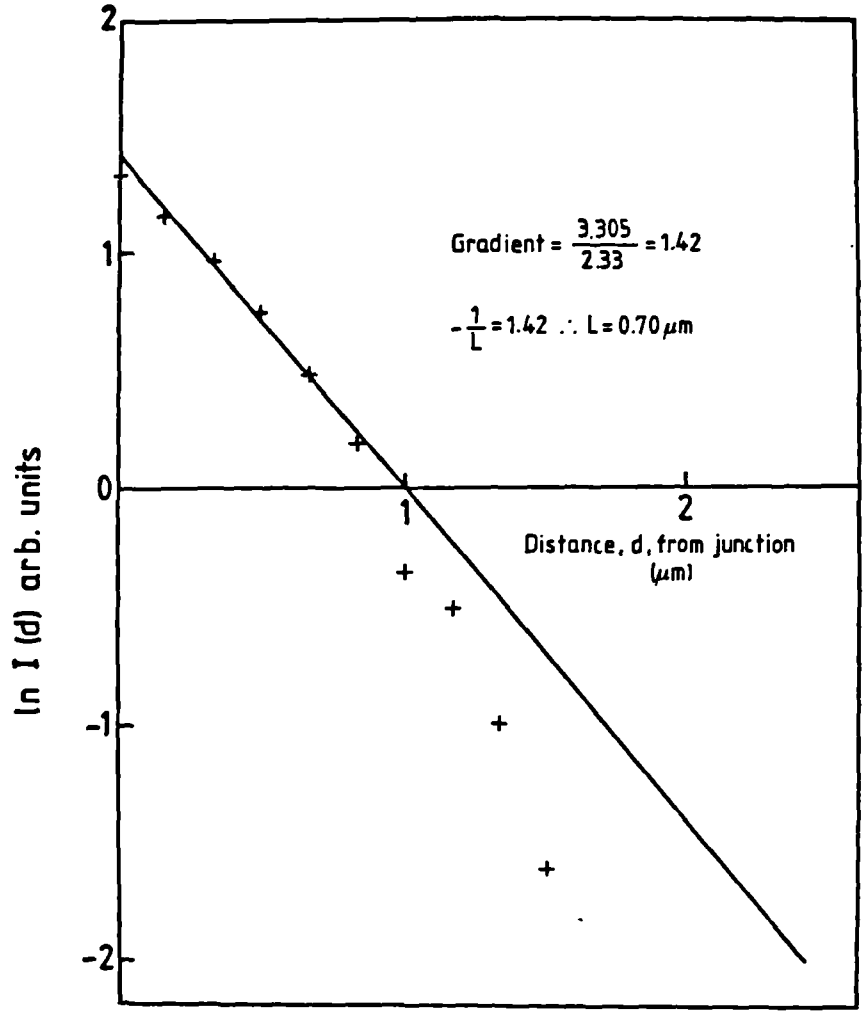

Figure 8.13 — A plot of ℓn I(d) versus d for the undoped p-i-n structure

8.3 Discussion

There are three particular points of interest to be discussed
(i) the effects of doping on the device characteristics
(ii) the comparison of p-i-n devices with those reported by other authors
(iii) the comparison of p-i-n devices with p-n junctions described in chapter 6.
Table 8.3 summarises the effects of doping the p-ZnTe on the p-i-n diode characteristics. An increase in efficiency can be attributed to the increased values of J_{sc} and V_{oc}. This is to be expected because of the increased carrier concentration and higher diffusion potential. The fill factor has remained unchanged and this can be accounted for by the still high series resistance of the device due to the thick (0.5 mm) CdS substrate. The rectification ratio is much higher in the doped device owing to the increased magnitude of the current value and higher V_{oc} value. The

value of I_o has also been reduced in the doped device as a result of the better junction formation and low leakage current. The reverse saturation current will also be smaller because of the increased barrier to minority carrier current flow in the reverse direction due to the displacement of the fermi level in the p and n doped regions.

Diode characteristics	
Undoped	Doped
$V_{oc} = 0.1V$	$V_{oc} = 0.37V$
$J_{sc} = 6.3$ mAcm^{-2}	$J_{sc} = 24.2$ mAcm^{-2}
$ff = 33\%$	$ff = 31\%$
$\eta = \leq 1\%$	$\eta = 3.2\%$
Rectification Ratio = 30 : 1	Rectification Ratio = 400 : 1
$I_o = 6.3\times10^{-6}$ A	$I_o = 3.3\times10^{-6}$ A
Current-transport characteristics	
(V$\leq$0.3V) $n = 1.98$	(T$\geq$250K) $n = 1.43$
(0.3V$\leq$V$\leq$1.0V) A = 4.0	(T$\leq$250K) A = 2.4
Capacitance-voltage characteristics	
	N_D - $N_A = 1.2\times10^{18}$cm^{-3}
	W = 1.3μm

Table 8.3 — A summary of the p-ZnTe/i-CdTe/n-CdS doped and undoped diode characteristics

The current-transport mechanism analysis has been conducted over different temperature ranges for the doped and undoped device. In the undoped device, the characterisation was only completed at temperatures greater than 250 K and here it was observed that at low voltage values the mechanism was found to be space-charge recombination. At higher voltage values the mechanism becomes dominated by tunneling, until at very high voltages this process becomes superseded by increased series resistance effects.

With the doped device analysis was carried out at all temperatures between 70-320 K. At low temperatures the device current transport mechanism was dominated by tunneling, whereas at temperatures above 250 K this was replaced by space-charge recombination mechanisms. If the mechanisms are related to the voltage values, as with the undoped device, then it can be seen that the reverse mechanisms are operating in the different voltage regions. Reasons for this are unclear, but can be related to the higher carrier concentrations in the doped device. As the temperature is reduced the carrier density in the various layers was reduced and so the doped device at the lower temperatures resembles the more resistive structures of previous studies.

Author	Cell	V_{oc}	I_{sc}	ff	η	n	W	I_o
		(V)	($mAcm^{-2}$)		(%)		μm	(A)
V. Ramanthan	ED	0.745	20.5	0.71	10.8	1.68	2.02	1×10^{-9}
A. Rohatgi	MOCVD	0.730	22.16	0.59	9.7	1.75	-	1.5×10^{-8}
A. Nouhi	MOVPE	0.697	22.1	0.61	9.4	1.56	-	1.06×10^{-9}
R. Sudharsanan	MOCVD	0.720	22.47	0.60	9.7	1.81	-	1.5×10^{-8}
P. Meyers	ED	0.68	20.5	0.63	8.8	-	-	-
M.Y. Simmons	MOVPE	0.37	24.2	0.31	3.2	1.43	1.3	3.3×10^{-6}

Table 8.4 — Comparison of p-i-n devices

It was not possible to record the capacitance-voltage characteristics of the undoped device due to the high series resistance of the CdTe/ZnTe layers. The characteristics of the doped device were however, able to be recorded and gives values of $N_A \approx 10^{18}$ cm^{-3}, and W=1.3μm in good agreement with XTEM results.

The comparison of this single crystal p-i-n structure with other polycrystalline devices of similar structure is shown in table 8.4. In general the values are much smaller for each parameter measured. From the spectral response measurements the value of J_{sc} for the cells grown in our laboratories was recalculated from the

theoretical maximum of 30.3 $mAcm^{-2}$ [19]. From figure 8.11 the quantum efficiency at the band gap of CdTe was ≈80% giving a value of J_{sc} as 24.2 $mAcm^{-2}$, compared with the value of 136 $mAcm^{-2}$ measured directly. Without any material growth and design optimisation p-ZnTe/i-CdTe/n-CdS cells with efficiencies of ≈ 3.2% were fabricated. This is low compared with that found by other authors [8,9,19,20,21] for polycrystalline p-i-n structures, but it is suspected that subtle changes in the process may have a significant effect on the device properties [1]. There is a lot of flexibility in the design of the structure, allowing room for future improvement, including the annealing and in-situ preheat treatments of the CdS substrate, the adjustment of the CdTe film deposition conditions and stoichiometry, along with the substitution of CdZnS for CdS to increase the band gap of the window layer.

The low value of V_{oc} can only be explained by large density of interface states. MOCVD cells of this nature have previously been shown to have lower V_{oc} and fill factor values than electrodeposited cells [21]. It is the poor quality of the CdTe/CdS interfaces that have led to low values of V_{oc} and fill factor. The fill factor is also still expected to be somewhat low because of high series resistance.

The annealing of the CdS was initially thought to reduce the presence of oxygen on the surface, which has been shown to reduce doping concentration by trapping electrons [22]. However this annealing process has been shown to cause Cd evaporation from the surface; leaving a CdS layer with a lower carrier concentration near the CdTe/CdS interface - this will lead to a lower value of the open circuit voltage. Thus although annealing gives better efficiencies, it also induced undesirable defects and may limit future improvement in efficiency for a given cell design, unless the fabrication process and design are optimised. C-V measurements are extremely useful in the analysis of p-i-n structures in determining whether the i-layer is fully depleted or not. Ideally, the i-layer should be fully depleted allowing the maximum separation of carriers across its width. If this is the case however then the interfaces inherently play an important role in limiting the cell performance. Another important parameter which affects the value of V_{oc} is the thickness of the i-CdTe layer. If this is larger than the depletion width of the device, then V_{oc} will be reduced and the series resistance increased. The distribution of the electric field in the entire CdTe layer is crucial to the production of high efficiencies. A

comparison of the p-i-n and p/n devices grown on the S face of {0001} CdS is given in table 8.5.

Cell	V_{oc}	I_{sc}	ff	η	A	n	W	N_A	I_o
	(V)	($mAcm^{-2}$)		(%)			(μm)	(cm^{-3})	(A)
p-i-n	0.37	22.4	0.31	3.2	2.4	1.43	1.3	1.2×10^{18}	3.3×10^{-6}
p-n	0.52	15.6	0.16	1.49	2.57	1.3	0.29	5.0×10^{16}	5.8×10^{-8}

Table 8.5 — Comparison of p-i-n and p-n devices

It can be seen that for the p-i-n device the values of I_{sc}, ff, η are much higher. The values of V_{oc} and I_o are however lower indicating the increase in interface state density in the p-i-n junction. This is to be expected due to the presence of two interfaces in the p-i-n structure. The p-i-n structure is also maintained at high temperatures for longer, possibly allowing interdiffusion at the interfaces causing leaky junctions and poorer V_{oc} and I_o values. The values of N_A and W are greater for the p-i-n device because of the high conductivity of the p-ZnTe (greater than p-CdTe), leading to larger depletion widths and more efficient carrier collection. The recombination in the field free region of the p-i-n device is responsible for losses and reduced values of fill factor. The design of the p-i-n device places little emphasis on the minority carrier diffusion length and lifetime, which is important in the p-n structures. The series resistances of the p-n devices are greater leading to lower fill factors and J_{sc} values. This is mainly due to the higher conductivity of the p-ZnTe epilayer compared with that of the p-CdTe.

Analysis of the spectral response data for the two cells shows that the p-i-n response is higher over most of the spectral range, due to the higher values J_{sc}, ff and η. Also the shape of the spectral response rises sharply and remains constant over the range to the ZnTe cut-off. For the n-CdS/p-CdTe device the response peaks at $\approx$1.5 eV, corresponding to collection at the CdS/CdTe interface, but for short wavelength light absorbed close to the CdTe surface, collection is limited due to diffusion and recombination. In the p-i-n device however carriers are also collected by the drift field.

The current transport in the two types of devices appears different. For the p/n devices tunneling was the major mechanism above 300 K, whereas below that the series resistance of the CdS dominated. For the p-i-n devices the current transport mechanism at temperatures greater than 250 K were dominated by emission/recombination mechanisms, whereas below 250 K tunneling was the predominant mechanism. The rectification ratios were approximately three times smaller. For the p-i-n device, the carrier densities in the various layers were reduced as the temperature was lowered and so the behaviour resembles that of the more resistive p-n structures.

Although the present processing conditions are far from ideal, respectable performance has been achieved. Further improvement in cell efficiency is possible, but more sophisticated studies are required to realise the full potential of the CdTe p-i-n structure. Optimisation of the ZnTe/CdS layers is expected to reduce the reflection and absorption of the window layers. Further improvements in V_{oc} can be obtained by reducing junction recombination. The problem of the J_{sc} calculations for the p-i-n devices has been realised by Meyers et al [23] who suggested using optical coupling of the layers to clarify grid alignment.

8.4 The n-GaAs/i-CdTe/p-ZnTe Solar Cell

8.4.1 Introduction

One of the problems encountered in the p-ZnTe/i-CdTe/n-CdS device was the quality of the single crystal substrate material. The x-ray rocking curve half width of the {0001} CdS was found to be approximately 66 arc s^{-1} and difficulty in preparation of the surfaces for epitaxial growth was encountered (see section 4.4). As a result the use of other n-type single crystal substrates was suggested. Since the ZnTe was to be used as the window layer there was no requirement for the other n-type substrate to be transparent to light. Gallium arsenide has been a well used substrate for the growth of $Cd_xHg_{1-x}Te$, with CdTe as a buffer layer so that the epitaxial growth of CdTe onto GaAs has thus been extensively studied, although no attempt had previously been made to fabricate p-i-n devices. Consequently it

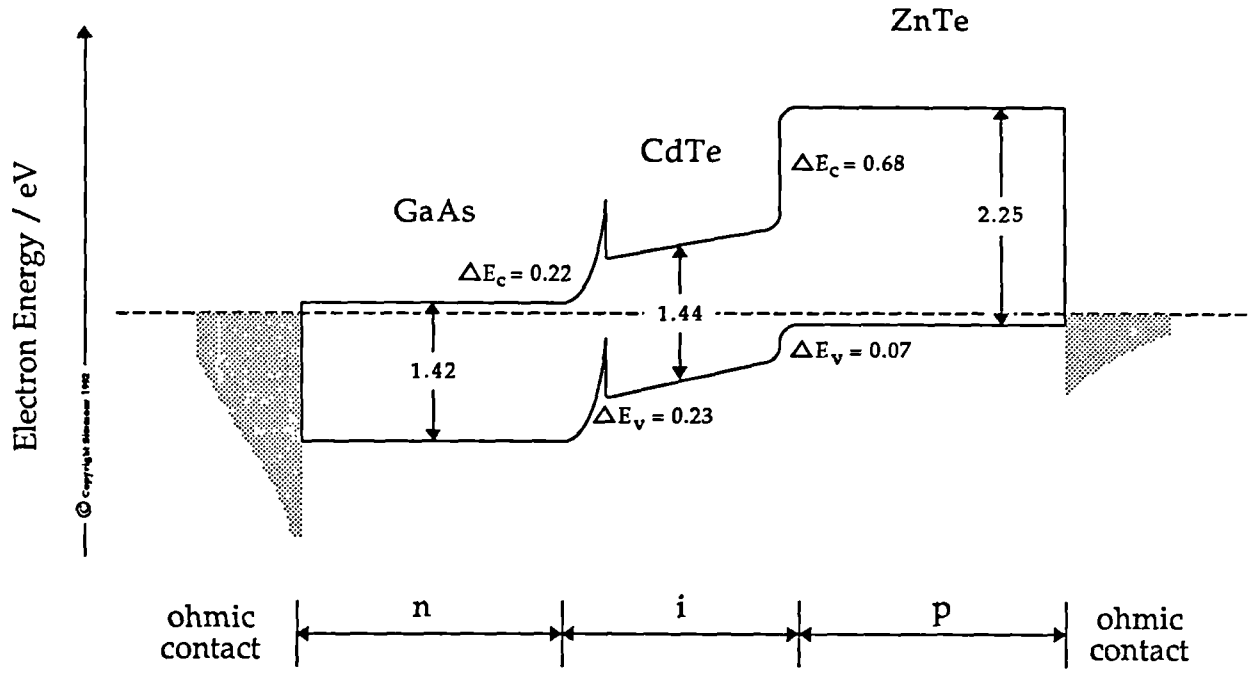

Figure 8.14 — The band structure diagram of the p-ZnTe/i-CdTe/n-GaAs device

was decided to investigate p-i-n structures grown on n-GaAs {001} substrates.

The suggested band diagram for the p-ZnTe/i-CdTe/n-GaAs device is presented in figure 8.14. It can be seen that the band alignments for this device are not ideal as there appears to be a conduction band spike at the CdTe/GaAs interface of 0.22 eV. This could lead to an accumulated layer in the CdTe adjacent to the GaAs, possibly leading to lower device efficiencies. The integration of a II-VI compound onto a III-V compound to form a novel heterojunction has rarely been considered using n-GaAs [24,25], however several authors have postulated the integration of II-VI and III-V structures for solar cell purposes [26,27,28]. The p-GaAs/n-ZnSe solar cell has been produced with an efficiency of ≈8-9% [28]. As yet no work has been published on the CdTe/ZnTe structure based on n-GaAs. This section of chapter 8 reports on the successful growth by MOVPE and characterisation of a p-ZnTe/i-CdTe/n-GaAs device.

8.4.2 Experimental

Silicon-doped {001} n-GaAs with a resistivity of $\approx 3 \times 10^{-3}$ Ωcm, purchased from MCP, was used as the single crystal substrate. The GaAs was prepared for use as the substrate by etching for 4 minutes in a 4:1:1 solution of H_2SO_4:H_2O_2:H_2O at 40°C. The substrate was then rinsed carefully in deionised water and refluxed in isopropyl alcohol. After loading into the MOVPE reactor, the substrates were given a standard heat clean at 400°C for ten minutes in an attempt to remove any oxide layer that may have formed. The CdTe layer was grown at a substrate temperature of 325°C using a II:VI precursor ratio of 1:1 with a H_2 dilution flow of 7 $lmin^{-1}$ for 1800 secs. This would result in a layer $\approx 1 \mu m$ thick with a resistivity greater than 10^3 Ωcm. The top ZnTe layer was grown at the same substrate temperature of 325°C using a II-VI ratio of 5:1 for 1800 seconds, to give a layer $\approx 0.6 \mu m$ thick (see section 5.6.3). The layers grown were oriented parallel to the {001} plane and contained very high densities of both misfit and threading dislocations [29]. Indium point contacts were evaporated onto the n-GaAs and either Au or C-paste contacts on the ZnTe side. Carbon has been found to give excellent room temperature contacts to high electron affinity p-type II-VI semiconductors [8]. However, C paste contacts freeze out at temperatures less than 250 K and thus Au was used when detailed current voltage characteristics were measured at low temperatures.

8.4.3 Diode characteristics

The photovoltaic output charactersistics for the n-GaAs/i-CdTe/p-ZnTe device, illuminated through the ZnTe is shown in figure 8.15. The values of V_{oc} and ff are 0.55 V and 27% respectively. I_{sc} was 1.85×10^{-4} A, which was remeasured from spectral response measurements to give a current density of 20.2 $mAcm^{-2}$ and an efficiency of 3.4%. The overall efficiency was low due to the high series resistance and contact resistance losses of the cell, leading to low values of the fill factor (27%). The open circuit voltage was high, but the cell is less efficient than the p-ZnTe/i-CdTe/n-CdS diode (described in section 8.2) due to the lower short circuit current density. However a respectable efficiency has been achieved, and future improvement in cell design should offer even higher efficiencies.

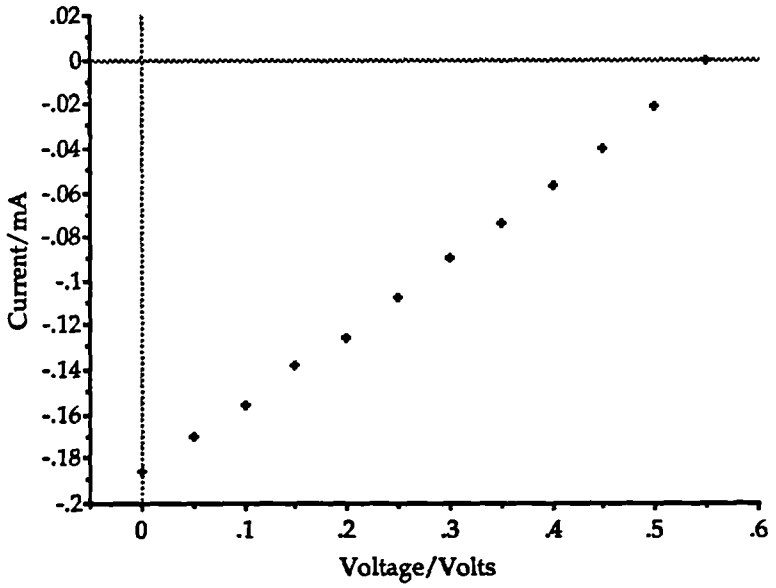

Figure 8.15 — The Photovoltaic output charactersistics for the p-ZnTe/i-CdTe/n-GaAs diode under AM1.5 illumination

8.4.4 Current-transport properties

The dark ℓn I_f-V characteristics for the p-ZnTe/i-CdTe/n-GaAs device, with Au contacts is shown in figure 8.16, whilst the reverse characteristics are shown in figure 8.17. The rectification ratio at 0.9 V bias was calculated to be 22:1 at 320K.

From these figures it can be seen that two separate regions exist, with change in voltage. At low temperatures ($T \leq 250$ K), region A ($0 \leq V \leq 0.3$ V) and region B ($V \geq 0.3$ V) are evident. Above 250 K region A extends up to 0.5 V and region B occurs at voltages exceeding 0.5 V. The analysis of the data presented is given in table 8.6. Unlike the p-i-n structure based on CdS substrates, the GaAs p-i-n device current transport mechanism appears to be dominated by a tunneling process at all temperatures investigated (77-320 K). The curves all show the same slope in both regions A (4.63± 3%) and region B (0.98±2.4 %) although at high current levels the slopes start to alter as expected from the high series resistance of the CdTe/ZnTe. To confirm the presence of tunneling at all temperatures a plot of ℓn I_o versus temperature is illustrated in figure 8.18.

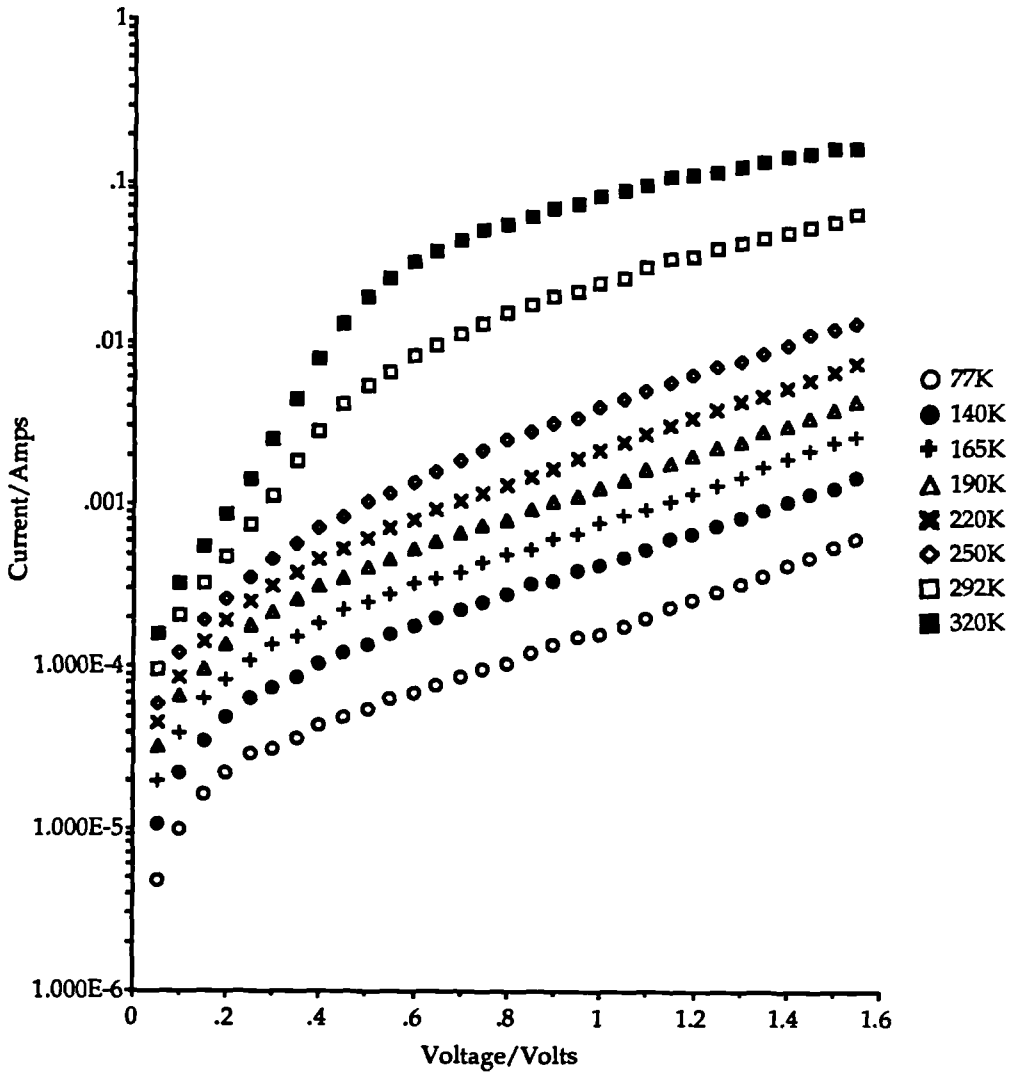

Figure 8.16 — The dark forward I_f-V charactersistics for the p-ZnTe/i-CdTe/n-GaAs diode

It can be seen that the relationship is linear giving a value of B as 0.0014 K^{-1}. Again, no other values of B have been published for this heterojunction, but the value can be compared with that found for the CdS-based p-i-n device (0.016 K^{-1}). Thus B is similar for the GaAs based device, although reasons for this are unknown.

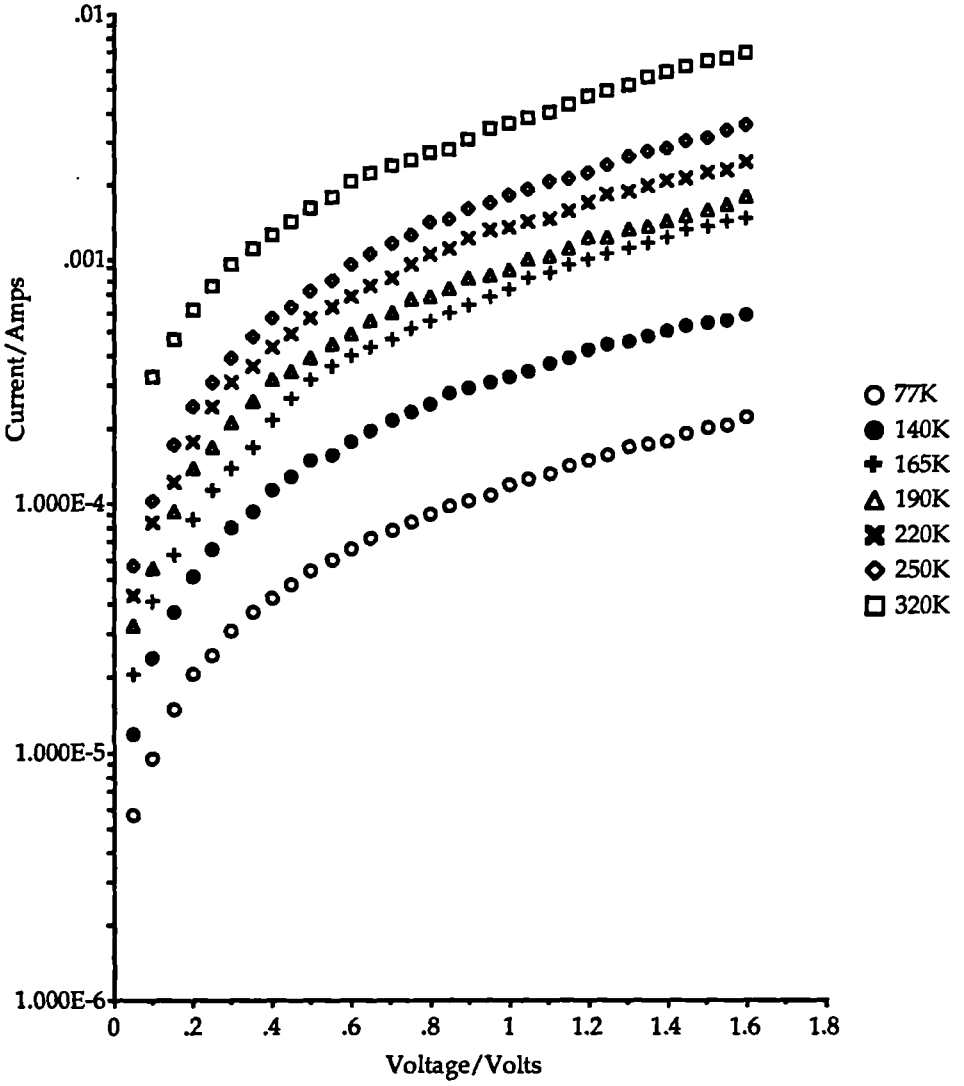

Figure 8.17 — The dark reverse I_r-V charactersistics for the p-ZnTe/i-CdTe/n-GaAs diode

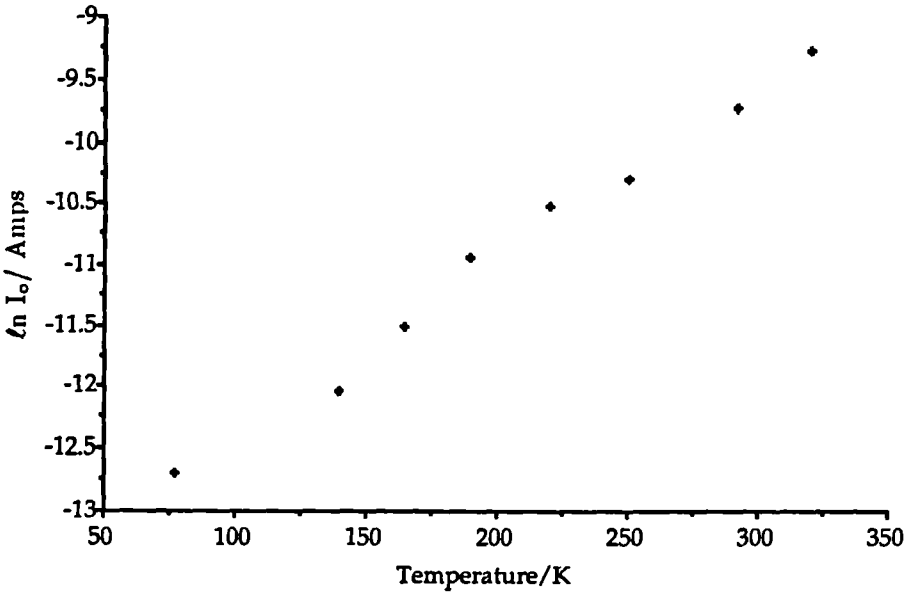

Figure 8.18 — A plot of $\ell n\ I_o$ versus temperature

Temperature/K	Region A (0≤V≤0.3V)			Region B (≥0.3V)		
	A	n	I_o/A	A	n	I_o/A
77	4.49	33.5	3.1×10^{-6}	1.0	150.6	1.7×10^{-5}
140	4.55	18.2	6.0×10^{-6}	0.96	86.3	4.6×10^{-5}
165	4.73	14.9	1.0×10^{-5}	0.97	72.4	8.0×10^{-5}
190	4.60	13.3	1.8×10^{-5}	0.99	61.6	1.3×10^{-4}
220	4.59	11.5	2.7×10^{-5}	0.99	53.2	2.2×10^{-4}
250	4.67	9.9	3.5×10^{-5}	0.99	46.8	3.9×10^{-4}
	Region A (0≤V≤0.5 V)			Region B (≥0.5V)		
292	4.70	8.4	6.0×10^{-5}	0.81	49.0	3.4×10^{-3}
320	4.73	7.7	9.5×10^{-5}	0.71	51.0	1.5×10^{-2}

Table 8.6 — Analysis of the forward I-V data for the p-ZnTe/i-CdTe/n-GaAs device

8.4.5 Capacitance-voltage characteristics

Dark junction capacitance-voltage characteristics of the GaAs-based p-i-n device were investigated at a temperatures of 295 K, see figures 8.19. Initial examination revealed a linear section between -2.5 and -0.75V, leading to an average acceptor density of 7.6×10^{18} cm^{-3} and a depletion layer width of 26.7μm.

Closer examination reveals three different regions of varying slope corresponding to regions within the device with different carrier concentrations. At the junction region the net donor density is lower than further away from the junction. This indicates the presence of a barrier at the interface which is impedeing the current transport. At high voltage values this barrier is exceeded, and the net donor density increases.

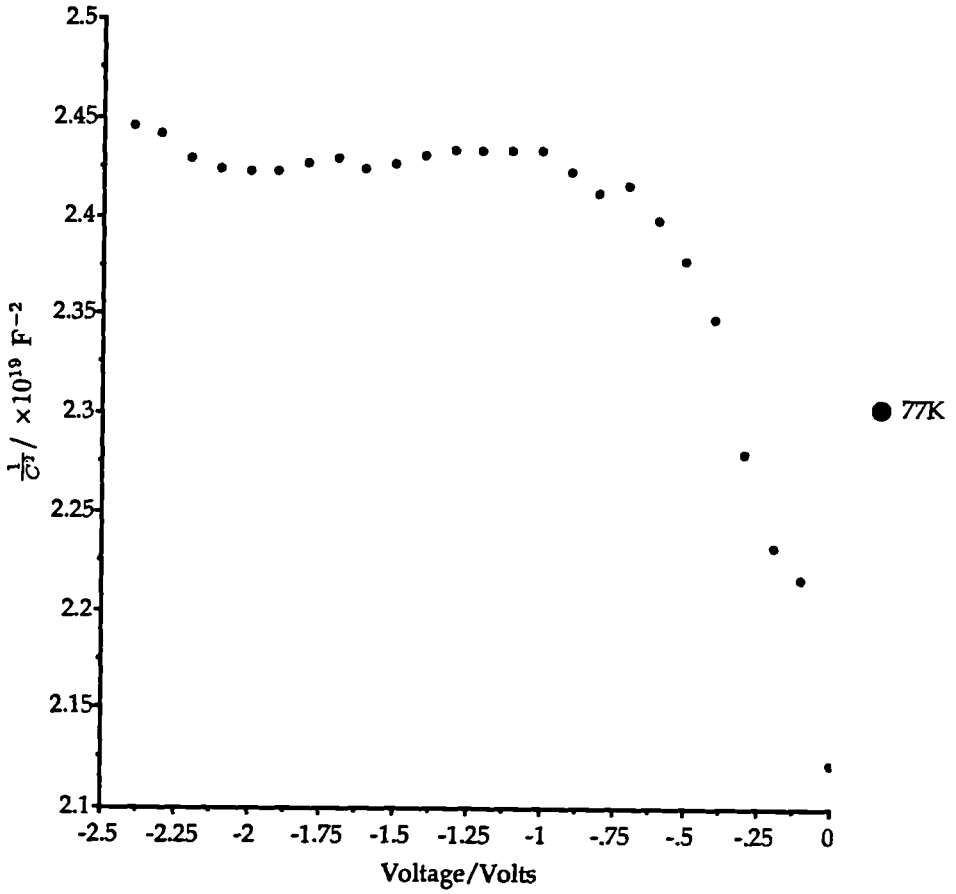

Figure 8.19 — The Capacitance-voltage characteristic at 295 K

8.4.6 Spectral response measurements

The spectral response quantum efficiency of the p-ZnTe/i-CdTe/n-GaAs device, illuminated through the ZnTe is shown in figure 8.20. It can be seen that whilst the CdTe cut-off is fairly sharp the response is quite narrow and did not extend to photon energies as high as the ZnTe band gap energy. The maximum quantum efficiency was $\approx$ 84%, which is fairly high but lower than that observed for the CdS-based p-i-n diode. The contrast between this response and the CdS-based diode response indicates that there is a different microstructural defect content in the CdTe i-layer grown on the two types of substrate. The CdTe layers grown on the GaAs substrates are thought to be more heavily dislocated than those grown

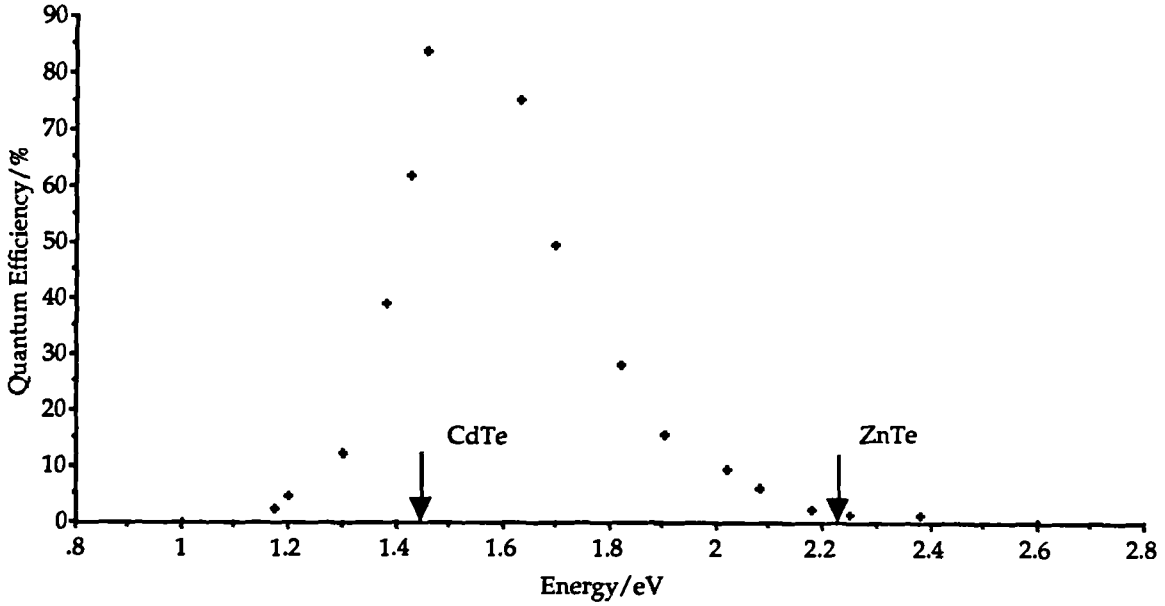

Figure 8.20 — The spectral response curve of the p-ZnTe/i-CdTe/n-GaAs diode

on the CdS where twinning helps to accomodate the lattice mismatch, the implications of this are discussed more fully in section 8.4.7.

8.4.7 Discussion

The lattice parameter of CdTe at 300 K is 6.4815 Å [30] and GaAs is 5.6533 Å [31], leading to a lattice mismatch of 14.6%. Such a large lattice mismatch between materials usually manifests itself by large numbers of dislocations at the epilayer/substrate interface which extend some distance (1-2μm) into the epilayer. In addition differential thermal expansion between the two materials may cause further degradation of the interfacial region of the device. Arch et al [32] used temperature dependent x-ray diffraction measurements of MOVPE grown CdTe epilayers on GaAs to observe the effects the mismatch and thermal expansion differences had on the layers grown. Their results confirmed the presence of strain at the interface due to the compression of the CdTe unit cell by the atoms of the GaAs substrate surface (which has a much lower lattice parameter). The growth of CdTe on foreign substrates has been a subject of interest because of its application as a buffer layer in the growth of $Cd_xHg_{1-x}Te$ for infrared detectors. Despite the

large mismatch of the (100)||(100)GaAs relationship, high quality single crystal CdTe films have been fabricated [33,34].

It is likely that a thin oxide has remained on the surface of the (100)GaAs substrate after the pre-growth anneal at 410°C. Generally GaAs is annealed at 600°C to remove completely any oxide layer on the surface [35], but for comparison purposes the CdS-based p-i-n diode was grown in the same growth run and high temperature anneals were inappropriate. Otsuka et al [35] proposed that as a result of low temperature anneals (below 450°C), the bonding of the epitaxial CdTe takes place via Te-O bonds at the interface, due to the presence of a thin oxide layer on the GaAs. Thus the importance of the preparation of the substrate surface is paramount to understanding the effects it may have on the device characteristics. Already it has been established that for the GaAs/CdTe interface, problems with misfit dislocations, strain and thin interfacial oxide layers are inherent. TEM micrographs presented in section 5.4 confirm the presence of the large density of misfit dislocations.

The presence of the spike in the conduction band at the GaAs/CdTe interface could lead to an accumulated layer in the CdTe adjacent to the GaAs. As a result, carriers would collect at this interface leading to a higher probability of recombination. The presence of this barrier is confirmed by the existence of a tunneling/recombination current transport mechanism at all temperatures. A comparison of the GaAs-based and CdS-based characteristics is given in table 8.7. From this table it can be seen that the efficiencies of the devices are similar. The values of V_{oc} are greater for the GaAs-based devices, but have smaller I_{sc} values, giving rise to net overall efficiencies that are similar to those found on the CdS-based devices. The large conduction band spike at the GaAs/CdTe interface has dominated all the device characteristics; the rectification ratio is low, I_o is high, W is large and the spectral response curve is narrow. For the CdS-based device, whilst the number of misfit dislocations is reduced, the layer contains twins parallel to the substrate/epilayer interface. This has led to alternate current-transport mechanisms, higher rectification ratios and higher I_o values. It is interesting to note that the net carrier concentration in the CdTe region is similar and so are efficiency values.

Diode characteristics	
GaAs-based p-i-n diode	CdS-based p-i-n diode
V_{oc} = 0.55V J_{sc} = 20.2 mAcm^{-2} ff = 27% η = 3.4% Rectification Ratio = 22 : 1 I_o = 6.0×10^{-5} A	V_{oc} = 0.37V J_{sc} = 24.2 mAcm^{-2} ff = 31% η = 3.2% Rectification Ratio = 400 : 1 I_o = 3.3×10^{-6} A
Current-transport characteristics	
- A = 4.63	n = 1.43 A = 2.4
Capacitance-voltage characteristics	
N_D - N_A =7.6×10^{18}cm^{-3} W = 26.7μm	N_D - N_A=1.2×10^{18}cm^{-3} W = 1.3μm

Table 8.7 — A comparison of the p-ZnTe/i-CdTe/n-GaAs and the p-ZnTe/i-CdTe/n-CdS devices

With higher pre-growth annealing temperatures the CdTe epilayer can be forced to grow on a {111} orientation on the GaAs [36], and this would lead to a better understanding of the difference the effects of twinning and misfit dislocations have on the efficiency. No other data has been published on the p-ZnTe/i-CdTe/n-GaAs solar cell, and it holds promise of being a likely alternative to that proposed by Meyers et al [1]. The differences between the CdS-based and the GaAs-based devices can possibly be explained by the presence of the conduction band spike at the GaAs/CdTe interface, which is not present in the CdS-based device or by the differences in the microstructural defect content of the i-CdTe layers. It was postulated in chapter 6 that twinning impeded the current flow, but in the case of the p-i-n device the reduced dislocation density may help by assisting the separation of generated carriers. As with the CdS-based p-i-n diode there are a number of parameters that can be optimised, not withstanding the GaAs substrate preparation.

8.5 Preliminary investigations into other device structures

8.5.1 Introduction

This section discusses preliminary results obtained for the following device strutures :

(i) p-ZnTe/i-CdTe/n-CdTe

(ii) p-ZnTe/i-$Cd_{1-x}Zn_xTe$/n-CdS

(iii) p-ZnTe/i-$Cd_{1-x}Zn_xTe$/n-GaAs

(iv) p-ZnTe/i-$Cd_{1-x}Zn_xTe$/n-CdTe

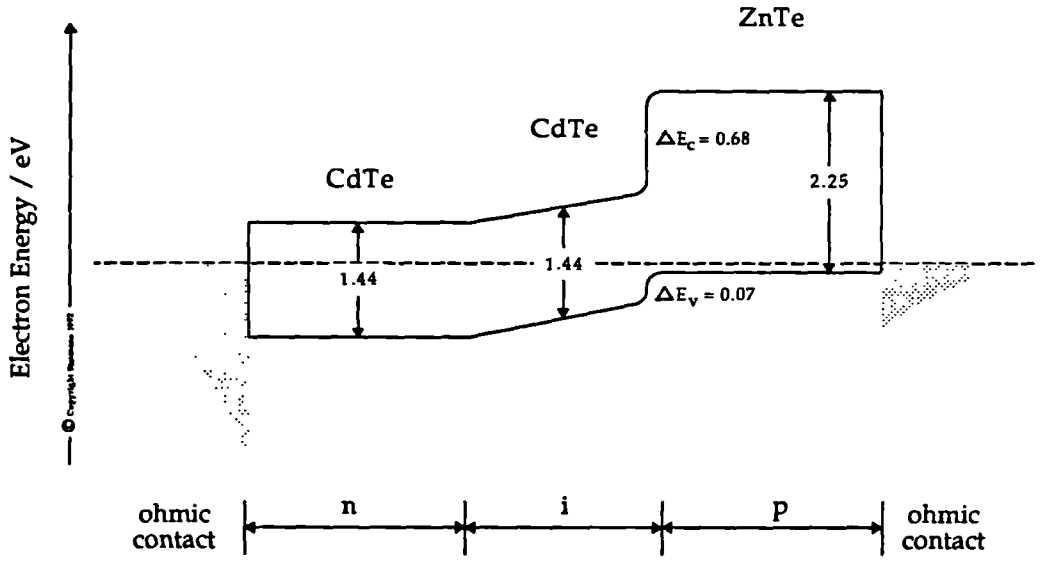

Figure 8.21 — The band structure diagram of the p-ZnTe/i-CdTe/n-CdTe device

using {111}CdTe, {0001}CdS and {001}GaAs as substrates. $(\bar{1}\bar{1}\bar{1})$B CdTe has previously been used as a substrate for CdTe epitaxial growth [37,38] for the production of substrates for $Cd_{1-x}Hg_xTe$. No work has been published on the MOVPE

growth of CdTe/ZnTe on n-type $(\bar{1}\bar{1}\bar{1})$B CdTe for use in solar cell fabrication. The suggested band diagram for this device is presented in figure 8.21, where it can be seen that the band alignments for this device are ideal. There are no spikes in the conduction or valence bands which would cause accumulation of carriers and hence a reduced efficiency.

The use of a graded i-layer in the p-i-n structure could help reduce the formation of misfit dislocations and increase device efficiency due to the absorption over a wider range of wavelengths. The use of a graded i-layer aids the formation of a larger field across the device leading to increased carrier separation. The incorporation of these graded layers will affect the band structure diagrams as shown in figure 8.22 (a), (b) and (c) for CdS, GaAs and CdTe-based p-i-n structures respectively. It can be seen that, especially in the case of the GaAs-based p-i-n structure the grading has reduced the effect of ΔE_c and this effect has been utilised in graded heterojunction devices [39]. This section reports the fabrication of p-ZnTe/i-CdTe/n-CdTe solar cell structures and the incorporation of graded $Cd_{1-x}Zn_xTe$ absorber layers into the p-i-n devices described in sections 8.1 and 8.2 (including the p-ZnTe/i-CdTe/n-CdTe device). Time did not permit further investigation into the structural and electrical properties of these devices.

8.5.2 Experimental

The n-type substrates were prepared for epitaxial growth as described in chapter 4; the $(000\bar{1})$B CdS was polished in a solution of 4.8g CrO_3, 9.1g HNO_3 and 50ml of deionised water for 10 minutes at 30°C, the (100) GaAs was etched in a 4:1:1 solution of H_2O:H_2SO_4:H_2O_2 at 40°C for 4 minutes and the CdTe was chemomechanically polished in a mixture of 0.5% Br_2 in 4:1 methanol:ethanediol.

After loading in the MOVPE reactor the system was flushed for 1 hour to remove all the oxygen from the system. All the substrates were then heat cleaned at 400°C for 10 minutes. With the CdTe p-i-n based structure the CdTe/ZnTe epilayers were grown under the same conditions as those used for the p-i-n based structures in sections 8.2 and 8.3, i.e a 1μm thick CdTe epilayer was grown at 325°C followed by a 0.6μm thick arsenic-doped ZnTe layer. The p-i-n structures

were then removed from the reactor and, after cooling, indium and gold point contacts were made to the n-CdTe and p-CdTe surfaces respectively.

The growth procedure for the graded $Cd_{1-x}Zn_xTe$ epilayer was more complex. The layer could be either step graded or graded gradually. Step grading is much easier to control, and the result of the growth more reproducible due to the growth study presented in section 5.8. Recent results have indicated that gradual increases in the composition of graded layers produce a much better solar efficiency [40]. The growth procedure thus consisted of the sequential growth of 8 different epilayers of varying Zn content from CdTe to ZnTe, see table 8.8. The initial CdTe epilayer was grown at 325°C at a 1:1 II:VI ratio, whilst the $Cd_{1-x}Zn_xTe$ growth was conducted at 400°C and a 17:1 II:VI ratio. Finally the arsenic doped ZnTe top layer was grown at 325°C with a II:VI ratio of 5:1.

Epilayer	Growth Temp/°C	II:VI ratio	Zn/Cd ratio	Growth time/secs
CdTe	325	1:1	0	300
$Cd_{0.96}Zn_{0.04}Te$	400	17:1	5:1	300
$Cd_{0.84}Zn_{0.16}Te$	400	17:1	10:1	300
$Cd_{0.60}Zn_{0.40}Te$	400	17:1	15:1	300
$Cd_{0.53}Zn_{0.47}Te$	400	17:1	20:1	300
$Cd_{0.38}Zn_{0.62}Te$	400	17:1	25:1	300
$Cd_{0.24}Zn_{0.76}Te$	400	17:1	30:1	300
ZnTe	325	5:1	1	300

Table 8.8 — Graded $Cd_{1-x}Zn_xTe$ growth procedure

Following growth Au point contacts were made to the ZnTe surface and In point contacts to the n-type substrate. The samples were then tested for device efficiency.

8.5.3 Results and discussion

The solar efficiencies of all devices were measured under AM1.5 illumination and a summary of these initial results are presented in table 8.9. It can be seen

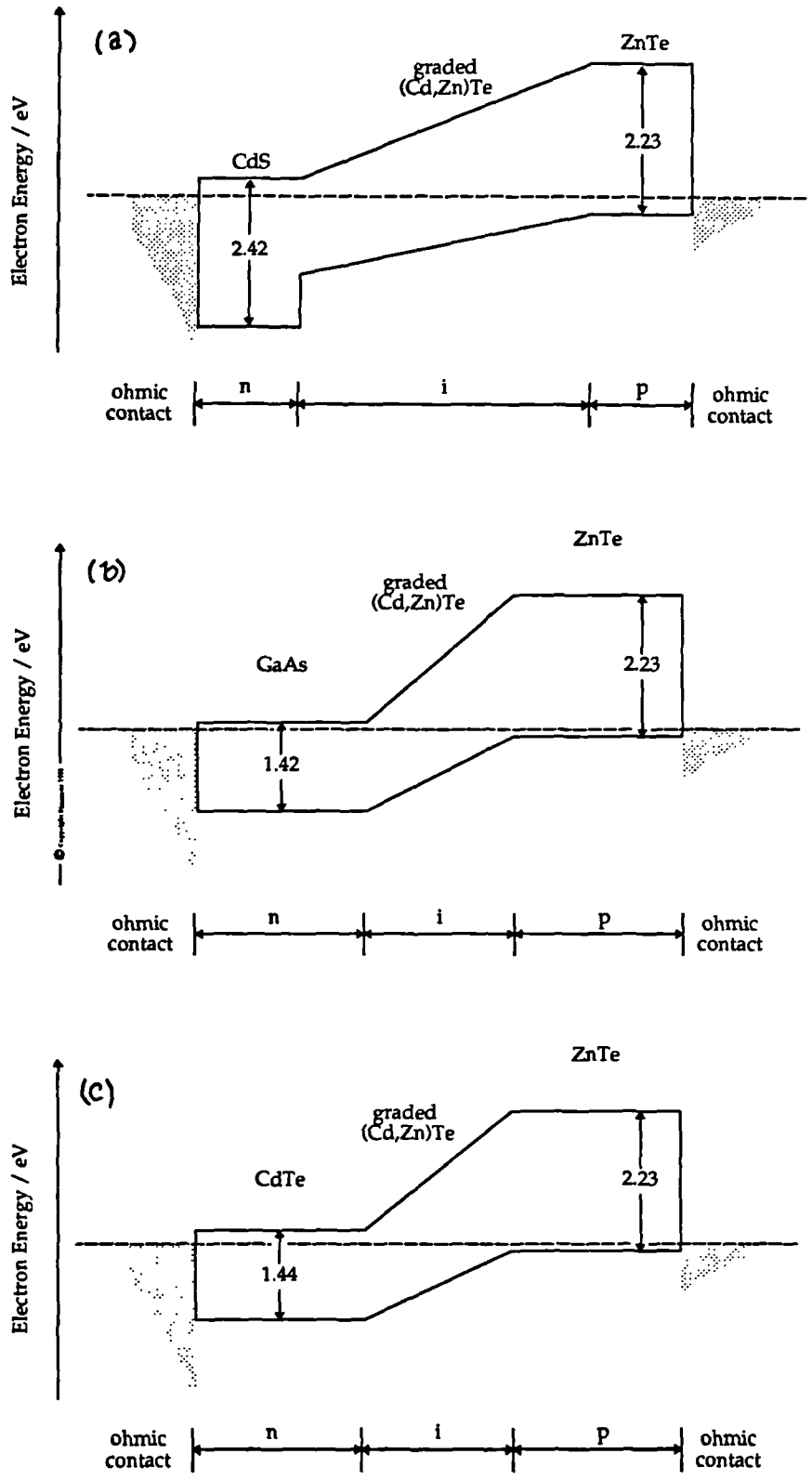

Figure 8.22 — The band structure diagrams for the graded $Cd_{1-x}Zn_xTe$ absorber layers on (a) n-CdS, (b) n-GaAs and (c) n-CdTe substrates respectively

that the p-ZnTe/i-CdTe/n-CdTe has a large value of V_{oc}≈0.51 V and a J_{sc} of 18.97 mAcm^{-2} giving an efficiency of 3.67%. This value is very similar to 3.7% obtained for the n-CdTe/p-ZnTe device described in chapter 7. The addition of the i-layer would therefore seem to have little effect on the device efficiency. The major difference is that the value of V_{oc} has decreased but the value of J_{sc} has increased, effectively cancelling each other out, whilst the fill factor has remained constant. The value of V_{oc} has probably been reduced by the presence of twins within the CdTe epilayer known to be present in the CdTe growth on ($\bar{1}\bar{1}\bar{1}$)B CdTe substrates (see section 5.5.3). The presence of the i-layer creating a greater field for carrier separation led to the increase in J_{sc}. Further improvement in the cell design such as optimising the i-layer thickness and using different orientations of CdTe should lead to higher efficiencies.

Structure	V_{oc}/V	I_{sc}/A	J_{sc}/mAcm^{-2}	ff	η
p-ZnTe/i-CdTe/n-CdTe	0.51	1.49×10^{-4}	19.0	33	3.67
p-ZnTe/i-$Cd_{1-x}Zn_xTe$/n-GaAs	0.56	3.2×10^{-5}	4.1	31	0.81
p-ZnTe/i-$Cd_{1-x}Zn_xTe$/n-CdS	0.47	1.71×10^{-5}	3.88	40	0.83
p-ZnTe/i-$Cd_{1-x}Zn_xTe$/n-CdTe	0.3	3.8×10^{-5}	8.6	48	1.42

Table 8.9 — Summary of preliminary device characteristics of novel solar cell structures

Results for the ternary i-layers seem to indicate an increased value of V_{oc} with reduced values of J_{sc}, and lower efficiencies, except for the p-ZnTe/i-$Cd_{1-x}Zn_xTe$/n-CdTe device. The use of graded i-layers is known to reduce values of V_{oc} since the band gap is increased in the regions of highest recombination, thus generating the photon current in the low band gap regions close to the junction. The p-ZnTe layer was only grown for 300 seconds as opposed to 1800 seconds in the previous device structures and thus the carrier density is much smaller. This could account for the reduced values of J_{sc}. By increasing the thickness of the p-layer, and further investigating the quality of the $Cd_{1-x}Zn_xTe$ layers, and their incorporation into p-i-n structures better device efficiencies should be obtainable.

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Chapter IX

Conclusions and suggestions for further work

The work in this thesis has principally been concerned with the fabrication of CdTe-based solar cells by MOVPE and a broad spectrum of device structures and assessment characterisation has been utilised. Rather than emphasising the optimisation of all procedures necessary for device formation the work forms a gateway for future production of high quality crystalline solar cell structures.

Initial chapters discuss the optimisation of steps in the fabrication procedure, including substrate preparation, thin film growth, doping and formation of ohmic contacts. Subsequent chapters describe the electrical and optical properties of the devices formed. It was found that for epitaxial cells to be produced the substrate surface had to be free from crystalline damage and relatively flat. The best surface for epitaxy using CdS substrates was obtained using a $CrO_3/HNO_3/H_2O$ polishing solution for a variety of orientations [1]. Other polishing solutions were found to be polarity sensitive and at best, only suitable for one particular surface. The finding that best epitaxial growth was only achieved on non-metal close packed $(000\bar{1})$B surfaces of CdS by MOVPE is consistent with observations of CdTe epitaxy on other polar substrates. Layers having good morphology are only obtained on the non metal surfaces of {111}GaAs [2] and CdTe [3]. The lamellar twins present within the {111} oriented CdTe layers grown on the $(000\bar{1})$B CdS substrates are also similar to those grown on GaAs and CdTe [4]. The inferior epitaxial growth on the (0001)A CdS surface is also in accordance with the results of MOVPE growth on {111}A surfaces of CdTe and GaAs [2,3]. The presence of twin islands beneath the polycrystalline surface on A face devices confirmed the nucleation of twin formation at the epilayer/substrate interface rather than as a result of an in-growth defect.

In order to eliminate the twinning effect, which is known to be deleterious to device performance, CdTe was grown on the $\{01\bar{1}6\}$ surfaces of CdS (after Awan

et al [5]). The growth of CdTe on these surfaces was found to be polarity sensitive. CdTe deposition on the $(01\bar{1}6)$A surface yielded polycrystalline films, but epitaxial layers were obtained on the $(01\bar{1}\bar{6})$B surfaces. Whilst epilayers with the best surface morphologies were those grown on $(01\bar{1}\bar{6})$B oriented CdS substrates, TEM analysis confirmed that the epilayers contained lamellar twins, as with the basal oriented CdS [6]. The twins were however inclined at 17° to the epilayer/substrate interface (the angle between the basal and the $\{01\bar{1}6\}$ planes). Growth on different orientations had not therefore eliminated twinning as originally thought, and growth on the prismatic planes would be the obvious next step to this investigation (see appendix D).

Before incorporation of an i-$Cd_{1-x}Zn_xTe$ layer as the absorber material in p-i-n devices, the ternary alloy had to be fabricated. Previous studies had denied the possibility of $Cd_{1-x}Zn_xTe$ formation due to the supposed inherent phase separation between the constituent binaries [7]. Epitaxial layers of $Cd_{1-x}Zn_xTe$ of varying composition have been grown by MOVPE on (100) GaAs substrates at a temperature of 400°C. At temperatures below 380°C, no zinc incorporation into the epilayers was observed and purely CdTe growth occurred. This confirms earlier experience with CdTe/ZnTe superlattices grown in this laboratory where ZnTe formation was seen to be suppressed by CdTe growth. The gas-solid distribution curve was found to bow towards a higher zinc content in the solid phase, in conflict with result obtained by Ahlgren et al [8]. However all epilayers were grown under Te-rich conditions and further investigation into the II:VI ratio would aid future improvements in the quality of these epilayers. Indeed preliminary results of double crystal rocking curve analysis on $Cd_{1-x}Zn_xTe$ grown with a 1:1 II:VI ratio confirmed them to have a rocking curve half width of 511 arc sec. The band gap and lattice parameter were shown to be tunable across the CdTe-ZnTe region and no phase separation was observed. TEM analysis confirmed that the threading dislocation density at the interface was higher than that observed for the corresponding binaries i.e CdTe and ZnTe. This is expected due to the greater driving force for the formation of these defects during cool down from a higher growth temperature of 400°C.

Epitaxial layers of ZnTe were found to be of excellent quality having a rocking curve width of only 370.5 arc sec compared to the best reported so far of 630 arc sec

[9]. The p-type doping of the CdTe and ZnTe using ammonia as a dopant source in the MOVPE reactor proved unsuccessful, possibly due to the formation of deep centres within the forbidden gap. This would account for the high resistivity of the layers obtained. Highly conductive p-type doping in the binaries was achieved down to levels of ≈10 Ωcm (CdTe) and 0.6 Ωcm (ZnTe) using an elemental arsenic dopant source. A stoichiometric excess of the group II element was necessary before successful p-type doping could be achieved, indicating that the incorporation of dopants occurred by substitution of the tellurium by the group V element.

An investigation in to various device structures was completed including :

(i) the n-CdS/p-CdTe single crystal cell
(ii) the n-CdTe/p-ZnTe single crystal cell
(iii) the n-CdS/i-CdTe/p-ZnTe single crystal cell
(iv) the n-GaAs/i-CdTe/p-ZnTe single crystal cell and
(v) the n-CdTe/i-CdTe/p-ZnTe single crystal cell
(vi) preliminary investigations into graded p-i-n structures

In all cases epitaxial structures were obtained and a summary of the important device characteristics presented in table 9.1

Device Structure	η	V_{oc}	J_{sc}	ff	Transport
	%	V	$mAcm^{-2}$	%	
n-CdS/p-CdTe (Cd face)	4.22	0.42	23.0	38	>300 K tunneling
n-CdS/p-CdTe (S face)	1.49	0.52	15.6	16	< 300 K series resistance
n-CdTe/p-ZnTe	3.7	0.61	16.3	32	tunneling<300 K> emission
n-CdS/i-CdTe/p-ZnTe S face (undoped)	<1	0.1	6.3	33	>250 tunneling (high V) emission (low V)
n-CdS/i-CdTe/p-ZnTe S face (doped)	3.2	0.37	24.2	31	emission<250 K <tunneling
n-GaAs/i-CdTe/p-ZnTe	3.5	0.55	20.2	27	tunneling

Table 9.1 — Summary of device parameters

Efficiencies of these devices are low in comparison to similar structures prepared by other techniques. These results constitute a pilot study into the use of MOVPE

for the production of solar cell structures and there remain aspects of the device fabrication that require future development. Structural studies of the thin film CdTe epilayers have confirmed them to be of good crystalline quality but with a high dislocation density at the interface. Attempts to optimise contact formation were limited by the absence of lithographic processing techniques. It is suspected that for such a high quality junction, non-ideal contacts could play a major role in limiting efficiencies. Despite better epitaxial growth on the non-metal surfaces of basal CdS devices, higher efficiencies were consistently obtained from Cd face samples. Reasons for this remain unclear, since both A and B faces were observed by TEM to have contained lamellar twins. The only conclusion to draw is that the dislocation density on the S face devices must be larger than that on the Cd face devices. It is tentatively suggested that devices grown on $\{01\bar{1}6\}$C planes of CdS devices with twins inclined at 17° to the substrate/epilayer interface may have a lower dislocation density, and thus higher efficiency than devices grown on {0001} CdS planes, where twins are parallel to the interface.

The addition of the i-layer to the more conventional n-CdS/p-CdTe heterojunction devices grown on the S face of basal CdS was found to double the efficiency, due in the main to the increase in fill factor. The higher conductivity of the p-type ZnTe compared to the CdTe is thought to account for this difference leading to more efficient carrier collection. V_{oc} values were found to decrease as expected because of the presence of two junction interfaces rather than one in single heterojunction devices, which would increase the defect density in the i-layer. Doping of the ZnTe in p-i-n devices was seen to have a dramatic effect on the value of V_{oc} and J_{sc} illuminating the importance of the carrier concentration available at the junction interface.

Device efficiencies for p-i-n structures fabricated on n-GaAs and n-CdS substrates were similar, the GaAs devices being slightly higher at 3.5% compared with 3.2% [10]. The presence of the conduction band spike at the GaAs/CdTe interface leading to the collection of carriers and higher probability of recombination does not appear to have had great effects on the device performance as would have been expected. Reasonable efficiencies were obtained despite this "handicap" and this is thought to be due to the higher quality GaAs substrate with a higher conductivity than for CdS substrate.

Operation	Suggestion
Substrate preparation	Different orientations of CdS (see appendix D), thinner substrates, different substrates e.g InP, CdTe
Epilayer growth	Alternative dopants, characterisation of epilayers by PL, grading of $Cd_{1-x}Zn_xTe$ epilayers, lower deposition temps
Contact technology	Improved contact methods such as photolithography, grid structures and optimisation of contact behaviour
Development of existing structures	Growth on metal surfaces e.g Cd face, growth on $\{01\bar{1}6\}$ surfaces, changing thickness of i-layer
Novel device structures	Quantum well structures, graded aborbers, tandem cells

Table 9.2 — Suggestions for future work

The work reported in this thesis has clearly demonstrated that the MOVPE growth technique can produce various epitaxial solar cell structures, although it is apparent that optimisation of the various fabrication procedures is necessary for the devices to reach their high potential efficiencies. The future prospects for solar cell development by MOVPE in the II-VI field are numerous. Developments in the growth technology to control important parameters such as dopant concentration and layer thicknesses will lead to improved device performance. The processing of layers after growth also needs serious consideration. Photolithography can lead to device fabrication with resolution as low as 100Å. It is believed that the feasibility of practical growth of a particular structure may well depend on the requirements of what is to be done with the grown layers. The potential of MOVPE to construct novel device structures is great, examples of which are graded absorber layers, tandem and multiquantum well devices. Utilising different substrates and ternary absorber layers will lead to a greater understanding that the various microstructural defect contents in the epilayers have on the device efficiency. A summary of suggestions for future developments in this field is given in table 9.2.

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Appendix A

Calculation of δ_n and δ_p

From device physics the concentration of holes in the valence band of a semiconductor, p_o is given by

$$p_o = N_v \, exp^{-\frac{(E_f - E_v)}{kT}} \tag{1}$$

where E_f is the Fermi level, E_v is the valence band and N_v is the effective density of states in the valence band given by

$$N_v = 2\left(\frac{2\pi m_p^* kT}{h^2}\right)^{\frac{3}{2}} \tag{2}$$

where m_p^* is the effective mass of the holes. Likewise the concentration of electrons in the conduction band is given by

$$n_o = N_c \, exp^{-\frac{(E_c - E_f)}{kT}} \tag{3}$$

where N_c is the effective density of states in the conduction band given by

$$N_v = 2\left(\frac{2\pi m_n^* kT}{h^2}\right)^{\frac{3}{2}} \tag{4}$$

Rearranging equation (1), and assuming that the concentration of holes in the valence band is given by the concentration of acceptors, N_A

$$E_f - E_v = kT \, \ell n \frac{N_v}{N_A} \tag{5}$$

likewise, rearranging equation (3) and assuming that the concentration of electrons in the conduction band is given by the concentration of donors, N_D

$$E_c - E_f = kT \, \ell n \frac{N_c}{N_D} \tag{6}$$

Knowing the values of N_A, N_D, m_n^* and m_p^*, the values of N_c and N_v can be calculated to give the values of δ_n and δ_p. For the n-CdS/p-CdTe junction the value of m_n^* is $0.11 m_e$ † and m_p^* is $0.8\ m_e$ ‡, whilst N_A and N_D were calculated from C-V measurements for our junctions to be 1.3×10^{16} cm^{-3} and 2.1×10^{17} cm^{-3}. The values of δ_n and δ_p were thus calculated to be 0.4 eV and 0.19 eV respectively.

† S.S. Ou et al Solid State Electronics 27(1984)21
‡ S.M. Sze "Semiconductor Physics"

Appendix B

Calculation of the value of R

The current-voltage relationship for tunneling conditions is expressed by

$$I_f = I_o(T)\ exp\ (BT)\ exp\ (AV) \tag{1}$$

and from multistep tunneling

$$I_f\ =\ B\ \psi\ N_t\ exp\ (-\alpha R^{-(\frac{1}{2})}\ (V_d - KV)) \tag{2}$$

Expanding equation (2) gives

$$I_f\ =\ B\ \psi\ N_t\ [exp\ (-\alpha R^{-\frac{1}{2}} V_d) exp\ (-\alpha R^{-\frac{1}{2}} KV)] \tag{3}$$

collecting like terms from equation (1) and (3), gives

$$BT = -\alpha R^{-\frac{1}{2}} V_d \tag{4}$$

$$A = -\alpha R^{-\frac{1}{2}} K \tag{5}$$

Differentiating equation (4) gives

$$B = -\alpha R^{-\frac{1}{2}} \frac{dV_d}{dT} \tag{6}$$

Thus,

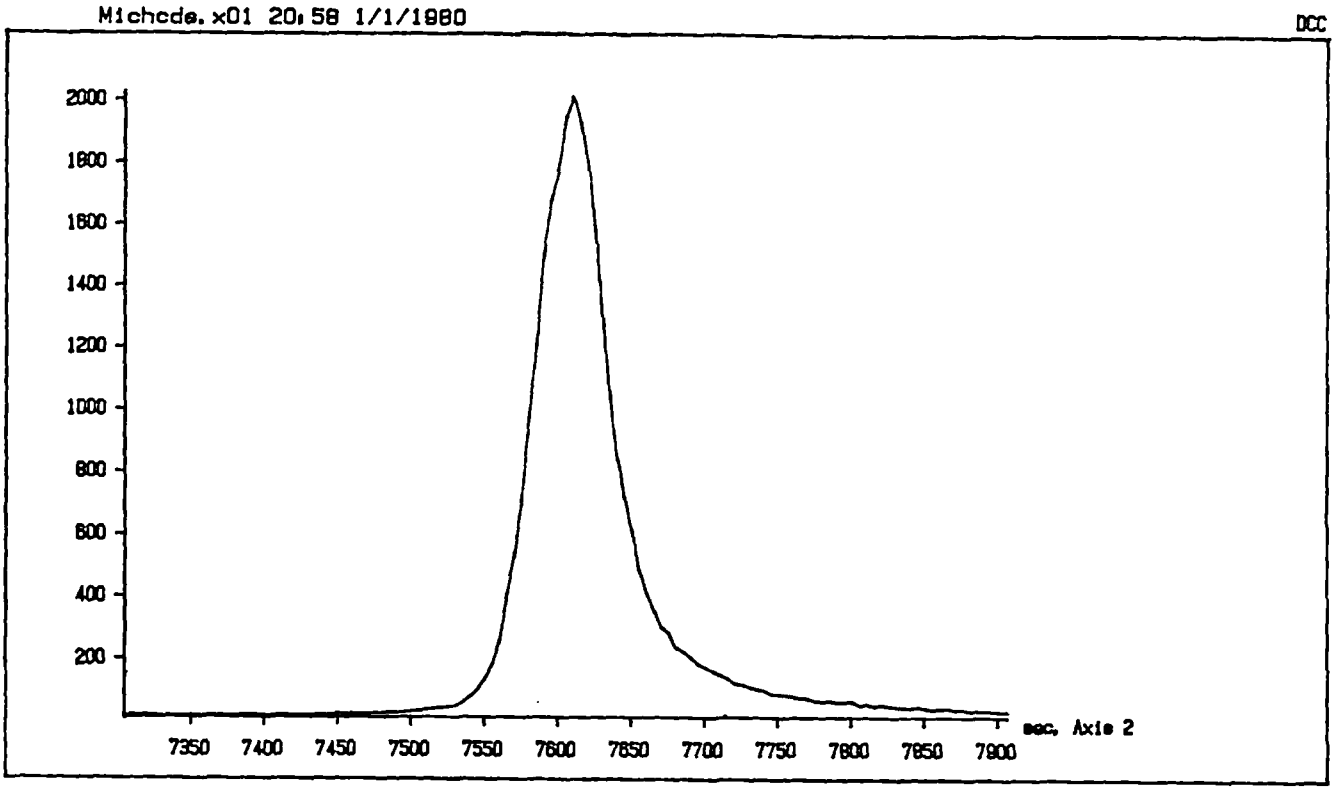
$$R\ =\ \left(\frac{K\alpha}{A}\right)^2 \tag{7}$$

and

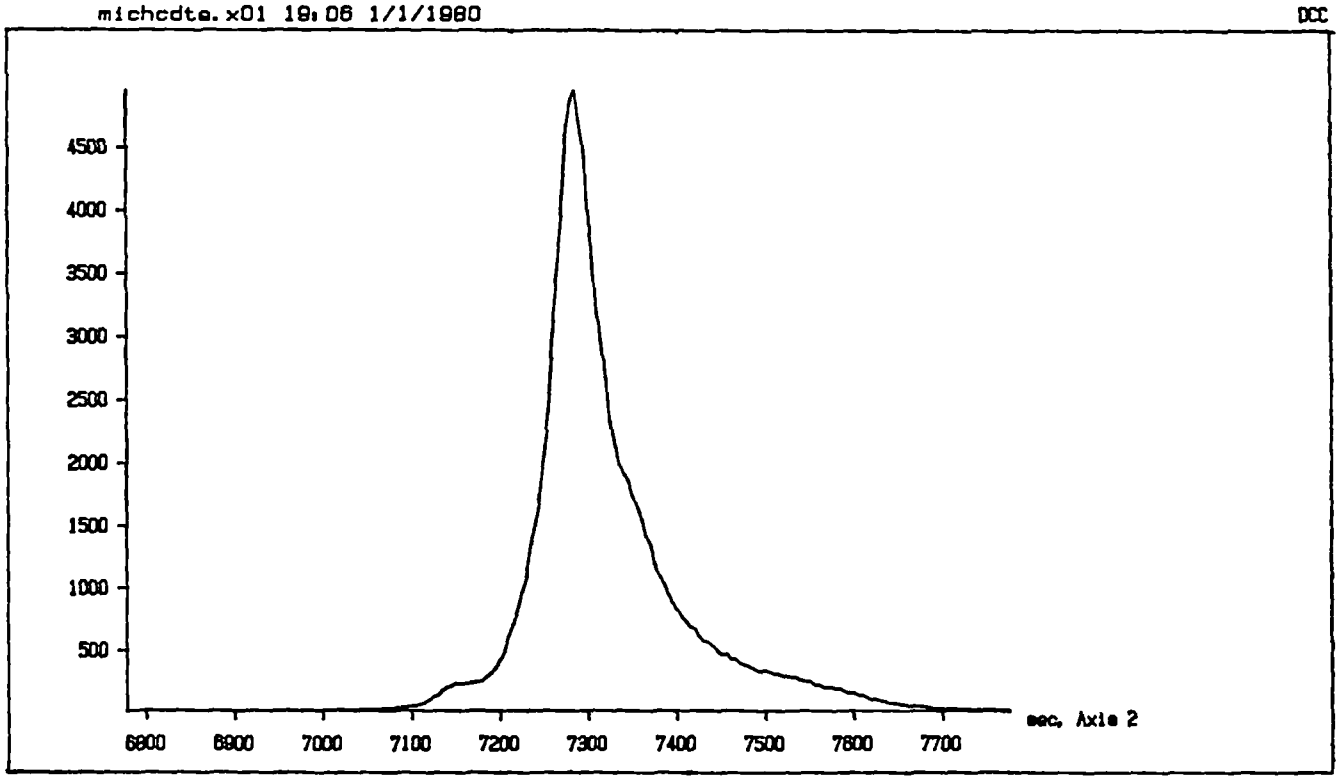
$$B = -\left(\frac{A}{K}\right)\ \frac{dV_d}{dT} \tag{8}$$

Appendix C

Double crystal rocking curve analysis of {0001}CdS and {111}CdTe single crystal substrates



The (002) reflection of a {0001} CdS single crystal substrate giving a FWHM of 55.02 arc sec.

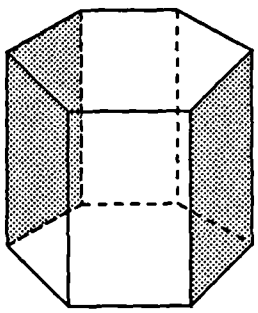


The (111) reflection of a {111} CdTe single crystal substrate giving a FWHM of 66.10 arc sec.

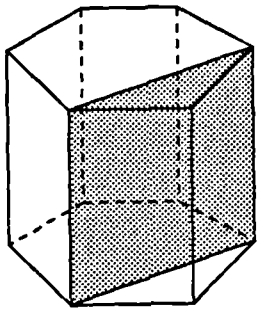
Appendix D

Alternative orientations of CdS

The epitaxial growth of CdTe on {0001} and {01$\bar{1}$6} CdS substrates has led to the formation of twinned CdTe epilayers. The presence of twinning could be eliminated if CdTe was grown on the prismatic planes of CdS, i.e. the {10$\bar{1}$0} and {11$\bar{2}$0} planes (see below).



{10$\bar{1}$0}



{11$\bar{2}$0}